Design of a Low Voltage Active Electric Accumulator with integrated dc-dc converters for control and protection

DESIGN OF A LOW VOLTAGE ACTIVE ELECTRIC ACCUMULATOR WITH INTEGRATED DC-DC CONVERTERS FOR CONTROL AND PROTECTION

BY

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A THESIS

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To my family and loved ones

Abstract

Emerging batteries based on Lithium ion (Li-ion) cells are of significant interest for aerospace, automotive and utility energy storage systems in terms of high energy density, reducing overall weight, volume, and maintenance but suffer from safety concerns such as fire, smoke and toxic emissions. Major issues with these batteries include: a) single point failure, b) complex and costly battery management system (BMS), c) varying output voltage, d) no self-protection, e) costly and ineffective cell balancing, and f) poor energy efficiency.

The main objective of this thesis is to investigate a 'Self-Regulated Low Voltage Active Electric Accumulator (LV-AEA)' as an alternative approach for the design of a Li-ion batteries and compare its benefits and limitations to the existing battery technologies. The analysis and design of LV-AEA for a 7kW Auxiliary Power Unit start application in a starter/generator system of a typical aircraft is presented. Computer simulation results using PSIM have been presented to help understand various working principles of the proposed approach and validate its feasibility. Finally, a small scale technology demonstrator using commercial off the shelf dc-dc converters is tested to verify the presented approach and get experimental results.

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Notation and abbreviations

APU Auxiliary Power Unit

Ah Ampere Hour

BB Building Block

BMS Battery Managememnt System

CCCV Constant Current Constant Voltage

C-rate Charge rate

ESU Energy Storage Unit

ESR Equivalent Series Resistance

Li-ion Lithium ion

$LiCoO_2$ Lithium Cobalt Oxide

$LiFePO_4$ Lithium Iron Phosphate

LMO Lithium Mangaese Oxide

LV-AEA Low Voltage Active Electric Accumulator

MOSFET Metal oxide semiconductor field effect transistor

MPL Magnetic Path Length

MLT Magnetic Length per Turn

Ni-Cd Nickel cadmium

NiMH Nickel metal hydride

NBPT No Break Power Transfer

PI Proportional Integral

PWM Pulse Width Modulation

SEI Solid Electrolyte Interface

S/GS Starter Generator System

SLA Sealed Lead Acid

SOC State of Charge

SOH State of Health

TRU Transformer Rectifier Unit

ZVS Zero Voltage Switching

Notations

A_p Area product of magnetic core

A_e Effective cross-sectional area of magnetic core

A_{bw} Bare wire area of the magnetic wire

B Maximum flux density

C_{cl} Clamp capacitor

C_o Output capacitor

C_{ob} Output bus capacitor

C_{in} Input filter capacitor

D Duty Cycle of the converter

D_{sw} Duty cycle of each switch

E Energy

f_{sw} Switching frequency

f_r Ripple current frequency

I_{in} Input current

ΔI_{in} Input current ripple

I_o Output Current

I_{L1} Average current in inductor L_1

I_{L2} Average current in inductor L_2

Δi_{L1} Change in current of inductor L_1

Δi_{L2} Change in current of inductor L_2

I_L Average current in each inductor

I_Lpk Peak current in each inductor

I_{Lmax} Peak current of each inductor

I_{Lp} Average current in parallel connected inductor

ΔI_{Lmax} Change in peak inductor current

I_{Lrms} Rms value of current in each inductor

I_{dpk} Peak current of each diode

I_{drms} Rms current of each diode

I_{dav} Average current in each diode

J Current density

K_u Utilization factor for the winding wire.

L_1 Inductance value for first input Inductor

L_2 Inductance value for second input Inductor

L Common inductance value for input inductors

L_p Inductance value of parallel connected inductors

L_{lk} Leakage inductance of transformer

I_{Lpmax} Maximum average current in each parallel connected inductor

L_{in} Input filter inductor

I(S1) Current in switch S_1

I(S11) Current in clamp switch S_{11}

I(S2) Current in switch S_2

I(S22) Current in clamp switch S_{22}

I_{pri} Rms value of primary side current of transformer

I_{sec} Rms value of secondary side current of transformer

I_{secpk} Peak value of secondary side current of transformer

I(Ccl) Current in clamp capacitor

I_{Srms} Rms current in main switches

I_{Scond} Conduction loss in main switches

I_{Ssw} Switching loss in main switches

I_{pri} Primary side rms current of transformer

I_{sec} Secondary side rms current of transformer

I_{ob1} Output current of block 1

I_{ob2} Output current of block 2

n Transformer turn's ratio

η Effeciency of the converter

N Number of building blocks

N_t Number of turns in inductor

N_p Number of primary turns of transformer

N_s Number of secondary turns of transformer

P_o Output power

P_{ob} Output power of each building block

P_{cu} Copper loss

P_{pcu} Primary side copper loss of transformer

P_{scu} Secondary side copper loss of transformer

P_{core} Core loss

R_{dcr} Series resistance of inductor

R_{esr} Equivalent series resistance in output capacitor

R_o Load Resistance

R_w Resistance of magnetic wire used in inductor and transformer

S_n Number of strands of magnetic wire used in inductor

S_{np} Number of strands of magnetic wire used on primary side of transformer

S_{ns} Number of strands of magnetic wire used on secondary side of transformer

S_1 First main switch of the converter

S_{11} Clamp/auxiliary switch for S_1

S_2 Second main switch of the converter

S_{11} Clamp/auxiliary switch for switch S_2

T Time period of switching cycle

V_{in} Input voltage

V_{cl} Clamp capacitor voltage

VgS1 Gating Signal of switch S_1

VgS11 Gating Signal of clamp switch S_{11}

VgS2 Gating Signal of switch S_2

VgS22 Gating Signal of clamp switch S_22

VdS1 Drain to source voltage of switch S_1

VdS11 Drain to source voltage of clamp switch S_{11}

VdS2 Drain to source voltage of switch S_2

VdS22 Drain to source voltage of clamp switch S_22

V_f Forward voltage of diode

V_{lk} Voltage across leakage inductance

$V(RL1)$ Voltage across current sensing resistor of L_1

$V(RL2)$ Voltage across current sensing resistor of L_2

V_{sec} Secondary side voltage of transformer

V_o Output Voltage

ΔV_o Change in output voltage

V_{pri} Primary side voltage of transformer

W_a Effective window area factor

W_{tfe} Magnetic core weight

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Chapter 1

Introduction

During the last few years, lithium ion (Li-ion) batteries have emerged as the rechargeable battery of choice and their use is of significant interest for aerospace, automotive, and utility energy storage systems. But, there have been safety and certification issues, which have prevented their widespread use in these applications. The main objective of this thesis is to focus on the description, analysis, and design of a 'Self-Regulated Low Voltage Active Electric Accumulator (LV-AEA)' as an alternative approach for the design of Li-ion batteries which makes them more fault tolerant by introducing control and protection distributed at the cell/module level and capable of much higher charge/discharge rate through introduced dc-dc converters [1].

Work on the development of Li-ion batteries began in 1980's and they were first introduced by Sony in 1991[2]. Replacing other rechargeable/secondary batteries such as sealed lead acid (SLA), nickel metal hydride (NiMH), and nickel cadmium (Ni-Cd) batteries with Li-ion enrgy storage systems provides significant benefits including high energy density, low self discharge rate, weight and volume savings, no memory

effect and reduced maintenance. Several Li-ion battery solutions, which initially seemed promising, were adopted by various aircraft manufacturers for use in aviation applications but later were abandoned due to major safety concerns including fire, smoke and toxic emissions. The Cessna 525C Citation CJ4 received certification to use Li-ion batteries in 2011. Subsequently, the Federal Aviation Administration (FAA) cancelled this after a fire broke-out on ground while charging a main Li-ion battery [3] mandating Cessna to replace it with Ni-Cd or SLA batteries. Recently, Boeing 787 Dreamliner employing Li-ion battery were grounded after several alarming incidents occurred within days which involved a fire break-out on ground in Boston, and another one generating warnings and burning smell forcing the pilots to make an emergency landing in Japan [4]. As a result of these safety issues and FAA rulings, major aircraft manufacturers have retreated from their plans to use Li-ion batteries and rather reverted to traditional battery solutions, which were proven safe but would be more costly to fly. Over the past decade or so automotive has had its own share of Li-ion battery incidents and mishaps, which has resulted in costly recalls. For instance, Chevrolet Volt employing Li-ion battery caught fire due to leakage of the liquid coolant of the battery after a crash test was conducted on it by NHTSA as reported in [5].

1.1 Motivation

A conventional battery is made up of multiple individual cells in series to get the desired rated voltage and several such strings in parallel to meet required battery capacity. There is no isolation at the cell/module level which leads to single point failures and lack of self-protection from internal/external faults requires use of auxiliary disconnect circuits for the protection of the battery. Furthermore, the output voltage varies widely depending on the state-of-charge (SOC), loading and environmental conditions. Complex and costly battery management systems (BMS) are often used to ensure safe and reliable operation of these batteries. One of the main functions of the BMS is to monitor cell voltages, current, and temperature to protect the battery against failure modes such as overcharge, over-discharge, and low/high temperature operation. The cell voltage measurement is a huge challenge as every indvidual series connected cell in a battery needs to be monitored separately. This is due to the fact that even cells having same chemistry can exhibit varied characteristics and voltage level of the cells can vary from one cell to the other. Taking the measurement of the terminal voltage of the battery does not guarantee reliable measurement and can lead to over-charging or over-discharging of the cells. Therefore, a large protection as well as measurement circuitry is required for the monitoring purposes in BMS which makes it complex in nature. Also, the BMS needs to establish charge equalization among all the cells and oversee proper charge and discharge of the battery. For charge equalization, cell-balancing methods such as passive cell balancing and active cell balancing need to be used so that the voltage in the cells remain at the same level. The use of passive cell balancing leads to alot of heat dissipation resulting in poor effeciency and thermal management burden whereas active cell balancing is costly and increases the

amount of power electronics used in the battery.

LV-AEA is a step forward in addressing these issues. The proposed accumulator is motivated by a United States Patent [1] which introduces a novel approach of partitioning the energy storage system into multiple building blocks/modules working in parallel such that each building block can be controlled and operated independently. Each building block consists of Li-ion cells connected in parallel to get the rated capacity and the rated voltage is obtained by boosting the voltage of a single cell or few cells connected in series through a dc-dc converter. The real time closed loop voltage control provides regulated output voltage and equal load sharing is achieved through a centralized controller. Such an accumulator not only reduces the number of series connected cells in a battery and makes it more fault tolerant but also eliminates the need for complex BMS and cell balancing.

1.2 Problem Statement

In order to ensure safe operation of Li-ion batteries, recent mandated Li-ion standards [6] require such batteries to be operated only at safe temperature, pressure, and accurate state of charge to avoid conditions such as thermal runaway, electrolyte leakage, and explosion of the battery. The batteries need to be charged and discharged at a controlled rate within electrical, thermal and structural limitations at the cell, module and battery pack level. Accurate and fairly fast acting sensing and protection systems are required in order to immediately isolate the battery from sources of energy to prevent known destructive failure modes such as over-charge, over-discharge, temperature surge, and low temperature operation. Even though Li-ion cells have

fairly high charge/discharge capability, it is difficult to take advantage of this feature due to the multiple cells in series. It is difficult to avoid damaging/stressing the Li-ion battery while conducting some of the tests mandated by FAA [6]. To meet the safety requirements of these batteries and to ensure high charge/discharge rate, there is need to introduce advanced charge/discharge power electronics to:

1. Tightly monitor and control safe flow of energy in and out of the battery, and
2. Enable the much higher C-rate of Li-ion batteries without having to de-rate the cells for peak-power demand and quick charge capability.

1.2.1 Solution

The LV-AEA discussed in this thesis makes isolation possible at the block level because of the partitioning of the whole system into parallel connected blocks such that even if one block fails, the other blocks can still continue their operation. Also, the dc-dc converter in each building block provides ability to interrupt the current flow by turning the PWM pattern off; thereby allowing a quick protection (within a few micro seconds). The use of advanced dc-dc converter that is dual inductor current fed push pull converter [7–10] makes the accumulator capable of high charge/discharge rate and the real time closed loop controls of the converter aid controlled charge/discharge from the battery on top of providing a regulated output voltage and equal load sharing.

1.3 Thesis Contribution

1.3.1 New Starter/Generator System in an Aircraft with Low Voltage Active Electric Accumulator(LV-AEA)

Fig. 1.1 shows a top-level functional block diagram for a typical aerospace starter/generator system (S/GS). For simplicity, redundant AC and DC buses are not shown and corresponding modes of operation are not discussed. In a traditional starter/generator system of an aircraft, a nominal 24V battery with a dedicated charger is used to provide: a) emergency/back-up power supply for 28V loads, and b) Auxiliary Power Unit (APU) start. There are three main modes of operation for the battery. In Mode 1, when switch S1 is closed, the battery voltage is boosted to 270 VDC through the unidirectional DC-DC converter. Then, energy is conditioned from this high voltage DC bus through a Start Converter Unit and used to start the APU engine. In Mode 2, switch S2 is closed (S1 remains open through an automatic interlock mechanism) and energy flows in the reverse direction back to the 28V loads though a Transformer Rectifier Unit (TRU). In Mode 3, AC power may be used to charge the battery. Nominal voltage for the battery is 24 VDC. This allows diode-or of the outputs of the TRU and battery to achieve an essential bus (not shown). Due to its higher rectified voltage, power will be first taken from the TRU and if not available from the battery.

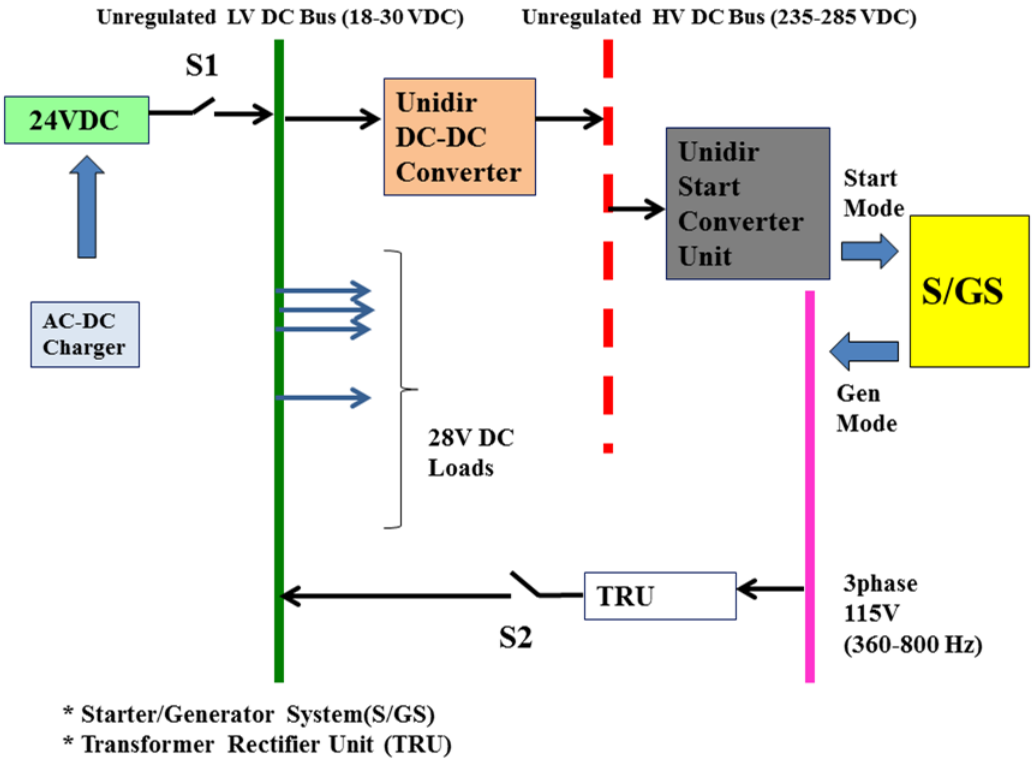


Figure 1.1: Simplified electric power architecture for a Starter/Generator System (S/GS)

Fig. 1.2 shows a new architecture for the S/GS in which the traditional battery charge/discharge system is replaced with a Li-ion LV-AEA. The proposed solution is a step forward in addressing the current limitations and failure modes of Li-ion batteries and provides other significant benefits. First it provides regulated DC bus at much higher voltage that is advantageous in reducing load currents. In a traditional architecture, the battery voltage could be as low as 18V. A battery having regulated output voltage at much higher voltage of 28VDC could reduce the load currents by over 36% and this would result in: a) significant reduction in weight and cost of lengthy high current cables, b) higher efficiency, c) cost-effective, fail-safe and

fast power flow control and protection at cell level, and d) ease of trouble-shooting and maintenance. This further results in reduced life cycle cost, overall weight and improved reliability. This type of system allows to further optimize the architecture; for example, in a dual battery aircraft the main and auxiliary batteries can be tied together facilitating a fault-tolerant common bus capable of No Break Power Transfer (NBPT).

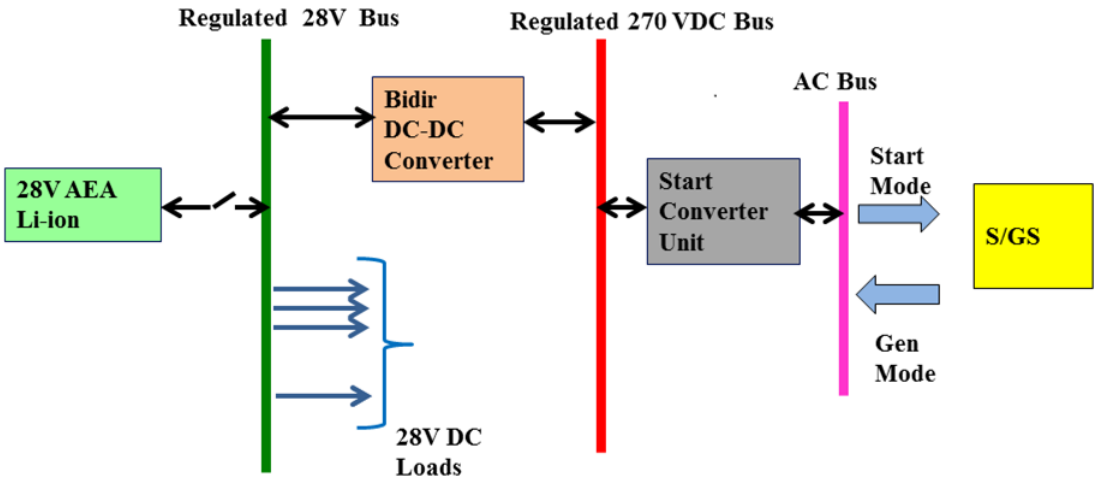


Figure 1.2: New proposed architecture for the S/GS in which the traditional battery charge/discharge system is replaced with a LV-AEA

1.4 Organization of the Thesis

This thesis is organized into five chapters. Chapter 2 provides the detailed description of the LV-AEA. The various components of the accumulator and their functioning will be discussed in detail. The steady state analysis of the dc-dc converter required for the design of each building block are also presented. Chapter 3 presents the design application for LV-AEA and each component design will be presented and

the corresponding simulation results would be documented. Chapter 4 will show the experimental results of the small scale technology demonstrator using commercially available dc-dc converters as a proof of concept. Chapter 5 will include the drawn conclusions from the test results using simulation and experimental set up and the scope for future work will also be discussed. Appendix A and Appendix B will include the simulation circuits for the experimental test set-ups used.

Chapter 2

Low Voltage Active Electric Accumulator(LV-AEA)

This chapter provides a general description of the various components used in LV-AEA, and their basic working principle. Fig. 2.1 represents the block diagram of LV-AEA which consists of the following components:

1. Energy Storage Unit (ESU)
2. DC-DC converter
3. Building Block (BB) controller
4. AEA controller

The accumulator is realized as a unit consisting of various building blocks where each block consists of an ESU with number of cells connected in parallel along with a dc-dc converter and a building block (BB) controller. The AEA master controller co-ordinates with the BB controller of each block to provide regulated output voltage,

load sharing, and protection for the whole unit. An inter-phase inductor is used as an output filter for each building block to facilitate proper load sharing amongst the multiple building blocks.

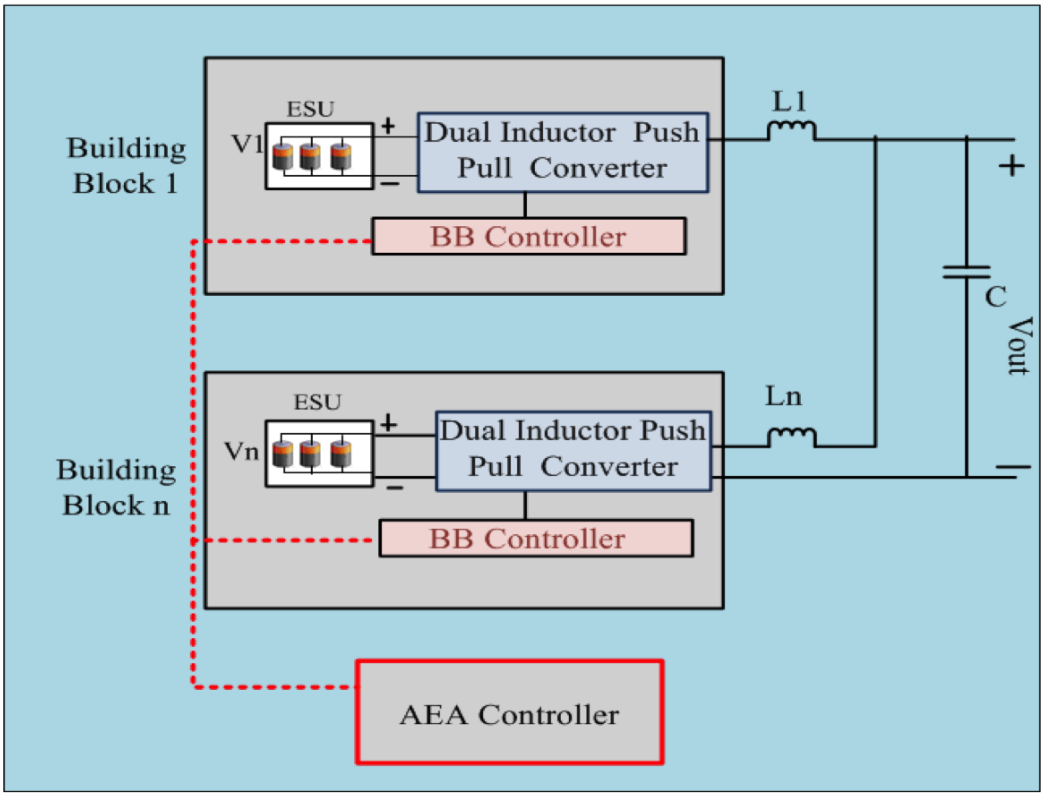


Figure 2.1: Block diagram of the proposed Li-ion active electric accumulator [1]

2.1 Energy Storage Unit (ESU)

The ESU of LV-AEA is formed by using a single Li-ion cell for series connection and a number of cells connected in parallel. Depending upon the application, more series connected cells can be considered to get the required output voltage but that will introduce the need to assess the requirement of cell balancing and measurement circuitry in the system.

Li-ion has been considered as a suitable candidate for use in ESU because of the various advantages that it has to offer. A Li-ion cell has high energy density and comes in various chemistries to choose from based upon the power/energy requirements. Also, in comparison to the other traditional batteries, certain Li-ion battery chemistries are capable of delivering much higher C-rate at the cell-level which is desirable for the operation of LV-AEA. Longer life cycle, lower self-discharge rate, low maintenance costs, and the absence of memory effect are another great advantages that this battery chemistry offers. Section 2.1.1 gives the basic description of the Li-ion cell and Section 2.1.2 explains its principle of operation.The various failure modes in Li-ion cell are discussed in Section 2.1.3 and the use of LV-AEA in mitigating them is also presented.

2.1.1 Li-ion cell description

In this section, the construction of the Li-ion cell has been explained [11],[12]. In a Li-ion cell, the two electrodes namely anode (negative electrode) and cathode (positive electrode), and an electrolyte (known as the conducting material) are the main components. The cathode can be chosen from various lithium metal oxides such as

lithium cobalt oxide($LiCoO_2$), lithium iron phosphate($LiFePO_4$), and lithium manganese oxide(LMO). The selection of the cathode is based on the requirement and the advantages that the different cathode materials have to offer. The anode is made out of carbon, most common being the graphite. The electrolyte is a non-aqueous organic solvent with lithium salt dissolved in it. The separator, which is a polymer film, provides the isolation between anode and cathode while admitting the Li-ions to traverse. The anode has a tendency to react with the electrolyte; therefore a Solid Electrolyte Interface (SEI) is formed when the cell is charged for the first time. This layer acts as a barrier between the anode and electrolyte but it allows the lithium ions of cathode to pass through.

2.1.2 Working principle

Li-ion cell being secondary can be charged and discharged repeatedly for its reuse. Constant current constant voltage (CCCV) method [13] is used for its charging.The cell is charged with a constant current till it reaches its final voltage using a set charge rate. The final voltage is then kept at a constant value using constant voltage method during which the current decreases until it reaches its minimum cut off value, which marks the completion of charging cycle. During charging, some of the lithium ions flow towards the anode and are intercalated [11] into it. This leads to the flow of equivalent electrons from the cathode to anode through the outer circuit. During discharging, the contrary of charging process occurs, when the lithium ions move from anode to cathode and electrons flow from anode to cathode causing a discharge. The Li-ion cell is discharged using a constant current until its reaches minimum cut off voltage. Fig. 2.2 and Fig. 2.3 represent Li-ion cell operation during charge and

discharge respectively.

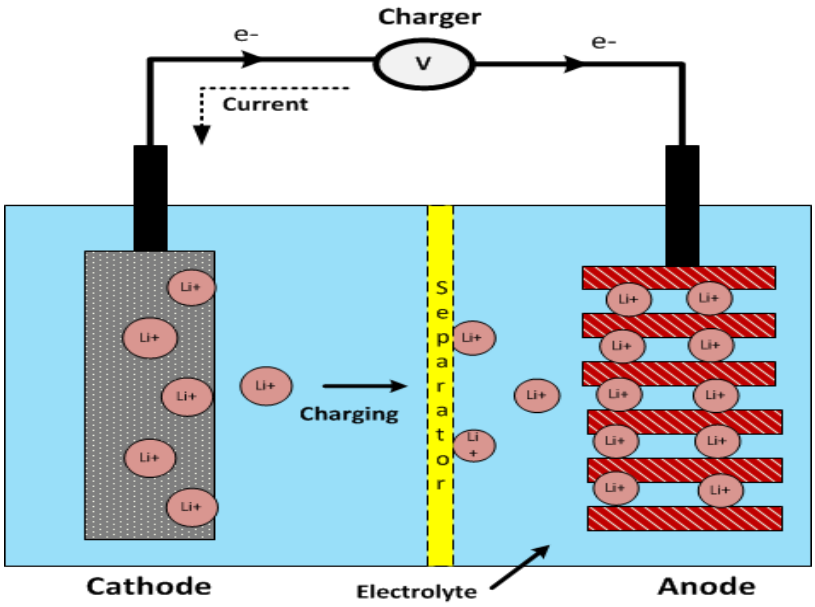


Figure 2.2: Li-on cell charging [14]

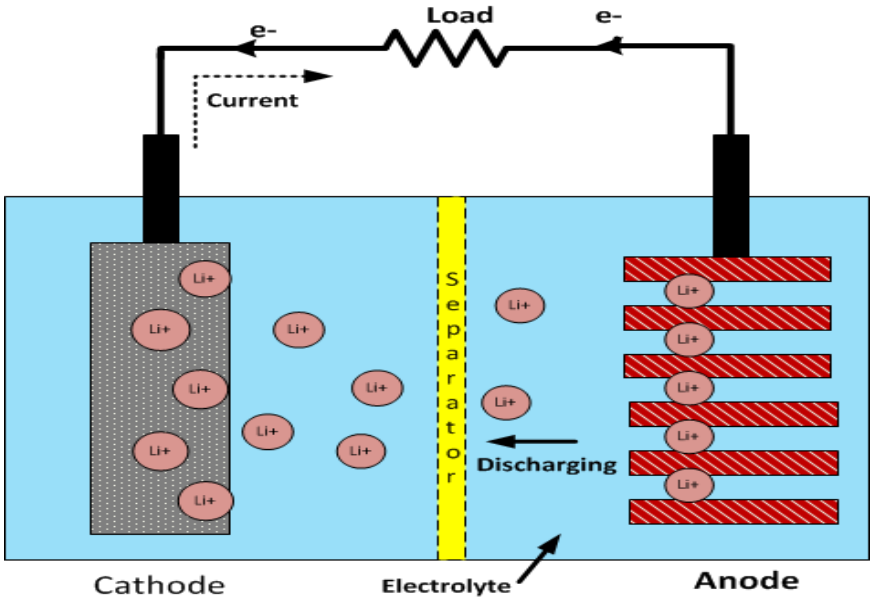


Figure 2.3: Li-ion cell discharging[14]

2.1.3 Failure modes in Li-ion cells

The safe operation of a Li-ion cell is determined by the operating conditions outlined in the datasheet of the cell. If any of the parameters go beyond their limit, it can result in the failure of a cell and eventually of the whole system. The operating conditions, which can lead to cell failure, and their effects, are listed in the Table 2.4. Besides the mechanical fault conditions, operating conditions leading to various failure modes [12],[15] are discussed below:

1. **Electrical conditions**

   Overcharge: If a Li-ion cell is charged beyond the maximum specified cell voltage, it leads to a high level of charge current and a condition known as lithium plating persists. Instead of being infused into the receiving electrode i.e. anode, deposition of lithium ions in the form of metal takes place on the surface of anode. If the charging process in continued, the cathode will fall short of conducting Li^+ ions and hence will result in capacity loss. Furthermore, short circuit between the electrodes can occur due to the continuous dendritic growth of metallic Li-ions ultimately resulting in an increased cell temperature. If not stopped, this can lead to a thermal runaway.

   Over-discharge: Allowing a Li-ion cell to discharge below the minimum cut off voltage is also not a safe practice. If the cell is over-discharged, copper from anode gets dissolved in the electrolyte and can be accumulated as metal anywhere in the cell during the next charge. This can lead to a potential short circuit particularly in the SEI of the cell.

2. **Thermal conditions**: The safe operation of a Li-ion cell is highly temperature dependent and its nominal temperature range should be maintained when operating or during its storage. The temperature of the cell lower than the operating temperature slows the rate at which Li^+ ions are absorbed or discharged from the electrodes during charging or discharging which results in capacity loss and lithium plating in some cases. High temperature operation as a result of increased reaction rate can cause high currents levels. Higher currents will lead to more power dissipation, thereby alleviating the temperatures even further.

   Thermal runaway All the failure modes discussed above can trigger a chain of reactions as a consequence of which more temperature rise occurs within the cell. This effect is known as thermal runaway. First of all, the Solid Electrolyte Interface (SEI) breaks down and accounts for high temperatures that cause electrolyte breakdown and release of flammable gases. Then melting of the separator film occurs as result of which short circuit between the two electrodes happens. The temperature rises even more and causes breakdown of the cathode as a consequence of which oxygen is released. If the flammable gases are not vented out,they can react with the oxygen released and cause explosion of the battery.

Operating Condition		Failure Mode	Cause of Failure
Cell voltage Temperature	High High	Thermal Runaway	SEI Layer Breakdown ↓ Release of flammable gases due to electrolyte breakdown ↓ Melting of separator film ↓ Breakdown of cathode
Cell Voltage Temperature	High Nominal	Capacity Loss	Lithium Plating at anode
Cell Voltage Temperature	Nominal Nominal	SAFE	OPERATION
Cell Voltage Temperature	Low Nominal	Short Circuit	Copper dissolved in electrolyte ↓ Deposition of metallic copper occurs during next charge.
Cell Voltage Temperature	Low Low	Capacity Loss Short Circuit	Slow reaction rate ↓ Lithium plating

Figure 2.4: Lithium ion cell failure modes [15]

2.1.4 Role of LV-AEA in avoiding failure modes:

In a traditional battery, there are a number of cells connected in series and if one cell goes bad, it leads to the whole battery failure. In LV-AEA , there is no series connection of cells which avoids propagation of the failure to the adjacent cells. Furthermore, LV-AEA uses a building block (BB) controller to measure cell voltage, current, and temperature with the help of measurement sensors. If any of the parameters are out of the safety limits, the BB controller shuts down that building block with the help of PWM signals for the switches of the dc-dc converter. The failed block is then isolated from the other blocks and the rest of the building blocks continue their operation with the help of AEA controller which re-distributes the load requirements to the building blocks to provide the required output power. The working of the control and protective functions is described more in Section 2.3 and Section 2.4.

2.2 DC-DC converter

In a coventional battery, number of cells are connected in series to get the desired voltage but in LV-AEA single cell voltage is stepped up to a higher voltage level using the dc-dc converter. Therefore, for the selection of the dc-dc converter to be used in LV-AEA, we need to look at the converters that offer boost operation. For this converters such as boost, flyback, and push pull can be considered. Besides these topologies, there are advanced topologies derived from these conventional topologies that offer additional benefits such as reduced ripple and higher effeciency. Such topologies are Current fed isolated full bridge converter with an active clamp [16, 17], Half bridge converter[18], Current fed dual bridge converter [19], Single inductor

current fed push pull converter[20], and Current fed dual inductor push pull converter [7–10].

Current fed isolated full bridge converters are considered useful due to their reduced source current ripple; but there are certain factors that limit their use. Due to the hard switching of this type of converter, range of switching frequency is limited. Also, high voltage transients can be seen during the turn off stage of the switches which account for more switching losses in the converter. To avoid voltage stress conditions and to achieve soft switching, the use of active clamp in an isolated current fed isolated full bridge converter has been discussed in [16, 17] but the clamping circuit adds to more switching losses and the switching operation of the converter gets directly affected by the load conditions. A half bridge dc-dc converter employing zero voltage switching [18] involves less use of components than the full bridge converter and eliminates the need for clamp circuit. But this converter increases the voltage stress across switches as the switch voltage is double than the source voltage [18]. Another converter known as the current fed dual bridge converter has been proposed in [19]. It takes advantage of functionalities of both current fed full bridge converter and the current fed half bridge converter.But large number of components and their corresponding snubber circuits makes it not very suitable for the design of LV-AEA.

2.2.1 Selected topology

The selected topology for the design of low voltage active accumulator is a current fed dual inductor push pull converter [7–10]. This converter is similar to the single inductor current fed push pull converter given in [20]. But it has two inductors at the input as compared with single inductor in the single inductor current fed push pull

converter and an active clamping circuit to reduce the voltage stress across switches. This type of converter is suitable for our proposed accumulator as it can be used in low voltage and high power applications where the current stress is considerably high. Fig. 2.5 shows a dual inductor current fed push pull converter [7–10] . The dual inductor current fed push pull converter allows two stages of boost operation with the help of the two input inductors and an isolating transformer. The transformer isolates the input side from the output side of the converter; therefore it acts as an additional protection in LV-AEA for mitigating a failure mode if it occurs. The overall operation of the DC-DC converter depends on the on and off state of the main (S_1 and S_2) and auxiliary switches (S_{11} and S_{22}). The switching signals for the main switches are overlapped and the auxiliary switch signals are complementary to their respective main switches. Each inductor stores energy when the corresponding main switch closes (S_1, S_2), and its energy is released to the primary winding of the transformer when the main switch is opened. Finally, the primary side voltage is further stepped-up by the transformer's turns ratio and rectified/filtered in the output stage. The auxiliary switches (S_{11} and (S_{22}) and a clamped capacitor C_{cl} help in reducing the voltage transients across the switches and also enable zero voltage switching (ZVS).

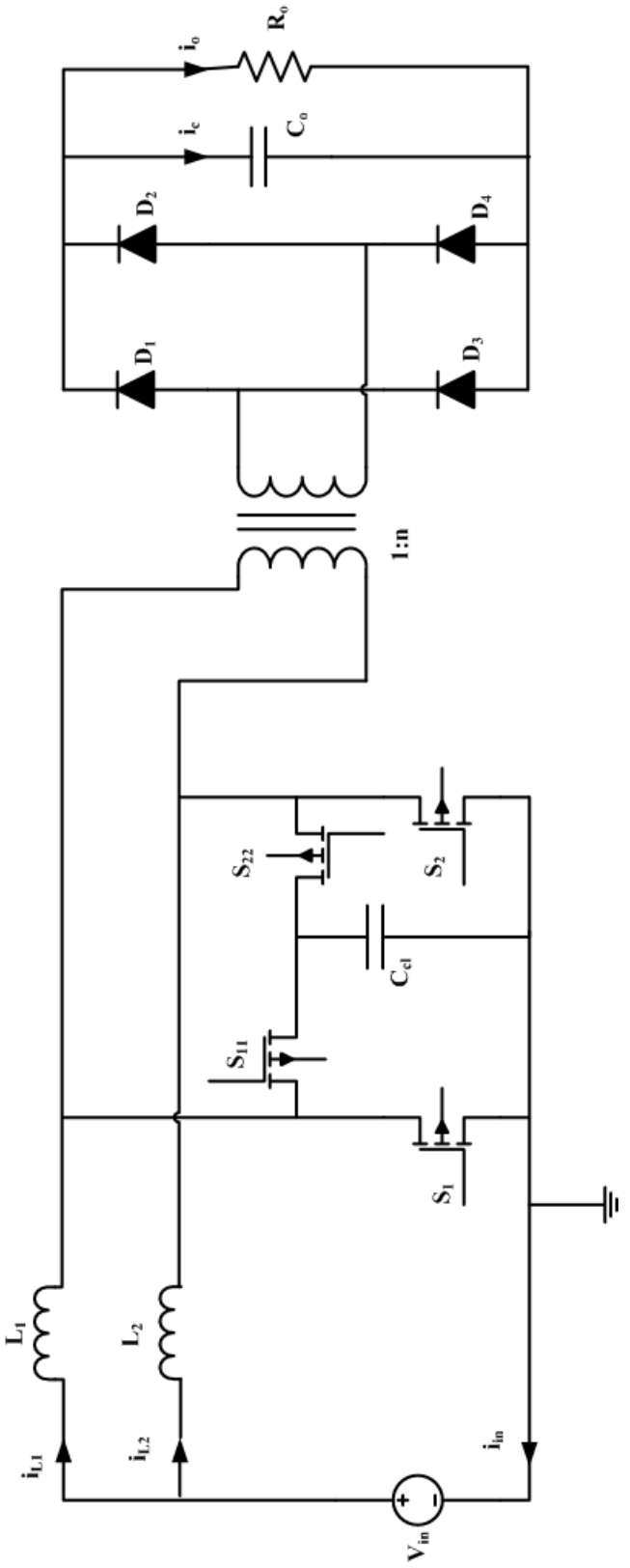


Figure 2.5: Dual inductor current fed push pull converter[7–10]

2.2.2 Steady state analysis of the Current Fed Dual Inductor Push Pull Converter

This section presents the steady state analysis of the dc-dc converter used in LV-AEA which are important for its design and control. For the simplification of the analysis, following assumptions have been made:

1. The input voltage source is considered as ideal.
2. The switches used are ideal switches.
3. The inductor current remains continuous.
4. The transformer behaves as an ideal transformer with no losses and no leakage inductance.
5. The voltage of the clamped capacitor remains constant such that the operation of the clamp circuit can be neglected.
6. The output capacitor losses are neglected and it is assumed that the output voltage remains constant.

The overall operation of the dual inductor current fed push pull converter can be explained by the on and off state of the main switches (S_1 and S_2). The various modes of operation are discussed below:

1. **Mode 1 (t_0-t_1):** At this time, both the main switches S_1 and S_2 are ON. The inductor current starts rising in both the inductors (L_1 and L_2) and is phase shifted by 180° with respect to each other. During this phase, the inductors

store the energy and no voltage appears across the primary winding of the transformer. Hence, no energy is transferred to the secondary side of the transformer. Therefore, the output capacitor supplies the required energy to the load.

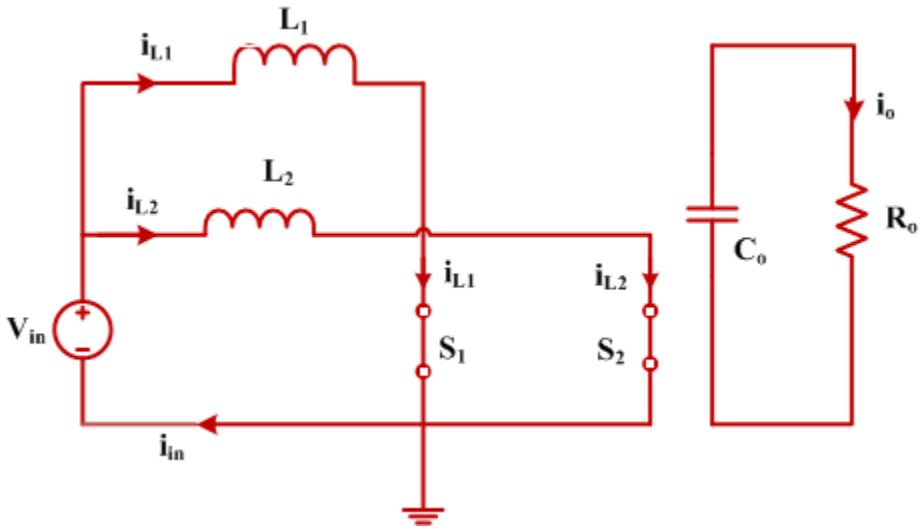


Figure 2.6: Mode1(t_0-t_1)

$$V_{in} = L_1 \left(\frac{di_{L1}}{dt} \right) \tag{2.1}$$

$$V_{in} = L_2 \left(\frac{di_{L2}}{dt} \right) \tag{2.2}$$

$$C_o \times \left(\frac{dV_o}{dt} \right) = -\frac{V_o}{R_o} \tag{2.3}$$

The above equations can be written as:

$$\Delta i_{L1} = \frac{V_{in}}{L_1} \times \frac{DT}{2} \tag{2.4}$$

$$\Delta i_{L2} = \frac{V_{in}}{L_2} \times \frac{DT}{2} \tag{2.5}$$

$$\Delta V_o = -\frac{V_o}{R_o \times C_o} \times \frac{DT}{2} \tag{2.6}$$

2. **Mode 2(t_1-t_2):** The main switch S_1 opens and the inductor current I_{L1} starts decreasing linearly while the main switch S_2 remains closed and current in I_{L2} keeps on increasing. The energy from inductor L_1 is then released to the primary side of the transformer and the voltage is further stepped up according to the turns ratio of the transformer. After rectification through diodes D_1 and D_4, the energy is fed to the load.

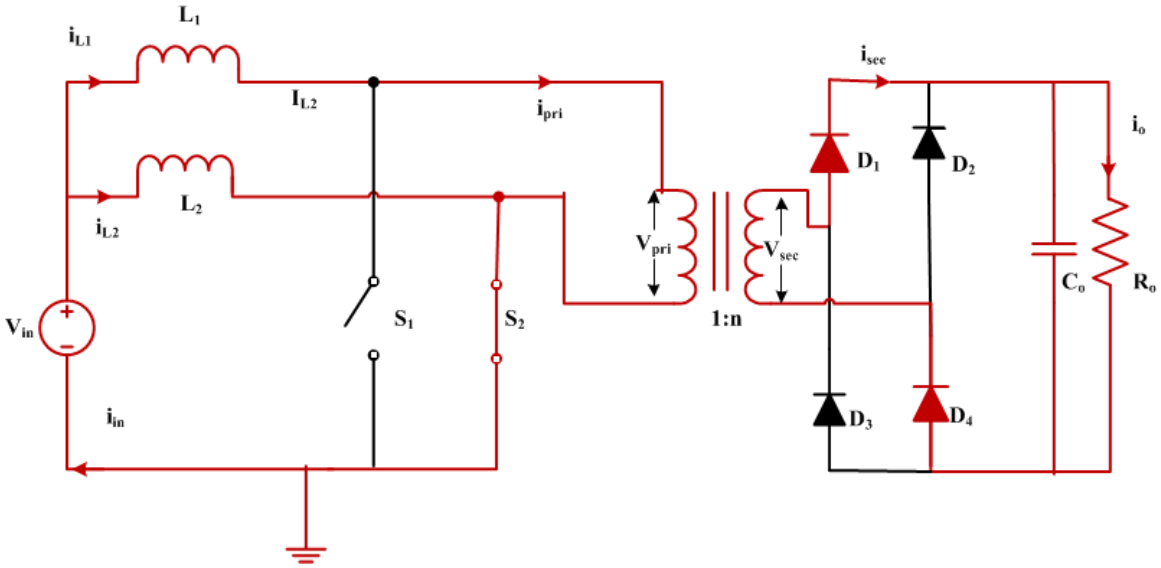


Figure 2.7: Mode2 (t_1-t_2)

$$V_{in} = L_1 \left(\frac{di_{L1}}{dt} \right) + V_{pri} \tag{2.7}$$

$$V_{in} = L_2 \left(\frac{di_{L2}}{dt} \right) \tag{2.8}$$

$$C_{out} \times \left(\frac{dV_o}{dt} \right) = \frac{I_{L1}}{n} - \frac{V_o}{R_o} \tag{2.9}$$

where n is the turn's ratio of the transformer.

Therefore,

$$\Delta i_{L1} = \frac{V_{in} - V_{pri}}{L_1} \times \frac{(1-D)T}{2} \tag{2.10}$$

$$\Delta i_{L2} = \frac{V_{in}}{L_2} \times \frac{(1-D)T}{2} \tag{2.11}$$

$$\Delta V_o = \frac{1}{C_o} \left(\frac{I_{L1}}{n} - \frac{V_o}{R_o} \right) \times \frac{(1-D)T}{2} \tag{2.12}$$

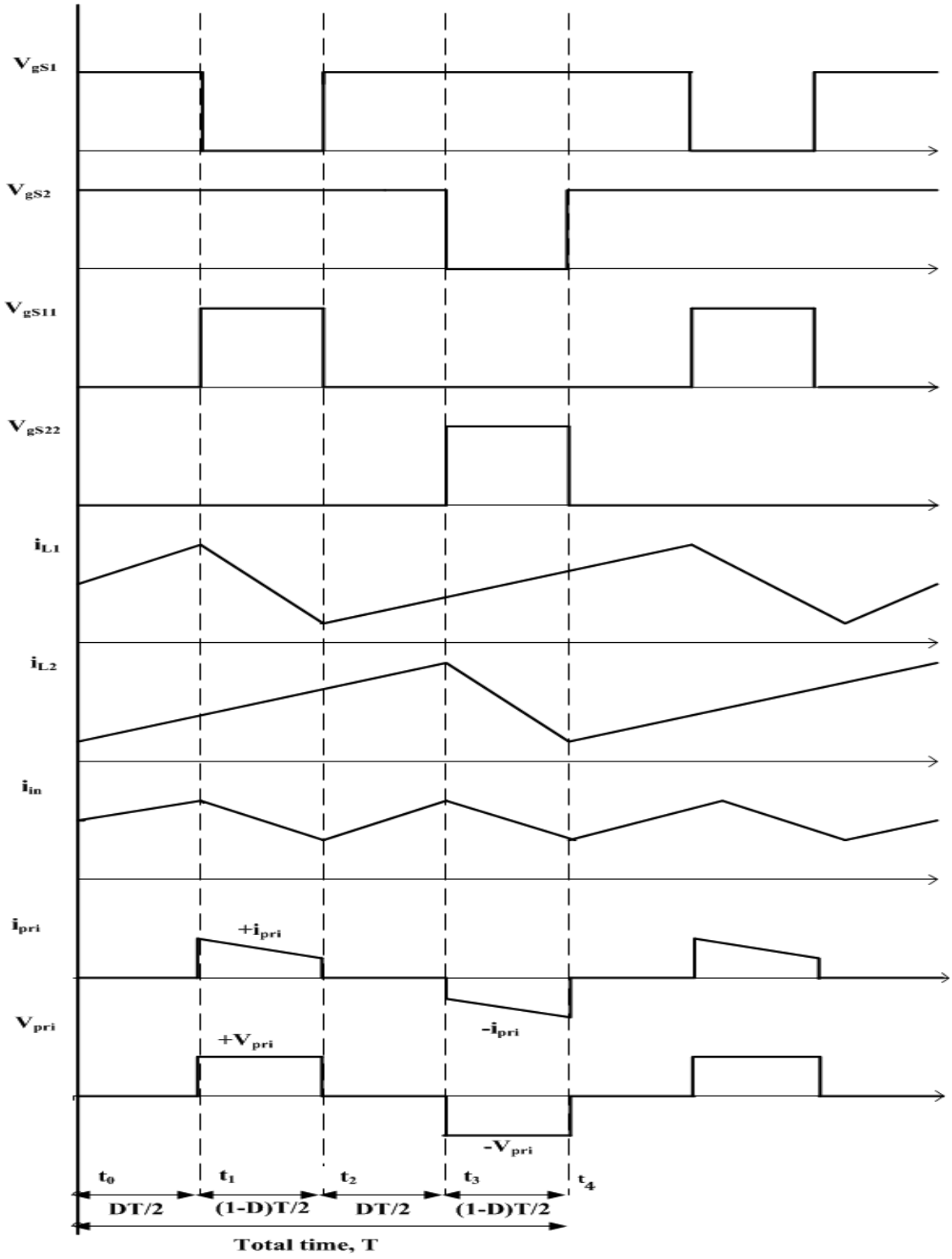


Figure 2.8: Operating waveforms of the dual inductor current fed push pull converter

3. **Mode 3 (t_2-t_3):** This mode of operation is similar to Mode 1. At this time, both the main switches S_1 and S_2 are ON again. The inductors get charged and the load is fed by the output capacitor.

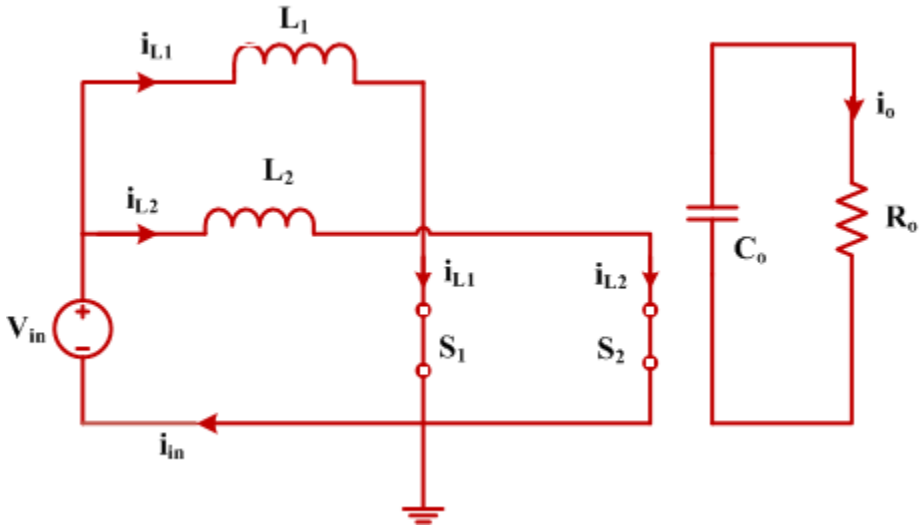


Figure 2.9: Mode3(t_2-t_3)

$$\Delta i_{L1} = \frac{V_{in}}{L_1} \times \frac{DT}{2} \tag{2.13}$$

$$\Delta i_{L2} = \frac{V_{in}}{L_2} \times \frac{DT}{2} \tag{2.14}$$

$$\Delta V_o = -\frac{V_o}{R_o \times C_o} \times \frac{DT}{2} \tag{2.15}$$

4. **Mode 4 (t_3-t_4):** At this mode of operation, the main switch S_2 opens and the inductor current I_{L2} is transferred to primary winding of the transformer. The voltage gets stepped up from the transformer and is rectified via diodes D_2 and D_3 of the synchronous rectifier on the secondary side . This rectified voltage is supplied to the load.

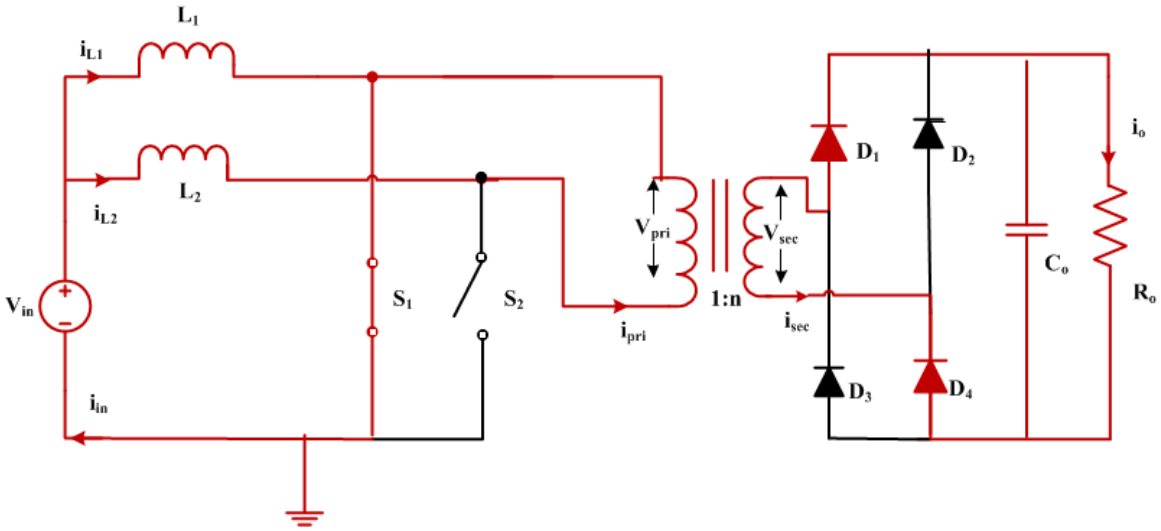


Figure 2.10: Mode4(t_3-t_4)

$$V_{in} = L_1 \left(\frac{di_{L1}}{dt} \right) - V_{pri} \tag{2.16}$$

$$V_{in} = L_2 \left(\frac{di_{L2}}{dt} \right) \tag{2.17}$$

$$C_o \times \left(\frac{dV_o}{dt} \right) = -\frac{I_{L2}}{n} - \frac{V_o}{R_o} \tag{2.18}$$

The above equations are reduced to:

$$\Delta i_{L1} = \frac{V_{in} + V_{pri}}{L_1} \times \frac{(1-D)T}{2} \tag{2.19}$$

$$\Delta i_{L2} = \frac{V_{in}}{L_2} \times \frac{(1-D)T}{2} \tag{2.20}$$

$$\Delta V_o = \frac{1}{C_o} \left(-\frac{I_{L2}}{n} - \frac{V_o}{R_o} \right) \times \frac{(1-D)T}{2} \tag{2.21}$$

Applying volt-second balance across one of the inductors,let us say L_1, from eq.2.4, eq.2.10, eq.2.13, and eq.2.19, we get:

$$\left[\frac{V_{in}}{L_1} \times \frac{DT}{2}\right] + \left[\frac{V_{in} - V_{pri}}{L_1} \times \frac{(1-D)T}{2}\right] + \left[\frac{V_{in}}{L_1} \times \frac{DT}{2}\right] + \left[\frac{V_{in}}{L_1} \times \frac{(1-D)T}{2}\right] = 0 \tag{2.22}$$

Solving eq.2.22, the primary side voltage of the transformer can be given as:

$$V_{pri} = \frac{2 \times V_{in}}{1-D} \tag{2.23}$$

Therefore, the output voltage which will be the product of primary side voltage of the transformer and the turns ratio (n) is equal to:

$$V_o = n \times V_{pri} = \frac{2n \times V_{in}}{1-D} \tag{2.24}$$

The generalized state space equations for the converter are as follows:

$$V_{in} = L_1 \left(\frac{di_{L1}}{dt}\right) + \frac{V_o}{n} \times \frac{(1-D)}{2} \tag{2.25}$$

$$V_{in} = L_2 \left(\frac{di_{L2}}{dt}\right) - \frac{V_o}{n} \times \frac{(1-D)}{2} \tag{2.26}$$

$$C_o \times \left(\frac{dV_o}{dt}\right) = -\frac{V_o}{R_{load}} + \frac{I_{L1}}{n} \times \frac{(1-D)}{2} - \frac{I_{L2}}{n} \times \frac{(1-D)}{2} \tag{2.27}$$

Taking Laplace transform of the above equations:

$$sL_1 I_{L1}(s) = V_{in}(s) - \frac{V_o(s)}{n} \times \frac{(1-D)}{2} \tag{2.28}$$

$$sL_2 I_{L2}(s) = V_{in}(s) - \frac{V_o(s)}{n} \times \frac{(1-D)}{2} \tag{2.29}$$

$$sC_o V_o(s) = -\frac{V_o(s)}{R_o} + \frac{I_{L1}(s)}{n} \times \frac{(1-D)}{2} - \frac{I_{L2}(s)}{n} \times \frac{(1-D)}{2} \tag{2.30}$$

If ac perturbation quantities $V_{in} = \hat{V}_{in}$,$D = \hat{D}$,$I_{L1} = \hat{I}_{L1}$,$I_{L2} = \hat{I}_{L2}$,$V_{out} = \hat{V}_{out}$ are added; the perturbed ac steady state space equations can be given by:

$$sL_1 \hat{I}_{L1}(s) = \hat{V}_{in}(s) - \frac{\hat{V}_o(s)}{n} \times \frac{(1-D)}{2} + \frac{V_o(s)}{n} \times \hat{D} \tag{2.31}$$

$$sL_2 I^{\wedge}_{L2}(s) = \hat{V}_{in}(s) - \frac{\hat{V}_o(s)}{n} \times \frac{(1-D)}{2} + \frac{V_o(s)}{n} \times \hat{D} \tag{2.32}$$

$$sC_o \hat{V}_o(s) = -\frac{\hat{V}_o(s)}{R_o} + \frac{\hat{I}_{L1}(s)}{n} . \left(\frac{1-D}{2}\right) - \frac{I_{L1}(s)}{n} . \hat{D} - \frac{\hat{I}_{L2}(s)}{n} . \left(\frac{1-D}{2}\right) + \frac{I_{L2}(s)}{n} . \hat{D} \tag{2.33}$$

If we consider that the value of inductors $L_1 = L_2 = L$,then the rate of change of inductor current will be the same and since the currents are phase shifted by $180°$,$I_{L1}(s) = -I_{L2}(s)$.The above equations can be reduced to :

$$2sL\hat{I}_L(s) = \hat{V}_{in}(s) - \frac{\hat{V}_o(s)}{n} \times (1-D) + 2\frac{V_o(s)}{n} \times \hat{D} \tag{2.34}$$

$$sC_o \hat{V}_o(s) = -\frac{\hat{V}_o(s)}{R_o} + \frac{\hat{I}_L(s)}{n} \times (1-D) - \frac{I_L(s)}{n} \times \hat{D} \tag{2.35}$$

where I_L is the average inductor current in each inductor.

After considering $\hat{V}_{in}(s)$ to be zero and solving the above equations, the voltage to duty cycle transfer function and the inductor current to duty cycle transfer function obtained is as follows:

$$\frac{\hat{V}_o}{\hat{D}} = \frac{\frac{4nV_{in}}{(1-D)^2} \times (1 - \frac{2sn^2L}{R_o(1-D)^2})}{\frac{2s^2n^2LC_o}{(1-D)^2)} + \frac{2sn^2LC_o}{R_o(1-D)^2} + 1} \tag{2.36}$$

$$\frac{\hat{I}_L}{\hat{D}} = \frac{\frac{4n^2V_{in}}{R(1-D)^2} \times (sC_oR_o + 2)}{\frac{2s^2n^2LC_o}{(1-D)^2} + \frac{2sn^2LC_o}{Ro(1-D)^2} + 1} \tag{2.37}$$

These derived transfer functions can be used for designing the compensators for voltage mode control and current mode control of the dc-dc converter used in each building block.

2.2.3 Advantages of selected topology

The selected topology is similar to a conventional boost converter which has an input boost inductor and single inductor current fed push pull converter with a boost inductor as well as isolating transformer described in [20]. But it provides several advantages over these topologies which are as follows:

1. The input current ripple is reduced as the phase shifted inductor currents in two inductors cancel out the ripple of the source current due to their interleaving operation.This further helps in reducing filtering requirements. Fig. 2.11 shows the interleaved operation of inductors at 50% duty cycle to reduce the input current ripple.

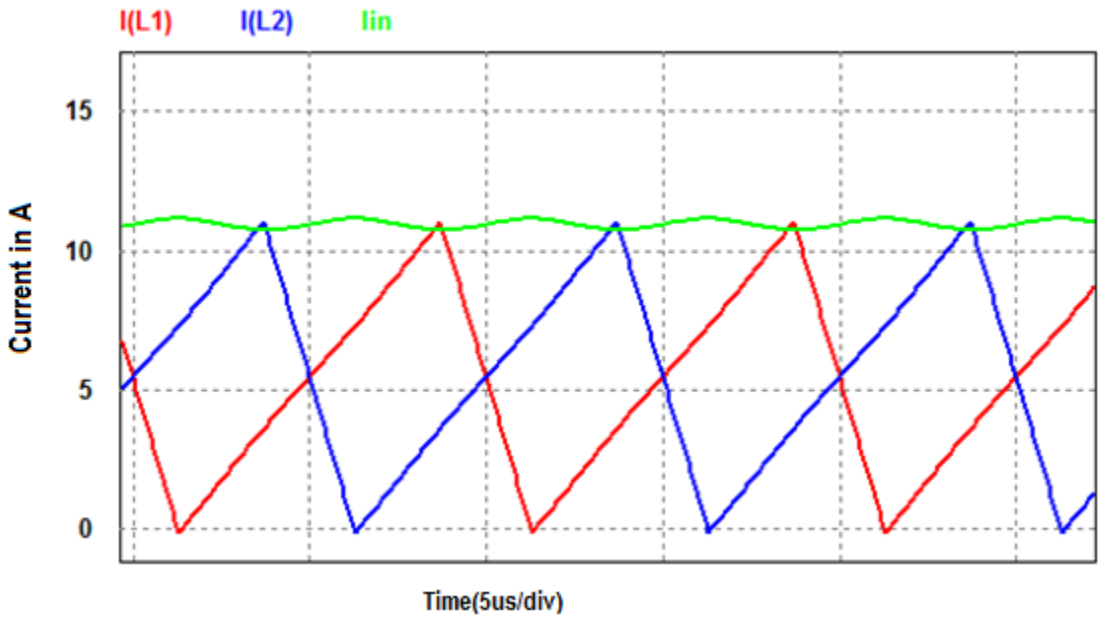


Figure 2.11: Interleaving operation of inductors to reduce ripple in input current

2. The inductor size is reduced to half due to the use of two inductors at the input.

3. The clamping circuit provides protection from voltage transients across switches and also from overload conditions.(Refer to Section 3.3.5)

4. The rms current across switches is reduced by half which again lowers the stress at the input side of the converter and the switching losses are reduced.

2.3 Building block controller

The building block controller performs the following functions:

1. **Control of the output voltage**

   The building block controller regulates the output voltage of the dc-dc converter to 28V. Its control is such that the output voltage can be adjusted depending upon the requirements of the system. A regulated voltage provides the benefit of reducing the load currents, which helps in making LV-AEA more efficient and cost-effective. For regulating the output voltage, error generated from the output obtained and the reference voltage of 28V is fed to the PI controller. The PI controller then reduces the error by adjusting the duty cycle of the switches. Fig.2.12 shows the gating signals for the open loop control of the converter.

2. **V, I and T monitoring**

   In an active electric accumulator where many building blocks are working in parallel, it becomes very important that every individual block is managed electrically and thermally. Therefore, it becomes crucial to monitor the voltage (V), current (I) and temperature (T) of each block. The input voltage (V_{in}) can be measured with the help of a resistor divider network connected to one of the parallel-connected cells. The output voltage generated from this network can then be compared with a reference voltage to determine the voltage status of the building block. The source current can be measured using a current sensing resistor in series with the two input inductors of the dc-dc converter. The voltage drop across this resistor is the measure of the current flowing through it. The measure of temperature can be done with the help of a thermistor whose

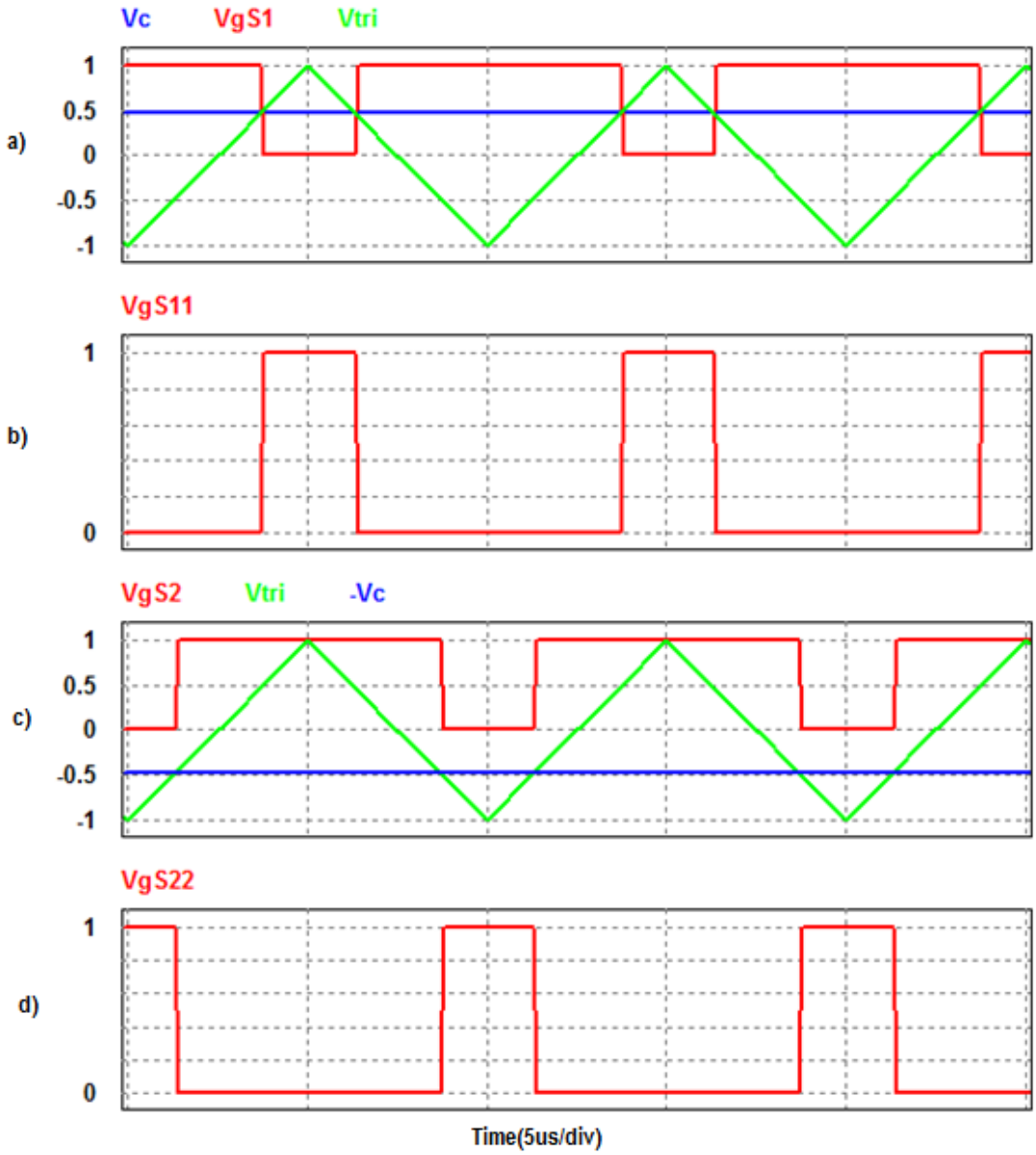


Figure 2.12: Gating signals of the dc-dc converter: a) Control voltage V_c,triangular waveform V_{tri}, gating signal of main switch S_1, b) Gating signal of clamp switch S_{11}, c) Control voltage V_c,triangular waveform V_{tri}, gating signal of main switch S_2, d) Gating signal of clamp switch S_{22}

resistance varies in proportion with the temperature. Any failure mode if detected can be shown with the help of a light emitting diode (LED), which turns on whenever such condition persists. The failure mode can then be reported to the AEA controller to disable the unoperational building block.

3. **Over voltage and under voltage protection**

   As mentioned in Section 2.1.3, overcharging or undercharging can lead to various failure modes in a Li-ion battery. Therefore it is of utmost importance that the Li-ion cell is protected from overvoltage or under voltage conditions. In case of a failure, the operation of the affected block can be stopped by disabling the PWM signals for the converter. This block can then be isolated form the rest of the blocks and the rest of the blocks still continue their operation to supply the load. For the protection purposes, a protection control loop is added to the voltage control loop. Its control is such that when the cell voltage reaches its maximum or the minimum limit, the main switches S_1 and S_2 of the converter are opened and the auxiliary/clamp switches S_{11} and S_{22} are closed so that the energy stored in the inductors gets transferred to the clamped capacitor.

4. **Overcurrent Protection**

   The main switches S_1 and S_2 of the dc-dc converter can control the discharging of the building block. In this thesis, only unidirectional mode of the converter is considered. Hence, charging mode is not discussed for overcurrent protection. Whenever the discharge current exceeds the maximum threshold limit, the main MOSFETs can be turned off using PWM signals. High current for few microseconds can be neglected using a delay timer in the control circuitry. But longer period currents will cause a fault condition and the MOSFETs will

be turned off until the normal operating conditions are regained. A snubber circuit can be added to each MOSFET to prevent any damage from the transients during turn on and turn off.

5. **Thermal protection**

   The performance of the Li-ion cell is highly affected by the change in temperature. To ensure safe operation, it becomes necessary to monitor and control the temperature of the energy storage unit (ESU) of each building block. A thermistor can be used to detect the temperature changes. If the cells in ESU are discharged at normal discharge rate, the effeciency of the dc-dc converter would be high and less amount of power will be dissipated. Interrupting the current flow and turning the building block off will be sufficient in that case. But if more power is dissipated, then advanced cooling methods need to be adopted. The issue of thermal management is out of scope for this thesis.

2.4 AEA master controller

1. **Synchronization and control of the building blocks**

   AEA controller needs to monitor and control the operation of all the building blocks. If one of the cells in the block or the whole block goes bad, it can isolate that particular block from the rest of the blocks by operating a single MOSFET switch. To know the working condition of the block, it makes use of the measurement signals sent by the BB controller. The AEA controller also needs to ensure that the building blocks are synchronized through interleaving of their gating signals. One of the options is to operate the building blocks as

a stand-alone unit such that the gating signals of each block remain unaffected from eachother. The other option is to follow a master-slave approach where the gating signals of the building blocks are phase shifted by $180°/N$ with respect to eachother, where N is the total number of building blocks.This approach is further discussed in Section 3.5.1.

2. **Load sharing**

   The AEA master controller facilitates co-ordination between different blocks. The load requirements for the whole system are managed with the help of the AEA master controller. The controller generates and sends the signals of required output power to every building block. It allocates or reallocates the output power required from each building block based on the sensor measurements and power demand by sending and receiving signals. Voltage and current sensors can be utilized to provide measurements of the output cell voltage and the output current of each block respectively. In case one of the blocks is disconnected, it reallocates the output power required from the other blocks.Load sharing can be achieved using a current control loop that enables equal power sharing between building blocks connected in parallel.

2.5 Summary

In this chapter, the description of the LV-AEA was provided. The ESU of LV-AEA contains only parallel connected cells, thereby making the LV-AEA more fault-tolerant due to lack of failure propagation as in series-connected cells. The voltage of ESU is boosted using a dual inductor current fed push pull converter, the steady state analysis of which were also presented. The main difference of this converter from the conventional boost converter is the presence of two input inductors and an isolating transformer. The transfer functions for the dc-dc converter obtained are very similar to that of a boost converter and hence the control design will have the same pros and cons as in boost compensator design. The building block (BB) controller of the LV-AEA provides voltage regulation and incorporates protective functions whereas the AEA controller takes care of the whole unit and enables equal load sharing.

Chapter 3

Design of the Low Voltage Active Electric Accumulator

In this chapter, the design of all the components in LV-AEA has been introduced. Section 3.1 provides the application example for which the LV-AEA will be designed. The design details of the ESU and the dc-dc converter of each building block are presented in Section 3.2 and Section 3.3 respectively. Section 3.4 explains the output voltage control and various protective functions of the BB controller. Finally, Section 3.5 describes the AEA controller operation and design required for proper load sharing in the LV-AEA.

3.1 Design example

For the design of LV-AEA, an Auxiliary Power Unit (APU) Start application for the aircraft is considered where a minimum of 7kW is required during a successful start attempt. The LV-AEA shall be able to support a successful start within three

attempts where each start could take one minute and should be able to give the rated Ah for 30 minutes.

3.2 ESU design

The selected Li-ion cell for use in ESU is GS YUASA-LVP10 [21] which has a nominal voltage of 3.7V and a rated capacity of 10Ah. At maximum discharge rate of 5C, the discharge capacity of a single Li-ion cell would be 50Ah. If five of these cells are connected in parallel and the minimum cell voltage of 2.75V is taken into account, the output power that can be derived at 5C discharge rate would be nearly 700W. The output power of 7kW required for the APU can be provided by connecting ten of such building blocks in parallel with each block supplying 700W. The design requirements for the APU start application have been defined in Table 3.1.

Output Power, P_o	7kW
Input voltage, V_{in}	2.75V - 4V
Output voltage, V_o	28V
Number of building blocks, N	10
Output Power of each block, P_{ob}	700W

Table 3.1: Design requirements for an APU application

The cell used was modeled using the Li-ion battery module given in PSIM for the purpose of conducting simulations for the building block operation. Fig. 3.1 and Fig. 3.3 show the PSIM charging and discharging model used to predict its charging and discharging characteristics. The charging characteristics of the cell at 0.5C rate and discharging characteristics at 1C rate of the cell are shown in Fig. 3.2 and Fig. 3.4 respectively.

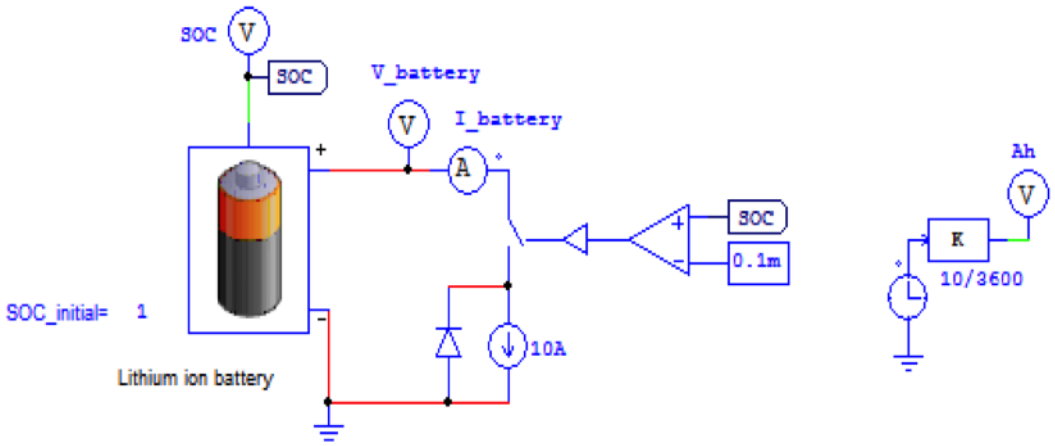


Figure 3.1: Li-ion cell discharge model

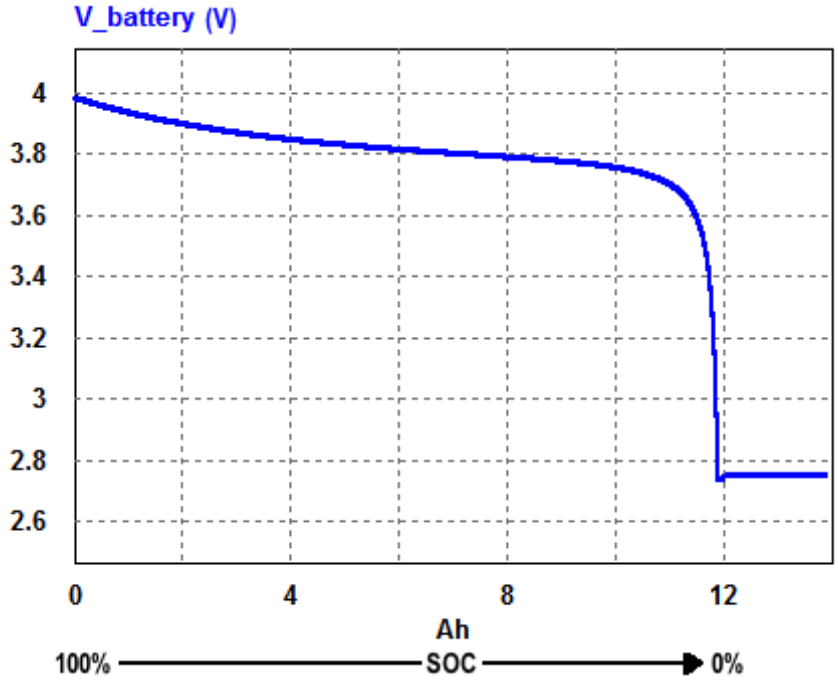


Figure 3.2: Li-ion cell discharge characteristics

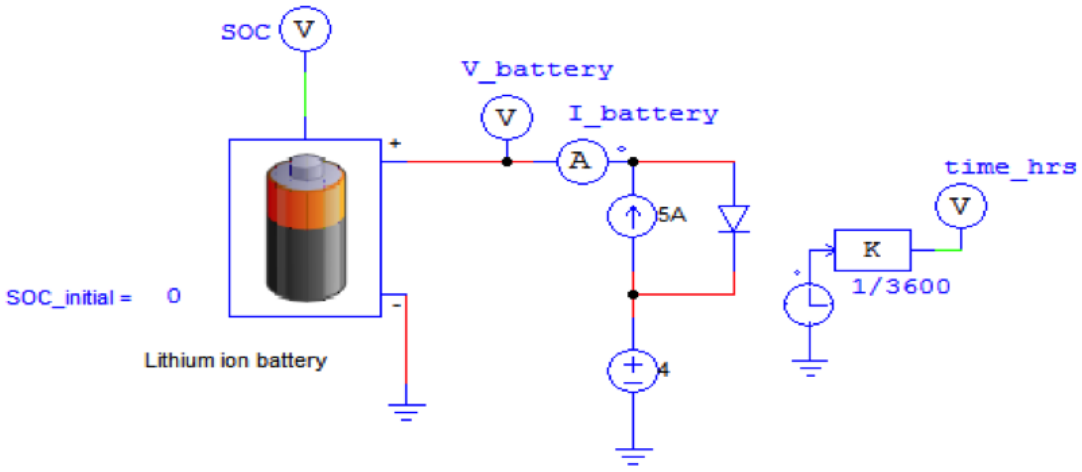


Figure 3.3: Li-ion cell charging model

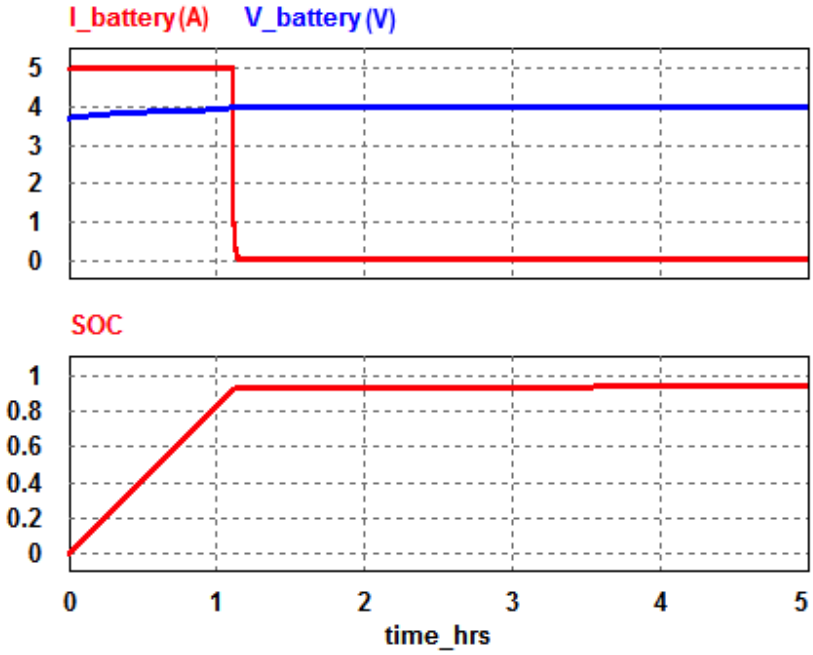


Figure 3.4: Li-ion cell charge characteristics

3.3 DC-DC converter design

Since, each building block of LV-AEA is supplying 700W, the dc-dc converter used in every block should be able to provide the required power at input cell voltage range of (2.75V-4V). The switching frequency of the converter is 100kHz which helps in reducing the size of magnetic components used in it. The assumed effeciency for the converter design is 98% and output voltage of 28V needs to be provided by it.The specifications for the design of the dc-dc converter are listed in Table 3.2 below:

Output Power,P_o	700W
Input voltage,V_{in}	2.75VDC - 4VDC
Output voltage,V_o	28VDC
Effeciency,η	98%
Switching frequnecy,f_{sw}	100kHz

Table 3.2: Converter design specifications

The following sections discuss the design of the components used in the converter:

3.3.1 Selection of Transfomer's turn ratio,n

From the voltage conversion ratio eq. 2.24, the duty cycle can be defined as:

$$D = 1 - \frac{2nV_{in}}{V_o} \tag{3.1}$$

where n is the transformer's turn's ratio.

If the transformer's turn ratio is selected as $n = 2$, the range of duty cycle for the converter will be $0.43 < D < 0.60$ from maximum input voltage of 4V to minimum input voltage of 2.75V. The duty cycle of the switches can be given by $D = 2(D_{sw}) - 1$ where D_{sw} is always greater than 50% as the switches cannot turn off at the same

time during converter's operation. With increase in the turn's ratio, the transformer's primary side voltage V_{pri} gets reduced. As a result lower-voltage but higher current MOSFETs can be used for the switches. Fig. 3.5 shows the variation of transformer primary voltage with respect to the transformer turn's ratio. At selected turn's ratio of 2, the primary side voltage is 14V which means that MOSFET with voltage rating of more than 14V can be chosen for the switches used in the converter.Usually a derating factor of 50% is considered for the safety of the power devices.

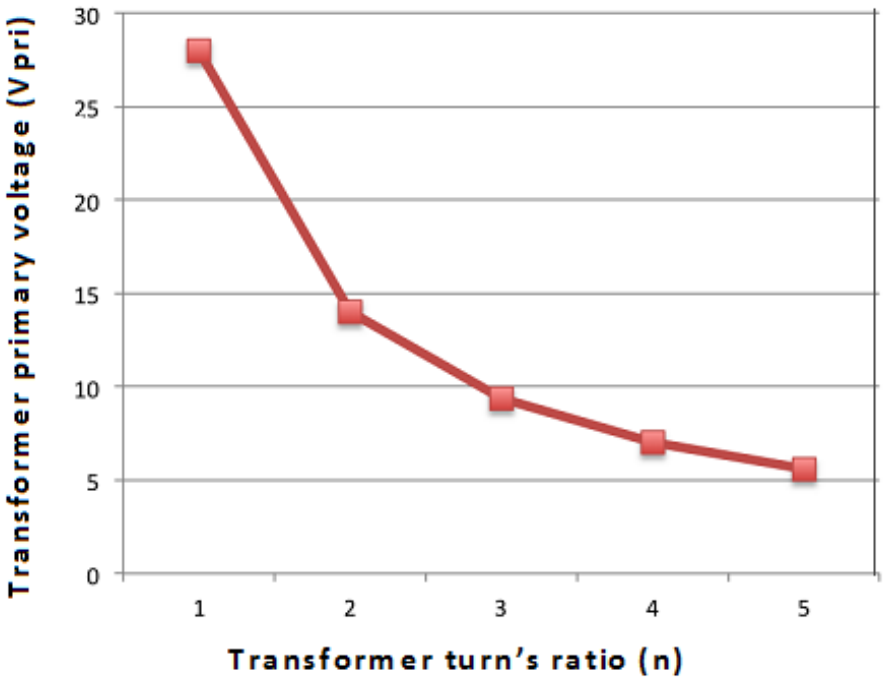


Figure 3.5: Transformer primary voltage versus transformer turn's ratio

3.3.2 Inductor design

Inductance value calculation

Taking into account 98% effeciency (η) and minimum input voltage of $V_{in} = 2.75V$, the average input current of the converter can be determined using the equation below:

$$I_{in} = \frac{P_o}{V_{in} \times \eta} = 259.7A \tag{3.2}$$

If the input ripple current is taken as 1% of the average input current, the value of the input ripple current would be 2.59A. For the design of the inductor, if we consider the same inductance values for both the input inductors i.e. $L_1 = L_2 = L$, the inductance value for each inductor can then be calculated using the equation given in [7] as follows:

$$L = \frac{V_{in}}{\Delta I_{in}} \times \frac{D}{f_{sw}} = 6.38\mu H \approx 6.4\mu H \tag{3.3}$$

Fig. 3.6 shows the preliminiary results of the interleaved operation of inductor currents to provide an input current ripple of less than 2.59A.

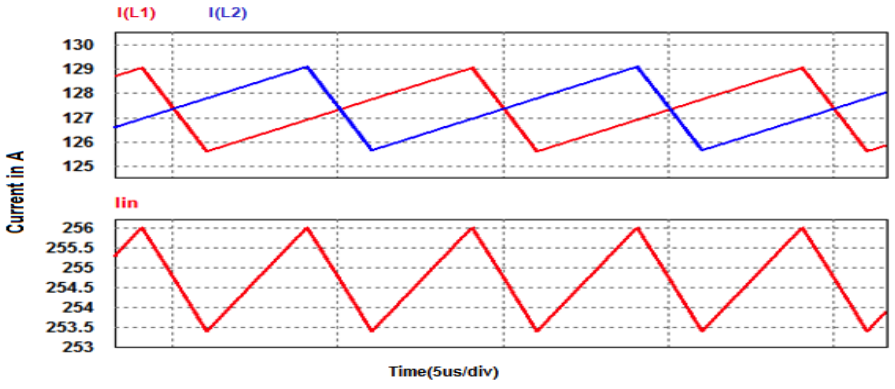


Figure 3.6: Input ripple current with $6.4\mu H$ inductance

Fig. 3.7 represents the change in inductor value with respect to switching frequency and percentage of ripple current.It can be seen that with increase in switching frequency the inductance value decreases and the ripple current decreases for higher inductance values.

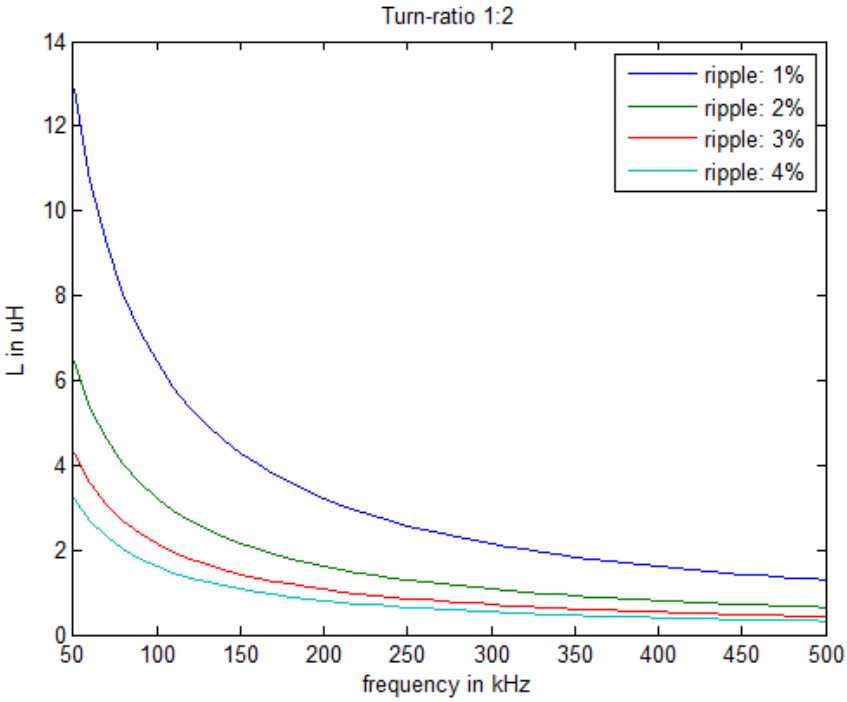


Figure 3.7: Inductor value vs Frequency

Inductor design based on calculated value of L

For the design of the inductor, it is important to know the average current in each inductor which is equal to half of the total average input current :

$$I_L = \frac{I_{in}}{2} = 129.8A \tag{3.4}$$

Because of such large current,four parallel connected inductors of value $L_p = 25.6\mu H$ have been considered for the design of each inductor. Each parallel connected inductor will carry one-fourth of the average inductor current, $I_{Lp} = 32.5A$ and this will further help in minimizing the conduction losses. The average maximum value of current I_{Lpmax} that each parallel connected inductor should carry without saturation is:

$$I_{Lpmax} = I_{Lp} + \frac{\Delta I_{in}}{2} = 34.1A. \tag{3.5}$$

For the design of the inductor, area product A_p method for gapped cores as given in Chapter 8 of [22] has been used.The following parameters are calculated for the design and loss estimation:

1. Calculation of the energy required

$$E = \frac{L_p I_{Lpmax}^2}{2} = 0.015Ws \tag{3.6}$$

2. Calculation of the area product A_p

$$A_p = \frac{2 \times E \times 10^4}{B \times J \times K_u} = 5cm^4 \tag{3.7}$$

where B is the maximum flux density of 0.3T; J is the current density of 500A/cm^2 ; and K_u is a factor of 0.4 related to the utilized core area by the winding wire.

As per the calculated area product A_p in eq.3.7, the core that meets our requirements is ETD-49 from Ferroxcube [23] with an area product of 7.25cm^4.

The cross-sectional area of the core is $A_e = 2.11cm^2$. The wire size calculated for the winding is AWG 8 with a bare wire area of $A_{bw} = 0.0837cm^2$. Since the cross-sectional area of calculated wire size makes it hard to wind,a stranded wire with 65 strands of AWG26 equivalent to AWG8 is used.

3. Calculation of the number of turns,N_t

   The number of winding turns can be calculated as follows:

$$N_t = \frac{A_e \times W_a \times K_f}{A_{bw}} = 11.3 \approx 11turns \tag{3.8}$$

   where W_a is the effective window area factor =0.75, and $K_f = 0.6$ is the fill factor

4. Calculation of series resistance,R_{dcr}

$$R_{dcr} = MLT \times N_t \times \frac{R_w}{S_n} \times 10^{-}6 = 10.3 \times 11 \times \frac{1345}{65} \times 10^{-}6 = 2.3m\Omega \tag{3.9}$$

   where R_w is the resistance of AWG26 wire in $\frac{\mu\Omega}{cm}$,S_n is the number of strands of wire used; $MLT = 10.3cm$ is the mean length per turn obtained from the datasheet[23].

5. Copper loss calculation,P_{cu}

   Since the parallel connected inductors equivalent to the one of the inductors of the converter are four in number, the total copper loss for each inductor is calculated as follows:

$$P_{Lcu} = I_L^2 \frac{R_{dcr}}{4} = 9.6W \tag{3.10}$$

For both the inductors,the total copper loss can be given by:

$$P_{cu} = 2 \times P_{Lcu} = 19.3W \tag{3.11}$$

3.3.3 Transformer design

The design requirements for the transformer are given in Table 3.3

Output Power,P_o	700W
Primary side voltage,V_{pri}	14V
Output voltage,V_o	28V
Effeciency,η	98%
Turn's ratio,n	2
Flux Density,B	0.1T
Switching Frequency,f_{sw}	100kHz

Table 3.3: Design requirements for the transformer

Using the area product (A_p) method from [22] ,the transformer design specifications calculated are illustrated in Table 3.4.

Core Selected	ETD54 [23]
Manufacturer	Ferroxcube
Magnetic Path Length, MPL	12.7cm
Magnetic Length per Turn, MLT	11.7cm
Effective area, A_e	$2.80cm^2$
Area product, A_p	$8.8cm^4$
Window area, A_w	$3.16cm^2$
Core Weight,W_{tfe}	180grams
Minimum wire size required	AWG13
Actual stranded wire used	AWG26
Number of primary turns,N_p	2
Number of strands of AWG26 on primary side,S_{np}	61
Number of secondary turns,N_s	4
Number of strands of AWG26 on secondary side,S_{ns}	30
Winding factor	0.28
Temperature rise	29.5° C

Table 3.4: Transformer design specifications

Calculation of the transformer losses

Also from [22], the transfomer losses can be calculated as follows:

1. Transformer copper loss,P_{cu}

   The copper loss in the transformer is the sum of primary side copper loss and

the secondary side copper loss.

$$P_{cu} = P_{pcu} + P_{scu} \tag{3.12}$$

$$P_{pcu} = I_{pri}^2 R_{pri} = 3.3W \tag{3.13}$$

I_{pri} is the rms value of the primary side current of the transformer which is given by:

$$I_{pri} = \sqrt{I_L^2 \times (1 - D)} = 82A \tag{3.14}$$

,and R_{pri} is the primary winding resistance calculated as follows:

$$R_{pri} = MLT \times N_p \times \frac{R_w}{S_{np}} \times 10^{-}6 = 0.5m\Omega \tag{3.15}$$

where

I_L is equal to the average current in each inductor,

D is the duty cycle of 0.6 at input voltage of 2.75V,

$MLT = 11.7cm$ is the mean length per turn,

R_w is the resistance of AWG26 wire = $1345\frac{\mu\Omega}{cm}$, and

S_{np} is the number of strands of wire used on primary side

$$P_{scu} = I_{sec}^2 R_{sec} = 4.2W \tag{3.16}$$

I_{sec} is the rms value of the secondary side current of the transformer which is given by:

$$I_{sec} = \sqrt{\left(\frac{I_L}{n}\right)^2 \times (1 - D)} = 41A \tag{3.17}$$

,and R_{sec} is the secondary winding resistance calculated as follows:

$$R_{sec} = MLT \times N_s \times \frac{R_w}{S_{ns}} \times 10^{-}6 = 2.5m\Omega \tag{3.18}$$

where

I_L is equal to the current in each inductor,

n is the transformer turn's ratio,

D is the duty cycle of 0.6 at input voltage of 2.75V,

$MLT = 11.7cm$ is the mean length per turn,

R_w is the resistance of AWG26 wire = 1345 $\frac{\mu\Omega}{cm}$,

S_{ns} is the number of strands of wire used on secondary side

Therefore the total core loss in the transformer is:

$$P_{cu} = P_{pcu} + P_{scu} = 7.5W \tag{3.19}$$

2. Transformer core loss,P_{core}

$$P_{core} = \frac{mW}{g} \times W_{tfe} \times 10^{-}3 = 4.5W \tag{3.20}$$

where W_{tfe} is the core weight of 180g [24],and

$$\frac{mW}{g} = 5.983 \times 10^{-}5 \times f_{sw}^{1.66} \times B^{2.68} = 24.9W$$

3. Total loss,P_{loss}

   From eq.3.19 and eq.3.20,total loss in the transformer is equal to

$$P_{loss} = P_{cu} + P_{core} = 12W \tag{3.21}$$

3.3.4 Main switches S_1 and S_2

As mentioned in Section 3.2.1, with the selected turn's ratio of 2, the voltage rating for the required MOSFETs is 14V. For the selection of the MOSFET for the main switches,it is important to know its rms value of current which can be calculated by referring to the Fig. 3.34 as follows:

$$I_{Srms} = \sqrt{\frac{a^2DT + (2a)^2(1-D)T}{T}} = a\sqrt{2-D};\ where\ a\ is\ I_{in}/2 \tag{3.22}$$

$$Therefore, I_{Srms} = \sqrt{2-D} \times \frac{I_{in}}{2} \tag{3.23}$$

Considering duty cycle at minimum input voltage of $V_{in} = 2.75V$, the MOSFET rms current is 153.6A. Because of such large current, four parallel connected MOSFETs have been considered carrying 38.4A each. Derating the current and voltage ratings, MOSFET IPB009N03LG[25] is selected with $V_{DSS} = 30V$ and $I_D = 180A$ which has $R_{DSon} = 0.95m\Omega$ at junction temperature $T_j$of $60°C$. The total losses from four parallel connected MOSFETs comprise of conduction and switching losses which are calculated using the equations given below:

$$I_{Scond} = I_{Srms}^2 \times \frac{R_{DSon}}{4} = 5.6W \tag{3.24}$$

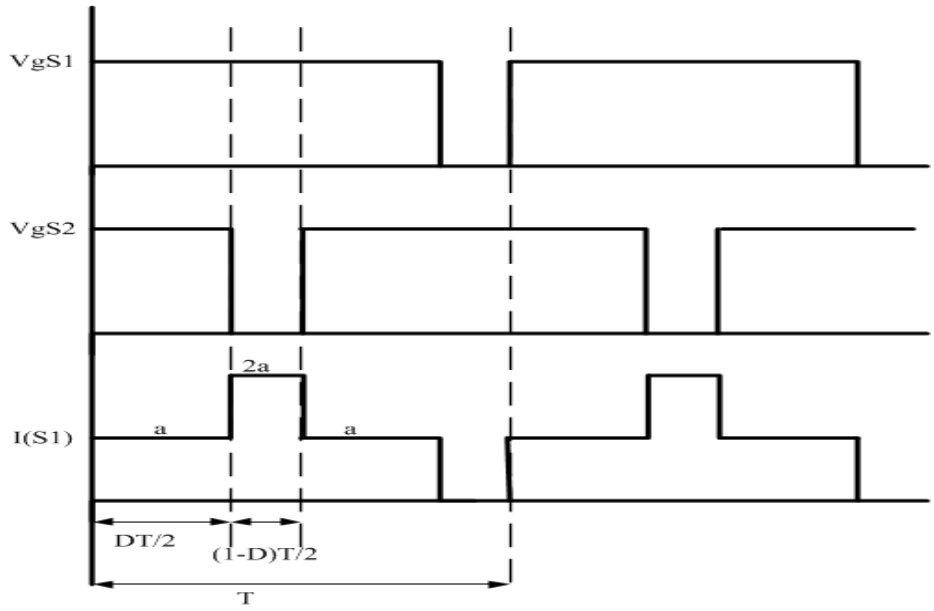


Figure 3.8: Gating signals of main switches S_1 and S_2 and corresponding current waveform of switch S_1

The switching loss of the MOSFET can be calculated by:

$$I_{Ssw} = \frac{I_{in}}{2} \times V_{pri} \times f_{sw} \times (t_{rise} + t_{fall}) = 6.5W \tag{3.25}$$

where I_{in} is the input current, f_{sw} is the switching frequency, and $t_{rise} = 14ns$,$t_{fall} = 22ns$ are the rise and fall times of MOSFETs from the datasheet[25]. Since there are two main MOSFETs used in the converter,therefore

$$\text{Total loss} = 2 \times I_{Scond} + 2 \times I_{Ssw} = 24.2W \tag{3.26}$$

3.3.5 Active clamp circuit

The main function of the active clamp circuit is to recover the leakage energy of the transformer without causing overvoltage conditions in the main conducting switches S_1 and S_2. Without the use of active clamp circuit, the leakage energy of the transformer causes high voltage spikes across the main MOSFETs during their turn off due to the resonance phenomena occuring between the leakage inductance and the MOSFET stray capacitance. Due to this high voltage rating MOSFETs with higher R_{DSon} are required and switching losses also increase, thereby the effeciency of the overall system is affected. Generally, RCD snubber circuits can be used to dissipate this leakage energy but the effeciency gets reduced. With the use of an active clamp circuit, the leakage energy is passed onto the clamp capacitor which then restores this energy rather than dissipating it and transfers it to the primary winding of the transformer [9]. The active clamp circuit consists of two clamp switches (S_{11},S_{22}) working in a complementary manner with respect to the main switches (S_1,S_2) and a clamped capacitorC_{cl}. The design of the active clamp circuit at input voltage of 2.75V,100kHz switching frequency and duty cycle of 60% is discussed below:

Selection of clamped capacitor, C_{cl}

The value of the clamped capacitor C_{cl} can be determined by using the equation below:

$$C_{cl} = \frac{I_{pri} \times D}{\Delta V_{cl} \times f_{sw} \times 2} \tag{3.27}$$

The value of I_{pri} calculated in Section 3.2.3 is 82A and considering ripple in clamp voltage V_{cl} to be 500mV at the maximum duty cycle operation of 0.60 ,the value of the clamped capacitor calculated is $33\mu F$.The maximum value of capacitor equivalent

series resistance (ESR) required is:

$$ESR = \frac{\Delta V_{cl}}{I_{pri}} = 6m\Omega \tag{3.28}$$

The selected capacitor based on the calculations above is $47\mu F$ ceramic capacitor C3216X5R1E476M160AC[26] from TDK with voltage rating of 25V and ESR of $2m\Omega$. As per [9], in order to ensure proper opertion of the clamp circuit, the minimum capacitor value should be selected such that it exceeds half of the resonant period formed by C_{cl} and L_{lk}.

$$C_{clamp} > \frac{T^2(1-D)^2}{\pi^2.L_{lk}} \tag{3.29}$$

To estimate the leakage inductance, we need to calculate the value of primary side inductance L_{pri} which can be given by:

$$Lpri = \frac{V_{in}}{\Delta I_{in}} \times \frac{D}{f_{sw} \times 2} = 3\mu H \tag{3.30}$$

where $\Delta I_{in} = 1\%$ of input current I_{in}.
If we assume the value of leakage inductance L_{lk} of the transformer to be 1% of L_{pri} i.e. $0.03\mu H$, the minimum value of clamped capacitor required is $5\mu F$.Thus, the selected capacitor meets the above mentioned criteria.

Selection of clamp switches (S_{11} and S_{22})

Same MOSFETs IPB009N03LG[25] with $V_{DSS} = 30V$ and $I_D = 180A$ used for the main switches can be used for the clamp switches but in this case no parallel connection of the MOSFETs is required. The main losses connected to the clamp circuit would be switching losses when the clamp switches operate to recover the leakage

energy. The losses of the clamp circuit are assumed to be equal to switching losses in main MOSFETs.

Simulation results for clamp operation

Fig. 3.9 and Fig. 3.10 show the operation of the dc-dc converter with and without using active clamp circuit respectively. From Fig. 3.9, it can be seen that the clamp voltage rises to compensate for the introduced leakage energy and the primary side current of the transformer I_{pri} increases due to the presence of leakage inductance. The voltage across the main switch remains equal to the clamped voltage and does not experience any overshoot as it does in the converter without the use of clamp shown in Fig. 3.10.

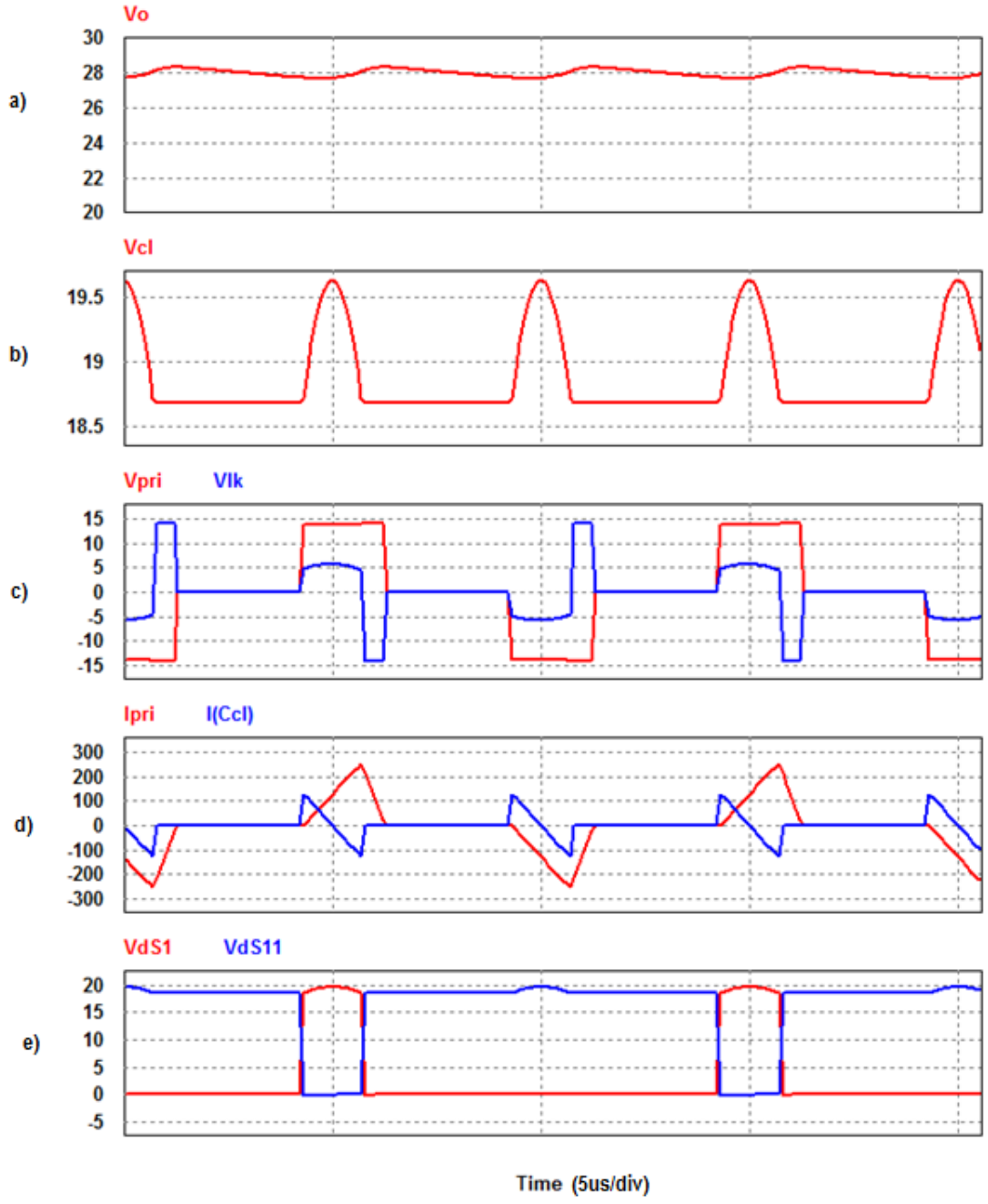


Figure 3.9: DC-DC converter operation with active clamp circuit: a) Output Voltage (V_o), b) Clamped capacitor voltage (V_{cl}), c) Primary side voltage of transformer (V_{pri}) and voltage across leakage inductor(V_{lk}), d) Transformer primary side current (I_{pri}) and current in the clamped capacitor (I_{Ccl}), and e) Drain to source voltage in main switch S_1 and clamp switch S_{11} (V_{dS1},V_{dS11})

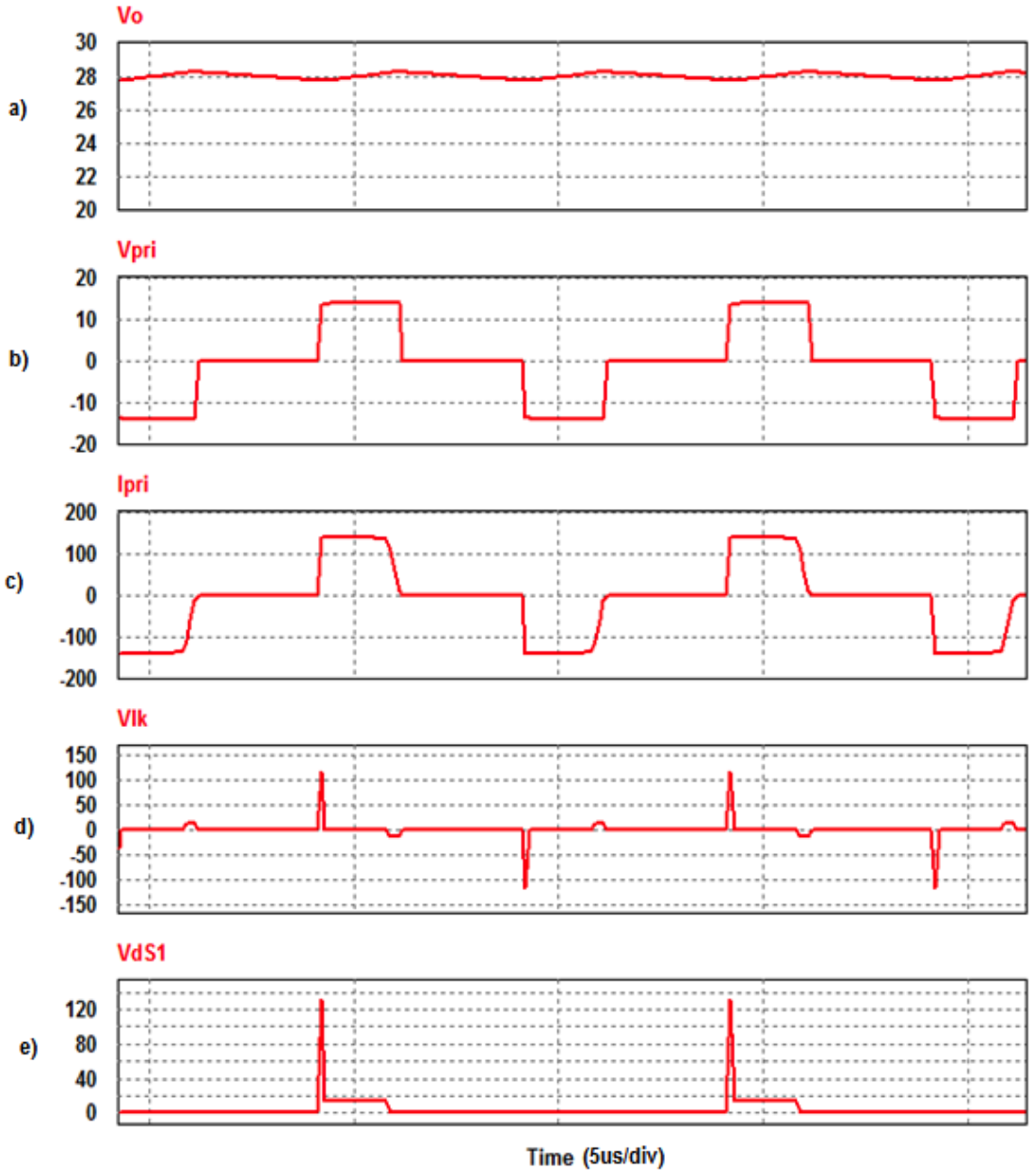


Figure 3.10: DC-DC converter operation without use of active clamping: a) Output Voltage(V_o), b) Primary side voltage of transformer (V_{pri}), c) Transformer primary side current (I_{pri}), and d) Drain to source voltage in main switch S_1 (V_{dS1})

Soft-Switching operation of active clamp circuit

The instantaneous turn on/off of the clamp switch working in complementary manner with respect to the main switch can cause ringing operation and high current spikes can be seen in the switches. This leads to increased losses in the converter. This condition can be avoided using ZVS which is achieved by ensuring that the maximum delay time between the turn on and turn off of the main and the corresponding auxiliary switch is less than one-fourth of the resonant period between leakage inductance L_{lk} and clamp capacitor C_{cl} [7]. Taking the selected capacitor value $C_{cl} = 47\mu F$ and leakage inductance $L_{lk} = 0.03\mu H$;the maximum time delay is calculated as follows:

$$T_{S1} - T_{S11} = \sqrt{L_{lk}.C_{cl}}.\frac{\pi}{2} = 1.86\mu s \tag{3.31}$$

After doing some analysis, a delay circuitry with time period of $1.16e^{-7}s$ as shown in Fig.3.11 was added to the control loop.Fig.3.12 and Fig.3.13 show the converter operation before and after the introduction of delay time.

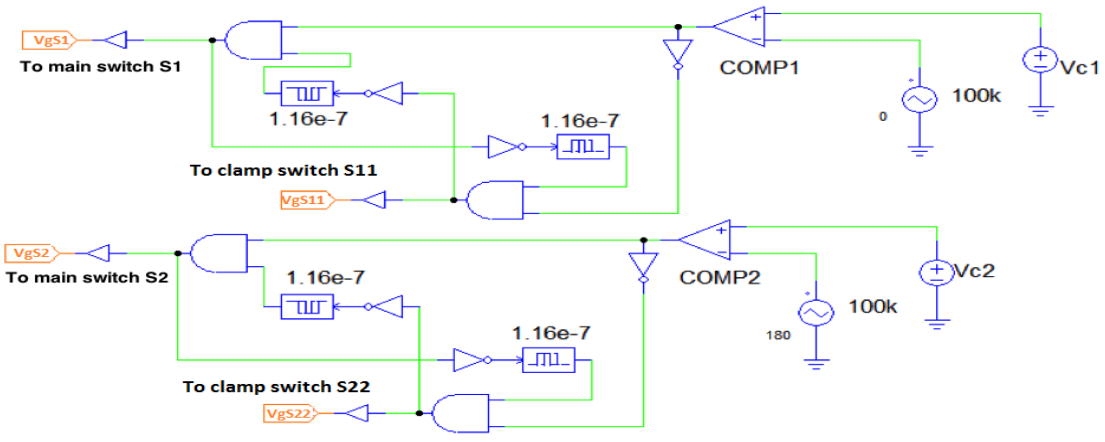


Figure 3.11: Delay Circuit

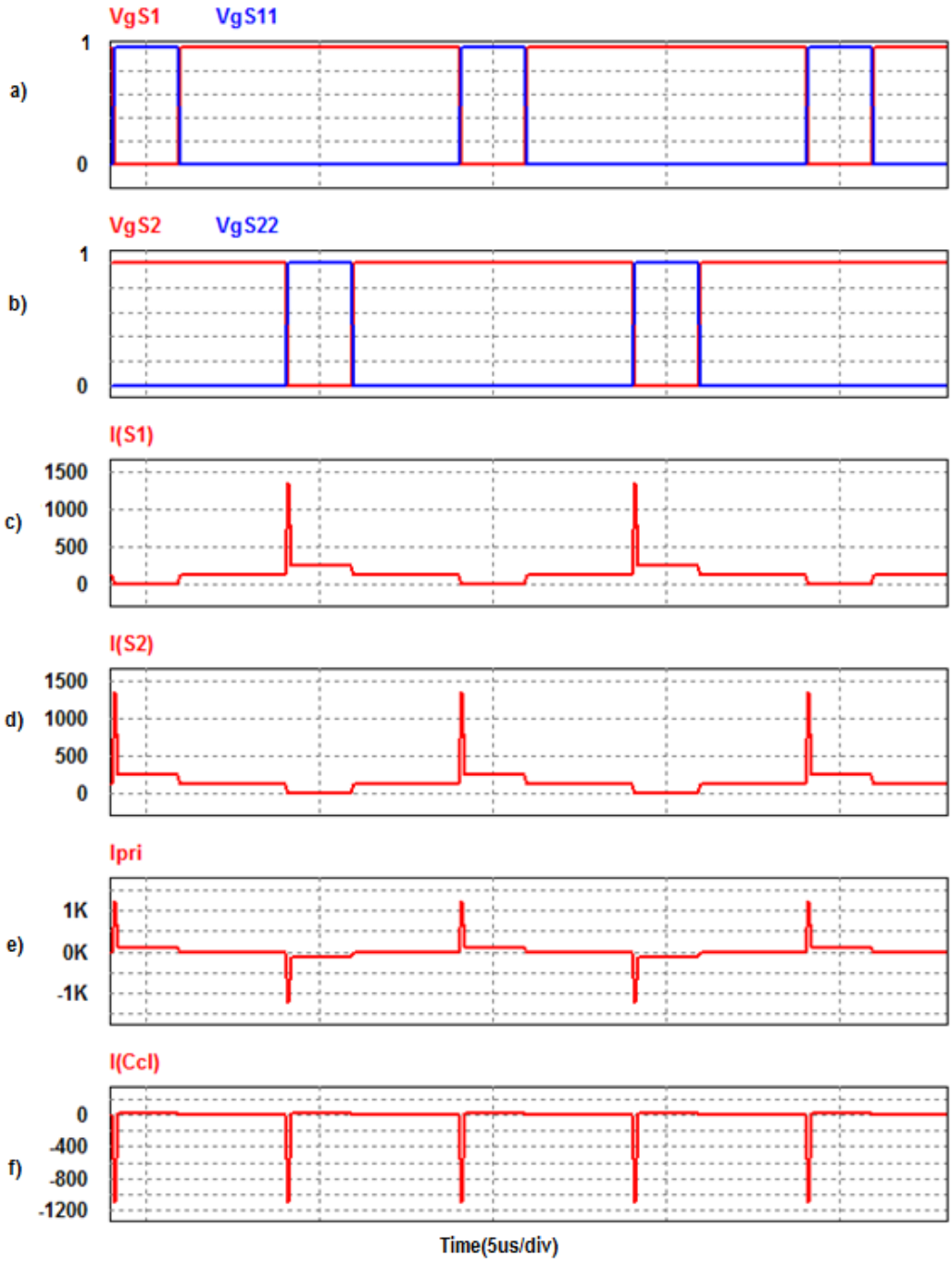


Figure 3.12: Performance of converter without delay time: a) Gating signal for main switch (V_{gS1}) and clamp switch (V_{gS11}), b) Gating signal for main switch (V_{gS2}) and clamp switch (V_{gS22}), c) Current in switch S_1, d) Current in switch S_2, e) Primary side current of transformer (I_{pri}), f) Current in clamp capacitor (I_{Ccl})

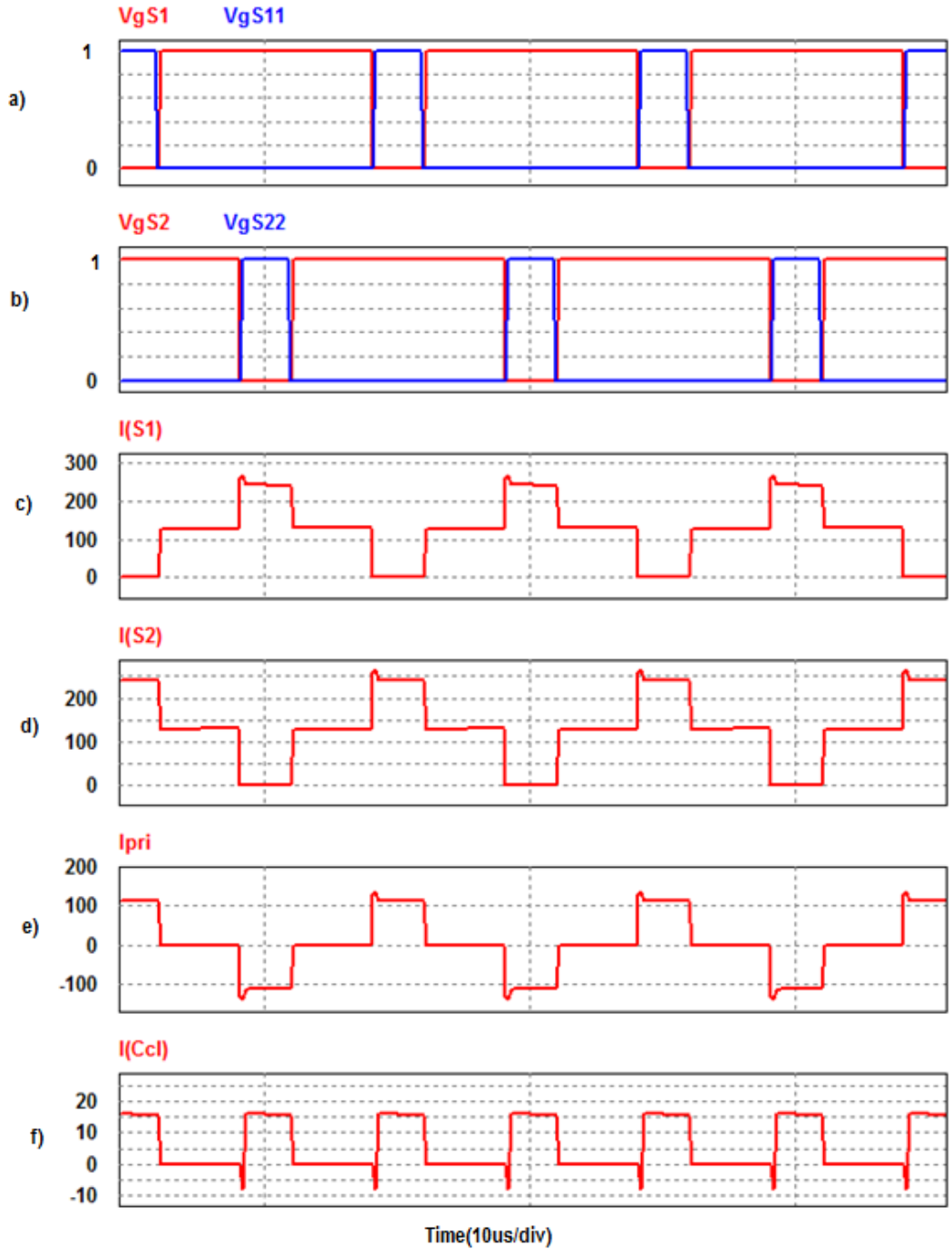


Figure 3.13: Performance of converter with delay time: a) Gating signal for main switch (V_{gS1}) and clamp switch (V_{gS11}), b) Gating signal for main switch (V_{gS2}) and clamp switch (V_{gS22}), c) Current in switch S_1, d) Current in switch S_2, e) Primary side current of transformer (I_{pri}), f) Current in clamp capacitor (I_{Ccl})

3.3.6 Synchronous rectifier

Considering the input current ripple to be negligible,the peak current through one of the diodes of the synchronous rectifier can be given by:

$$I_{dpk} = I_{secpk} = \frac{I_{in}}{2n} = 65A \tag{3.32}$$

where I_{sec} is the secondary side rms current of the transformer.
The rms current of the diode can be calculated as follows:

$$I_{drms} = \sqrt{\frac{1}{3}\frac{(a+\Delta a)^2 + (a-\Delta a)^2 + a^2 - \Delta a^2 \times (1-D)T}{2T}}, \text{where } a = \tfrac{I_{in}}{2n} \tag{3.33}$$

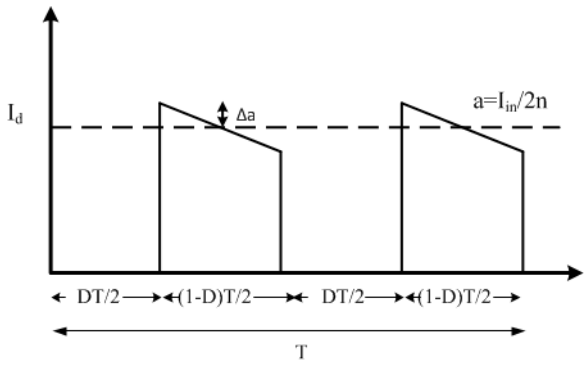


Figure 3.14: Diode current in synchronous rectifier

If we again consider the ripple Δa to be zero;the above equation can be reduced to:

$$I_{drms} = \frac{I_{in}}{2n} \times \sqrt{\frac{1-D}{2}} \tag{3.34}$$

At maximum duty cycle of 0.60, the rms current of a diode is 29A and the voltage across the diode will be equal to the output voltage i.e. 28V. Since two diodes conduct

at the same time, the average forward current in each diode can be given by:

$$I_{dav} = \frac{I_o}{2} = 12.5A \tag{3.35}$$

Therefore, M(B,I)3035S from Vishay [27] with a forward voltage of $Vf = 0.61V$ at 30A can be selected as a diode in the synchronous rectifier. The power dissipation in each diode will be:

$$P_{diss} = I_{dav} \times V_f = 7.6W \tag{3.36}$$

Hence, the total power dissipation of four diodes in synchronous rectifier is 30.5W.

3.3.7 Output capacitor

The value of the output capacitor should be such that the dc output voltage remains constant with minimum amount of ripple. The maximum amount of ripple occurs at the minimum input voltage i.e. when the duty cycle is maximum. Referring to eq.2.6 , we can calculate the value of output capacitor as follows:

$$C_o = \frac{I_o \times D}{\Delta V_o \times f_{sw} \times 2} \tag{3.37}$$

where ΔV_o is the ripple in the output voltage,

f_{sw} is the switching frequency, and

I_o is the output current of the capacitor given by:

$$I_o = \frac{I_{in} \times 1 - D}{2 \times n} \tag{3.38}$$

The desired ripple voltage should be less than 1V; therefore at minimum input

voltage of 2.75V and corresponding duty cycle of 0.6; the value of the output capacitor required is $75\mu F$.

The rms current of the output capacitor can be calculated as :

$$I_{crms} = \sqrt{I_{drms}^2 - I_o^2} = \frac{I_{in}}{2 \times n} \times \sqrt{\frac{D}{1-D}} \times 1 - D = 31.8A \tag{3.39}$$

Hence, the maximum value of equivalent series resistance (ESR) of the capacitor required to keep the ripple voltage less than 1V is:

$$ESR = \frac{\Delta V_o}{I_{crms}} \tag{3.40}$$

From the above equation, the ESR of the capacitor should be less than $30m\Omega$. The selected capacitor is 40HVHZ120M from Suncon [28] with a voltage rating of 40V and capacitance of $120\mu F$ with $16m\Omega$ ESR. Due to high capacitor current, three parallel connected capacitors have been considered in order to reduce the power dissipation in the output capacitor.The total power dissipation is equal to:

$$P_{dis} = I_{crms}^2 \times \frac{ESR}{3} = 5.36W \tag{3.41}$$

Fig. 3.15 shows that the normalized value of ripple current ratio in the output capacitor reduces to zero at duty cycle of 50% because of the two inductor phases. The normalized ripple current ratio of the output capacitor is calculated as follows:

$$\frac{I_{crms} - I_o}{I_o} = \sqrt{\frac{D}{1-D}} - 1 \tag{3.42}$$

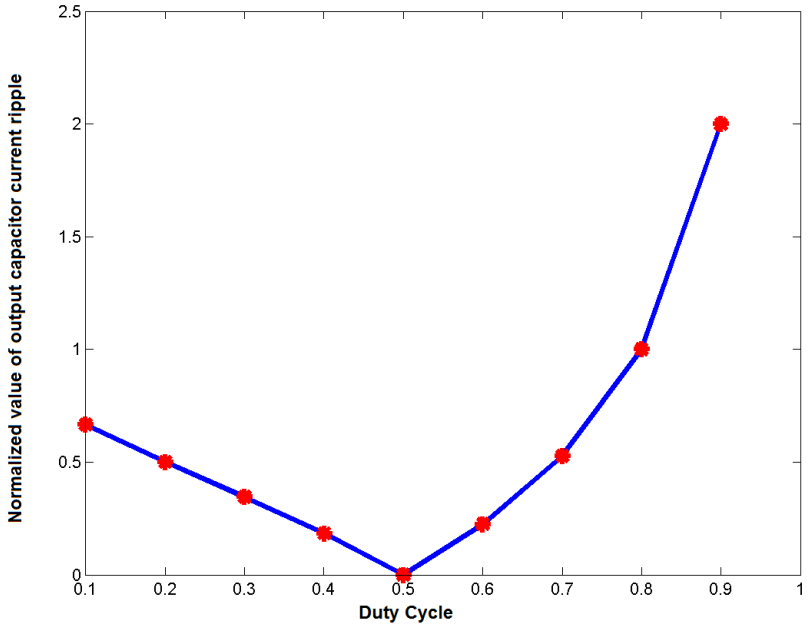


Figure 3.15: Change in ripple current ratio of capacitor w.r.t duty cycle

3.3.8 Input filter

The ripple in the input current can overheat the cells in the LV-AEA. Therefore,there is need to shunt the ripple using an input LC filter. The inductor is used to reduce the amount of ac ripple and the input capacitor keeps the source voltage within a desired range. The value of the input inductor can be calculated using the equation for inductor design given in Chapter 15 of [22] which is as follows:

$$L_{in} = \frac{\Delta V_{in} \times D(1-D)}{\Delta I_{in} \times f_r} \tag{3.43}$$

where ΔV_{in} is the peak to peak ripple voltage in the dc source

ΔI_{in} is the peak to peak source current ripple

f_r is the ripple current frequency

The ripple current frequency is twice the switching frequency. Considering ΔV_{in} to be less than 50mV andΔI_{in} to less than 50mA,the inductor value calculated at minimum voltage operating conditions is $1\mu H$. The value of the input capacitor can be calculated as follows:

$$C_{in} = \frac{\Delta I_{in} \times D}{\Delta V_{in} \times f_r} = 10\mu F \tag{3.44}$$

3.3.9 Efficiency calculation

The total power dissipation in the components of dc-dc converter is presented in the Table 3.5 given below:

Component	**Power Dissipation**
Inductors L_1,L_2	19.3W
Transformer	12W
Main Switches S_1,S_2	24.2W
Clamp Switches S_{11},S_{22}	13W
Synchronous rectifier	30.4W
Output Capacitor	5.36W
Total Power Dissipated, P_{diss}=104.26W	

Table 3.5: Theoretical efficiency calculation

The theorectical efficiency(η) can be calculated as:

$$\eta = \frac{P_o}{P_o + P_{diss}} \times 100 = \frac{700}{804.3} \times 100 = 87\% \tag{3.45}$$

3.4 Building block controller design

3.4.1 Output Voltage Control

Each building block in LV-AEA needs to provide a regulated output voltage of 28V within a reasonable settling time. For this, a PI controller can be designed that changes the duty cycle of the switches depending upon the difference between the reference voltage and the actual output voltage obtained. The control can be designed based on the transfer function for the output voltage with respect to the duty cycle which is given as:

$$\frac{\hat{V_o}}{\hat{D}} = \frac{\frac{4nV_{in}}{(1-D)^2} \times (1 - \frac{2sn^2L}{R_o(1-D)^2})}{\frac{2s^2n^2LC_o}{(1-D)^2)} + \frac{2sn^2LC_o}{R_o(1-D)^2} + 1} \tag{3.46}$$

The above given transfer function depicts that the system is not a minimum phase system and contains a right half plane zero (RHP) which makes the system prone to instability easily. The presence of RHP zero increases the gain but decreases the phase margin substantially. The response time of the PI controller is decreased due to the presenceof RHP zero. When the error signal is more than the carrier signal, the PI controller turns off one of the main switches in order to compensate the voltage error and feed the load. But due to the RHP zero, output voltage decreases before it reaches its desired value again. Thus, it becomes important to eliminate this RHP zero or change it into left hand plane (LHP) zero.

Some of the methods to alleviate this issue have been mentioned in [29],[30].[29] lists few methods for eliminating the effects of RHP zero. One of the methods is to operate the converter in discontinuous mode of operation (DCM) which is not possibe with the topology used in this thesis. Another method suggested is to either decrease

the inductor value or increase the value of the output resistor such that:

$$T < \frac{2L}{R_o D(1-D)^2} \tag{3.47}$$

where T the time period of switching frequency.

This method too does not solve our problem as the minimum inductor value required in this case would be $0.53\mu H$ which makes the inductor current go discontinuous. [30] describes a lead compensation method where the ESR of the output capacitor is taken into account to change the RHP zero into LHP zero. From [30],the modified transfer function voltage to duty cycle transfer function can be written as:

$$\frac{\hat{V_o}}{\hat{D}} = \frac{\frac{4nV_{in}}{(1-D)^2} \times (1 + \frac{2n^2 s(LR_o R_{esr} C_o D)}{R_o(1-D)^2})}{\frac{2s^2 n^2 LC_o}{(1-D)^2)} + \frac{2sn^2 LC_o}{R_o(1-D)^2} + 1} \tag{3.48}$$

provided that

$$R_{esr} C_o > \frac{L}{R_o(1-D)}$$

Even in this case the ESR value required for the capacitor is too large and will result in large output voltage ripple.Further analysis of the converter for boundary mode of operation need to be done to understand and resolve this issue. For the controller design, it was assumed that the RHP zero has been shifted to left hand plane which gave intial proportional (P) and integral (I) values to work with. These values were then tuned after looking at the transient response of the converter from PSIM simulation model. The transfer function of the PI controller obtained is :

$$C(s) = 0.005 + \frac{5}{s}. \tag{3.49}$$

The integrator time constant used in the PI block of PSIM is equal to $\frac{Kp}{Ki} = 0.001$.Fig.3.16 depicts the transient response of the system which shows that the output voltage of 28V is achieved within settling time of 0.2 seconds.

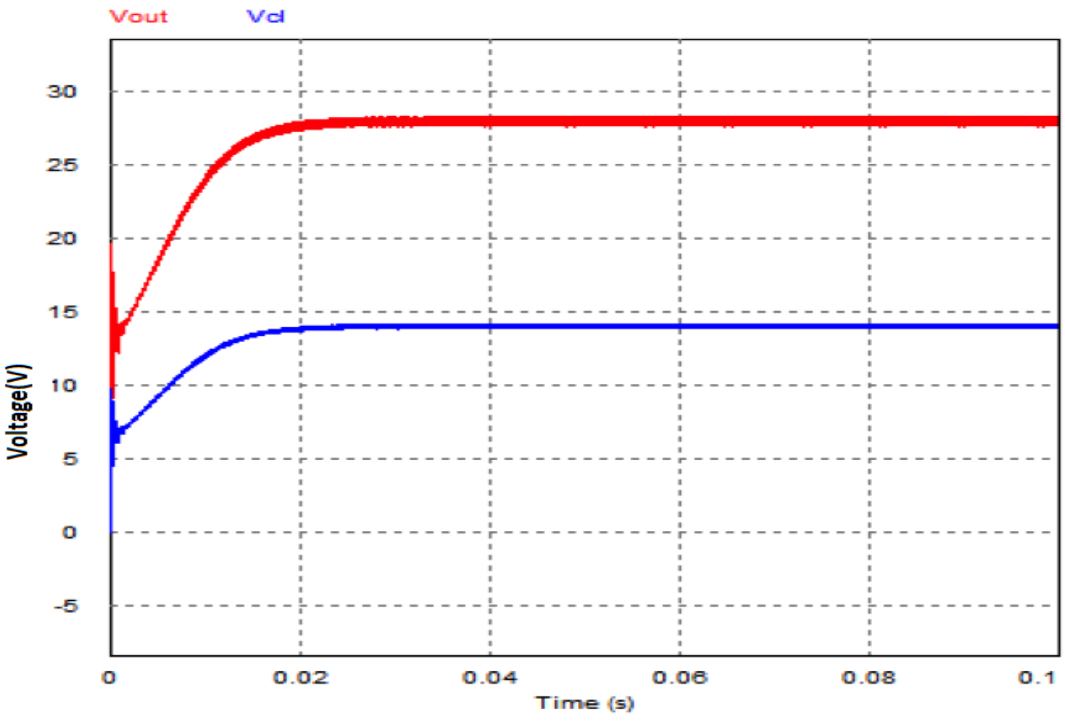


Figure 3.16: Voltage of clamped capacitor V_{cl} and regulated output voltage V_o

3.4.2 Simulation results of the building block operation

The PSIM simulation model of the deisgned dual inductor current fed push pull converter with the closed loop output voltage control is shown in Fig. 3.17. Simulations were conducted for two different operating cell voltages: a) minimum cell voltage of 2.75V and b) nominal cell voltage of 3.7V. For the purpose of simulations, the following things were taken into consideration:

1. ESU designed using selected Li-ion cell model with five cells in parallel was used as an input to the dc-dc converter.

2. The series resistance R_{dcr} used for input inductors was equal to the R_{dcr} of the four parallel connected inductors.

3. Equivalent switch model with four parallel connected MOSFETs was considered for the main switches S_1 and S_2.

4. The value of output capacitor and its ESR was taken to be equal to the three parallel connected capacitors.

5. Non-ideal transformer with copper losses and leakage inductance was used. Core losses of the transformer were ignored during effeciency calculation.

6. Actual thermal module of the selected diodes was used for the synchronous rectifier.

7. The input LC filter was assumed to be lossless.

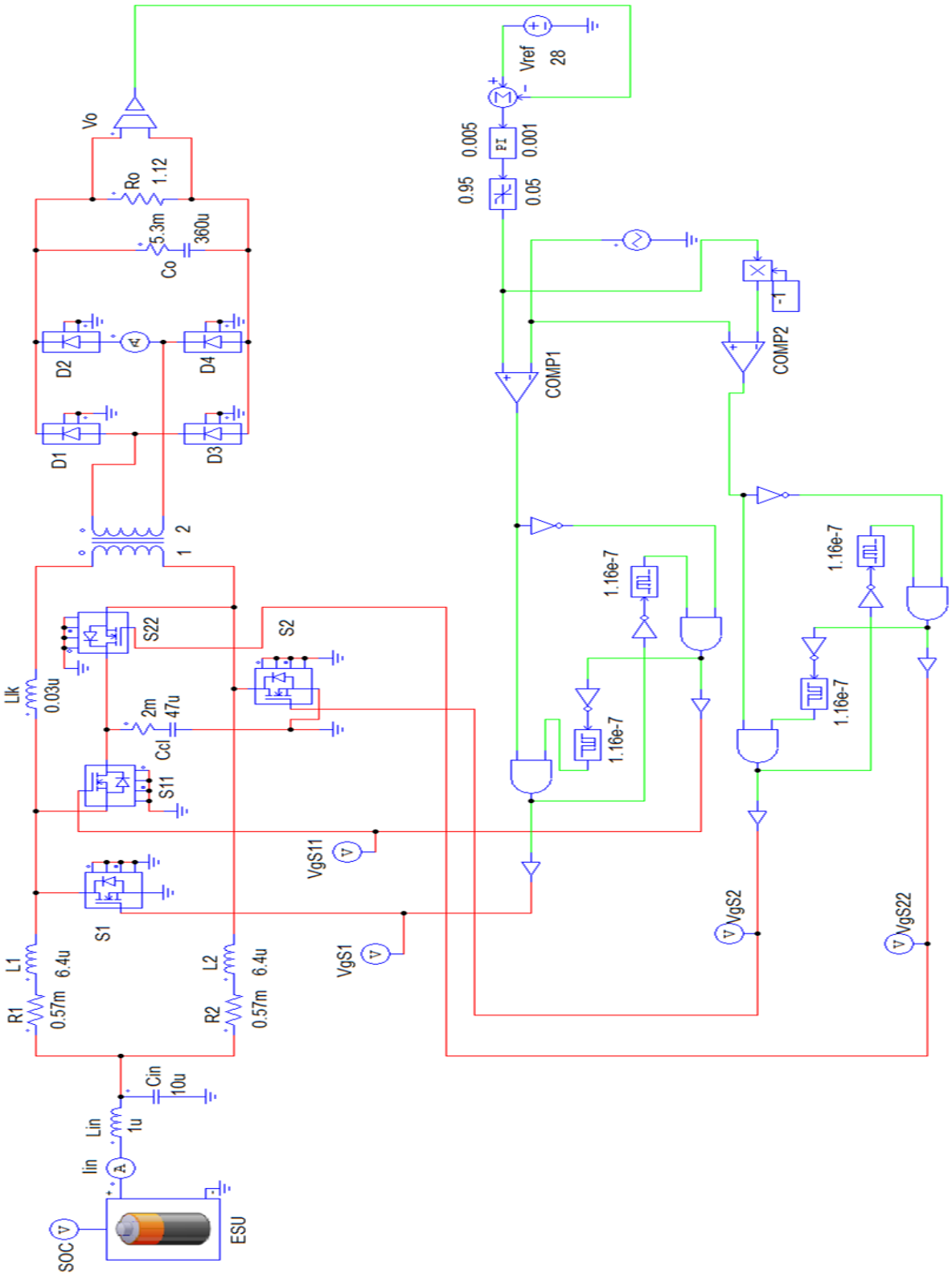


Figure 3.17: PSIM model of the building block with output voltage control

Table 3.6 and Table 3.7 show the efficiency report of the dc-dc converter for input cell voltages of 2.75V and 3.7V respectively.

Component	Current (peak value in A)	Current (rms value in A)	Power Dissipation (in W)
Inductors L_1,L_2	154.7	153	26.7
Main Switches S_1,S_2	429	180.6	43.8
Clamp Switches S_{11},S_{22}	136.7	27.62	23.74
Transformer	273.2 (pri)	100(pri)	11.25
Synchronous rectifier	137.4	35.3	25.5
Output Capacitor	110.5	42.7	9.66
Total Power Dissipated			140.6
Efficiency			83.3%

Table 3.6: Efficiency report of the dc-dc converter in each building block at operating voltage of 2.75V

Component	Current (peak value in A)	Current (rms value in A)	Power Dissipation (in W)
Inductors L_1,L_2	110.2	108.26	13.4
Main Switches S_1,S_2	303.3	134.4	29.14
Clamp Switches S_{11},S_{22}	101.1	27.64	17.55
Transformer	196.4 (pri)	84.56(pri)	10.03
Synchronous rectifier	95.5	29.59	22.54
Output Capacitor	70	33.17	6.83
Total Power Dissipated			99.86
Efficiency			87.5%

Table 3.7: Efficiency report of the dc-dc converter in each building block at operating voltage of 3.7V

The simulation results for the designed dc-dc converter for the operating condition (2.75V,700W) are presented in Fig. 3.18 and Fig. 3.19. And the results for the operating condition (3.7V,700W) are given in Fig. 3.20 and Fig. 3.21. The following conclusions were drawn from the simulation analysis:

1. The efficiency of the dc-dc converter obtained is not very high due to the high discharge current from the ESU. Considering few more cells in series can help improve the efficiency or more parallel connected building blocks can be considered to reduce the current stress in each building block. The difference in the calculated theoretical efficiency and simulated efficiency report is due to the fact that effect of leakage inductance was not considered while doing the converter analysis.

2. Even though the clamp circuit helps in avoiding voltage transients across the switches and reduces the conduction losses, it also contributes to a significant amount of switching losses.

3. Alot of the power dissipation occurs in the MOSFETs and the diodes. Replacing the MOSFETs and diodes with SiC power devices with low R_{DSon} can help in improving the efficiency.

4. The maximum output voltage ripple is 1.2V and the capacitor ripple current is 1A. The value of the voltage ripple is high for a 28V system and therefore in order to reduce the voltage ripple even more, capacitors with very low ESR connected in parallel will be required. For this, use of tantalum capacitors with low ESR can be considered.

5. Need for parallel connection of components increases the weight of LV-AEA. Therefore, planar magnetics for inductor and transformer design, SiC power devices for MOSFETs and diodes need to be considered for the design of LV-AEA.

6. Due to large amount of heat dissipation, advanced thermal management will be required in such a system.

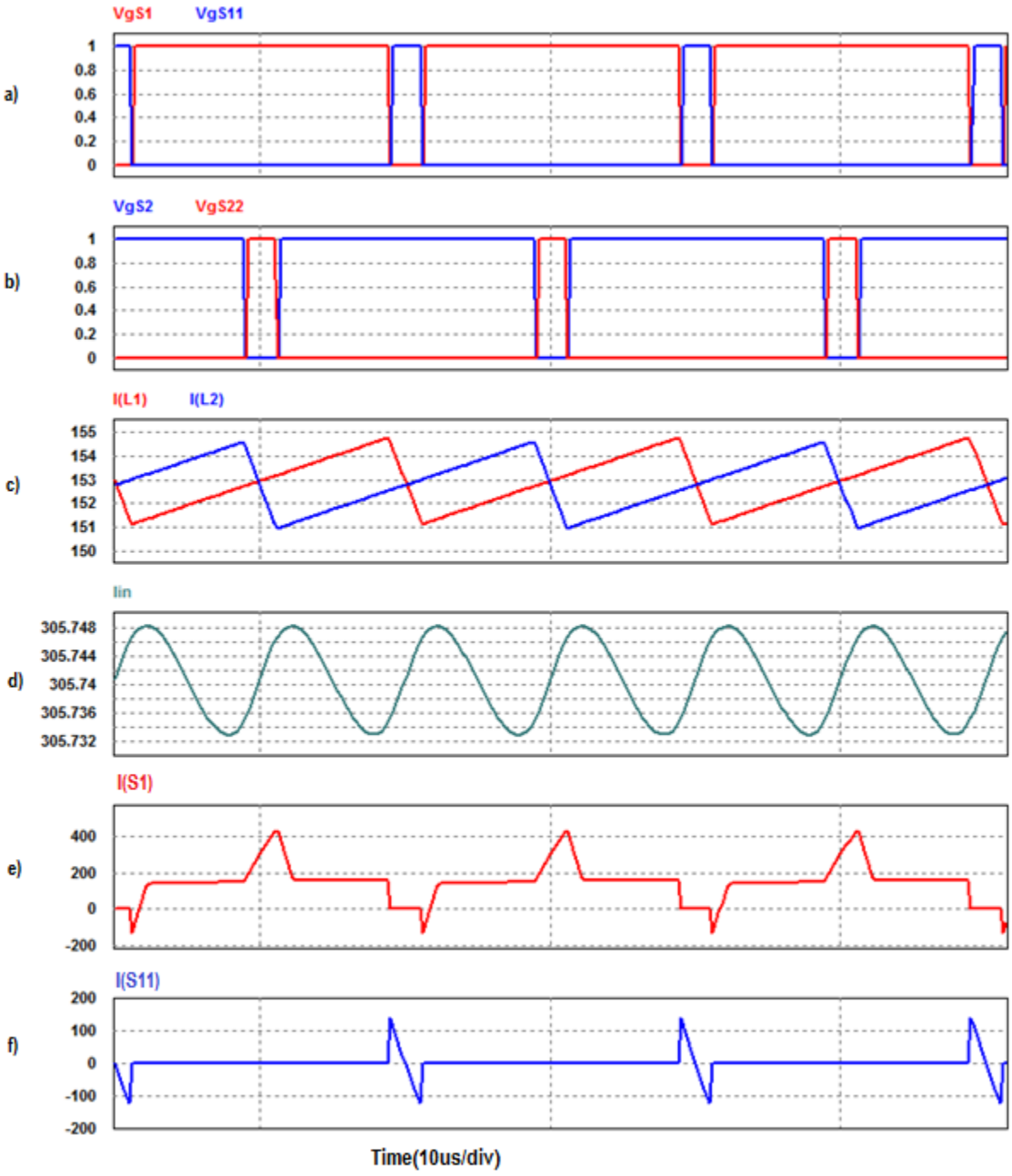


Figure 3.18: Building block operation at $V_{in} = 2.75V$ and $P_{out} = 700W$: a) Gating signals for main switch S_1 and clamp switch S_11, b) Gating signals for main switch S_2 and clamp switch S_{22}, c) Inductor currents I_{L1} and I_{L2}, d) Input current I_{in}, e) Current in main switch S_1, f) Current in clamp switch S_{11}

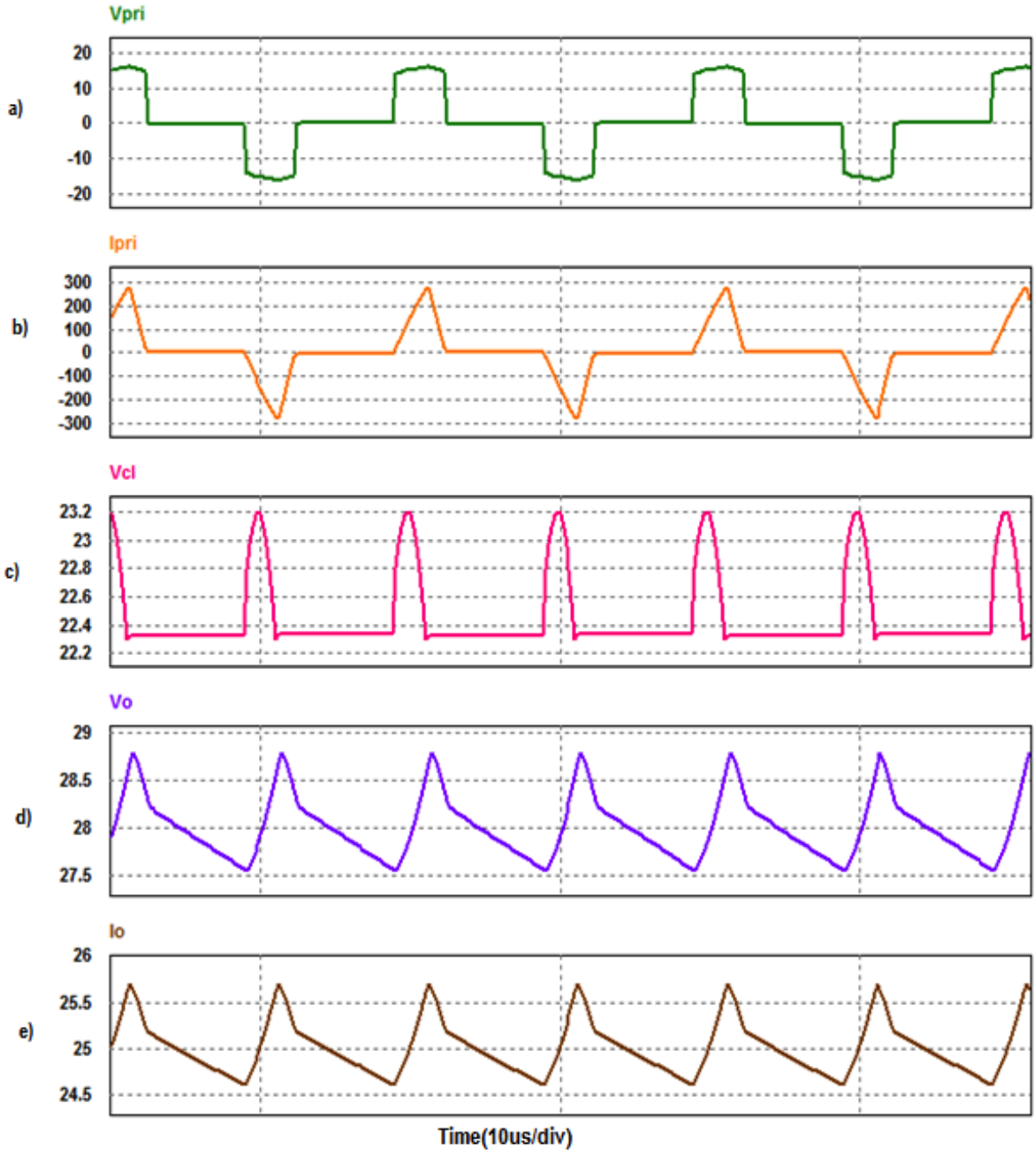


Figure 3.19: Building block performance at Vin=2.75V and Pout=700W : a) Primary side voltage of transformer V_{pri}, b)Primary current of transformer I_{pri}, c) Clamped capacitor voltage V_{cl}, d)Output voltage V_o, and e) Output current I_o

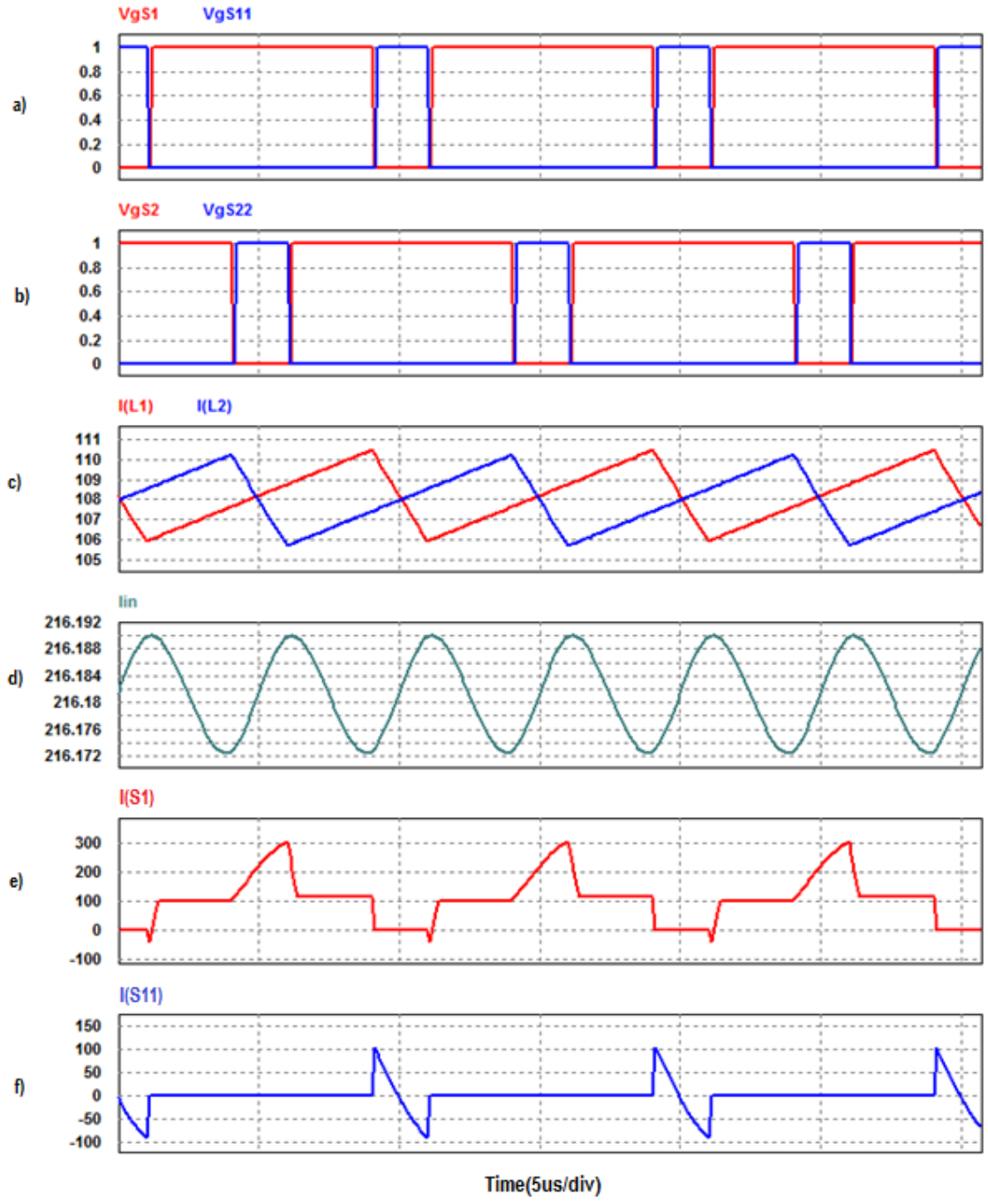


Figure 3.20: Building block operation at $V_{in} = 3.7V$ and $P_{out} = 700W$: a) Gating signals for main switch S_1 and clamp switch S_{11}, b) Gating signals for main switch S_2 and clamp switch S_{22}, c) Inductor currents I_{L1} and I_{L2}, d) Input current I_{in}, e) Current in main switch S_1, f) Current in clamp switch S_{11}

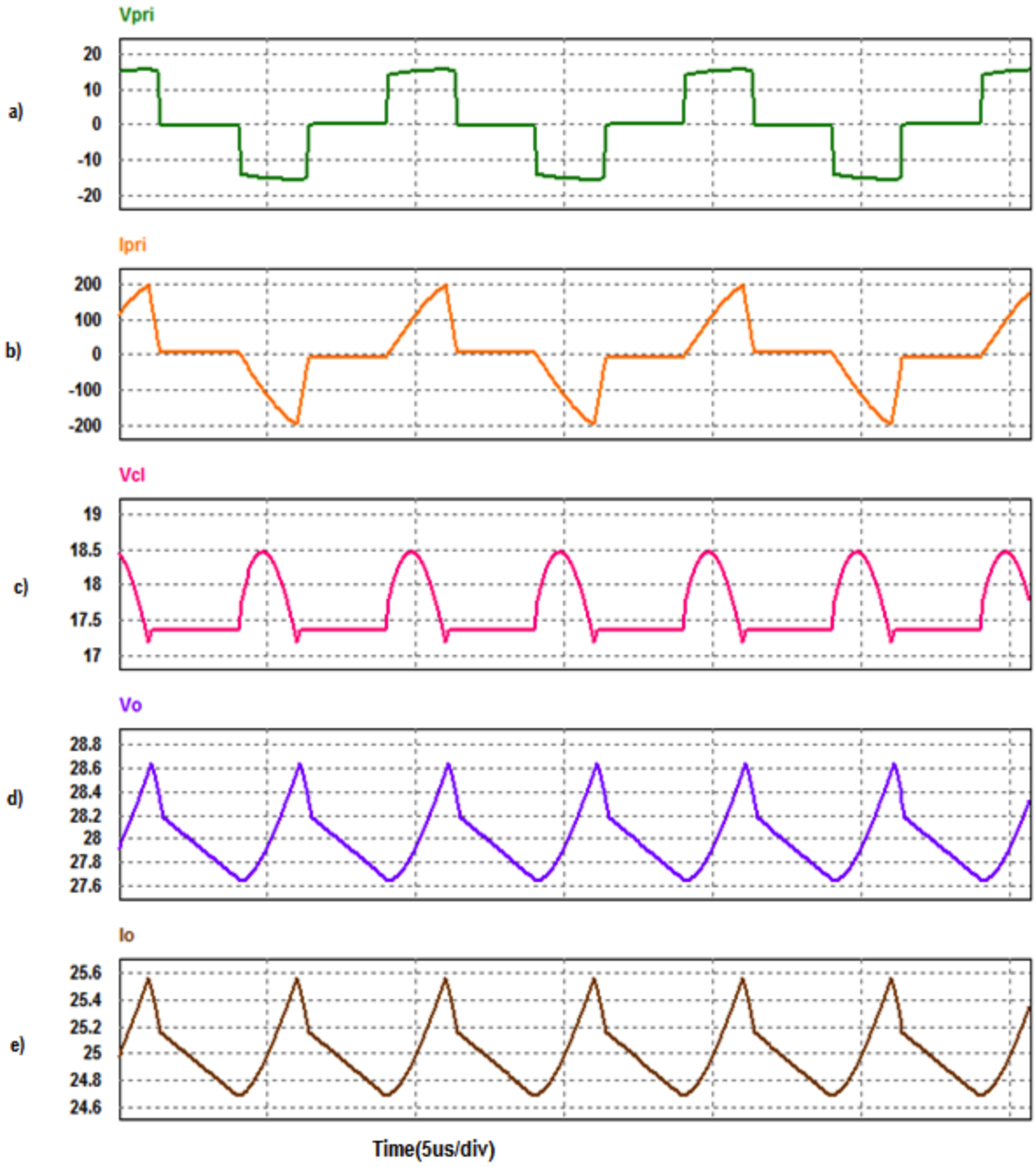


Figure 3.21: Building block performance at Vin=2.75V and Pout=700W : a) Primary side voltage of transformer V_{pri}, b)Primary current of transformer I_{pri}, c) Clamped capacitor voltage V_{cl}, d)Output voltage V_o, and e) Output current I_o

3.4.3 Over-voltage and under-voltage protection

Fig. 3.23 shows the PSIM model of the building block controller with over-voltage and under-voltage protection. The measured input Voltage V_{in} is fed as an input to the over-voltage comparator as well as the under-voltage comparator. The maximum and minimum voltage limit for the selected li-ion cell GS YUASA-LVP10 [21] is 4V and 2.75V respectively. Considering hysteresis of 100mV to avoid ringing operation, the overvoltage and under voltage limits of the comparators are set as 4.1V and 2.65V. When the cell voltage rises or drops below the upper limit or the lower limit, the main switches S_1 and S_2 are turned off while their clamp/auxiliary switches get turned on. The remaining energy in the inductors is dissipated into the clamped capacitor. In addition to the control protection, a reverse current protection using a diode or a switch at the input can be added. The added switch can also serve the purpose of isolating the failed block from rest of the working building blocks. Fig. 3.22 shows the controller operation when the cell voltage drops from its minimum cut off value of 2.75V to 2.5V.

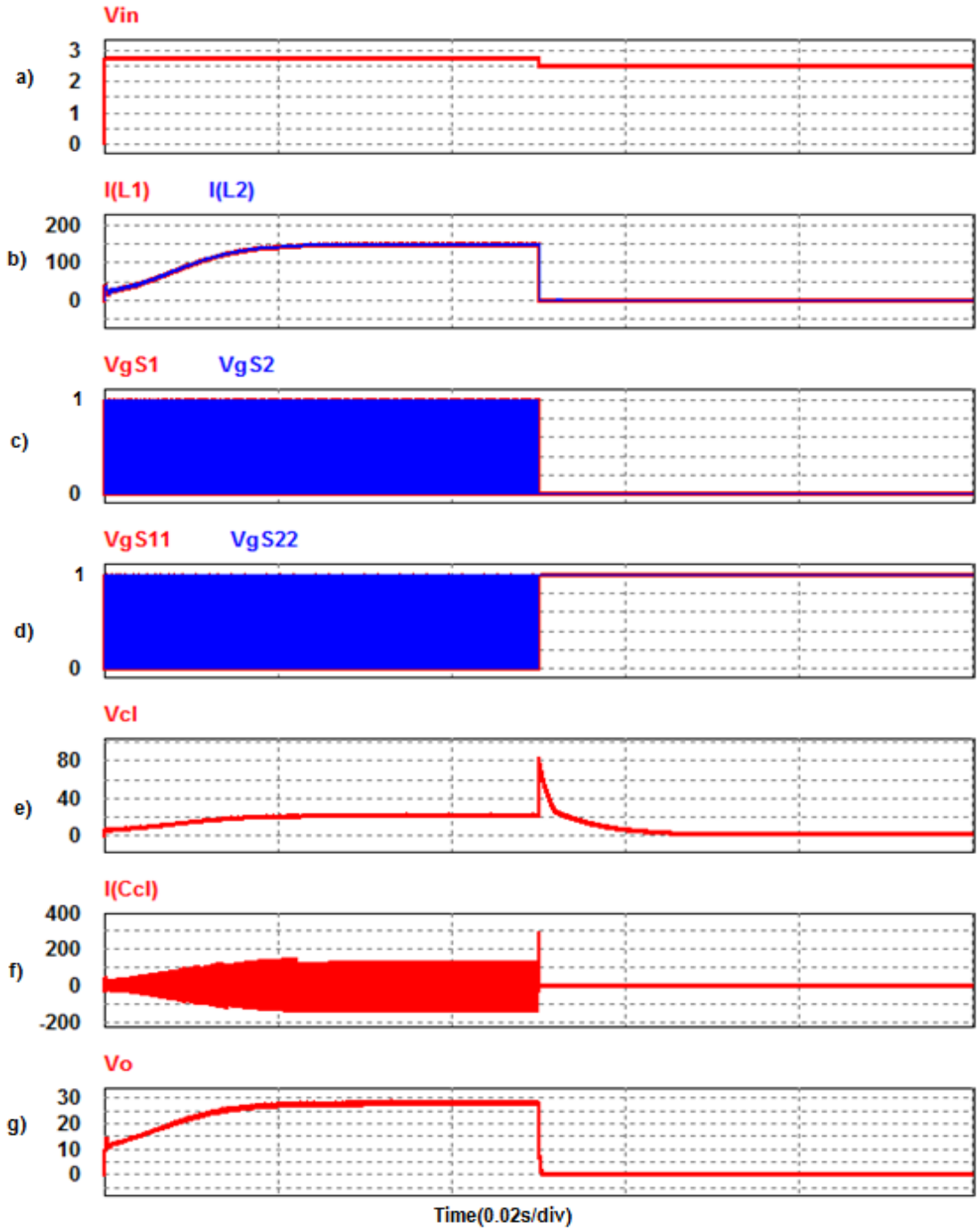


Figure 3.22: Building block performance when input voltage drops from 2.75V to 2.5V: a) Input Voltage,V_{in}, b) Currents in inductors L_1 and L_2, c) Gating signals for main switches S_1 and S_2, d) Gating signals for clamp switches $S_1 1$ and $S_2 2$, e) Clamped capacitor voltage, V_{cl}, f) Current in clamp capacitor, I_{Ccl}, g) Output Voltage, V_o

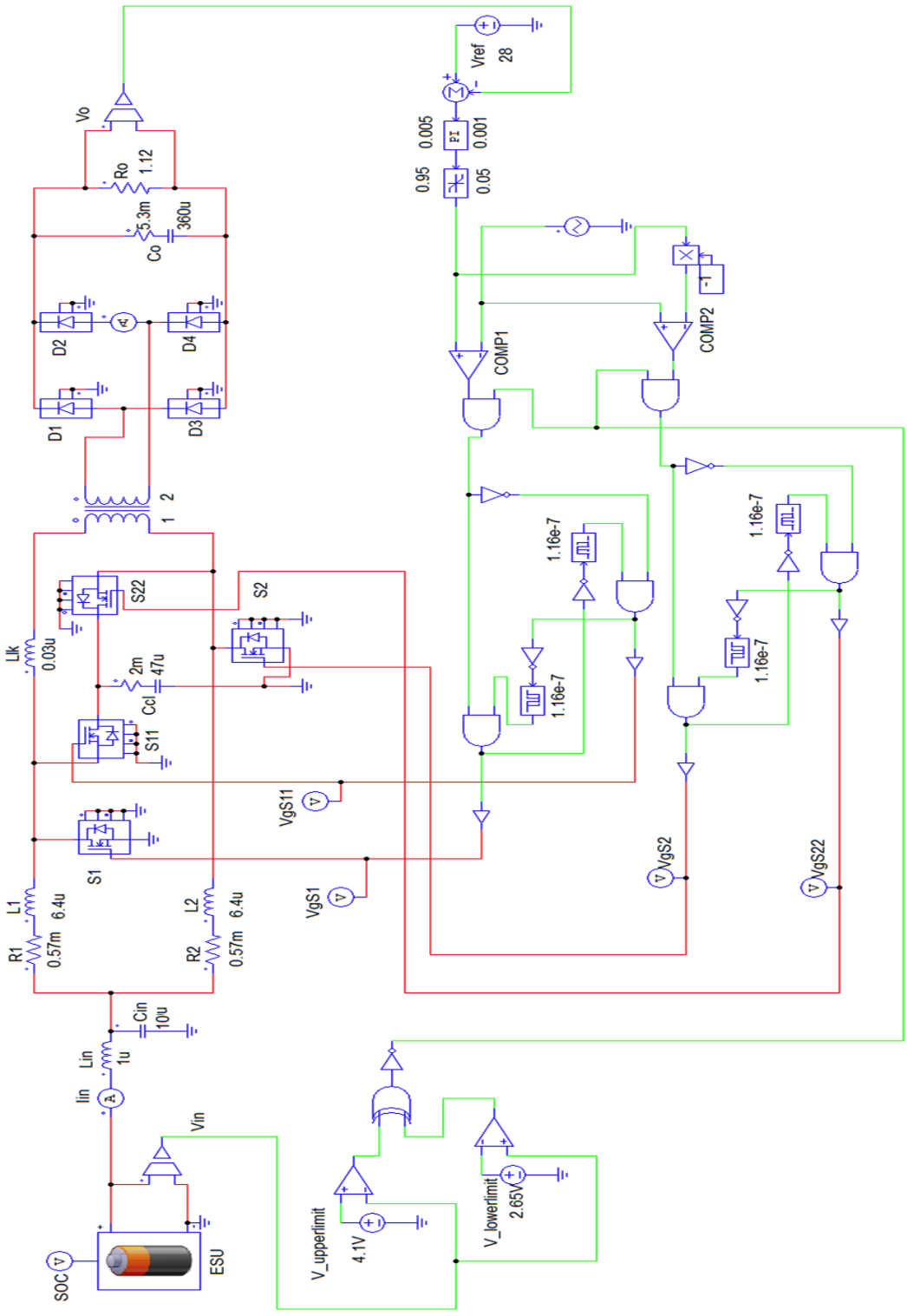


Figure 3.23: PSIM model of building block with output voltage control and overvoltage and undervoltage protection

3.4.4 Overcurrent protection

For the overcurrent control, similar protection loop as voltage protection loop can be implemented. The output of both the voltage protection loop and current protection loop can be summed together. If either of the voltage or current values go out of limit,the protective function loops will start working and stop the operation of the converter by switching off the main MOSFETs. The only difference will be the reference value for current comparators. The inductor currents for discharge protection can be measured using the series connected resistor and the voltage drop across each inductor will act as a reference value for the comparators.

3.5 AEA controller

3.5.1 Synchronization of the building blocks

For the design of the AEA controller, it is important to ensure that the building blocks work in a synchronized manner to generate the required output power. For this, we need to look at the interleaving of gating signals of all the blocks. One of the methods is to synchronize the gating patterns by phase shifting them by $\frac{180^\circ}{N}$ with respect to one of the blocks (master block) where N is the total number of building blocks. For example, if two blocks are connected together, the gating signals for the second block will be phase shifted by 90° with respect to the first block. However, the switches operate with 180° phase difference from eachother within the block. In our case, since 10 building blocks are connected in parallel,the phase shift between the blocks will be 18°. The interleaving pattern of gating signals and inductor currents of two synchronized blocks is shown in Fig.3.24.

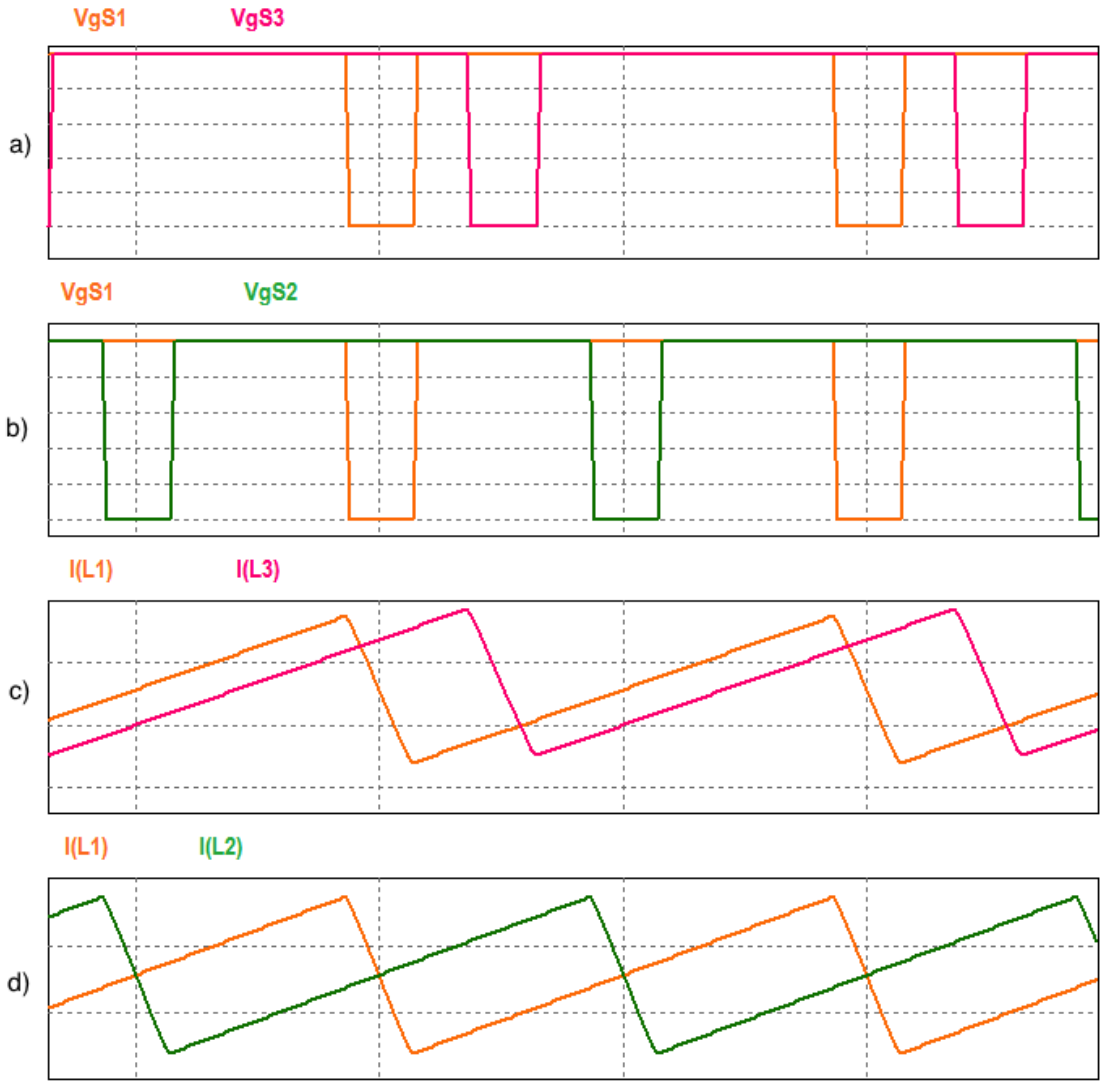


Figure 3.24: Synchronization between two blocks : a) Gating signals of one block w.r.t the other, b) Gating signals of the switches of each building block, c) Corresponding inductor currents of interleaved blocks with 90° phase shift, d) Inductor currents in each block working with 180° phase difference from one another

3.5.2 Load sharing controller

Equal load sharing can be achieved by ensuring that the output voltage and output current are same from each building block. Since the building block (BB) controller already provides a regulated voltage, the AEA load controller has to ensure that the current is shared equally between the building blocks.Various methods have been proposed in literature for this[31–33]. The method used for LV-AEA is active current sharing[31–33] in which the current from each building block is summed up and averaged.The average current can be given by:

$$I_{av} = \frac{I_{o(N-(N-1))} + I_{o(N-(N-2))} + I_{o(N-(N-3)} + I_{o(N-(N-5))} + \ldots\ldots\ldots\ldots + I_{o(N)}}{N} \quad (3.50)$$

where N is the number of building blocks and $I_{o(N)}$ is the output current from Nth block.

This average current of all the building blocks is then compared with the individual output current of each building block. The error generated is then compensated and the reference value is added to the error amplifier of the voltage control loop of the BB controller in each building block. To do this, communication between different building blocks is necessary which is established using the common DC bus. The parallel connection is established using the inter-phase inductor L_{out} and a bus capacitor C_{bout}.The value of these components can be calculated as follows:

$$L_{ob} = \frac{V_o}{\Delta I_o} \times \frac{1-D}{f_{sw} \times 2 \times n} = 10\mu H \quad (3.51)$$

where $\Delta I_o = \frac{\Delta I_{in} \times (1-D)}{2n}$ and I_{in} is taken as1% of the input current of 259.7A

The value of the output bus capacitor can be taken as same as the output capcitor for each block.

$$C_{bo} = \frac{I_o \times D}{\Delta V_o \times f_{sw} \times 2} = 100\mu F \tag{3.52}$$

Since the rate of change in output current is equal to the change in inductor current I_L; we can use the transfer function of inductor current w.r.t duty cycle to get the current compensator values. By referring to eq. 2.37 ,the transfer function of the inductor current with respect to duty cycle is given as:

$$\frac{\hat{I_L}}{\hat{D}} = \frac{\frac{4n^2V_{in}}{R(1-D)^2} \times (sC_oR_o + 2)}{\frac{2s^2n^2LC_o}{(1-D)^2)} + \frac{2sn^2LC_o}{R_o(1-D)^2} + 1} \tag{3.53}$$

The current compensator designed is given by:

$$C(s) = Kp + \frac{Ki}{s} = 0.003 + \frac{1}{s} \tag{3.54}$$

and the integrator time constant is $\frac{Kp}{Ki} = 0.003$.

Fig.3.25 shows blode plot of current compensator with infinite gain margin and 94.9° the phase margin at bandwidth of 3.2kHz.

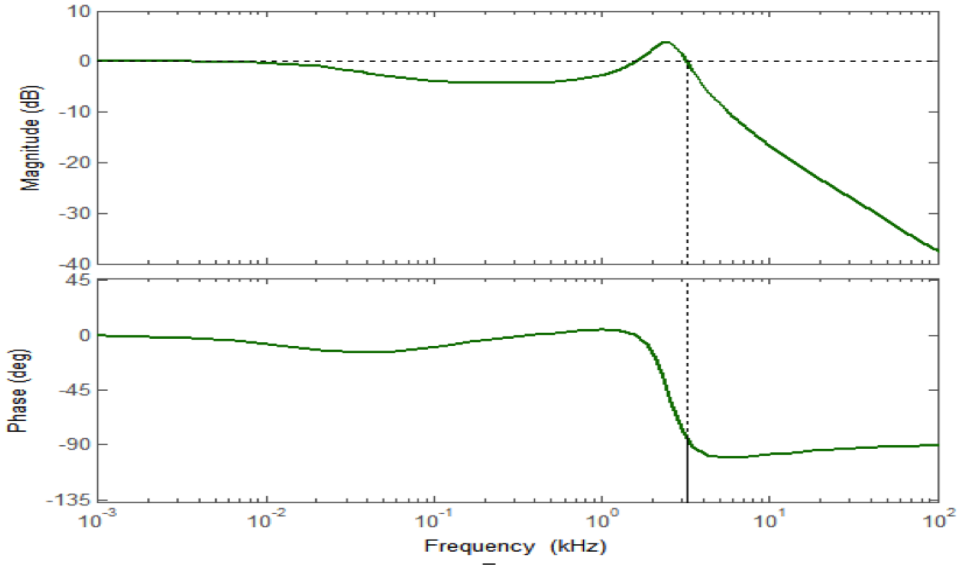


Figure 3.25: Bode plot for current compensator

3.5.3 Simulation results for the load sharing controller

Fig. 3.26 shows two building blocks of LV-AEA working in parallel with current sharing control. The output currents I_{ob1} and I_{ob2} from both the blocks are measured and compared against sum of their average value. The compensted current references I_{ref1} and I_{ref2} are added to the error emplifier of their corresponding building block (BB) controller. In this manner, ten building blocks were connected in parallel to verify the operation of LV-AEA with load controller. Fig.3.27 provides the simulated results of the overall operation of ten building blocks working in a synchronized manner to provide output power of 7kW with each block providing 700W under battery operating condition of 2.75V (ideal components used for the converter for ease of simulation).

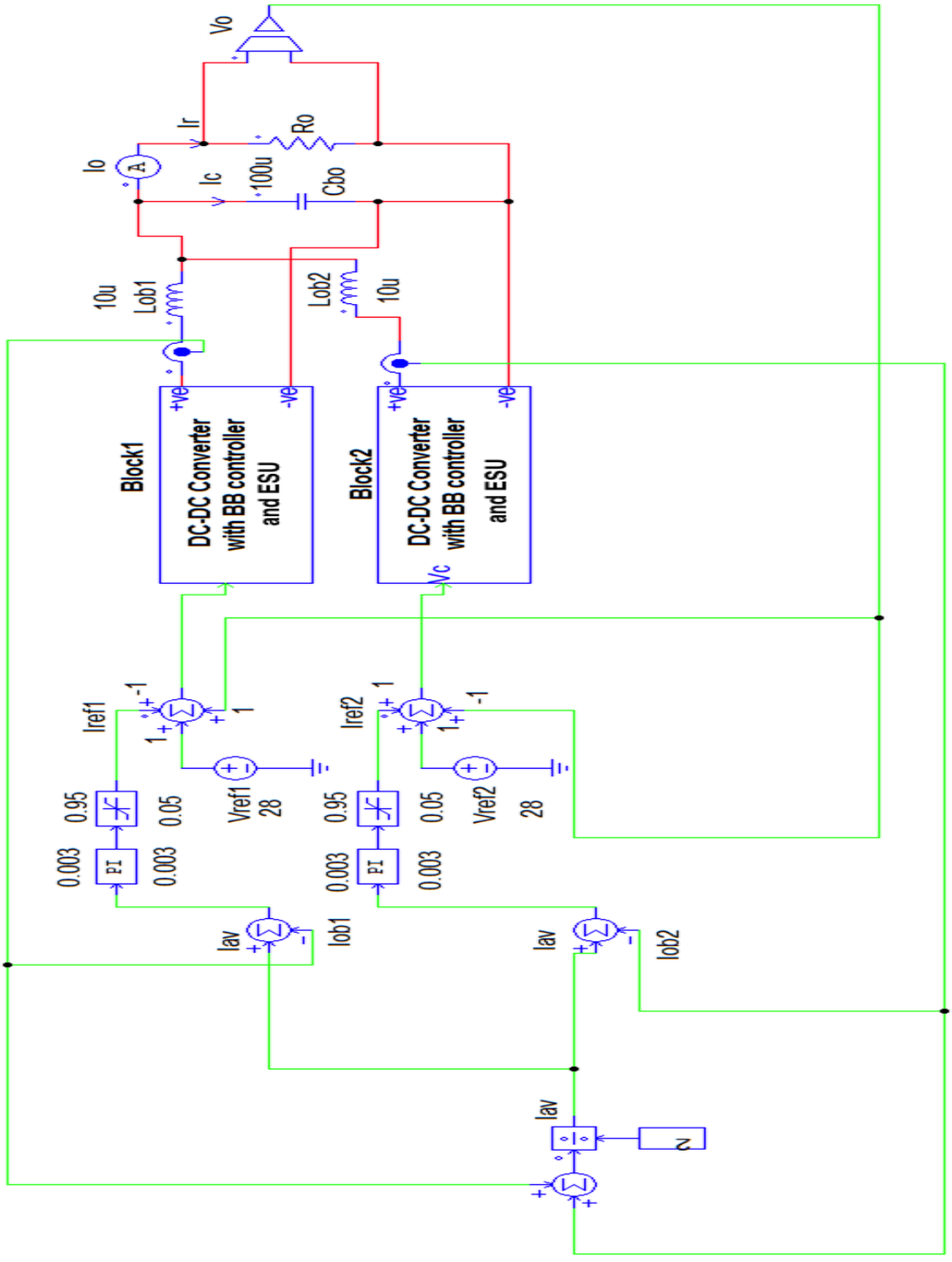


Figure 3.26: PSIM model of two building blocks working in parallel with load sharing

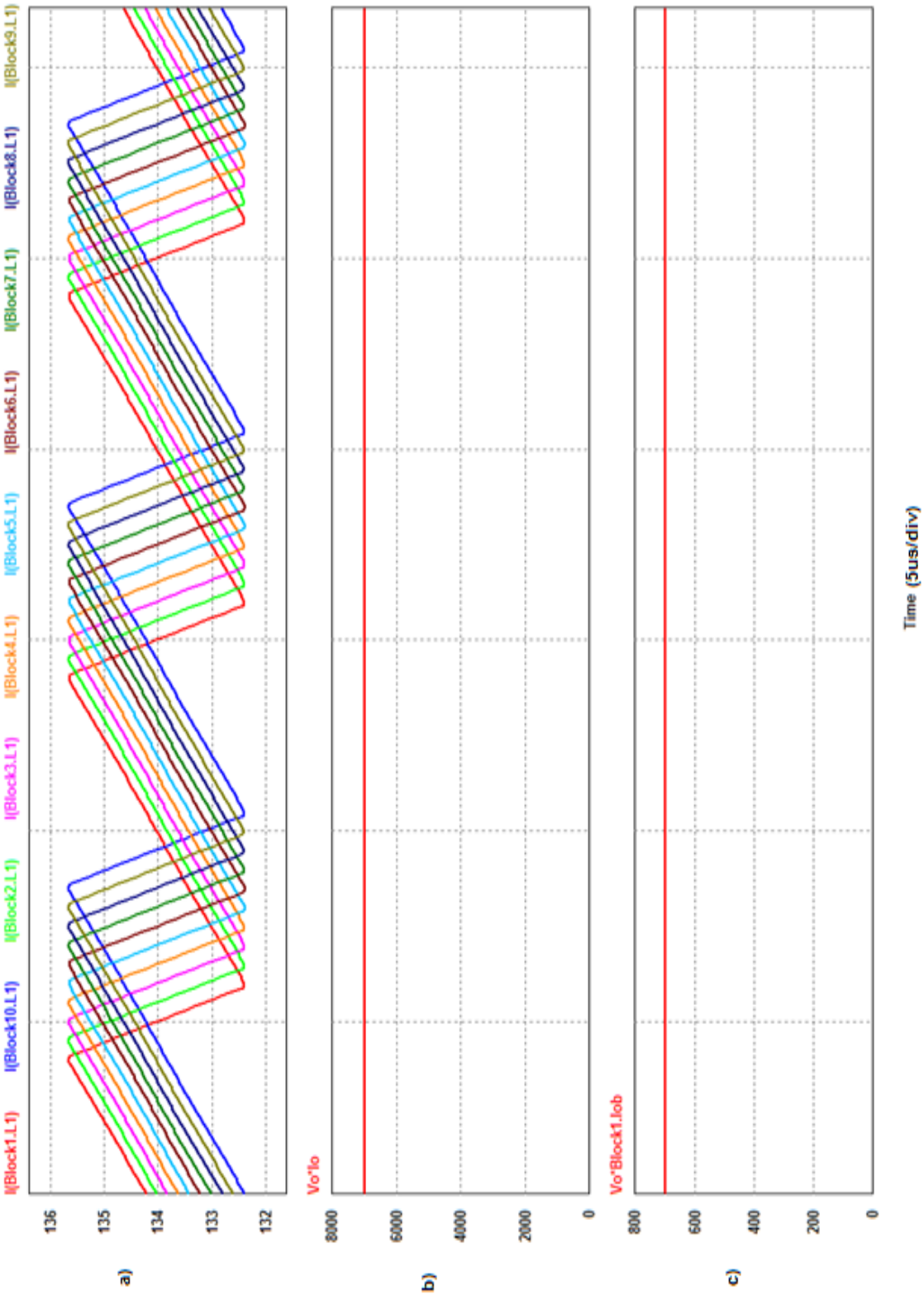


Figure 3.27: 10 building blocks working in parallel: a) Current in single inductor of all the building blocks, b) Total output power obtained, c) Total output power from each building block

The load controller was also analyzed for two modes of operation:

1. Normal Mode

   Fig.3.28 shows the working of the LV-AEA consisiting of two building blocks in the normal mode of operation. In this mode both the blocks share the power equally.The inductor currents in each block are phase shifted by 180° and the phase difference between the inductor currents of both the blocks is 90°.

2. Fault Mode

   Fig.3.29 represents the fault mode of operation of the LV-AEA when one out of the two block stops working. In this situation, full load is supplied by the other working block.

Furthermore, simulations were conducted for analyzing equal power sharing in a unit made of three building blocks (lower number of blocks selected just for the sake of simplifying the task of simulation) with two of the building blocks having a turn's ratio of 2 while the third ones turns ratio is 3 as shown in Fig.3.30. The load of LV-AEA was increased from 700W to 1.4kW in each building block. It can be seen that all the blocks respond to the increased power requirement and also share the power equally even in case of load variation and different working conditions.

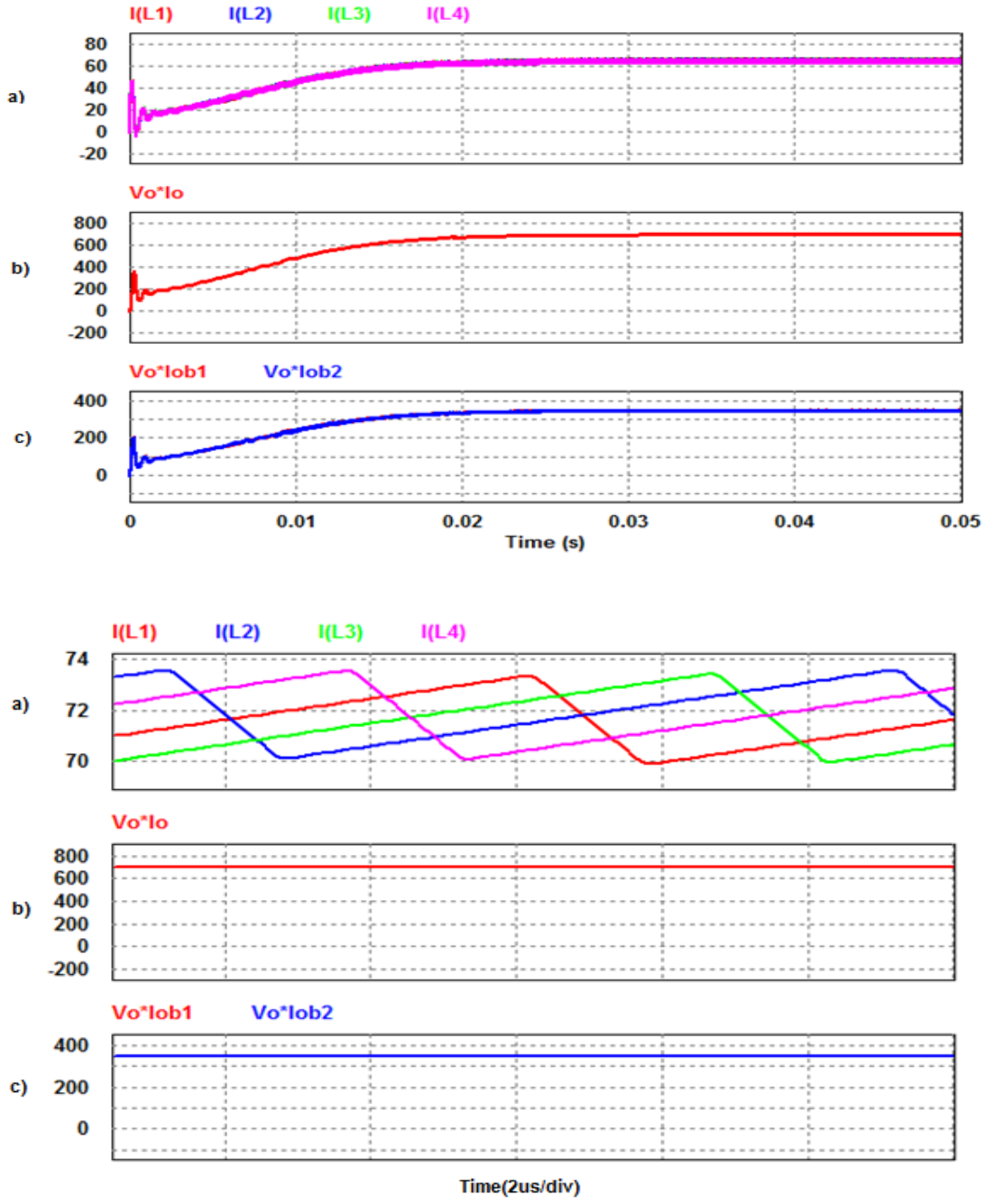


Figure 3.28: Two building blocks sharing equal power of 350W a) Inductor currents I_{L1},I_{L2} from block 1, Inductor currents I_{L3},I_{L4} from block 2,b)Total output power, and c) Output power from each building block

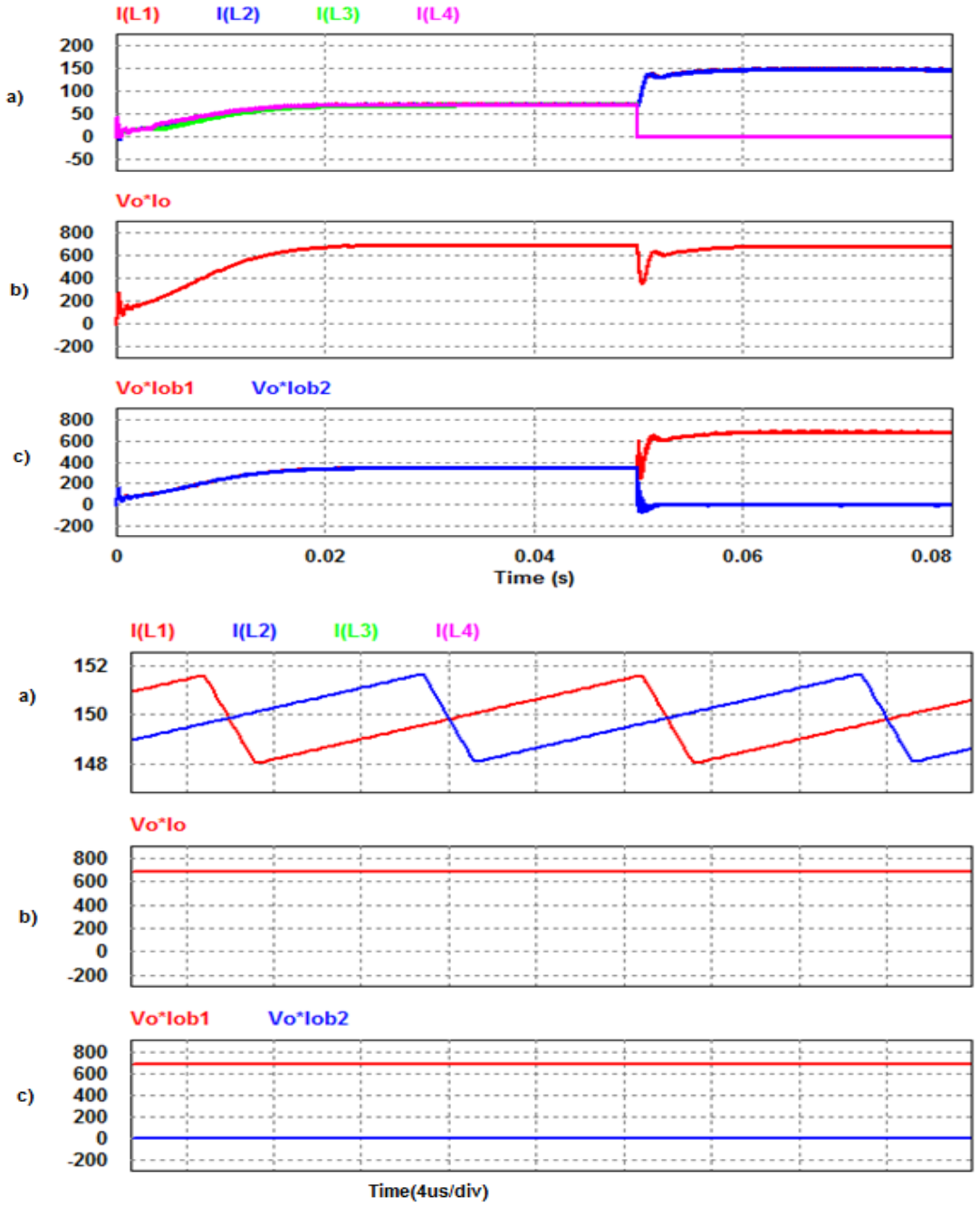


Figure 3.29: LV-AEA operation when one of the building blocks goes bad a) Inductor currents I_{L1},I_{L2} from block 1, Inductor currents I_{L3},I_{L4} from block 2,b)Total output power,and c) Output power from each building block

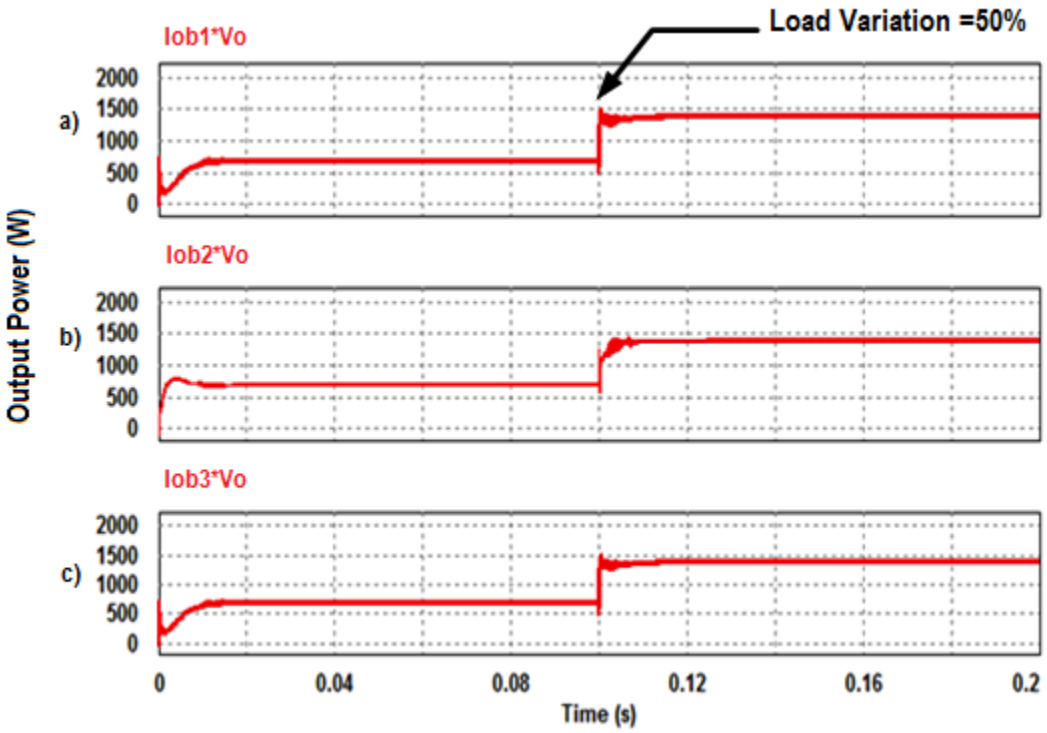


Figure 3.30: Power sharing between a) Building block 1 with turn's ratio 2, b) Buildng block 2 with turn's rato 3, c) Building block 3 with turn's ratio 2

3.6 Summary

The design of a 7kW APU start unit using LV-AEA has been presented.The following considerations merit special attention when designing the LV-AEA:

1. Design of the components: Due to the presence of high discharge current, paralleling of the components in the dc-dc converter need to be considered which can help in reducing the conduction losses and can possibly reduce the number of building blocks if needed. Also, SiC power devices and use of planar magnetics can be considered where high power is required from each building block.

2. Implementation of the Closed Loop Control: Accurate and proper interleaving of gating patterns is essential for achieving harmonic cancellation in order to minimize filtering requirements. In this thesis, interleaving of the gating patterns for each building block by 180 degrees phase-shift between respective gating patterns (S_1/S_{11} and S_2/S_{22}) was considered.

3. Equal Power Sharing: For equal distribution of the power demand between the building blocks, there is need for current control in addition to the voltage control so that current can be shared equally. Also, proper synchronization between the building blocks by interleaving their gating signals is required.

4. Bidirectional Operation: For this thesis, only unidirectional operation is shown. Bidirectional operation can be achieved by replacing diodes in the output stage with controlled devices and incorporating proper gating patterns/controls.

5. Protection and Failure Mode Analysis: Basic protection schemes have been discussed and the operation of LV-AEA under fault conditions was analyzed.

Chapter 4

Experimental Results and Discussion

In this chapter, experimental results obtained from a small scale prototype using two off the shelf dual phase synchronous boost converters with LTC3787 controller from Linear Technology [34] are discussed. The controller used provides a regulated output voltage and also enables equal current sharing between the converters for parallel operation. The principle of operation of the dual phase synchronous boost converter is similar to the dc-dc converter discussed in this thesis where two input inductors work in an interleaved manner to boost the input voltage to a higher value. The primary difference is the absence of transformer before the rectification stage. Even though the transformer can add a second boost stage depending upon the transformer turn's ratio, the main purpose for selecting an isolated dual inductor converter was to make each building block of the LV-AEA more fault-tolerant. In case a short-circuit condition occurs,the input side will remain protected from the large amount of energy that will flow due to low impedance path. Table 4.1 lists the instruments used for

testing the set up. Fig.4.1 represents the experimental test set up for standalone operation of a building block and Fig.4.2 shows the experimental test set up for parallel operation of the building blocks.

Instrument Used	**Part Number**	**Manufacturer**	**Ratings**
DC power supply	SGA 330/30	Sorensen	330V/30A
Oscilloscope	MSO-X-2024A	Agilent Technologies	200MHz;2GSa/s
Battery operated oscilloscope	THS730A	Tekscope	200MHz;500 MS/s
Differential voltage probe	N2791A	Agilent Technologies	25MHz BW
Current probe	1146A	Agilent Technologies	100 kHz BW; 0-70A
Digital Multimeter	2000	Keithley	GPIB/RS232

Table 4.1: Instruments used for experiments

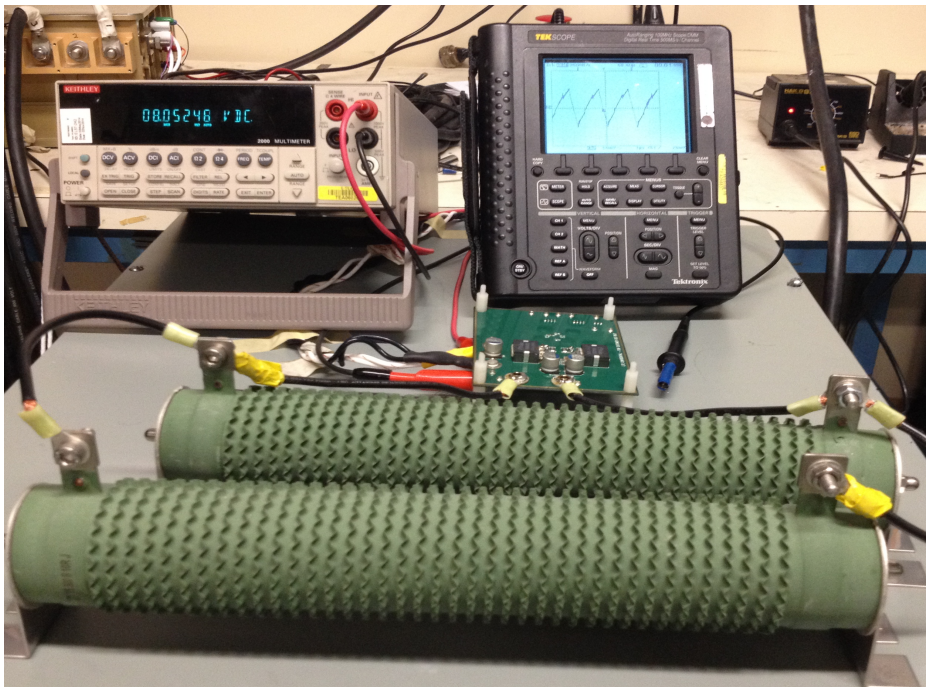


Figure 4.1: Experimental test set up for stand-alone operation of a building block

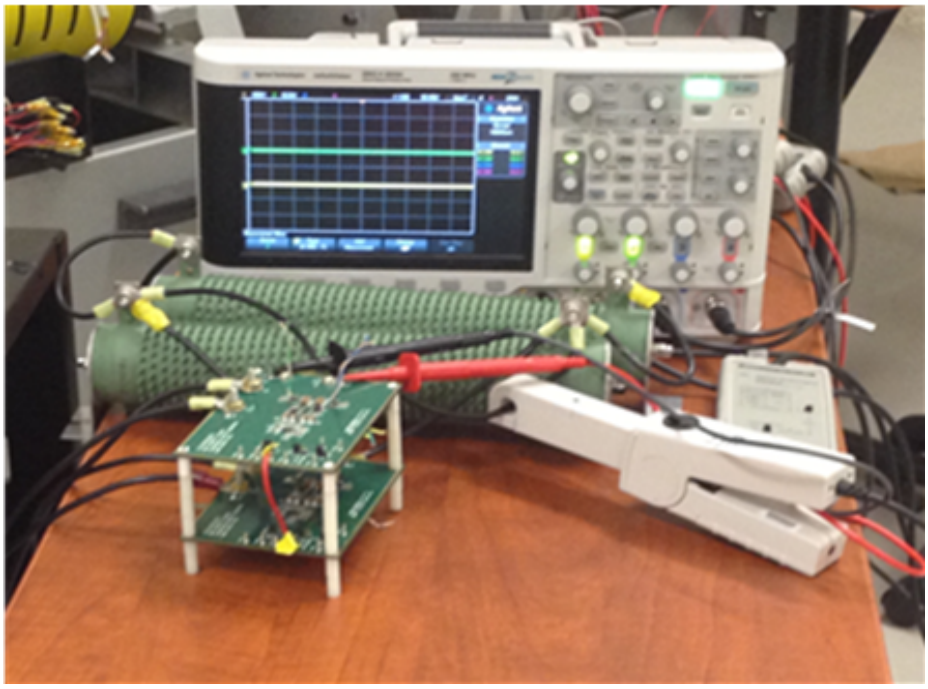


Figure 4.2: Experimental test set up for parallel operation of two building blocks

4.1 Stand-alone operation

Fig. 4.3 shows the predicted waveforms for the operation of a singe building block at input voltage (V_{in}) of 8V to supply a load of 156.8W. The simulations were conducted using LtSpice simulation tool with the circuit of the experimental set up as shown in Appendix A. The input used for the dc-dc converter is dc power supply instead of the energy storage unit (ESU). The waveforms show that the inductors share the average input current through an interleaving operation with 180° phase difference from each other. The current sensing resistors R_{L1} and R_{L2} of value $8m\Omega$ connected in series

with L_1 and L_2 determine the peak current in each input inductor such that

$$I_{Lpk} = \frac{V_{RLpk}}{R_L} \tag{4.1}$$

where I_{Lpk} is the peak value of inductor current, V_{RLpk} is the maximum sensed voltage, and R_L is the value of each sensing resistor.

By referring to the simulated waveforms, we can see the peak current in each inductor is 12.5A at the maximum resistor sense voltage of 100mV. Fig. 4.4 and Fig. 4.5 represent the experimental waveforms for the voltage across current sensing resistors of the two input inductors L_1 and L_2. It can be seen that the inductors operate in an interleaved mannner with 180° phase-shift from one another. The peak voltage of the resistors is equal to the predicted maximum voltage across the sense resistors, therefore each inductor carries a peak current of 12.5A.The average current in each input inductor can be determined as follows:

$$I_L = I_{Lpk} - \frac{\Delta I_L}{2} \tag{4.2}$$

where ΔI_L is the ripple in each inductor.

From the predicted waveforms we can see that that the ripple is equal to 5A.Therefore,each inductors is carrying an average current of 10A.

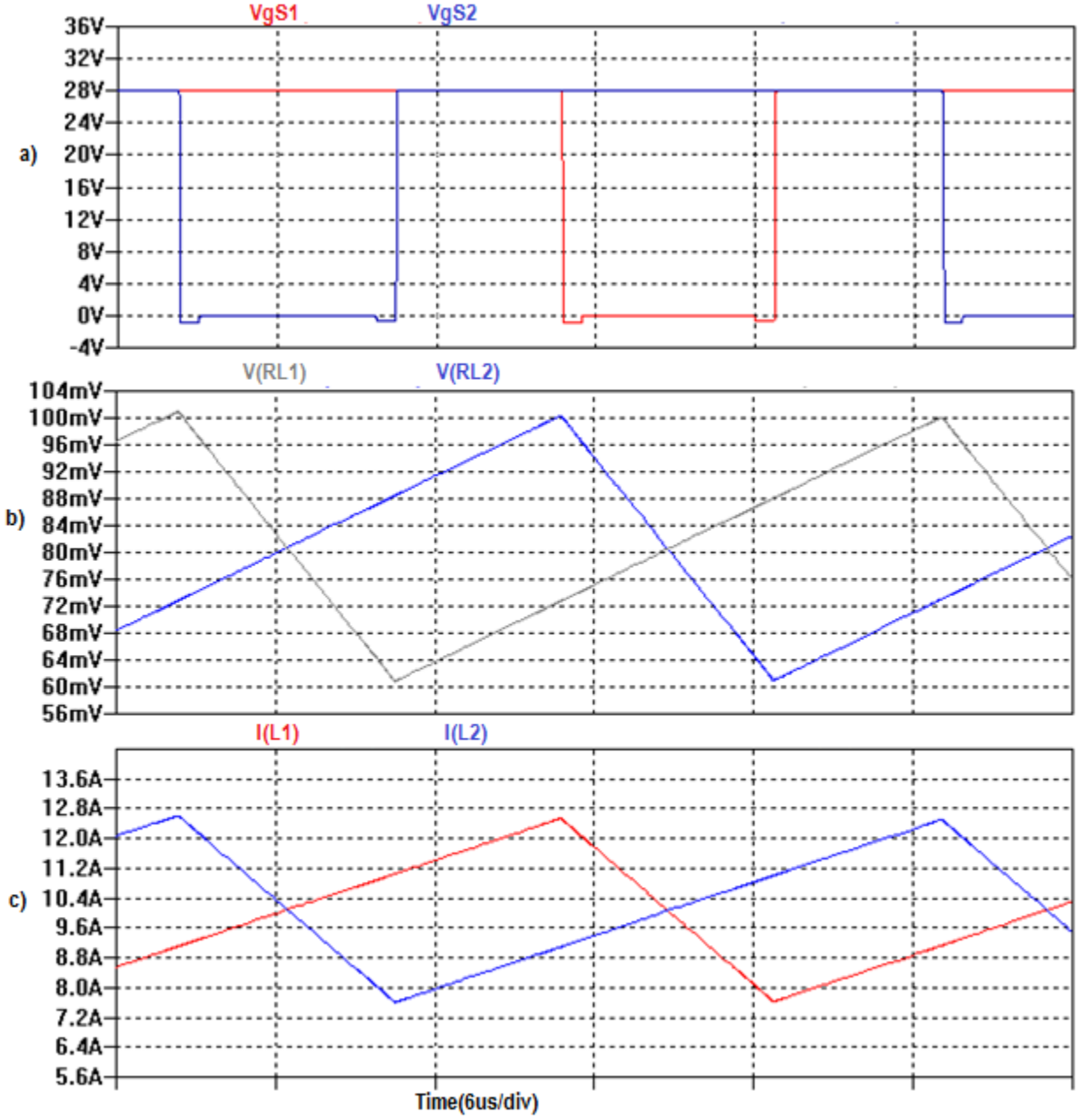


Figure 4.3: Predicted waveforms for operation of a single building block: a) Drain to source voltage V_{ds} for main switches S_1 and S_2, b) Voltage across current sensing resistors R_{L1} and R_{L2}, c) Current in inductors L_1 and L_2

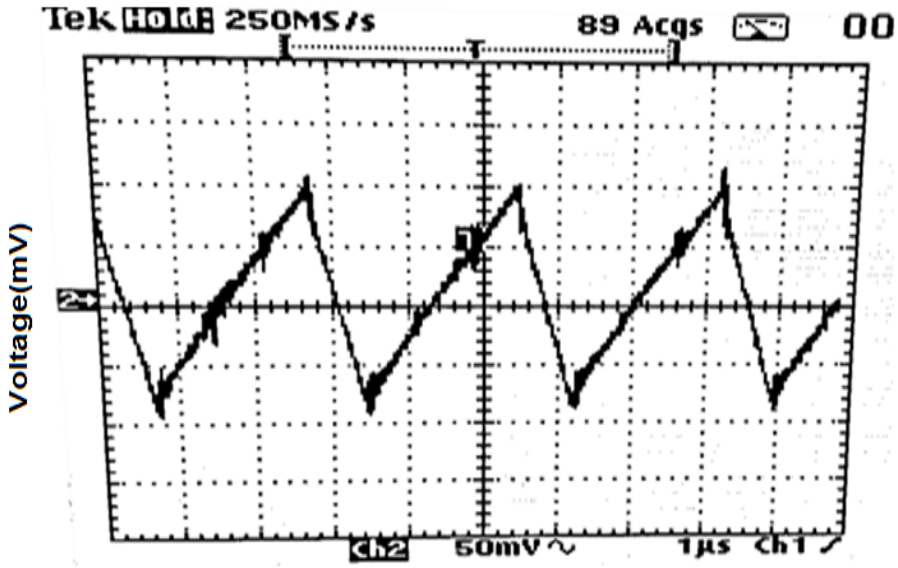


Figure 4.4: Experimental waveform for voltage across current sensing resistor R_{L1}

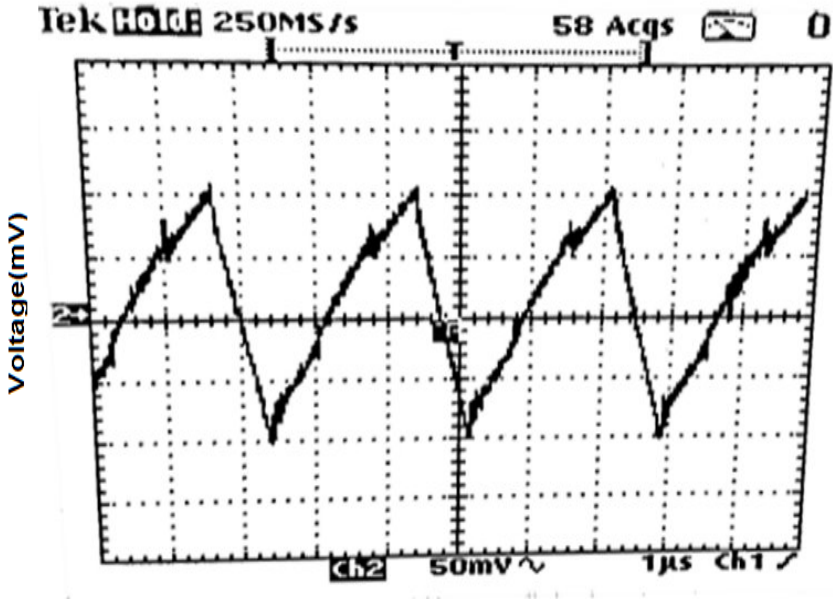


Figure 4.5: Experimental waveform for voltage across current sensing resistor R_{L2}

4.2 Parallel Operation of building blocks

To show the parallel operation of building blocks, two dual phase synchronous boost converters were connected in parallel and tested. The LTC3787 controller used in the dc-dc converters is capable of synchronized poly-phase operation. The converters were synchronized together by connecting the CLKOUT signal of the first controller to Phase Locked Loop (PLL) of the second controller (see Appendix B). As mentioned in Section 3.4.1, for multi-phase operation,the phase difference between operation of two blocks can be selected using the formula:

$$Phaseangle = 180^{\circ}/N \tag{4.3}$$

where N is the number of building blocks.

Keeping the PHASEMD pin of the LTC3787 controller floating allows 90° phase difference between the corresponding inductor currents of the two converters/blocks.Fig. 4.6 shows the predicted waveforms for the interleaved parallel operation of two building blocks to feed 156.8W load at input voltage (V_{in}) of 12V. Inductor currents of same block have a phase difference of 180° and the corresponding inductor currents of one block with respect to the other are phase shifted by 90°. The measured voltage of 25mV across the current sensing resistor ($(4m\Omega)$ used in this case) determines that each inductor is carrying equal current of 3.25A each.

Fig. 4.7 shows experimental waveforms for the drain to source voltage (V_{ds}) of the main switches of each building block and Fig.4.8 represents the voltage across current sensing resistors. Fig. 4.9 shows the drain to source voltage (Vds) of the main switch of one building block with respect to the corresponding main switch

voltage of other building block. Fig.4.10 represents the waveforms of voltage across the current sensing resistors($4m\Omega$) of inductors of the two corresponding blocks. It can be observed that the experimental waveforms complement the predicted operation of the building blocks. Because of the bandwidth of the voltage probe used for measuring voltage across current sensing resistors, the resulting signals are distorted.

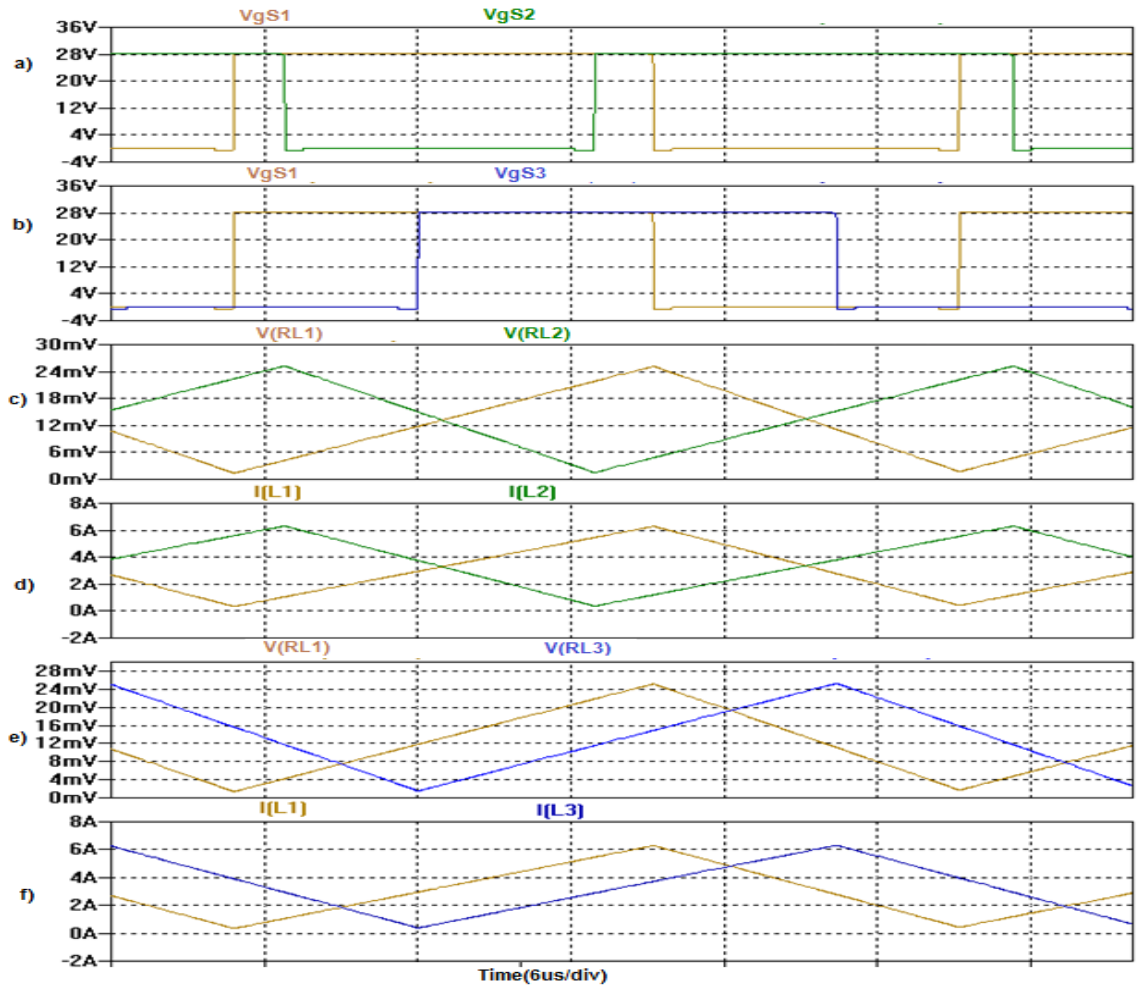


Figure 4.6: Predicted waveforms for two building blocks working in parallel:a) Drain to source voltage V_{ds} for main switches S_1 and S_2, b) Drain to source voltage V_{ds} for main switches S_1 and S_3, c) Voltage across current sensing resistors R_{L1} and R_{L2}, d) Current in inductors L_1 and L_2, e) Voltage across current sensing resistors R_{L1} and R_{L3}, f)Current in inductors L_1 and L_3

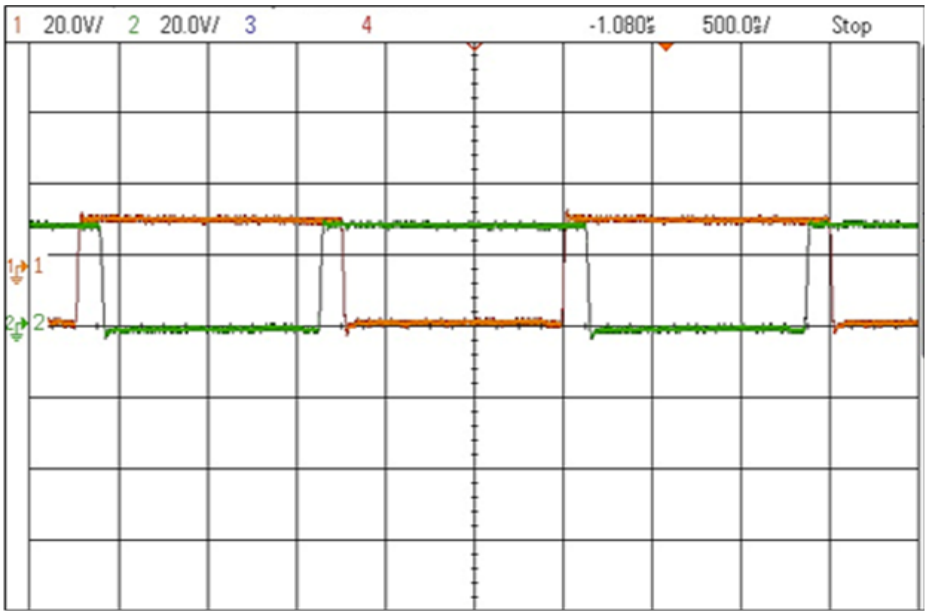


Figure 4.7: Channel 1(Yellow-20V/div) and 2(Green-20V/div) shows drain to source voltage (Vds) of main switches of block1 working 180° out of phase w.r.t. each other

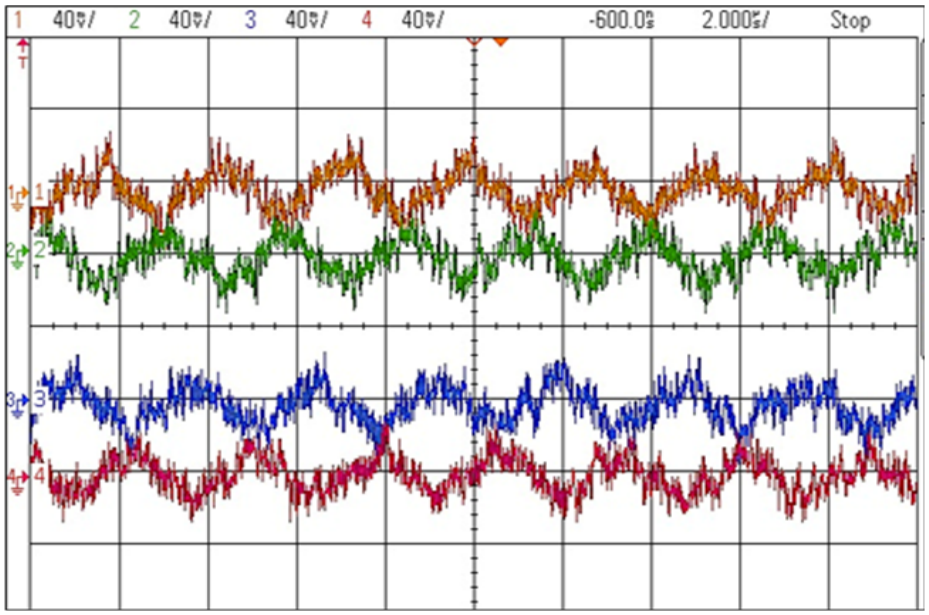


Figure 4.8: Channel (1,2) and (3,4) (40mv/div) depicting waveforms of voltage across current sensing resistors of inductor pairs in each building block (L_1,L_2) and (L_3,L_4) phase shifted by 180° respectively

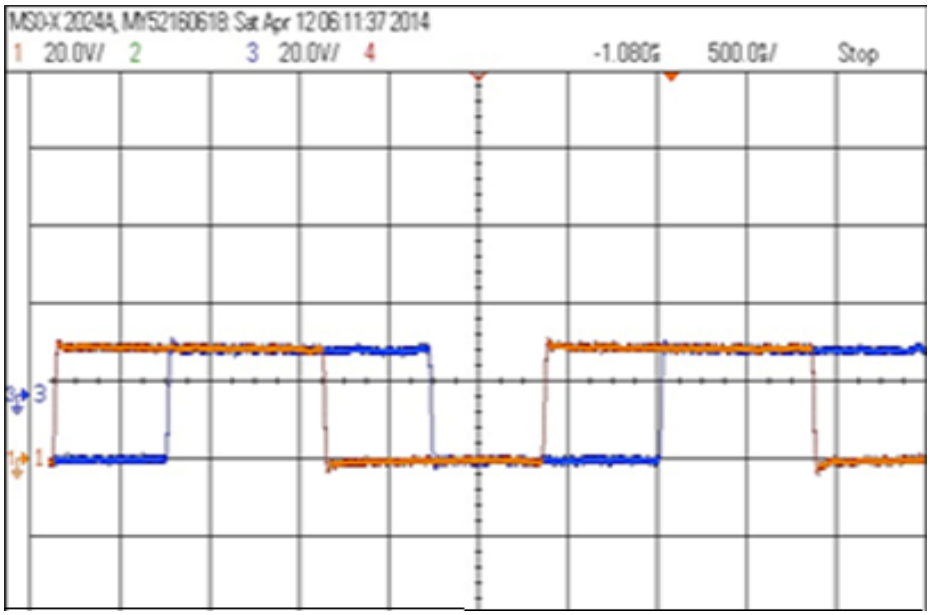


Figure 4.9: Channel 1(Yellow-20V/div) and 3(Blue-20V/div) shows drain to source voltage (Vds) of main switches of block1 and block 2 working 90° out of phase w.r.t. each other

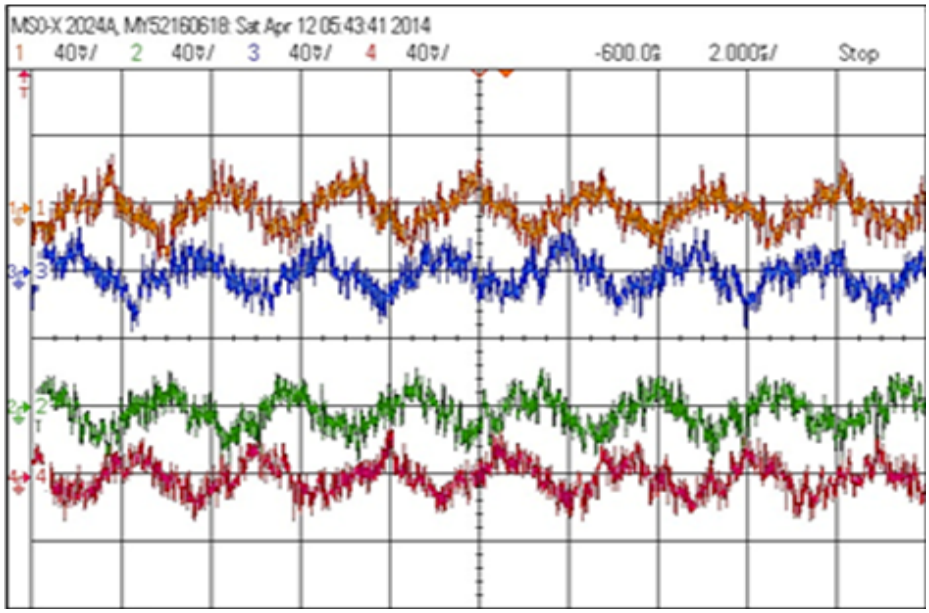


Figure 4.10: Channel (1,3) and (2,4) (40mv/div) depicting waveforms of voltage across current sensing resistor of inductor pairs of each building block (L_1,L_3) and (L_2,L_4) phase shifted by 90° respectively

Chapter 5

Conclusion

The description, analysis and design of a 'Self-Regulated Low Voltage Active Electric Accumulator (LV-AEA)' with inherent protection and control have been presented in this thesis. The design of LV-AEA for a 7kW Auxiliary Power Unit start up with ten building blocks working in parallel providing 700W each has been demonstrated. Computer simulations and analysis of the dc-dc converter in each block have been used to identify the feasibility of the proposed approach and the key design constraints. Finally, experimental results from a small-scale prototype using two commercial off the shelf dc-dc converters show the working of LV-AEA and prove the validity of the proposed approach.

The main limiting factor in the design of LV-AEA is the large input current because of high power requirement of 700W from each building block at input voltage of 2.75V-4V. This leads to significant challenges such as selecting the MOSFET switching devices with high current carrying capacity and lower R_{dsON}, large number of parallel connected components to reduce conduction losses, thermal management

burden, increased cost and weight. The efficiency calculated for each building block is also quite low (about 83% at minimum input voltage of 2.75V) even after considering parallel connection and lower series resistance for components.

Therefore, in order to overcome the above mentioned challenges, there is need to reduce the amount of input current and make building blocks used in LV-AEA more efficient. This can be attained if the maximum power required from each building block is reduced and more number of building blocks are connected in parallel. Another way of improving the efficiency and reducing the current will be to increase the input voltage by connecting few cells in series. In this scenario, the limitations of the series connection of cells have to be assessed. Considering use of parallel-connected MOSFETs, SiC power devices and planar magnetics for the design of LV-AEA can further help in minimizing the losses, size and weight. The replacement of diodes of the synchronous rectifier in dc-dc converter by switching devices can contribute in more reduction of conduction losses. Additionally, advanced thermal management is required to minimize the heat dissipation. Also, off -the shelf dc-dc controllers can be used for the closed loop controls of the LV-AEA to reduce the development time and cost.

Despite the design challenges, the proposed solution offers various advantages. The regulated output voltage from LV-AEA reduces the load currents whereas in a traditional battery lower terminal voltages can result in drawing more current from the battery. The proposed LV-AEA is fault tolerant and can operate even in case of a cell/block failure. During the fault mode of operation, it can isolate the damaged

block and the remaining building blocks can re-distribute the load amongst them to supply the required power with the help of AEA controller. The use of complex and costly BMS in conventional Li-ion batteries may be eliminated as each building block is controlled and operated independently using the building block (BB) controller. Furthermore, each building block is capable of high charge/discharge capacity with the help of dc-dc converters used. The boost operation of the dc-dc converter also reduces the number of series connected cells in LV-AEA. In this thesis, a single series connected cell was considered but few more series connected cells can be considered depending upon the type of application. The absence of large number of series connected cells alleviates the need for active or passive cell balancing which accounts for increased cost and large amount of heat dissipation. The proposed solution may be seem to come with a potential penalty of cost, weight, and power dissipation for the additional power electronics, but its has lesser safety concerns, offers high reliability, and low operational cost.

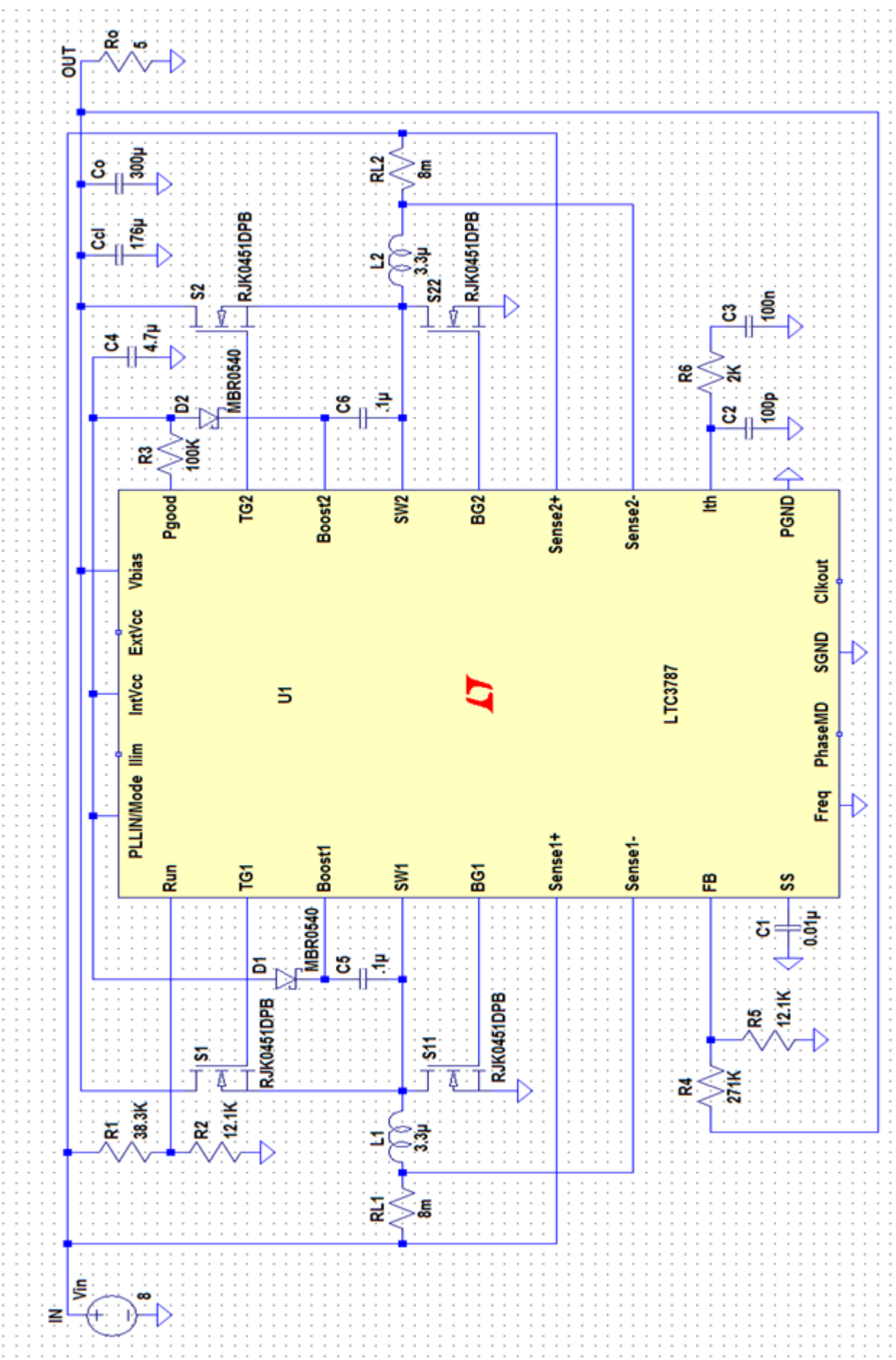
5.1 Future Scope of Work

The future scope of work is to build the technology demonstrator for a 7kW APU start application and identify its pros and cons. Another opportunity for future work is to try and make the LV-AEA more compact by reducing the number of building blocks. Increasing the power of each block to 2kW-3kW can reduce the number of parallel connected blocks to 3-4 blocks in parallel. For such high power requirement, few series connected cells have to be used and the issue of cell balancing needs to be addressed. Currently, functions of the AEA master controller of LV-AEA are only to provide synchronization and load sharing between the building blocks. Functions such

as SOC and SOH estimation, communication and data recording can be considered and investigated. Since this thesis is focused only on the unidirectional approach of LV-AEA, bi-directional mode of operation of the dc-dc converter to include the charging mode can be taken into account.

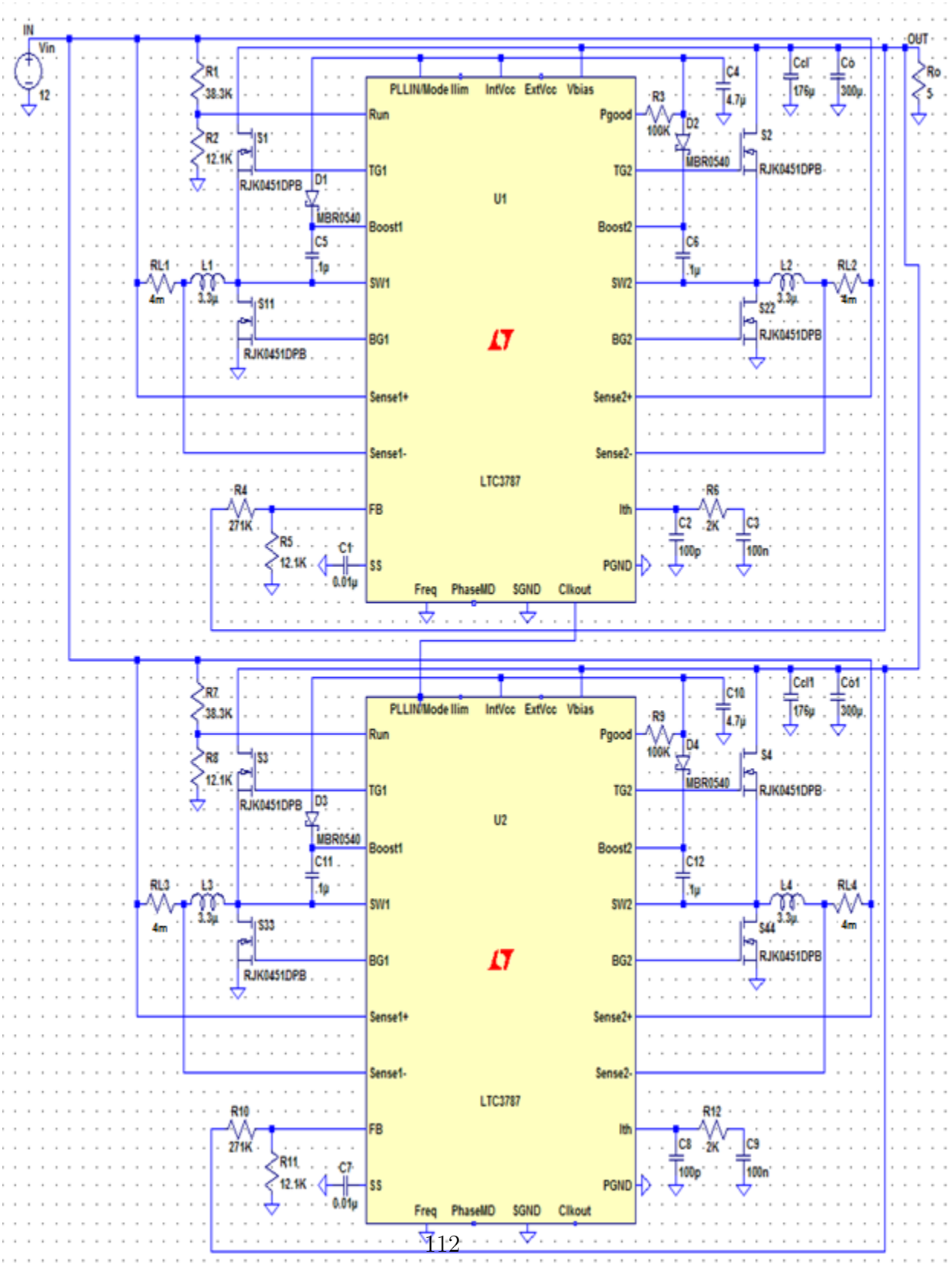
Appendix A

This appendix shows the circuit diagram of the experimental test set up [34] used for stand-alone operation of a building block.


OUT
Ro
5
Co
300µ
Ccl
176µ
C4
4.7µ
S2
RJK0451DPB
RL2
8m
L2
3.3µ
S22
RJK0451DPB
C3
100n
R6
2K
C2
100p
D2
MBR0540
C6
.1µ
R3
100K
Pgood
TG2
Boost2
SW2
BG2
Sense2+
Sense2-
Ith
PGND
Vbias
ExtVcc
IntVcc
Ilim
PLLIN/Mode
Run
TG1
Boost1
SW1
BG1
Sense1+
Sense1-
FB
SS
Clkout
SGND
PhaseMD
Freq
U1
LTC3787
D1
MBR0540
C5
.1µ
S1
RJK0451DPB
S11
RJK0451DPB
C1
0.01µ
R5
12.1K
R4
271K
R1
38.3K
R2
12.1K
L1
3.3µ
RL1
8m
IN
Vin
8

Appendix B

This appendix shows the circuit diagram of the experimental test set up [34] used for parallel operation of the building blocks.


IN
Vin
12
R1
38.3K
R2
12.1K
S1
RJK0451DPB
D1
MBR0540
C5
.1µ
RL1
4m
L1
3.3µ
S11
RJK0451DPB
R4
271K
R5
12.1K
C1
0.01µ
PLLIN/Mode Ilim IntVcc ExtVcc Vbias
Run
TG1
Boost1
SW1
BG1
Sense1+
Sense1-
FB
SS
Pgood
TG2
Boost2
SW2
BG2
Sense2+
Sense2-
Ith
PGND
Freq PhaseMD SGND Clkout
U1
LTC3787
R3
100K
D2
MBR0540
C4
4.7µ
S2
RJK0451DPB
C6
.1µ
L2
3.3µ
S22
RJK0451DPB
RL2
4m
R6
2K
C2
100p
C3
100n
Ccl
176µ
Co
300µ
OUT
Ro
5
R7
38.3K
R8
12.1K
S3
RJK0451DPB
D3
MBR0540
C11
.1µ
RL3
4m
L3
3.3µ
S33
RJK0451DPB
R10
271K
R11
12.1K
C7
0.01µ
U2
LTC3787
R9
100K
D4
MBR0540
C10
4.7µ
S4
RJK0451DPB
C12
.1µ
L4
3.3µ
S44
RJK0451DPB
RL4
4m
R12
2K
C8
100p
C9
100n
Ccl1
176µ
Co1
300µ

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