

**STATISTICAL AND ELECTROMAGNETIC
CIRCUIT OPTIMIZATION TECHNOLOGY**

J.W. Bandler

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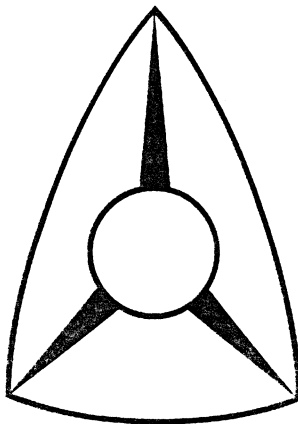
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STATISTICAL AND ELECTROMAGNETIC CIRCUIT OPTIMIZATION TECHNOLOGY

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presented at

WORKSHOP ON STATISTICAL MMIC AND MODULE DESIGN TECHNIQUES
1996 IEEE MTT-S Int. Microwave Symposium, San Francisco, CA, June 21, 1996



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Introduction

microwave CAD systems must link geometry, layout, physical and process parameters with performance, yield and system specifications

hierarchically structured CAD systems must integrate electromagnetic (EM) theory, circuit theory and system theory

fast, predictable, physics-based modeling and simulation of devices and circuits are important aspects of manufacturable mm-wave designs

CAD technology must account for statistical uncertainties and parameter spreads

CAD modules must facilitate an effective path from process, physical or geometrical description to a yield-driven, optimization-oriented design environment



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First-Pass Success Approach

performance *and* cost specifications

automated optimization

accurate simulation models taking into account

- material and dimensional constraints

- operating environment

- production tolerances

Situations Needing Better Simulation Methodology

satellite system environmental temperature variations

cutting cost by lowering machining precision requirement

self-heating in high-density circuits

modulated and transient high-frequency signals

EM proximity couplings



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Overview of Presentation

design centering; yield optimization; cost-driven design

integration through Datapipe™

EM optimization

parameterization through Geometry Capture™

parallel computation

Space Mapping™ optimization



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Physics-Based Yield Optimization of MMICs

random variations in manufacturing process may lead to outcomes failing design specifications

production tuning of MMICs is restricted

component replacement is not possible

circuits manufactured in batches rather than individually

cost is directly affected by yield

the ability to predict and enhance production yield is critical

accurate EM simulations of passive elements combined with physical simulations of active devices will be enhanced by Space Mapping optimization



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Yield Optimization of a Three-Stage MMIC Amplifier *(Bandler, Biernacki, Cai, Chen, Ye and Zhang, 1992)*

the three-stage X-band MMIC amplifier is based on the circuit topology and fabrication layout originally designed by Thomson-Semiconductors (*Kernmarrec and Rumelhard, 1988*)

intended as a gain block for phased-array antennas

the amplifier contains three GaAs MESFETs using an interdigitated structure with two gate fingers of dimensions $150\text{ }\mu\text{m} \times 1.0\text{ }\mu\text{m}$

all passive elements are realized using lumped MMIC elements: spiral inductors, MIM capacitors and bulk resistors

37 statistical variables with correlations and 16 design variables

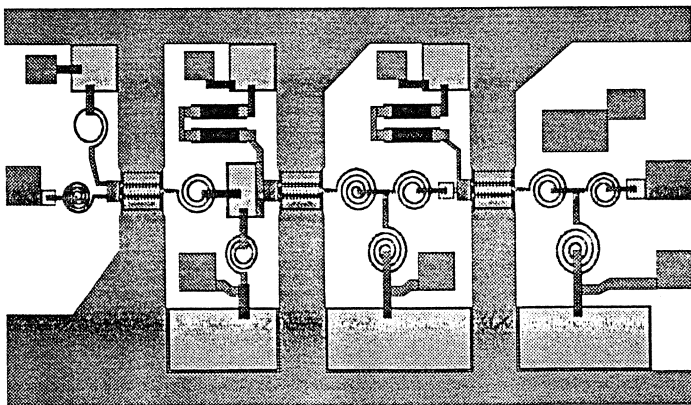
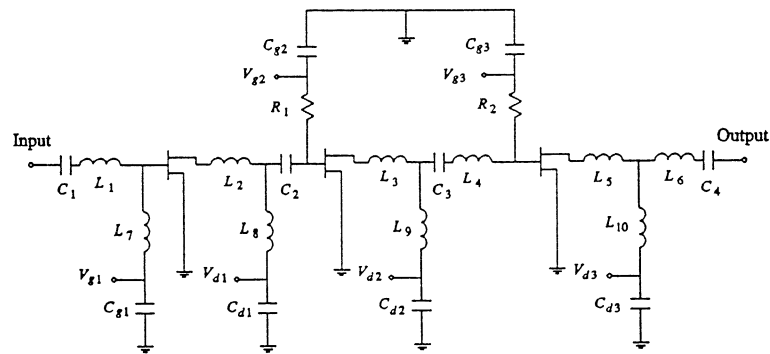
yield optimization carried out by OSA90/hope

yield is improved from 26% at the nominal design to 69%



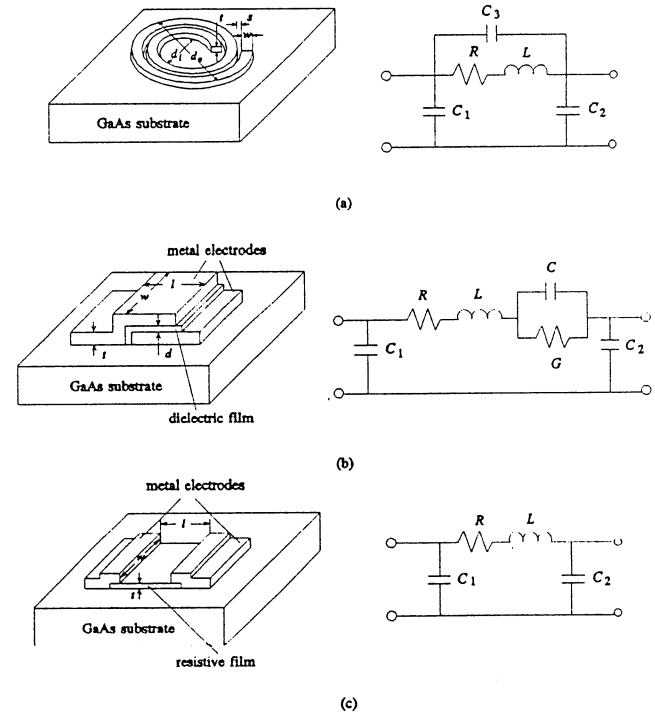
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Circuit Schematic and Layout of the Three-Stage Amplifier



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Passive Elements (Bahl, 1988)



the expressions for the equivalent circuit components are derived from (simplified) device physics



Predictable Yield-Driven Circuit Optimization

(Bandler, Ye, Cai, Biernacki and Chen, 1992)

usefulness of yield-driven design depends on the accuracy of yield estimated using the statistical model

yield predicted by Monte Carlo simulation using the model should be consistent with the yield predicted directly from the device measurement data

the advantage of a statistical model over the measurement data is that the model provides for convenient interpolation

the selection of device parameters for yield optimization can be assisted by yield sensitivity analyses

the yield can be significantly increased by simultaneous circuit-device optimization

design of a small-signal broadband amplifier is investigated using OSA90/hope with the KTL model w.r.t. a number of specifications

the predicted yield is verified using the device data



Yield Verification

	Before Yield Optimization		After Yield Optimization	
	Predicted Yield (%)	Verified Yield (%)	Predicted Yield (%)	Verified Yield (%)
Spec. 1	17.5	15.7	67	57.9
Spec. 2	21	20	83	75.7
Spec. 3	44	37.1	98	93.6

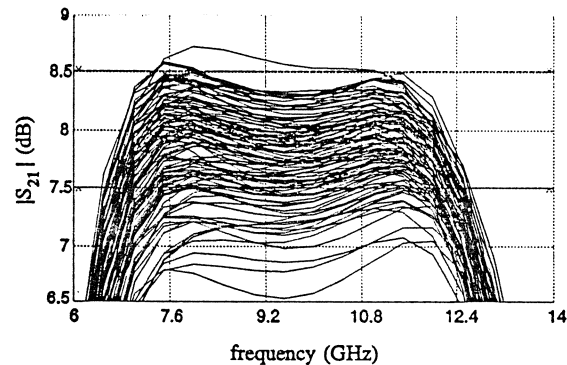
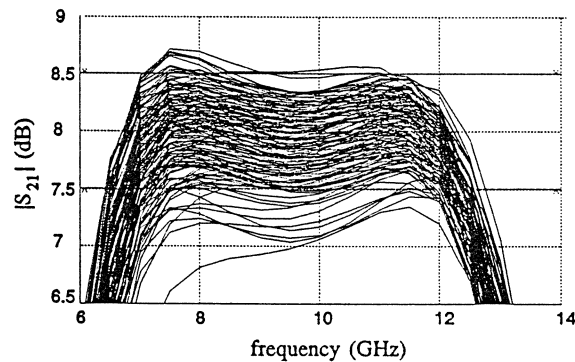
Spec. 1: $7.5\text{dB} < |S_{21}| < 8.5\text{dB}$, $|S_{11}| < 0.5$, $|S_{22}| < 0.5$.
Spec. 2: $6.5\text{dB} < |S_{21}| < 7.5\text{dB}$, $|S_{11}| < 0.5$, $|S_{22}| < 0.5$.
Spec. 3: $6.0\text{dB} < |S_{21}| < 8.0\text{dB}$, $|S_{11}| < 0.5$, $|S_{22}| < 0.5$.

200 Monte Carlo outcomes are used for predicted yield, 140 for verified yield



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Gain After Optimization from Model and from Data



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Physics-Based Cost-Driven Design

(Bandler, Biernacki, Cai and Chen, 1995)

yield optimization maximizes the yield by adjusting the nominal values of the design variables keeping tolerances fixed

the cost for obtaining small tolerances may be very high

there is a trade-off between the yield and the cost

cost-driven design minimizes the cost while maintaining the required yield

cost-driven optimization

$$\underset{x}{\text{minimize}} \quad C(x)$$

$$\text{subject to } Y \geq Y_s$$

x vector of parameter tolerances

Y design yield

Y_s specified yield

$C(x)$ cost function, e.g.,

$$C(x) = \sum_{i=1}^m \frac{c_i}{x_i}$$



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OSA's Datapipe™

encapsulating simulators as black-box executables with alphanumeric inputs and outputs

built-in support for network and parallel computing

preprocessing and postprocessing of data

preprocessing of $x1, x2, \dots$;

FILE="simulator"

INPUT=(*text*, $x1, x2, \dots$)

OUTPUT=($y1, y2, \dots$);

postprocessing of $y1, y2, \dots$;

hierarchy of variables

multiple simulators can be combined (serial and parallel)

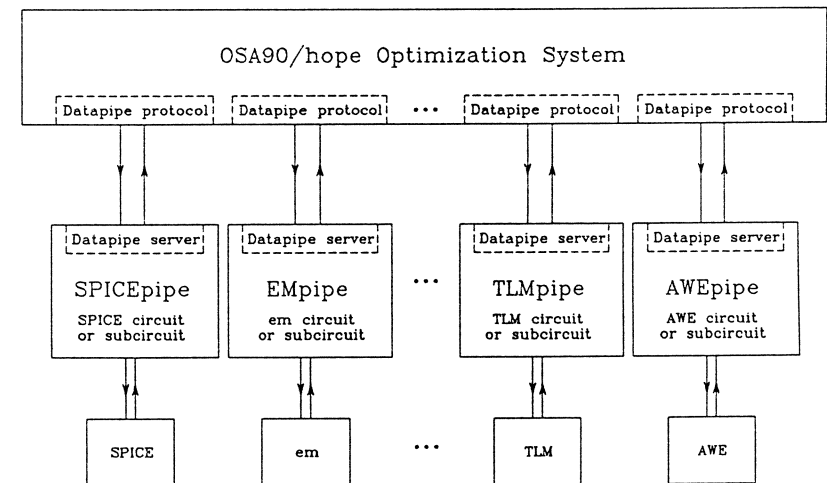
simultaneous specifications in different domains

symbolic algebra and gradients



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OSA's Datapipe™ System





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Challenges of Automated EM Optimization

(Bandler et al., 1993, 1994)

drastically increased analysis time

discrete nature of some EM solvers

continuity of optimization variables

gradient information

interpolation and modeling

integrated data bases



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Geometry Capture™ *(OSA, 1994)*

EM simulators deal directly with the layout representation of circuits in terms of absolute coordinates

geometrical coordinates are not directly related to designable parameters

geometrical parameterization is needed for every new structure

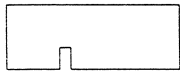
using a graphical layout editing tool the user marks the evolution of the structure as the designable parameters change

processed by OSA's Empipe to extract the relevant information

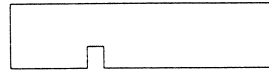
a mapping between the geometrical coordinates and the designable parameter values is established



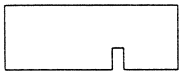
Various Object Evolutions



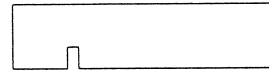
(a)



(b)



(c)

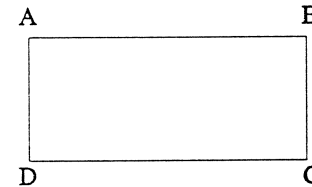


(d)

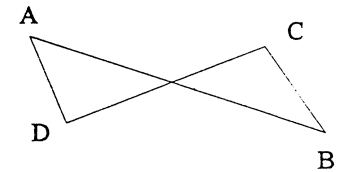
- (a) initial geometry
- (b) proportional expansion of the whole structure along the x axis
- (c) only the location of the slit in the fixed line is allowed to change
- (d) only the segment to the right of the slit is allowed to expand



Possible Pitfalls of Arbitrary Movement of Vertices



(a)



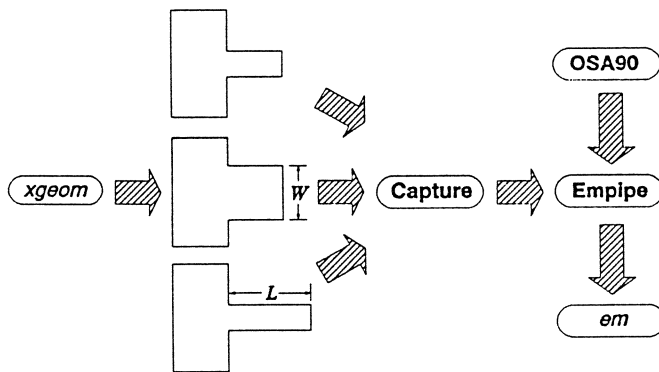
(b)

- (a) initial geometry
- (b) an unwanted result due to an arbitrary and independent movement of vertices



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Implementation of Geometry Capture™



employs a sophisticated algorithm in a manner completely transparent to the user

extremely easy to use



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Empipe Geometry Capture™ Form Editor

The screenshot shows the Empipe V3.1 Form Editor interface. It includes a menu bar with 'Load New File', 'Save To File', 'Simulate Optimize', and 'Quit'. Below the menu bar, there are input fields for 'Noninal Geo File: tpad0.geo', 'en Control File: tpad.an', 'DC S-par File:', and 'en Run Options: -Qdn'. A table displays the following data:

Parameter Name	Geo File Name	Noninal Value	Perturbed Value	# of Grids	Unit Name
L1	tpad1.geo	22	24	1	nil
L2	tpad2.geo	7	8	1	nil
M1	tpad3.geo	11	13	1	nil
M2	tpad4.geo	10	12	1	nil



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Select Optimization Variables Windows

Select Optimization Variables					
Mark All		Unmark All		Go	Cancel
Variable?	(Unit)	Lower Bound	Starting Point	Upper Bound	
<input checked="" type="checkbox"/> L1	(mil)		22		
<input checked="" type="checkbox"/> L2	(mil)		7		
<input checked="" type="checkbox"/> W1	(mil)		11		
<input checked="" type="checkbox"/> W2	(mil)		10		

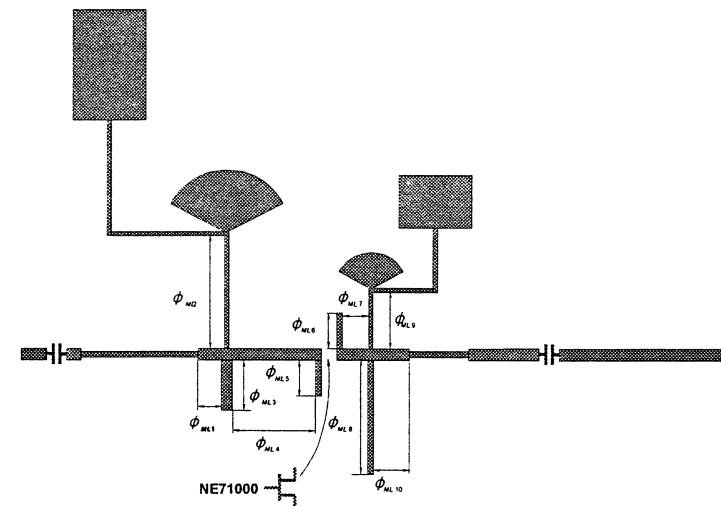
Specifications for Optimization Windows

Specifications for Optimization	
Add a new specification defined as follows	
FREQ (GHz) from: 2	to: 18 step: 4
MS11_dB	< -10 weight: 1
Specifications Currently Defined	
FREQ: from 2GHz to 18GHz step=4GHz MS21_dB < -9 W=5	
FREQ: from 2GHz to 18GHz step=4GHz MS21_dB > -11 W=5	
FREQ: from 2GHz to 18GHz step=4GHz MS11_dB < -10	



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Nonlinear FET Class B Frequency Doubler (Microwave Engineering Europe, 1994)



using Geometry Capture™, the linear subcircuit is defined as one optimizable structure with 10 variables



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Direct EM Optimization of the Frequency Doubler
(Bandler, Biernacki, Cai, Chen and Grobelny, 1995)

Geometry Capture for optimization of arbitrary planar structures is used

Empipe handles direct optimization with Sonnet's *em*

the complete structure between the two capacitors is considered as a whole and simulated by Sonnet's *em*

the circuit is directly optimized by OSA90/hope through Empipe with 10 optimization variables

design specification:

conversion gain > 3 dB
spectral purity > 20 dB

at 7 GHz and 10 dBm input power



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Parallel Computing Options

multiprocessor computers and specialized compilers vs. distributing EM analyses over a computer network

the overhead of parallelization is negligible as compared to the CPU-intensive EM analyses

splitting at the component/subcircuit level

suitable when several EM simulation results are needed simultaneously

off-grid interpolation

numerical gradient estimation

multiple outcomes in statistical analysis

suits best the operational flow of interpolation, optimization and statistical analysis



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Organization of Parallel Computing

organized by EmPIPE from one of the networked computers (master host)

using standard UNIX protocols (remote shell and equivalent hosts) an EM analysis is started on each of the available hosts

when the analysis is finished on a host, the next job, if any, is dispatched to that host

EM simulation results are gathered from all the hosts and stored in a data base created on the master host

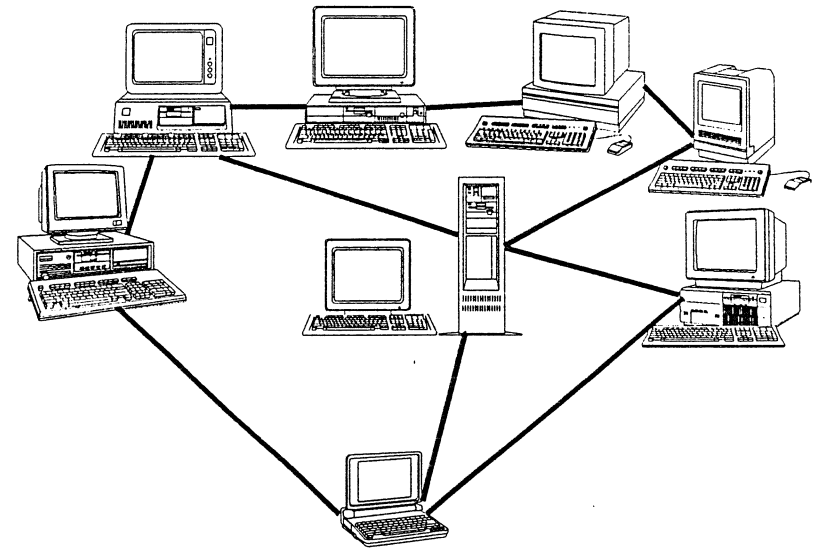
no platform specific mechanisms

applicable to both local and wide area networks of heterogeneous workstations



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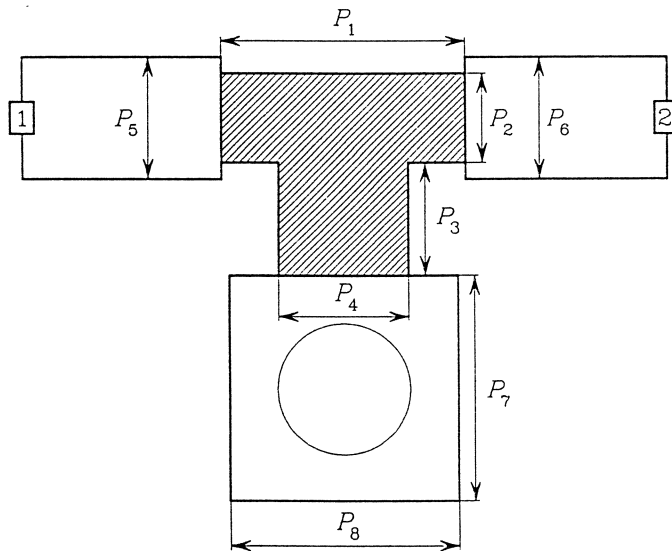
Heterogeneous Network of Computers





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A 10 dB Distributed Attenuator



built on a 15 mil thick substrate with relative dielectric constant of 9.8

metallization of a high resistivity ($50 \Omega/\text{sq}$)

the feed lines and the grounding pad are assumed lossless



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Statistical Design of the Attenuator

design specifications (from 2 GHz to 18 GHz)

$9.5 \text{ dB} \leq \text{insertion loss} \leq 10.5 \text{ dB}$

return loss $\geq 10 \text{ dB}$

the structure, treated as a whole, is described by 8 geometrical parameters

designable: 4 parameters describing the resistive area

statistical variables: all 8 parameters (with a standard deviation of 0.25 mil)

em simulation at a single frequency requires about 7 CPU minutes on a Sun SPARCstation 1+



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Parallel Computing in Nominal Design of the Attenuator

30 *em* analyses

an average of 3.8 analyses run in parallel

about 168 minutes on the network of Sun SPARCstations 1+

time is reduced by 75%

Parallel Computing in Statistical Design of the Attenuator

additional 113 *em* analyses

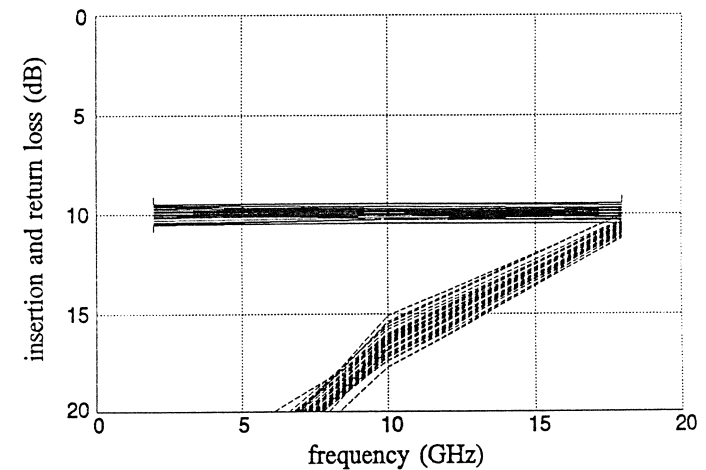
an average of 2.5 analyses run in parallel

time is reduced by 60%



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Monte Carlo Sweeps of the Attenuator Responses

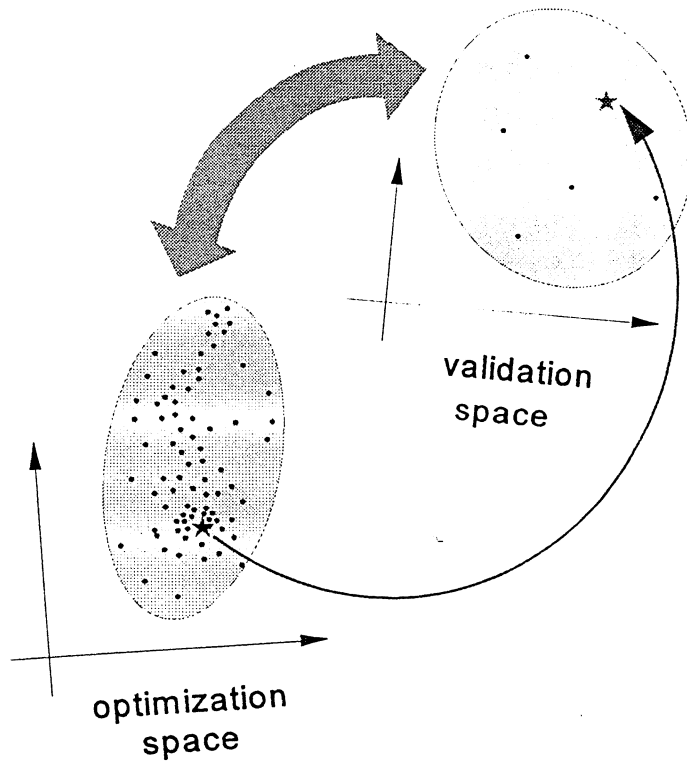


yield (estimated from 250 Monte Carlo outcomes) is increased from 82% to 97%



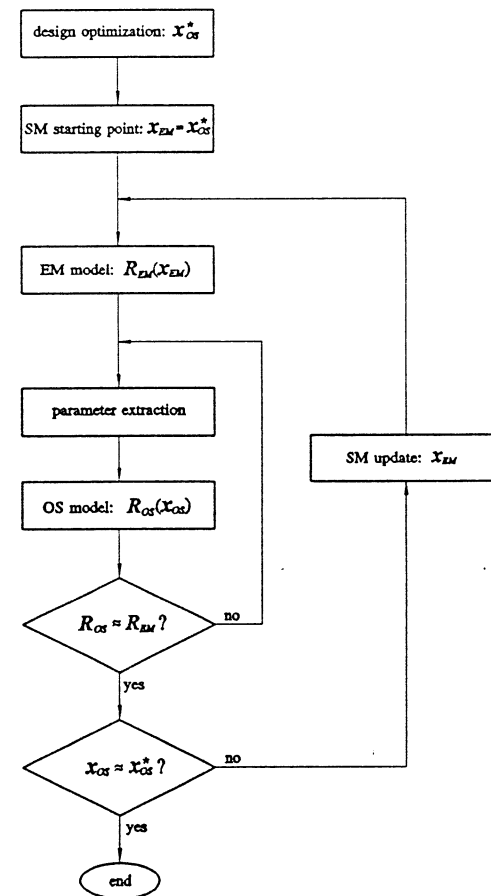
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Space Mapping™
(Bandler et al., 1994)



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Automated Aggressive Space Mapping™





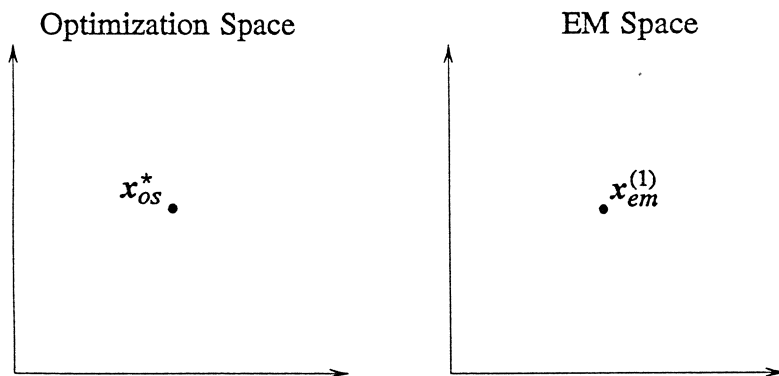
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Illustration of Aggressive Space Mapping Optimization

Step 0

find the optimal design x_{os}^* in Optimization Space

Step 1



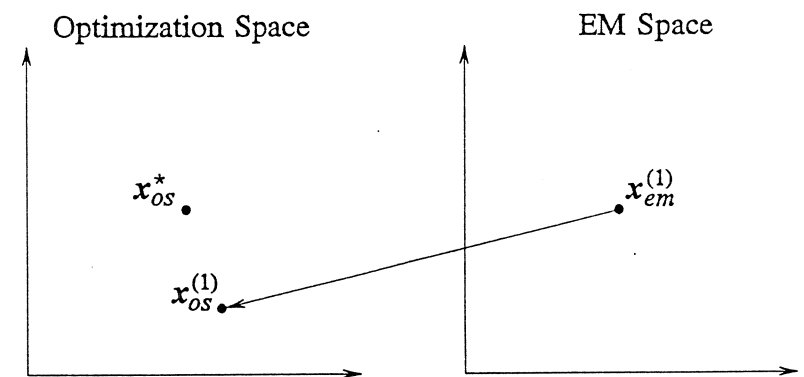
set $x_{em}^{(1)} = x_{os}^*$ assuming x_{em} and x_{os} represent the same physical parameters



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Illustration of Aggressive Space Mapping Optimization

Step 2

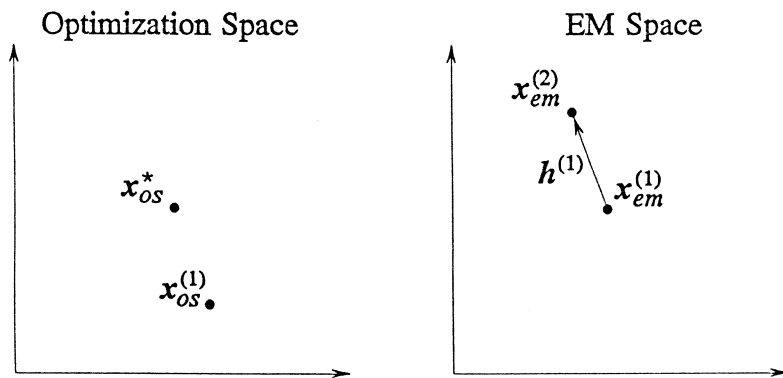


perform X_{os} -space model parameter extraction



Illustration of Aggressive Space Mapping Optimization

Step 3



initialize Jacobian approximation $B^{(1)} = 1$

obtain $x_{em}^{(2)}$ by solving

$$B^{(1)}h^{(1)} = -f^{(1)}$$

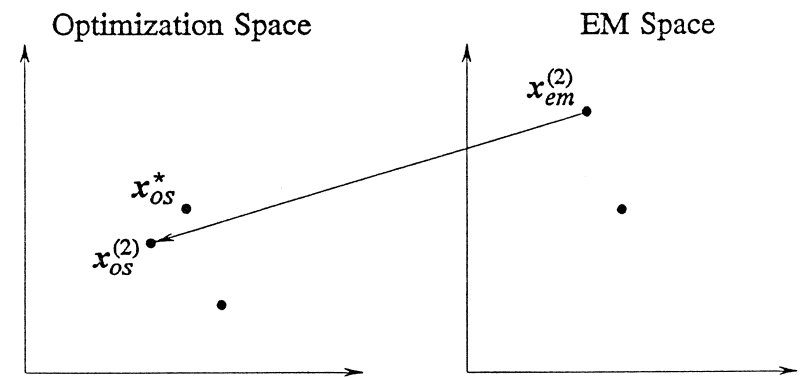
where

$$f^{(1)} = x_{os}^{(1)} - x_{os}^*$$



Illustration of Aggressive Space Mapping Optimization

Step 4

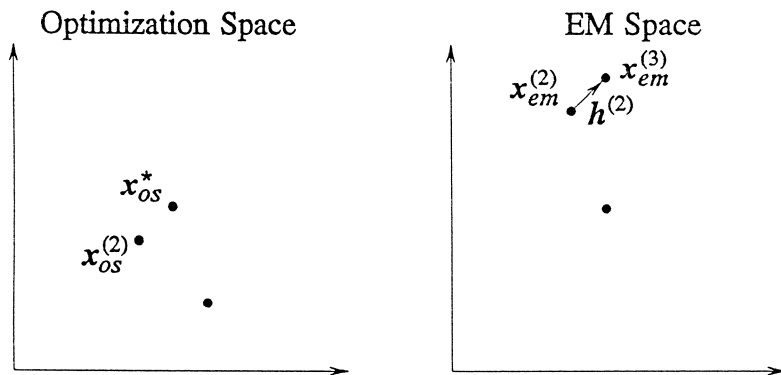


perform X_{os} -space model parameter extraction



Illustration of Aggressive Space Mapping Optimization

Step 5



update Jacobian approximation from $B^{(1)}$ to $B^{(2)}$

obtain $x_{em}^{(3)}$ by solving

$$B^{(2)}h^{(2)} = -f^{(2)}$$

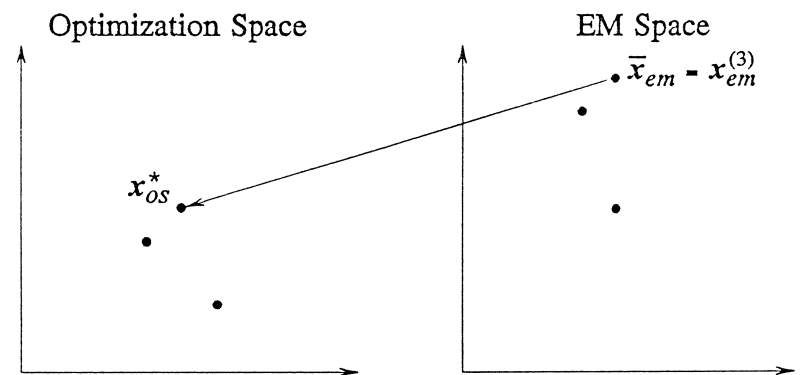
where

$$f^{(2)} = x_{os}^{(2)} - x_{os}^*$$



Illustration of Aggressive Space Mapping Optimization

Step 6



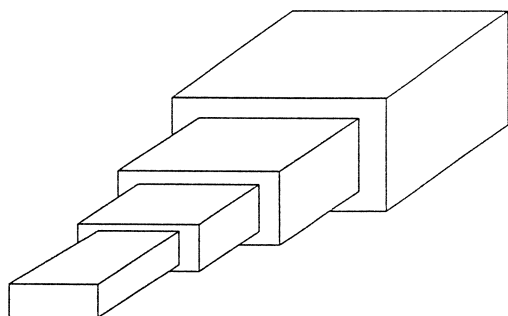
perform X_{os} -space model parameter extraction

if $\|x_{os}^{(3)} - x_{os}^*\| \leq \epsilon$ then $\bar{x}_{em} = x_{em}^{(3)}$ is considered as the SM solution



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EM Optimization of 3D Structures



a two-section waveguide transformer

two cases of Space Mapping used to align

- (a) an ideal empirical model and a non-ideal empirical model
- (b) an empirical model and HFSS simulations



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Conclusions

cost-effective yield-driven design technology is indispensable

integrated EM and physical simulation and optimization capable of handling arbitrary structures is the future

Space Mapping promises the accuracy of EM and physical simulation and the speed of circuit-level optimization

heterogeneous parallel CAD over a local or wide area network significantly increases design power

integration of EM simulators from various vendors into automated design using OSA's optimizers

Geometry Capture allows analysis and optimization of complicated structures as a whole

EM optimization of arbitrary geometries exerts a massive demand on resources, particularly for yield-driven design

parallel computation speeds up CPU intensive optimization

integrating parallel computation with interpolation, response function modeling and data base techniques will immensely reduce the overall design time



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