NONLINEAR ANALYSIS OF A CLASS B FREQUENCY DOUBLER: DETAIL RESULTS

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I. INTRODUCTION

A Class B frequency doubler was provided by Microwave Engineering Europe (MEE) to several CAD vendors as a benchmark example. The circuit consists of a FET and distributed microstrip elements including two radial stubs and bias pads. The FET used in the circuit is NE71000 from NEC. The simulations required by MEE are as follows.

(a) Coupling between the third harmonic stubs situated at the gate and drain ports of the FET.

(b) The effects of the bias pads as they are in close proximity to the circuit.

(c) Output power (up to the 4th harmonic) and multiplication gain (conversion gain) at 7 GHz and input power range of -3 dBm to 16 dBm, under the bias condition V_{gs} = -1.2 V and V_{ds} = 3.0 V.

(d) Frequency response (power and multiplication gain) from 6.5 GHz to 8 GHz.

We used HarPE [1], OSA90/hope [2] and em [3] to carry out all the required work including FET parameter extraction, em simulation to consider the stub coupling effect and bias pad effect, nonlinear harmonic balance (HB) simulation of the entire circuits. Additionally, we performed Monte Carlo simulation to investigate the effect of FET model uncertainty, and minimax optimization to obtain better circuit performance. The details of these experiments are reported here.

II. FET PARAMETER EXTRACTION

Since no large-signal model of the FET was provided by the editor, nor it was available from the manufacturer, we used HarPE to perform parameter extraction to create the large-signal FET model. The data that we utilized for parameter extraction contain typical DC characteristics and typical S parameters from 2 GHz to 26 GHz with 1 GHz step at two bias points published in the "NEC California Eastern Laboratories, RF and microwave Semiconductors" data book [4]. The

built-in Curtice and Ettenberg model together with the Extrinsic4 linear subcircuit is chosen to model the FET. The parameter extraction is performed by fitting simultaneously the DC curves at 12 points, and the *S* parameters at the two bias points and 25 frequencies. The values of the extracted parameters are listed in Table I. The DC matching and *S*-parameter matching at two bias points are shown in Figs. 1, 2 and 3, respectively. Very good DC match and reasonable *S*-parameter match are obtained.

TABLE I
PARAMETER VALUES OF THE EXTRACTED CURTICE FET MODEL

Parameter	Value	Parameter	Value
A0	0.0826627	A1	0.335942
A2	0.367757	A3	0.00858573
GAMMA	1.86239	BETA	0.121412
VDS0	0.742967	IS	5.26136E-11
N	3.28559	CGD0	0.108206pF
CGS0	0.227312pF	FC	0.173912E-12
Tau	1.0947ps	Gmin	0.841032E-12
RG	1.33301	RD	0.888452
RS	5.04386	CDS	0.0414509pF
GDS	0.00441929	CX	100pF
LG	0.160598nH	LD	5.3121E-06nH
LS	0.0718402nH	CGE	0.143109pF
CDE	0.0924559pF		

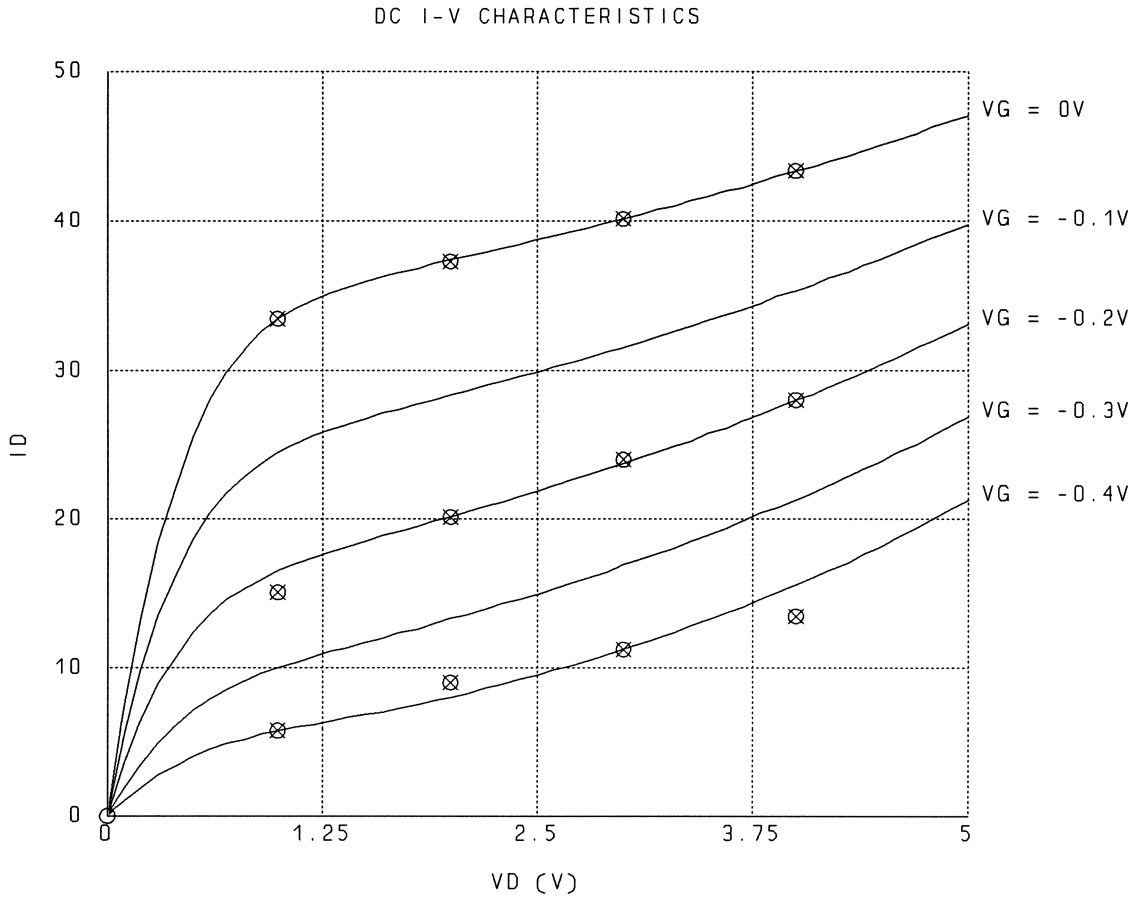

Fig. 1 DC match between the simulated responses from the model (solid lines) and typical transistor data (o) [4].

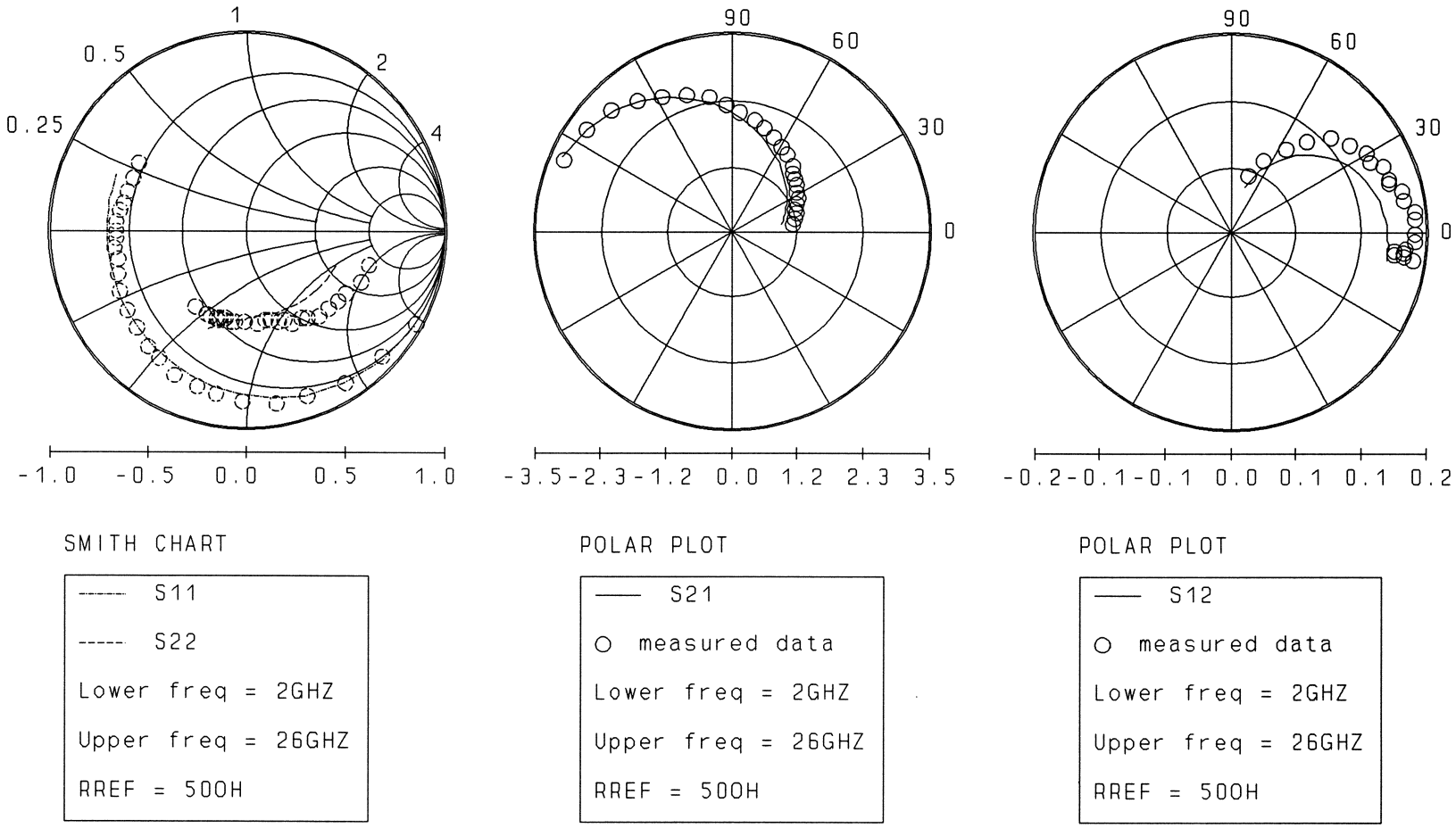

Fig. 2 *S*-parameter match between the model (solid and dashed lines) and typical transistor data (o) at $V_{ds} = 3$ V, $I_{ds} = 10$ mA [4].

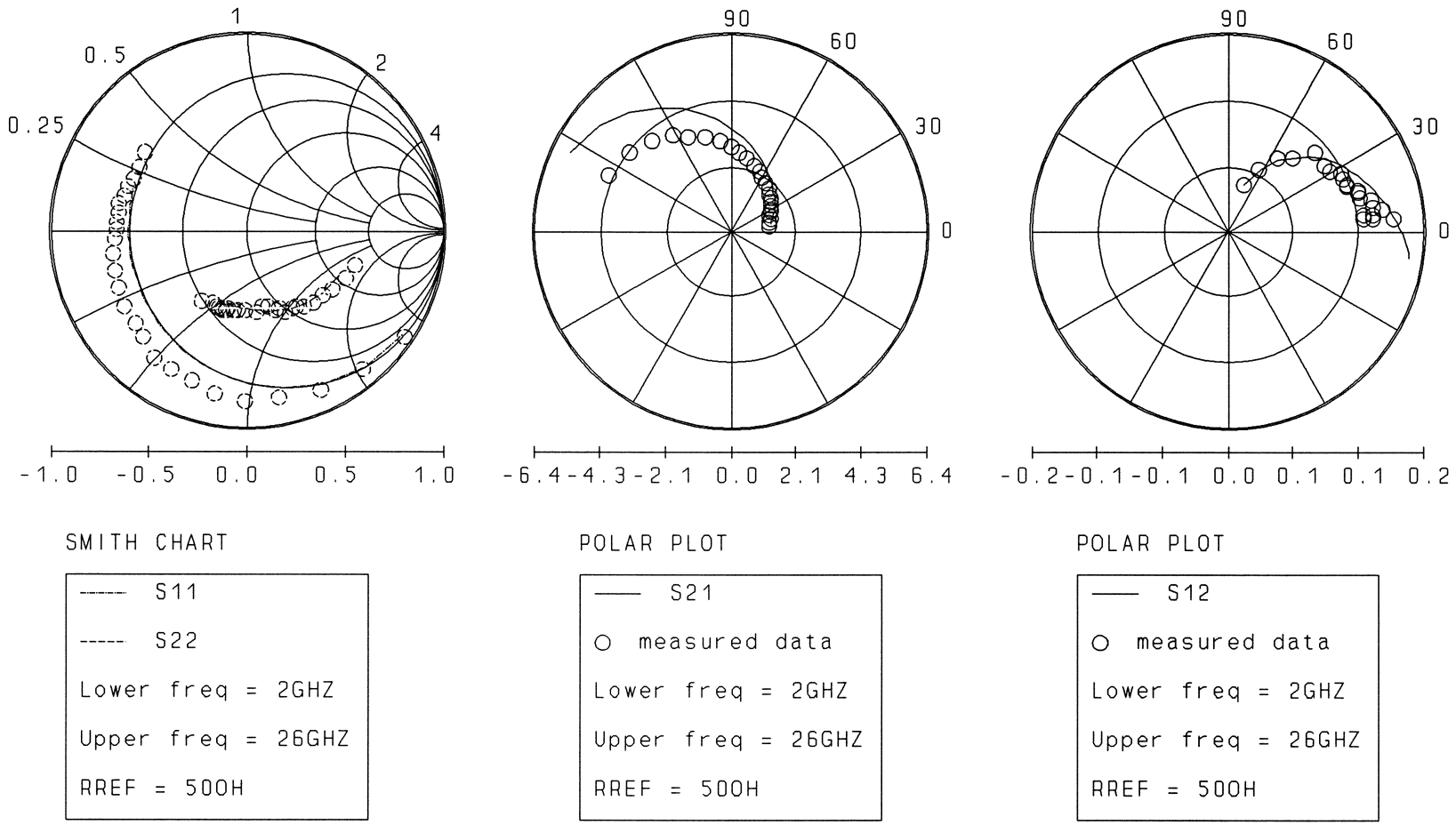

Fig. 3 *S*-parameter match between the model (solid and dashed lines) and typical transistor data (o) at $V_{ds} = 3$ V, $I_{ds} = 30$ mA [4].

III. NONLINEAR HARMONIC BALANCE SIMULATION

We use OSA90/hope to carry out the nonlinear harmonic balance (HB) simulation of the overall circuit with various component simulations, as summarized by the following three cases.

Case I: All microstrip components are simulated using OSA90/hope's built-in models. This naturally does not include couplings between the components.

Case II: The third harmonic stubs situated at the gate and drain ports of the FET are simulated by *em* [3]. This reflects the coupling between the two stubs.

Case III: In addition to the third harmonic stubs, the bias pads together with the radial stubs are also simulated by *em* [3]. This reflects the couplings in the biasing subcircuit as well as between the third harmonic stubs.

The conversion gain is calculated by

conversion gain = output power at the second harmonic / available input power.

The spectral purity is computed by

$$\text{spectral purity} = P_2 / (P_1 + P_3 + P_4)$$

where P_i is the output power at the ith harmonic.

A. Results for Case I:

In this case we simulate the circuit by considering all the microstrip elements as independent elements. We use OSA90/hope's built-in microstrip empirical models for all transmission lines, stubs, pads and discontinuities. This approach neglects any couplings between the components, in particular the third harmonic stubs situated at the gate and drain ports of the FET and the bias pads.

The output power, conversion gain and spectral purity versus input power at 7 GHz are shown in Figs. 4, 5 and 6, respectively. The output power, conversion gain and spectral purity versus frequency at 9 dBm input power are shown in Figs. 7, 8 and 9, respectively. A 3D view of conversion gain versus frequency and input power is given in Fig. 10. The source and output voltage waveforms at 7 GHz and 9 dBm input power are plotted in Fig. 11.

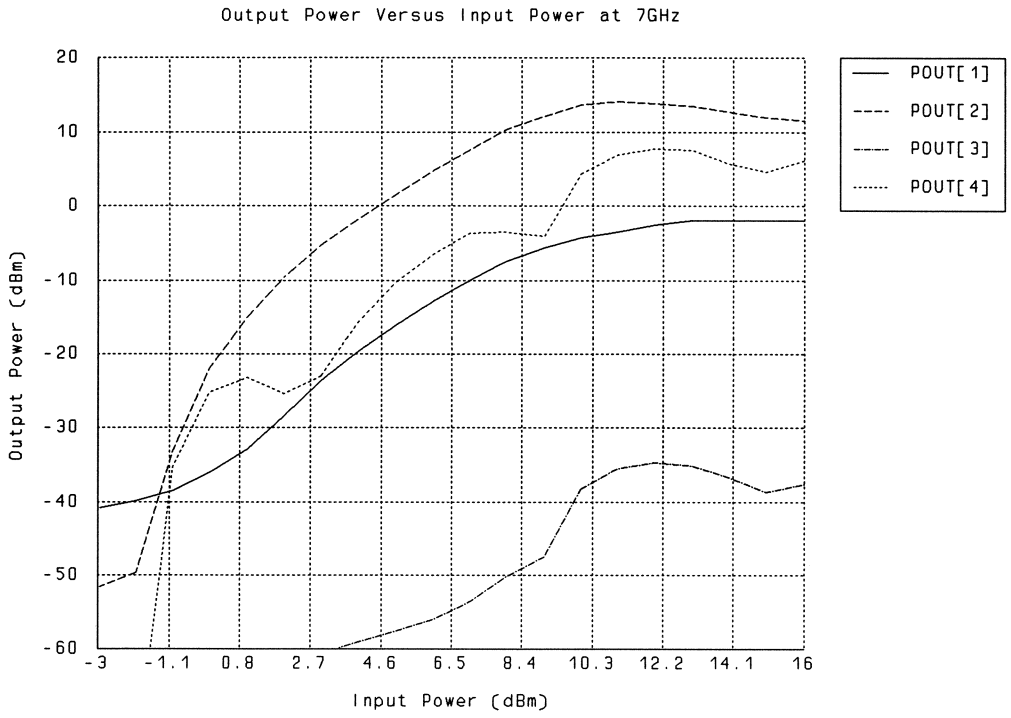

Fig. 4 Output power versus input power at 7 GHz. Couplings are not taken into account.

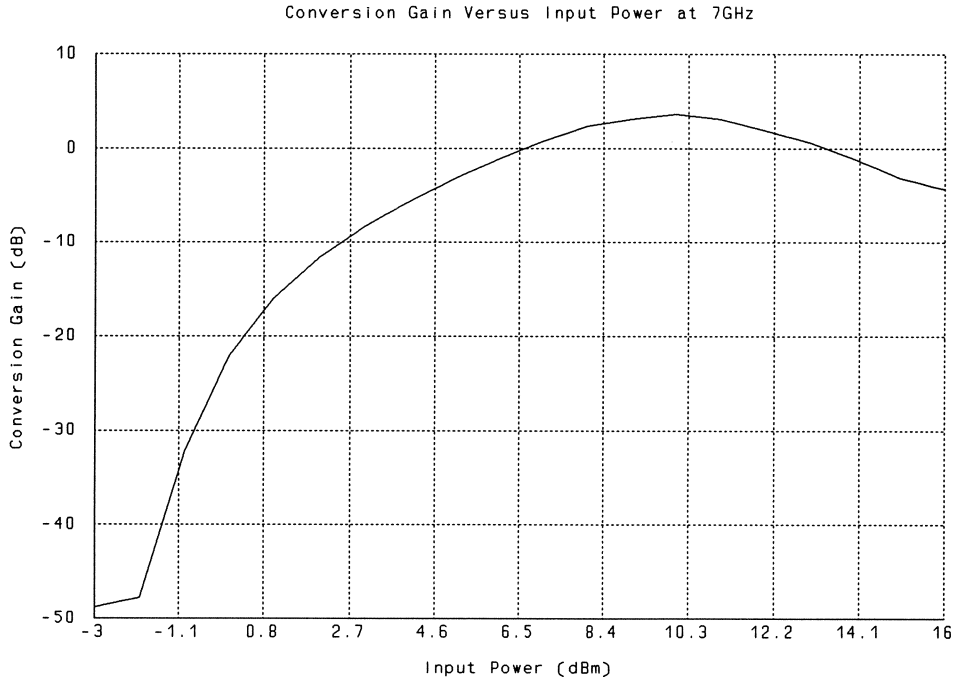

Fig. 5 Conversion gain versus input power at 7 GHz. Couplings are not taken into account.

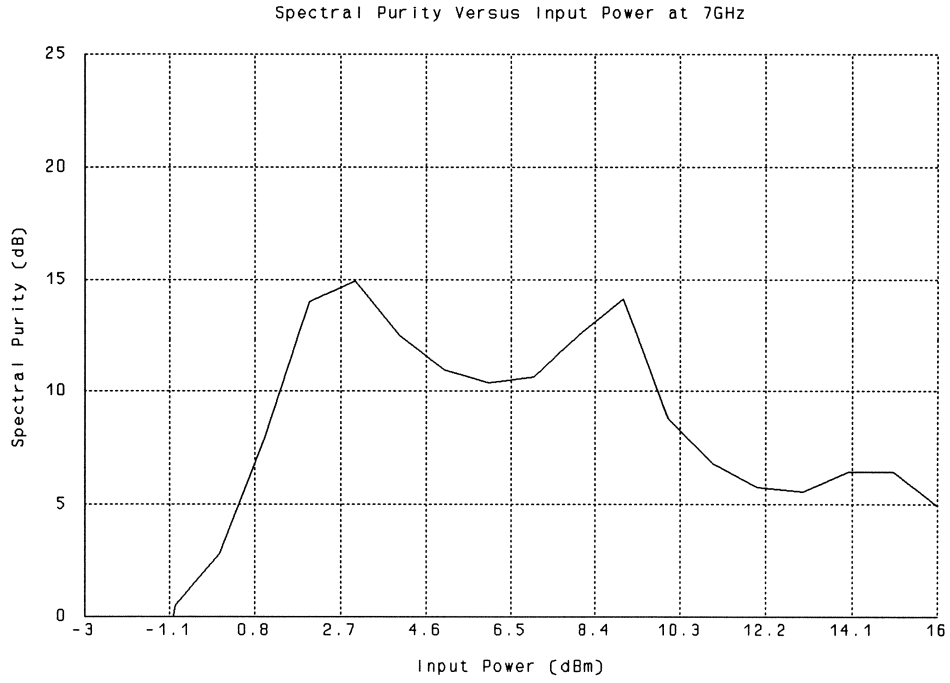

Fig. 6 Spectral purity versus input power at 7 GHz. Couplings are not taken into account.

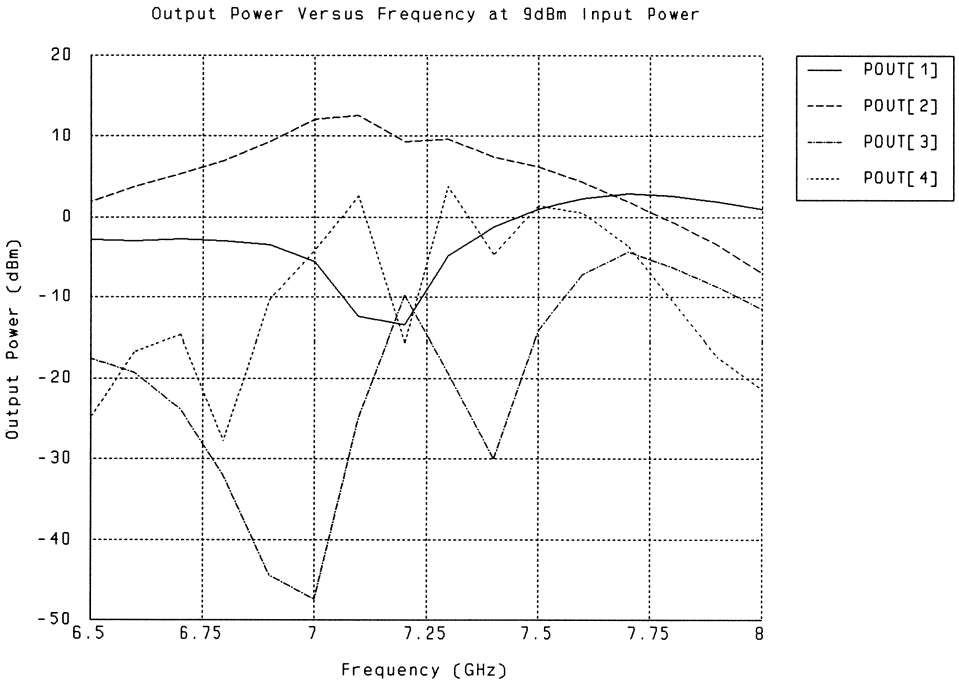

Fig. 7 Output power versus frequency at 9 dBm input power. Couplings are not taken into account.

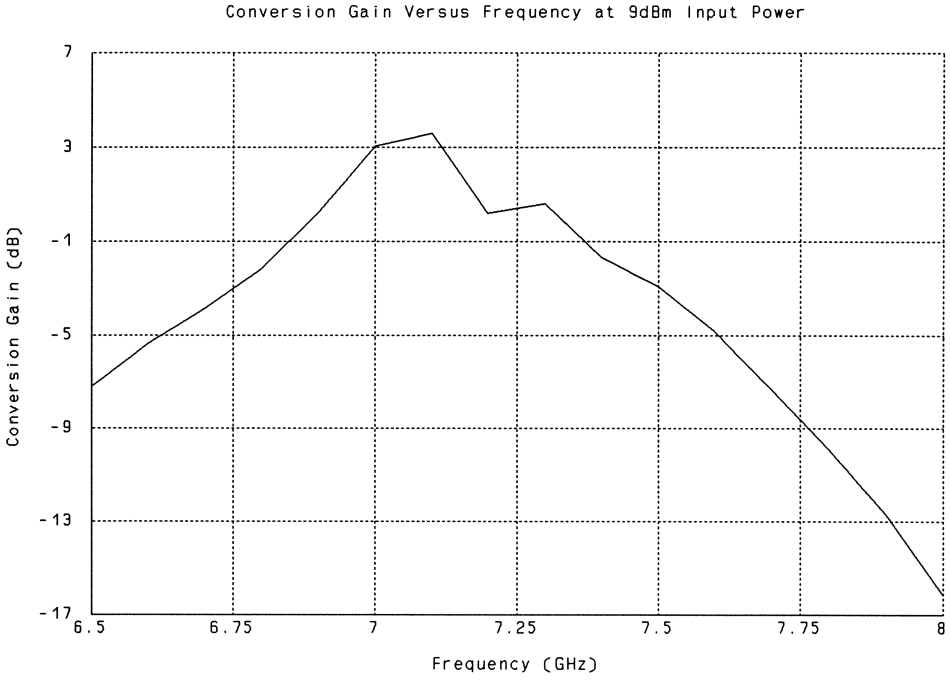

Fig. 8 Conversion gain versus frequency at 9 dBm input power. Couplings are not taken into account.

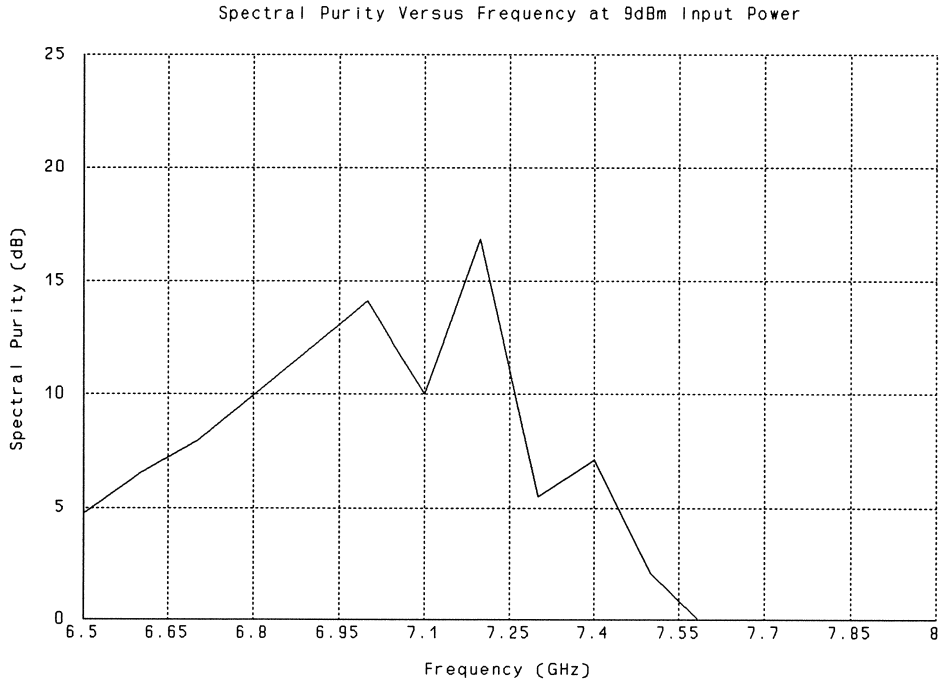

Fig. 9 Spectral purity versus frequency at 9 dBm input power. Couplings are not taken into account.

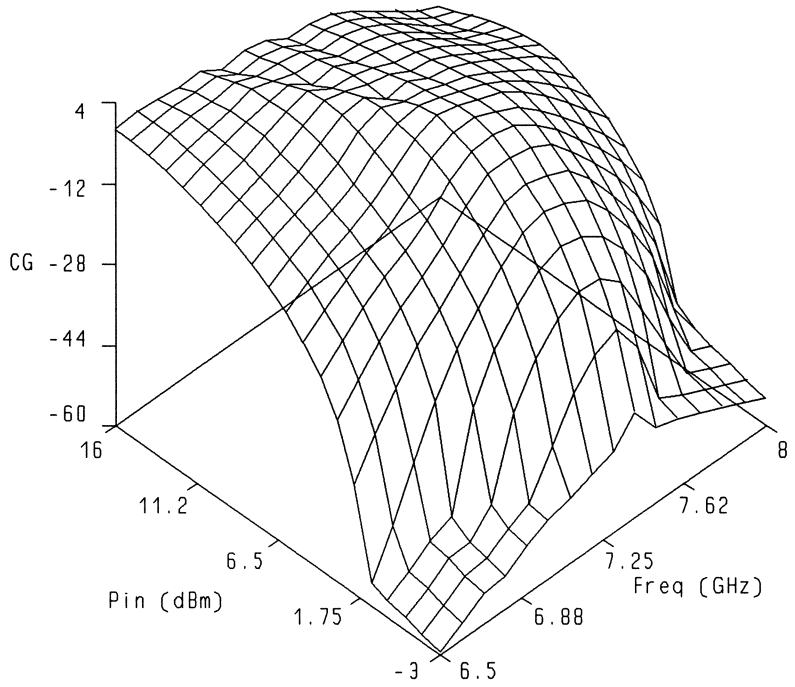

Fig. 10 3D view of conversion gain versus input power and frequency. Couplings are not taken into account.

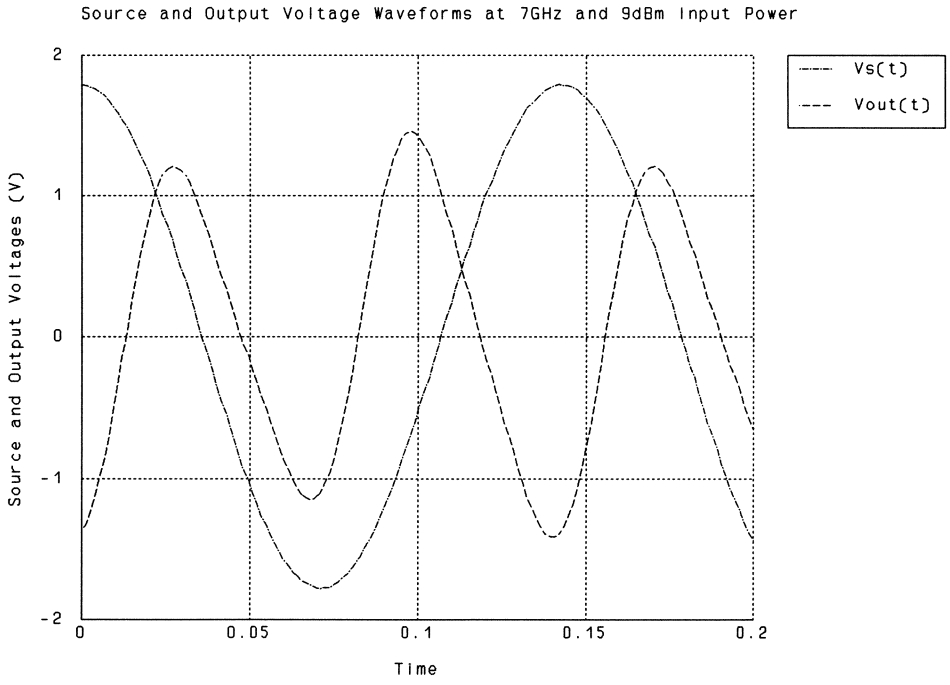

Fig. 11 Source and output voltage waveforms at 7 GHz and 9 dBm input power. Couplings are not taken into account.

B. Results for Case II:

In this case we consider the coupling effect of the third harmonic stubs situated at the gate and drain ports of the FET. Both stubs are considered as one four-port element which is simulated by ***em*** [3] and imported to OSA90/hope for circuit-level simulation.

The output power, conversion gain and spectral purity versus input power at 7 GHz are shown in Figs. 12, 13 and 14, respectively. The output power, conversion gain and spectral purity versus frequency at 9 dBm input power are shown in Figs. 15, 16 and 17, respectively. A 3D view of conversion gain versus frequency and input power is given in Fig. 18. The input and output voltage waveforms at 7 GHz and 9 dBm input power are plotted in Fig. 19.

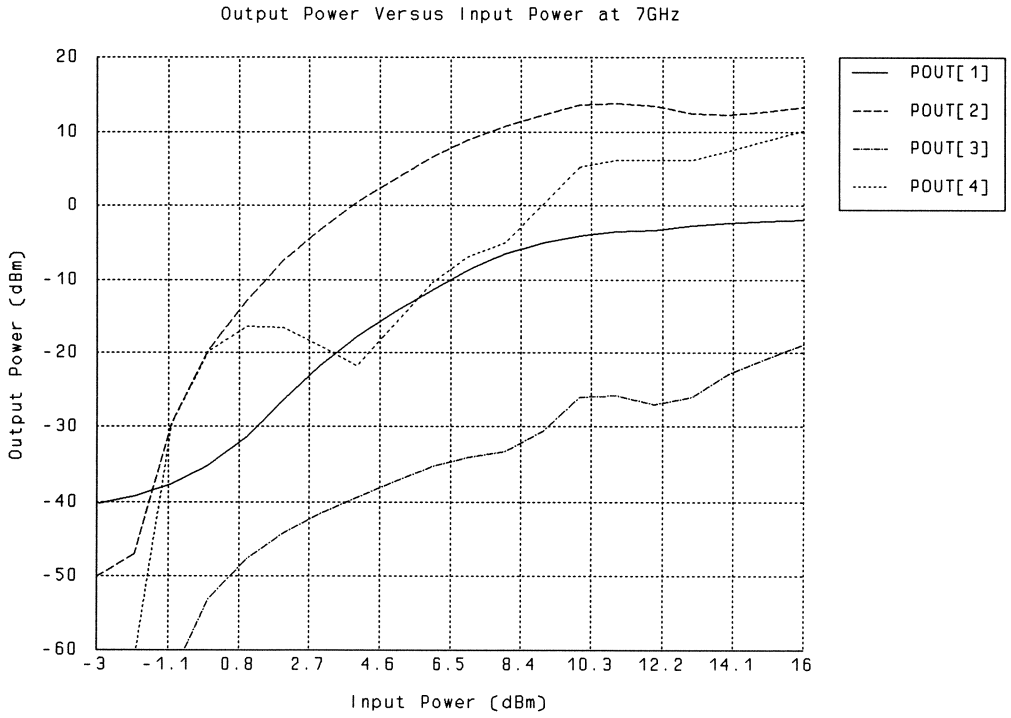

Fig. 12 Output power versus input power at 7 GHz. The coupling between the third harmonic stubs is simulated by ***em*** [3].

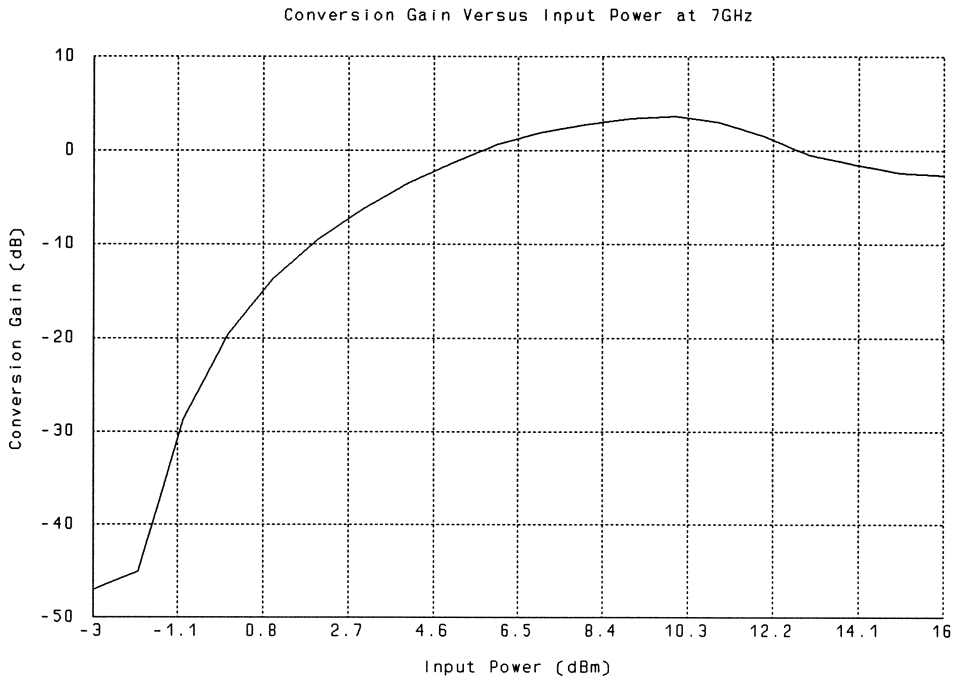

Fig. 13 Conversion gain versus input power at 7 GHz. The coupling between the third harmonic stubs is simulated by *em* [3].

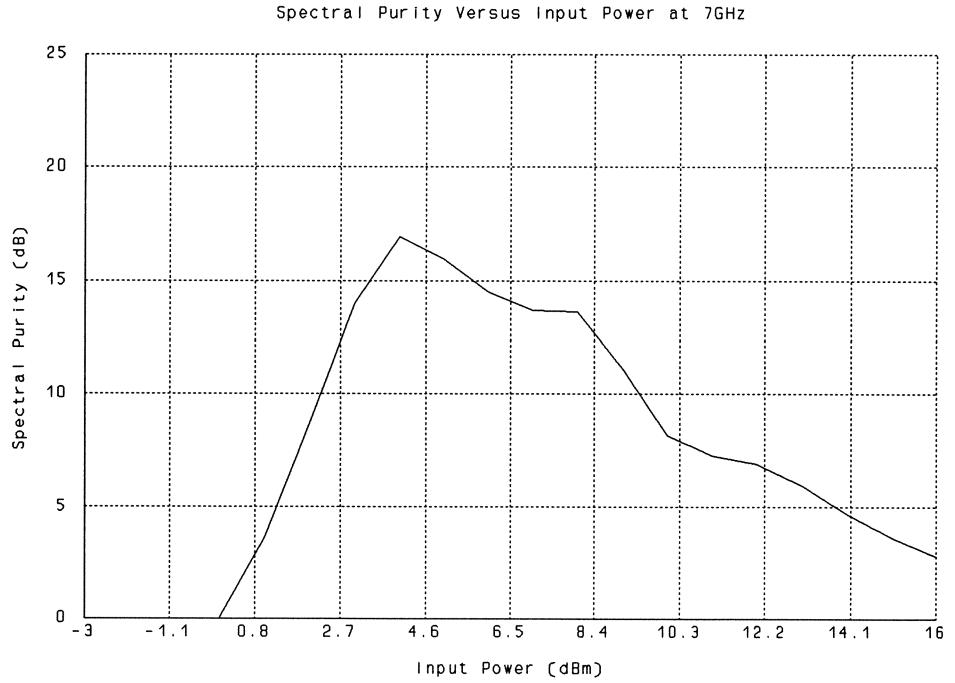

Fig. 14 Spectral purity versus input power at 7 GHz. The coupling between the third harmonic stubs is simulated by *em* [3].

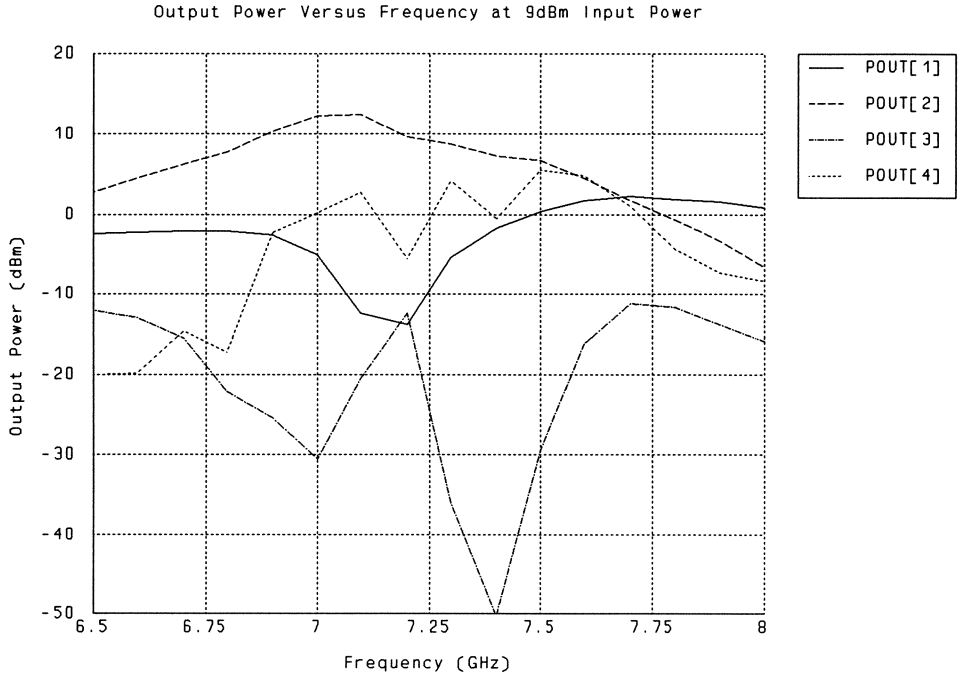

Fig. 15 Output power versus frequency at 9 dBm input power. The coupling between the third harmonic stubs is simulated by *em* [3].

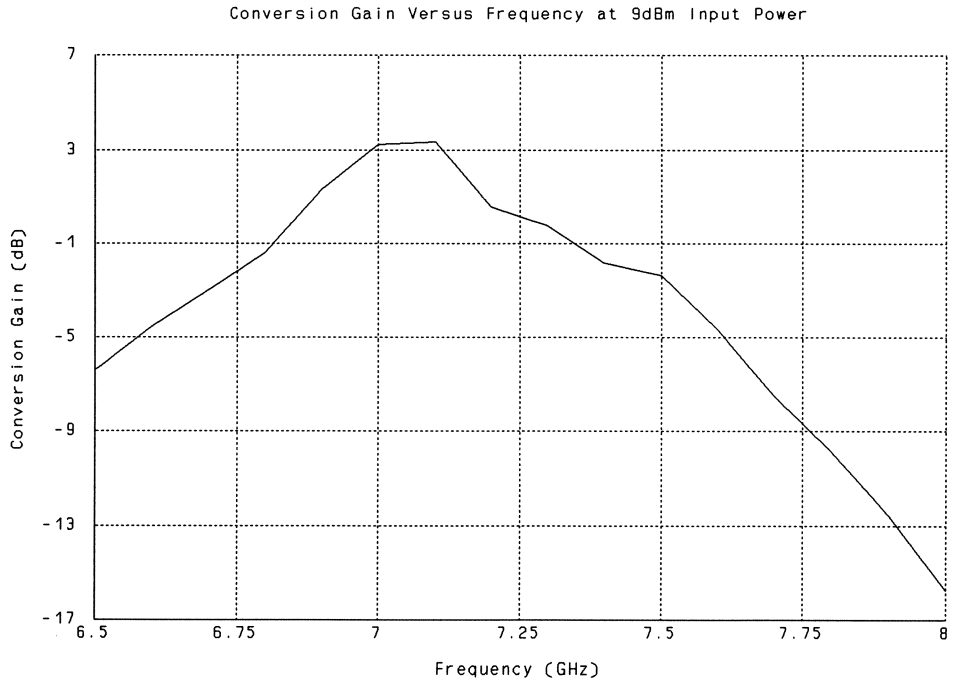

Fig. 16 Conversion gain versus frequency at 9 dBm input power. The coupling between the third harmonic stubs is simulated by *em* [3].

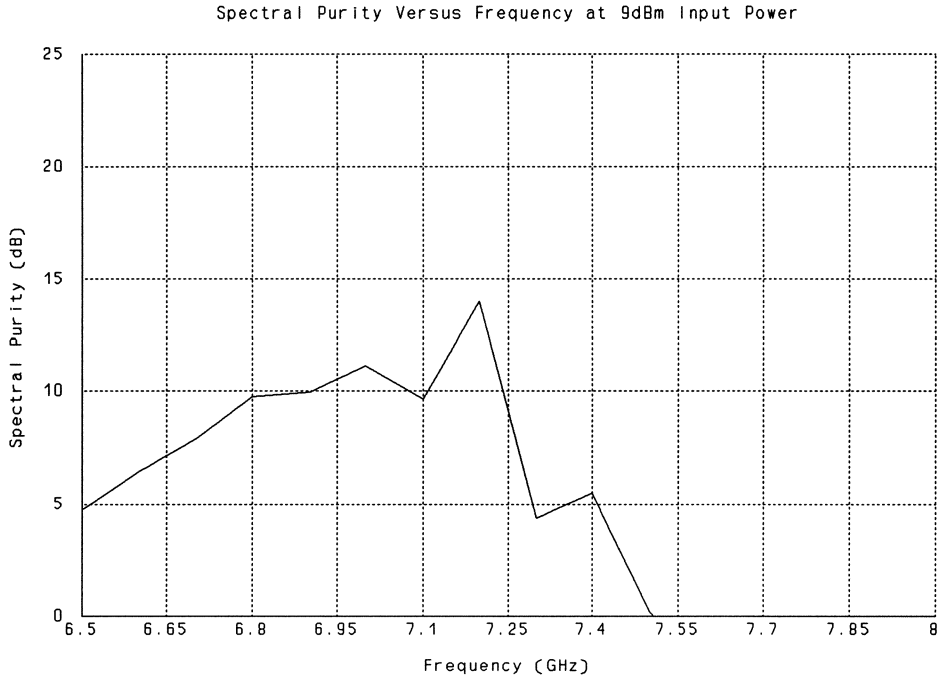

Fig. 17 Spectral purity versus frequency at 9 dBm input power. The coupling between the third harmonic stubs is simulated by ***em*** [3].

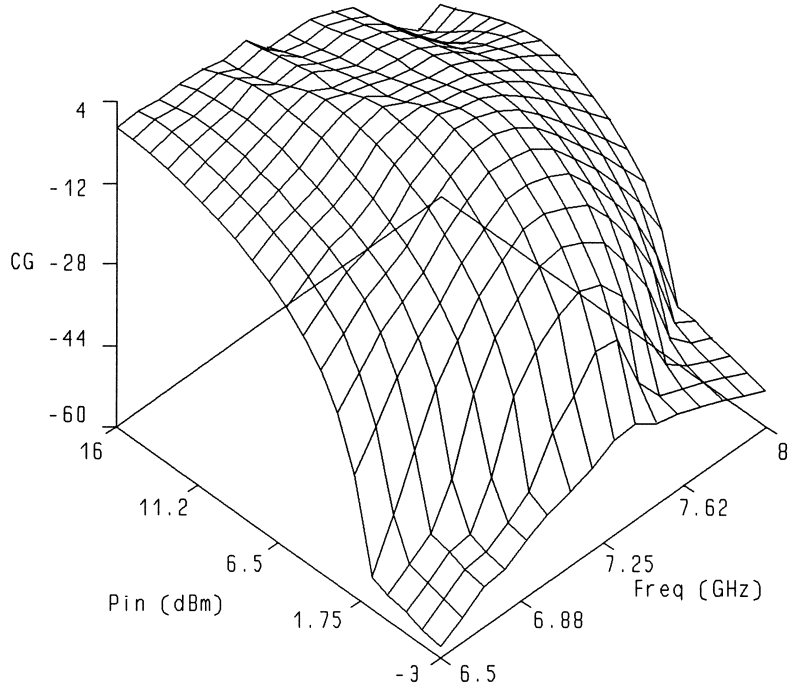

Fig. 18 3D view of conversion gain versus input power and frequency. The coupling between the third harmonic stubs is simulated by ***em*** [3].

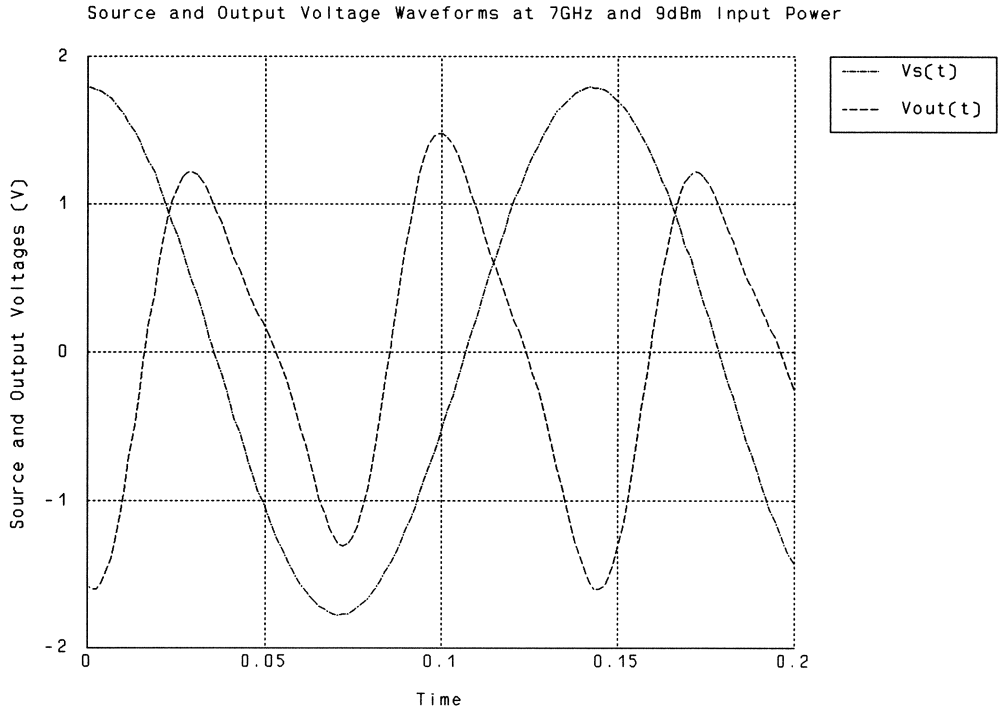

Fig. 19 Source and output voltage waveforms at 7 GHz and 9 dBm input power. The coupling between the third harmonic stubs is simulated by *em* [3].

Comparing Fig. 12 with Fig. 4 we can see that the output power at the third and fourth harmonics at 7 GHz of Case II are higher than those of Case I. Due to the coupling effect the resulting output waveform is slightly more distorted, as seen by comparing Figs. 11 and 19.

C. Results for Case III:

In this case we consider both the coupling of the third harmonic stubs situated at the gate and drain ports of the FET and the effect of the bias pads. In addition to the third harmonic stubs, each bias pad together with the adjacent radial stub is also simulated by *em* [3] as a two-port. These three subcircuits are simulated by *em* [3] and imported into OSA90/hope for overall circuit-level simulation. This reflects the couplings within those three subcircuits (the third harmonic stubs, the gate biasing circuit, and the drain biasing circuit).

The output power, conversion gain and spectral purity versus input power at 7 GHz are

shown in Figs. 20, 21 and 22, respectively. The output power, conversion gain and spectral purity versus frequency at 9 dBm input power are shown in Figs. 23, 24 and 25, respectively. A 3D view of conversion gain versus frequency and input power is given in Fig. 26. The input and output voltage waveforms at 7 GHz and 9 dBm input power are plotted in Fig. 27.

Comparing the results of this case with those of Case I and Case II, we can see that the effect of couplings between the bias pads and the radial stubs is quite significant. The output waveform is significantly distorted as seen from Fig. 27.

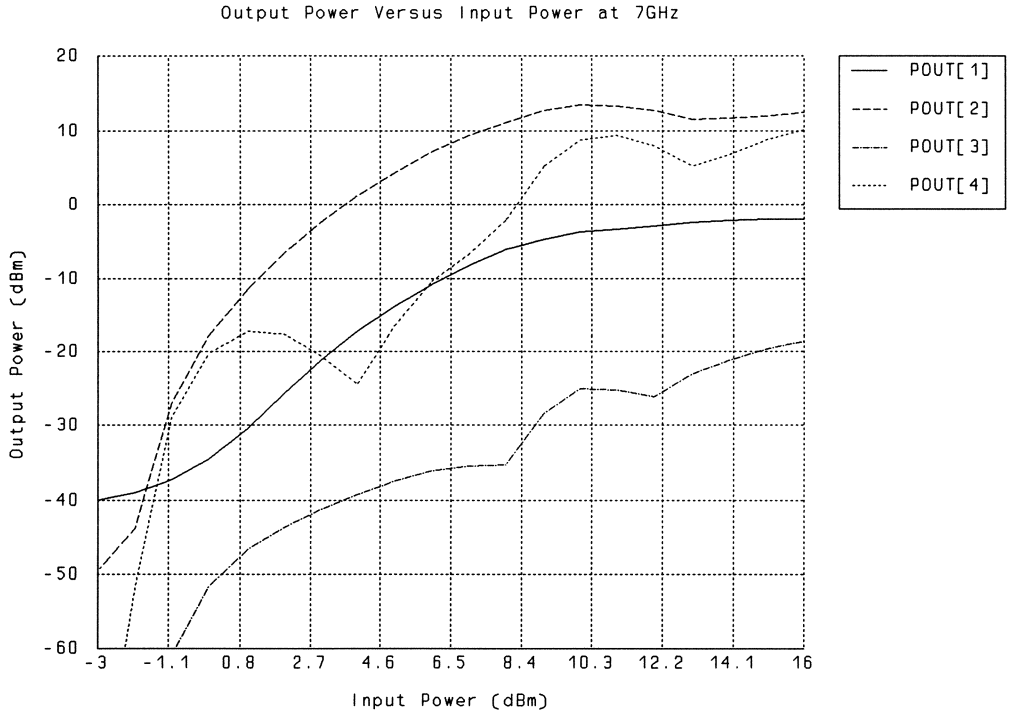

Fig. 20 Output power versus input power at 7 GHz. The couplings between the third harmonic stubs and between the bias pads and the corresponding radial stubs are simulated by ***em*** [3].

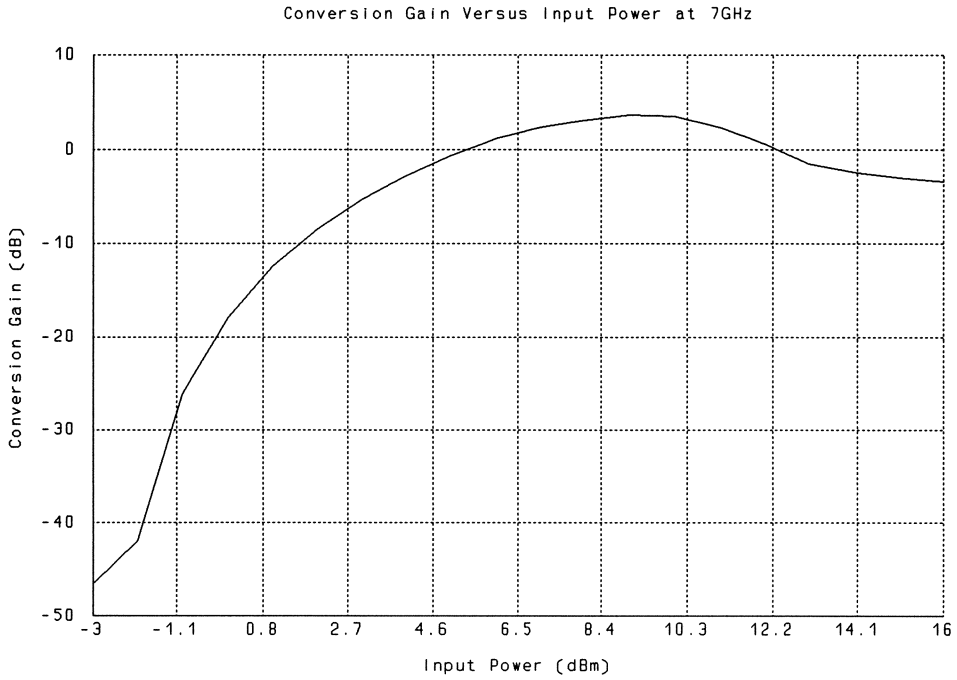

Fig. 21 Conversion gain versus input power at 7 GHz. The couplings between the third harmonic stubs and between the bias pads and the corresponding radial stubs are simulated by ***em*** [3].

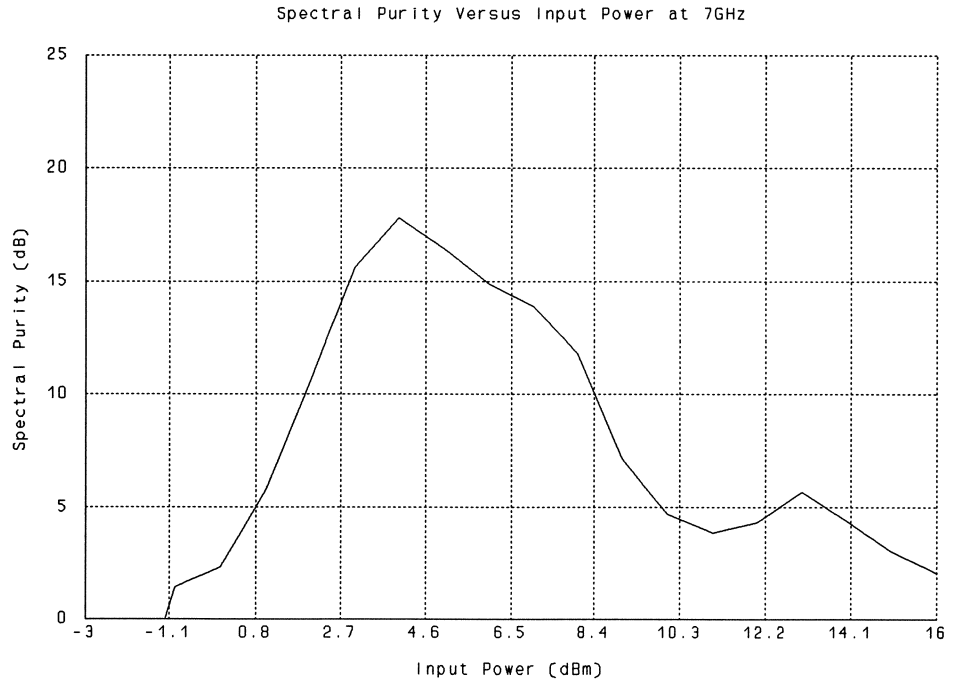

Fig. 22 Spectral purity versus input power at 7 GHz. The couplings between the third harmonic stubs and between the bias pads and the corresponding radial stubs are simulated by ***em*** [3].

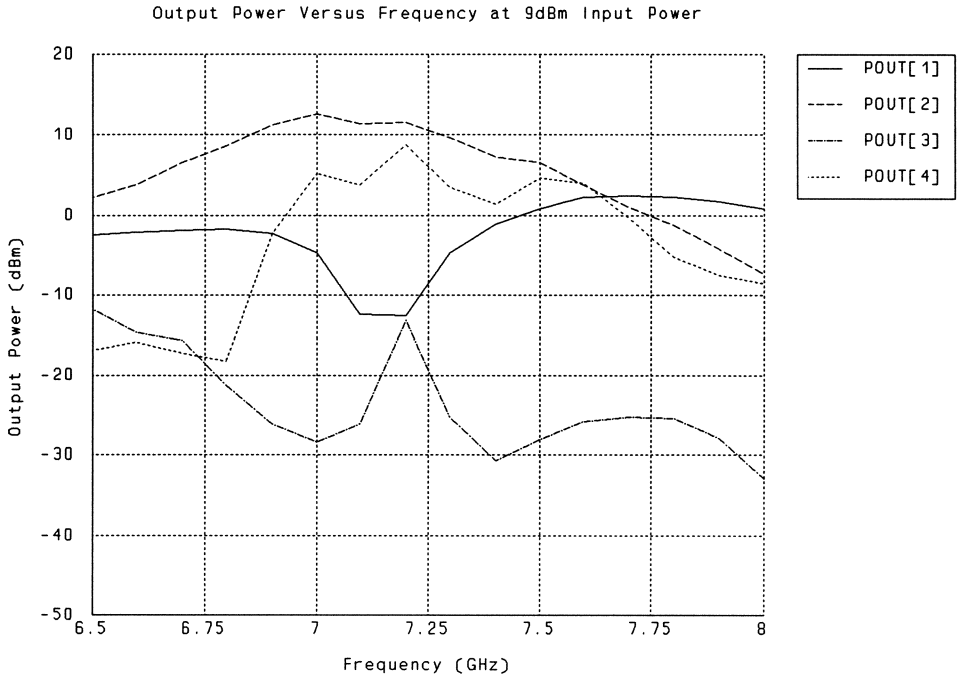

Fig. 23 Output power versus frequency at 9 dBm input power. The couplings between the third harmonic stubs and between the bias pads and the corresponding radial stubs are simulated by *em* [3].

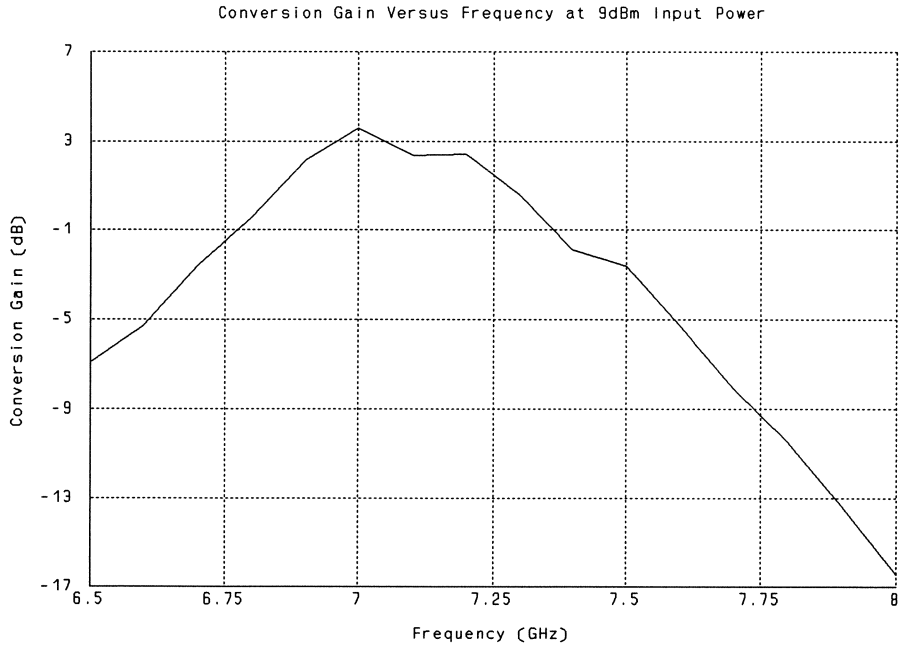

Fig. 24 Conversion gain versus frequency at 9 dBm input power. The couplings between the third harmonic stubs and between the bias pads and the corresponding radial stubs are simulated by *em* [3].

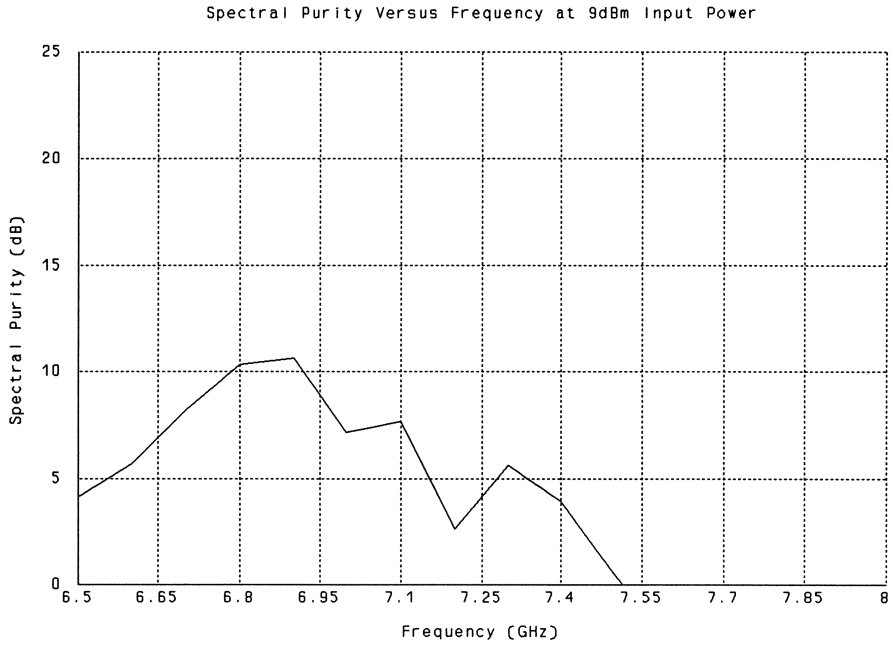

Fig. 25 Spectral purity versus frequency at 9 dBm input power. The couplings between the third harmonic stubs and between the bias pads and the corresponding radial stubs are simulated by *em* [3].

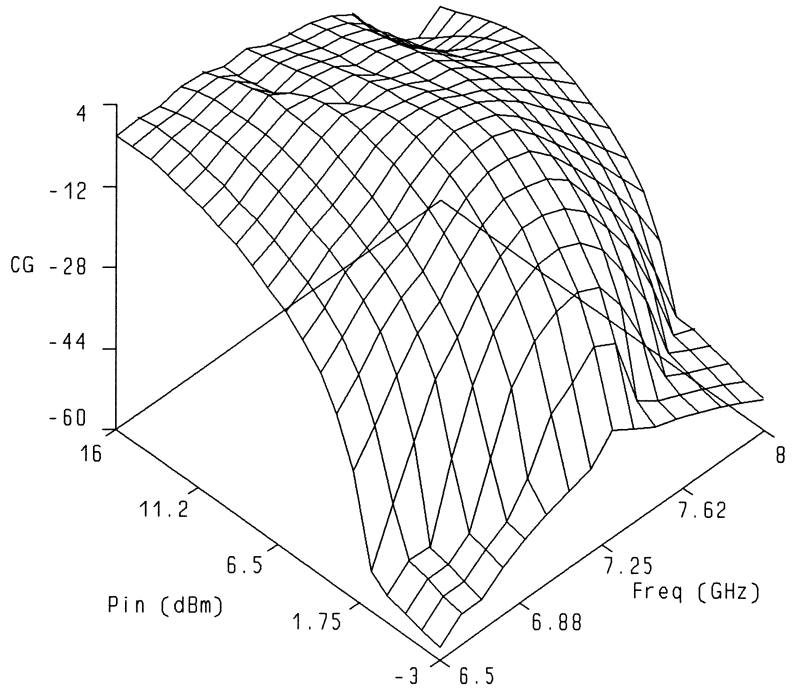

Fig. 26 3D view of conversion gain versus input power and frequency. The couplings between the third harmonic stubs and between the bias pads and the corresponding radial stubs are simulated by *em* [3].

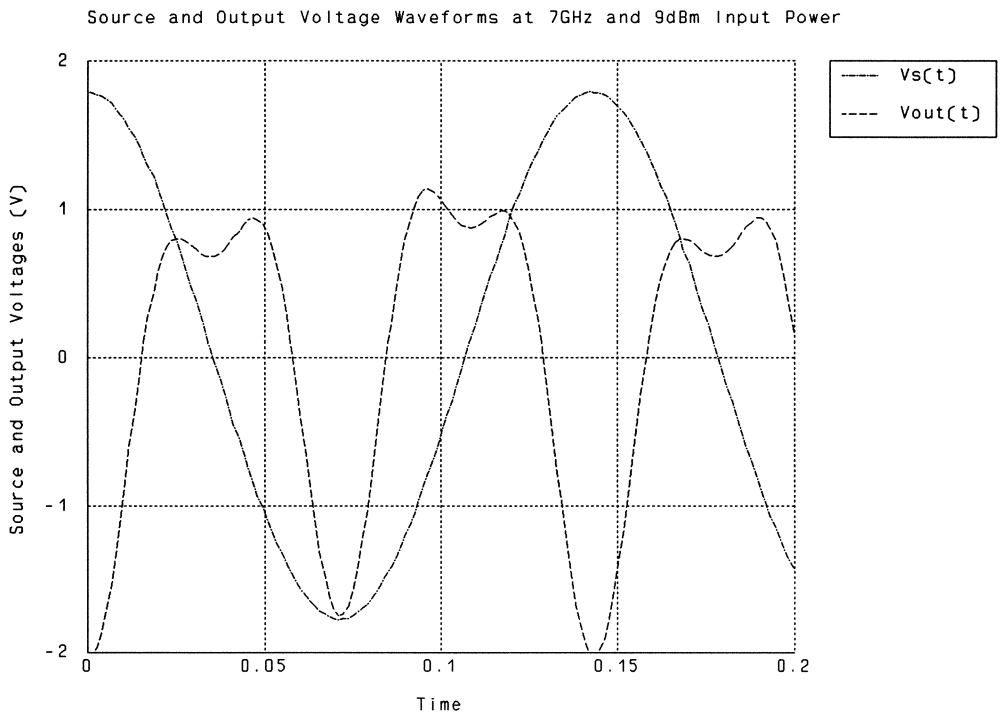

Fig. 27 Source and output voltage waveforms at 7 GHz and 9 dBm input power. The couplings between the third harmonic stubs and between the bias pads and the corresponding radial stubs are simulated by *em* [3].

IV. STATISTICAL ANALYSIS

To investigate the effect of the FET model uncertainty on the simulation result of the circuit, we perform statistical Monte Carlo analysis by assigning tolerances to the model parameters. A uniform distribution with 20 % tolerance is assigned to all model parameters. Monte Carlo analysis with OSA90/hope's built-in microstrip component models (as in Case I) is carried out using 50 outcomes.

The Monte Carlo sweep of the conversion gain and spectral purity versus input power at 7 GHz are shown in Figs. 28 and 29, respectively. The histograms of the conversion gain and spectral purity at 7 GHz and 9 dBm input power are shown in Figs. 30 and 31, respectively. The conversion gain at 7 GHz and 9 dBm input power are spread between -2.4 dB and 4.7 dB. The spectral purity at 7 GHz and 9 dBm input power are spread between 8.08 dB and 18.42 dB. This

reflects the model uncertainty. From these results we can see that the effect of doubling the frequency is not very sensitive to the transistor parameters, but the spectral purity of the output waveform is.

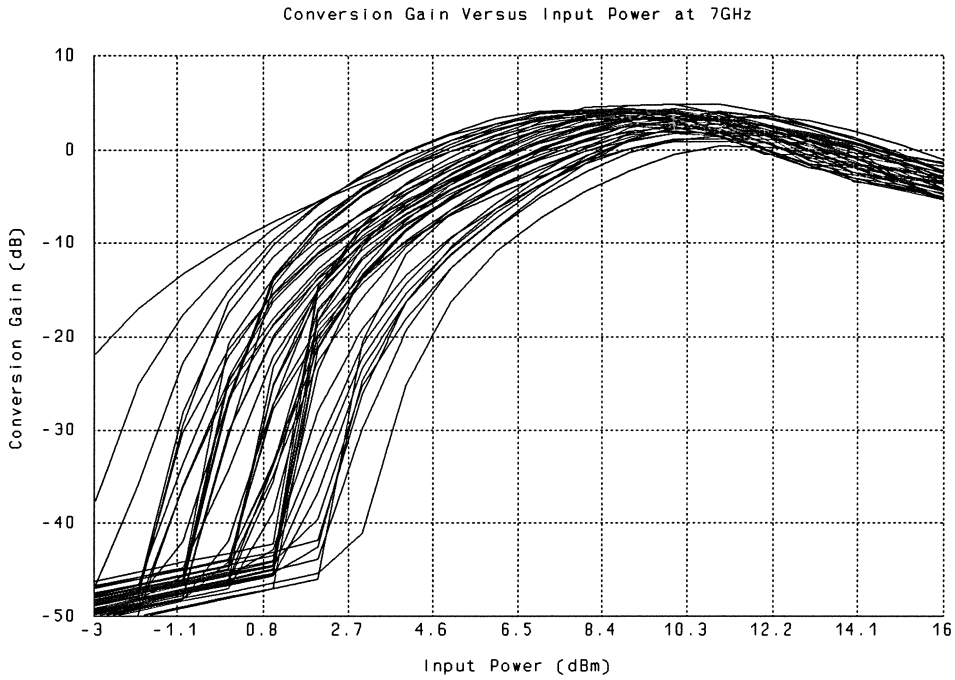

Fig. 28 Monte Carlo sweep of conversion gain versus input power at 7 GHz. Couplings are not taken into account.

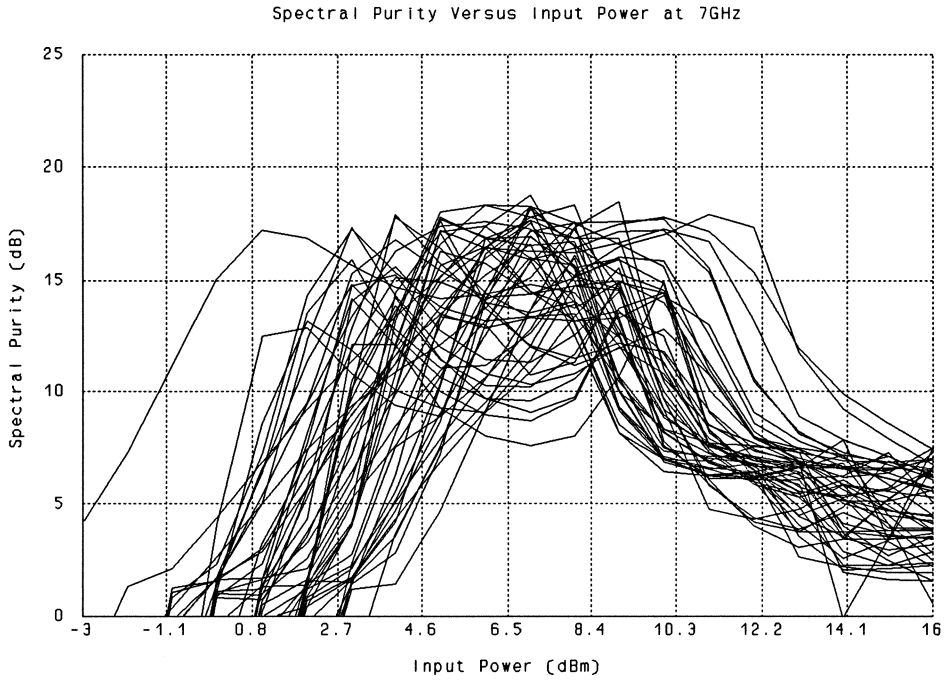

Fig. 29 Monte Carlo sweep of spectral purity versus input power at 7 GHz. Couplings are not taken into account.

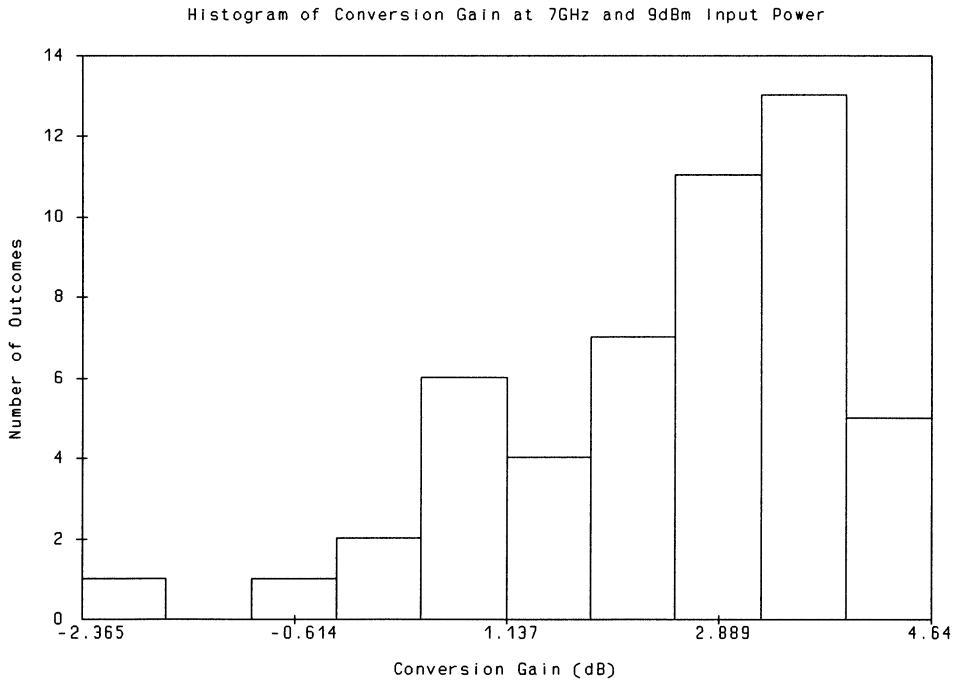

Fig. 30 Histogram of conversion gain at 7 GHz and 9 dBm input power. Couplings are not taken into account.

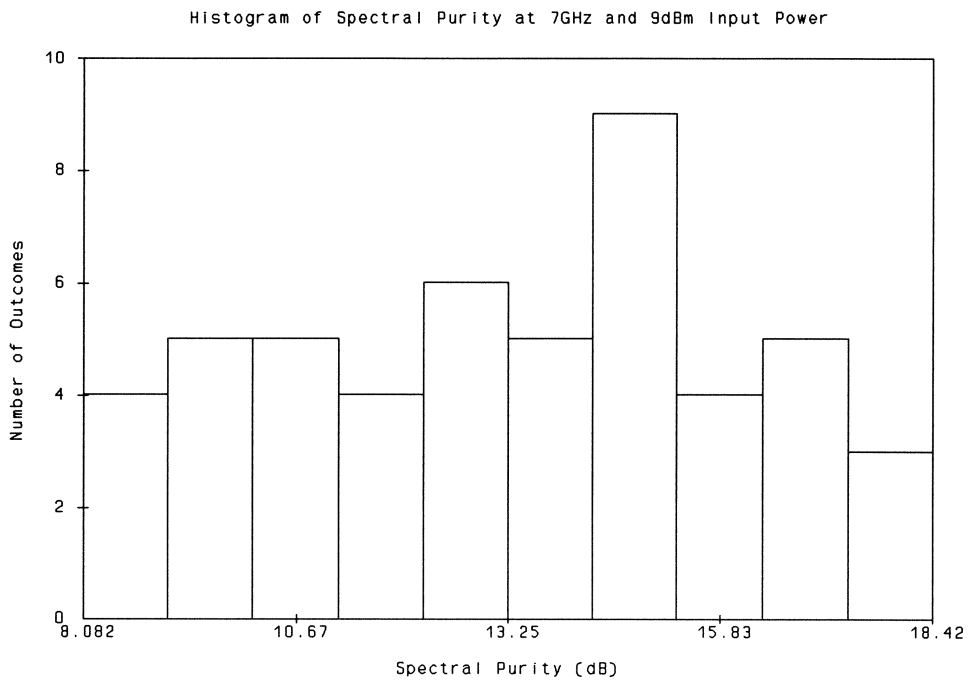

Fig. 31 Histogram of spectral purity at 7 GHz and 9 dBm input power. Couplings are not taken into account.

V. CIRCUIT OPTIMIZATION

In order to improve the responses of the doubler we use OSA90/hope to optimize the circuit. The specifications for optimization are

conversion gain > 3 dB
spectral purity > 20 dB

at 7 GHz and 9 dBm input power.

The optimization is performed based on the situation of Case III where both the coupling of the third harmonic stubs situated at the gate and drain ports of the FET and the effect of the bias pads are considered. A total of 15 variables are selected for optimization as indicated in Fig. 32.

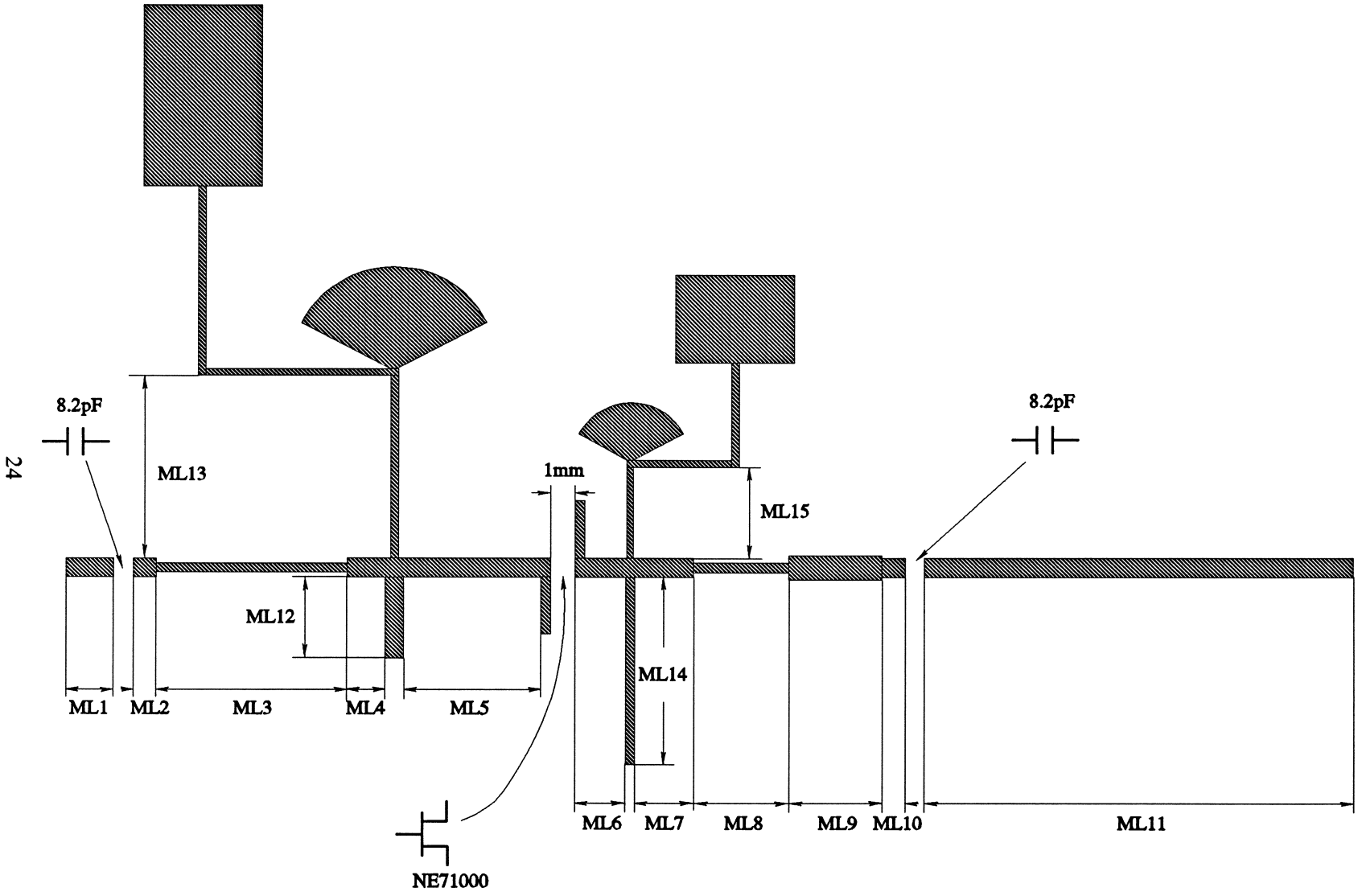

Fig. 32 The doubler circuit and optimization variables.

The minimax optimizer of OSA90/hope is used for this circuit optimization. All specifications are satisfied after optimization. The values of the variables before and after optimization are listed in Table II.

TABLE II
VARIABLE VALUES BEFORE AND AFTER OPTIMIZATION

Variable	Before Optimization	After Optimization
ML1	2.0	1.691
ML2	1.0	0.901
ML3	7.95	6.792
ML4	1.55	1.759
ML5	5.75	5.182
ML6	2.11 + 0.38	1.601 + 0.38
ML7	2.5	2.842
ML8	3.99	3.903
ML9	3.87	3.698
ML10	1	0.994
ML11	20	17.35
ML12	3.395	4.500
ML13	7.68	7.510
ML14	7.85	7.903
ML15	3.82	3.804

All dimensions are in mm.

From Table II we can see that the most influencing variables are ML3, ML11 and ML12. The output power, conversion gain and spectral purity versus input power at 7 GHz are shown in Figs. 33, 34 and 35, respectively. The output power, conversion gain and spectral purity versus frequency at 9 dBm input power are shown in Figs. 36, 37 and 38, respectively. A 3D view of conversion gain versus frequency and input power is given in Fig. 39. The input and output voltage waveforms at 7 GHz and 9 dBm input power are plotted in Fig. 40.

Comparing Figs. 33-40 with Figs. 20-27 we can see that better circuit performance is achieved after circuit optimization.

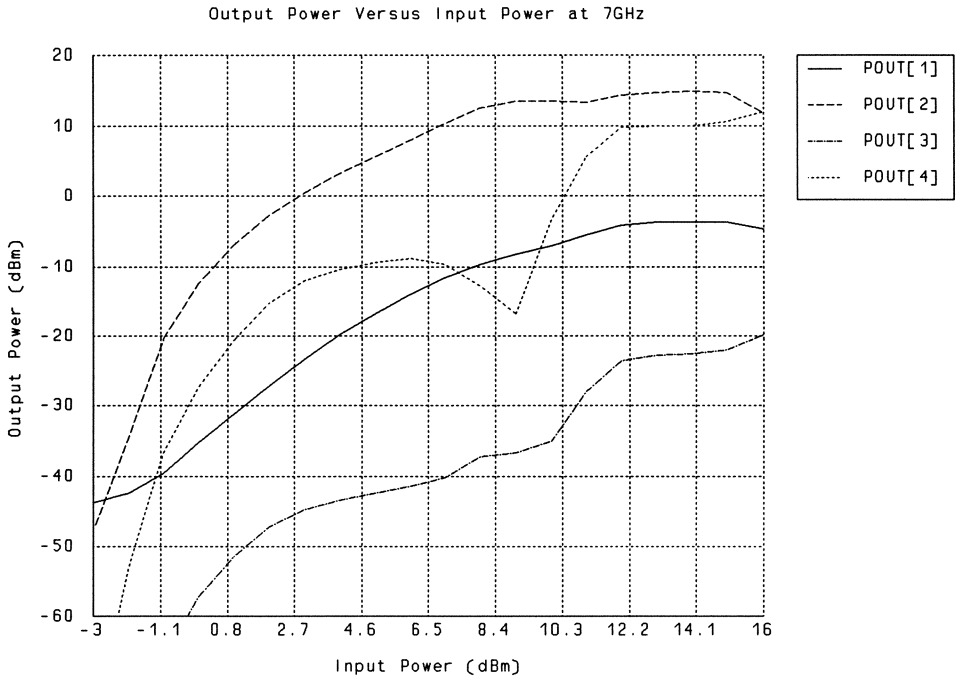

Fig. 33 Output power versus input power at 7 GHz after optimization. The couplings between the third harmonic stubs and between the bias pads and the corresponding radial stubs are simulated by *em* [3].

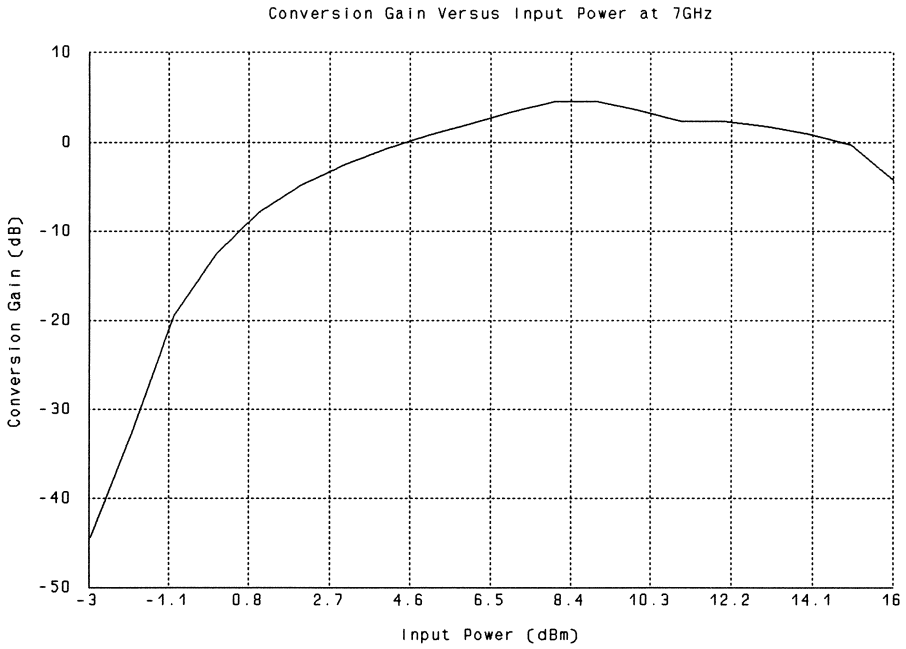

Fig. 34 Conversion gain versus input power at 7 GHz after optimization. The couplings between the third harmonic stubs and between the bias pads and the corresponding radial stubs are simulated by *em* [3].

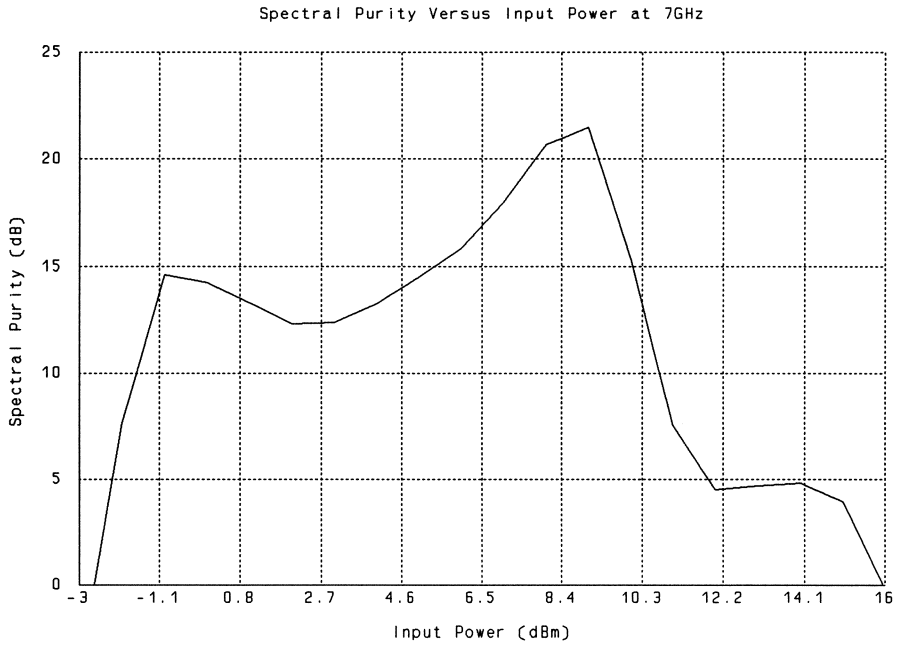

Fig. 35 Spectral purity versus input power at 7 GHz after optimization. The couplings between the third harmonic stubs and between the bias pads and the corresponding radial stubs are simulated by *em* [3].

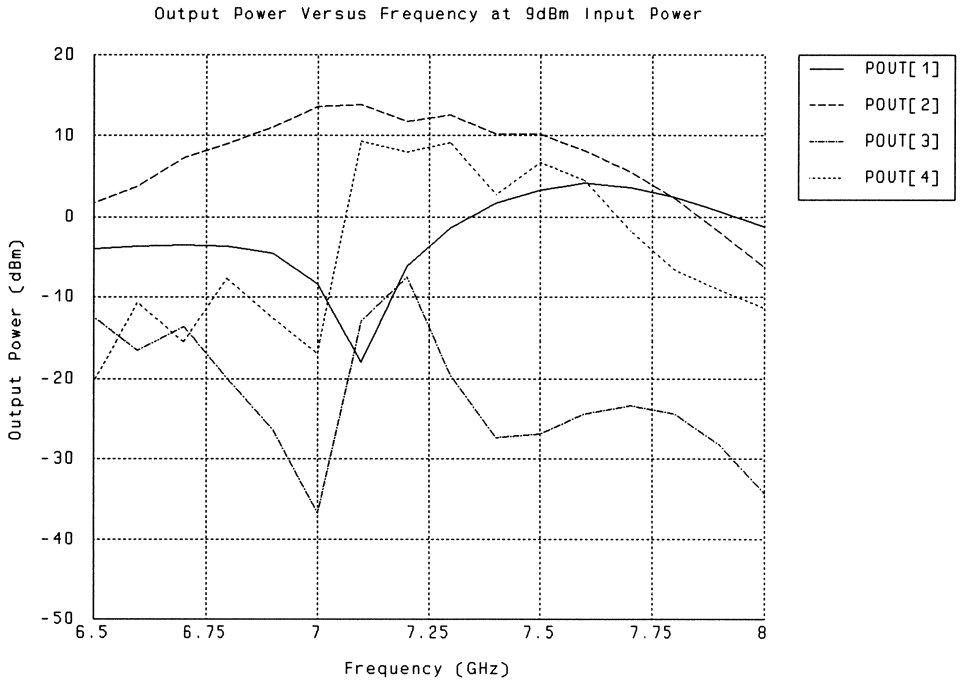

Fig. 36 Output power versus frequency at 9 dBm input power after optimization. The couplings between the third harmonic stubs and between the bias pads and the corresponding radial stubs are simulated by *em* [3].

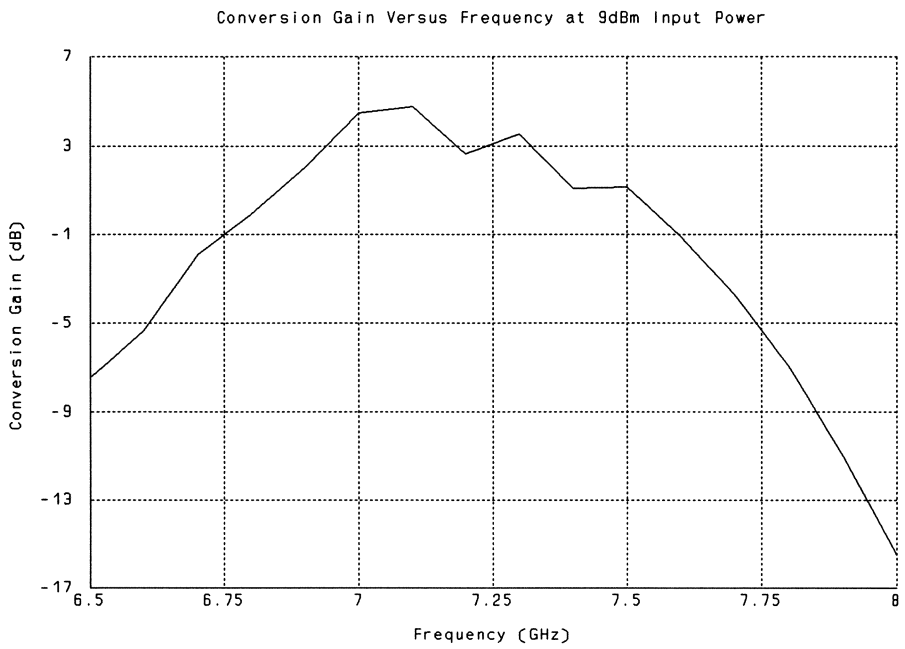

Fig. 37 Conversion gain versus frequency at 9 dBm input power after optimization. The couplings between the third harmonic stubs and between the bias pads and the corresponding radial stubs are simulated by *em* [3].

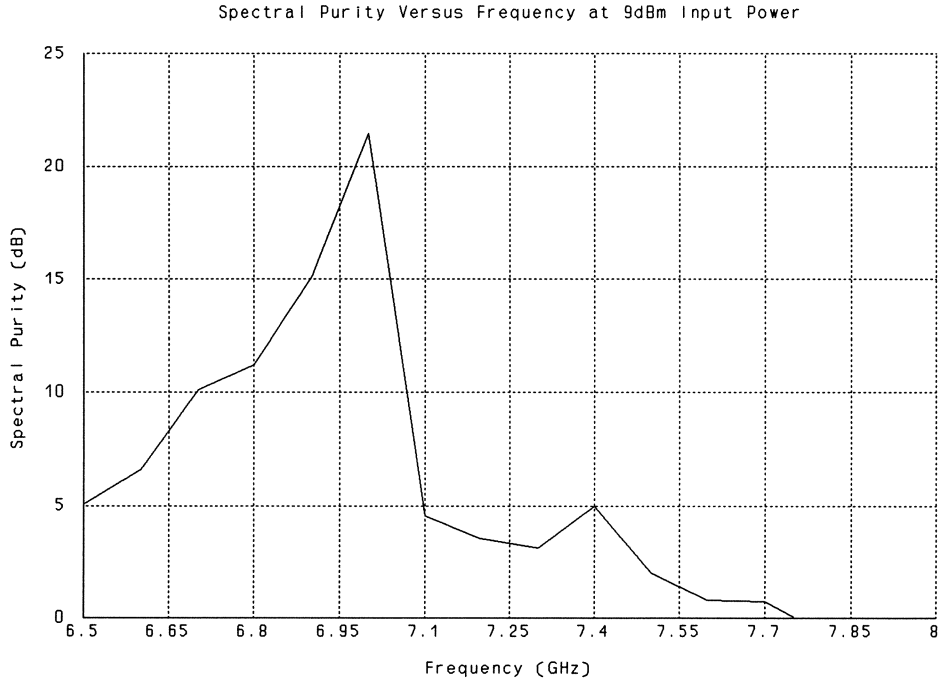

Fig. 38 Spectral purity versus frequency at 9 dBm input power after optimization. The couplings between the third harmonic stubs and between the bias pads and the corresponding radial stubs are simulated by *em* [3].

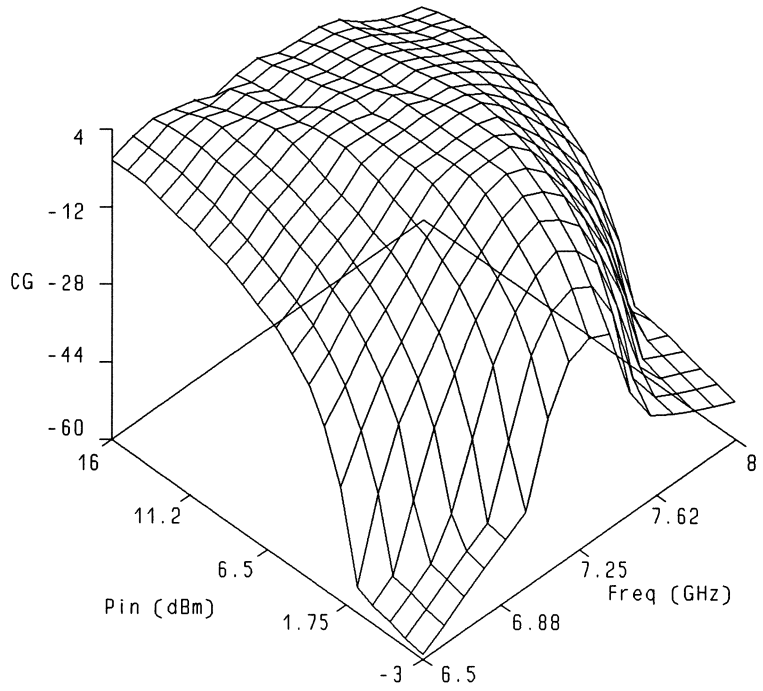

Fig. 39 3D view of conversion gain after optimization. The couplings between the third harmonic stubs and between the bias pads and the corresponding radial stubs are simulated by ***em*** [3].

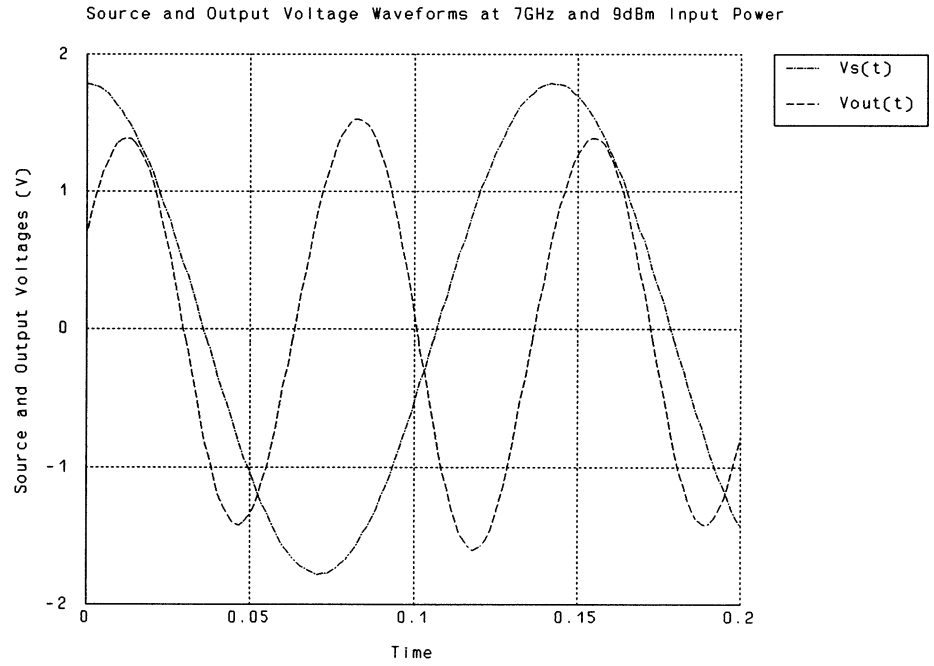

Fig. 40 Source and output voltages after optimization. The couplings between the third harmonic stubs and between the bias pads and the corresponding radial stubs are simulated by ***em*** [3].

VI SIMULATION TIME

All the experiments reported here were carried out on a Sun SPARCstation 10 workstation. The total time for simulating the complete circuit in Case I with the OSA90/hope built-in models for all the elements including the FET and distributed elements at 320 points (frequency: from 6.5 GHz to 8 GHz with 0.1 GHz step, input power: from -3 dBm to 16 dBm with 1 dBm step) is 1 minute and 45 seconds, about 0.3 second per point.

VII REFERENCES

[1] *HarPE*™, Optimization Systems Associates Inc., P.O. Box 8083, Dundas, Ontario, Canada L9H 5E7, 1993.

[2] *OSA90/hope*™, Optimization Systems Associates Inc., P.O. Box 8083, Dundas, Ontario, Canada L9H 5E7, 1993.

[3] *Em* Version 2.4, Sonnet Software, Inc., Suite 203, 135 Old Cove Road, Liverpool, NY 13090-3774, 1993.

[4] "RF and Microwave Semiconductors," *NEC Data Book*, California Eastern Laboratories, 1994.

APPENDIX: THE CIRCUIT FILE FOR CASE I

```
! dbl_c31.ckt
! Simulation of a Class B frequency doubler
! CAD benchmark example provided by Microwave Engineering Europe
! Model used: built-in Curtice and Ettenberg model extracted by HarPE
! The coupling between the 2 stubs at gate and drain and the effect
! of bias pads are not considered
! All the distributed elements are modelled by OSA90/hope's built-in models

Model
   MSUB  EPSR=2.2  H=0.254mm  T=0.0178mm  ROC=2.44e-8  RHS=0.001mm;

   MSL    1   2   W=0.76mm   L=2.0mm;
   CAP    2   3   C=8.2pf;
   MSL    3   4   W=0.76mm   L=1.0mm;
   MSTEP  4   5   W1=0.76mm  W2=0.4mm;
   MSL    5   6   W=0.4mm    L=7.95mm;
   MSTEP  6   7   W1=0.4mm   W2=0.76mm;
   MSL    7   8   W=0.76mm   L=1.55mm;
   MCROSS 10  8  9  11  W1=0.76mm  W2=0.76mm  W3=0.3mm;
   MSL    11  12  W=0.76mm   L=5.75mm;
   MTEE   12  13  14  W1=0.76mm  W2=0.38mm  W3=0.76mm;
   MTEE   15  16  17  W1=0.76mm  W2=0.38mm  W3=0.76mm;
   MSL    17  18  W=0.76mm   L=2.11mm;
   MCROSS 20  18  21  19  W1=0.38mm  W2=0.76mm  W3=0.3mm;
   MSL    19  22  W=0.76mm   L=2.5mm;
   MSTEP  22  23  W1=0.76mm  W2=0.38mm;
   MSL    23  24  W=0.38mm   L=3.99mm;
   MSTEP  24  25  W1=0.38mm  W2=1.04mm;
   MSL    25  26  W=1.04mm   L=3.87mm;
   MSTEP  26  27  W1=1.04mm  W2=0.76mm;
   MSL    27  28  W=0.76mm   L=1mm;
   CAP    28  29  C=8.2pf;
   MSL    29  30  W=0.76mm   L=20mm;
   MSL    10  31  W=0.76mm   L=3.395mm;
   OPEN   31;
   MSL    13  32  W=0.38mm   L=2.4mm;
   OPEN   32;
   MSL    16  42  W=0.38mm   L=2.4mm;
   OPEN   42;
   MSL    20  33  W=0.38mm   L=7.85mm;
   OPEN   33;
   MSL    9   34  W=0.3mm    L=7.68mm;
   MTEE   34  35  36  W1=0.3mm  W2=0.3mm  W3=0.3mm;
   MSL    36  37  W=0.3mm    L=7.68mm;
   MBEND2 37  38  W=0.3mm;
   MSL    38  39  W=0.3mm    L=7.68mm;
   MSTEP  39  40  W1=0.3mm   W2=5.0mm;
   MSL    40  41  W=5.0mm    L=7.42mm;
   MSL    21  43  W=0.38mm   L=3.82mm;
   MTEE   43  44  45  W1=0.3mm  W2=0.3mm  W3=0.3mm;
   MSL    45  46  W=0.3mm    L=4.1mm;
   MBEND2 46  47  W=0.3mm;
   MSL    47  48  W=0.3mm    L=4.1mm;
   MSTEP  48  49  W1=0.3mm   W2=5.0mm;
   MSL    49  50  W=5.0mm    L=3.7mm;
   MRSTUB 35  W=0.3mm  L=4.45mm  ANG=130;
   MRSTUB 44  W=0.3mm  L=2.3mm   ANG=130;

   EXTRINSIC4  141 142 143 14 15
       RG=1.33301       RD=0.888452       RS=5.04386
       CDS=0.0414509pF  GDS=0.00441929    CX=100pF
       LG=0.160598nH    LD=5.3121e-06nH   LS=0.0718402nH
       CGE=0.143109pF   CDE=0.0924559pF;
```

```
   FETC 141 142 143
       A0=0.0826627   A1=0.335942      A2=0.367757      A3=0.00858573
       GAMMA=1.86239  BETA=0.121412    VDS0=0.742967    IS=5.26136e-11
       N=3.28559      CGD0=0.108206pF  CGS0=0.227312pF  FC=0.173912e-12
       Tau=1.0947ps   Gmin= 0.841032e-12;

   VGS=-1.2;
   VDS=3;
   IND      41   411 L=1000nH;
   IND      50   501 L=1000nH;
   VSOURCE 411   0   NAME=B_VGS  VDC=VGS;
   VSOURCE 501   0   NAME=B_VDS  VDC=VDS;

   PIN = 9dBm;
   PORT.in  1  0  P[1]=PIN  R=50;
   PORT     30  0  NAME=OUT  R=50;

   CIRCUIT;

   Pout[0:N_SPECTRA] = if (PWout > 0) (10 * log10(PWout) + 30) else (NAN);

   Vs: sqrt(400 * 10^((Pin - 30)/10));
   MVs[0:N_SPECTRA] = [0 Vs 0 0 0];
   PVs[0:N_SPECTRA] = 0;

   Conversion_Gain = POUT[2] - PIN;
End

Sweep
   HB: FREQ: 7GHZ Pin: from -3dBm to 16dBm step=1dBm
       Pout Conversion_Gain MVout PVout MVs PVs
       {Xsweep title="Output Power Versus Input Power at 7GHz"
        Y=Pout[1].green & Pout[2].red & Pout[3].yellow & Pout[4].pink
        NXticks=10  Ymin=-60 Ymax=20 NYticks=8}
       {Xsweep title="Conversion Gain Versus Input Power at 7GHz"
        Y=Conversion_gain.green NXticks=10 Ymin=-50 Ymax=10 NYticks=6}
       {Waveform  Title="Frequency Doubler Source and Output Voltage Waveforms"
        Spectrum=(MVs, PVs)."Vs(t)" & (MVout, PVout)."Vout(t)"
        Tmin=0 Tmax=0.2 NT=150  Ymin=-2 Ymax=2 NYTicks=4 pin=9};

   HB: FREQ: from 6.5GHZ to 8GHZ step 0.1GHZ
       Pin: from -3dBm to 16dBm step=1dBm
       Pout Conversion_Gain
       {Xsweep title="Output Power Versus Frequency at 9 dBm Input Power"
        Y=Pout[1].green & Pout[2].red & Pout[3].yellow & Pout[4].pink
        NXticks=6  Ymin=-50 Ymax=20 NYticks=7 Pin=9}
       {Xsweep title="Conversion Gain Versus Frequency at 9 dBm Input Power"
        Y=Conversion_Gain.green NXticks=6  Ymin=-17 Ymax=7 NYticks=6 Pin=9}
       {Visual Z=Conversion_Gain Z_title="CG" Zmin=-60 Zmax=4 Lines=ON
        Frame=OFF Paint=OFF Smooth=ON}
End
```