Spicepipe - A CASE STUDY OF FLEXIBLE CIRCUIT OPTIMIZATION

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Abstract

This paper is concerned with the problem of applying efficient and powerful optimization techniques to drive various simulators in a flexible and versatile manner. In particular, we present Spicepipe, an interface between the optimization environment of OSA90/hope™ and SPICE-PAC, a modular version of SPICE. Powerful features of OSA90/hope's state-of-the-art design optimization, which includes user-definable expressions and objective functions, statistical capabilities, as well as built-in linear and nonlinear frequency-domain simulation, are combined with SPICE-PAC's time-domain simulation, noise analysis, device models, etc. For the first time, techniques such as the one-sided ℓ_1 yield optimization, with a proven track record in frequency-domain applications, can be applied to time-domain or simultaneous time- and frequency-domain yield optimization. Quadratic modeling for yield optimization also becomes available for time-domain applications to significantly reduce the simulation cost. Spicepipe utilizes the efficient, high-speed Datapipe technology of OSA90/hope and exemplifies our approach to and the benefits of flexible circuit design optimization with independent simulators, regardless of their nature. Our approach is illustrated by examples involving simulation, optimization, Monte Carlo analysis and yield-driven design in both the frequency and time domains.

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SUMMARY

Introduction

Circuit CAD is supported by a great variety of software tools, each addressing a different aspect of circuit design. However, solving complex design problems requires efficient and flexible interaction between systems featuring optimization, statistical analysis, post-processing of results, etc., on the one hand and various simulators on the other. Commercially available general purpose CAD systems do not address all these aspects adequately. Optimization capabilities of such systems are typically limited to a few optimizers with rigid restrictions imposed on design parameters, specifications or objective functions. Simulation is often limited to one domain and adding new simulators can be extremely difficult. Research oriented systems may represent state-of-the-art methodology, but typically they lack generality and desired flexibility. We feel that these problems can be effectively addressed by designing general purpose CAD systems featuring a suitable open architecture [1].

In this paper we discuss the problem of flexible circuit optimization, where we can select different optimizers, freely define responses and objectives, functionally interrelate variables, etc., and interact with various external simulators. Our approach is exemplified by Spicepipe, an interface integrating SPICE-PAC [2], a modular version of SPICE [3], into the friendly optimization environment of OSA90/hope [4]. OSA90/hope provides very flexible multipurpose optimization, which is embedded in a language featuring scalar, vector and matrix expression processing and supporting user-definable optimization objectives. It features statistical Monte Carlo analysis, design centering and quadratic modeling, and includes DC, AC, and frequency-domain harmonic-balance simulators. SPICE-PAC contributes time-domain simulation, noise analysis, SPICE device models, etc.

OSA90/hope with the Spicepipe connection to SPICE-PAC allows us to solve design problems in both the frequency and time domains. Also, the optimization capabilities of OSA90/hope can be applied to parameter extraction for device models available in SPICE-PAC.

We have the flexibility to simulate nonlinear circuits by the harmonic-balance (HB) method [5] for steady-state problems or to use time-domain simulation for transient analysis or for problems requiring too many harmonics to be handled by the HB method. For mixed time- and frequency-domain problems the specifications can be split and simulation carried out in both domains simultaneously.

Spicepipe is based on the Datapipe technology [1,4,6], which is an open software architecture allowing us to integrate independent software packages. It is particularly suitable for design optimization.

In this summary we report two applications of Spicepipe. For an NMOS inverter circuit, simulated by SPICE-PAC, the responses are checked against the time-domain specifications in order to estimate Monte Carlo yield. The generation of the outcomes, Monte Carlo estimation, and processing of the responses are performed by OSA90/hope. As a second application, a simple second-order RLC circuit is optimized for maximum yield with specifications in both the frequency and time domains. In the final paper we will also present parameter extraction of SPICE device models and provide comparison between simulations of a nonlinear circuit performed separately in the frequency and the time domains.

Datapipe technology

Developed by OSA, Datapipe technology [1,4,6] is based on the UNIX pipe utility. A pipe is a fast I/O channel between two processes. Datapipe establishes and maintains high-speed data exchange between a parent process and an external process or processes called children. Spicepipe is a child specifically designed to organize and control the exchange of information between OSA90/hope (the parent) and SPICE-PAC.

To define a Datapipe connection we need to specify the input and output for the Datapipe and attach a small server to the child program. The access to the parent program source code is not needed. Furthermore, the internal organization of the Datapipe transfer mechanism is transparent to the user.

We have also used Datapipe to interconnect other specialized simulators. For example, our Empipe child interfaces OSA90/hope with *Em* [7,8,9], a commercial, field-based electromagnetic simulator. Empipe makes it possible, for the first time, to optimize entire circuits with components simulated by an electromagnetic simulator. We also performed yield optimization with Empipe. Our experience shows that, for simple applications, the CPU time overhead due to the Datapipe connections is of the order of a few percent. It becomes even more negligible for complex problems. Several Datapipe children, such as Spicepipe or Empipe can interact through the parent program. There are virtually no limits for such interaction.

The SPICE-PAC system [2]

SPICE-PAC, developed by Zuberek [2], is a modular version of SPICE [3]. It accepts the same circuit description language as SPICE, with a few exceptions, and provides the same circuit analyses. Additionally, it supports a number of extensions and refinements.

The main difference between SPICE and SPICE-PAC lies in the internal organization of the programs. While SPICE is a program with a fixed structure, SPICE-PAC is a library of loosely coupled simulation primitives [10]. Typical examples of simulation primitives include reading circuit description, performing specific circuit analyses or redefining parameters. To utilize SPICE-PAC it is necessary to write a program called SPICE-PAC driver in which the simulation primitives are used as functional blocks.

The modular structure of SPICE-PAC makes the package very attractive, particularly for specialized or optimization-oriented applications, where it usually enjoys significantly improved computational efficiency [11,12]. This modularity allows SPICE-PAC to return the simulation results to OSA90/hope without any file operations. Though not always possible, this approach is best in terms of efficiency. When we deal with "sealed" programs, such as *Em*, communication through files becomes necessary.

Spicepipe

Spicepipe invokes SPICE-PAC in a completely transparent manner. SPICE-PAC's modularity allowed us to link the Datapipe server with SPICE-PAC through a specially created SPICE-PAC driver and a small interfacing driver, altogether forming Spicepipe: a pipe-ready version of SPICE-PAC. The structure of the connection is shown in Fig. 1.

The primary task of the interfacing driver is to maintain communication between OSA90/hope and the child. OSA90/hope sends to SPICE-PAC the values of optimizable variables, requested analysis types, etc. SPICE-PAC returns the simulation results through the interfacing driver which is also responsible for some error checking and necessary data type conversions.

When optimization or multiple simulations are to be performed for the same circuit, Spicepipe skips the initialization operations of SPICE-PAC for the second and all subsequent calls. Such organization significantly saves CPU time. The SPICE-PAC driver allows the optimizer to request one type of analysis at a time, out of the following: DC transfer curve, transient, AC, noise, distortion or Fourier analysis. If two or more analyses are required, separate Datapipe calls are made to the same child process.

The *create_file* child, called through a separate Datapipe channel (Fig. 1) may by employed to create the input (disk) file for SPICE-PAC.

Circuit optimization with Spicepipe

Design optimization involves minimization of an objective function U. Frequently, we consider the generalized ℓ_p function v of errors e_j [13]

$$v(\phi) = \begin{cases} \left(\sum_{j \in J(\phi)} [e_j(\phi)]^p \right)^{1/p} & \text{if } J(\phi) \neq \varnothing \\ -\left(\sum_{j=1}^{m} [-e_j(\phi)]^{-p} \right)^{-1/p} & \text{if } J(\phi) = \varnothing \end{cases} \tag{1}$$

or some variations of (1), where

$$J(\phi) = \{ j \mid e_j(\phi) \geq 0 \} \tag{2}$$

Errors e_j, $j = 1, ..., m$, are functions of circuit parameters ϕ and arise from the differences between the given specifications and the calculated circuit responses. Letting $p = 1$ we obtain the ℓ_1 function exhibiting properties best suited for data-fitting, fault location and robust device modelling. At the other extreme, for $p = \infty$, we have the minimax objective function, which is extensively used in circuit design due to its optimal equal-ripple behaviour.

Unlike the traditional ℓ_2 function, both the ℓ_1 and ℓ_∞ functions are not differentiable. Optimization of these functions requires much more sophisticated algorithms.

Spicepipe, through OSA90/hope, supports a number of variations of the ℓ_1, ℓ_2 and ℓ_∞ objective functions, including one-sided and generalized, associated with specialized and robust algorithms. Also the optimization of the Huber function is supported [14]. This newly developed optimizer is extremely powerful in data-fitting, fault location and parameter extraction.

A circuit design problem can be approached in the frequency and/or the time domain and with the objective function best suited for the problem. For example, nonlinear steady-state design problems can be approached using OSA90/hope's HB simulator and the minimax optimizer while parameter extraction for SPICE-PAC device models could involve SPICE-PAC simulators and OSA90/hope's ℓ_1, ℓ_2 or Huber optimizer.

In the presence of manufacturing tolerances and uncertainties maximization of the production yield becomes of utmost importance. We define yield as $1 - N_{fail}/N_t$, where N_{fail} is the number of circuit outcomes violating the design specifications and N_t is the total number of circuit outcomes. To optimize yield we use the one-sided ℓ_1 objective function [15] defined as

$$U(\phi^0) = \sum_{i \in I} \alpha_i v(\phi^i) \tag{3}$$

where

$$I = \{i \mid v(\phi^i) > 0\} \tag{4}$$

ϕ^0 and ϕ^i are vectors of the nominal and ith circuit parameter values, respectively. $v(\phi^i)$ is given by (1). The α_i are computed from the following formula

$$\alpha_i = \frac{1}{|v(\phi^i)|} \tag{5}$$

at the starting point and then they are kept fixed during optimization. As a result $U(\phi^0)$ equals N_{fail} at the starting point and provides a continuous approximation to N_{fail} during optimization. Consequently, minimization of $U(\phi^0)$ leads to yield improvement. If necessary, yield optimization can be restarted with α_i updated according to (5).

This algorithm has proved to be very efficient and reliable for yield-driven design in the frequency domain [16]. Spicepipe makes it available, for the first time, for the time- and mixed time- and frequency-domain applications. Additionally, yield optimization in either of the domains can be supported by OSA90/hope's quadratic modelling capability. Quadratic models of circuit responses are built from just a few actual circuit simulations. Subsequently, costly circuit simulations are replaced by model evaluation to reduce the computational effort. This technique becomes crucial for CPU intensive problems such as field simulation [7,8].

Time-domain response and Monte Carlo analysis of an NMOS inverter

An NMOS inverter with depletion load [17], shown in Fig. 2, is used to illustrate the utilization of Spicepipe to perform Monte Carlo analysis with time-domain specifications. We used the level 1 option of the SPICE-PAC MOS transistor model [3,17] to model the transistors. We chose the channel length (σ=2%), the channel width (σ=2%), the threshold voltage (σ=12%) and the transconductance (σ=6%) of both load and inverting transistors as the statistical parameters. Numbers in brackets indicate standard deviations of assumed normal distributions of the parameters. We selected the inverter's propagation time t_P < 2.5 ns as the acceptability criterion. The propagation time t_P was computed from SPICE-PAC time-domain response of the inverter by an additional Datapipe child program. The inverter was excited by a trapezoidal signal and its output was connected to another inverter of the same type to simulate a more realistic load. The production yield, estimated using 200 outcomes, was 79.5%. The time-domain response of the nominal circuit as well as the Monte Carlo results are presented in Fig. 3.

Mixed frequency-time-domain optimization of an RLC circuit

We used a simple second-order RLC circuit of Fig. 4. to demonstrate mixed frequency and time-domain optimization capability available through Spicepipe. We wanted this circuit to model an analytically given time-domain response of a different circuit when the input to the modelling system was a step function. We allowed 0.01 absolute difference between the model response and the specification. In addition, we imposed a frequency-domain specification on the insertion loss of the modelling circuit. We wanted the insertion loss to be less than 20 dB in the frequency range from 0.1 to 0.4 Hz. C_1, R_1 and R_2 are optimizable variables; R_{in}, R_{out} and L_1 are fixed. Optimization was carried out in both domains simultaneously.

The Monte Carlo estimate of the production yield at the optimum solution to the nominal problem was 50 %. After 30 yield optimization iterations the yield was increased to 90.5 %. We used 50 outcomes to optimize yield and 200 outcomes to estimate it. Table I lists the values of the optimization variables and assumed standard deviations for statistical variables.

Conclusions

We have presented a new approach to utilizing efficient and powerful optimization techniques in conjunction with various simulators in a flexible and versatile manner. We have exemplified our method with Spicepipe, which interconnects SPICE-PAC to OSA90/hope and allows OSA90/hope's state-of-the-art optimization, featuring user-definable expressions and objective functions, to drive SPICE-PAC's simulators. For the first time powerful and unique techniques, such as the one-sided ℓ_1 yield optimization supported by efficient quadratic modeling, were made available for time-domain or simultaneous time- and frequency-domain applications. We have illustrated the flexibility and benefits of the Spicepipe connection between OSA90/hope and SPICE-PAC on two circuit examples involving simulation, optimization, Monte Carlo analysis and yield-driven design in both the frequency and time domains. To create Spicepipe we have used the high-speed Datapipe technology designed to establish and maintain efficient interconnections between independent software tools.

Acknowledgment

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TABLE I
YIELD OPTIMIZATION OF THE RLC CIRCUIT

Element	Before Optimization	After Optimization	After Yield Optimization	Standard Deviation (%)
R_{in} (Ω)	1.00	1.00	1.00	-
R_1 (Ω)	0.50	0.92	1.00	5
C_1 (F)	0.50	0.43	0.44	5
L_1 (H)	1.00	1.00	1.00	5
R_2 (Ω)	2.00	0.28	0.26	5
R_{out} (Ω)	1.00	1.00	1.00	-

- indicates elements assumed fixed and non-statistical.

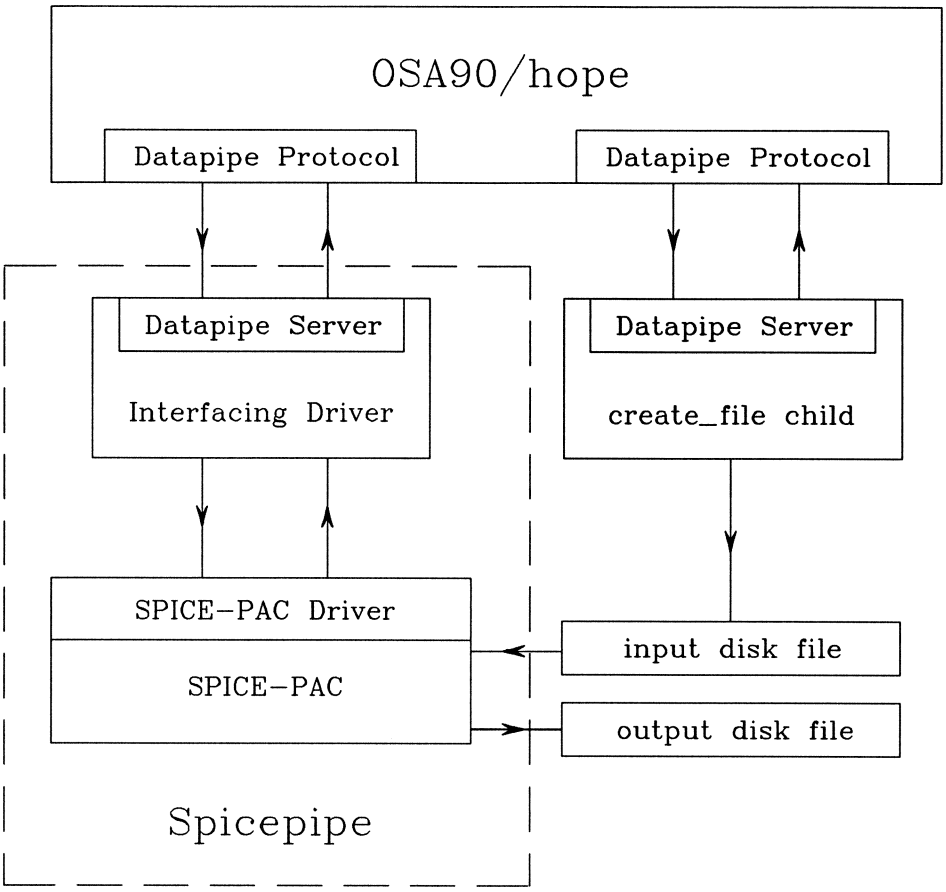


Fig. 1. Integrating SPICE-PAC with OSA90/hope. Spicepipe consists of the interfacing driver, SPICE-PAC driver and the SPICE-PAC library. The *create_file* child creates the SPICE-PAC input disk file.

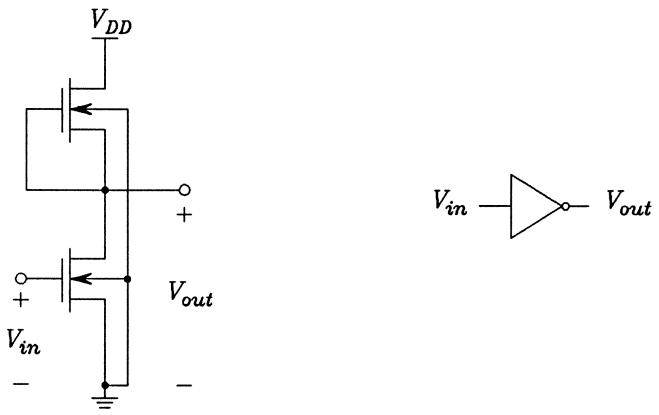
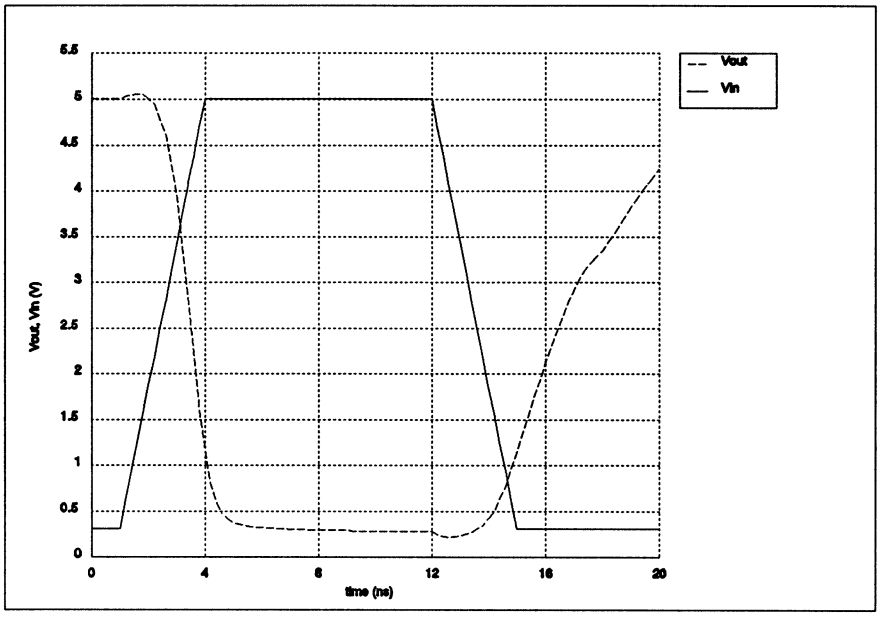
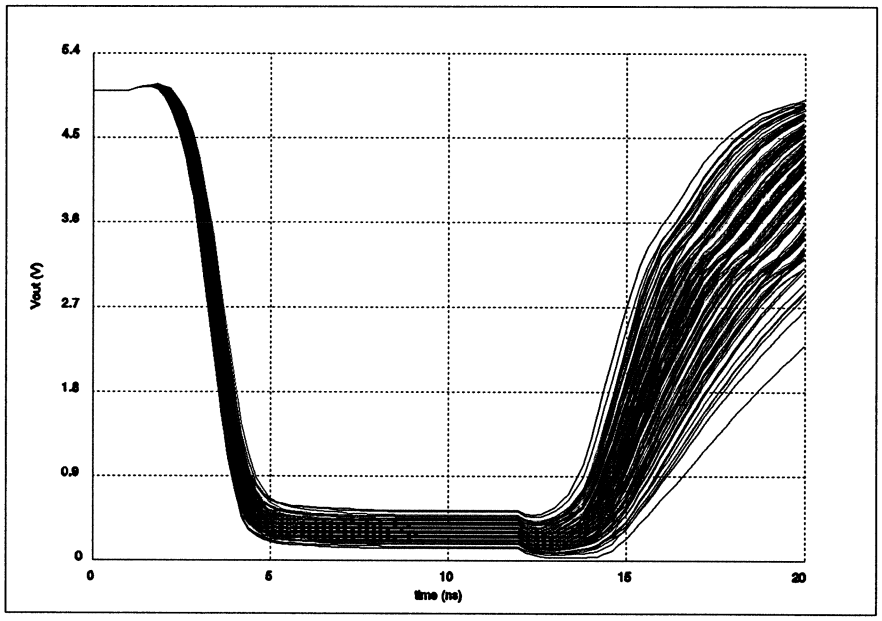


Fig. 2. NMOS inverter, depletion load [17].



(a)



(b)

Fig. 3. Time-domain response of an NMOS inverter, (a) input and output waveforms and (b) Monte Carlo output waveform sweep.

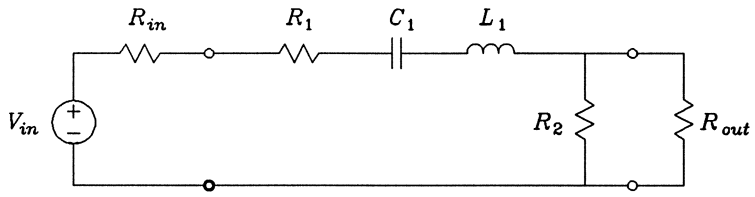


Fig. 4. RLC second-order circuit.

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This paper is concerned with the problem of applying efficient and powerful optimization techniques to drive various simulators in a flexible and versatile manner. In particular, we present Spicepipe, an interface between the optimization environment of OSA90/hope™ and SPICE-PAC, a modular version of SPICE. Powerful features of OSA90/hope's state-of-the-art design optimization are combined with SPICE like simulation. For the first time, techniques such as the one-sided ℓ_1 yield optimization can be applied to time-domain or simultaneous time- and frequency-domain yield optimization. Spicepipe utilizes the efficient, high-speed Datapipe technology of OSA90/hope and exemplifies our approach to and the benefits of flexible circuit design optimization with independent simulators. Our approach is illustrated by examples involving simulation, optimization, parameter extraction, Monte Carlo analysis and yield-driven design.

1. INTRODUCTION

We address the problem of flexible circuit optimization [1], where we can select different optimizers, freely define responses and objectives, functionally interrelate variables, etc., and interact with various external simulators. We exemplify our approach with Spicepipe, an interface integrating SPICE-PAC [2] into OSA90/hope [3]. OSA90/hope provides very flexible multipurpose optimization, which is embedded in a language featuring scalar, vector and matrix expression processing and supporting user-definable optimization objectives. It features statistical Monte Carlo analysis, design centering and sensitivity analysis and includes DC, AC, and frequency-domain harmonic-balance (HB) simulators. SPICE-PAC contributes time-domain simulation, noise analysis, SPICE device models, etc.

OSA90/hope with the Spicepipe connection to SPICE-PAC allows us to solve design problems in both the frequency and time domains. Also, the optimization capabilities of OSA90/hope can be applied to extract parameters of SPICE device models. For mixed time-

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and frequency-domain problems the specifications can be split and simulation carried out in both domains simultaneously.

We report three applications of Spicepipe. For an NMOS inverter circuit we perform Monte Carlo analysis to estimate yield with respect to time-domain specifications. As a second application, we extract parameters of the SPICE-PAC Bipolar Junction Transistor (BJT) model using OSA90/hope optimizers. Finally, we optimize a simple second-order RLC circuit for maximum yield with specifications in both the frequency and time domains.

2. Spicepipe

Spicepipe is based on the Datapipe technology [3, 4], which is an open software architecture allowing us to integrate independent software packages. A Datapipe establishes and maintains high-speed data exchange between a parent process and an external process or processes called children. Spicepipe is a child specifically designed to organize and control the exchange of information between OSA90/hope (the parent) and SPICE-PAC.

The main difference between SPICE and SPICE-PAC lies in the internal organization of the programs. While SPICE is a program with a fixed structure, SPICE-PAC is a library of loosely coupled simulation primitives such as reading circuit description or performing specific circuit analyses. To utilize SPICE-PAC it is necessary to write a program termed SPICE-PAC driver in which the simulation primitives are used as functional blocks. The modular structure of SPICE-PAC makes the package very attractive, particularly for specialized or optimization-oriented applications [5], where it usually enjoys significantly improved computational efficiency.

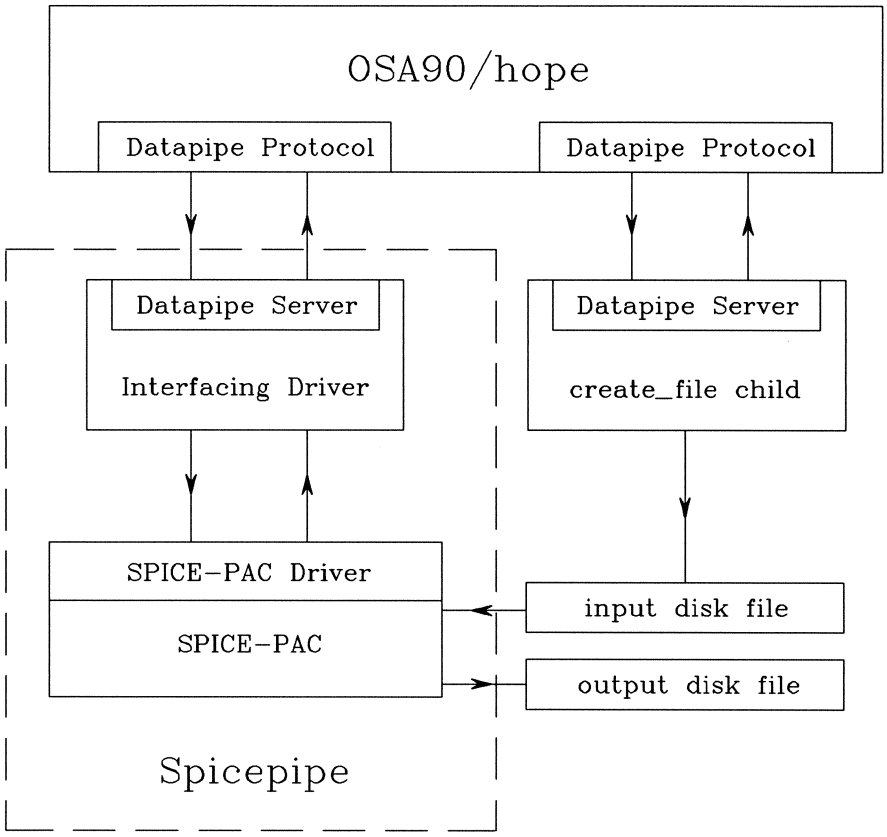
Spicepipe invokes SPICE-PAC in a completely transparent manner. SPICE-PAC's modularity allowed us to link the Datapipe server with SPICE-PAC through a specially created SPICE-PAC driver and a small interfacing driver, altogether forming Spicepipe. The structure of the connection is shown in Fig. 1.

The primary task of the interfacing driver is to maintain communication between OSA90/hope and the child. OSA90/hope sends to SPICE-PAC the values of optimization variables, requested analysis types, etc. SPICE-PAC returns the simulation results. The *create_file* child, called through a separate Datapipe channel (Fig. 1), may by employed to create the input (disk) file for SPICE-PAC.

3. CIRCUIT OPTIMIZATION WITH Spicepipe

Design optimization involves minimization of an objective function U. Frequently, we consider the generalized ℓ_p function v of errors $\boldsymbol{e}$ [6]. Errors $\boldsymbol{e}$ are functions of circuit parameters $\boldsymbol{\phi}$ and arise from the differences between the given specifications and the calculated circuit responses. Letting $p = 1$ we obtain the ℓ_1 function exhibiting properties best suited for data-fitting, fault location and robust device modelling. At the other extreme, for $p = \infty$, we have the minimax objective function, which is extensively used in circuit design due to its optimal equal-ripple behaviour.

Spicepipe, through OSA90/hope, supports a number of variations of the ℓ_1, ℓ_2 and ℓ_∞ objective functions, including one-sided and generalized, associated with specialized and robust algorithms. A circuit design problem can be approached in the frequency and/or the



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time domains and with the objective function best suited to the problem. For example, nonlinear steady-state design problems can be approached using OSA90/hope's HB simulator and the minimax optimizer while parameter extraction for SPICE-PAC device models could involve SPICE-PAC simulators and OSA90/hope's ℓ_1, ℓ_2 or the recently added Huber optimizer.

In the presence of manufacturing tolerances and uncertainties maximization of the production yield becomes of utmost importance. We define yield as $1 - N_{fail}/N_t$, where N_{fail} is the number of circuit outcomes violating the design specifications and N_t is the total number of circuit outcomes. To optimize yield we use the OSA90/hope one-sided ℓ_1 optimizer which has proved to be very efficient and reliable for yield-driven design in the frequency domain. Spicepipe makes it available, for the first time, for time- and mixed time- and frequency-domain applications.

3.1. Monte Carlo analysis of an NMOS inverter

An NMOS inverter with depletion load is used to illustrate the utilization of Spicepipe to perform Monte Carlo analysis with time-domain specifications. We used the level 1 option of the SPICE-PAC MOS transistor model to model the transistors. We chose the channel length (σ = 2%), the channel width (σ = 2%), the threshold voltage (σ = 12%) and the transconductance (σ = 6%) of both load and inverting transistors as the statistical parameters. Numbers in brackets indicate standard deviations of assumed normal

distributions of the parameters. As the acceptability criterion we assumed the inverter's propagation time t_P to be less than 2.5 ns. t_P is the average between t_{PHL} (high-to-low) and t_{PLH} (low-to-high) propagation times. t_{PHL} (t_{PLH}) is defined as the delay of the output waveform w.r.t. the input waveform measured at the 50% signal swing level. t_P was computed from the SPICE-PAC time-domain response of the inverter by an additional Datapipe child program. The inverter was excited by a trapezoidal signal and its output was connected to another inverter of the same type to simulate a more realistic load. Yield, estimated using 200 outcomes, was 79.5%. The Monte Carlo output waveform sweep is presented in Fig. 2.

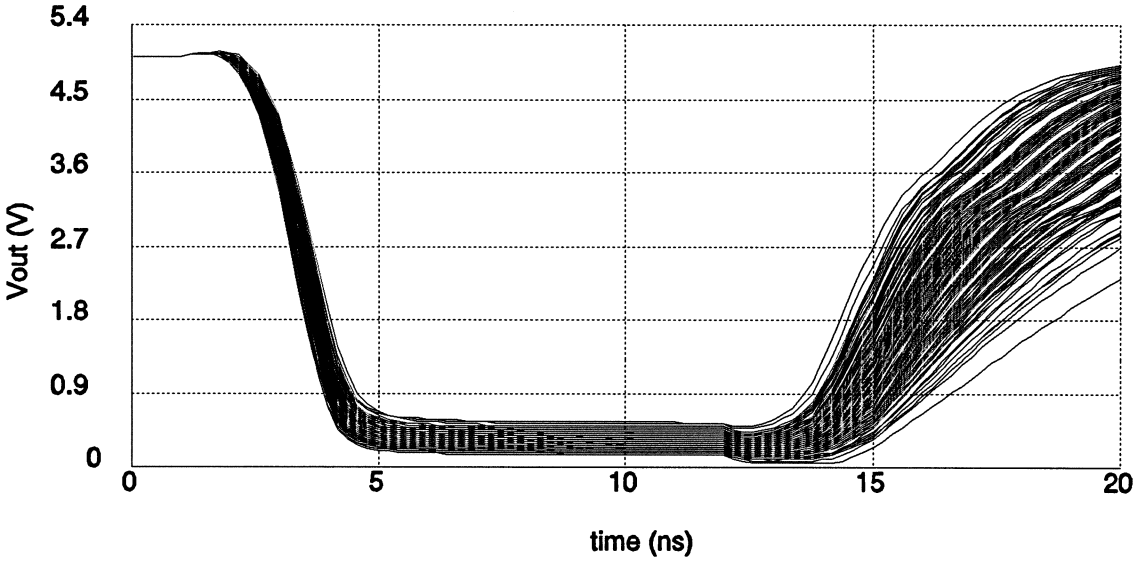

Figure 2. 200 outcome Monte Carlo output waveform sweep of the NMOS inverter.

3.2. SPICE-PAC BJT model parameter extraction

We wanted to match the small-signal AC parameters of the SPICE-PAC BJT model to *S* parameter data. The data corresponded to one biasing point and covered the frequency range from 1 MHz to 1 GHz. We used the OSA90/hope expression processing capability to convert SPICE-PAC responses, that is port voltages and currents, into *S* parameters. In order to uniquely determine all four *S* parameters of the BJT we simulate the transistor twice under two different termination conditions. We used the OSA90/hope ℓ_1 optimizer for optimization. The SPICE-PAC model parameters before and after optimization are listed in Table 1. 15 BJT model parameters were optimized. Fig. 3 shows the *S* parameter match before and after optimization for S_{11} and S_{21}. Very good match of model response to data can be observed for the extracted BJT model. In addition, we separately extracted the DC parameters of the BJT model for a wide range of biasing conditions. The DC characteristic match was also good.

3.3. Mixed frequency-time-domain yield optimization of an RLC circuit

We wanted to design a simple second-order RLC circuit which would closely approximate an analytically given time-domain response of a fourth order circuit. We allowed 0.01 absolute difference between the actual response and the given function at 51 evenly spaced time points in the interval from 0 to 10 s. In addition, we imposed a frequency-domain specification on the insertion loss: less than 20 dB in the frequency range from 0.1 to 0.4 Hz.

Table 1
Small-signal AC parameter extraction of the SPICE-PAC BJT model

Parameters	Before Optimization	After Optimization	Parameters	Before Optimization	After Optimization
IS(A)	10×10^{-15}	25.26×10^{-15}	RC(Ω)	10	1.05
VAF(V)	100	262.21	CJC(F)	5×10^{-12}	4.75×10^{-12}
BF	300	354.9	MJC	0.5	0.16
NE	1.5	1.22	CJE(F)	51×10^{-12}	42.8×10^{-12}
ISE(A)	10×10^{-15}	7.83×10^{-15}	MJE	0.5	0.076
BR	0.01	0.04	TR(S)	10×10^{-9}	35.97×10^{-9}
IKF(A)	0.2*	0.2*	TF(S)	100×10^{-12}	101.93×10^{-12}
XTB	1*	1*	RB(Ω)	100	9.92
NC	2*	2*	RE(Ω)	1	0.021

* Parameters not optimized.
We use SPICE 2G keywords according to Table 2-1 in [7].

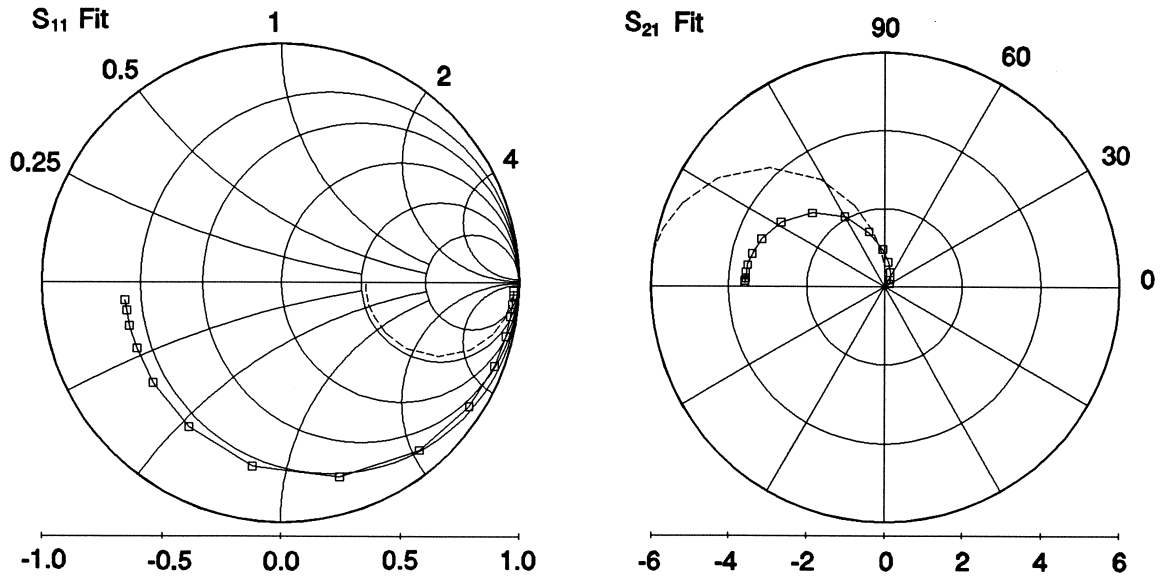

Figure 3. S_{11} and S_{21} parameter match for the SPICE-PAC BJT model. Squares (▫) correspond to the data, dashed (---) and solid (—) lines correspond to the model responses before and after optimization, respectively.

Three parameters were optimized and all four circuit parameters were subject to statistical variation with normal distribution and 5% standard deviation. The source and load resistances were fixed. Optimization was carried out in both domains simultaneously. We

started yield optimization at the point obtained from the nominal design. We used 50 outcomes to optimize yield and 200 outcomes to estimate it. The Monte Carlo yield was increased from 50% before to 91% after optimization.

4. CONCLUSIONS

We have presented a new approach to utilizing efficient and powerful optimization techniques in conjunction with various simulators in a flexible and versatile manner. We have exemplified our method with Spicepipe, which interconnects SPICE-PAC to OSA90/hope and allows OSA90/hope's state-of-the-art optimization, featuring user-definable expressions and objective functions, to drive SPICE-PAC's simulators. For the first time powerful and unique techniques, such as the one-sided ℓ_1 yield optimization, were made available for time-domain or simultaneous time- and frequency-domain applications. We have illustrated the flexibility and benefits of the Spicepipe connection between OSA90/hope and SPICE-PAC with three circuit examples. Using the same Datapipe technology, we have developed similar interfaces to other specialized simulators. For example, our Empipe™ interfaces OSA90/hope with a commercial electromagnetic field simulator ***em***™. Empipe™ allowed us, for the first time, to optimize entire circuits with components simulated by an electromagnetic field simulator.

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