PREDICTABLE YIELD-DRIVEN

CIRCUIT OPTIMIZATION

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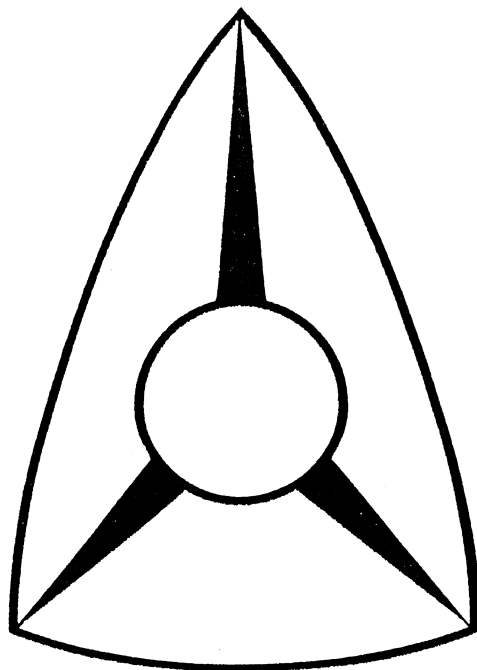
PREDICTABLE YIELD-DRIVEN CIRCUIT OPTIMIZATION

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Abstract

This paper presents a comprehensive approach to predictable yield optimization. We utilize a new physics-based statistical GaAs MESFET model which combines the advantages of the DC Khatibzadeh and Trew model and the small-signal Ladbrooke formulas. The yield of a broadband amplifier is significantly improved after optimization. Predicted yield over a range of specifications is verified by device data. The benefits of simultaneous circuit-device yield optimization assisted by yield sensitivity analysis are demonstrated.

Outline

- we present a new physics-based MESFET model (KTL) combining the respective advantages of the Khatibzadeh-Trew model and the Ladbrooke model

- we show that yield predicted by Monte Carlo simulation using KTL can be consistent with yield predicted directly from device data

- we show how the selection of device parameters for yield optimization can be assisted by yield sensitivity analyses

- we advocate simultaneous circuit-device optimization by illustrating that a significantly higher yield can be achieved by optimizing suitable FET parameters

Statistical Physics Based Models (PBMs)

usefulness of yield optimization depends on

    accuracy of the statistical models

    predictability of yield

statistical modeling in term of *physical parameters* has clear advantages over equivalent circuit models

    nominal values and their statistical spreads may be known

    statistics are modeled at the level where they originate

    statistical models are more reliable

Statistical Modeling of GaAs MESFETs

statistical modeling is a prerequisite for yield-driven and cost-driven circuit design

statistical modeling may be approached at

    equivalent circuit parameter level

    measurement level

    physical and material parameter level

equivalent circuit models can accurately fit the data from which the model parameters are extracted because they have

    fewer constraints

    more variables than physical models

models based on physical parameters can better preserve statistical characteristics of actual devices

for yield-driven and cost-driven circuit design physics-based statistical models are more accurate

The KTL MESFET Model

we combine the DC Khatibzadeh-Trew characterization and the small-signal Ladbrooke formulas to form *a new physics-based small-signal FET model* called *KTL*

the small-signal Ladbrooke model provides more reliable estimates of device statistics than both the equivalent circuit models and the Khatibzadeh-Trew model

the Ladbrooke model does not offer DC simulation

the physics-based Khatibzadeh and Trew model provides good DC simulation results

KTL is applicable to bias-dependent small-signal MESFET statistical modeling

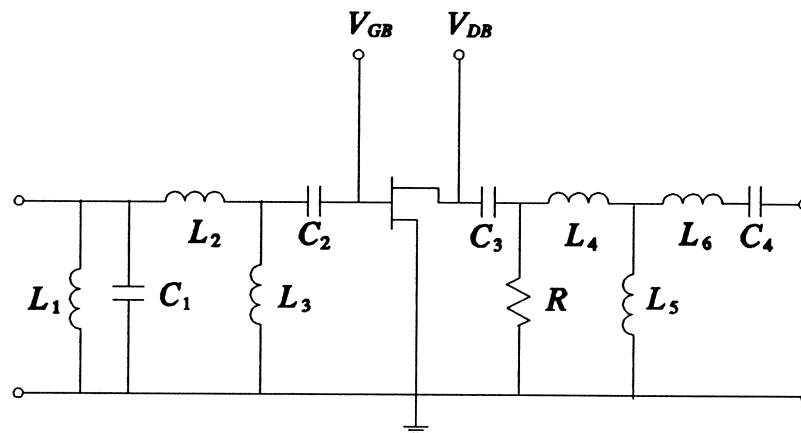KTL has been tested within the statistical environment of HarPE™ and OSA90/hope™

Predictable Yield-Driven Design Using KTL

we use the KTL physics-based small-signal FET model

statistical KTL is extracted from measurement data for
0.5μm GaAs MESFETs (Plessey Research Caswell)

design of a small-signal broadband amplifier is investigated
using OSA90/hope

specification

$$|S_{21}| = 8dB \pm 0.5dB$$

$$|S_{11}| \leq 0.5$$

$$|S_{22}| \leq 0.5$$

design variables are the matching network elements

$$L_1, L_2, L_3, L_4, L_5, L_6, C_1, C_2, C_3, C_4, R$$

Predictable Yield-Driven Design Using KTL (cont'd)

two-stage design procedure:

(1) nominal design

(2) yield optimization (using 100 outcomes)

yield estimated by Monte Carlo analysis with 200 outcomes was 17.5% before and 67% after yield optimization

Design Variable	Before Yield Optimization	After Yield Optimization
$C_1(pF)$	0.6161	0.4372
$C_2(pF)$	5.2556	6.1365
$C_3(pF)$	0.2606	0.2757
$C_4(pF)$	0.1385	0.1570
$R(\Omega)$	589.00	708.08
$L_1(nH)$	0.5947	0.9110
$L_2(nH)$	0.9916	0.9430
$L_3(nH)$	1.9203	1.6395
$L_4(nH)$	1.5754	1.7516
$L_5(nH)$	2.0039	2.3933
$L_6(nH)$	1.0085	0.7537

Yield Verification for KTL

practical usefulness of yield optimization depends on whether yield predicted by statistical models is consistent with yield predicted from actual device measurements

we substitute device data for the KTL model and compare Monte Carlo yields

the Materka and Kacprzak model is used to interpolate individual device data at the same bias point $(V_{GB} = -0.7\text{V}$ and $V_{DB} = 5\text{V})$

Yield	Before Yield Optimization	After Yield Optimization
Predicted (%)	17.5	67.0
Verified (%)	15.7	57.9

Yield Verification for KTL (cont'd)

the yield verification procedure is applied again to the same circuit, but with varying design specifications

it shows that the good agreement is not a singular exception

	Before Yield Optimization		After Yield Optimization	
	Predicted Yield (%)	Verified Yield (%)	Predicted Yield (%)	Verified Yield (%)
Spec. 1	17.5	15.7	67	57.9
Spec. 2	21	20	83	75.7
Spec. 3	44	37.1	98	93.6

Spec. 1: $7.5dB < |S_{21}| < 8.5dB$, $|S_{11}| < 0.5$, $|S_{22}| < 0.5$.
Spec. 2: $6.5dB < |S_{21}| < 7.5dB$, $|S_{11}| < 0.5$, $|S_{22}| < 0.5$.
Spec. 3: $6.0dB < |S_{21}| < 8.0dB$, $|S_{11}| < 0.5$, $|S_{22}| < 0.5$.

200 Monte Carlo outcomes are used for predicted yield, 140 for verified yield.

Monte Carlo simulation using the KTL model
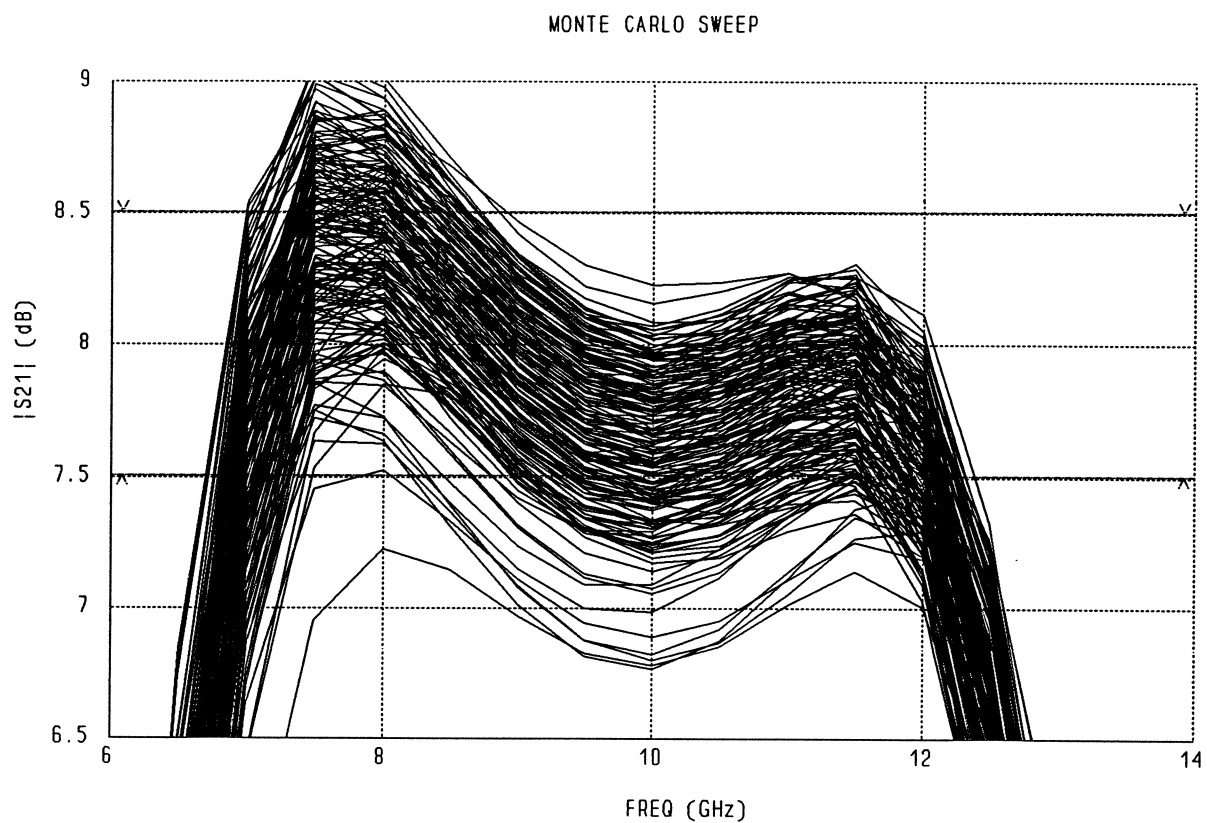
MONTE CARLO SWEEP

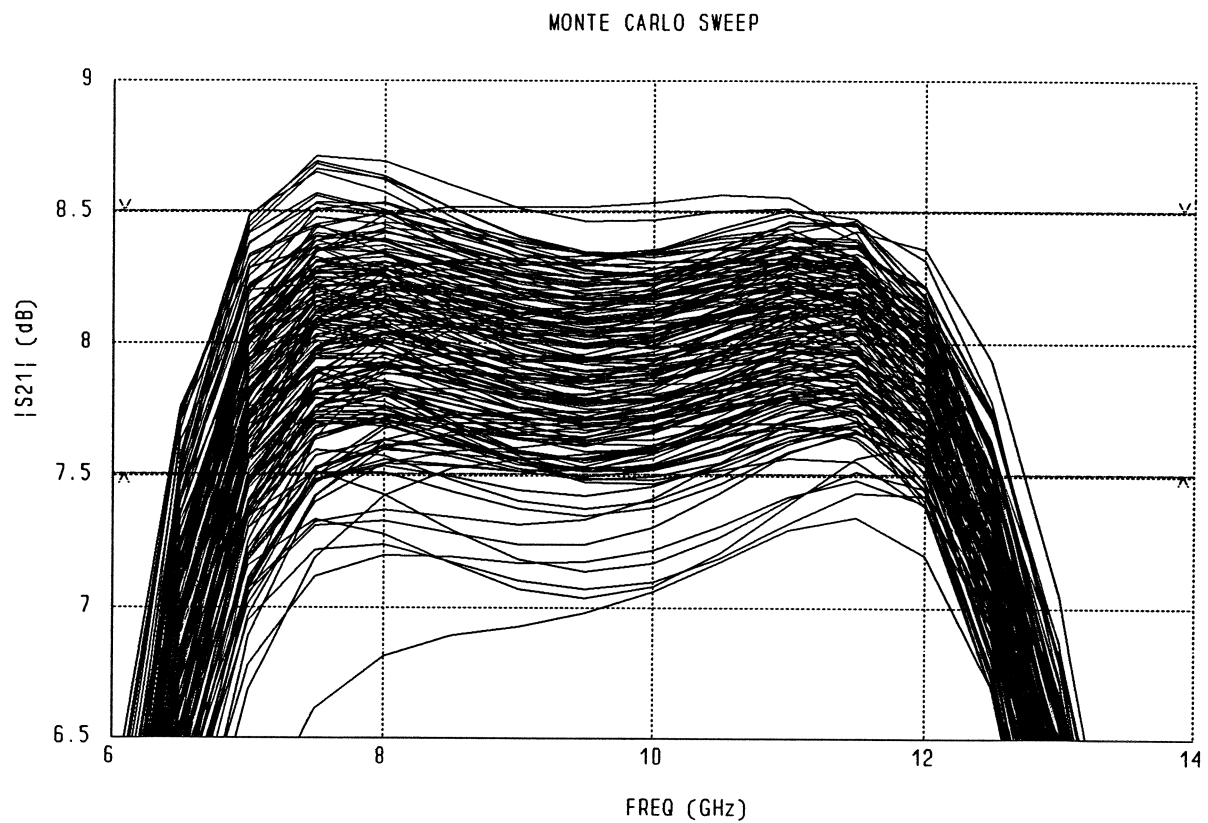# Gain vs. Frequency Before Optimization

Monte Carlo simulation using device data

MONTE CARLO SWEEP

Gain vs. Frequency Before Optimization

Monte Carlo simulation using the KTL model

MONTE CARLO SWEEP

Gain vs. Frequency After Optimization

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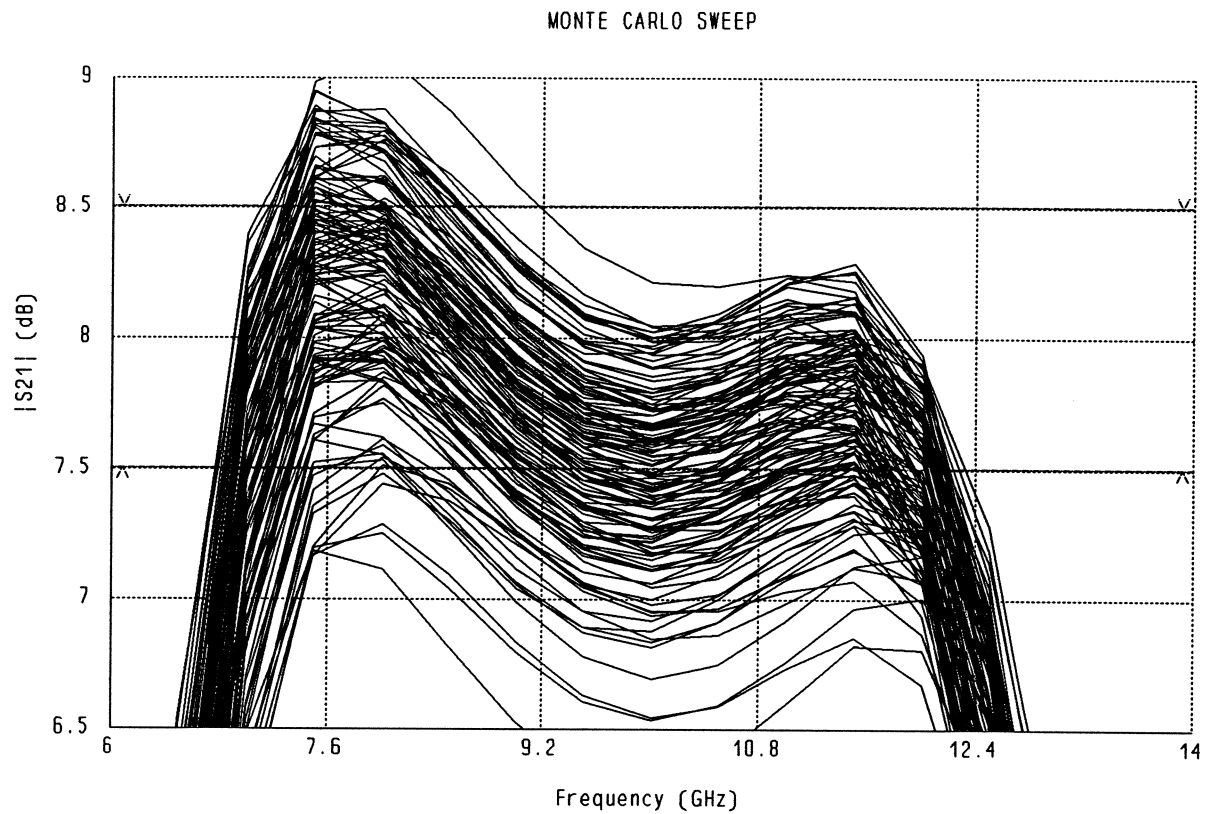
Monte Carlo simulation using device data

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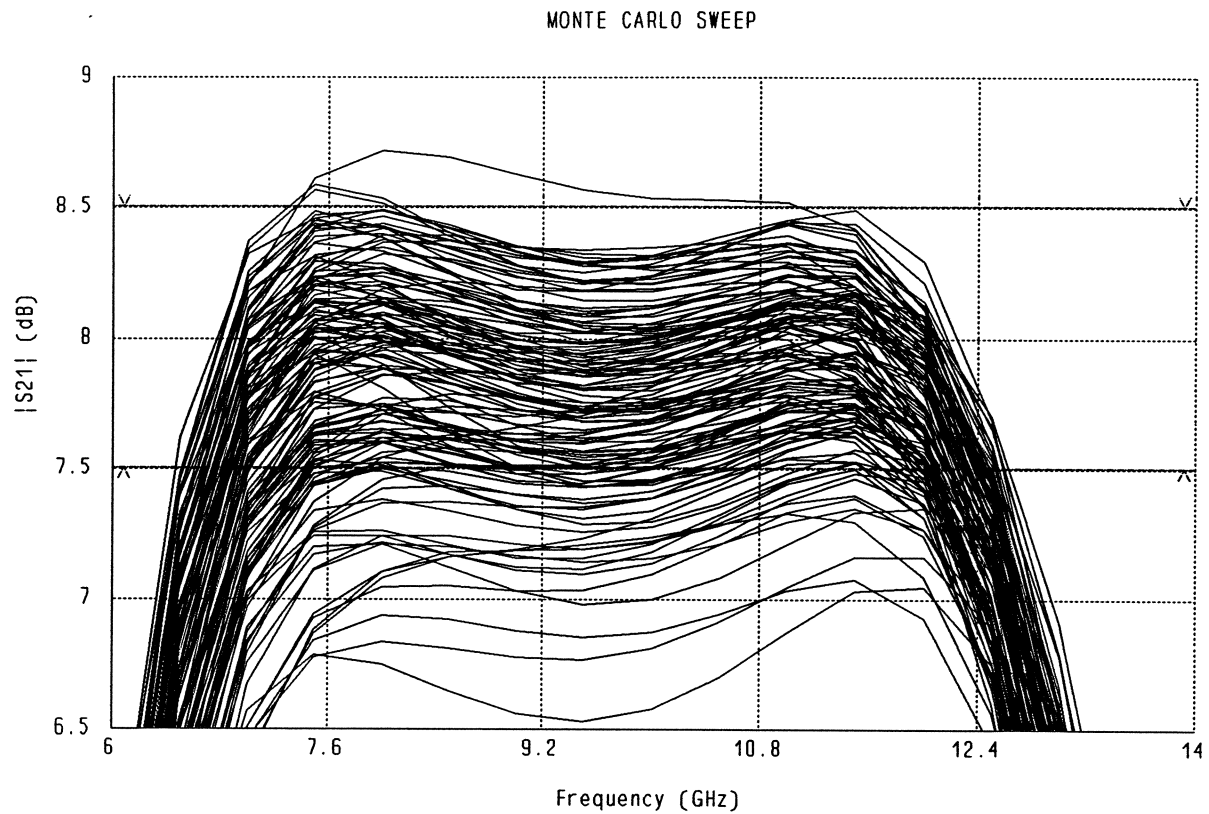
Gain vs. Frequency After Optimization

Yield Sensitivity Analysis

yield is a function of device parameters, circuit elements, parameter statistics and design specifications

selecting a proper set of variables for yield optimization can be delicate

we use OSA90/hope to calculate the sensitivities of yield w.r.t. circuit and design parameters

this reveals the influence of different parameters on yield and assists us in selecting variables for yield optimization

we performed yield sensitivity analysis w.r.t. the FET gate length which was not included in the first design
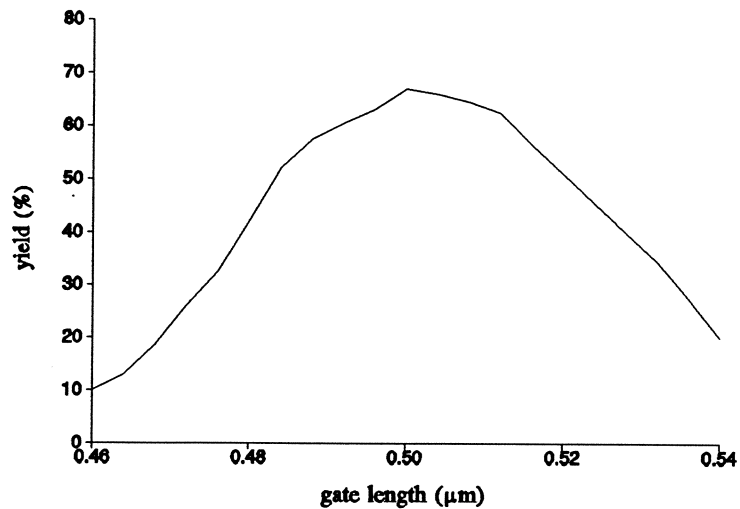
we also performed yield sensitivity analysis w.r.t. the lower design specification to illustrate how the specification can be traded off for yield

Yield Sensitivity
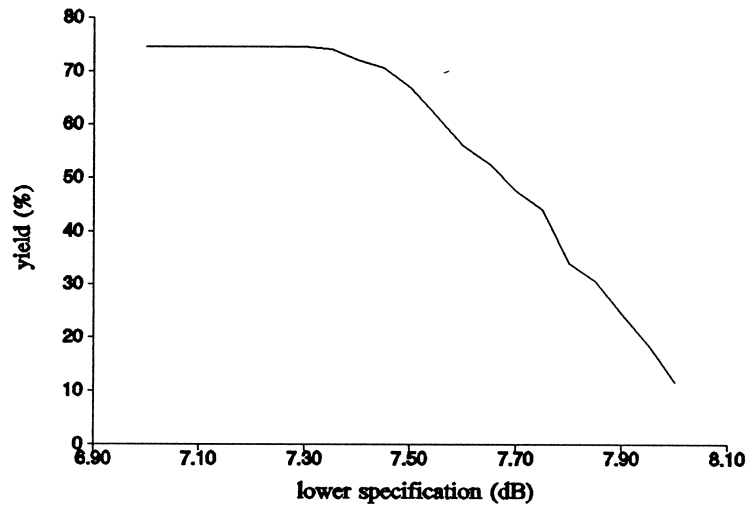
Yield versus the lower specification on the gain

Yield versus the FET gate length

Simultaneous Device-Circuit Design

representing devices by statistical PBMs has a clear
advantage over direct use of the measured S parameters

>   the model can interpolate device behaviour at
>   frequency and bias points not contained in the data

>   an unlimited number of outcomes can be generated for
>   Monte Carlo analysis

>   PBMs permit optimization of the parameters of active
>   devices, not possible if the devices are represented by
> S parameters

Simultaneous Device-Circuit Design (cont'd)

we consider the same small-signal broadband amplifier with tightened upper specification on $|S_{11}|$ from 0.5 to 0.4 in the passband, while the other specifications remain the same

two separate cases of optimization were constructed

> only the matching circuits are optimized

> the gate length and channel thickness of the MESFET are included as design variables in addition to the matching circuits

Variables	Yield (%) before optimization	Yield (%) after optimization
Matching network only	7.5%	27.5%
Matching network and device parameters	12.5%	64.5%

Conclusions

a comprehensive approach to yield-driven circuit optimization has been presented

- statistical modeling

- nominal design optimization

- yield optimization

- yield verification

- device optimization

we have demonstrated

- the statistical KTL model: a novel, accurate physics-oriented model for GaAs MESFETs, particularly suitable for statistical device characterization

- for the first time that yield predicted by Monte Carlo simulation using an analytical PBM can be consistent with yield predicted directly from device measurement data

- simultaneous device and circuit optimization assisted by yield sensitivity analyses has great potential in the physics-based technique for MICs and MMICs