OSA

HARMONIC BALANCE SIMULATION AND OPTIMIZATION OF NONLINEAR CIRCUITS

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Optimization Systems Associates Inc.

Dundas, Ontario, Canada

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Introduction

advances in IC technology demand the next generation CAE software

efficient algorithms for large-scale optimization of nonlinear circuits are crucial

cost reduction is a primary goal

yield-driven optimization methodology is essential

statistical representation of physical, process and geometrical parameters must be integral to CAE

Increasing Sophistication of Design Methodology

deterministic

- performance-driven design
- fixed tolerance worst-case design
- variable tolerance worst-case design

statistical

- fixed tolerance yield-driven design
- correlated tolerances
- variable tolerance cost-driven design

Nonlinear Circuit Simulation

most analog microwave circuits operate under steady-state conditions

harmonic balance (HB) has become the major simulation tool for nonlinear microwave circuits

popular harmonic balance software:

- typical algorithms inhibit fast optimization
- yield-driven design may be prohibitively CPU intensive
- inaccurate, slow sensitivity/gradient evaluation

OSA's research and development successfully addresses these issues:

HarPE	device modeling (both deterministic and statistical)
OSA90/hope	general purpose linear/nonlinear circuit design system

Notation and Definitions

the overall nonlinear circuit is divided into linear and nonlinear parts

$\mathbf{v}(t)$ and $\mathbf{i}(t)$	voltage and current waveforms at the linear-nonlinear connection ports
$\mathbf{V}(k)$ or $\mathbf{I}(k)$	kth harmonic of voltage and current spectrum

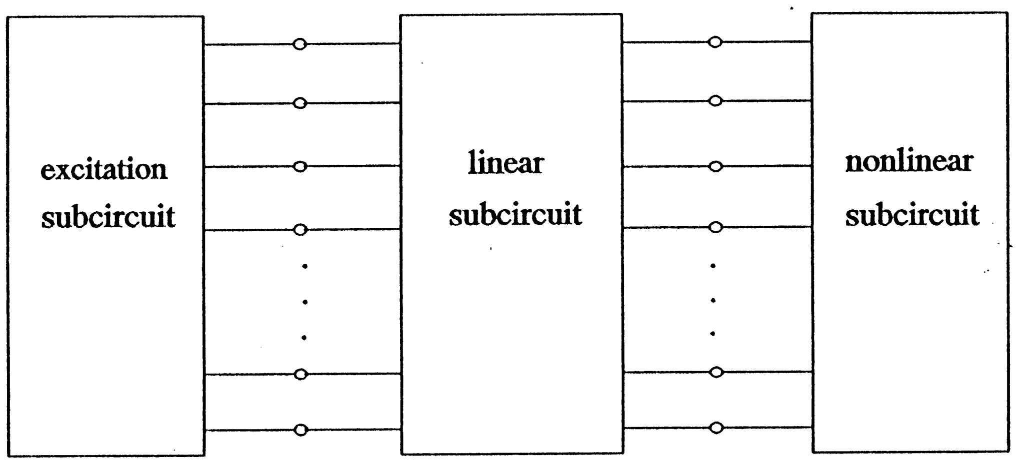
bar denotes the split real and imaginary parts of complex quantities

$\bar{\mathbf{V}}$ or $\bar{\mathbf{I}}$	real vectors containing the real and the imaginary parts of $\mathbf{V}(k)$ or $\mathbf{I}(k)$ for all harmonics k, $k = 0, 1, \dots, H$

hat distinguishes quantities of the adjoint system

$\hat{\bar{\mathbf{V}}}$	real vector containing the real and the imaginary parts of adjoint voltages for all harmonics k, $k = 0, 1, \dots, H$

Circuit Partitioning for the HB Technique



frequency-domain simulation ⟷ time-domain simulation

FFT or DFT used for frequency-time-frequency transformations

Basics of the HB Technique

the harmonic balance equation is formulated in the frequency domain as

$$\mathbf{F}(\mathbf{V}) = \mathbf{I}_{NL}(\mathbf{V}) + \mathbf{I}_{L}(\mathbf{V}) = \mathbf{0}$$

where $\mathbf{I}_{NL}$ and $\mathbf{I}_{L}$ are currents (spectra) entering the nonlinear and linear subcircuit, respectively

or, in the split real-imaginary form as

$$\bar{\mathbf{F}}(\bar{\mathbf{V}}) = \mathbf{0}$$

a simple Newton's update for the equation is

$$\bar{\mathbf{V}}_{new} = \bar{\mathbf{V}}_{old} - \bar{\mathbf{J}}^{-1}\,\bar{\mathbf{F}}(\bar{\mathbf{V}}_{old})$$

where $\bar{\mathbf{J}}$ is the Jacobian matrix

Starting Point for the HB Iterations

conventional DC/small-signal analysis:

solve for DC operating point

linearize the circuit at DC operating point

solve small-signal AC circuit

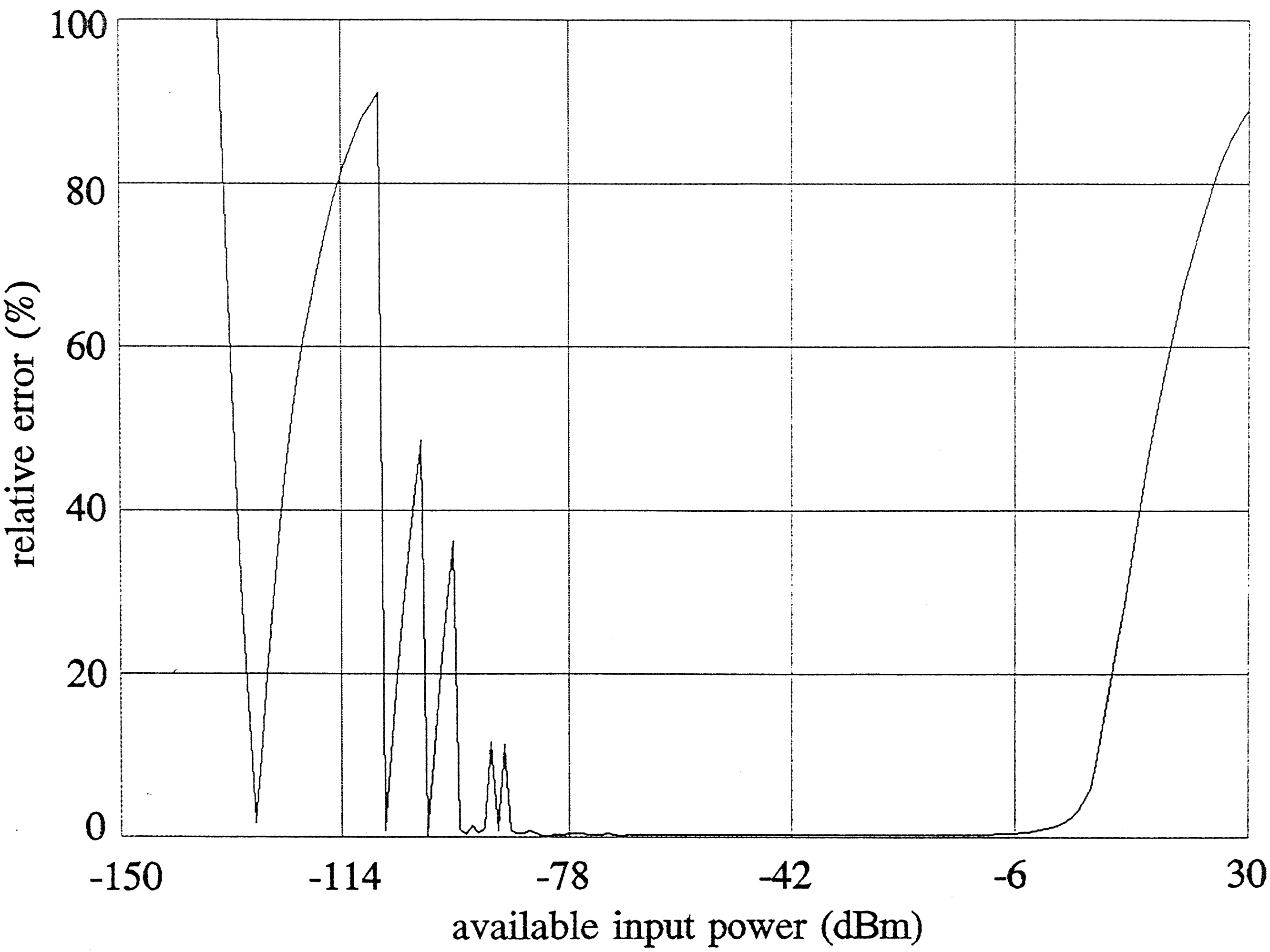
power stepping

several HB solutions are generated with the source power increased gradually up to the specified value

each intermediate solution is applied as a starting point in solving the HB equation for the next power level

Rizzoli et al. (1988) proposed a quasi-Newton iteration to obtain the starting point

HBSS - Harmonic Balance under Small-Signal Excitations



relative error between conventional DC/small-signal simulation and HB simulation for different power levels

voltage gain of a simple single-FET circuit

Harmonic Balance Sensitivities

extensive number crunching required by HB simulators inhibits fast optimization of nonlinear circuits if sensitivity and Jacobian calculations are performed expensively and inaccurately by perturbations (PAST)

Kundert and Sangiovanni-Vincentelli (1986) and *Rizzoli et al.* (1986) suggested exact Jacobian approach

Rizzoli et al. combined both optimization and solving nonlinear equations - disadvantages:

> incompatibility with established yield optimization formulations
>
> the HB equation may not be accurately satisfied at the solution

Bandler, Zhang and Biernacki (1988) developed the exact adjoint sensitivity technique (EAST) for the HB method

Bandler, Zhang and Biernacki (1989) developed the feasible adjoint sensitivity technique (FAST) for the HB method

EAST

if the output (response) voltage is selected by

$$\bar{\mathbf{V}}_{out} = \mathbf{c}^T \bar{\mathbf{V}}$$

then the adjoint system is defined as

$$\bar{\mathbf{J}}^T \hat{\bar{\mathbf{V}}} = \bar{\mathbf{c}}$$

where $\bar{\mathbf{J}}$ is the Jacobian matrix at the solution

exact sensitivity expressions in terms of $\bar{\mathbf{V}}$ and $\hat{\bar{\mathbf{V}}}$ have been derived for different circuit components

50 times faster than perturbation in our tests

expensive to implement in general purpose programs

FAST

combines efficiency of exact adjoint sensitivities with simplicity of conventional perturbations

advantages of FAST over PAST are its unmatched speed and accuracy

advantage of FAST over EAST is its implementational simplicity

particularly suitable for implementation in general purpose CAE software

carries over to practically implementable Jacobians for fast harmonic balance simulation

FAST is directly compatible with established formulations of yield optimization and provides high-speed gradient evaluation essential for yield optimization of nonlinear circuits by general purpose software

Gradient Analysis Using FAST

the approximate sensitivity of output voltage $\bar{V}_{out}$ w.r.t. variable ϕ can be computed as

$$\partial \bar{V}_{out} / \partial \phi \quad = \quad - \hat{\bar{V}}^{T} \, \bar{F} \, (\phi + \Delta \phi , \bar{V}_{solution}) \, / \, \Delta \phi$$

where

$\bar{V}_{solution}$ solution of the harmonic balance equations

$\hat{\bar{V}}$ adjoint voltages obtained from solving the linear equations:

$$\bar{J}^{T} \hat{\bar{V}} = \bar{c}$$

the adjoint linear equations are easy to solve since the LU factors of the Jacobian matrix are available from solving the harmonic balance equations

FAST Analysis of a FET Mixer

the mixer circuit

LO frequency	f_{LO} = 11 GHz
RF frequency	f_{RF} = 12 GHz
IF frequency	f_{IF} = 1 GHz
DC bias voltages	V_{GS} = -0.9, V_{DS} = 3.0
LO power	P_{LO} = 8 dBm
RF power	P_{RF} = -15 dBm
conversion gain	6.9 dB

computed sensitivities of the conversion gain w.r.t. all 26 variables

- all parameters in the linear part
- all parameters in the nonlinear part
- DC bias, LO power, RF power
- IF, LO and RF terminations

Results of FAST Analysis of a FET Mixer

excellent agreement between sensitivities computed using FAST, PAST and EAST

CPU times on VAX 8600

circuit simulation	22 seconds
FAST sensitivity analysis	10.7 seconds
EAST sensitivity analysis	3.7 seconds
PAST sensitivity analysis	240 seconds

NUMERICAL VERIFICATION OF FAST FOR THE MIXER EXAMPLE

Variable	Sensitivity from FAST	Sensitivity from EAST	Sensitivity from PAST	Difference between FAST and EAST (%)	Difference between FAST and PAST (%)
linear subnetwork					
C_{ds}	-24.28082	-24.28081	-24.03669	0.00	1.01
C_{gd}	-32.16238	-32.16237	-32.33670	0.00	-0.54
C_{de}	-8.8×10^{-13}	1.7×10^{-13}	0	120.21	100.00
R_g	10.00754	10.00756	9.89609	-0.00	1.11
R_d	11.71325	11.71327	11.71338	-0.00	-0.00
R_s	-4.98829	-4.98827	-4.98861	0.00	-0.01
R_{de}	-0.07171	-0.07171	-0.07115	0.00	0.79
L_g	-0.30238	-0.30238	-0.30054	0.00	0.61
L_d	-0.87824	-0.87824	-0.87247	0.00	0.66
L_s	-0.33527	-0.33527	-0.33191	0.00	1.00
nonlinear subnetwork					
C_{gs0}	-5.43110	-5.43110	-5.38265	0.00	0.89
τ	1.52983	1.52984	1.56057	-0.00	-2.01
V_ϕ	-20.84224	-20.84223	-20.84308	-0.00	-0.00
V_{p0}	-14.62206	-14.62206	-14.62469	0.00	-0.02
V_{dss}	0.30209	0.30209	0.30210	0.00	-0.00
I_{dsp}	9.39335	9.39335	9.39338	-0.00	-0.00
bias and driving sources					
V_{GS}	-4.94402	-4.94402	-4.94271	-0.00	0.03
V_{DS}	-0.67424	-0.67424	-0.67429	0.00	-0.01
P_{LO}	2.02886	2.02885	2.02882	0.00	0.00
P_{RF}	-0.09073	-0.09072	-0.09077	0.01	-0.05
terminations					
$R_g(f_{LO})$	8.83598	8.83596	8.76244	0.00	0.83
$X_g(f_{LO})$	2.20500	2.20496	2.16567	0.00	1.78
$R_g(f_{RF})$	0.71282	0.71281	0.70568	0.00	1.00
$X_g(f_{RF})$	0.46410	0.46409	0.45702	0.00	1.53
$R_d(f_{IF})$	0.65950	0.65950	0.65272	-0.00	1.03
$X_d(f_{IF})$	0.09024	0.09024	0.09207	-0.00	-2.02

Simple and Efficient Computation of Jacobian

exact Jacobian for HB simulation is available but very expensive to implement

Kundert and Sangiovanni-Vincentelli (1986)
Rizzoli et. al. (1986)

the perturbation (or incremental) approach is typically used in practice but is slow

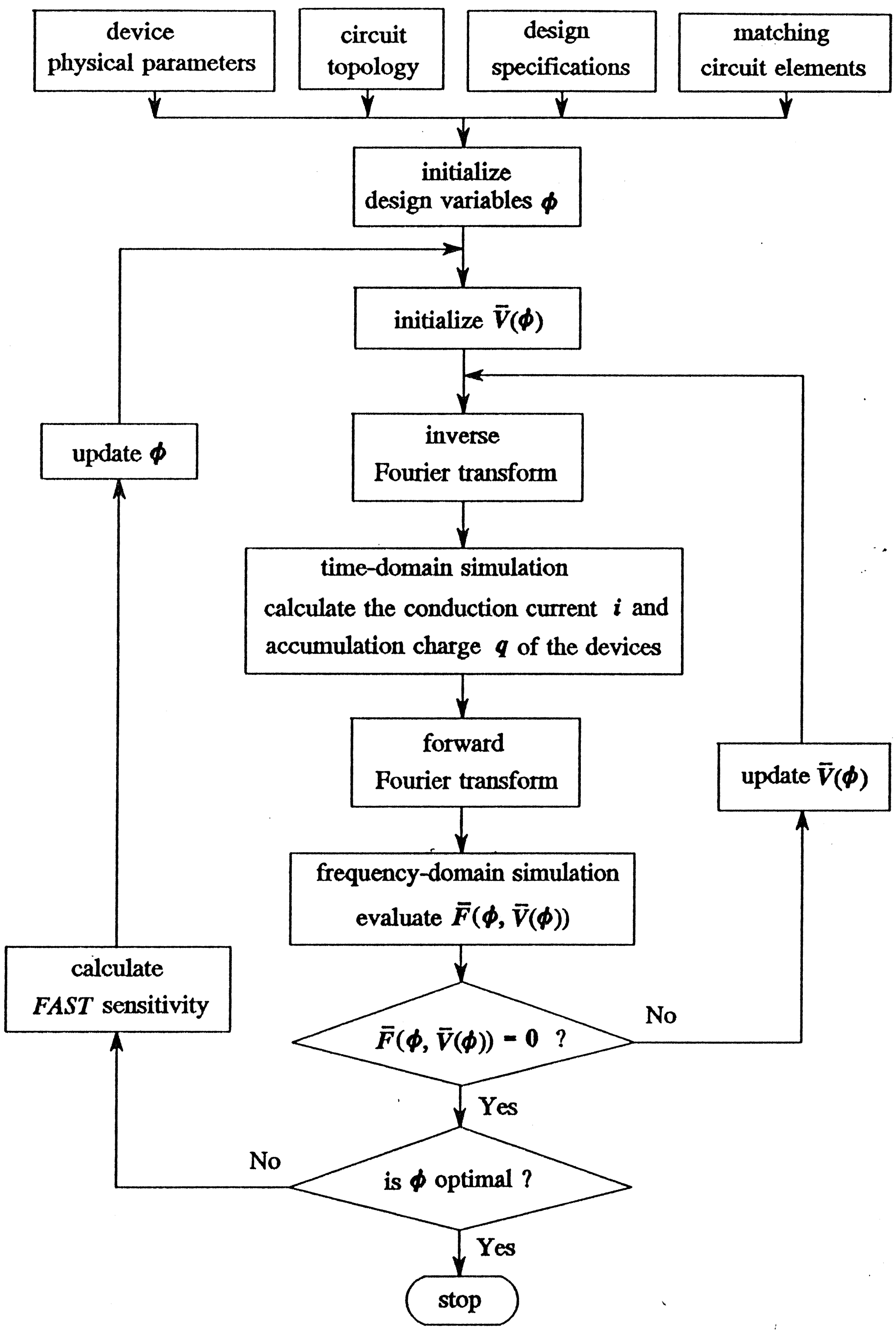
FAST concept extends to Jacobian calculation by

computing time-domain derivatives at the device level using perturbations

converting these derivatives to the frequency domain by a Fourier transform

assembling the resulting Fourier coefficients into the Jacobian matrix

Optimization of Nonlinear Circuits



Nonlinear Modeling using Harmonics

simulation of linear/nonlinear circuits requires accurate linear/nonlinear device models

device is excited under practical (large-signal) working conditions

spectrum measurements are taken at different bias, input power and fundamental frequency combinations

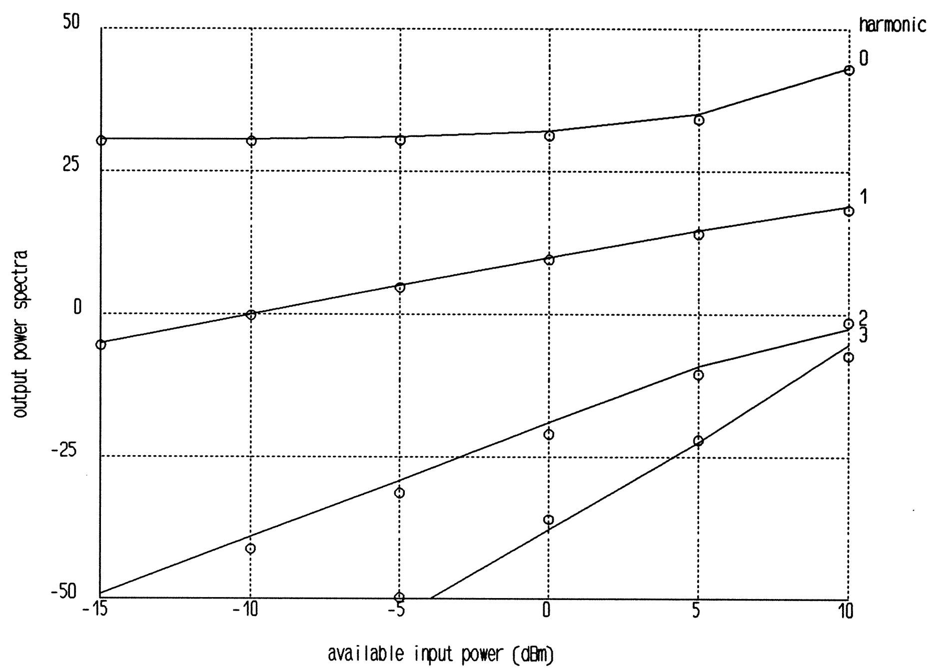
parameters are extracted by optimizing the model response to match the spectrum measurements

harmonic balance simulation technique for nonlinear circuit simulation in the frequency domain is used

nonlinear adjoint sensitivity analysis for gradient computation of nonlinear circuit responses (FAST)

ℓ_1 optimization

FET Modeling from Power Spectrum Measurements



power spectrum measurements at two bias points, three fundamental frequencies, and six input power levels

20 variables, 113 error functions and 30 simultaneous nonlinear circuit simulations

Unified Small- and Large-Signal Design

combining DC, small-signal and large-signal simulations and specifications into one unified optimization problem

requires the same nonlinear device models to be utilized for all types of simulation in order to achieve analytically consistent results

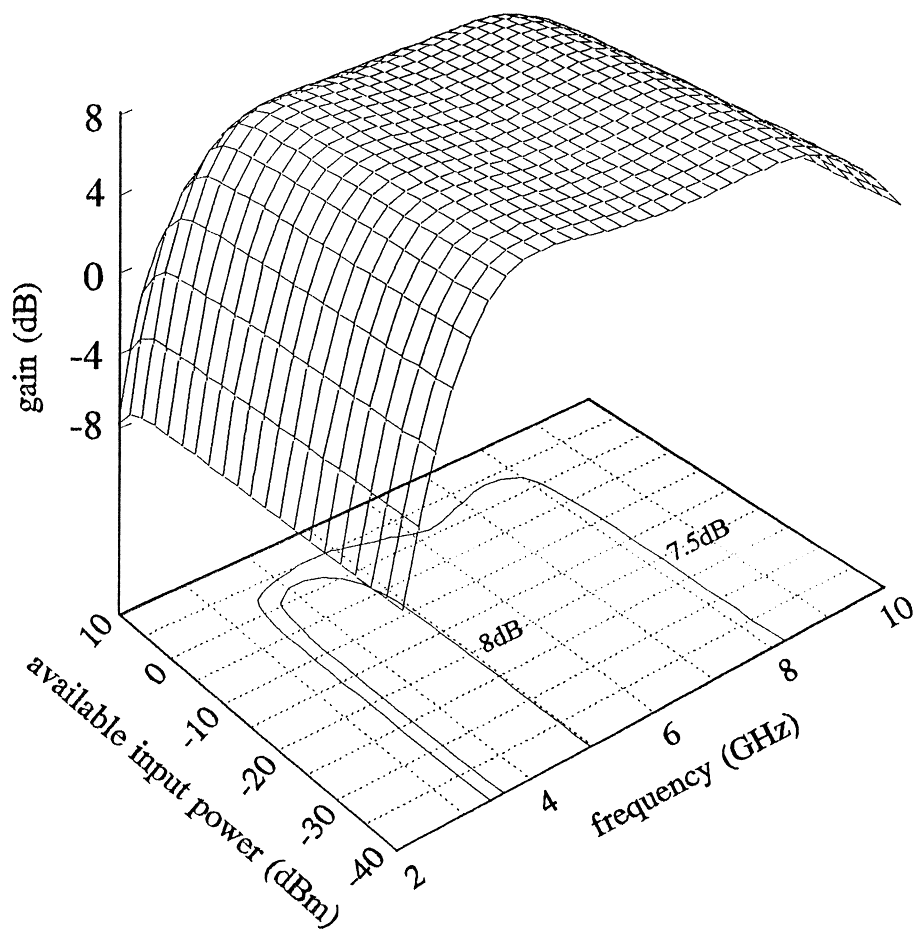
DC models derived from global models by ignoring inductive and capacitive effects

small-signal models derived from global models by linearization at the DC operating point

global models used for harmonic balance simulation

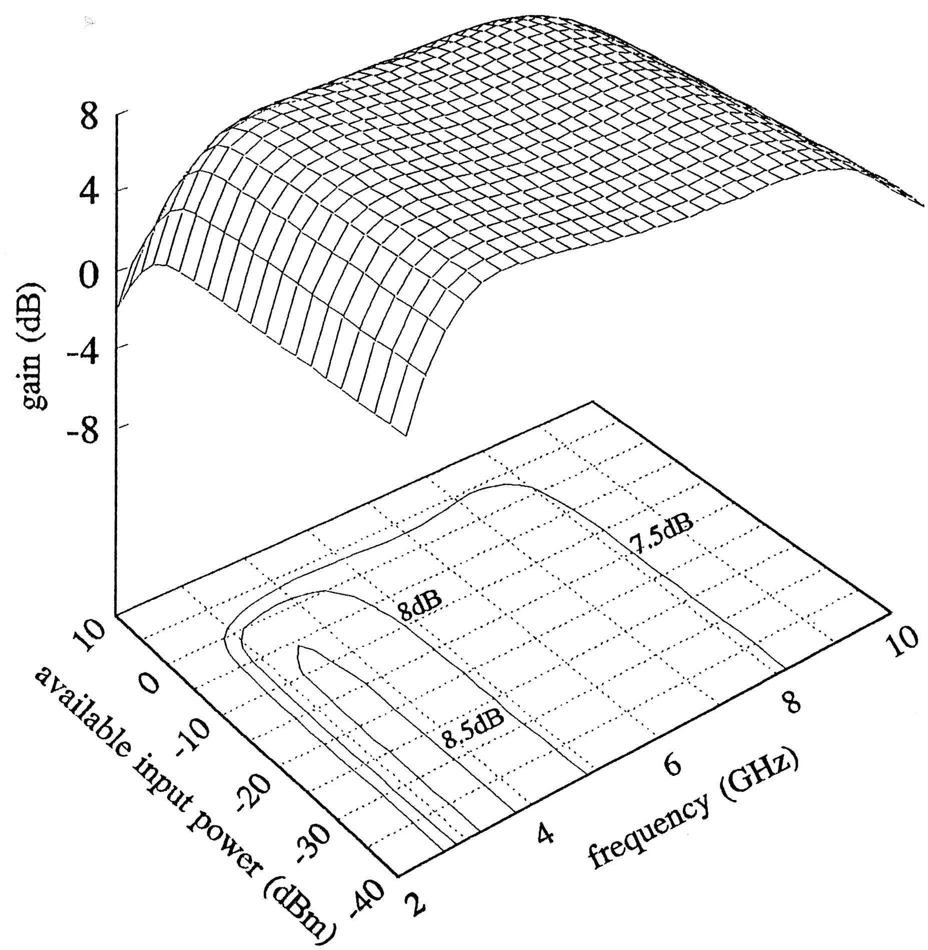
unified design extends traditional design methodology

Conventional Small-Signal Design



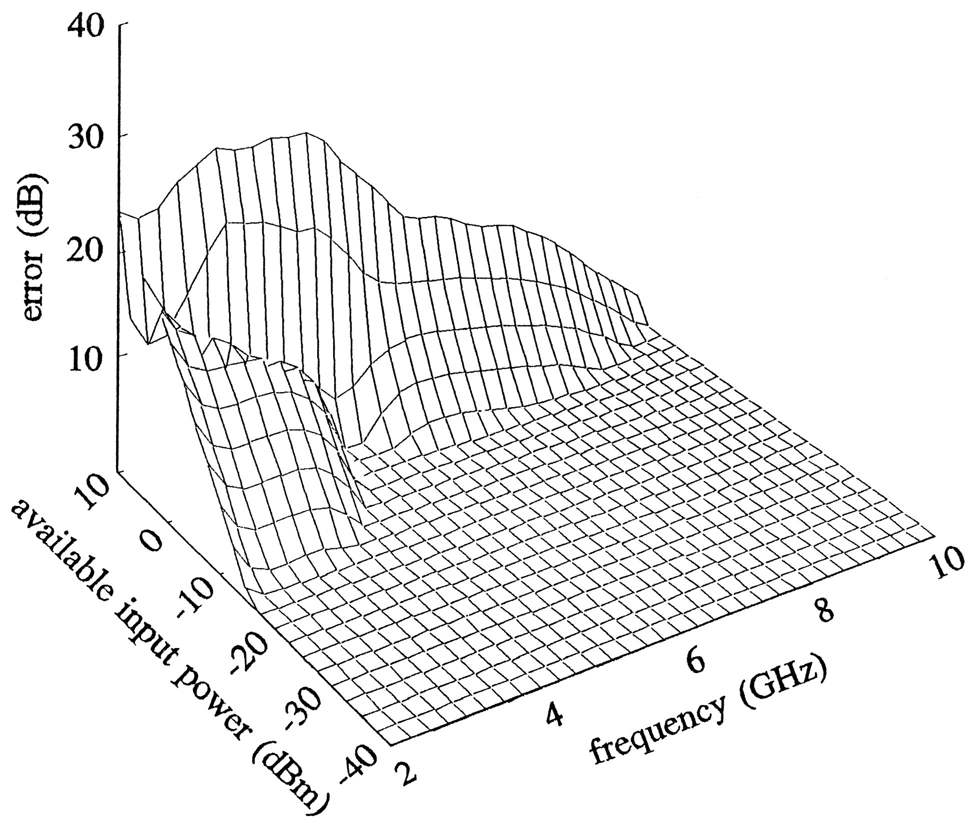
gain surface of a small-signal broad-band amplifier designed using small-signal simulations and specifications

Simultaneous Small- and Large-Signal Design



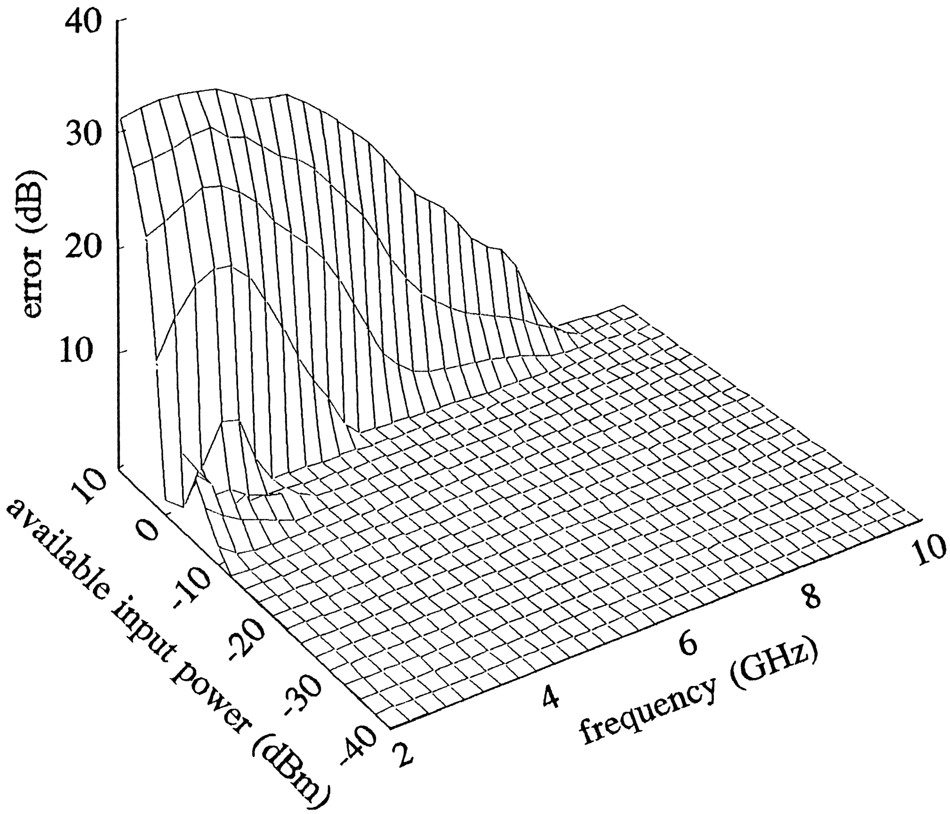
gain surface of a small-signal broad-band amplifier designed using harmonic balance simulations and both small- and large-signal specifications

Conventional Small-Signal Design



error surface for the second harmonic output power of a small-signal broad-band amplifier designed using small-signal simulations and specifications

Simultaneous Small- and Large-Signal Design



error surface for the second harmonic output power of a small-signal broad-band amplifier designed using harmonic balance simulations and both small- and large-signal specifications

Yield Optimization

high yield is essential for large volume production of ICs

useful CAE must account for manufacturing tolerances, model uncertainties, variations of process parameters, environmental uncertainties, etc.

yield optimization is computationally intensive

optimization is iterative

each iteration requires simulation of many statistically related circuits

simulation of each nonlinear circuit is iterative

yield-driven design demands powerful, robust, fast optimizers and effective statistical representation of devices and subcircuits

Manufacturing Yield

Manufacturing yield is simply the ratio

$$Y = N_{pass}/N_t$$

where

N_{pass} is the number of circuit outcomes satisfying the manufacturing specifications

N_t is the total number of circuit outcomes

Yield Optimization Problem Formulation

centering problem with fixed tolerances

$$\underset{\mathbf{x}^0}{\text{maximize}}\ Y$$

where $\mathbf{x}^0$ denotes the nominal design parameter vector

Yield Optimization of Nonlinear Circuits

comprehensive treatment of yield optimization of nonlinear microwave circuits with statistically characterized devices

one-sided ℓ_1 circuit centering with gradient approximations

efficient harmonic balance simulation with exact Jacobians

statistical representation of nonlinear devices:

> multidimensional statistical distributions of the intrinsic device and parasitic parameters

yield enhanced from 31% to 74% for a frequency doubler design having 34 statistically toleranced parameters

Specifications and Responses

nominal design $\mathbf{x}^0$

statistically sampled outcomes $\mathbf{x}^i$, i = 1, 2, ... , N

the *j*th specification is defined at the *k*th harmonic

$$S_j(k)$$

the corresponding circuit response for the outcome, $\mathbf{x}^i$, is denoted by

$$F_j(\mathbf{x}^i, k)$$

Error Functions

the error functions for the *i*th outcome, $\mathbf{e}(\mathbf{x}^i)$, comprise the entries

$$F_j(\mathbf{x}^i, k) - S_{uj}(k)$$

or

$$S_{lj}(k) - F_j(\mathbf{x}^i, k)$$

where $S_{uj}(k)$ and $S_{lj}(k)$ are upper and lower specifications

Objective Function for Yield Optimization

the generalized ℓ_1 function $v(\mathbf{e}(\mathbf{x}^i))$ for individual outcomes

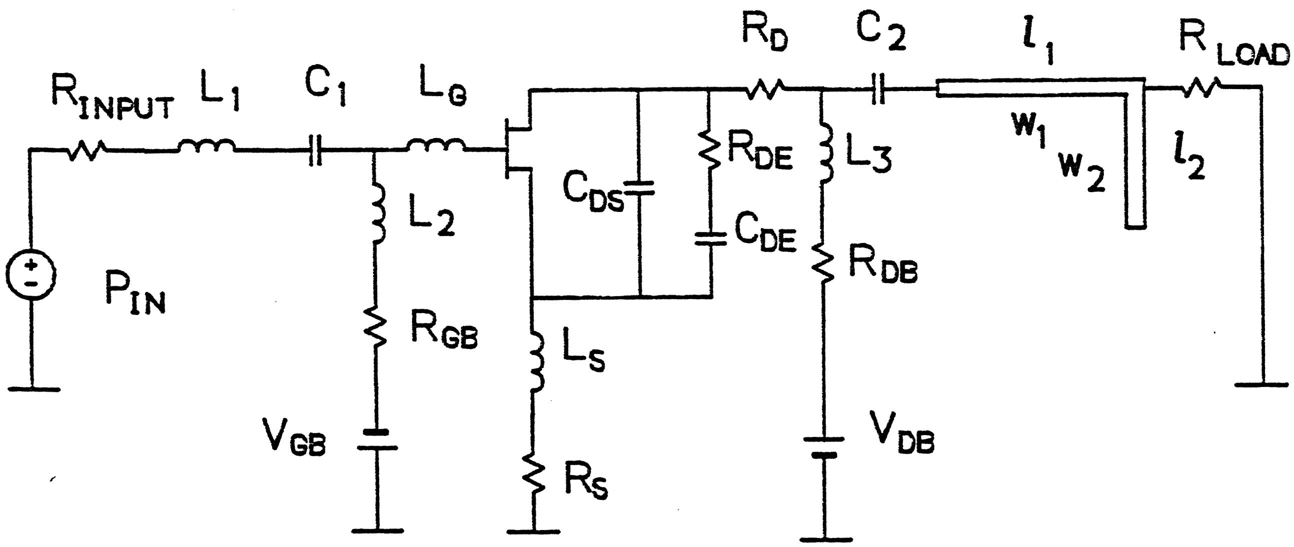
$$v(\mathbf{e}(\mathbf{x}^i)),\ i = 1, 2, \ldots, N$$

the one-sided ℓ_1 objective function for multiple outcomes

$$u(\mathbf{x}^0) = \sum_{i \in J} a_i v(\mathbf{e}(\mathbf{x}^i))$$

where $J = \{i \mid v(\mathbf{e}(\mathbf{x}^i)) > 0,\ i = 1, 2, \ldots, N\}$ and a_i are properly chosen nonzero multipliers

FET Frequency Doubler



lumped input matching circuit

microstrip output matching and filter circuit

Yield Optimization of the FET Frequency Doubler

design specifications

lower specification of 2.5 dB on conversion gain

lower specification of 19 dB on spectral purity

optimization variables

input inductance L_1

microstrip lengths l_1 and l_2

bias voltages V_{GB} and V_{DB}

driving power level P_{IN}

Yield Optimization of the FET Frequency Doubler (cont'd)

tolerances assumed

uniform distributions with 3% tolerances for 6 optimization variables

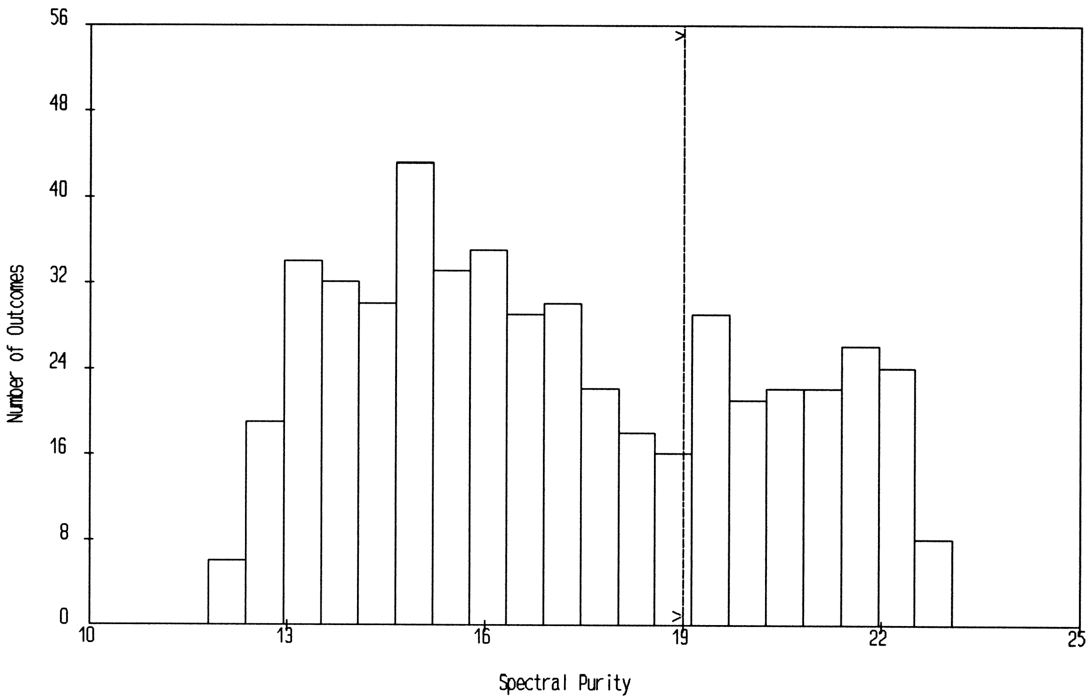
uniform distributions with 5% tolerances for 6 other elements

the large-signal FET model

modified Materka and Kacprzak model, normal distributions and correlations assumed for 22 parameters

mean values, standard deviations and correlations based on information given by *Purviance et al.* (1988)

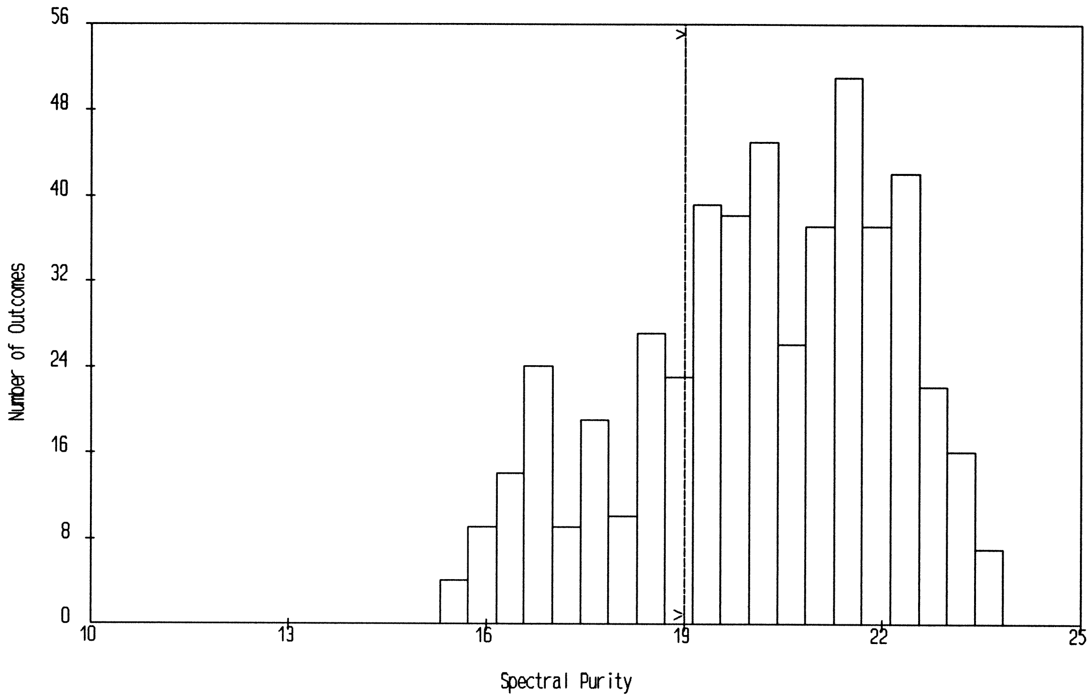
Frequency Doubler before Yield Optimization



yield estimated by Monte Carlo analysis using 500 outcomes

initial yield of 31%

Frequency Doubler after Yield Optimization



yield estimated by Monte Carlo analysis using 500 outcomes

final yield of 74%

Datapipe Architecture

software modules of diverse origin such as specialized simulators must be accommodated in general CAD systems

Datapipe (IPPC: inter-program pipe communication) utilizes UNIX interprocess pipes and facilitates high speed numerical interaction between independent programs

no modification to the IPPC-based parent program

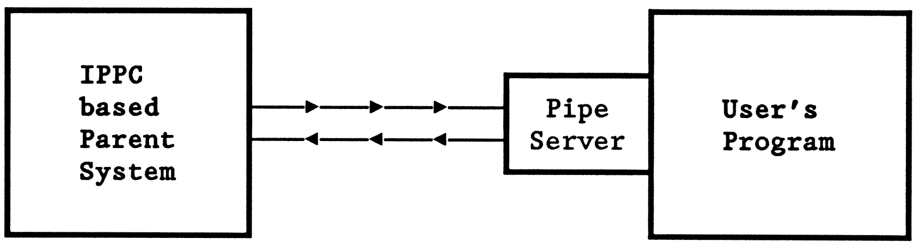
only minor modification to the child program is needed - the IPPC server has to be added to generate a pipe-ready version

during simulation or optimization involving the child, the parent executes the child as a separate process

communication between one parent and several children and grandchildren is possible

the overhead CPU cost in practical situations is found to be negligible - it typically adds only about 1% to the conventional approach of subroutine calls

Basic Form of the IPPC



in forking the child process, two interprocess pipes are created

Datapipe Applications in OSA90/hope

predefined Datapipe protocols in OSA90/hope allow an unlimited number of non-predetermined and new software modules to be added in a versatile manner with no re-compilation, no re-linking and no modification to OSA90/hope

OSA90/hope's optimizers, statistical drivers, etc., become available to interact iteratively with the new modules

the new modules can be functionally interconnected: outputs of one program can be postprocessed using expressions and applied as inputs to other programs

full graphical capabilities of OSA90/hope become available to the child programs

OSA90/hope is interfaced with Zuberek's SPICE-PAC and the *em* electromagnetic simulator from Sonnet Software, Inc.

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