COMPUTER-AIDED ENGINEERING OF NONLINEAR MICROWAVE CIRCUITS: YIELD-DRIVEN DESIGN

Interim Report

OSA-91-OS-8-R

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1. Title of the Project

COMPUTER-AIDED ENGINEERING OF NONLINEAR MICROWAVE CIRCUITS: YIELD-DRIVEN DESIGN

2. Project IRAP Code

20557U

3. IRAP Funding

July 1, 1991 - March 31, 1992:	$45,800.00
April 1, 1992 - June 30, 1992:	$15,200.00
TOTAL IRAP FUNDING	$61,000.00

4. Project Team

P1.	J.W. Bandler	Project Leader
P2.	R.M. Biernacki	Project Engineer
P3.	S.H. Chen	Project Engineer

5. Project Objectives

The purpose of the project is to research the area of statistical design centering for computer-aided design of nonlinear RF and microwave circuits, in particular for design of high frequency analog integrated circuits. The ultimate goal of this research is to develop a software system for yield-driven circuit design in the presence of device, process and other statistics. Based on the research results we are developing yield-driven design features to be included in our new, marketable packaging of OSA's technology: software system OSA90™. A number of user-oriented features are being created in order to enable the users to utilize their existing software within the power of our new system.

6. Progress To-Date

Research and development carried out within the framework of the project and their status are outlined in the following subsections.

Research towards Yield-Driven Design System

1. Study and develop theory for yield optimization of nonlinear microwave circuits operating in the steady state under large-signal excitations.

   Completed. We have studied theoretical aspects of yield optimization in conjunction with the harmonic balance simulation technique. We have identified individual error functions for different harmonics and for different circuit responses w.r.t. design specifications. This allows us to further investigate different objective functions for yield optimization.

2. Study and implement objective function formulations for yield-driven design of nonlinear microwave circuits operating in the steady state under large-signal excitations.

   In progress. We have studied and experimentally implemented a two stage formulation of the objective function where all the error functions for individual outcomes are assembled into a single generalized ℓ_p function, and then the resulting functions for all the outcomes are used to formulate a single one-sided ℓ_1 function. Currently, we are investigating a novel "yield probability function" which has certain smoothing properties and, therefore may behave better than the one-sided ℓ_1 function.

3. Study and implement the best approach to gradient estimation to facilitate the powerful gradient based optimizers.

   Completed. Our previously published FAST technique has been adapted and utilized.

4. Study the optimal time sample selection for generalized Discrete Fourier Transform in two-tone mixer and intermodulation harmonic balance analysis.

   Completed. To achieve a satisfactory level of robustness, two algorithms have been implemented. The first is an efficient method proposed by Ngoya *et al.* (*IEEE Trans. Circuits and Systems*, 1990, pp. 1339-1355). If that method fails we invoke our algorithm based on a subsidiary optimization process which aims at improving the condition number of the DFT matrix.

5. Study and implement efficient modeling techniques that can take advantage of available gradient information in constructing reliable approximate models which will then be used instead of actual circuit simulations.

   In progress. Multidimensional quadratics are used to model both the circuit responses and their gradients. Only statistical variables are utilized as the model parameters. Non-statistical design (optimizable) parameters are not involved, thus dimensionality of the model is reduced.

6. Study and develop new methods and numerical algorithms aimed at improving efficiency of statistical design of analog microwave circuits.

   In progress. Other schemes are still to be investigated.

7. Apply statistical design techniques to practical analog microwave circuits reflecting fabrication parameter spreads.

   To be done.

8. Interact with process and fabrication engineers for measurement data and process information.

   To be done during the testing stage.

9. Develop a framework for a comprehensive yield-driven design system for monolithic microwave integrated circuits.

   In progress. This involves all previous tasks.

Modules for Yield-Driven Design System

1. Module for User Interface and Command Processor for Yield Optimization.

   We have completed structural planning of the module. We have developed the input file syntax for yield optimization to allow for both statistical analysis and design optimization to be performed simultaneously. We have expanded global data structures and the user interface layout, including menus and windows.

2. Parser Module for Yield Optimization Information in the Circuit File.

   The input file Specification Block parser of OSA90 has been modified to allow for both statistical analysis and design optimization to be performed simultaneously.

3. Module for Error Function Formulation for Yield Optimization.

   A new module for assembling all the error functions for an individual outcome into a single generalized ℓ_p function has been completed. Another module for assembling those functions into a single objective function for yield optimization is currently experimented with. Further extensions to include the quadratic modeling features have been partially implemented.

4. Driver Module for Yield Optimization.

   Completed.

5. Library Modules for new Active Device and Passive Component Models.

   We are now working on an extremely promising statistical model for GaAs MESFETs. It is based on physical parameters such as gate length, gate width, doping density, etc. A preliminary version of the model has been implemented. We have also expanded our linear library by including all types of controlled sources, both ideal and non-ideal.

6. Modules for Inter-Process Communication.

   We are expanding the inter-process communication capabilities of OSA90. In addition to previously available FUN and FDF protocols we have developed the SIM and COM protocols which allow the user to pre- or post-process the input and/or output of the user's programs connected to OSA90 through pipes. Running child processes on different networked machines is being investigated.

7. Output Data Processor for Yield Optimization.

   We are currently developing a postprocessing capability for yield sensitivity option after Monte Carlo analysis. It will allow for sorting multiple statistical outcomes for displaying partial yield, both graphically and numerically.

8. Graphics Interface for Yield Optimization.

   We are developing graphics modules for plotting partial yield versus sweep parameters to graphically illustrate their influence on satisfying or violating design specifications for multiple statistical circuit outcomes.

7. Delays and Anticipated Difficulties

The project has been carried out to date according to the planned schedule. Delays have not been experienced so far. We do not anticipate insurmountable obstacles for the remainder of the project.

8. Impact of Support

OSA has the technical expertise for the proposed project. However, without financial assistance the project could not be carried out. Successful completion of the project will increase profitability and substantially contribute to development of OSA. The expected growth of the company will generate further jobs in Canada. Also, the algorithms and software modules created within this project will be extremely valuable in OSA's future products, thus reducing their development cost.

Upon completion the project will contribute to Canadian competitiveness in the microwave CAE arena and in the high-tech industry in general, currently dominated by the Americans.