DESIGN CENTERING, TOLERANCING AND TUNING: A MULTICIRCUIT OPTIMIZATION APPROACH

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A MULTICIRCUIT OPTIMIZATION APPROACH

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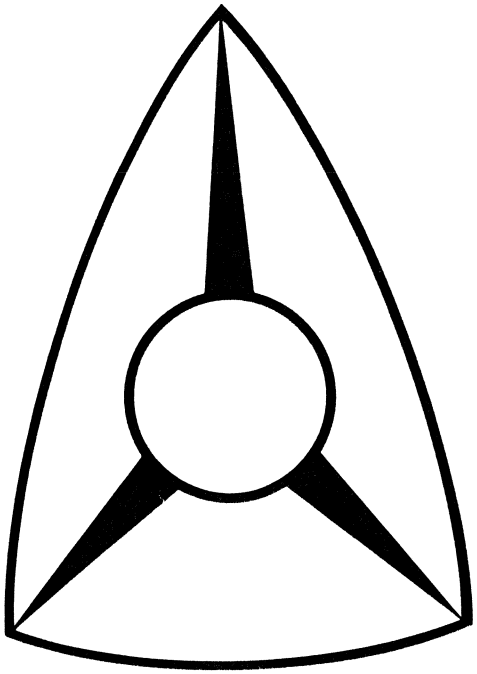

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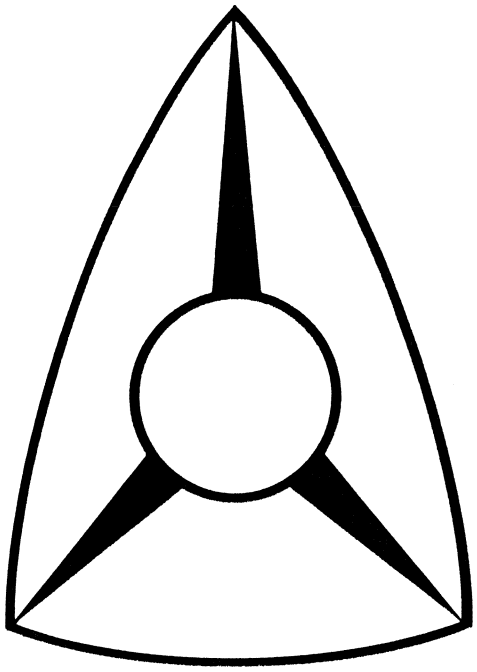


Introduction

advances in GaAs MMIC technology demand the next generation CAE software

efficient algorithms for large-scale optimization of nonlinear circuits are crucial

cost reduction is a primary goal

yield-driven optimization methodology is essential

statistical representation of physical, process and geometrical parameters must be integral to CAE

Increasing Sophistication of Design Methodology

deterministic

- performance-driven design
- fixed tolerance worst-case design
- variable tolerance worst-case design

statistical

- fixed tolerance yield-driven design
- correlated tolerances
- variable tolerance cost-driven design

Nonlinear Circuit Simulation

most analog microwave circuits operate under steady-state conditions

harmonic balance has become the major simulation tool for nonlinear circuits

popular harmonic balance software:

- typical algorithms inhibit fast optimization
- yield-driven design may be prohibitively CPU intensive
- inaccurate, slow sensitivity/gradient evaluation

OSA's research and development successfully addresses these issues

Yield Optimization

high yield is essential for large volume production of MMICs

useful CAE must account for manufacturing tolerances, model uncertainties, variations of process parameters, environmental uncertainties, etc.

yield optimization is computationally intensive

- optimization is iterative
- each iteration requires simulation of many statistically related circuits
- simulation of each nonlinear circuit is iterative

yield-driven design demands powerful, robust, fast optimizers and effective statistical representation of devices and subcircuits

Manufacturing Yield

Manufacturing yield is simply the ratio

$$Y = N_{pass}/N_t$$

where

N_{pass} is the number of circuit outcomes satisfying the design specifications

N_t is the total number of circuit outcomes

Yield Optimization Problem Formulation

centering problem with fixed tolerances

$$\underset{\mathbf{x}^0}{\text{maximize}}\ Y$$

where $\mathbf{x}^0$ denotes the nominal design parameter vector

Milestones in Yield Optimization

Bandler begins formal exploitation of parameter tolerances in circuit optimization in 1969-70

cost-driven worst-case design with optimized tolerances (1972)

optimal centering and tolerance assignment integrated with tuning at the design stage (1974)

integrated approach to microwave design with parameter tolerances, model uncertainties, mismatches and reference plane uncertainties (1975)

yield-driven optimization using general statistical distributions (1976)

optimal tuning and alignment at the production stage (1980)

Milestones in Yield Optimization (cont'd)

foundation of multicircuit ℓ_1 yield optimization (1987)

world's first yield-driven design features introduced into commercial CAD (Super-Compact 1987)

yield optimization of large-scale microwave circuits (1988)

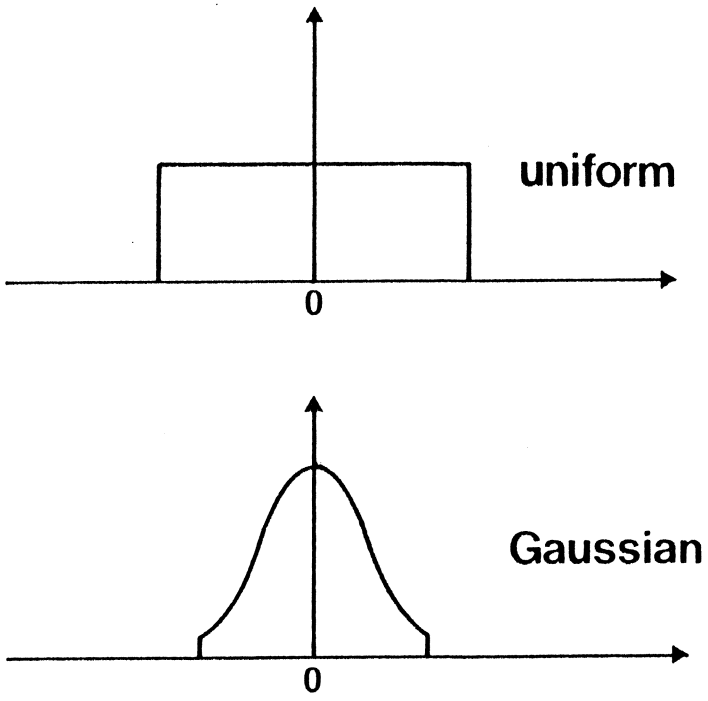
yield optimization of nonlinear circuits within the harmonic balance simulation environment (1989)

IGAT (integrated gradient approximation technique) based yield optimization of nonlinear circuits (1990)

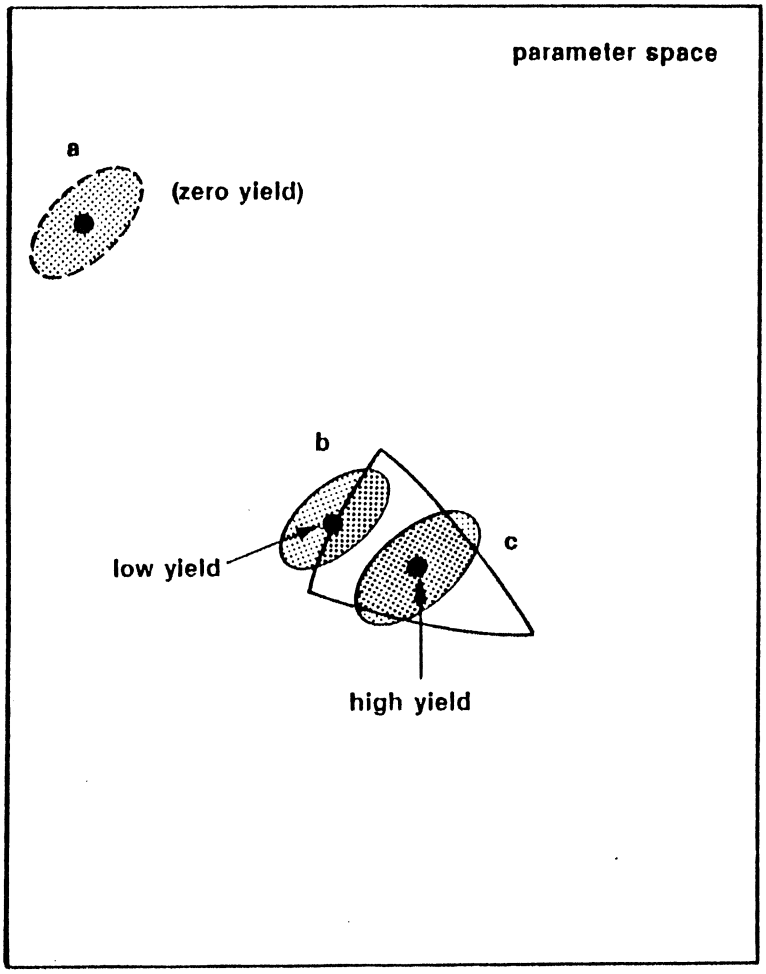
FAST™ (feasible adjoint sensitivity technique) gradient based yield optimization of nonlinear circuits (1990)

yield-driven design with dynamically integrated physics based device models (1990)

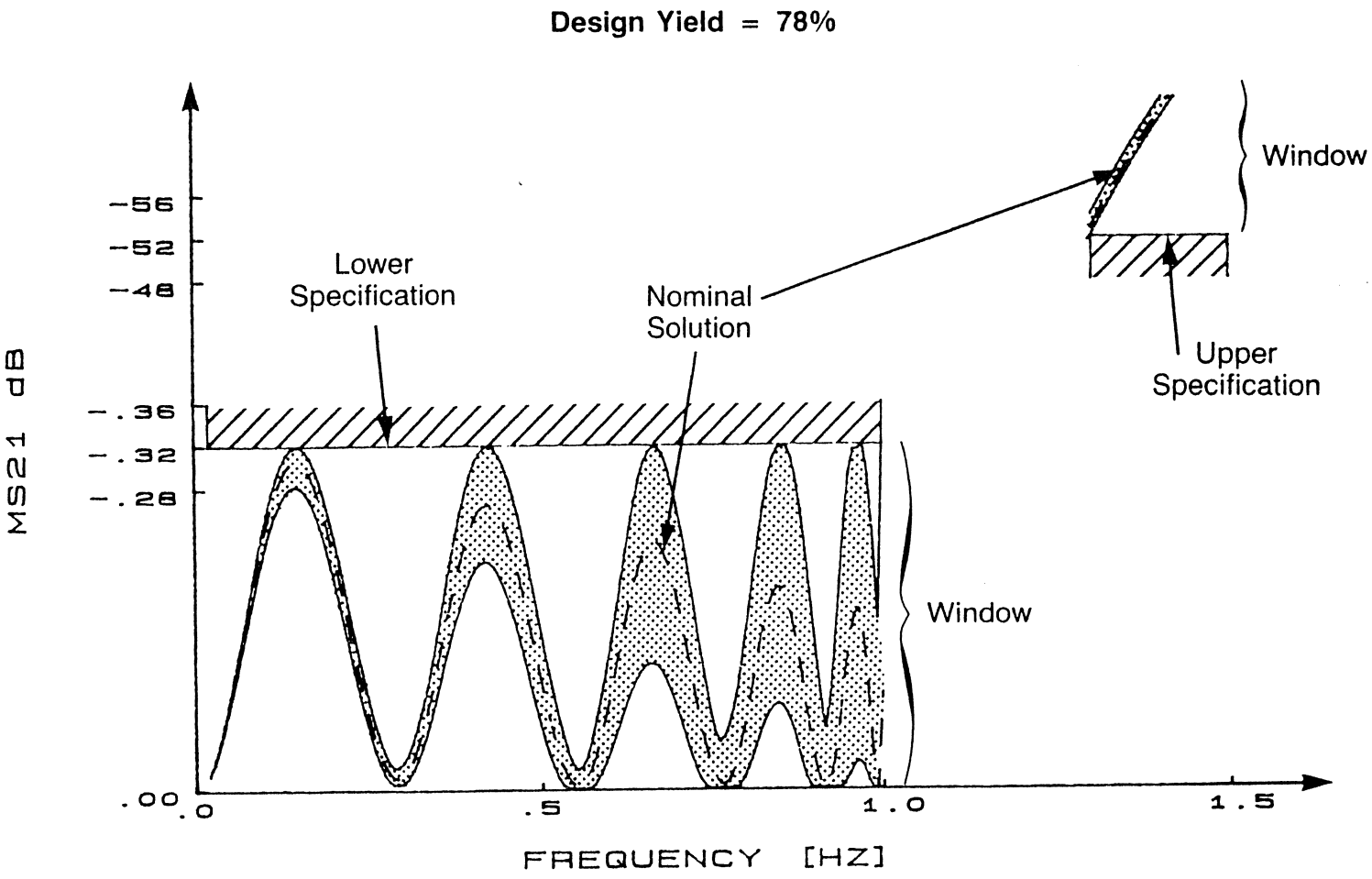
statistical modeling for HarPE™ (1990+)



Typical statistical distributions



Yield interpretation in the parameter space



Envelope diagram for the magnitude of S_{21} for centered design of 11 element LC filter

Yield Optimization of Nonlinear Microwave Circuits

pioneered by OSA

comprehensive treatment of yield optimization of nonlinear microwave circuits with statistically characterized devices

one-sided ℓ_1 circuit centering with gradient approximations

efficient harmonic balance simulation with exact Jacobians

statistical representation of nonlinear devices:

> multidimensional statistical distributions of the intrinsic device and parasitic parameters

yield enhanced from 25% to 61% for a frequency doubler design having 34 statistically toleranced parameters

Specifications and Responses

nominal design $\mathbf{x}^0$

statistically sampled outcomes $\mathbf{x}^i$, i = 1, 2, ... , N

the *j*th specification is defined at the *k*th harmonic

$S_j(k)$

the corresponding circuit response for the outcome, $\mathbf{x}^i$, is denoted by

$F_j(\mathbf{x}^i, k)$

Error Functions

the error functions for the *i*th outcome, $\mathbf{e}(\mathbf{x}^i)$, comprise the entries

$$F_j(\mathbf{x}^i, k) - S_{uj}(k)$$

or

$$S_{lj}(k) - F_j(\mathbf{x}^i, k)$$

where $S_{uj}(k)$ and $S_{lj}(k)$ are upper and lower specifications

Objective Function for Yield Optimization

the generalized ℓ_1 function $v(\mathbf{e}(\mathbf{x}^i))$ for individual outcomes

$$v(\mathbf{e}(\mathbf{x}^i)),\ i = 1, 2, \ldots, N$$

the one-sided ℓ_1 objective function for multiple outcomes

$$u(\mathbf{x}^0) = \sum_{i \in J} a_i v(\mathbf{e}(\mathbf{x}^i))$$

where $J = \{i \mid v(\mathbf{e}(\mathbf{x}^i)) > 0,\ i = 1, 2, \ldots, N\}$ and a_i are properly chosen nonzero multipliers

Yield Optimization of the FET Frequency Doubler

design specifications

lower specification of 2.5 dB on conversion gain

lower specification of 19 dB on spectral purity

optimization variables

input inductance L_1

microstrip lengths l_1 and l_2

bias voltages V_{GB} and V_{DB}

driving power level P_{IN}

Yield Optimization of the FET Frequency Doubler (cont'd)

tolerances assumed

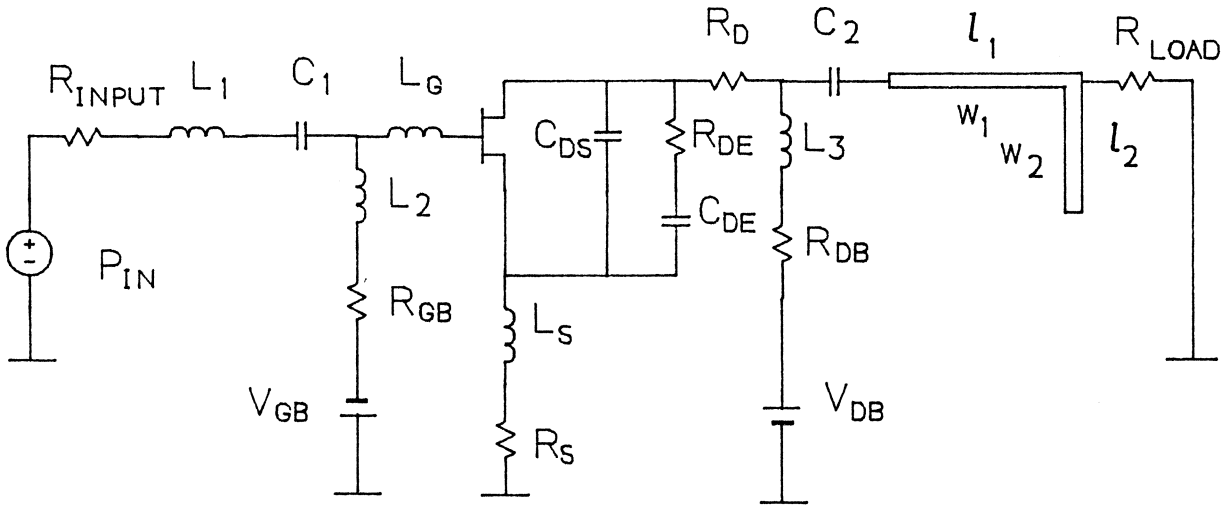
- uniform distributions with 3% tolerances for 6 optimization variables

- uniform distributions with 5% tolerances for 6 other elements

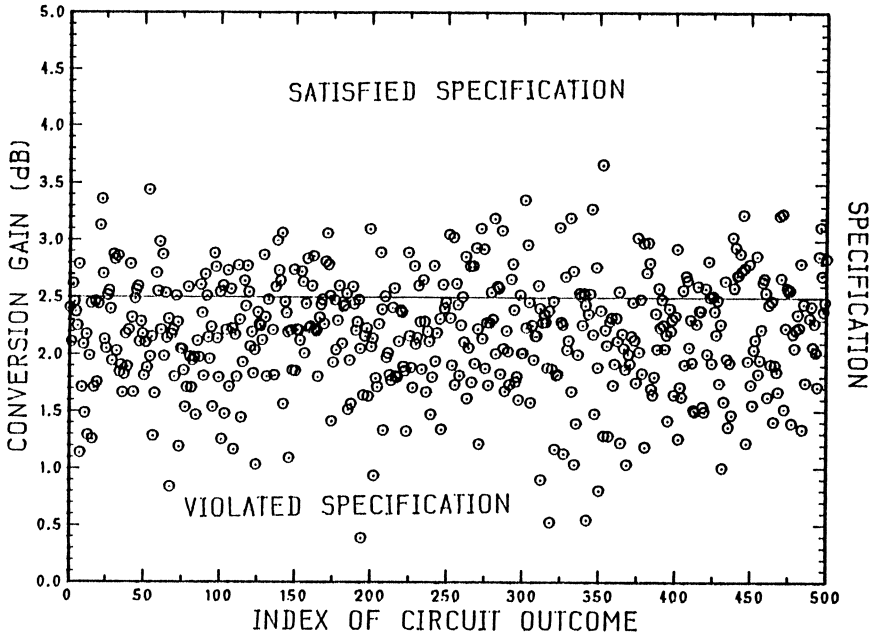
the large-signal FET model

- modified Materka and Kacprzak model, normal distributions and correlations assumed for 22 parameters

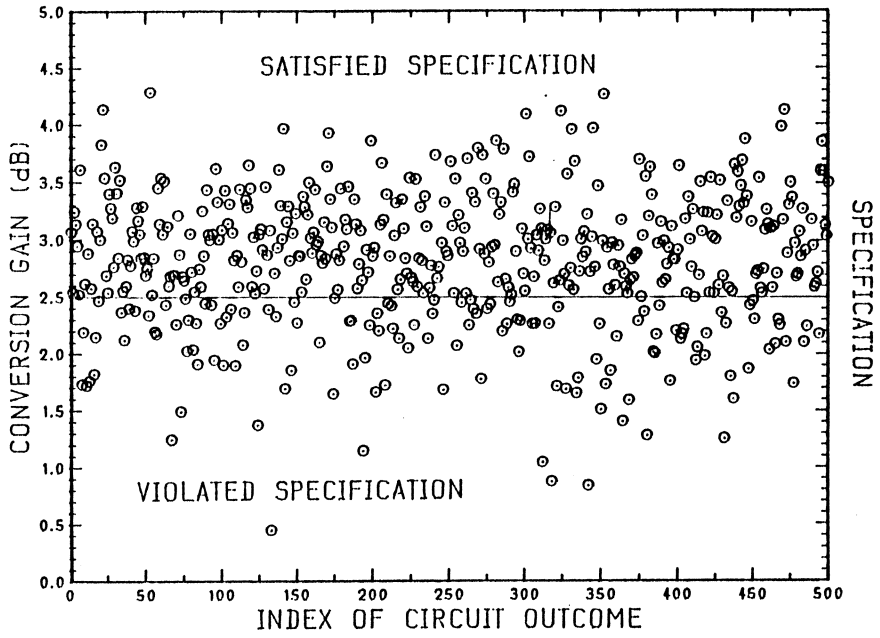
mean values, standard deviations and correlations based on information given by *Purviance et al.* (1988)



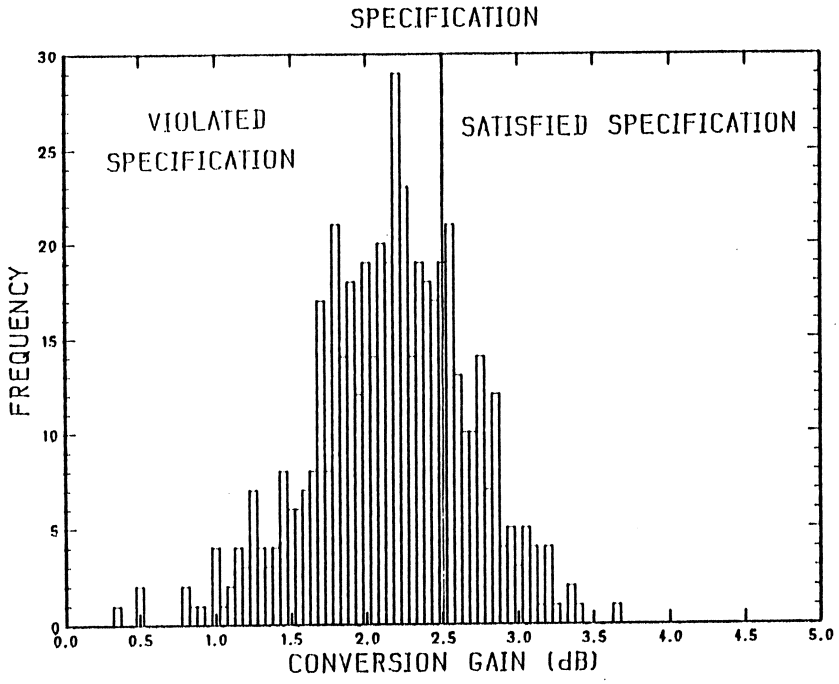
FET frequency doubler



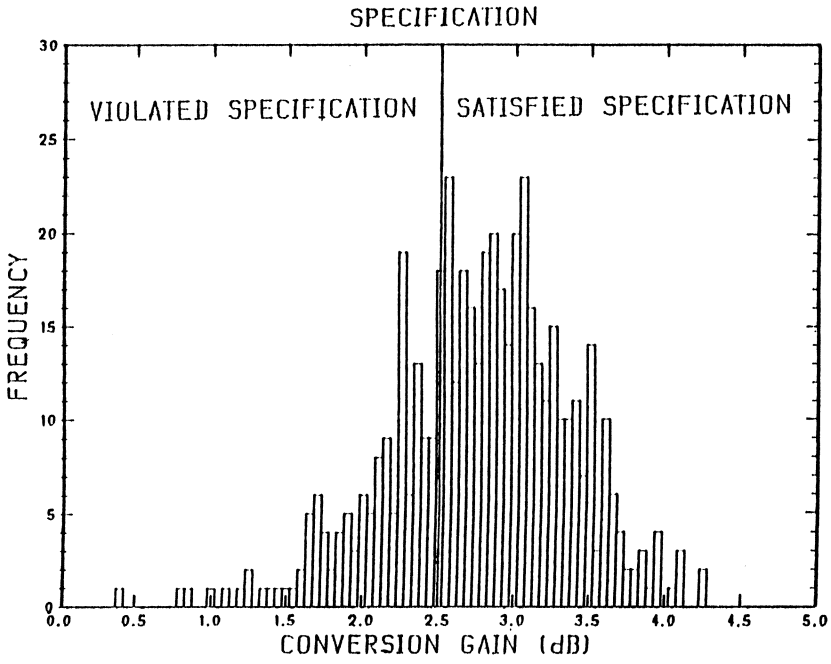
Run chart of the conversion gain for
the frequency doubler - before optimization



Run chart of the conversion gain for the frequency doubler - after optimization



Histogram of the conversion gains for 500 frequency doubler outcomes - before optimization



Histogram of the conversion gains for 500 frequency doubler outcomes - after optimization

FAST™

a breakthrough in circuit theory

an expedient implementation of the EAST concept

unmatched speed and accuracy over perturbation

implementable in general purpose CAE architectures

combines efficiency of exact adjoint sensitivities with simplicity of conventional perturbation

concept applicable to Jacobian evaluation for fast harmonic balance simulation

the basis of the world's most powerful harmonic balance optimizer (featured in HarPE)

Optimization with Physics Based Model

true device design: optimization to adjust physical, geometrical and process variables before device fabrication

overall circuit performance reflects geometrical dimensions, material parameters, doping profile, channel thickness, etc.

essential for meaningful statistical analysis and yield optimization

HarPE implementation (1990) of analytical large-signal model based on the work of Khatibzadeh and Trew (1988)

Impact of Yield Optimization on Tunable Circuit Design

drive up the probability of obtaining circuits that exhibit good initial responses for the tuning process

increase the possibility of the circuit outcomes satisfying specifications after tuning easy-to-tune elements

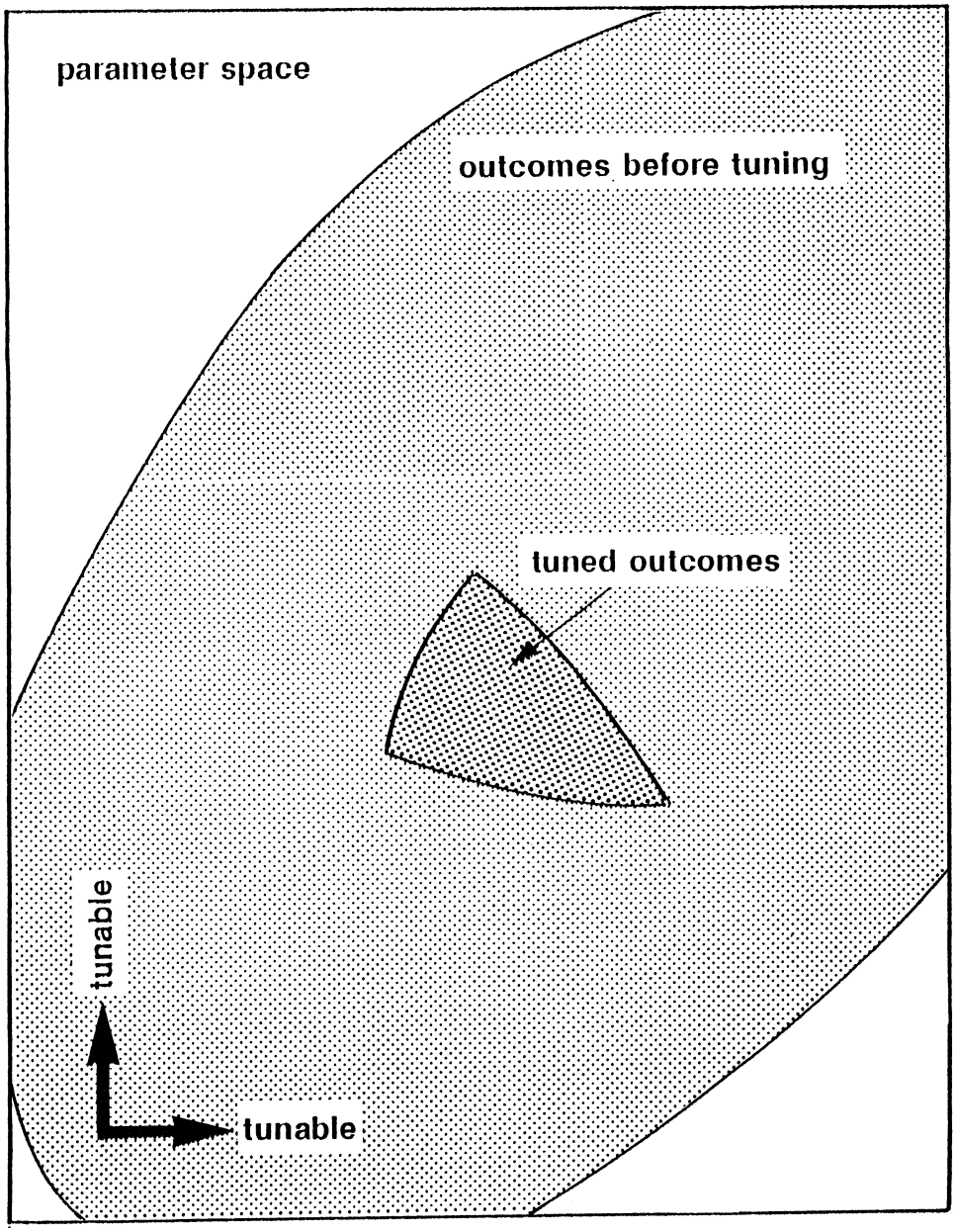
Statistical Outcomes

the *k*th tunable outcome $\mathbf{x}^k$ may be described by

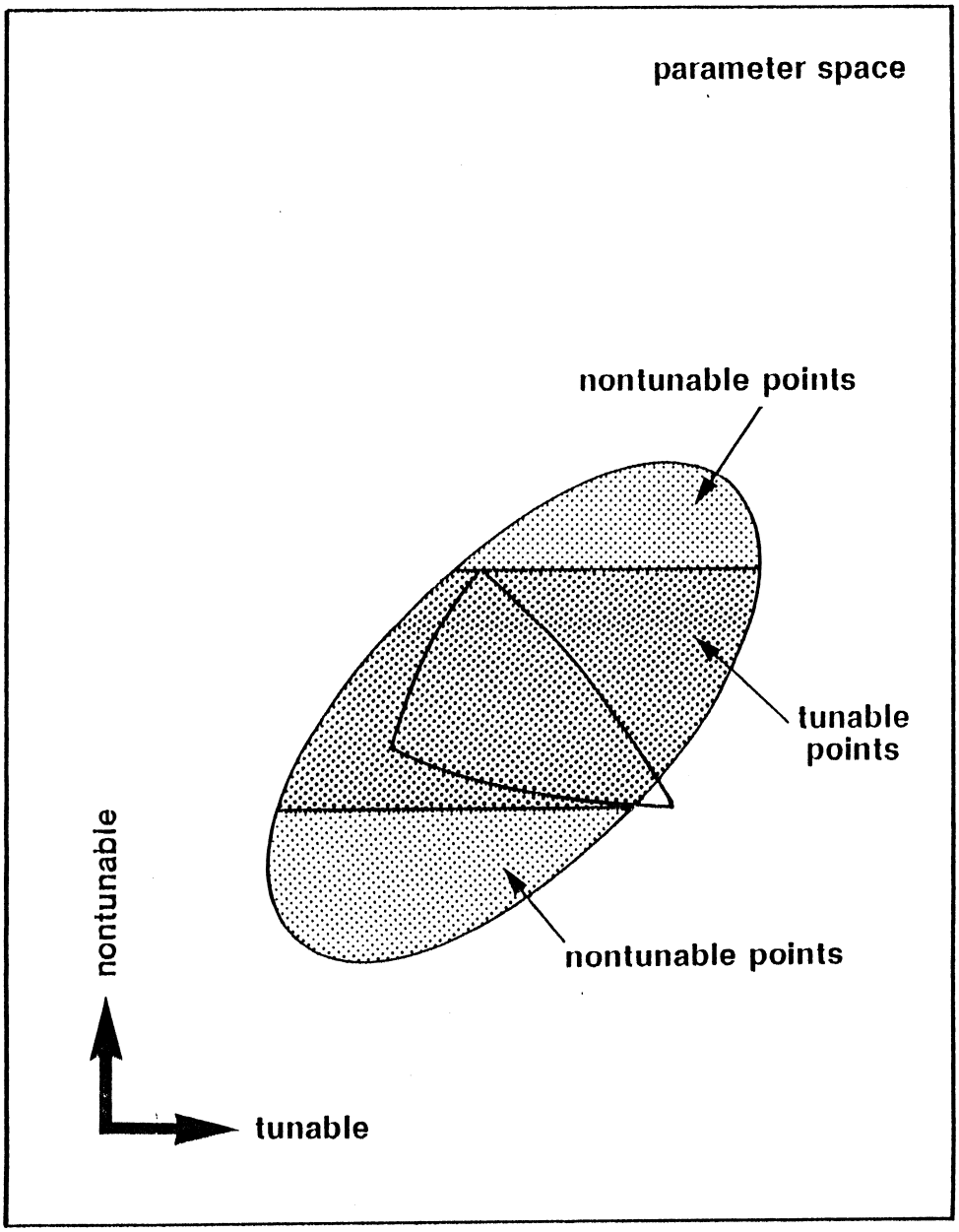
$$\mathbf{x}^k = \mathbf{x}^0 + \mathbf{r}^k, \quad \mathbf{r}^k = \mathbf{s}^k + \mathbf{t}^k + \mathbf{s}_t^k, \quad k = 1, 2, \ldots, N_t$$

where

- $\mathbf{s}^k$ represents model uncertainties and manufacturing tolerances
- $\mathbf{t}^k$ represents postproduction tuning adjustments
- $\mathbf{s}_t^k$ represents tuning imprecisions

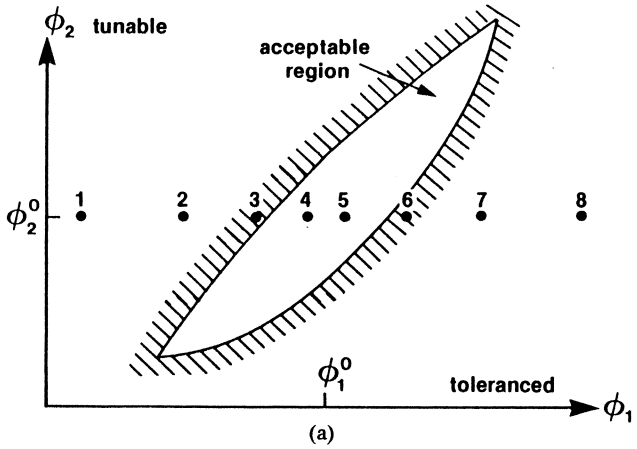


Effect of tuning



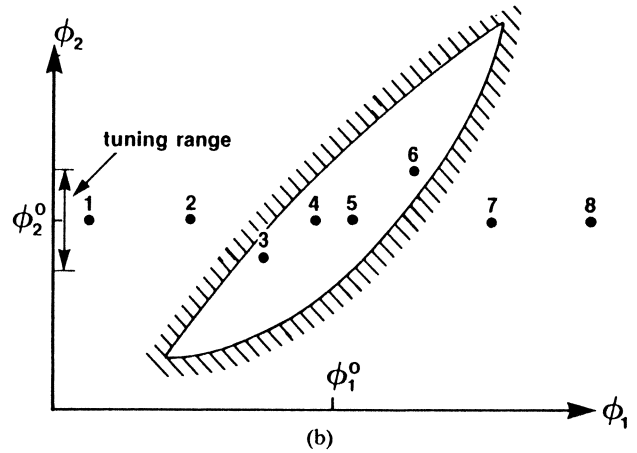
Impact of tunable and nontunable parameters

no tuning
yield = 25%



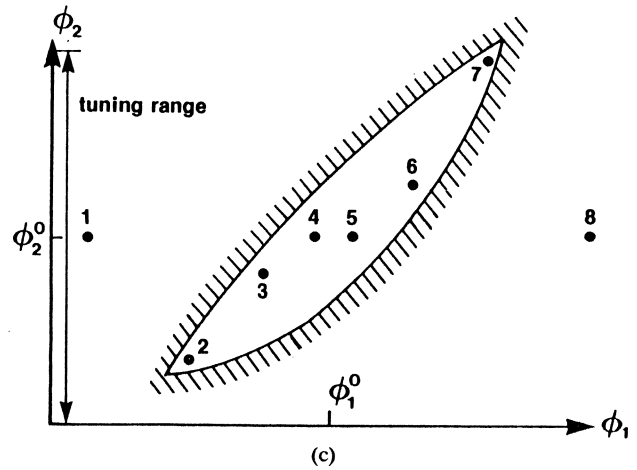
(a)

small tuning range
yield = 50%



(b)

large tuning range
yield = 75%



(c)

Worst-Case Design

goal: centered design with largest possible tolerances

vertex selection

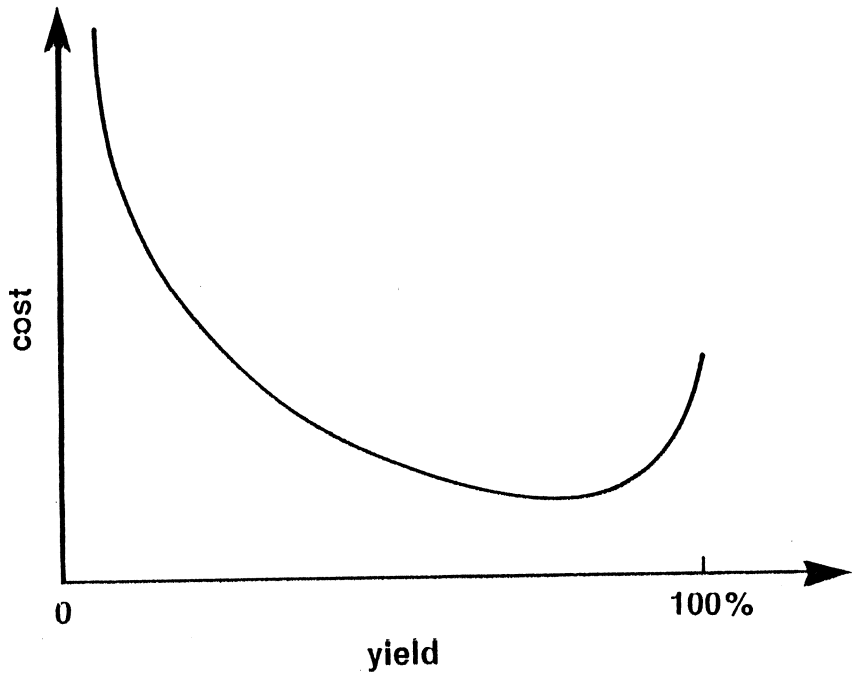
worst-case estimates by sensitivities

worst-case estimates by exact simulation

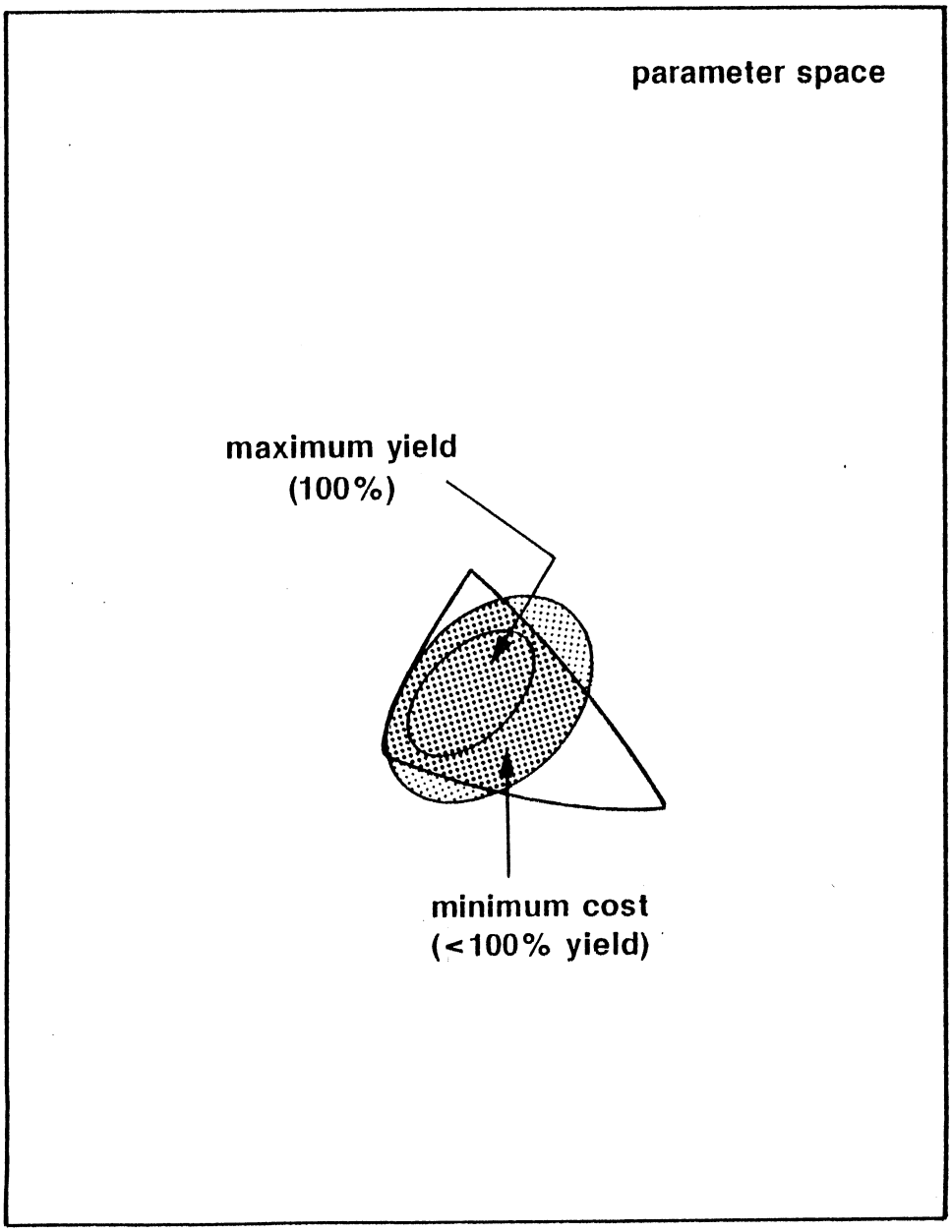
worst-case estimates by optimization

Monte-Carlo estimate of worst cases

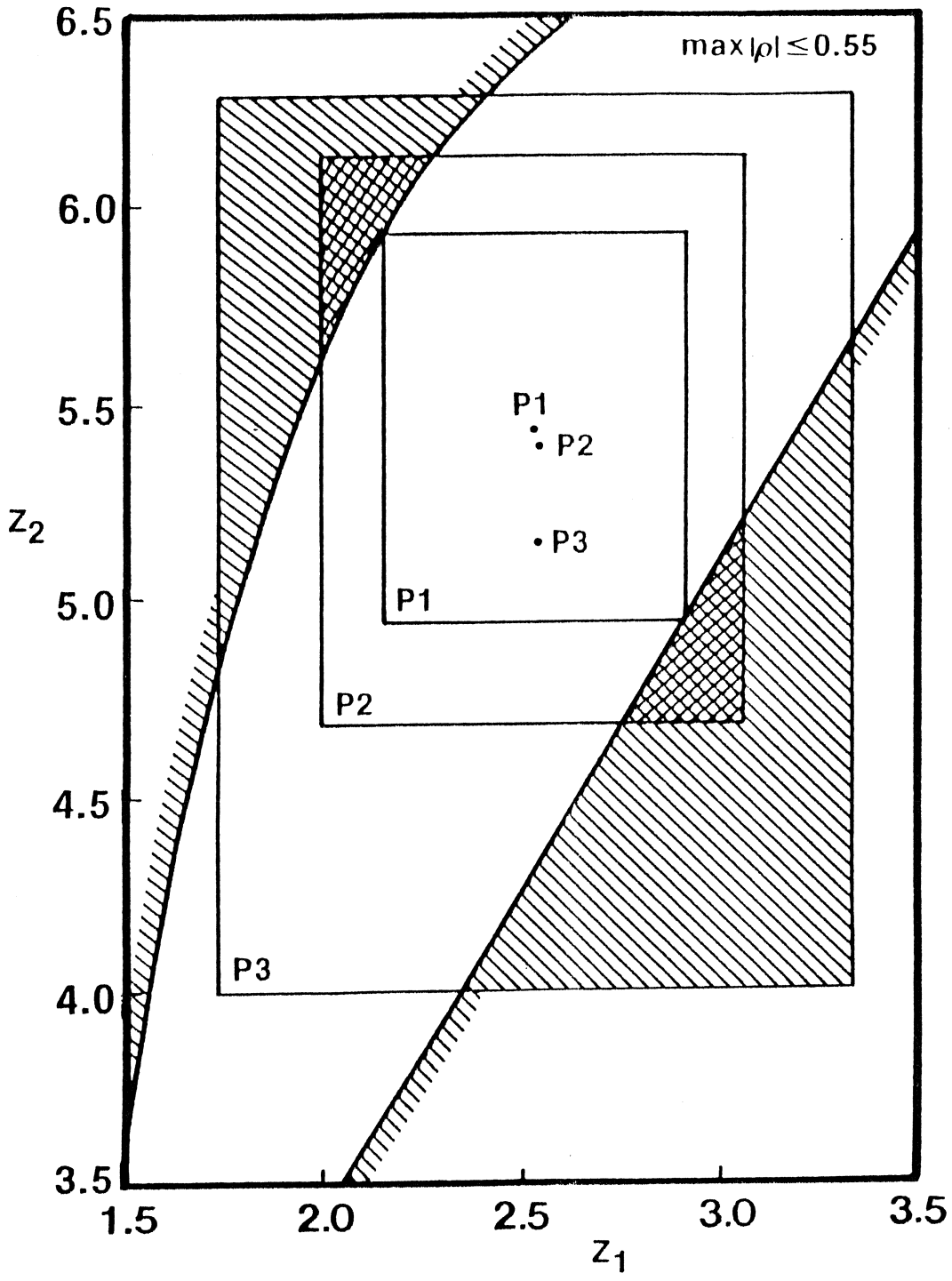
optimization for 100% yield

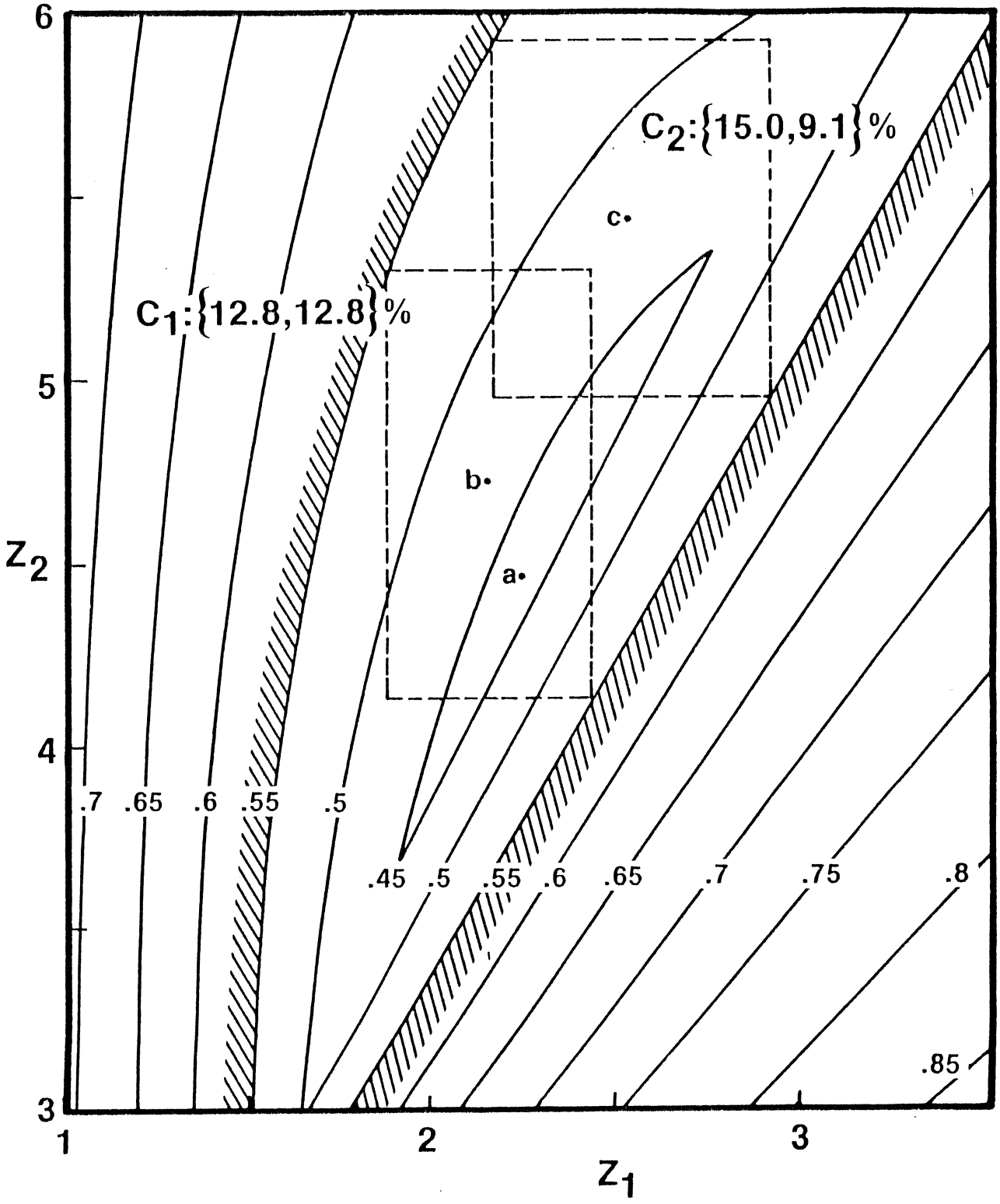


Yield-cost relationship



Cost optimization


max |ρ| ≤ 0.55
P1
P2
P3
P1
P2
P3
6.5
6.0
5.5
5.0
4.5
4.0
3.5
Z2
1.5
2.0
2.5
3.0
3.5
Z1


6
5
4
3
1
2
3
Z_2
Z_1
C_1:{12.8,12.8}%
C_2:{15.0,9.1}%
a•
b•
c•
.7
.65
.6
.55
.5
.45
.5
.55
.6
.65
.7
.75
.8
.85

Basis for World's Most Advanced Microwave Optimizer

multicircuit concept *Bandler, Chen and Daijavad* (1986)

the highly efficient optimization algorithm of *Bandler, Chen and Madsen* (1988)

the integrated gradient approximation technique (IGAT) by *Bandler, Chen, Daijavad and Madsen* (1988)

the exact adjoint sensitivity technique (EAST) for harmonic balance *Bandler, Zhang and Biernacki* (1988)

efficient quadratic approximation to circuit responses *Biernacki, Bandler, Song and Zhang* (1989)

the feasible adjoint sensitivity technique (FAST™) for harmonic balance *Bandler, Zhang and Biernacki* (1989)

dynamically integrated physics based device models *Bandler, Zhang and Cai* (1990)

analytically unified DC/small-signal/large-signal design *Bandler, Biernacki, Chen, Song, Ye and Zhang* (1990)