YIELD OPTIMIZATION OF NONLINEAR CIRCUITS WITH STATISTICALLY CHARACTERIZED DEVICES

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YIELD OPTIMIZATION OF NONLINEAR CIRCUITS WITH STATISTICALLY CHARACTERIZED DEVICES

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Outline

yield optimization of nonlinear microwave circuits with statistically characterized devices

one-sided ℓ_1 circuit centering with gradient approximations

harmonic balance simulation with exact Jacobians

multidimensional statistical distributions of the intrinsic FET and parasitic parameters

yield optimization of a FET frequency doubler and a FET small-signal amplifier

Specifications and Responses

nominal design ϕ^0

statistically sampled outcomes ϕ^i, i = 1, 2, ... , N

the *j*th specification is defined at the *k*th harmonic

$S_j(k)$

the corresponding circuit response for the outcome, ϕ^i, is denoted by

$F_j(\phi^i, k)$

Error Functions

the error functions for the ith outcome, $\mathbf{e}(\boldsymbol{\phi}^i)$, comprise the entries

$$F_j(\boldsymbol{\phi}^i, k) - S_{uj}(k)$$

or

$$S_{lj}(k) - F_j(\boldsymbol{\phi}^i, k)$$

where $S_{uj}(k)$ and $S_{lj}(k)$ are upper and lower specifications

Yield Estimation

an outcome ϕ^i represents an acceptable circuit if all entries in $e(\phi^i)$ are nonpositive

yield can be estimated by

$$Y \approx N_{pass}/N$$

where N_{pass} is the number of acceptable circuits

Objective Function for Yield Optimization

the generalized ℓ_1 function $v(e(\phi^i))$ for individual outcomes

$$v(e(\phi^i)),\ i = 1, 2, \ldots, N$$

the one-sided ℓ_1 objective function for multiple outcomes

$$u(\phi^0) = \sum_{i \in J} \alpha_i v(e(\phi^i))$$

where $J = \{i \mid v(e(\phi^i)) > 0,\ i = 1, 2, \ldots, N\}$ and α_i are properly chosen nonzero multipliers

Optimization Algorithm and Gradient Approximations

the highly efficient optimization algorithm of Bandler, Chen and Madsen (1988) is used to minimize $u(\phi^0)$, achieving a centered design with improved yield

the flexible and effective gradient approximation algorithm proposed by Bandler, Chen, Daijavad and Madsen (1988) is modified here to provide numerical gradients

Circuit Simulation

our circuit simulation uses the harmonic balance method with exact Jacobian matrices

Statistical Models of Large-Signal FETs

statistical models consisting of large-signal equivalent circuits, statistical distributions of parameters and correlations among parameters

Generation of Statistical Outcomes

a random number generator capable of generating statistical outcomes from uniform and normal distributions, including correlations between some parameters

Yield Optimization of the FET Frequency Doubler

Design Specifications

lower specification of 2.5 dB on conversion gain
lower specification of 19 dB on spectral purity

Optimization Variables

input inductance L_1
microstrip lengths l_1 and l_2
bias voltages V_{GB} and V_{DB}
driving power level P_{IN}

Yield Optimization of the FET Frequency Doubler (cont'd)

Tolerances Assumed

uniform distributions with 3% tolerances for 6 optimization variables
uniform distributions with 5% tolerances for 6 other elements

The Large-Signal FET Model

modified Materka and Kacprzak model, normal distributions and correlations assumed for 22 parameters

mean values, standard deviations and correlations based on information given by Purviance *et al.* (1988)

Yield Optimization of the FET Frequency Doubler (cont'd)

starting point for yield optimization
(solution of nominal design)

estimated yield: 24.8%

the first phase of yield optimization

50 statistical outcomes, 41 circuit simulations
estimated yield: 57.0%

the second phase of yield optimization

50 statistical outcomes, 26 circuit simulations
estimated yield: 61.4%

Yield Optimization of the FET Small-Signal Amplifier

Design Specifications

$|S_{11}| \leq$ -6 dB, $|S_{22}| \leq$ -6 dB and 18 dB $\leq |S_{21}| \leq$ 20 dB

Optimization Variables

bias voltages V_{GB} and V_{DB}, characteristic impedances and electrical lengths of 4 transmission lines

Tolerances Assumed

uniform distributions with 3% tolerances are assumed for 10 optimization variables and 6 elements in the input and output networks

Yield Optimization of the FET Small-Signal Amplifier (cont'd)

starting point for yield optimization
(solution of nominal design)

estimated yield: 35.8%

the first phase of yield optimization

50 statistical outcomes, 30 circuit simulations
estimated yield: 49.6%

the second phase of yield optimization

50 statistical outcome, 88 circuit simulations
estimated yield: 68.4%

Conclusions

first demonstration of yield optimization of statistically characterized nonlinear microwave circuits

advanced one-sided ℓ_1 design centering combined with efficient harmonic balance simulation

large-signal FET parameter statistics fully handled

comprehensive numerical experiments verify our approach

bias conditions variable for optimal small-signal performance

ASSUMED STATISTICAL DISTRIBUTIONS FOR THE FET PARAMETERS

FET Parameter	Nominal Value	Standard Deviation	FET Parameter	Nominal Value	Standard Deviation
L_G(nH)	0.16	5%	S_l	0.676×10^{-1}	0.65%
R_D(Ω)	2.153	3%	K_G	1.1	0.65%
L_S(nH)	0.07	5%	τ(pS)	7.0	6%
R_S(Ω)	1.144	5%	S_S	1.666×10^{-3}	0.65%
R_{DE}(Ω)	440	14%	I_{G0}(A)	0.713×10^{-5}	3%
C_{DE}(pF)	1.15	3%	α_G	38.46	3%
C_{DS}(pF)	0.12	4.5%	I_{B0}(A)	-0.713×10^{-5}	3%
I_{DSS}(A)	6.0×10^{-2}	5%	α_B	-38.46	3%
V_{p0}(V)	-1.906	0.65%	R_{10}(Ω)	3.5	8%
γ	-15×10^{-2}	0.65%	C_{10}(pF)	0.42	4.16%
E	1.8	0.65%	C_{F0}(pF)	0.02	6.64%

The following parameters are considered as deterministic:
$K_E = 0.0$, $K_R = 1.111$, $K_1 = 1.282$, $C_{1S} = 0.0$, and $K_F = 1.282$

FET MODEL PARAMETER CORRELATIONS

	L_G	R_S	L_S	R_{DE}	C_{DS}	g_m	τ	R_{IN}	C_{GS}	C_{GD}
L_G	1.00	-0.16	0.11	-0.22	-0.20	0.15	0.06	0.15	0.25	0.04
R_S	-0.16	1.00	-0.28	0.02	0.06	-0.09	-0.16	0.12	-0.24	0.26
L_S	0.11	-0.28	1.00	0.11	-0.26	0.53	0.41	-0.52	0.78	-0.12
R_{DE}	-0.22	0.02	0.11	1.00	-0.44	0.03	0.04	-0.54	0.02	-0.14
C_{DS}	-0.20	0.06	-0.26	-0.44	1.00	-0.13	-0.14	0.23	-0.24	-0.04
g_m	0.15	-0.09	0.53	0.03	-0.13	1.00	-0.08	-0.26	0.78	0.38
τ	0.06	-0.16	0.41	0.04	-0.14	-0.08	1.00	-0.19	0.27	-0.46
R_{IN}	0.15	0.12	-0.52	-0.54	0.23	-0.26	-0.19	1.00	-0.35	0.05
C_{GS}	0.25	-0.24	0.78	0.02	-0.24	0.78	0.27	-0.35	1.00	0.15
C_{GD}	0.04	0.26	-0.12	-0.14	-0.04	0.38	-0.46	0.05	0.15	1.00

Certain modifications have been made to adjust these small-signal parameter correlations to be consistent with the large-signal FET model.

YIELD OPTIMIZATION
OF THE FET FREQUENCY DOUBLER

Variables	Starting Point	Nominal Design	Solution I	Solution II
P_{IN}(W)	2.0000×10^{-3}*	2.0000×10^{-3}	2.5000×10^{-3}	2.4219×10^{-3}
V_{GB}(V)	-1.9060*	-1.9060	-1.9010	-1.9011
V_{DB}(V)	5.0000*	5.0000	4.9950	4.9949
L_1(nH)	1.0000	5.4620	5.4670	5.4670
l_1(m)	1.0000×10^{-3}	1.4828×10^{-3}	1.6306×10^{-3}	1.7088×10^{-3}
l_2(m)	5.0000×10^{-3}	5.7705×10^{-3}	5.7545×10^{-3}	5.7466×10^{-3}
Yield		24.8%	57.0%	61.4%
No. of Optimization Iterations			11	8
No. of Function Evaluations			41	26

* Not considered as variables in nominal design

The yield is estimated from 500 outcomes

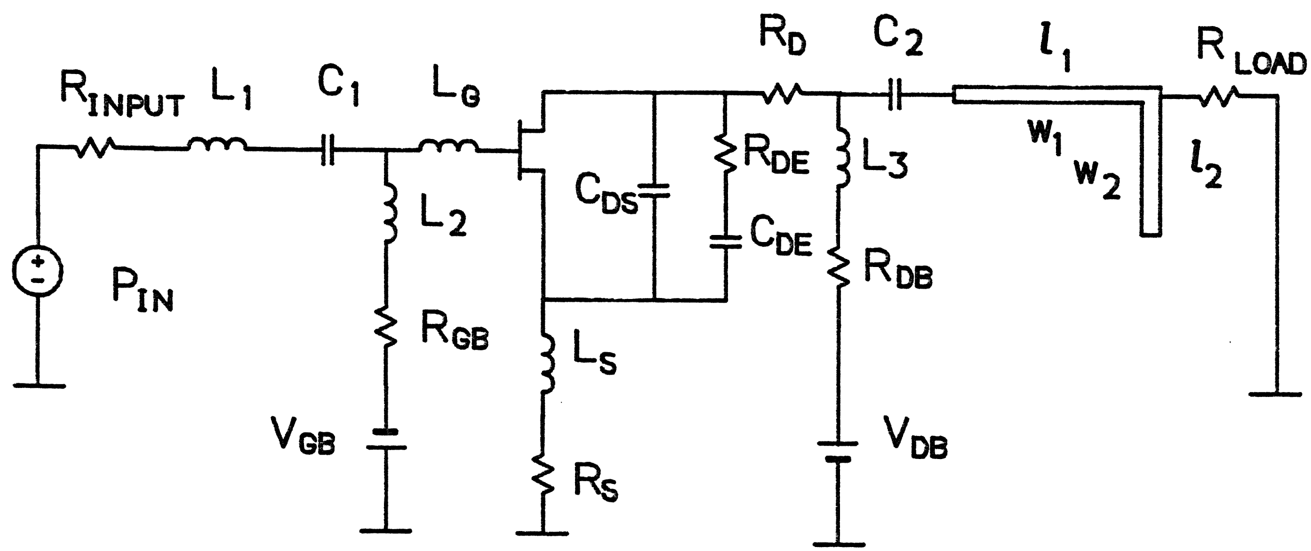
YIELD OPTIMIZATION
OF THE FET SMALL-SIGNAL AMPLIFIER

Variables	Starting Point	Nominal Design	Solution I	Solution II
V_{GB}(V)	-0.9500*	-0.9500	-0.9485	-0.9394
V_{DB}(V)	4.000*	4.000	3.824	3.733
L_1(nH)	*	3.973	4.066	4.086
$Z_1(\Omega)$	50.00	77.15	77.32	77.38
$l_1(°)$	50.00	63.02	63.21	63.27
$Z_2(\Omega)$	50.00	90.76	90.85	90.87
$l_2(°)$	50.00	31.37	31.38	31.36
$Z_3(\Omega)$	50.00	49.45	49.54	49.60
$l_3(°)$	50.00	74.11	74.21	74.30
Yield		31.0%	64.2%	71.4%
No. of Optimization Iterations			17	10
No. of Function Evaluations			72	40

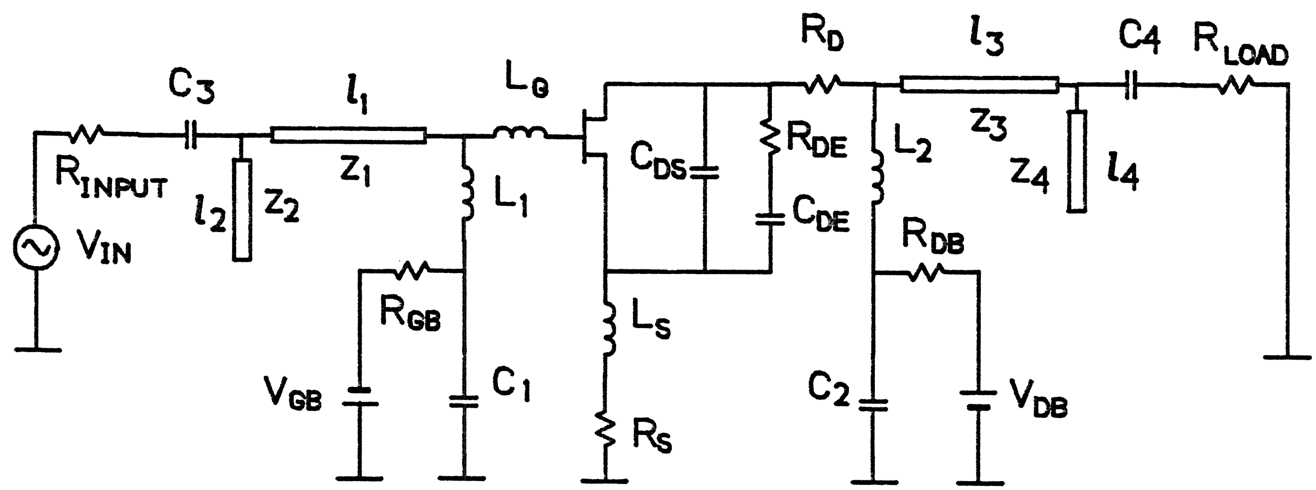
* Not considered as variables in nominal design

The yield is estimated from 500 outcomes

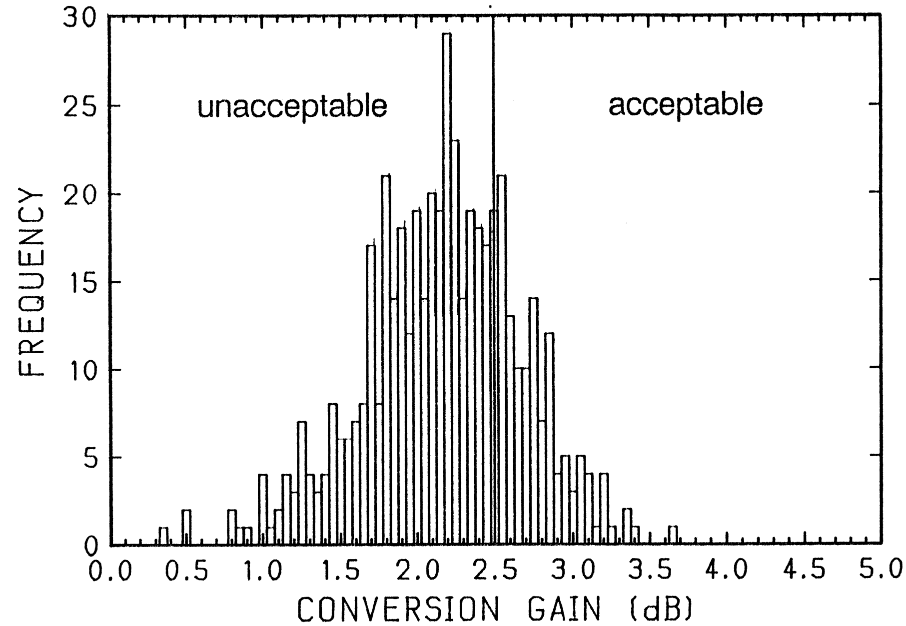
The FET Frequency Doubler



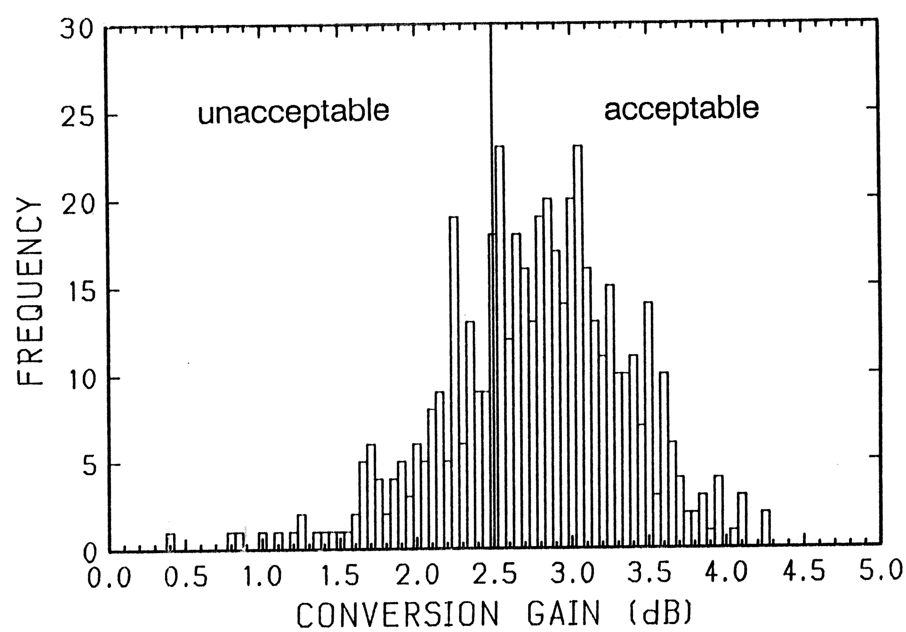
The FET Small-Signal Amplifier



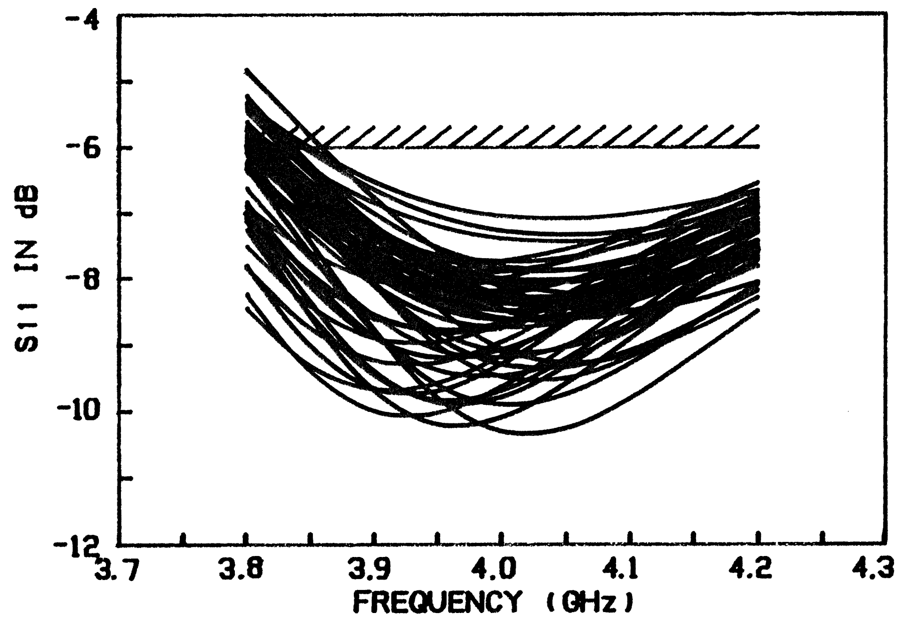
Histogram of Conversion Gains for 500 Outcomes Before Yield Optimization



Histogram of Conversion Gains for 500 Outcomes After Yield Optimization



| S_{11} | *for 50 Outcomes Before Yield Optimization*



| S_{11} | *for 50 Outcomes After Yield Optimization*