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Abstract A comprehensive treatment of yield optimization of nonlinear microwave circuits with statistically characterized devices is proposed. Yield-driven design for nonlinear microwave circuits is formulated as a one-sided ℓ_1 optimization problem. An advanced one-sided ℓ_1 algorithm is fully exploited in the solution process. Effective gradient approximations make the these difficult practical problems tractable. Attention is focused on microwave nonlinear circuits suitable for simulation by the harmonic balance method. With exact Jacobian matrices, the harmonic balance technique delivers fast and reliable solutions. The generation of statistical outcomes for design involves various kinds of statistical distributions and correlations of circuit elements. Multidimensional statistical distributions of the intrinsic and parasitic parameters of FETs are fully handled. Our approach has been verified by two microwave circuit examples. Yield is driven from 25% to 61% for a frequency doubler design having 34 statistically toleranced parameters. By optimizing the bias conditions, yield of a small-signal amplifier is increased from 31% to 71%.

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I. INTRODUCTION

Yield optimization [1-3] has been extensively explored in the literature. A number of algorithms have been proposed for statistical design centering, e.g., by Director and Hachtel [4] (simplicial approximation), Soin and Spence [5] (the center of gravity method), Bandler and Abdel-Malek [6, 7] (updated approximations and cuts), Styblinski and Ruszczynski [8] (stochastic approximation), Polak and Sangiovanni-Vincentelli [9] (outer approximation), Singhal and Pinel [10] (parametric sampling). For linear circuits, it is currently finding its way into commercial microwave CAD software.

Because of its special difficulties, yield optimization of practical nonlinear microwave circuits remains unaddressed hitherto. Requirements essential to yield optimization of nonlinear microwave circuits are: (a) effective approaches to design centering, (b) highly efficient optimization techniques, (c) fast and reliable simulation, (d) flexibility of handling various statistical representations of devices and elements, and (e) low design costs and short design cycles.

The primary purpose of this paper is to describe general concepts related to yield optimization of nonlinear microwave circuits with statistically characterized devices and to offer an efficient approach for yield-driven optimization. We formulate the yield problem for nonlinear circuits as a one-sided ℓ_1 optimization problem. A powerful and robust one-sided ℓ_1 algorithm proposed by Bandler et al. [11] is adopted. An effective gradient approximation technique presented by Bandler et al. [12] is integrated with the one-sided ℓ_1 algorithm to handle inexact gradients. The harmonic balance method is implemented with exact Jacobian matrices for fast convergence and improved robustness. Independent and/or correlated normal distributions and uniform distributions describing large-signal FET model parameters and passive elements are fully accommodated.

The yield optimization of a microwave frequency doubler with a large-signal excitation and statistically simulated FET model is successfully carried out. The performance yield is

increased from 25% to 61%. We believe that this is the first demonstration of yield optimization of nonlinear microwave circuits operating under large-signal steady-state periodic or almost periodic conditions.

We also consider a small-signal amplifier. The harmonic balance method enables us to simulate the small-signal linearized circuit under variable DC bias conditions and, consequently, to study the effects of operating conditions on performance yield of the circuit. The yield of the amplifier is increased from 31% to 71%.

In Section II we introduce the yield problem for nonlinear circuit design. Section III gives the mathematical formulation of yield optimization [3], the one-sided ℓ_1 optimization algorithm [11], and the effective gradient approximation technique [12]. A brief description of the harmonic balance method is provided in Section IV. In Section V we discuss the generation of statistical outcomes for nonlinear circuits with large-signal FET models. In Sections VI and VII two yield optimization examples of microwave circuits are presented.

II. THE YIELD PROBLEM FOR NONLINEAR CIRCUITS

Let $\boldsymbol{\phi}^0$ be the nominal design. Parameters in $\boldsymbol{\phi}^0$ can be lumped element values, device model parameters, and dimensions of a physical realization. Manufactured outcomes are spread over a region which can be described by $\boldsymbol{\phi}^0$ along with statistical distributions of parameters. In yield estimation and statistical circuit design, to simulate the realistic manufacturing environment the circuit outcomes are generated according to the element statistics including possible correlations. A set of N outcomes around $\boldsymbol{\phi}^0$, denoted by $\boldsymbol{\phi}^i$, can be written as

$$\boldsymbol{\phi}^i = \boldsymbol{\phi}^0 + \Delta\boldsymbol{\phi}^i, \qquad i = 1, 2, \ldots, N, \tag{1}$$

where $\Delta\boldsymbol{\phi}^i$ is the deviation of the ith outcome from the nominal circuit and N is the number of outcomes considered. In this paper, we assume that the element statistical properties are known. If there are N statistical outcomes generated, then the production yield can be estimated by

$$Y \approx N_{pass}/N, \tag{2}$$

where N_{pass} is the number of acceptable circuits.

We shall concentrate our attention on nonlinear circuits that are to be simulated by the harmonic balance technique. Typically, multiple design specifications are imposed. For instance, specifications may be applied to various responses for multiple design goals. Additionally, the fundamental frequency may vary to cover a frequency band of interest. More importantly, for nonlinear circuits under consideration, specifications can be imposed on DC levels and/or several different harmonics. Suppose that the fundamental frequency is denoted by f and the corresponding harmonic index vector is

$$\mathbf{h} = [h_0 \quad h_1 \quad h_2 \ \ldots \ h_{N_h}]^T, \tag{3}$$

where N_h is the total number of harmonics. A single specification is imposed on a response relating electrical quantities at different ports. Let the vector of port indices be

$$\mathbf{p} = [p_1 \quad p_2 \ \ldots \ p_{N_p}]^T, \tag{4}$$

where N_p is the number of circuit ports. Now, the set of specifications can be expressed as

$$S(f, \mathbf{h}, \mathbf{p}). \tag{5}$$

The subscripts u and *l* can be introduced to distinguish upper and lower specifications

$$S_u(f, \mathbf{h}, \mathbf{p}), \tag{6a}$$

and

$$S_l(f, \mathbf{h}, \mathbf{p}). \tag{6b}$$

The corresponding set of circuit responses of the *i*th outcome, $\boldsymbol{\phi}^i$, is

$$F(\boldsymbol{\phi}^i, f, \mathbf{h}, \mathbf{p}). \tag{7}$$

For this outcome, we can define error functions comprising components of

$$F(\boldsymbol{\phi}^i, f, \mathbf{h}, \mathbf{p}) - S_u(f, \mathbf{h}, \mathbf{p}) \tag{8a}$$

and/or

$$S_l(f, \mathbf{h}, \mathbf{p}) - F(\boldsymbol{\phi}^i, f, \mathbf{h}, \mathbf{p}). \tag{8b}$$

For convenience we assemble the error functions systematically into vector $\mathbf{e}^i$, defined for the

ith outcome $\boldsymbol{\phi}^i$. If all entries of this vector are nonpositive, the ith outcome $\boldsymbol{\phi}^i$ represents an acceptable circuit.

For amplifier design a typical response of interest is power gain. In this case, **h** may only have one entry which corresponds to the fundamental frequency. If we want to design a frequency doubler with an expected conversion gain, **h** should include the fundamental harmonic at the input and the desired harmonic at the output.

Production yield associated with a particular design can be predicted as follows. (1) For a given nominal design and statistics of elements, generate statistical outcomes. (2) Simulate each outcome. (3) Calculate error functions of responses with respect to the given specifications. (4) Evaluate yield by counting the number of circuits whose error functions are nonpositive.

III. YIELD OPTIMIZATION

Yield optimization is a process where adjustments to element values will be made to increase yield. The problem of yield optimization can be properly converted to a mathematical programming one so that modern mathematical optimization techniques are applicable. In the following the design variables are nominal values $\boldsymbol{\phi}^0$, because $\Delta\boldsymbol{\phi}^i$ is assumed to be related to $\boldsymbol{\phi}^i$ through known statistical relations.

A. Formulation of the Objective Function for Yield Optimization

In the previous section, the error vector $\mathbf{e}^i$ for the ith outcome $\boldsymbol{\phi}^i$ has been defined. Here we rearrange it as

$$\mathbf{e}^i = [e_1(\boldsymbol{\phi}^i) \quad e_2(\boldsymbol{\phi}^i) \ . \ . \ . \ e_M(\boldsymbol{\phi}^i)]^T, \tag{9}$$

where M is the total number of errors considered.

The formulation of the objective function for our yield optimization approach consists of two steps. First, we create the generalized ℓ_1 function v^i to indicate the status of the ith outcome $\boldsymbol{\phi}^i$. The generalized ℓ_1 function v^i can be calculated from $\mathbf{e}^i$ [3] as

$$v^i = \begin{cases} \sum_{j \in J(\phi^i)} e_j(\phi^i), & \text{if } J(\phi^i) \neq \varnothing, \quad (10a) \\ -\left[\sum_{j=1}^{M} (-e_j(\phi^i))^{-1} \right]^{-1}, & \text{if } J(\phi^i) = \varnothing, \quad (10b) \end{cases}$$

where $J(\phi^i) = \{j \mid e_j(\phi^i) \geq 0\}$. In other words, v^i is given by (10a) when at least one of the entries in $\mathbf{e}^i$ is nonnegative, or by (10b) when all the error functions are negative. The sign of v^i actually indicates whether the ith outcome ϕ^i satisfies all specifications.

The one-sided ℓ_1 objective function for yield optimization [3] is defined by

$$U(\phi^0) = \sum_{i \in I} \alpha_i v^i, \quad (11)$$

where $I = \{i \mid v^i > 0\}$ and α_i are properly chosen non-zero multipliers. It is clear that I identifies all outcomes violating at least one specification. Only positive error functions of individual outcomes contribute to the overall objective function. This mechanism of the one-sided ℓ_1 function naturally imitates the fact that only the unacceptable outcomes effect yield. As suggested in [3], if we let

$$\alpha_i = \frac{1}{|\, v^i \,|}, \quad (12)$$

then $U(\phi^0)$ is the exact number of unacceptable circuits. From (2) and (11) we have

$$Y = 1 - U(\phi^0)/N. \quad (13)$$

Thus, the task of maximizing yield Y is converted to one of minimizing $U(\phi^0)$. That is

$$\underset{\phi^0}{\text{minimize}}\ U(\phi^0). \quad (14)$$

In order to construct a well-behaved objective function, we fix the α_i during the optimization process.

Compared with other methods, our method is less dependent on conceptually heuristic assumptions and more capable of handling arbitrary tolerance distributions.

B. The One-Sided ℓ_1 Optimization Algorithm with Gradient Approximations

In the previous section we converted the problem of yield optimization for nonlinear circuits into an abstract optimization problem. We now turn our attention to solving the abstract problem stated in (14). A highly efficient one-sided ℓ_1 optimization algorithm was recently reported in [11]. We use this algorithm to minimize $U(\phi^0)$. This algorithm is a two-stage method combining a first order method with a second order method.

The first order method is the trust region Gauss-Newton method. At the kth iteration, we use ϕ_k^0 to denote the kth iterate of ϕ^0 and v_k^i to denote the generalized ℓ_1 error function for the outcome ϕ_k^i. The local bound, or trust region, is represented by Λ_k. The trust region Gauss-Newton method solves for $\mathbf{r}_k$ the linearized subproblem of (14)

$$\underset{\mathbf{r}_k}{\text{minimize}}\ \overline{U}(\phi_k^0, \mathbf{r}_k) = \sum_{i \in I_k} \alpha_i [v_k^i + (\nabla v_k^i)^T \mathbf{r}_k], \tag{15}$$

$$\text{subject to } \| \mathbf{r}_k \|_\infty \leq \Lambda_k,$$

where $I_k = \{ i \mid \alpha_i [v_k^i + (\nabla v_k^i)^T \mathbf{r}_k] > 0\}$ and ∇v_k^i is the gradient of v_k^i. At the kth iteration, the problem stated by (15) is equivalent to a linear programming problem with the constraint Λ_k on the variables $\mathbf{r}_k$. The trust region, in which the linearized problem is considered as a good approximation to the original nonlinear problem, should be adjusted after each iteration according to the accuracy of the linear approximation. This method is intended to be used to provide the global convergence to a neighbourhood of a solution.

The second method is the quasi-Newton method, which solves a set of optimality equations defined by

$$\sum_{i \in I} \alpha_i \nabla v_k^i + \sum_{i \in Z} \delta_i \alpha_i \nabla v_k^i = 0, \tag{16}$$

where $Z = \{i \mid \alpha_i v_k^i = 0\}$ and δ_i must satisfy $0 \leq \delta_i \leq 1$. Equations of (16) result from applying the Kuhn-Tucker conditions to the one-sided ℓ_1 problem. The quasi-Newton method has fast convergence when a local minimum is approached.

The switch between two methods is automatically made according to the judgment on the convergence behaviour of the problem to best fit the methods.

In (15) and (16), the gradients of individual functions are required. However, analytical gradients are traditionally not produced by general purpose large-scale simulators of nonlinear circuits. They are often approximated by using perturbations. Since gradient evaluations from perturbations are very expensive, especially for our application where multiple circuit outcomes are considered, we employ the flexible and effective gradient approximation method proposed in [12]. This gradient approximation technique incorporates normal (conventional) perturbations, the Broyden update and special iterations. The initial gradient is approximated by applying the normal perturbation. The Broyden update generates the gradient for the $(k + 1)$th iteration from the gradient used in the kth iteration,

$$\nabla v_{k+1}^i = \nabla v_k^i + \frac{v_{k+1}^i - v_k^i - \nabla v_k^{i\,T} r_k}{r_k^T r_k} r_k , \tag{17}$$

where $\mathbf{r}_k$ is the step from $\boldsymbol{\phi}_k^0$ to $\boldsymbol{\phi}_{k+1}^0$. If $\boldsymbol{\phi}_k^0$ and $\boldsymbol{\phi}_{k+1}^0$ are iterates of optimization, the updated gradient can be obtained without additional circuit simulations. To improve gradient approximations, special iterations may be applied to avoid possible convergence difficulties due to a simple use of the Broyden update. Compared with the traditional perturbation method, this gradient approximation algorithm provides excellent accuracy and significant computational savings. In our application, all involved gradient evaluations are associated with outcomes violating specifications. Thus, when a reasonable yield has been reached during optimization, computational effort can be further reduced.

Several successive optimization procedures may be applied to further increase yield. Each of these can use different numbers of statistical outcomes.

IV. SIMULATION OF NONLINEAR CIRCUITS USING HARMONIC BALANCE METHOD

Responses of nonlinear circuits operating in a periodic steady-state regime are calculated by the harmonic balance method [13]. For a given circuit ϕ^i, this method solves the following set of nonlinear algebraic equations

$$\overline{F}(\overline{V}, \phi^i) = \overline{I}_{NL}(\overline{V}, \phi^i_{NL}) + \overline{I}_L(\overline{V}, \phi^i_L) = 0, \tag{18}$$

where the vectors $\overline{I}_{NL}$ and $\overline{I}_L$ represent the currents into the nonlinear and linear subcircuit, respectively, $\overline{V}$ contains the split real and imaginary parts of the voltages on the ports connecting nonlinear and linear subcircuit, and ϕ^i is divided into two parts corresponding to the elements in the nonlinear subcircuit, ϕ^i_{NL}, and the elements in the linear subcircuit, ϕ^i_L. The Newton-type methods are commonly suggested to solve (18).

In statistical design, the circuit simulation accounts for an extremely large portion of the overall computational effort, because of the large number of outcomes simulated individually. To achieve fast convergence and reliable solutions, our program calculates exact Jacobian matrices [13]

$$\overline{J} = \left[\frac{\partial \overline{F}^T}{\partial \overline{V}} \right]^T. \tag{19}$$

V. GENERATION OF STATISTICAL OUTCOMES

There are actually two possible ways to represent statistical properties of circuit elements and devices. One is to use mathematical models which abstract the physical behaviour. The other is to use actual measured data from physical devices. We use the first one in our approach. Mathematical models to characterize statistical distributions of element values must be available before yield optimization. Correlations among elements should also be taken into account, because several equivalent circuit elements may be related to a group of manufacturing/process parameters simultaneously. Hence, the statistical description of a

nonlinear device consists of a model in the form of the equivalent circuit, parameter distributions and correlations among parameters. In either yield estimation or yield optimization, statistical outcomes are generated using an arithmetical algorithm called a random number generator. To reflect the most commonly met statistical distributions, a desirable random number generator is capable of generating outcomes from the independent and multidimensional correlated normal distributions and from uniform distributions.

Purviance et al. [14] treated the statistical characterization of the small-signal FET model. Our proposed yield optimization requires the statistical description of the large-signal FET model, which includes a large-signal model, statistical distributions and correlations of parameters.

Parameters of nonlinear large-signal models have certain physical limits. Within these limits, models are well characterized to simulate actual physical behaviour. It should be noticed that a normal distribution random number generator may generate outcomes far beyond these limits. These outcomes may cause two problems. Firstly, the simulation results of these outcomes are physically meaningless, and therefore mislead optimization. Secondly, unlike the linear circuit case, these outcomes will create extreme difficulties for the nonlinear simulator. Such outcomes must be carefully detected and eliminated during optimization.

VI. THE FREQUENCY DOUBLER EXAMPLE

Consider the FET frequency doubler example shown in Fig. 1 used by Microwave Harmonica [15]. It consists of a common-source FET with a lumped input matching network and a microstrip output matching and filter section. The fundamental frequency is 5GHz. Let the first response be the conversion gain between the input power at fundamental frequency and the output power at the second harmonic, i.e.

$$F_1(\phi, f, \mathbf{h}, \mathbf{p}) = CG(\phi, 5GHz, \mathbf{h}, \mathbf{p})$$

$$= 10\ell og \frac{\text{power of the second harmonic at the output port}}{\text{power of the fundamental frequency at the input port}}.$$

Let the second response be the spectral purity of the output port at the second harmonic, i.e.

$$F_2(\phi, f, \mathbf{h}, \mathbf{p}) = SP(\phi, 5GHz, \mathbf{h}, \mathbf{p})$$

$$= 10\ell og \frac{\text{power of the second harmonic at the output port}}{\text{total power of all other harmonics at the output port}}.$$

The design specifications are 2.5 dB for the conversion gain and 19 dB for the spectral purity. The error functions are

$$e_1(\phi) = 2.5 - CG(\phi, 5GHz, \mathbf{h}, \mathbf{p})$$

and

$$e_2(\phi) = 19 - SP(\phi, 5GHz, \mathbf{h}, \mathbf{p}).$$

The optimization variables include the input inductance L_1 and the microstrip lengths l_1 and l_2. The operating condition of a frequency doubler is essential for its performance. Therefore, two bias voltages V_{GB} and V_{DB} and the driving power level P_{IN} are also considered as optimization variables.

Independent uniform distributions are assumed with fixed tolerances of 3% for P_{IN}, V_{GB}, V_{DB}, L_1, l_1 and l_2. Independent uniform distributions are assumed with fixed tolerances of 5% for L_2, L_3, C_1, C_2, w_1 and w_2. The intrinsic large-signal FET model is the modified Materka and Kacprzak model [15]. Normal distributions are assumed for all FET intrinsic and extrinsic parameters. The standard deviations of these distributions are listed in Table I. The correlation parameters are assumed based on [14]. Certain modifications have been made to adjust the correlations of our large-signal FET model parameters to be consistent with that of the small-signal FET model dealt with in [14]. The correlation coefficients are given in Table II.

The starting point for yield optimization is the solution of the conventional nominal design w.r.t. the same specifications, using L_1, l_1 and l_2 as optimization variables. The initial

yield based on 500 outcomes is 24.8%. This shows that the traditional nominal design cannot give a satisfactory yield.

In the yield optimization, 50 statistically selected outcomes are used. The solution found by our approach improves the yield to 57%. Then another set of 50 outcomes is selected and optimization restarted. After this, the final yield is 61.4%. Computational details are given in Table III. Figs. 2 (a) and (b) show histograms of the conversion gain before and after yield optimization. The improvement is very clearly illustrated by two histograms. Before yield optimization, the center of the distribution is on the left-hand side of the design specification of 2.5 dB, indicating that most outcomes are unacceptable. After yield optimization, the center of the distribution is shifted to the right-hand side of the 2.5 dB specification. Most outcomes then satisfy the specification. The statistical properties of the spectral purity performance are demonstrated by their scattered distributions in Fig. 3 (a) and (b) for 500 outcomes before and after yield optimization, respectively.

VII. A FET AMPLIFIER EXAMPLE

We consider the small-signal amplifier shown in Fig. 4. The conventional design is to optimize the linear elements of the circuit under fixed bias conditions. The effect of bias on the equivalent linear elements representing the nonlinear elements is generally neglected. Such a design has obvious shortcomings. Employing both the DC and fundamental frequency, the harmonic balance method not only solves the small-signal linearized circuit, but also simulates the DC bias condition. We perform a yield optimization allowing the bias voltages to vary during optimization. This enables us to study the effects of operating conditions on performance yield of a linear circuit.

Performance specifications are imposed as $|S_{11}| \leq$ -6dB, $|S_{22}| \leq$ -6dB and 18dB $\leq |S_{21}| \leq$ 20dB. Totally 9 frequency points were selected from the interval of 3.8GHz ~ 4.2GHz. The FET model and statistics used for this example are the same as those used in the doubler

example. The starting point for yield optimization is the solution of conventional nominal design in which two bias voltages are held constant. Estimated yield at this point is 31%.

In yield optimization, besides two bias voltages, the inductor L_1, characteristic impedances and electrical lengths of the transmission line and of the open stubs in the input and output matching networks are also chosen as optimization variables. Independent uniform distributions with 3% tolerances are assumed for V_{GB}, V_{DB}, L_1, Z_1, l_1, Z_2, l_2, Z_3, l_3, C_1, C_2, C_3, C_4, L_2, and L_3.

In the first design, 50 statistical outcomes are used. Each outcome has four error functions and 9 frequency points. This results in 1800 individual functions at a time. The yield at the solution point of this design is 64%. Optimization is restarted with 50 outcomes. Yield is improved to 71%.

After yield optimization the bias voltages, V_{GB} and V_{DB}, have been changed from -0.95 and 4 to -0.9394 and 3.733, respectively. The computational details are listed in Table IV.

Figs. 5 (a) and (b) show response curves of $|S_{11}|$ for 50 statistical outcomes before and after yield optimization, respectively. From Figs. 5 (a) and (b), it can be seen that the dense band at the lower frequency end is pushed towards the specification. This indicates that, after yield optimization, more circuit outcomes satisfy the specification on $|S_{11}|$.

The response distributions of statistical outcomes can also be revealed by the curve of yield versus different specifications. Fig. 6 (a) shows how yield changes with different specifications on either $|S_{11}|$ or $|S_{22}|$ while keeping the remaining specifications fixed. Fig. 6 (b) shows how yield changes with different upper or lower specifications on $|S_{21}|$ while keeping the remaining ones fixed. The steeper a segment of the curve is, the more outcomes fall into the corresponding response interval shown on the horizontal axis.

Fig. 7 vividly illustrates the effects of the bias voltages V_{GB} and V_{DB} on the performance of the circuit. The acceptable region is clearly exposed. Our yield optimized solution is very close to the center of this region.

VIII. CONCLUSIONS

This paper presents a generalized description of yield optimization for nonlinear circuits operating within the harmonic balance simulation environment. The first comprehensive demonstration of yield optimization of statistically characterized nonlinear microwave circuits has been made. Important aspects of our approach have been addressed. The formulation of the objective function for yield optimization has been given. At the core of the optimization process, an advanced one-sided ℓ_1 algorithm with gradient approximations was exploited. The harmonic balance method has been used to efficiently simulate circuits. Generation of statistical outcomes for yield-driven design of nonlinear circuits should allow different statistical distributions and correlations. Large-signal FET parameter statistics are fully facilitated. Comprehensive numerical experiments directed at yield-driven optimization of a FET frequency doubler and a small-signal amplifier verify our approach. Our approach provides a powerful tool to meet the very pressing need for microwave nonlinear circuit design. This success should strongly motivate the development of statistical modeling of microwave devices for large-signal applications.

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REFERENCES

[1] A.J. Strojwas, *Statistical Design of Integrated Circuits*. New York, NY: IEEE Press, 1987.

[2] E. Wehrhahn and R. Spence, "The performance of some design centering methods," *Proc. IEEE Int. Symp. Circuits Syst.* (Montreal, Canada), 1984, pp. 1424-1438.

[3] J.W. Bandler and S.H. Chen, "Circuit optimization: the state of the art," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-36, 1988, pp. 424-443.

[4] S. W. Director and G. D. Hachtel, "The simplicial approximation approach to design centering," *IEEE Trans. Circuits and Systems*, vol. CAS-24, 1977, pp. 363-372.

[5] R. S. Soin and R. Spence, "Statistical exploration approach to design centering," *Proc. Inst. Elec. Eng.*, vol. 127, pt. G., 1980, pp. 260-269.

[6] J.W. Bandler and H.L. Abdel-Malek, "Optimal centering, tolerancing, and yield determination via updated approximations and cuts," *IEEE Trans. Circuits and Systems*, vol. CAS-25, 1978, pp. 853-871.

[7] H.L. Abdel-Malek and J.W. Bandler, "Yield optimization for arbitrary statistical distributions: Part I-theory," *IEEE Trans. Circuits and Systems*, vol. CAS-27, 1980, pp. 245-253.

[8] M. A. Styblinski and A. Ruszczynski, "Stochastic approximation approach to statistical circuit design," *Electron. Lett.*, vol. 19, no. 8, 1980, pp. 300-302.

[9] E. Polak and A. L. Sangiovanni-Vincentelli, "Theoretical and computational aspects of the optimal design centering, tolerancing, and tuning problem," *IEEE Trans. Circuits and Systems*, vol. CAS-26, 1979, pp. 795-813.

[10] K. Singhal and J.F. Pinel, "Statistical design centering and tolerancing using parametric sampling," *IEEE Trans. Circuits and Systems*, vol. CAS-28, 1981, pp. 692-701.

[11] J.W. Bandler, S.H. Chen and K. Madsen, "An algorithm for one-sided ℓ_1 optimization with application to circuit design centering," *IEEE Int. Symp. Circuits Syst.* (Espoo, Finland), 1988, pp. 1795-1798.

[12] J.W. Bandler, S.H. Chen, S. Daijavad and K. Madsen, "Efficient optimization with integrated gradient approximations," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-36, 1988, pp. 444-454.

[13] K.S. Kundert and A. L. Sangiovanni-Vincentelli, "Simulation of nonlinear circuits in the frequency domain," *IEEE Trans. Computer-Aided Design*, vol. CAD-5, 1987, pp. 521-535.

[14] J. Purviance, D. Criss and D. Monteith, "FET model statistics and their effects on design centering and yield prediction for microwave amplifiers," *IEEE Int. Microwave Symp. Dig.* (New York, NY), 1988, pp. 315-318.

[15] *Microwave Harmonica User's Manual*, Compact Software Inc., Paterson, NJ, 07504, 1987.

[16] A. Materka and T. Kacprzak, "Computer calculation of large-signal GaAs FET amplifier characteristics," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-33, 1985, pp. 129-135.

TABLE I

ASSUMED STATISTICAL DISTRIBUTIONS
FOR THE FET PARAMETERS

FET Parameter	Nominal Value	Standard Deviation	FET Parameter	Nominal Value	Standard Deviation
L_G(nH)	0.16	5%	S_I	0.676×10^{-1}	0.65%
R_D(Ω)	2.153	3%	K_G	1.1	0.65%
L_S(nH)	0.07	5%	τ(pS)	7.0	6%
R_S(Ω)	1.144	5%	S_S	1.666×10^{-3}	0.65%
R_{DE}(Ω)	440	14%	I_{G0}(A)	0.713×10^{-5}	3%
C_{DE}(pF)	1.15	3%	α_G	38.46	3%
C_{DS}(pF)	0.12	4.5%	I_{B0}(A)	-0.713×10^{-5}	3%
I_{DSS}(A)	6.0×10^{-2}	5%	α_B	-38.46	3%
V_{p0}(V)	-1.906	0.65%	R_{10}(Ω)	3.5	8%
γ	-15×10^{-2}	0.65%	C_{10}(pF)	0.42	4.16%
E	1.8	0.65%	C_{F0}(pF)	0.02	6.64%

The following parameters are considered as deterministic:
K_E = 0.0, K_R = 1.111, K_1 = 1.282, C_{1S} = 0.0, and K_F = 1.282.
For definitions of the FET parameters, see [16].

TABLE II

FET MODEL PARAMETER CORRELATIONS [14]

	L_G	R_S	L_S	R_{DE}	C_{DS}	g_m	τ	R_{IN}	C_{GS}	C_{GD}
L_G	1.00	-0.16	0.11	-0.22	-0.20	0.15	0.06	0.15	0.25	0.04
R_S	-0.16	1.00	-0.28	0.02	0.06	-0.09	-0.16	0.12	-0.24	0.26
L_S	0.11	-0.28	1.00	0.11	-0.26	0.53	0.41	-0.52	0.78	-0.12
R_{DE}	-0.22	0.02	0.11	1.00	-0.44	0.03	0.04	-0.54	0.02	-0.14
C_{DS}	-0.20	0.06	-0.26	-0.44	1.00	-0.13	-0.14	0.23	-0.24	-0.04
g_m	0.15	-0.09	0.53	0.03	-0.13	1.00	-0.08	-0.26	0.78	0.38
τ	0.06	-0.16	0.41	0.04	-0.14	-0.08	1.00	-0.19	0.27	-0.46
R_{IN}	0.15	0.12	-0.52	-0.54	0.23	-0.26	-0.19	1.00	-0.35	0.05
C_{GS}	0.25	-0.24	0.78	0.02	-0.24	0.78	0.27	-0.35	1.00	0.15
C_{GD}	0.04	0.26	-0.12	-0.14	-0.04	0.38	-0.46	0.05	0.15	1.00

Certain modifications have been made to adjust these small-signal parameter correlations to be consistent with the large-signal FET model.

TABLE III

YIELD OPTIMIZATION
OF THE FET FREQUENCY DOUBLER

Variable Point	Starting Design	Nominal	Solution I	Solution II
P_{IN}(W)	2.0000×10^{-3}*	2.0000×10^{-3}	2.5000×10^{-3}	2.4219×10^{-3}
V_{GB}(V)	-1.9060*	-1.9060	-1.9010	-1.9011
V_{DB}(V)	5.0000*	5.0000	4.9950	4.9949
L_1(nH)	1.0000	5.4620	5.4670	5.4670
l_1(m)	1.0000×10^{-3}	1.4828×10^{-3}	1.6306×10^{-3}	1.7088×10^{-3}
l_2(m)	5.0000×10^{-3}	5.7705×10^{-3}	5.7545×10^{-3}	5.7466×10^{-3}
Yield		24.8%	57.0%	61.4%
No. of Optimization Iterations			11	8
No. of Function Evaluations			41	26

* Not considered as variables in nominal design.

The yield is estimated from 500 outcomes.

TABLE IV

YIELD OPTIMIZATION
OF THE FET SMALL-SIGNAL AMPLIFIER

Variable	Starting Point	Nominal Design	Solution I	Solution II
V_{GB}(V)	-0.9500*	-0.9500	-0.9485	-0.9394
V_{DB}(V)	4.000*	4.000	3.824	3.733
L_1(nH)	*	3.973	4.066	4.086
$Z_1(\Omega)$	50.00	77.15	77.32	77.38
$l_1(°)$	50.00	63.02	63.21	63.27
$Z_2(\Omega)$	50.00	90.76	90.85	90.87
$l_2(°)$	50.00	31.37	31.38	31.36
$Z_3(\Omega)$	50.00	49.45	49.54	49.60
$l_3(°)$	50.00	74.11	74.21	74.30
Yield		31.0%	64.2%	71.4%
No. of Optimization Iterations			17	10
No. of Function Evaluations			72	40

* Not considered as variables in nominal design.

The yield is estimated from 500 outcomes.

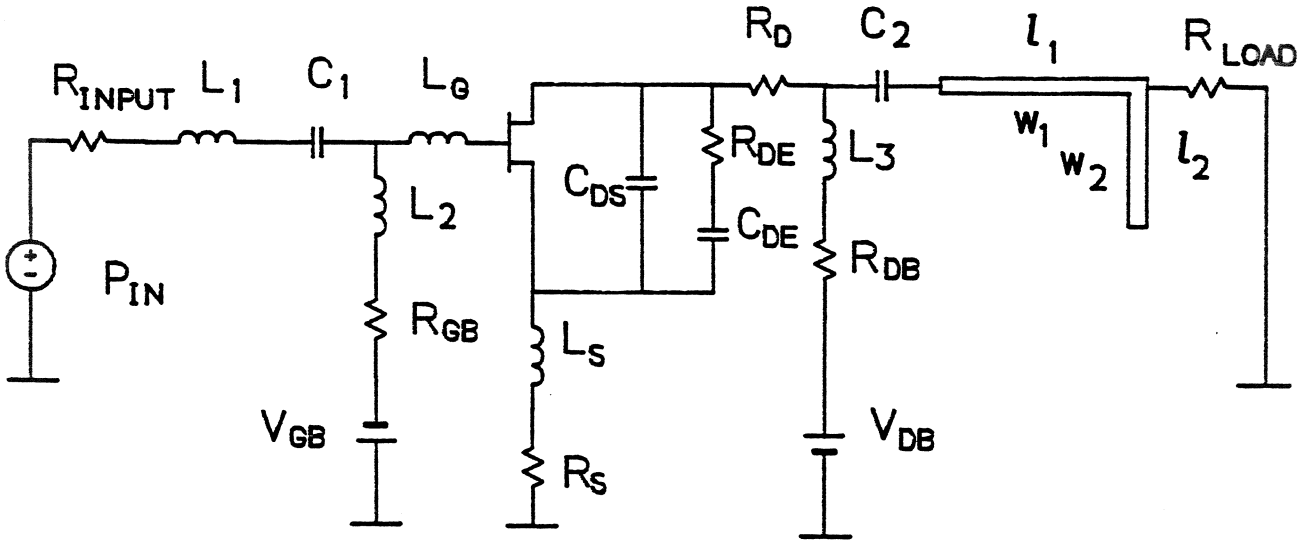
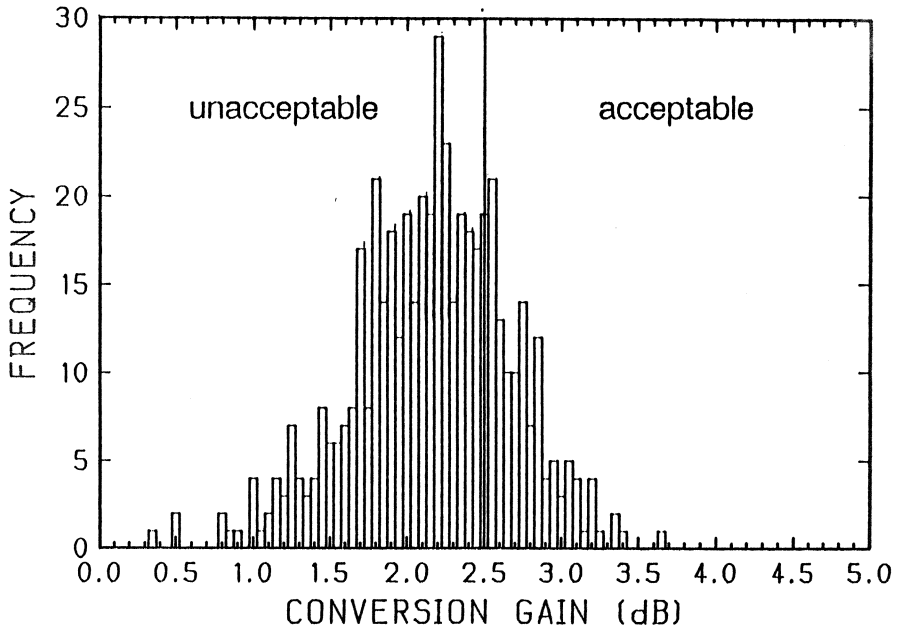
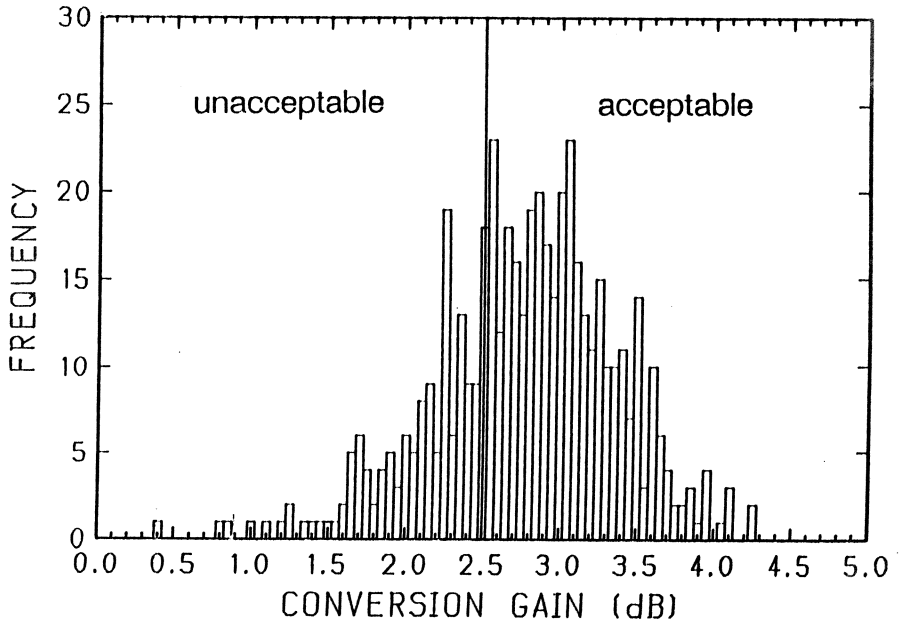


Fig. 1 Circuit diagram of the FET microwave frequency doubler example. The nominal values for non-optimization variables are: L_2 = 15nH, L_3 = 15nH, C_1 = 20pF, C_2 = 20pF, w_1 = 0.1×10^{-3}m, w_2 = 0.635×10^{-3}m, R_{LOAD} = R_{INPUT} = 50Ω, and R_{GB} = R_{DB} = 10Ω.

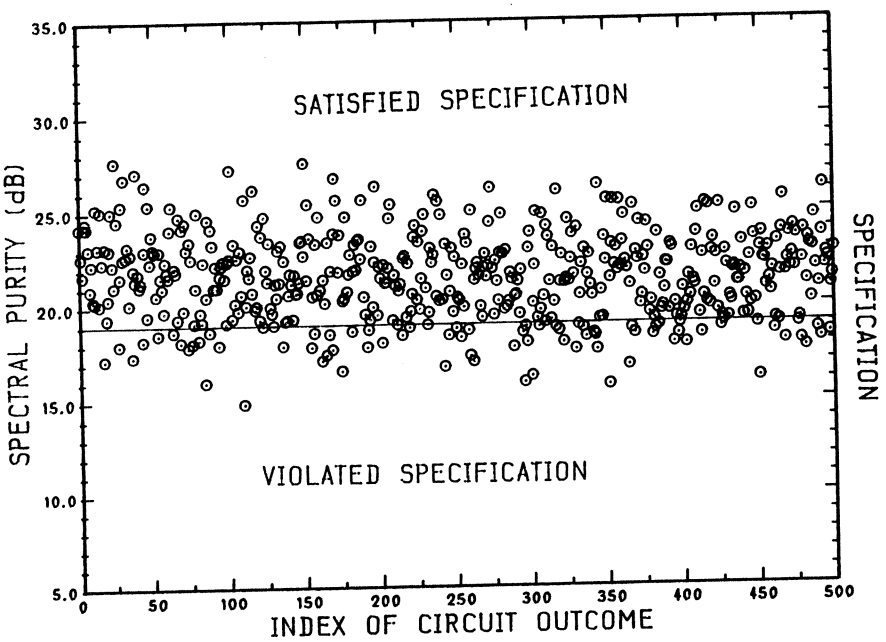


(a)

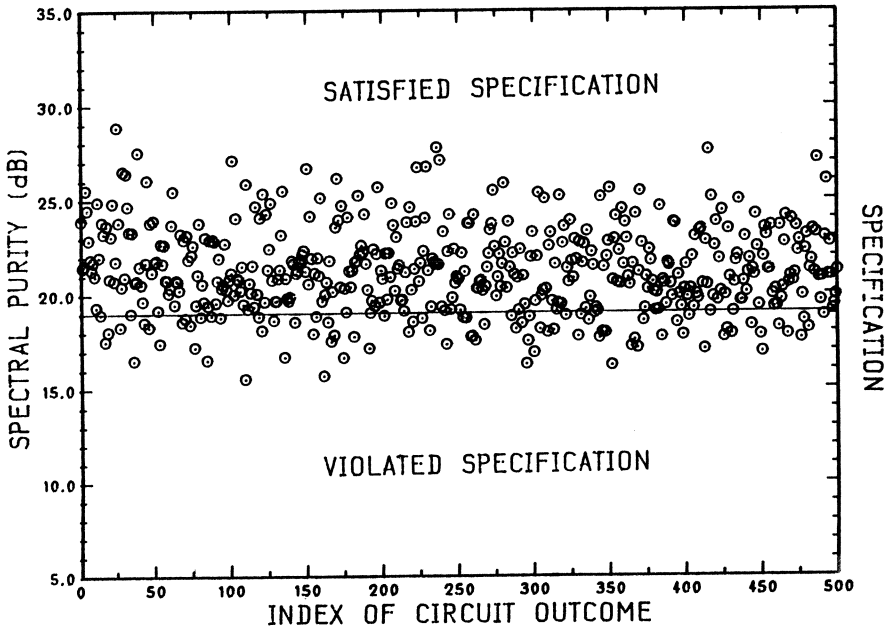


(b)

Fig. 2 Histogram of conversion gains of the frequency doubler based on 500 statistical outcomes, (a) before and (b) after yield optimization. The center of the distribution is moved from the left hand side of the specification shown by a vertical line to the right hand side.



(a)



(b)

Fig. 3 Run charts for spectral purity based on 500 statistical outcomes for the frequency doubler, (a) before and (b) after yield optimization.

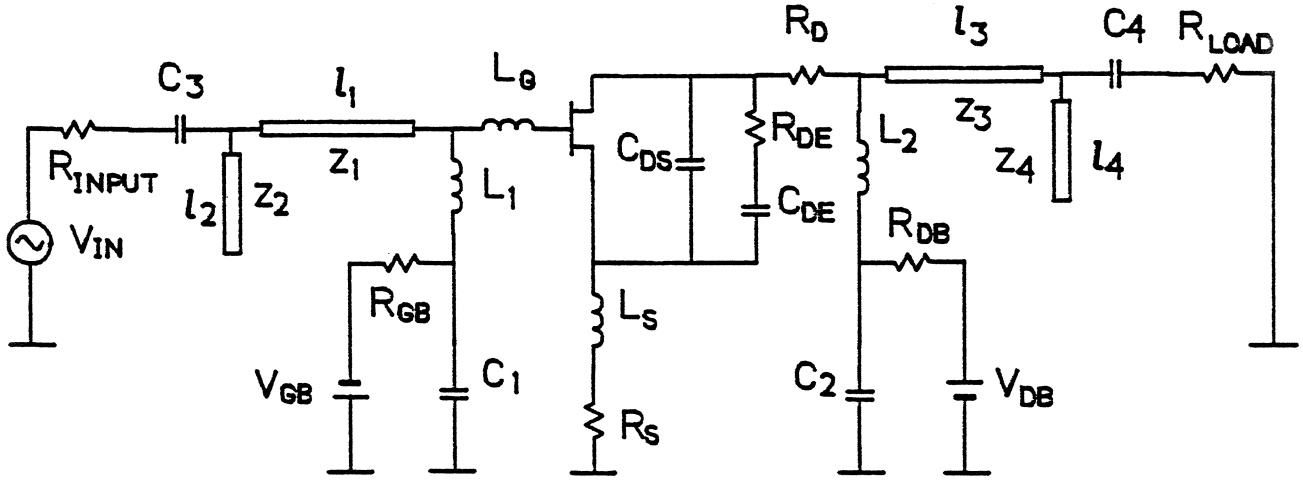
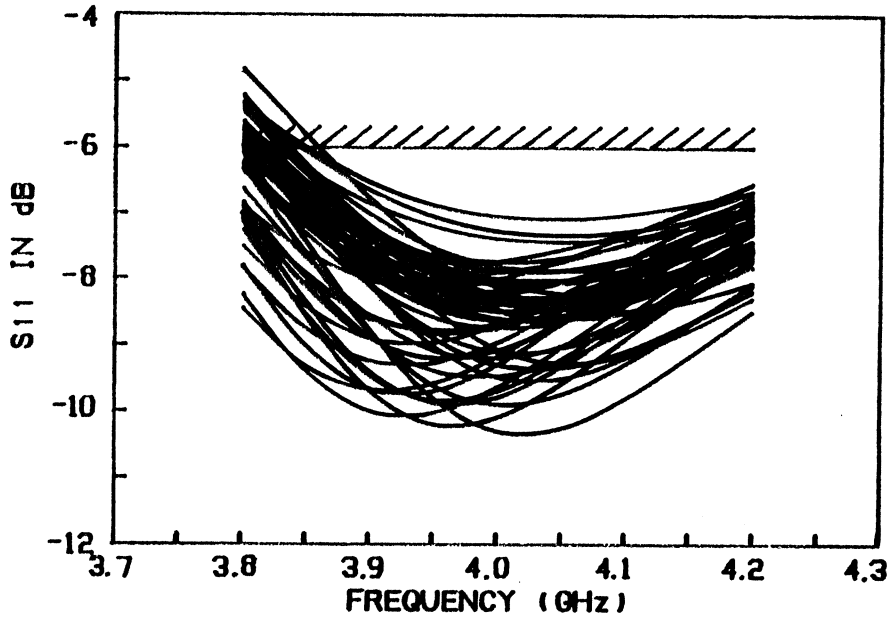
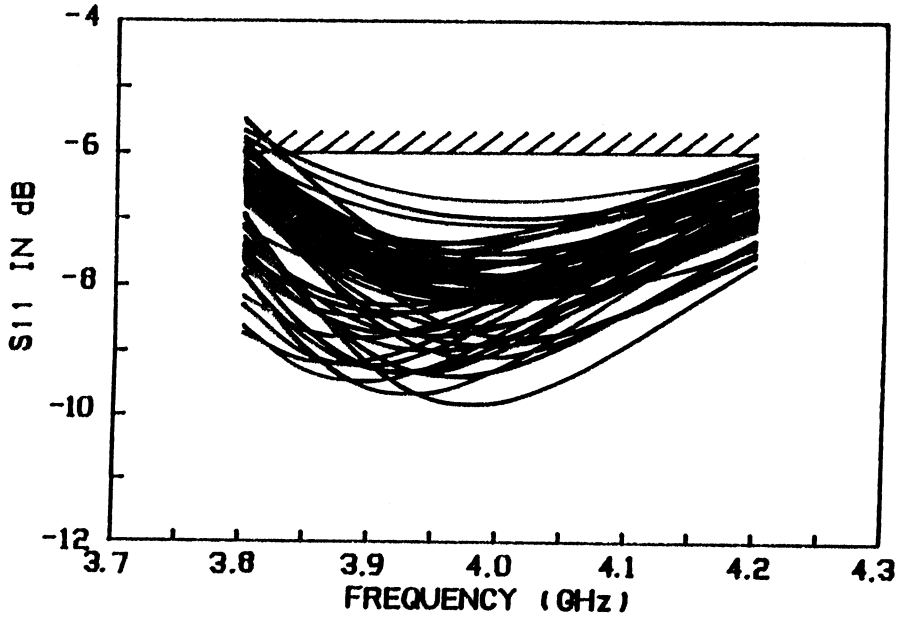


Fig. 4 Circuit diagram of the FET small-signal amplifier example. The nominal values for non-optimization variables are: $C_1 = C_2 = C_3 = 25pF$, $L_2 = L_3 = 100nH$, $R_{LOAD} = R_{INPUT} = 50\Omega$, and $R_{GB} = R_{DB} = 10\Omega$.



(a)



(b)

Fig. 5 Response curves of $|S_{11}|$ for 50 statistical outcomes of the small-signal amplifier, (a) before and (b) after yield optimization.

(a)

(b)

Fig. 6 Yield versus specification curves for the small-signal amplifier. (a) The solid line shows yield variation with different specifications on $|S_{11}|$, the dashed line with different specifications on $|S_{22}|$. (b) The solid line shows yield variation with different upper specifications on $|S_{21}|$, the dashed line with different lower specifications on $|S_{21}|$.

Fig. 7 The effect of bias variation on the performance of the small-signal amplifier. The circuit is simulated for different bias combinations while remaining element values are held at nominal values of the solution. The crosses form the acceptable region and the small dot identifies the solution values of V_{GB} and V_{DB}. The solution of V_{GB} and V_{DB} after optimization is obviously close to the center of the acceptable region.