MODELING, SIMULATION AND OPTIMIZATION OF NONLINEAR MICROWAVE CIRCUITS FOR THE 1990's

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MODELING, SIMULATION AND OPTIMIZATION

OF NONLINEAR MICROWAVE CIRCUITS FOR THE 1990's

This is a collection of three papers to be presented at the 1989 IEEE MTT-S International Microwave Symposium in Long Beach, CA, June 13-15, 1989.

The first paper [1], by Bandler, Zhang, Ye and Chen, addresses a novel technique dedicated to the true large signal nonlinear parameter extraction problem for gallium arsenide MESFET devices.

The second paper [2], by Bandler, Zhang, Song and Biernacki, presents for the first time a comprehensive treatment of yield optimization of nonlinear microwave circuits with statistically characterized devices.

The third paper [3], by Bandler, Zhang and Biernacki, presents a theoretical and computational concept which we feel will replace the traditional perturbation technique for sensitivity evaluation. This method is called FAST.

This collection of works is a significant step in Optimization Systems Associates' continuing penetration into advanced algorithms essential for design of MIC's and MMIC's. OSA's future plans include software exploitation of the techniques described in these papers.

[1] J.W. Bandler, Q.J. Zhang, S. Ye and S.H. Chen, "Efficient large-signal FET parameter extraction using harmonics", IEEE Int. Microwave Symp. (Long Beach, CA, June 1989).

[2] J.W. Bandler, Q.J. Zhang, J. Song and R.M. Biernacki, "Yield optimization of nonlinear circuits with statistically characterized devices", IEEE Int. Microwave Symp. (Long Beach, CA, June 1989).

[3] J.W. Bandler, Q.J. Zhang and R.M. Biernacki, "Practical, high speed gradient computation for harmonic balance simulators", IEEE Int. Microwave Symp. (Long Beach, CA, June 1989).

EFFICIENT LARGE-SIGNAL FET PARAMETER

EXTRACTION USING HARMONICS

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Abstract

We present a novel approach to large-signal nonlinear parameter extraction of GaAs MESFET devices measured under harmonic conditions. Powerful nonlinear adjoint-based optimization simultaneously processes multi-bias, multi-power-input, multi-fundamental-frequency excitations and multi-harmonic measurements to uniquely reveal the parameters of the intrinsic FET. One test successfully processed 111 error functions of 20 model parameters.

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SUMMARY

Introduction

An accurate nonlinear large-signal FET model is critical to nonlinear microwave CAD. Various approaches to FET modeling have been proposed, e.g., [1]-[4]. The dominant nonlinear bias-dependent current source, namely, the drain-to-source current source, in these models is commonly determined by fitting static or dynamic DC I-V characteristics only [1, 2, 4, 5, 6], or by matching DC characteristics and small-signal S-parameters simultaneously [3]. Other nonlinear elements in the model are either determined by applying special DC biases so as to determine the parameters of the gate-to-source nonlinear current source in the Materka and Kacprzak model [2], or by using small-signal S-parameters.

The FET models obtained by these methods may provide accurate results under DC and/or small-signal conditions. They may not, however, be accurate enough for high-frequency large-signal applications [7], since they are determined under small-signal conditions and then used to predict the behaviour for large-signal operation.

For the first time, a truly nonlinear large-signal FET parameter extraction procedure is proposed which utilizes spectrum measurements, including DC bias information and power output at different harmonics under practical working conditions [8]. The harmonic balance method [9] is employed for fast nonlinear frequency domain simulation in conjunction with ℓ_1 and ℓ_2 optimization for extracting the parameters of the nonlinear elements in the large-signal FET model.

Numerical experiments have shown that all the parameters can be uniquely identified under actual high-frequency large-signal working conditions, demonstrating the importance of higher harmonics in large-signal parameter extraction. In addition, powerful nonlinear adjoint analysis for sensitivity computation [10] has been implemented with attendant advantages in computation time.

Formulation

Nonlinear intrinsic FET parameters are to be determined using large signal data. All linear FET model elements such as parasitics are extracted using small-signal data.

The FET and its measurement environment are shown in Fig. 1, where Y_{in} and Y_{out} are input and output 2-ports, Y_g and Y_d are gate and drain bias 2-ports, respectively. We apply a large signal power input P_{in} to the circuit. DC voltages and output power P_{out} at several harmonics [8] are measured.

In addition to the multi-bias, multi-frequency concept we pioneered for small-signal parameter extraction, we allow the circuit to be excited at several input power levels. Various combinations of bias points, fundamental frequencies and input levels result in a variety of measurement information needed for parameter extraction. Assume for the *j*th bias-input-frequency combination, j=1, 2, ... M, the measurement is

$$S_j = [S_j(0) \quad S_j(\omega_1) \quad S_j(\omega_2) \quad \dots \quad S_j(\omega_H)]^T, \tag{1}$$

where $S_j(0)$ is the DC component of the measurement, and $S_j(\omega_k)$, k=1, ..., H, are the *k*th harmonic components. Correspondingly, the model response $\mathbf{F}_j(\boldsymbol{\phi})$ can be expressed as

$$\mathbf{F}_j(\boldsymbol{\phi}) = [F_j(\boldsymbol{\phi},0) \quad F_j(\boldsymbol{\phi},\omega_1) \quad F_j(\boldsymbol{\phi},\omega_2) \quad \dots \quad F_j(\boldsymbol{\phi},\omega_H)]^T, \tag{2}$$

where $\boldsymbol{\phi}$ stands for the parameters of the model to be determined.

The parameter extraction optimization problem can then be formulated as

$$\min_{\boldsymbol{\phi}} \sum_{j=1}^{M} \left(w_{jdc} \left| F_j(\boldsymbol{\phi},0) - S_j(0) \right|^p + \sum_{k=1}^{H} w_{jk} \left| F_j(\boldsymbol{\phi},\omega_k) - S_j(\omega_k) \right|^p \right), \tag{3}$$

where w_{jdc} and w_{jk} are weighting factors, and p=1 or 2 corresponds to ℓ_1 or ℓ_2 optimization, respectively.

Model responses $F_j(\phi)$ are computed using the harmonic balance method [9]. The powerful nonlinear adjoint sensitivity analysis [10] is implemented to provide gradients for optimization. This significantly accelerates the optimization and makes our parameter extraction approach computationally practical.

An automatic weight assignment algorithm has been developed, improving robustness and enhancing convergence speed. Also, by converting measured powers to voltages, we achieve a well-conditioned optimization problem.

The FET Model Used in Our Experiment

In our numerical experiments, we used the Microwave Harmonica [11] modified Materka and Kacprzak FET model as the intrinsic FET, as shown in Fig. 2. The nonlinear elements of the model are described by [11]

$$i_D = F[v_G(t - \tau), v_D(t)] \left(1 + S_S \frac{v_D}{I_{DSS}}\right),$$

$$F(v_G, v_D) = I_{DSS} \left(1 - \frac{v_G}{V_{p0} + \gamma v_D}\right)^{(E + K_E v_G)} \cdot \tanh\left(\frac{S_1 v_D}{I_{DSS}(1 - K_G v_G)}\right),$$

$$i_G = I_{G0} [\exp(\alpha_G v_G) - 1],$$

$$i_B = I_{B0} \exp[\alpha_B(v_D - v_1 - V_{BC})], \qquad (4)$$

$$\begin{cases} R_1 = R_{10}(1 - K_R v_G), \\ R_1 = 0, \quad \text{if } K_R v_G \geq 1, \end{cases}$$

$$\begin{cases} C_1 = C_{10}(1 - K_1 v_G)^{-1/2} + C_{1S}, \\ C_1 = C_{10}\sqrt{5} + C_{1S}, \quad \text{if } K_1 v_G \geq 0.8, \end{cases}$$

and

$$\begin{cases} C_F = C_{F0}[1 - K_F(v_1 - v_D)]^{-1/2}, \\ C_F = C_{F0}\sqrt{5}, \quad \text{if } K_F(v_1 - v_D) \geq 0.8, \end{cases}$$

where I_{DSS}, V_{P0}, γ, E, K_E, S_1, K_G, τ, S_S, I_{G0}, α_G, I_{B0}, α_B, V_{BC}, R_{10}, K_R, C_{10}, K_1, C_{1S}, C_{F0}, and K_F are the parameters to be determined. Since only one of I_{B0} and V_{BC} is independent, we fix V_{BC} and let

$$\phi = [I_{DSS}\ V_{P0}\ \gamma\ E\ K_E\ S_1\ K_G\ \tau\ S_s\ I_{G0}\ \alpha_G\ I_{B0}\ \alpha_B\ R_{10}\ K_R$$
$$C_{10}\ K_1\ C_{1S}\ C_{F0}\ K_F]^T. \quad (5)$$

The parasitics of the FET are illustrated in Fig. 1 and their values are listed in Table I [3].

Test 1: Robustness of the Parameter Extraction Approach

Assume that the solution of the model is [3]

$$\phi = [0.1888\ \ -4.3453\ \ -0.3958\ \ 2\ \ 0\ \ 0.0972\ \ -0.1678\ \ 3.654\ \ 0\ \ 0.5\times10^{-9}\ \ 20$$
$$0.5\times10^{-9}\ \ 1\ \ 4.4302\ \ 0\ \ 0.6137\ \ 0.7686\ \ 0\ \ 0.0416\ \ 0]^T. \quad (6)$$

The circuit is simulated at three bias points: (V_{GB}=0, V_{DB}=5), (V_{GB}=−1.5, V_{DB}=5) and (V_{GB}=−3, V_{DB}=5). P_{in}=5 and 10dBm are applied at (V_{GB}=0, V_{DB}=5), and P_{in}=5, 10 and 15dBm at the other two bias points, respectively. At each bias point two fundamental frequencies (1 and 2GHz) are used, respectively. There are 16 bias-input-frequency combinations in total. Six harmonics are considered in the harmonic balance simulation. The output power at the first 3 harmonics are measured and used in the objective function, i.e., H=3 in (3). Therefore we have 20 variables and 64 error functions.

To examine uniqueness of the solution we uniformly perturbed the solution in (6) by 20 to 40 percent, and re-optimized with the ℓ_1 norm, i.e., p=1 in (3). Several starting points were tested and all of them converged to the known solution exactly. This verifies the strong identifiability induced by the higher harmonics.

Table II demonstrates the significance of the nonlinear adjoint sensitivity analysis, where we compare the CPU execution time for two different starting points with and without nonlinear adjoint analysis for gradient computation. With the adjoint analysis, the program runs approximately 10 times faster than that without adjoint analysis.

Test 2: Parameter Extraction with Measurement Errors

In this test, we added 10% normally distributed random noise to the simulated measurements used in Test 1. We used the same bias-input-frequency combinations and the same starting points as those in Test 1. We applied ℓ_2 optimization, i.e., p=2 in (3). Measurements at the first 4 harmonics are used, i.e., H=4 in (3). Any signal below -35dBm was discarded. After optimization, all points converged to virtually one solution quite close to (6) except for I_{B0} and α_B because of their relatively low sensitivities to the response functions. Still, I_{B0} and α_B converged to their respective order.

Test 3: Fitting to the Curtice Model

Here we use set of data generated by the Curtice model [4,11]. The circuit is similar to that of Fig. 1 except that the intrinsic FET is replaced by the intrinsic part of the Curtice model. Some of the parameters of the Curtice model are taken from Fig. 13 of [4]. See Table III.

We selected 32 bias-input-frequency combinations, as shown in Table IV. The first 3 harmonics were assumed as measurement data. Any signal below -30dBm was discarded. There were 111 error functions in total.

ℓ_2 optimization was applied to extract the model parameters, resulting in

$$\phi = [0.05208\ -1.267\ -0.08774\ 1.269\ -0.3224\ 0.07312\ -0.6482\ 5.322\ 4.462\times10^{-5}\ 8.782\times10^{-9}\ 34.04\ 5.96\times10^{-12}\ 4.245\ 0.03610\ 9.892\times10^{-3}\ 1.066\ 1.531\ 0.03141\ 1.321\ 1.638]^T.$$

Fig. 3 illustrates the modeling results at a bias point other than those considered in the optimization. Excellent agreement is observed.

As for Test 1, parameters at the solution were perturbed uniformly by 20 to 40 percent and re-optimized. Of six starting points, four converged to the same solution with little variances in R_{10} and K_R. The other two converged to different points with different final objective function values.

Fig. 4 shows the characteristics of drain-to-source nonlinear current sources of the Curtice model and the modified Materka and Kacprzak model, and again we have reached an excellent match. Notice that only 6 bias points are used in the optimization which is even less than the total number of parameters for this current source. However, since we modeled under actual large-signal conditions, employing higher harmonic measurements, a much larger range of information has been covered than single individual points on the DC I-V curve can provide.

Conclusions

In this paper an accurate and truly nonlinear large-signal parameter extraction approach has been presented, where not only DC bias and fundamental frequency, but also higher harmonic responses have been used. Such information effectively reflects the nonlinearities of the model. The harmonic balance method for nonlinear circuit simulation, adjoint analysis for nonlinear circuit sensitivity calculation and optimization methods have been applied. Numerical results demonstrate that the method can uniquely and efficiently determine the parameters of the nonlinear elements of the GaAs MESFET model under actual large-signal operating conditions.

Consideration of the parameter extraction problem under two-tone measurements is planned.

Acknowledgements

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TABLE I

LINEAR PARASITIC PARAMETER VALUES OF THE FET MODEL (FIG. 1) USED IN ALL NUMERICAL TESTS

Parameter	Value	Unit
R_g	0.0119	Ω
L_g	0.1257	nH
R_s	0.3740	Ω
L_s	0.0107	nH
R_d	0.0006	Ω
L_d	0.0719	nH
C_{ds}	0.1927	pF
R_{de}	440	Ω
C_{de}	1.5	pF

TABLE II

CPU TIME WITH AND WITHOUT NONLINEAR ADJOINT GRADIENT CALCULATIONS IN TEST 1

	Without Adjoint Ana.*		With Adjoint Ana.	
	CPU** (sec.)	Obj. fun. value	CPU** (sec.)	Obj. fun. value
Starting point 1	1800	1.158×10^{-3}	230	1.013×10^{-3}
	2600	2.235×10^{-4}	260	1.734×10^{-4}
Starting point 2	2600	1.366×10^{-3}	200	1.115×10^{-3}
	2900	5.479×10^{-4}	220	4.894×10^{-4}

* The gradient is estimated by perturbations at every other iteration.
** Fortran program run on a VAX 8650.

TABLE III

PARAMETERS OF THE CURTICE MODEL USED IN TEST 3

Parameter	Value	Unit
β_2	0.04062	1/V
A_0	0.05185	A
A_1	0.04036	A/V
A_2	-0.009478	A/V^2
A_3	-0.009058	A/V^3
γ	1.608	1/V
V_{DS0}	4.0	V
I_S	1.05×10^{-9}	A
N	1.0	-
C_{GS0}	1.1	pF
C_{GD0}	1.25	pF
F_C	0.5	-
G_{MIN}	0.0	$1/\Omega$
V_{BI}	0.7	V
V_{BR}	20	V
τ	5.0	ps
see [4] and [11]		

TABLE IV

INPUT LEVELS USED WITH DIFFERENT FUNDAMENTAL FREQUENCIES AND DIFFERENT BIASES IN TEST 3

(V_{GB}, V_{DB})	P_{in} (dBm)			
	f_1=0.5GHZ	f_1=1.0GHZ	f_1=1.5GHZ	f_1=2.0GHZ
(-0.3, 3)	0, 4	0, 4	0, 4	0, 4
(-0.3, 7)	0, 4	0, 4	0, 4	0, 4
(-1.0, 3)	0	0	0	0
(-1.0, 7)	0	0, 4	0, 4	0
(-0.5, 3)	--	8	8	--
(-0.5, 7)	8	8	8	8

f_1 denotes the fundamental frequency

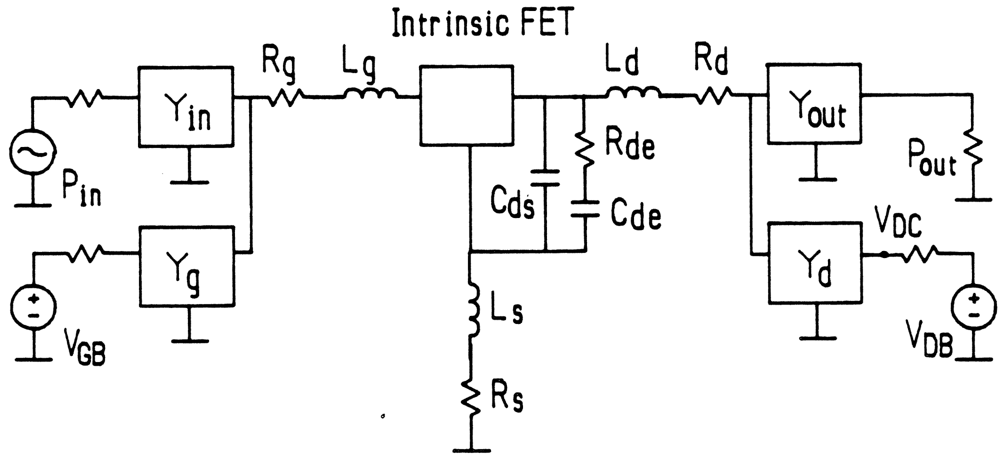

Fig. 1 Circuit setup for large-signal multi-harmonic FET measurement.

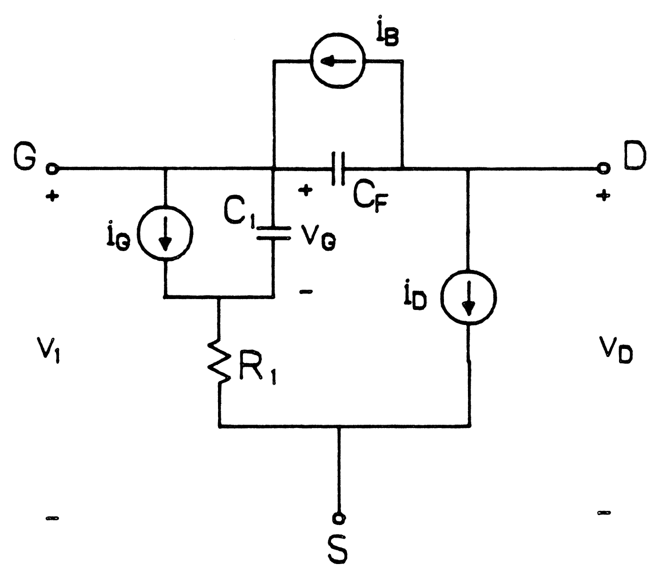

Fig. 2 Intrinsic part of the modified Materka and Kacprzak FET model.

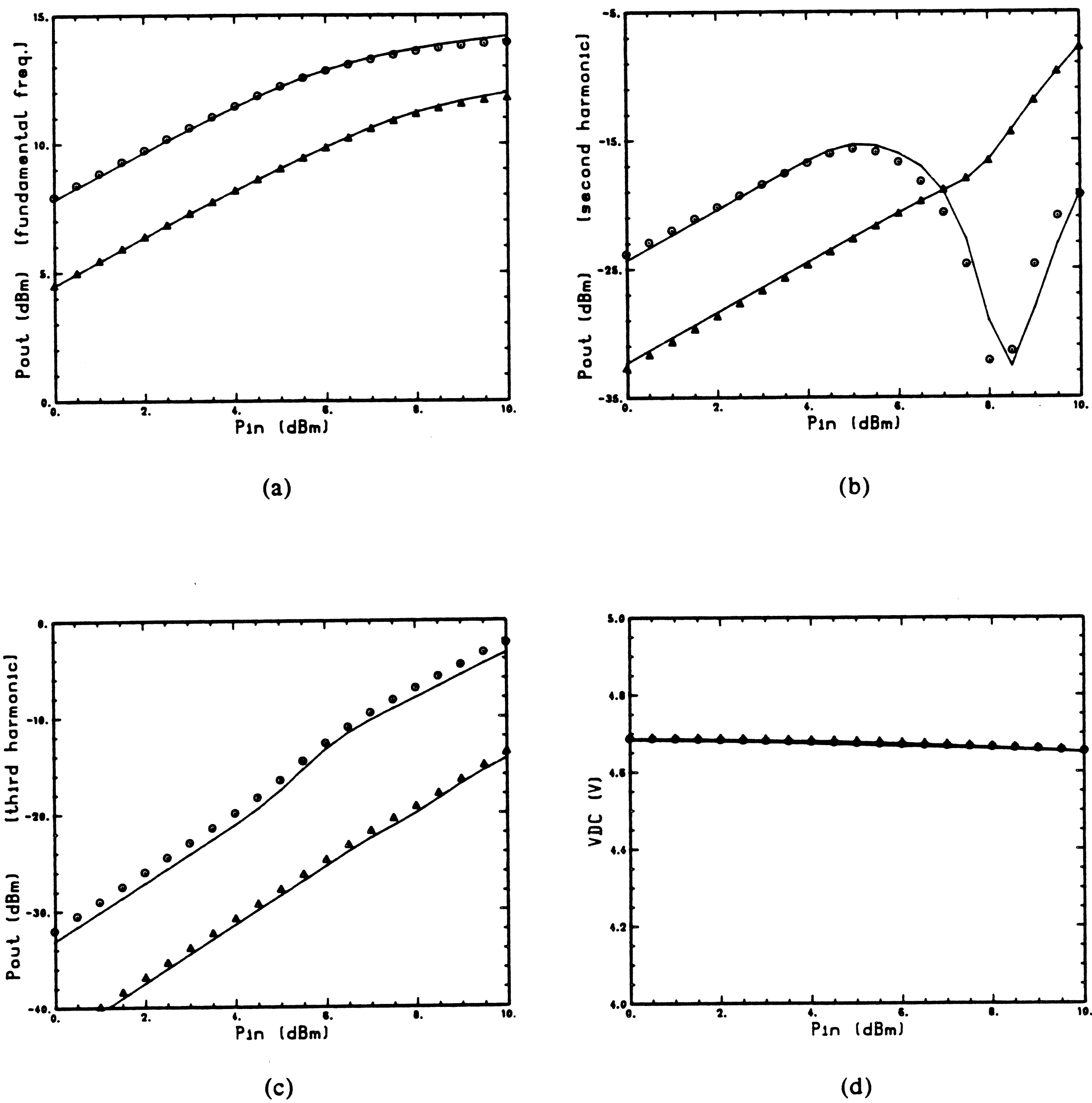

Fig. 3 Agreement between the (Materka) model response and the simulated measurements (using the Curtice model) at V_{GB}=-0.5 and V_{DB}=5 in Test 3. Solid lines represent the (Materka) computed model response. Circles denote the simulated measurements at fundamental frequency 0.5GHZ and triangles the simulated measurements at fundamental frequency 1.0GHZ. (a) Fundamental component, (b) second harmonic component, (c) third harmonic component, and (d) DC component.

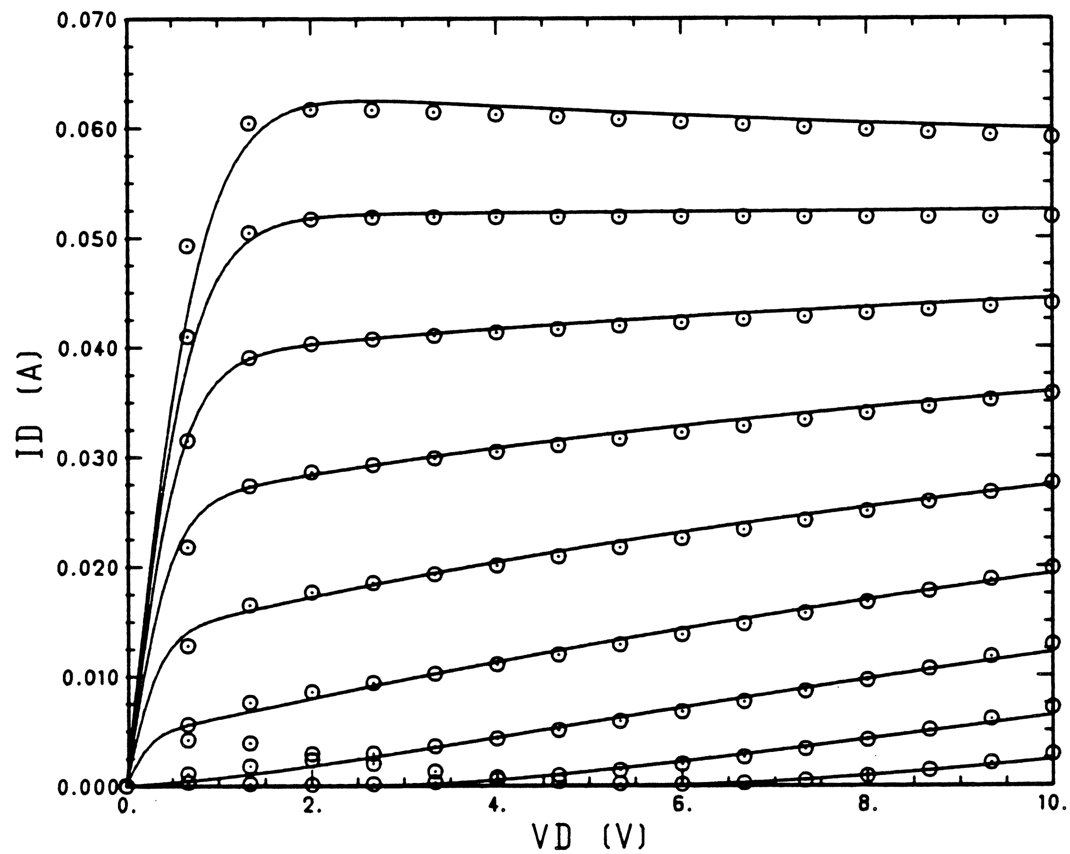

Fig. 4 Agreement between the DC characteristics of the modified Materka and Kacprzak model and the simulated measurements (from the Curtice model) in Test 3. V_G is from -1.75V to 0.25V in steps of 0.25V, and V_D is from 0 to 10V. (Curtice uses V_{in} and V_{out}, respectively.) Solid lines represent the (Materka) model, and the circles represent the measurements.

YIELD OPTIMIZATION
OF NONLINEAR CIRCUITS WITH
STATISTICALLY CHARACTERIZED DEVICES

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Abstract

A comprehensive treatment of yield optimization of nonlinear microwave circuits with statistically characterized devices is proposed. We fully exploit advanced techniques of one-sided ℓ_1 circuit centering with gradient approximations, and efficient harmonic balance simulation with exact Jacobians. Multidimensional statistical distributions of the intrinsic and parasitic parameters of FETs are fully handled. Yield is driven from 25% to 61% for a frequency doubler design having 34 statistically toleranced parameters.

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SUMMARY

Introduction

Yield optimization [1,2] has been extensively explored in the literature. For linear circuits, it is currently finding its way into commercial microwave CAD software. Yield optimization of practical nonlinear microwave circuits remains unaddressed hitherto.

Requirements essential to yield optimization of nonlinear microwave circuits are: (1) effective approaches to design centering, (2) highly efficient optimization techniques, (3) fast and reliable simulation, (4) flexibility of handling various statistical representations of devices and elements, and (5) low design costs and short design cycles.

In this paper, we offer an approach for efficient yield-driven optimization of nonlinear microwave circuits with statistically characterized devices. The formulation of the yield problem for nonlinear circuits is described. A very powerful and robust one-sided ℓ_1 optimization algorithm for design centering recently proposed by Bandler et al. [3] is adopted. An effective gradient approximation technique presented by Bandler et al. [4] is integrated with the one-sided ℓ_1 algorithm to handle inexact gradients. The harmonic balance method is implemented with exact Jacobian matrices for fast convergence and improved robustness. Independent and/or correlated normal distributions and uniform distributions describing large-signal FET model parameters and passive elements are fully accommodated.

Modern supercomputers have found applications in microwave CAD [5, 6] with attractive performance-to-cost ratios. Our software has been developed for possible use on supercomputers. The computational performance on the Cray X-MP/44 will be reported in the full paper.

The yield optimization of a microwave frequency doubler with a large-signal statistically simulated FET model is successfully carried out. The performance yield was increased from 25% to 61%.

We believe that this is the first demonstration of yield optimization of nonlinear

circuits operating under large-signal steady-state periodic or almost periodic conditions.

Formulation of the Yield Problem for Nonlinear Circuits

In yield estimation and statistical circuit design, a set of outcomes around the given nominal design ϕ^0 is considered. These outcomes are sampled according to the element statistics including possible correlations and are denoted by ϕ^i, i = 1, 2, ... , N.

Suppose that the number of harmonics considered in simulation is H. Specifications are given at the DC level and/or several harmonics. Suppose that specifications are applied to circuit responses at the *k*th harmonic. The set of specifications and the corresponding set of calculated response functions of the outcome, ϕ^i, are denoted by

$$S_j(k), \quad 0 \leq k \leq H, \quad j = 1, 2, ..., M \tag{1}$$

and

$$F_j(\phi^i, k), \qquad 0 \leq k \leq H, \quad j = 1, 2, ..., M, \tag{2}$$

where M is the number of specifications. The error functions for the *i*th outcome, $e(\phi^i)$, comprise the entries

$$F_j(\phi^i, k) - S_{uj}(k), \tag{3}$$

and/or

$$S_{lj}(k) - F_j(\phi^i, k), \tag{4}$$

where $S_{uj}(k)$ and $S_{lj}(k)$ are upper and lower specifications. More than one harmonic index can be introduced to these functions to cope with responses such as conversion gain or power added efficiency, etc.

An outcome ϕ^i represents an acceptable circuit if all entries in $e(\phi^i)$ are negative. Yield can be estimated by

$$Y \approx N_{pass}/N, \tag{5}$$

where N_{pass} is the number of acceptable circuits and N is the total number of circuit outcomes.

Yield Optimization

The formulation of the objective function for our yield optimization approach consists of two steps. First, the generalized ℓ_1 function $v(e(\phi^i))$ can be calculated from $e(\phi^i)$. Then, the one-sided ℓ_1 objective function for yield optimization [3] is defined by

$$u(\phi^0) = \sum_{i \in J} \alpha_i v(e(\phi^i)), \tag{6}$$

where $J = \{i \mid v(e(\phi^i)) > 0, i = 1, 2, ..., N\}$ and α_i are properly chosen non-zero multipliers. Only positive error functions of individual outcomes contribute to the overall objective function. The highly efficient optimization algorithm of [3] is used to minimize $u(\phi^0)$, achieving a centered design with improved yield.

Since the one-sided ℓ_1 algorithm requires gradients, the flexible and effective gradient approximation algorithm proposed in [4] is modified here to address the fact that analytical gradients are traditionally not produced by general purpose large-scale simulators of nonlinear circuits.

Harmonic Balance Method as Simulation Tool

Responses of nonlinear circuits operating in a periodic steady-state regime are calculated by the harmonic balance method. In statistical design, the circuit simulation accounts for an extremely large portion of the overall computational effort, because of the large number of outcomes simulated individually. The notable difference between linear and nonlinear simulations is that the harmonic balance method is an iterative process. To achieve fast convergence and reliable solutions, our program calculates exact Jacobian matrices.

Statistical Outcomes

Purviance et. al. [7] treated the statistical characterization of small-signal FET models. Our proposed yield optimization requires statistically described large-signal FET models. We use a random number generator capable of generating statistical outcomes from the independent and multidimensional correlated normal distributions and from uniform distributions.

Unlike linear FET models, the nonlinear large-signal models employed are valid only in certain regions. A normal distribution random generator may generate outcomes far beyond the valid region. Such outcomes must be carefully detected and eliminated.

A FET Frequency Doubler Example

Consider the FET frequency doubler example (Fig. 1) used by Microwave Harmonica [8]. It consists of a common-source FET with a lumped input matching network and a microstrip output matching and filter section. The fundamental frequency is 5GHz. Let $CG(\phi,2,1)$ be the conversion gain between input port at fundamental frequency and the output port at the second harmonic. Let $SP(\phi,2)$ be the spectral purity of the output port at the second harmonic. The design specifications are 2.5 dB for the conversion gain and 19 dB for the spectral purity. The error functions are

$$e_1(\phi) = 2.5 - CG(\phi,2,1)$$

and

$$e_2(\phi) = 19 - SP(\phi,2).$$

The optimization variables include the input inductance L_1 and the microstrip lengths l_1 and l_2. The operating condition of a frequency doubler is essential for its performance. Therefore, two bias voltages, V_{GB} and V_{DB}, and the driving power level, P_{IN} are also considered as optimization variables.

The intrinsic large-signal FET model is the modified Materka and Kacprzak model [8]. The model is shown in Fig. 2. Independent uniform distributions with fixed tolerances of 3% are assumed for all design variables. Normal distributions are assumed for all FET intrinsic and extrinsic parameters. The standard deviations of these distributions are listed in Table I. The statistical correlations of the nonlinear intrinsic FET are based on [7]. The assumed correlation parameters are shown in Table II.

The starting point for yield optimization is the solution of the conventional nominal design w.r.t. the same specifications, using L_1, l_1 and l_2 as optimization variables. The initial yield based on 500 outcomes is 24.8%. 50 statistically selected outcomes were used in the yield optimization process. The solution found by our approach improves the yield to

57%. Then another set of 50 outcomes was selected and optimization restarted. After this, the final yield was 61.4%. Computational details are given in Table III.

Run charts for the conversion gain and the spectral purity before and after yield optimization are shown in Figs. 3, 4, 5 and 6, respectively. The statistical properties of these two responses can be seen from the run charts. Figs. 7 and 8 show histograms of the conversion gain before and after yield optimization. Before yield optimization, the center of the distribution is on the left-hand side of the design specification of 2.5 dB, indicating that most outcomes are unacceptable. After yield optimization, the center of the distribution is shifted to the right-hand side of the 2.5 dB specification. Most outcomes then satisfy the specifications.

A FET Amplifier Example

By considering the DC and fundamental frequency, the harmonic balance method not only solves the small-signal linearized circuit, but also simulates the DC bias condition. We have exploited this in the design of a FET amplifier.

Performance specifications were imposed on small-signal S-parameter responses. The modified Materka and Kacprzak large-signal FET model [9] was used. We performed a yield optimization allowing the bias voltages to vary during optimization. This enables us to study the effects of operating conditions on performance yield of a linear circuit.

Conclusions

The first comprehensive demonstration of yield optimization of statistically characterized nonlinear microwave circuits operating within the harmonic balance simulation environment has been made. Advanced one-sided ℓ_1 design centering combined with efficient harmonic balance simulation using exact Jacobians are exploited. Large-signal FET parameter statistics are fully facilitated. Comprehensive numerical experiments directed at yield-driven optimization of a FET frequency doubler support our confidence. It lends significant credence to the necessity of statistical modeling of nonlinear microwave devices for large-signal applications.

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TABLE I

ASSUMED STATISTICAL DISTRIBUTIONS FOR THE FREQUENCY DOUBLER

Element and FET Parameter	Nominal Value	Type of Distribution	Relative Tolerance or Standard Deviation
V_{GB}	optimized	uniform	3%
V_{DB}	optimized	uniform	3%
P_{IN}	optimized	uniform	3%
l_1	optimized	uniform	3%
l_2	optimized	uniform	3%
L_1	optimized	uniform	3%
L_2	15nH	uniform	5%
L_3	15nH	uniform	5%
C_1	20pF	uniform	5%
C_2	20pF	uniform	5%
w_1	0.1×10^{-3}m	uniform	5%
w_2	0.635×10^{-3}m	uniform	5%
L_G	0.16nH	normal	5%
R_D	2.153Ω	normal	3%
L_S	0.07nH	normal	5%
R_S	1.144Ω	normal	5%
R_{DE}	440Ω	normal	14%
C_{DE}	1.15pF	normal	3%
C_{DS}	0.12pF	normal	4.5%
I_{DSS}	6.0×10^{-2}	normal	5%
V_{p0}	-1.906	normal	0.65%
γ	$-15.\times10^{-2}$	normal	0.65%
E	1.8	normal	0.65%
S_l	0.676×10^{-1}	normal	0.65%
K_G	1.1	normal	0.65%
τ	7.0pS	normal	6%
S_S	1.666×10^{-3}	normal	0.65%
I_{G0}	0.713×10^{-5}	normal	3%
α_G	38.46	normal	3%
I_{B0}	-0.713×10^{-5}	normal	3%
α_B	-38.46	normal	3%
R_{10}	3.5Ω	normal	8%
C_{10}	0.42pF	normal	4.16%
C_{F0}	0.02pF	normal	6.64%

The following parameters are considered as deterministic:
K_E = 0.0, K_R = 1.111, K_1 = 1.282, C_{1S} = 0.0, and K_F = 1.282.

V_{GB} and V_{DB} are bias voltages, and P_{IN} is the driving power level.
For the definitions of the FET parameters listed here, see [9].

TABLE II

FET MODEL PARAMETER CORRELATIONS [7]

	L_G	R_S	L_S	R_{DE}	C_{DS}	g_m	τ	R_{IN}	C_{GS}	C_{GD}
L_G	1.00	-0.16	0.11	-0.22	-0.20	0.15	0.06	0.15	0.25	0.04
R_S	-0.16	1.00	-0.28	0.02	0.06	-0.09	-0.16	0.12	-0.24	0.26
L_S	0.11	-0.28	1.00	0.11	-0.26	0.53	0.41	-0.52	0.78	-0.12
R_{DE}	-0.22	0.02	0.11	1.00	-0.44	0.03	0.04	-0.54	0.02	-0.14
C_{DS}	-0.20	0.06	-0.26	-0.44	1.00	-0.13	-0.14	0.23	-0.24	-0.04
g_m	0.15	-0.09	0.53	0.03	-0.13	1.00	-0.08	-0.26	0.78	0.38
τ	0.06	-0.16	0.41	0.04	-0.14	-0.08	1.00	-0.19	0.27	-0.46
R_{IN}	0.15	0.12	-0.52	-0.54	0.23	-0.26	-0.19	1.00	-0.35	0.05
C_{GS}	0.25	-0.24	0.78	0.02	-0.24	0.78	0.27	-0.35	1.00	0.15
C_{GD}	0.04	0.26	-0.12	-0.14	-0.04	0.38	-0.46	0.05	0.15	1.00

Certain modifications have been made to adjust these small-signal parameter correlations to be consistent with the large-signal FET model.

TABLE III

YIELD OPTIMIZATION OF THE FET FREQUENCY DOUBLER

Variable	Starting Point	Nominal Design	Solution I	Solution II
P_{IN}	$2.0000\times10^{-3*}$	2.0000×10^{-3}	2.5000×10^{-3}	2.4219×10^{-3}
V_{GB}	-1.9060^{*}	-1.9060	-1.9010	-1.9011
V_{DB}	5.0000^{*}	5.0000	4.9950	4.9949
L_1	1.0000	5.4620	5.4670	5.4670
l_1	1.0000×10^{-3}	1.4828×10^{-3}	1.6306×10^{-3}	1.7088×10^{-3}
l_2	5.0000×10^{-3}	5.7705×10^{-3}	5.7545×10^{-3}	5.7466×10^{-3}
Yield		24.8%	57.0%	61.4%
Number of Optimization Iterations			11	8
Number of Function Evaluations			41	26

* Not considered as variables in nominal design.

Variable Definitions:
P_{IN} Driving power level in watts
V_{GB} Gate bias in volts
V_{DB} Drain bias in volts
L_1 Inductor in the input matching network in nH
l_1 Length of the microstrip section in meters
l_2 Length of the open-circuited microstrip stub in meters

The yield is estimated from 500 outcomes.

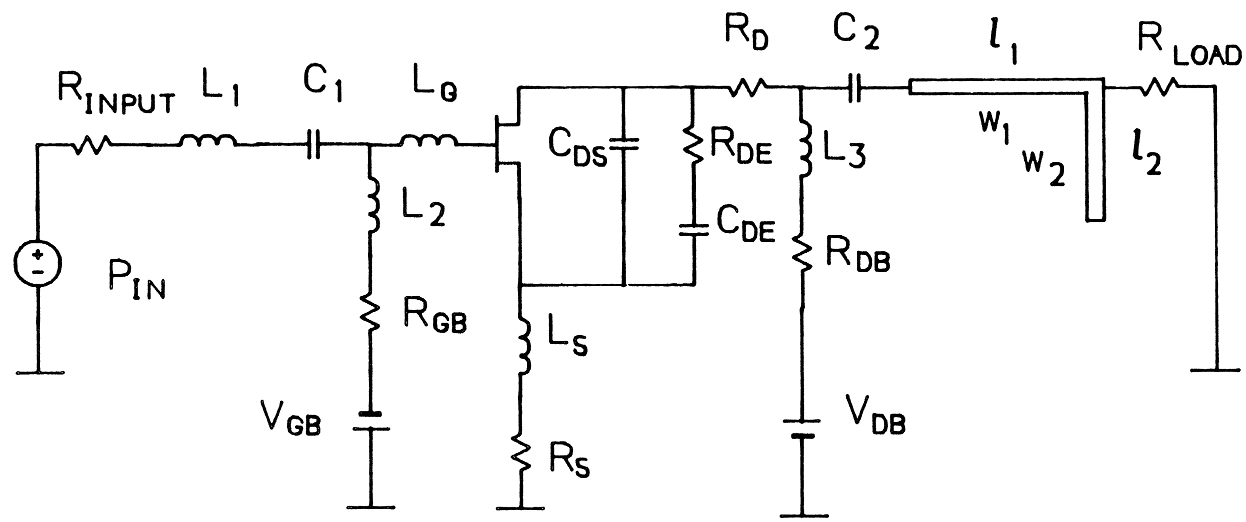

Fig. 1 Circuit diagram of the FET microwave frequency doubler example.

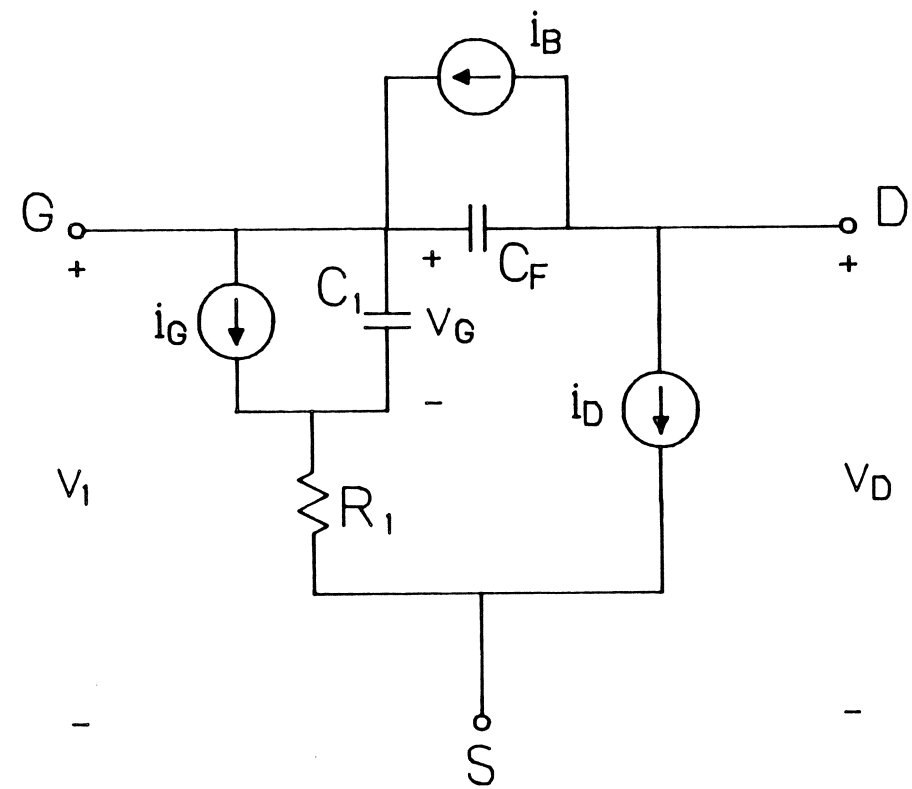

Fig. 2 Modified Materka and Kacprzak large-signal FET model [8].

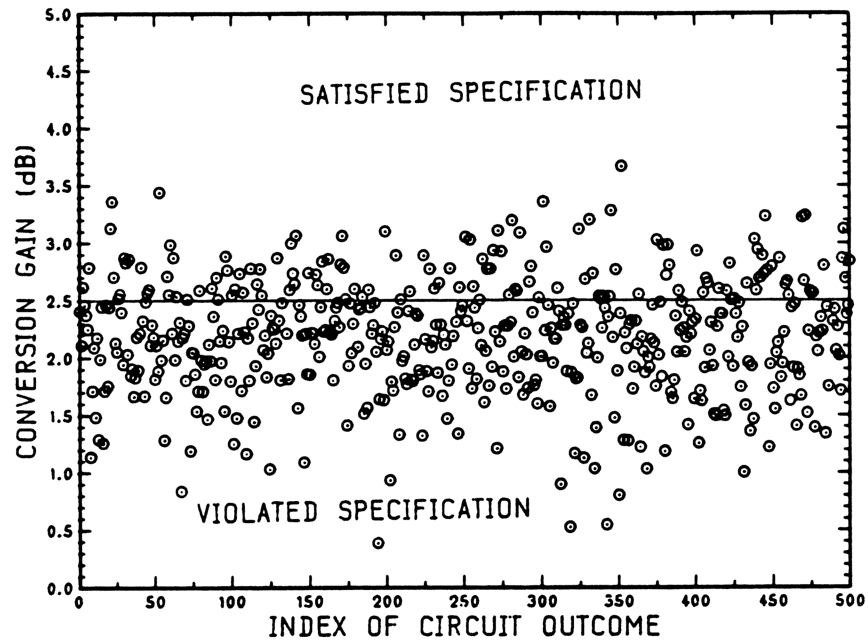

Fig. 3 Run chart of the conversion gain for up to 500 statistical outcomes of the frequency doubler before yield optimization. The straight line shown is the performance specification.

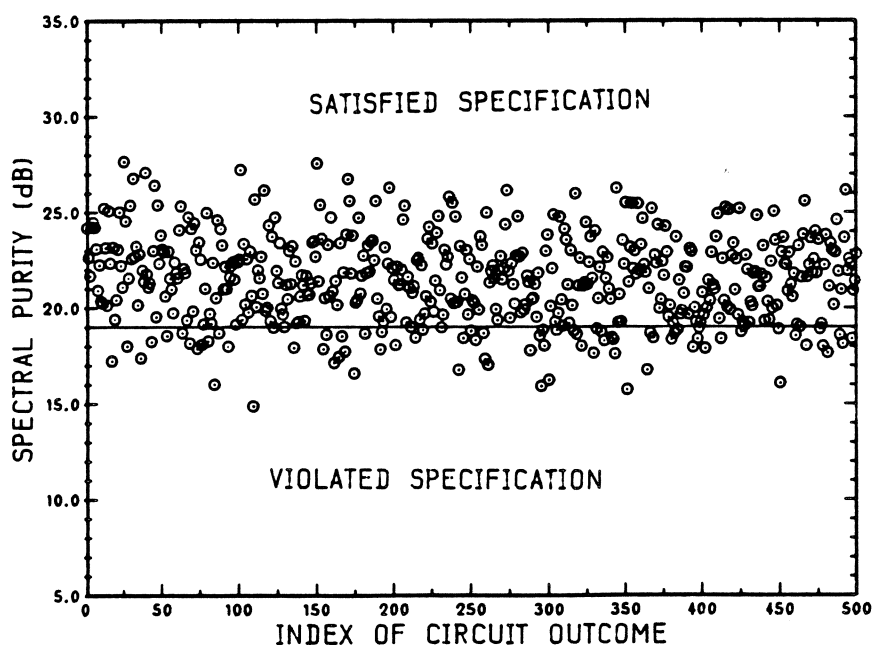

Fig. 4 Run chart of the spectral purity for up to 500 statistical outcomes of the frequency doubler before yield optimization. The straight line shown is the performance specification.

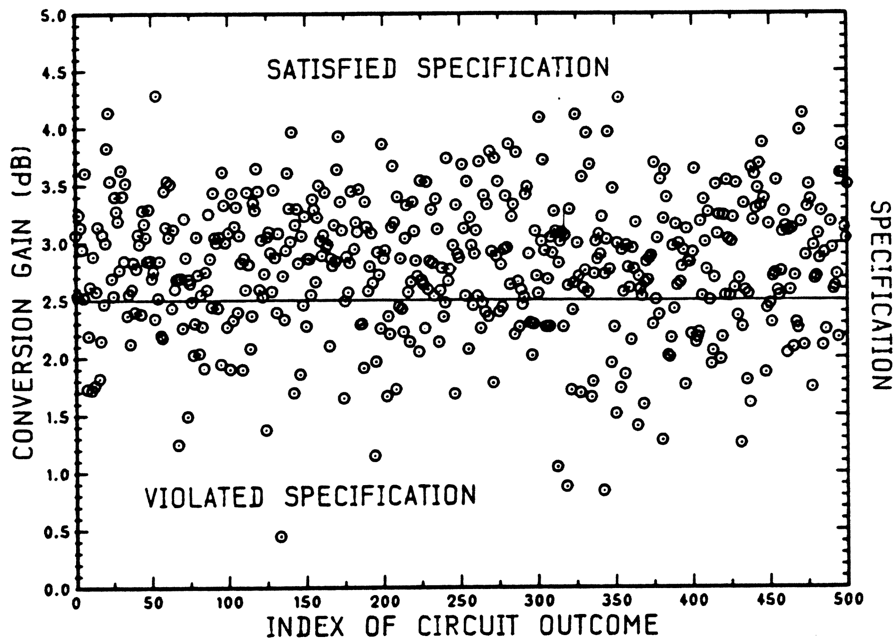

Fig. 5 Run chart of the conversion gain for up to 500 statistical outcomes of the frequency doubler after yield optimization. The straight line shown is the performance specification.

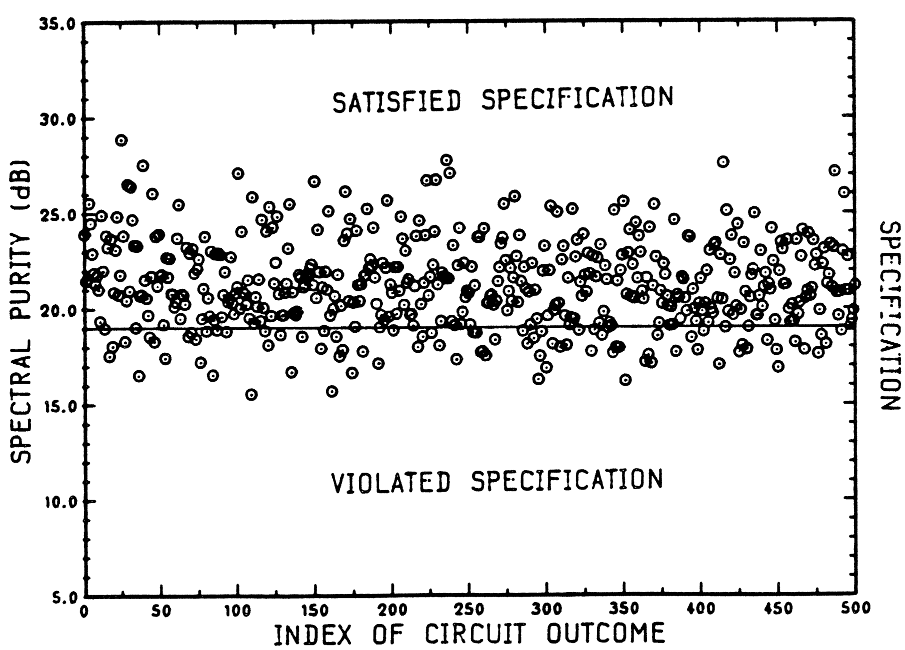

Fig. 6 Run chart of the spectral purity up to 500 statistical outcomes of the frequency doubler after yield optimization. The straight line shown is the performance specification.

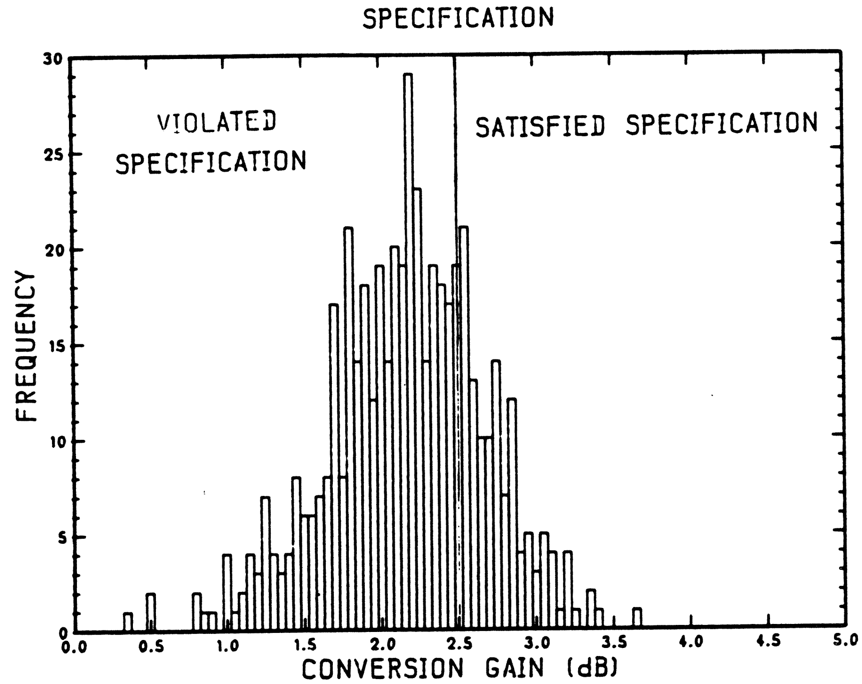

Fig. 7 Histogram of conversion gains of the frequency doubler based on 500 statistical outcomes before yield optimization. The center of the distribution is below the specification shown by a vertical line. Most statistical outcomes violate this specification.

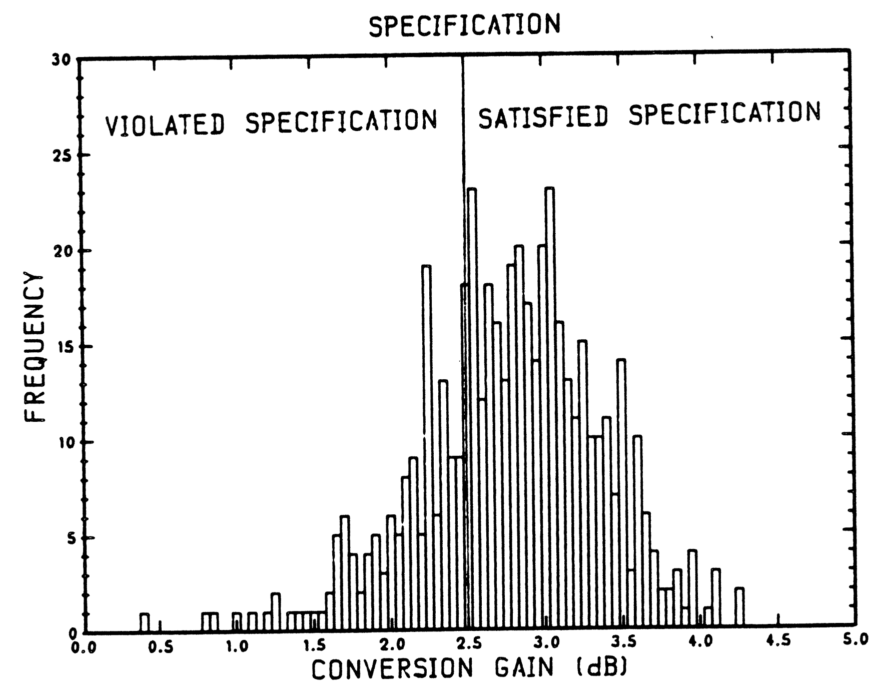

Fig. 8 Histogram of conversion gains of the frequency doubler based on 500 statistical outcomes after yield optimization. The center of the distribution is above the specification shown by a vertical line. Most statistical outcomes satisfy this specification.

PRACTICAL, HIGH SPEED GRADIENT COMPUTATION FOR HARMONIC BALANCE SIMULATORS

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Abstract

We introduce a powerful computational concept which we name the future adjoint sensitivity technique (FAST). FAST combines the efficiency of the exact adjoint sensitivity technique with the simplicity of the conventional perturbation technique. The same concept carries over to a practically implementable Jacobian for fast harmonic balance simulation. Our result promises high speed gradient evaluation essential for yield optimization of nonlinear MMIC circuits by general purpose software.

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SUMMARY

Introduction

Recent years have witnessed a resurgence of interest in harmonic balance (HB) simulation methods in the microwave industry. A growing number of microwave engineers are using HB simulators to design nonlinear circuits. Extensive number crunching currently required by available HB simulators have inhibited fast optimization of nonlinear circuits and its extension to yield driven design. Another significant drawback of current implementations is due to inaccurate sensitivity and gradient calculations.

For researchers in the HB area, improving HB efficiency and robustness has always been a serious task. Kundert and Sangiovanni-Vincentelli [1] and Rizzoli et al. [2, 3] have already suggested an exact Jacobian approach. Rizzoli et al. [4] combined both optimization and solving nonlinear equations at a single level, affording certain advantages. Its most serious disadvantage is its incompatibility with established yield optimization formulations.

Recently Bandler, Zhang and Biernacki developed the exact adjoint sensitivity technique (EAST) for the HB technique [5, 6]. The EAST has been implemented in a nonlinear HB-based parameter extraction program and demonstrated to be extremely powerful [7].

Motivated by the potential impact of the adjoint sensitivity approach on general purpose CAD programs we have studied its implementation aspects. We have discovered a practically implementable technique which we name FAST (future adjoint sensitivity technique). It retains most of the efficiency and accuracy of the EAST while accommodating the simplicity of the conventional perturbation method, which we name PAST (perturbation approximate sensitivity technique).

FAST is directly applicable not only to the node/port formulation of the

HB equations [1, 5, 6] but also to the state variable formulation [2-4], both within the framework of general purpose software.

The FAST concept has also been implemented in computation of Jacobians for high speed HB simulation. By avoiding the analytical differentiation of device equations, our approach easily accommodates complicated and piecewise device descriptions.

The features of FAST and its Jacobian extensions are exposed by a mixer example and a frequency doubler example, respectively.

Notation and Definitions

We follow the notation of [5]. The overall nonlinear circuit is divided into linear and nonlinear parts. The voltage and the current waveforms at the linear-nonlinear connection ports are represented by real vectors $\mathbf{v}(t)$ and $\mathbf{i}(t)$, respectively. The kth harmonic of these voltage and current spectrums are represented by capital letters V(k) or I(k), respectively. Y(k) is the port (linear-nonlinear connection ports) admittance matrix of the linear part. A bar denotes the split real and imaginary parts of a complex quantity. The hat distinguishes quantities of the adjoint system. In particular, $\overline{\mathbf{V}}$ or $\overline{\mathbf{I}}$ are real vectors containing the real and the imaginary parts of V(k) or I(k) for all harmonics k, k = 0, 1, ..., H. $\overline{\mathbf{Y}}$ is a real matrix containing the real and the imaginary parts of Y(k) for all harmonics k, k = 0, 1, ..., H.

Basics of the HB Technique

Let $\overline{\mathbf{I}}_{LN}$ and $\overline{\mathbf{I}}_{NL}$ represent the current into the linear and the nonlinear parts, respectively. The harmonic balance equation is

$$\overline{\mathbf{F}}(\overline{\mathbf{V}}) = \overline{\mathbf{I}}_{LN} + \overline{\mathbf{I}}_{NL} = \mathbf{0}\,. \tag{1}$$

A simple Newton's update for solving (1) is

$$\overline{\mathbf{V}}_{new} = \overline{\mathbf{V}}_{old} - \overline{\mathbf{J}}^{-1}\overline{\mathbf{F}}(\overline{\mathbf{V}}_{old}) \tag{2}$$

where $\overline{\mathbf{J}}$ is the Jacobian matrix.

Gradient Analysis Using FAST

Suppose the output voltage $\overline{V}_{out}$ can be computed from $\overline{V}$ as

$$\overline{V}_{out} = \bar{e}^T\overline{V}. \tag{3}$$

The adjoint voltage $\hat{\overline{V}}$ is the solution from the linear equation

$$\overline{J}^T\hat{\overline{V}} = \bar{e}. \tag{4}$$

Suppose ϕ is a generic circuit design variable. For a given value of ϕ, we first solve the harmonic balance equation (1) to obtain the solution $\overline{V}_{solution}$, i.e.,

$$\overline{F}(\phi, \overline{V}_{solution}) = 0. \tag{5}$$

Then the approximate sensitivity of output voltage $\overline{V}_{out}$ w.r.t. variable ϕ can be computed as

$$\partial\overline{V}_{out}/\partial\phi = - \hat{\overline{V}}^T\overline{F}(\phi+\Delta\phi, \overline{V}_{solution})/\Delta\phi. \tag{6}$$

This formula is much easier to implement than our previously published EAST [5, 6]. The function $\overline{F}$ in (6) is evaluated by perturbation and can be readily implemented. The effort for solving the linear equations (4) is small since the LU factors of the Jacobian matrix are available from the final iteration of (2).

Comparison of FAST with PAST

Suppose there are 10 design variables in the nonlinear circuit. Using PAST to calculate circuit sensitivities, one needs to perturb all design variables and to solve the entire nonlinear circuit for each perturbation, i.e., 10 times. The best possible situation for this approach is that all 10 simulations use the same Jacobian and all converge in one iteration.

Using FAST, we also need to perturb all variables. But instead of completely solving 10 nonlinear circuits, we only evaluate 10 error functions in the form of (1). The solution of adjoint equation (4) is accomplished in 2 forward/backward substitutions.

A detailed comparison reveals that FAST always requires less computation than that of the best possible situation of PAST. In our numerical experiment, FAST is 23 times faster than PAST.

Accuracy is a particularly important feature of FAST. In our numerical experiment, gradients from FAST are about 100 times more accurate than those from PAST. This means that HB optimization will be more robust by using FAST.

Comparison of FAST with EAST

The generic EAST is accepted by all circuit theoreticians as the most powerful tool. However, to implement it, we have to keep track of all arbitrary locations of variables and to compute branch voltages at all these locations. This requirement, in general, is so involved that microwave software engineers virtually abandoned hope of generally implementing the EAST.

In FAST, we completely eliminate the need of track variable locations. We only need to identify the output port which is the simplest step in adjoint sensitivity theory.

High Performance FAST

Like any numerical techniques, the performance of the FAST can be enhanced to deal with ill-conditioned or large scale problems. The choice of the step length has a significant effect on accuracy. An optimal step length adjustment scheme will be presented.

FAST Analysis of a FET Mixer

Consider the mixer example used in [5, 6, 8]. Figs. 1 and 2 show the large-signal MESFET model and the DC characteristics of the device. The frequencies are f_{LO} = 11 GHz, f_{RF} = 12 GHz and f_{IF} = 1 GHz. The DC bias voltages are V_{GS} = -0.9 V and V_{DS} = 3.0 V. With LO power P_{LO} = 8 dBm and RF power P_{RF} = -15 dBm, the conversion gain was 6.9 dB. 26 variables were considered including all parameters in the linear as well as in the nonlinear part, DC bias, LO power, RF power, IF, LO and RF terminations. We used FAST theory to compute the sensitivities of the conversion gain w.r.t. all variables. The same sensitivities were also evaluated by the EAST and PAST. Excellent agreement between the three approaches is shown in Table I.

From Table I, we notice that the FAST sensitivities are almost identical to the exact sensitivities. But the PAST sensitivities are typically 1 to 2 percent different from their exact values. This fact reveals that the FAST is much more reliable than PAST.

The circuit was solved in 22 seconds on a VAX 8600. The CPU time for the FAST, the EAST and the PAST were 10.7, 3.7 and 240 seconds, respectively. FAST is 3 times slower than EAST but 23 times faster than PAST.

Simple and Efficient Approach to Computation of Jacobian

Kundert and Sangiovanni-Vincentelli [1] and Rizzoli et. al. [2, 3] have investigated exact Jacobians for accelerating the HB procedure. However, as observed by Rizzoli et. al. [3], differentiating complicated or piecewise device equations may be very annoying from a programmer's view point. The perturbation (or incremental) approach is often used in practice.

Such difficulties associated with the exact Jacobians can be eliminated by extending the concept of FAST to the Jacobian calculation. We compute the time domain derivatives $\partial i(t)/\partial v(t)$ at the device level using perturbations. These derivatives are then converted to the frequency domain by a Fourier transform. The Jacobian matrix is then assembled from these Fourier coefficients using the formulas in [1, 3].

Approximate Jacobian for a Frequency Doubler

We have used our Jacobian approach in solving the FET frequency doubler example from Microwave Harmonica [9]. The circuit consists of a common source

FET with a lumped input matching network and a microstrip output matching and filtering section. The circuit diagram is shown in Fig. 3. The input frequency is 5GHz. The output is at 10GHz. 4 harmonics are considered. We have also used the conventional perturbation approach to compute the Jacobian. The numerical results from the two approaches agree very well. The CPU time for our approach and the perturbation approach is .89 and 5.3 seconds, respectively, on Micro VAX II.

Conclusion

Our FAST is an expedient tool for gradient calculation in the HB environment. The advantages of FAST over PAST are its unmatched speed and accuracy, and over the EAST is its implementational simplicity. FAST is directly compatible with established formulations of yield optimization. FAST is particularly suitable for implementation in general purpose microwave CAD software. We feel that FAST provides a key to the new generation of yield optimizers for MMICs.

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TABLE I

NUMERICAL VERIFICATION OF FAST FOR THE MIXER EXAMPLE

Var.	Sensitivity from FAST	Sensitivity from EAST	Sensitivity from PAST	Difference between FAST and EAST (%)	Difference between FAST and PAST (%)
linear subnetwork					
C_{ds}	-24.28082	-24.28081	-24.03669	0.00	1.01
C_{gd}	-32.16238	-32.16237	-32.33670	0.00	-0.54
C_{de}	-8.8×10^{-13}	1.7×10^{-13}	0	120.21	100.00
R_g	10.00754	10.00756	9.89609	-0.00	1.11
R_d	11.71325	11.71327	11.71338	-0.00	-0.00
R_s	-4.98829	-4.98827	-4.98861	0.00	-0.01
R_{de}	-0.07171	-0.07171	-0.07115	0.00	0.79
L_g	-0.30238	-0.30238	-0.30054	0.00	0.61
L_d	-0.87824	-0.87824	-0.87247	0.00	0.66
L_s	-0.33527	-0.33527	-0.33191	0.00	1.00
nonlinear subnetwork*					
C_{gs0}	-5.43110	-5.43110	-5.38265	0.00	0.89
τ	1.52983	1.52984	1.56057	-0.00	-2.01
V_ϕ	-20.84224	-20.84223	-20.84308	0.00	-0.00
V_{p0}	-14.62206	-14.62206	-14.62469	0.00	-0.02
V_{dss}	0.30209	0.30209	0.30210	-0.00	-0.00
I_{dsp}	9.39335	9.39335	9.39338	-0.00	-0.00
bias and driving sources					
V_{GS}	-4.94402	-4.94402	-4.94271	-0.00	0.03
V_{DS}	-0.67424	-0.67424	-0.67429	0.00	-0.01
P_{LO}	2.02886	2.02885	2.02882	0.00	0.00
P_{RF}	-0.09073	-0.09072	-0.09077	0.01	-0.05

TABLE I (continued)

NUMERICAL VERIFICATION OF FAST FOR THE MIXER EXAMPLE

Var.	Sensitivity from FAST	Sensitivity from EAST	Sensitivity from PAST	Difference between FAST and EAST (%)	Difference between FAST and PAST (%)
terminations+					
$R_g(f_{LO})$	8.83598	8.83596	8.76244	0.00	0.83
$X_g(f_{LO})$	2.20500	2.20496	2.16567	0.00	1.78
$R_g(f_{RF})$	0.71282	0.71281	0.70568	0.00	1.00
$X_g(f_{RF})$	0.46410	0.46409	0.45702	0.00	1.53
$R_d(f_{IF})$	0.65950	0.65950	0.65272	-0.00	1.03
$X_d(f_{IF})$	0.09024	0.09024	0.09207	-0.00	-2.02

* Nonlinear elements are characterized by

$$C_{gs}(v_1) = C_{gs0} / \sqrt{1 - v_1/V_\phi} \ ,$$

$$R_i(v_1) C_{gs}(v_1) = \tau$$

and the function for $i_m(v_1, v_2)$ is shown in Fig. 2, whose mathematical expression is consistent with [8]. V_ϕ, V_{p0}, V_{dss} and I_{dsp} are parameters in the function $i_m(v_1, v_2)$.

\+ R and X represent the real and the imaginary parts of the terminating impedances, respectively. Subscripts g and d represent the gate and the drain terminations, respectively.

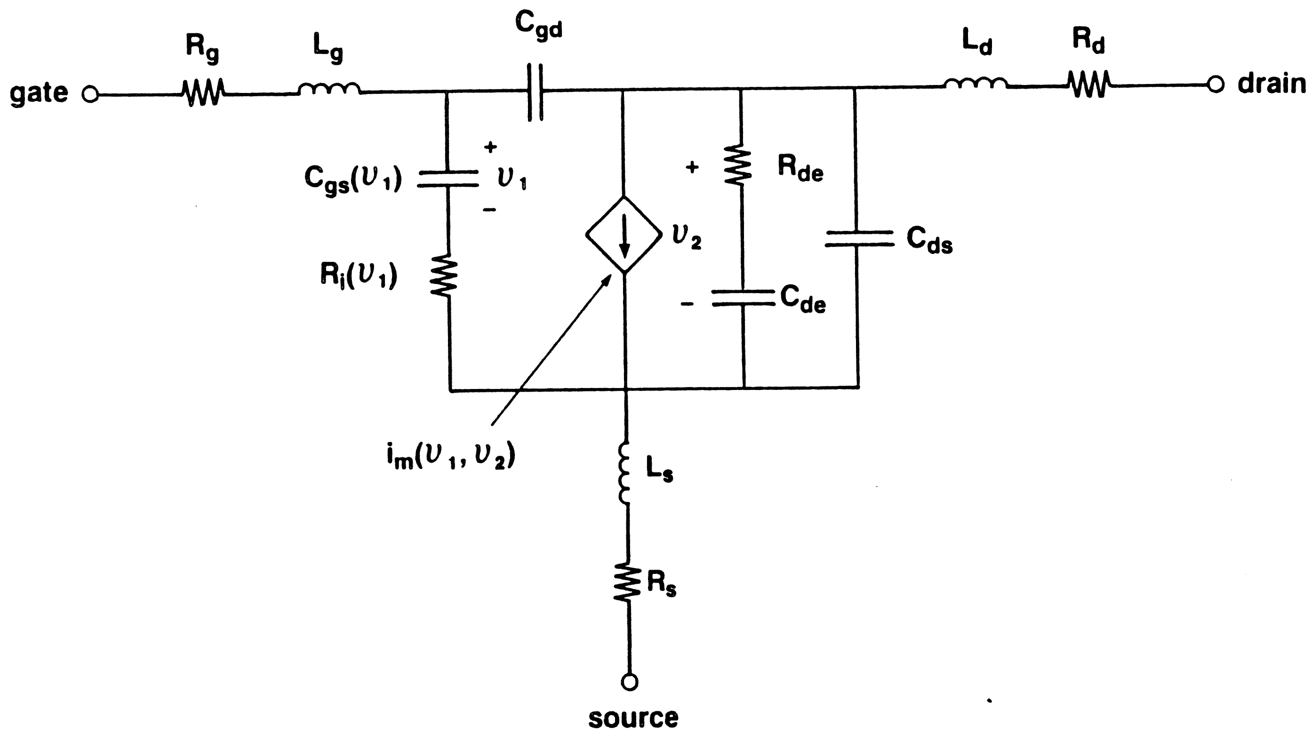

Fig. 1 A large-signal MESFET model used for the mixer example. All parameter values are consistent with [8].

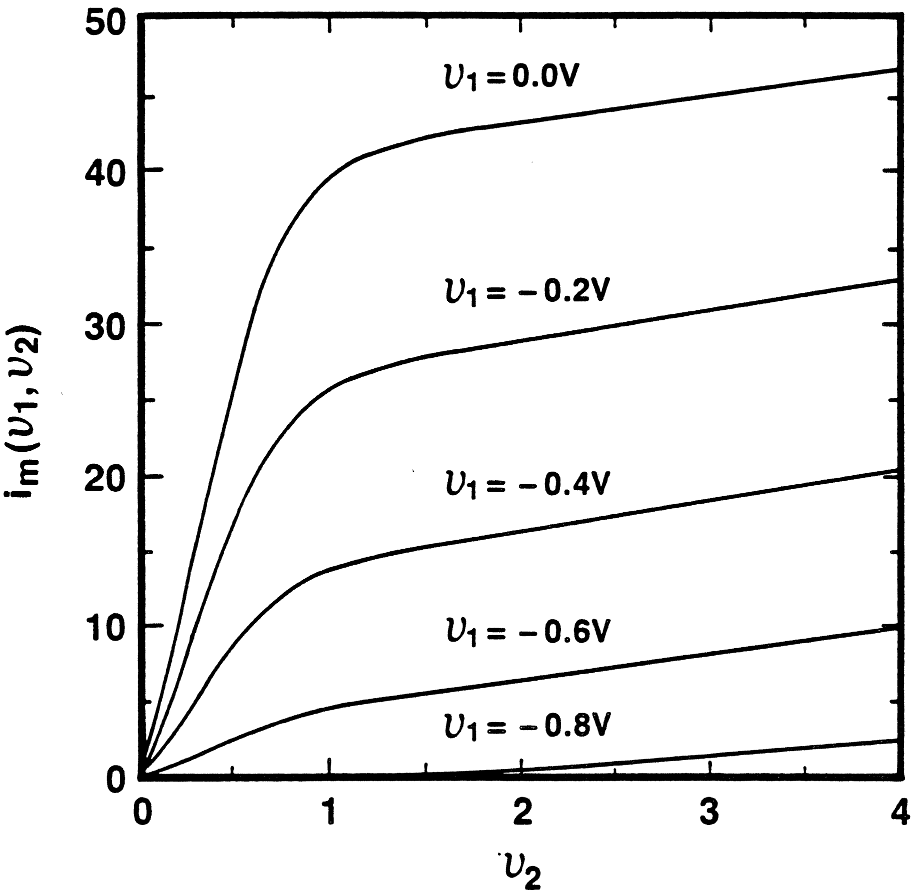

Fig. 2 The DC characteristics of the MESFET model in Fig. 1.

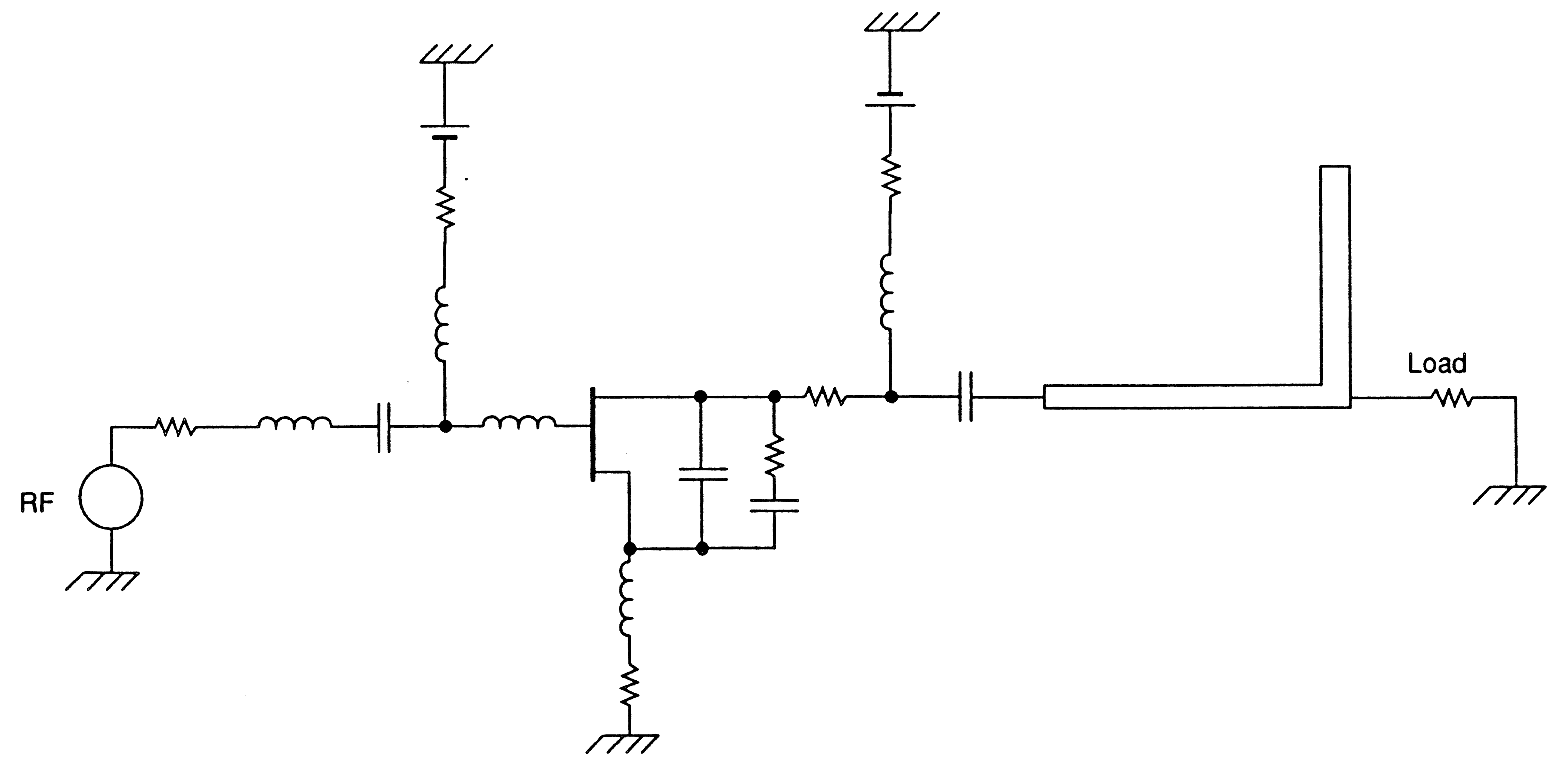

Fig. 3 The frequency doubler example used for testing the Jacobian matrix.