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*Abstract*

A comprehensive treatment of yield optimization of nonlinear microwave circuits with statistically characterized devices is proposed. We fully exploit advanced techniques of one-sided $\ell_1$ circuit centering with gradient approximations, and efficient harmonic balance simulation with exact Jacobians. Multidimensional statistical distributions of the intrinsic and parasitic parameters of FETs are fully handled. Yield is driven from 25% to 61% for a frequency doubler design having 34 statistically toleranced parameters.


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## SUMMARY

*Introduction*

Yield optimization [1,2] has been extensively explored in the literature. For linear circuits, it is currently finding its way into commercial microwave CAD software. Yield optimization of practical nonlinear microwave circuits remains unaddressed hitherto.

Requirements essential to yield optimization of nonlinear microwave circuits are: (1) effective approaches to design centering, (2) highly efficient optimization techniques, (3) fast and reliable simulation, (4) flexibility of handling various statistical representations of devices and elements, and (5) low design costs and short design cycles.

In this paper, we offer an approach for efficient yield-driven optimization of nonlinear microwave circuits with statistically characterized devices. The formulation of the yield problem for nonlinear circuits is described. A very powerful and robust one-sided $\ell_1$ optimization algorithm for design centering recently proposed by Bandler et al. [3] is adopted. An effective gradient approximation technique presented by Bandler et al. [4] is integrated with the one-sided $\ell_1$ algorithm to handle inexact gradients. The harmonic balance method is implemented with exact Jacobian matrices for fast convergence and improved robustness. Independent and/or correlated normal distributions and uniform distributions describing large-signal FET model parameters and passive elements are fully accommodated.

Modern supercomputers have found applications in microwave CAD [5, 6] with attractive performance-to-cost ratios. Our software has been developed for possible use on supercomputers. The computational performance on the Cray X-MP/44 will be reported in the full paper.

The yield optimization of a microwave frequency doubler with a large-signal statistically simulated FET model is successfully carried out. The performance yield was increased from 25% to 61%.

We believe that this is the first demonstration of yield optimization of nonlinear

circuits operating under large-signal steady-state periodic or almost periodic conditions.

*Formulation of the Yield Problem for Nonlinear Circuits*

In yield estimation and statistical circuit design, a set of outcomes around the given nominal design $\phi^0$ is considered. These outcomes are sampled according to the element statistics including possible correlations and are denoted by $\phi^i$, i = 1, 2, ... , N.

Suppose that the number of harmonics considered in simulation is H. Specifications are given at the DC level and/or several harmonics. Suppose that specifications are applied to circuit responses at the *k*th harmonic. The set of specifications and the corresponding set of calculated response functions of the outcome, $\phi^i$, are denoted by

$$S_j(k), \quad 0 \leq k \leq H, \quad j = 1, 2, ..., M \tag{1}$$

and

$$F_j(\phi^i, k), \qquad 0 \leq k \leq H, \quad j = 1, 2, ..., M, \tag{2}$$

where M is the number of specifications. The error functions for the *i*th outcome, $\mathbf{e}(\phi^i)$, comprise the entries

$$F_j(\phi^i, k) - S_{uj}(k), \tag{3}$$

and/or

$$S_{lj}(k) - F_j(\phi^i, k), \tag{4}$$

where $S_{uj}(k)$ and $S_{lj}(k)$ are upper and lower specifications. More than one harmonic index can be introduced to these functions to cope with responses such as conversion gain or power added efficiency, etc.

An outcome $\phi^i$ represents an acceptable circuit if all entries in $\mathbf{e}(\phi^i)$ are negative. Yield can be estimated by

$$Y \approx N_{pass}/N, \tag{5}$$

where $N_{pass}$ is the number of acceptable circuits and N is the total number of circuit outcomes.

*Yield Optimization*

The formulation of the objective function for our yield optimization approach consists of two steps. First, the generalized $\ell_1$ function $v(e(\phi^i))$ can be calculated from $e(\phi^i)$. Then, the one-sided $\ell_1$ objective function for yield optimization [3] is defined by

$$u(\phi^0) = \sum_{i \in J} \alpha_i v(e(\phi^i)), \tag{6}$$

where $J = \{i \mid v(e(\phi^i)) > 0,\ i = 1, 2, ..., N\}$ and $\alpha_i$ are properly chosen non-zero multipliers. Only positive error functions of individual outcomes contribute to the overall objective function. The highly efficient optimization algorithm of [3] is used to minimize $u(\phi^0)$, achieving a centered design with improved yield.

Since the one-sided $\ell_1$ algorithm requires gradients, the flexible and effective gradient approximation algorithm proposed in [4] is modified here to address the fact that analytical gradients are traditionally not produced by general purpose large-scale simulators of nonlinear circuits.

*Harmonic Balance Method as Simulation Tool*

Responses of nonlinear circuits operating in a periodic steady-state regime are calculated by the harmonic balance method. In statistical design, the circuit simulation accounts for an extremely large portion of the overall computational effort, because of the large number of outcomes simulated individually. The notable difference between linear and nonlinear simulations is that the harmonic balance method is an iterative process. To achieve fast convergence and reliable solutions, our program calculates exact Jacobian matrices.

*Statistical Outcomes*

Purviance et. al. [7] treated the statistical characterization of small-signal FET models. Our proposed yield optimization requires statistically described large-signal FET models. We use a random number generator capable of generating statistical outcomes from the independent and multidimensional correlated normal distributions and from uniform distributions.

Unlike linear FET models, the nonlinear large-signal models employed are valid only in certain regions. A normal distribution random generator may generate outcomes far beyond the valid region. Such outcomes must be carefully detected and eliminated.

*A FET Frequency Doubler Example*

Consider the FET frequency doubler example (Fig. 1) used by Microwave Harmonica [8]. It consists of a common-source FET with a lumped input matching network and a microstrip output matching and filter section. The fundamental frequency is 5GHz. Let $CG(\phi,2,1)$ be the conversion gain between input port at fundamental frequency and the output port at the second harmonic. Let $SP(\phi,2)$ be the spectral purity of the output port at the second harmonic. The design specifications are 2.5 dB for the conversion gain and 19 dB for the spectral purity. The error functions are

$$e_1(\phi) = 2.5 - CG(\phi,2,1)$$

and

$$e_2(\phi) = 19 - SP(\phi,2).$$

The optimization variables include the input inductance $L_1$ and the microstrip lengths $l_1$ and $l_2$. The operating condition of a frequency doubler is essential for its performance. Therefore, two bias voltages, $V_{GB}$ and $V_{DB}$, and the driving power level, $P_{IN}$ are also considered as optimization variables.

The intrinsic large-signal FET model is the modified Materka and Kacprzak model [8]. The model is shown in Fig. 2. Independent uniform distributions with fixed tolerances of 3% are assumed for all design variables. Normal distributions are assumed for all FET intrinsic and extrinsic parameters. The standard deviations of these distributions are listed in Table I. The statistical correlations of the nonlinear intrinsic FET are based on [7]. The assumed correlation parameters are shown in Table II.

The starting point for yield optimization is the solution of the conventional nominal design w.r.t. the same specifications, using $L_1$, $l_1$ and $l_2$ as optimization variables. The initial yield based on 500 outcomes is 24.8%. 50 statistically selected outcomes were used in the yield optimization process. The solution found by our approach improves the yield to

57%. Then another set of 50 outcomes was selected and optimization restarted. After this, the final yield was 61.4%. Computational details are given in Table III.

Run charts for the conversion gain and the spectral purity before and after yield optimization are shown in Figs. 3, 4, 5 and 6, respectively. The statistical properties of these two responses can be seen from the run charts. Figs. 7 and 8 show histograms of the conversion gain before and after yield optimization. Before yield optimization, the center of the distribution is on the left-hand side of the design specification of 2.5 dB, indicating that most outcomes are unacceptable. After yield optimization, the center of the distribution is shifted to the right-hand side of the 2.5 dB specification. Most outcomes then satisfy the specifications.

*A FET Amplifier Example*

By considering the DC and fundamental frequency, the harmonic balance method not only solves the small-signal linearized circuit, but also simulates the DC bias condition. We have exploited this in the design of a FET amplifier.

Performance specifications were imposed on small-signal S-parameter responses. The modified Materka and Kacprzak large-signal FET model [9] was used. We performed a yield optimization allowing the bias voltages to vary during optimization. This enables us to study the effects of operating conditions on performance yield of a linear circuit.

*Conclusions*

The first comprehensive demonstration of yield optimization of statistically characterized nonlinear microwave circuits operating within the harmonic balance simulation environment has been made. Advanced one-sided $\ell_1$ design centering combined with efficient harmonic balance simulation using exact Jacobians are exploited. Large-signal FET parameter statistics are fully facilitated. Comprehensive numerical experiments directed at yield-driven optimization of a FET frequency doubler support our confidence. It lends significant credence to the necessity of statistical modeling of nonlinear microwave devices for large-signal applications.

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TABLE I

ASSUMED STATISTICAL DISTRIBUTIONS FOR THE FREQUENCY DOUBLER

| Element and FET Parameter | Nominal Value | Type of Distribution | Relative Tolerance or Standard Deviation |
|---|---|---|---|
| $V_{GB}$ | optimized | uniform | 3% |
| $V_{DB}$ | optimized | uniform | 3% |
| $P_{IN}$ | optimized | uniform | 3% |
| $l_1$ | optimized | uniform | 3% |
| $l_2$ | optimized | uniform | 3% |
| $L_1$ | optimized | uniform | 3% |
| $L_2$ | 15nH | uniform | 5% |
| $L_3$ | 15nH | uniform | 5% |
| $C_1$ | 20pF | uniform | 5% |
| $C_2$ | 20pF | uniform | 5% |
| $w_1$ | $0.1 \times 10^{-3}$m | uniform | 5% |
| $w_2$ | $0.635 \times 10^{-3}$m | uniform | 5% |
| $L_G$ | 0.16nH | normal | 5% |
| $R_D$ | 2.153Ω | normal | 3% |
| $L_S$ | 0.07nH | normal | 5% |
| $R_S$ | 1.144Ω | normal | 5% |
| $R_{DE}$ | 440Ω | normal | 14% |
| $C_{DE}$ | 1.15pF | normal | 3% |
| $C_{DS}$ | 0.12pF | normal | 4.5% |
| $I_{DSS}$ | $6.0 \times 10^{-2}$ | normal | 5% |
| $V_{p0}$ | -1.906 | normal | 0.65% |
| $\gamma$ | $-15. \times 10^{-2}$ | normal | 0.65% |
| E | 1.8 | normal | 0.65% |
| $S_l$ | $0.676 \times 10^{-1}$ | normal | 0.65% |
| $K_G$ | 1.1 | normal | 0.65% |
| $\tau$ | 7.0pS | normal | 6% |
| $S_S$ | $1.666 \times 10^{-3}$ | normal | 0.65% |
| $I_{G0}$ | $0.713 \times 10^{-5}$ | normal | 3% |
| $\alpha_G$ | 38.46 | normal | 3% |
| $I_{B0}$ | $-0.713 \times 10^{-5}$ | normal | 3% |
| $\alpha_B$ | -38.46 | normal | 3% |
| $R_{10}$ | 3.5Ω | normal | 8% |
| $C_{10}$ | 0.42pF | normal | 4.16% |
| $C_{F0}$ | 0.02pF | normal | 6.64% |

The following parameters are considered as deterministic:
$K_E = 0.0$, $K_R = 1.111$, $K_1 = 1.282$, $C_{1S} = 0.0$, and $K_F = 1.282$.

$V_{GB}$ and $V_{DB}$ are bias voltages, and $P_{IN}$ is the driving power level.
For the definitions of the FET parameters listed here, see [9].

TABLE II

FET MODEL PARAMETER CORRELATIONS [7]

| | $L_G$ | $R_S$ | $L_S$ | $R_{DE}$ | $C_{DS}$ | $g_m$ | $\tau$ | $R_{IN}$ | $C_{GS}$ | $C_{GD}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| $L_G$ | 1.00 | -0.16 | 0.11 | -0.22 | -0.20 | 0.15 | 0.06 | 0.15 | 0.25 | 0.04 |
| $R_S$ | -0.16 | 1.00 | -0.28 | 0.02 | 0.06 | -0.09 | -0.16 | 0.12 | -0.24 | 0.26 |
| $L_S$ | 0.11 | -0.28 | 1.00 | 0.11 | -0.26 | 0.53 | 0.41 | -0.52 | 0.78 | -0.12 |
| $R_{DE}$ | -0.22 | 0.02 | 0.11 | 1.00 | -0.44 | 0.03 | 0.04 | -0.54 | 0.02 | -0.14 |
| $C_{DS}$ | -0.20 | 0.06 | -0.26 | -0.44 | 1.00 | -0.13 | -0.14 | 0.23 | -0.24 | -0.04 |
| $g_m$ | 0.15 | -0.09 | 0.53 | 0.03 | -0.13 | 1.00 | -0.08 | -0.26 | 0.78 | 0.38 |
| $\tau$ | 0.06 | -0.16 | 0.41 | 0.04 | -0.14 | -0.08 | 1.00 | -0.19 | 0.27 | -0.46 |
| $R_{IN}$ | 0.15 | 0.12 | -0.52 | -0.54 | 0.23 | -0.26 | -0.19 | 1.00 | -0.35 | 0.05 |
| $C_{GS}$ | 0.25 | -0.24 | 0.78 | 0.02 | -0.24 | 0.78 | 0.27 | -0.35 | 1.00 | 0.15 |
| $C_{GD}$ | 0.04 | 0.26 | -0.12 | -0.14 | -0.04 | 0.38 | -0.46 | 0.05 | 0.15 | 1.00 |

Certain modifications have been made to adjust these small-signal parameter correlations to be consistent with the large-signal FET model.

TABLE III

YIELD OPTIMIZATION OF THE FET FREQUENCY DOUBLER

| Variable | Starting Point | Nominal Design | Solution I | Solution II |
|---|---|---|---|---|
| $P_{IN}$ | $2.0000\times10^{-3*}$ | $2.0000\times10^{-3}$ | $2.5000\times10^{-3}$ | $2.4219\times10^{-3}$ |
| $V_{GB}$ | $-1.9060^{*}$ | -1.9060 | -1.9010 | -1.9011 |
| $V_{DB}$ | $5.0000^{*}$ | 5.0000 | 4.9950 | 4.9949 |
| $L_1$ | 1.0000 | 5.4620 | 5.4670 | 5.4670 |
| $l_1$ | $1.0000\times10^{-3}$ | $1.4828\times10^{-3}$ | $1.6306\times10^{-3}$ | $1.7088\times10^{-3}$ |
| $l_2$ | $5.0000\times10^{-3}$ | $5.7705\times10^{-3}$ | $5.7545\times10^{-3}$ | $5.7466\times10^{-3}$ |
| Yield | | 24.8% | 57.0% | 61.4% |
| Number of Optimization Iterations | | | 11 | 8 |
| Number of Function Evaluations | | | 41 | 26 |

* Not considered as variables in nominal design.

Variable Definitions:
$P_{IN}$ Driving power level in watts
$V_{GB}$ Gate bias in volts
$V_{DB}$ Drain bias in volts
$L_1$ Inductor in the input matching network in nH
$l_1$ Length of the microstrip section in meters
$l_2$ Length of the open-circuited microstrip stub in meters

The yield is estimated from 500 outcomes.

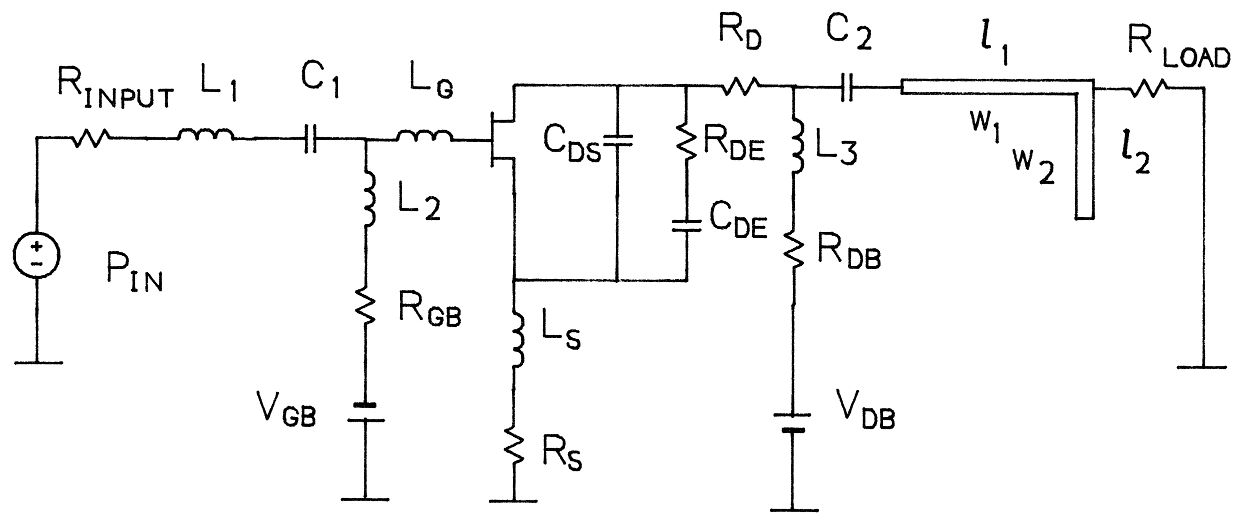


Fig. 1 Circuit diagram of the FET microwave frequency doubler example.

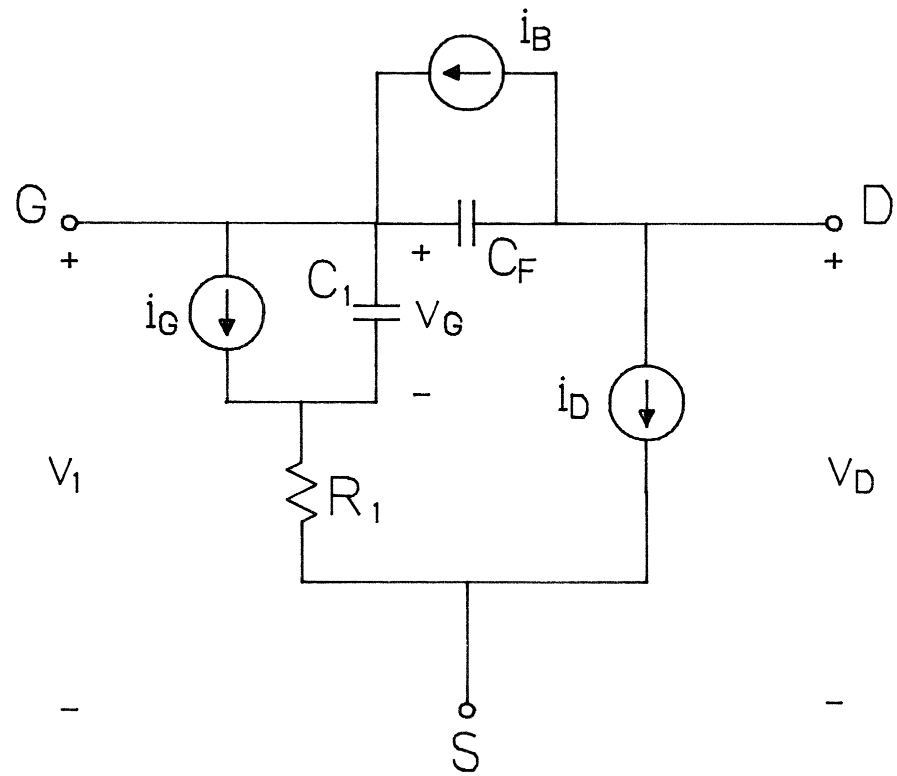


Fig. 2 Modified Materka and Kacprzak large-signal FET model [8].

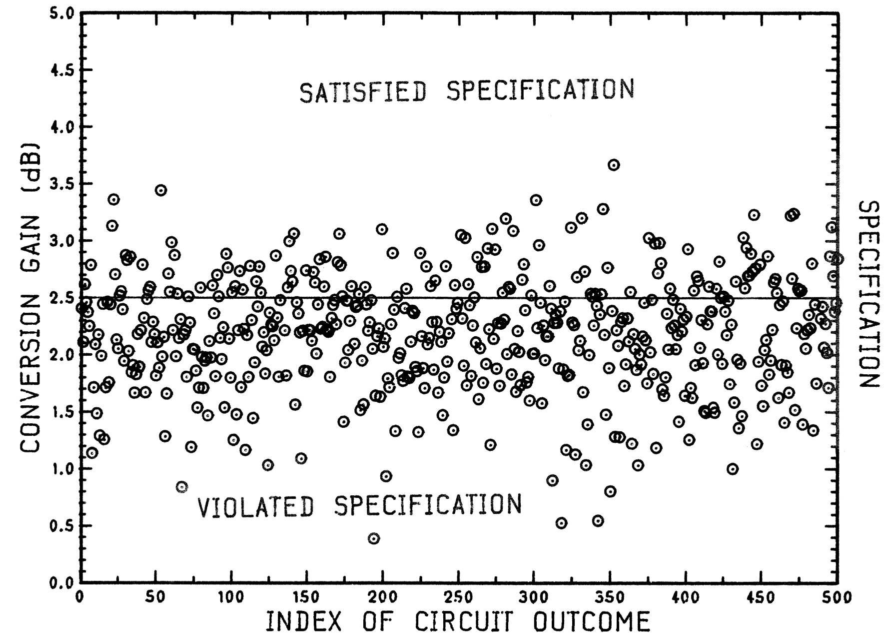


Fig. 3 Run chart of the conversion gain for up to 500 statistical outcomes of the frequency doubler before yield optimization. The straight line shown is the performance specification.

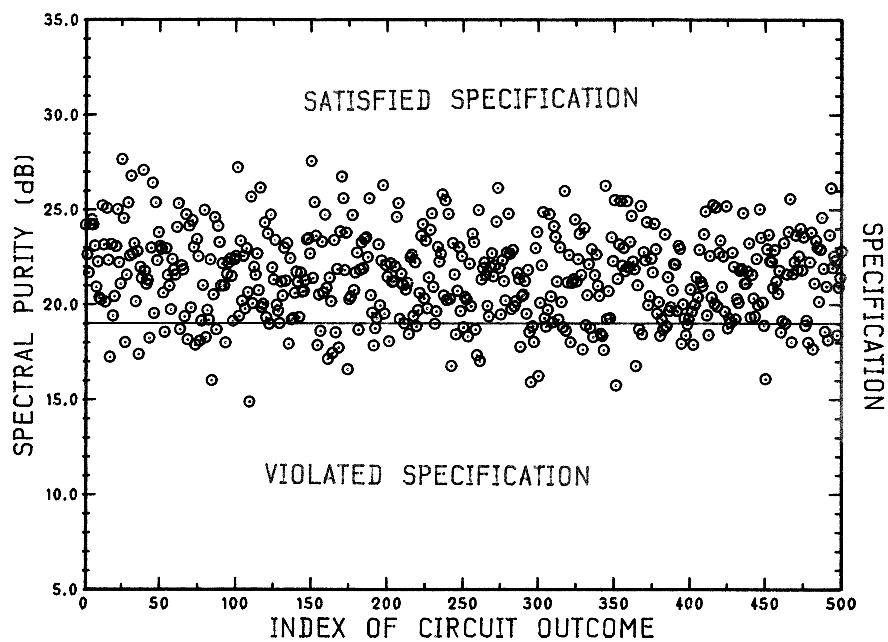


Fig. 4 Run chart of the spectral purity for up to 500 statistical outcomes of the frequency doubler before yield optimization. The straight line shown is the performance specification.

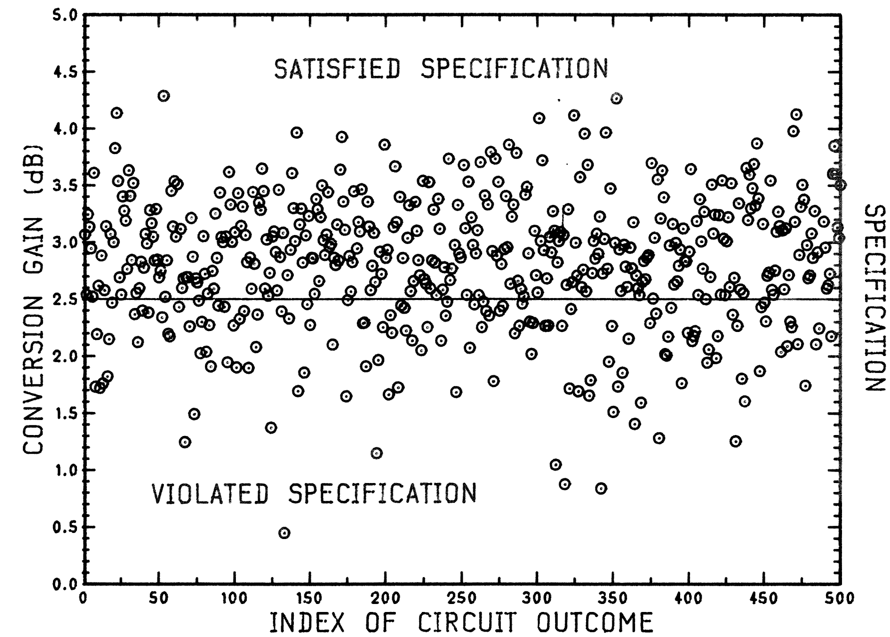


Fig. 5 Run chart of the conversion gain for up to 500 statistical outcomes of the frequency doubler after yield optimization. The straight line shown is the performance specification.

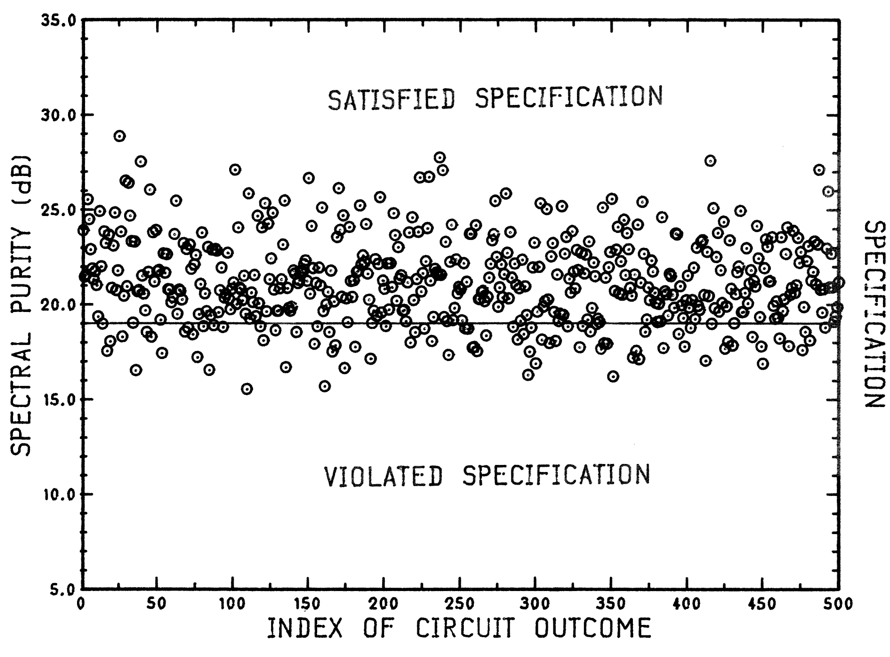


Fig. 6 Run chart of the spectral purity up to 500 statistical outcomes of the frequency doubler after yield optimization. The straight line shown is the performance specification.

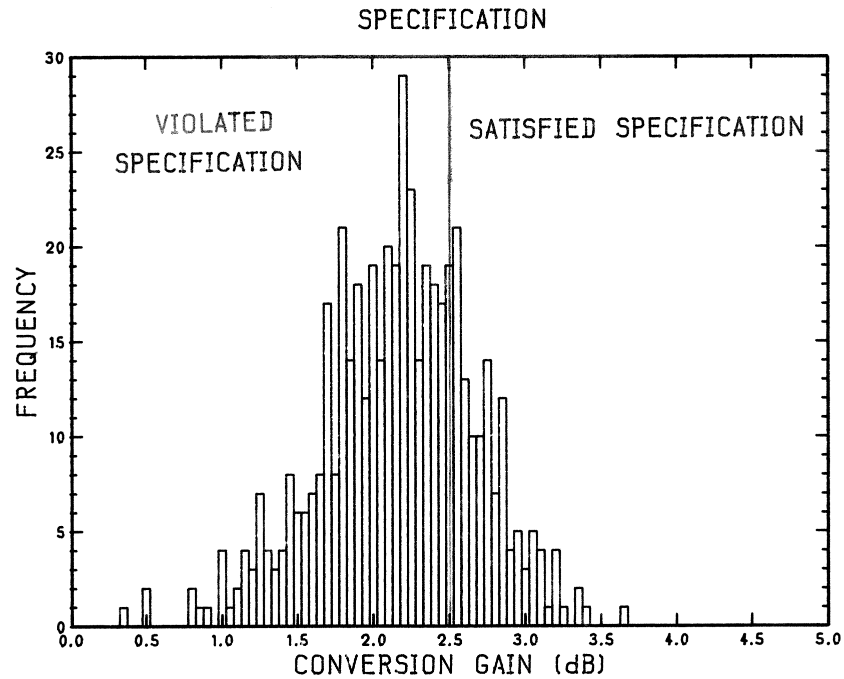


Fig. 7 Histogram of conversion gains of the frequency doubler based on 500 statistical outcomes before yield optimization. The center of the distribution is below the specification shown by a vertical line. Most statistical outcomes violate this specification.

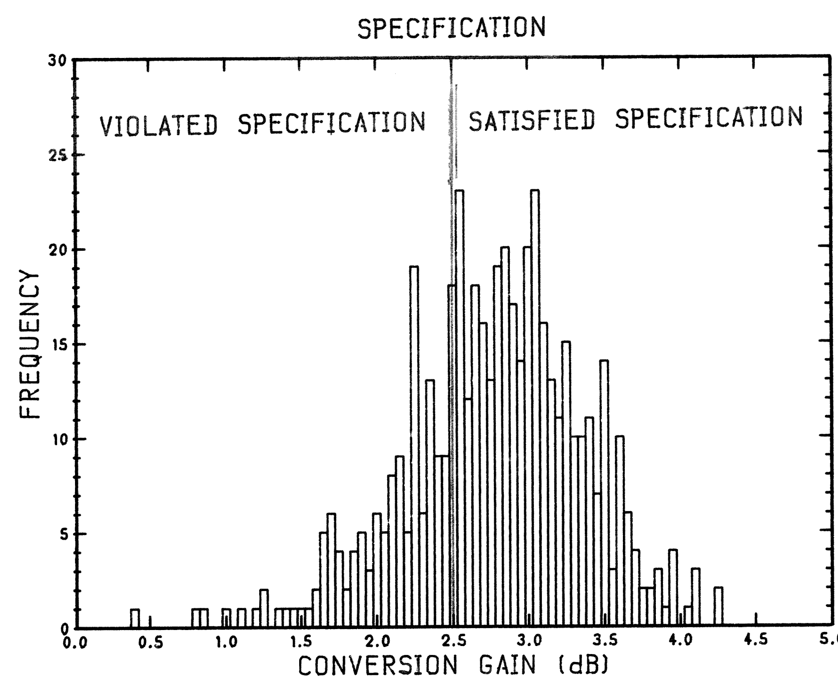


Fig. 8 Histogram of conversion gains of the frequency doubler based on 500 statistical outcomes after yield optimization. The center of the distribution is above the specification shown by a vertical line. Most statistical outcomes satisfy this specification.