A UNIFIED THEORY FOR FREQUENCY DOMAIN SIMULATION AND SENSITIVITY ANALYSIS OF LINEAR AND NONLINEAR CIRCUITS

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A UNIFIED THEORY FOR FREQUENCY DOMAIN SIMULATION AND SENSITIVITY ANALYSIS OF LINEAR AND NONLINEAR CIRCUITS

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Abstract

In this paper, a unified theory for frequency domain simulation and sensitivity analysis of linear and nonlinear circuits is presented. An elegant derivation expands the harmonic balance technique from nonlinear simulation to nonlinear adjoint sensitivity analysis. This provides an efficient tool for the otherwise expensive but essential gradient calculations in design optimization. The hierarchical approach, widely used for circuit simulation, is generalized to sensitivity analysis and to computing responses in any subnetwork at any level of the hierarchy. Therefore, important aspects of frequency domain circuit CAD such as simulation and sensitivity analysis, linear and nonlinear circuits, hierarchical and nonhierarchical approaches, voltage and current excitations, or open and short circuit terminations are unified in this general framework. Our theory provides a key for the coming generation of microwave CAD software. It will take advantage of the many existing and mature techniques such as the syntax-oriented hierarchical analysis, optimization and yield driven design, to handle nonlinear as well as linear circuits. Our novel sensitivity analysis approach has been verified by a MESFET mixer example exhibiting 98% saving of CPU time over the prevailing perturbation method.

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I. INTRODUCTION

In this paper, we present a unified approach to the simulation and sensitivity analysis of linear/nonlinear circuits in the frequency domain. The linear part of the circuit can be large and can be hierarchically decomposed, highly suited to modern microwave CAD. Analysis of the nonlinear part is performed in the time domain and the large signal steady-state periodic analysis of the overall circuit is carried out by means of the harmonic balance (HB) method.

The HB method has become an important tool for the analysis of nonlinear circuits. The work of Rizzoli et al. [1], Curtice and Ettenberg [2], Curtice [3,4], Gilmore and Rosenbaum [5], Gilmore [6], Camacho-Penalosa and Aitchison [7] stimulated work on HB in the microwave CAD community. The excellent paper of Kundert and Sangiovanni-Vincentelli [8] provided systematic insight into the HB method. Many others, e.g., [9-15], have also contributed substantially to the state-of-the-art of the HB technique. The first step towards design optimization was made by Rizzoli et al. [1] who used the perturbation method to approximate the gradients. A recent review of this area was given by Rizzoli and Neri [16].

In our paper, we extend to nonlinear circuits the powerful adjoint network concept, a standard sensitivity analysis approach in linear circuits. The concept involves solving a set of linear equations whose coefficient matrix is available in many existing HB programs. The solution of a single adjoint system is sufficient for the computation of sensitivities w.r.t. all parameters in both the linear and nonlinear subnetworks, in the bias circuit, driving sources and terminations. No parameter perturbation or iterative simulations are required.

To make our theory highly suitable for microwave oriented CAD programs, we have also developed a hierarchical treatment of the adjoint system analysis. Preferred by leading experts, e.g., Jansen [17], and used in circuit simulators such as Super-Compact and Touchstone, the syntax-oriented hierarchical approach has proven very convenient and efficient in analyzing linear circuits. Our theory further extends such an approach to adjoint sensitivity analysis.

The sensitivities we propose are exact in terms of the harmonic balance method itself. Our exact adjoint sensitivity analysis can be used with various existing HB simulation techniques, e.g., the basic HB [8], the modified HB [6] and the APFT HB [15]. The only computational effort includes solving the adjoint linear equations and calculating the Fourier transforms of all time-domain derivatives at the nonlinear element level. Significant CPU time savings are achieved over the perturbation method.

In Section II, we define the notation used throughout this paper. In Section III, the simulation of linear and nonlinear circuits is reviewed under a general circuit hierarchy. In Section IV, a new and unified treatment to adjoint systems for linear and nonlinear circuits is introduced. Novel sensitivity formulas for nonlinear circuits are derived in Section V. Finally, in Section VI, a MESFET mixer example is used to verify our theory.

II. NOTATION AND DEFINITION

We follow the notation of [8]. Real vectors containing voltages and currents at time t are denoted by $\mathbf{v}(t)$ and $\mathbf{i}(t)$. Capitals $\mathbf{V}(k)$ and $\mathbf{I}(k)$ are used to indicate complex vectors of voltages and currents at harmonic k. A subscript t at $\mathbf{V}_t(k)$ indicates that the vector contains the nodal voltage at all N_t nodes (both internal and external) of a linear subnetwork. If there is no subscript, then the vector corresponds to the port voltages (currents) at all N ports of the reduced subnetwork. A bar denotes the split real and imaginary parts of a complex vector. In particular, $\overline{V}$ or $\overline{I}$ are real vectors containing the real and the imaginary parts of V(k) or I(k), respectively, for all harmonics k, k = 0, 1, ..., H-1. The total number of harmonics taken into consideration, including DC, is H. The hat distinguishes quantities of the adjoint system. For example, $\hat{V}_t(k)$ represents adjoint voltages at internal and external nodes of a subnetwork at harmonic k. A detailed definition of the notation is given in Table I.

III. LINEAR AND NONLINEAR SIMULATION

Circuit Structure

Our exact adjoint sensitivity analysis can be used for hierarchically structured linear subcircuits. Consider the arbitrary circuit hierarchy of Fig. 1. A typical subnetwork containing internal and external nodes is shown in Fig. 2. A general representation of a terminated circuit is depicted in Fig. 3. An unpartitioned or nonhierarchical approach is a special case of Fig. 1 when only one level exists.

For a completely linear circuit, the sources and loads are applied at the highest level of the hierarchy, as depicted in Fig. 3. For a nonlinear circuit, the linear part of the overall circuit can have an arbitrary hierarchy as illustrated by Fig. 1 while the nonlinear part is connected directly at the highest level to the linear part. Therefore, in any case we consider an unterminated N-port circuit at the highest level of hierarchy. Such an approach simultaneously facilitates both the effect of the reference plane in microwave circuits and the need for the harmonic balance equations.

Hierarchical Simulation of the Linear Network

Hierarchical simulation of linear circuits has been successfully used in many microwave CAD packages. It is summarized and expanded here into a set of formulas, enabling voltage responses at any nodes (internal or external) for any subnetwork at any level to be systematically computed. Firstly, we solve the terminated circuit at the highest level of the hierarchy using

$$\left\{ \begin{bmatrix} 1 & 0 \\ 0 & Y_s(k) \end{bmatrix} + \begin{bmatrix} Z_s(k) & 0 \\ 0 & 1 \end{bmatrix} Y(k) \right\} V(k) = \begin{bmatrix} V_s(k) \\ I_s(k) \end{bmatrix}, \tag{1}$$

where the overall quantity in the curly bracket is an N by N matrix linking the port voltages V(k) with the external sources for the terminated circuit. As defined in Table I, $Y_s(k)$ and $Z_s(k)$ are diagonal matrices containing terminating admittances or impedances, respectively, of the circuit shown in Fig. 3. Y(k) is the admittance matrix of the unterminated circuit. $V_s(k)$ and $I_s(k)$ denote the voltage and current excitations of the circuit, respectively. The solution vector V(k) contains external voltages of the circuit block under consideration. Then, all (both internal and external) nodal voltages $V_t(k)$ of this subnetwork can be obtained from the equation

$$A(k) \begin{bmatrix} V_t(k) \\ I(k) \end{bmatrix} = \begin{bmatrix} 0 \\ V(k) \end{bmatrix}, \tag{2}$$

where A(k) is the modified nodal admittance matrix of the subnetwork as defined in Table I. I(k) represents currents into the subcircuit through its external ports.

The solution of (2), i.e., $V_t(k)$ provides external voltages of all the subnetworks at the next level down the hierarchy. Therefore, (2) is used iteratively for the 1st, 2nd, ..., levels of the hierarchy until all desired nodal voltages are found.

Our formulas can directly accommodate both open and short circuit terminations. For example, a short circuit termination at port 1 simply means

$Z_1 = 0$ in the matrix $\mathbf{Z}_s$ in (1). An open circuit termination at port n_E+2 simply means $Y_2 = 0$ in the matrix $\mathbf{Y}_s$ in (1).

Simulation of Nonlinear Circuits

The frequency domain simulation of a nonlinear circuit is done effectively by the harmonic balance technique [1-16]. The problem is to find a $\overline{\mathbf{V}}$ such that

$$\overline{\mathbf{F}}(\overline{\mathbf{V}}) \triangleq \overline{\mathbf{I}}_{NL}(\overline{\mathbf{V}}) + \overline{\mathbf{I}}_L(\overline{\mathbf{V}}) = \mathbf{0} \; , \tag{3}$$

where the vectors $\overline{\mathbf{I}}_L$ and $\overline{\mathbf{I}}_{NL}$ are defined as the currents into the linear and nonlinear parts at the ports of their connection. $\overline{\mathbf{V}}$ contains the split real and imaginary parts of voltages as defined in Table I. The Newton update for solving (3) is

$$\overline{\mathbf{V}}_{new} = \overline{\mathbf{V}}_{old} - \overline{\mathbf{J}}^{-1}\overline{\mathbf{F}}(\overline{\mathbf{V}}_{old}) \; , \tag{4}$$

where $\overline{\mathbf{J}}$ is the Jacobian matrix defined by

$$\overline{\mathbf{J}} \triangleq (\partial \overline{\mathbf{F}}^T / \partial \overline{\mathbf{V}})^T \; . \tag{5}$$

The (i, j)th entry of the Jacobian matrix $\overline{\mathbf{J}}$ is the derivative of the ith entry of $\overline{\mathbf{F}}$ w.r.t. the jth entry of $\overline{\mathbf{V}}$.

In the context of the overall hierarchical structure, the solution of (3) provides the external voltages V(k), k = 0, 1, ..., H-1 at the highest level of the linear part. The desired internal and external voltages at all levels of the hierarchy can be solved by using (2) iteratively.

IV. ADJOINT SYSTEM SIMULATION

Efficient and exact sensitivity analysis can be achieved via solving an adjoint system. In this section, a new and unified formulation of adjoint systems for hierarchically structured linear/nonlinear circuits is presented.

Adjoint System for Linear Networks

At the highest level of the hierarchy, the adjoint systems is excited by a unit source at the output port. Suppose the output voltage V_{out} can be selected from V(k) by an N-vector **e** as

$$V_{out} = \mathbf{e}^T V(k) . \tag{6}$$

For example, if V_{out} is chosen as the voltage at the first port then the vector **e** contains 1 as the first entry and zeros everywhere else. By solving

$$\{ \begin{bmatrix} 1 & 0 \\ 0 & Y_s(k) \end{bmatrix} + \begin{bmatrix} Z_s(k) & 0 \\ 0 & 1 \end{bmatrix} Y^T(k) \} \hat{V}(k) = \mathbf{e} , \tag{7}$$

we obtain adjoint voltages $\hat{V}(k)$ at external ports at the highest level of the hierarchy. $Y_s(k)$, $Z_s(k)$ and Y(k) are the same matrices as used in (1). In order to obtain adjoint voltages $\hat{V}_t(k)$ at all (both internal and external) nodes of the circuit block, we solve the equation

$$A^T(k) \begin{bmatrix} \hat{V}_t(k) \\ -\hat{I}(k) \end{bmatrix} = \begin{bmatrix} 0 \\ -\hat{V}(k) \end{bmatrix} , \tag{8}$$

where $A^T(k)$ is the transpose of the modified nodal admittance matrix of the subnetwork as used in (2). The solution vector $\hat{V}_t(k)$ provides external adjoint voltages for all subnetworks at the next level down the hierarchy. Therefore, (8) can be used iteratively for the 1st, 2nd, ..., levels of the hierarchy until all desired adjoint voltages are found.

Notice that (8) is a convenient formulation of the adjoint system since the LU factors of A(k) can already be available from solving (2).

Adjoint System for Nonlinear Networks

Suppose $\overline{V}_{out}$ is the real or imaginary part of output voltage V_{out} and can be selected from the voltage vector $\overline{V}$ by a vector $\overline{\mathbf{e}}$ as

$$\overline{V}_{out} = \overline{\mathbf{e}}^T \overline{V} . \tag{9}$$

The adjoint system is the linear equation

$$\bar{J}^T \hat{V} = \bar{e} , \tag{10}$$

where $\bar{J}$ is the Jacobian at the solution of (3). Notice that $\bar{V}$ and $\hat{V}$ are both 2HN-vectors containing the split real and imaginary parts of voltages at the connection ports of the linear and nonlinear subcircuits. According to our notation $\bar{V}$ is defined for the original network and $\hat{V}$ is defined for the adjoint network. Also notice that the LU factors of $\bar{J}$ can be available from the last iteration of (4). Therefore, to obtain $\hat{V}$ from (10), we need only the forward and backward substitutions.

The adjoint voltages can be computed even if the output port is suppressed from the harmonic equation (3). Although the theoretical derivation for this case is rather involved, as given in Appendix A, we found a very logical and easy-to-implement method to handle this situation. First, we compute the adjoint voltages at the external ports of the linear subnetwork. This can be done by disconnecting the nonlinear part and then solving the linear part for individual harmonics separately. The resulting vector, denoted by $\hat{V}_L$, is then transformed to the actual adjoint excitations of the overall circuit (including both linear and nonlinear parts) to be incorporated to (10) in place of $\bar{e}$. The final equation takes the form

$$\bar{J}^T \hat{V} = \bar{Y}^T \hat{V}_L . \tag{11}$$

In (11), $\hat{V}$ and $\hat{V}_L$ have exactly the same dimensions and both represent the split real and imaginary parts of adjoint voltages at the connection ports of the linear and nonlinear subcircuits. The former is computed from the overall circuit and the latter is computed from the linear subcircuit only.

Equations (10) or (11) provide adjoint voltages at external ports at the highest level of the hierarchy. We then use (8) iteratively for the 1st, 2nd, ..., levels of the hierarchy to obtain adjoint voltages at both internal and external nodes of all subnetworks.

V. SENSITIVITY ANALYSIS

Adjoint System Approach to Sensitivity Evaluation

Let x be a design variable of the nonlinear circuit. Differentiating (3) w.r.t. x gives

$$(\partial \overline{\mathbf{F}}^T/\partial \overline{\mathbf{V}})^T(\partial \overline{\mathbf{V}}/\partial x) + (\partial \overline{\mathbf{F}}/\partial x) = \mathbf{0} \tag{12}$$

or

$$\partial \overline{\mathbf{V}}/\partial x = -\overline{\mathbf{J}}^{-1}(\partial \overline{\mathbf{F}}/\partial x) . \tag{13}$$

where $\overline{\mathbf{J}}$ has been defined in (5). Premultiplying (13) by $\overline{\mathbf{e}}^T$ results in

$$\begin{aligned} \partial \overline{V}_{out}/\partial x &= -\overline{\mathbf{e}}^T\overline{\mathbf{J}}^{-1}(\partial \overline{\mathbf{F}}/\partial x) \\ &= -\hat{\overline{\mathbf{V}}}^T(\partial \overline{\mathbf{F}}/\partial x) . \end{aligned} \tag{14}$$

This expression is further simplified by considering the locations of x in $\overline{\mathbf{F}}$. Notice that each entry of vector $\overline{\mathbf{F}}$ corresponds to a port and to a harmonic of the circuit. Take, for instance, a nonlinear resistor described by i(t) = i(v(t), x) and connected across the jth port. x enters $\overline{\mathbf{F}}$ at the positions relating to port j and harmonic k, k = 0, 1, ..., H-1, by the Fourier transform of i(v(t), x). In this case, (14) is simplified to

$$\partial \overline{V}_{out}/\partial x = -\sum_k \text{Real}\,[\hat{V}_j(k)G^*(k)] , \tag{15}$$

where $\hat{V}_j(k)$ is the adjoint voltage at the jth port, G(k) is the kth Fourier coefficient of $\partial i/\partial x$ and superscript * denotes the complex conjugate.

Sensitivity Expressions

Suppose a variable x belongs to branch b. We have derived the following general formula for computing the exact sensitivity of V_{out} w.r.t. x,

$$
\frac{\partial \overline{V}_{out}}{\partial x} = \begin{cases} -\sum_k \text{Real}\,[\hat{V}_b(k) V_b^*(k) G_b^*(k)] & \text{if } x \in \text{linear subnetwork} \quad (16a) \\ -\sum_k \text{Real}\,[\hat{V}_b(k) G_b^*(k)] & \text{if } x \in \text{nonlinear VCCS or nonlinear resistor or real part of a complex driving source} \quad (16b) \\ -\sum_k \text{Imag}\,[\hat{V}_b(k) G_b^*(k)] & \text{if } x \in \text{nonlinear capacitor or imaginary part of a complex driving source.} \quad (16c) \end{cases}
$$

Complex quantities $V_b(k)$ and $\hat{V}_b(k)$ are the voltages of branch b at harmonic k and are obtained from vectors $V_t(k)$ and $\hat{V}_t(k)$, respectively. $G_b(k)$ denotes the sensitivity expression of the element containing variable x. For example, if x is the conductance of a linear resistor, $G_b(k) = 1$. If x belongs to a nonlinear resistor represented by $i = i(v(t), x)$, $G_b(k)$ is the <u>kth Fourier coefficient</u> of $\partial i/\partial x$. A list of various cases of $G_b(k)$ is given in Table II.

Our sensitivity formula (16) has no restrictions on the selection of harmonic frequencies or the time samples. In a multi-tone case, the index k in (16) corresponds to all the harmonics used in the harmonic equation (3). When the multidimensional Fourier transform is used, we simply place a multidimensional summation in (16).

Notice that our sensitivity formulas permit variable x to appear in any subcircuit at any level of the hierarchy since all required voltages can be calculated as needed.

<u>Comparison with the Perturbation Method</u>

To approximate the sensitivities using the traditional perturbation method, one needs a circuit simulation for each variable. The best possible situation for this method is that all simulations finish in one iteration. For our exact adjoint sensitivity analysis, the major computation, i.e., solving the adjoint equations, is done only once for <u>all</u> variables. A detailed comparison reveals that the worst case for our approach takes less computation than the best situation of the perturbation method. In our experiment, we used only

1.6% of the CPU time required by the perturbation method to obtain all sensitivities.

Gradient Vector for Optimization

The novel formula (16) can be used as a key to formulate the gradient vectors for design optimization and yield maximization of nonlinear circuits. Table III lists the gradients of a FET mixer conversion gain w.r.t. various variables, expressed as simple functions of $\partial V_{out}/\partial x$.

VI. EXAMPLES

Example 1: Hierarchical Circuit Description

Many researchers, e.g., [3, 7] have used FET mixer examples to test harmonic balance simulators. Here, we describe a mixer under the framework of hierarchical analysis. Such a description fits in with existing commercial software such as Super-Compact. The overall nonlinear circuit with its biasing and driving sources is described by a Super-Compact like circuit file as follows.

```
*   HIERARCHICAL ANALYSIS OF A MESFET MIXER
BLOCK
*   INPUT MATCHING AND GATE BIAS SUBNETWORK
    IND   3  4  L=15NH
    IND   2  3  L=.5NH
    CAP   3  0  C=2.2PF
    CAP   1  2  C=2.2PF
    IND   2  5  L=.55NH
*   DEFINE THE SUBCIRCUIT AS A 3-PORT
    CKT1:  3PORT 1  4  5
END
BLOCK
*   OUTPUT MATCHING AND DRAIN BIAS SUBNETWORK
    IND   2  3   L=15NH
    IND   1  2   L=1.1NH
    CAP   2  0   C=20PF
    CAP   1  4   C=20PF
*   DEFINE THE SUBCIRCUIT AS A 3-PORT
    CKT2:  3PORT 1  4  3
END
```

```
BLOCK
*   THE HIGHEST HIERARCHY
    CKT1   1   3   5
    CKT2   7   2   4
    CAP    6           C=2PF
*   A TRANSMISSION LINE BETWEEN PORT 6 0 AND PORT 7 0
    MIC    6   7
*   BIAS SOURCES
    BIAS   3    V=-.9
    BIAS   4    V=3.
*   NONLINEAR FET
*   NODE NUMBERS REFER TO GATE, DRAIN AND SOURCE
    NFET   5   6   0
END
FREQUENCIES
*   DEFINE LO FREQUENCY
    TONE 1
    11GHZ
*   DEFINE RF FREQUENCY
    TONE 2
    12GHZ
END
SOURCES
*   DEFINE LO DRIVING SOURCE
    TONE 1
    POWER  1   0   P=7DBM
*   DEFINE RF DRIVING SOURCE
    TONE 2
    POWER  1   0   P=-15DBM
END
```

The LO and RF input matching and the gate bias circuits are analyzed separately in subnetwork CKT1. The IF output matching and drain bias circuits are analyzed in subnetwork CKT2. These subnetworks are then connected to a higher level of the hierarchy formulating an unterminated circuit block. This circuit block is then connected to nonlinear device ports. Using formulas developed in Sections III and IV, we are able to hierarchically simulate the original circuit as well as the adjoint circuit. This is a direct realization of the syntax-oriented step-by-step topological description [17], permitting the sensitivity analysis of a large circuit to be performed by solving a set of small original and adjoint systems.

Example 2: Simulation and Sensitivity Analysis of a MESFET Mixer

The MESFET mixer example reported in [7] was used to verify our theory. Figs. 4 and 5 show the large-signal MESFET model and the DC characteristics of the device. The frequencies are f_{LO} = 11 GHz, f_{RF} = 12 GHz and f_{IF} = 1 GHz. The DC bias voltages are V_{GS} = −0.9 V and V_{DS} = 3.0 V. With LO power P_{LO} = 7 dBm and RF power P_{RF} = −15 dBm, the conversion gain was 6.4 dB. 26 variables were considered including all parameters in the linear as well as the nonlinear parts, DC bias, LO power, RF power, IF, LO and RF terminations. Exact sensitivities of the conversion gain w.r.t. all the variables are computed using our novel theory. The results were in excellent agreement with those from the perturbation method, as shown in Table IV. The circuit was solved in 22 seconds on a VAX 8600. The CPU time for sensitivity analysis using our method and the perturbation method are 3.7 seconds and 240 seconds, respectively.

The dangling node between the nonlinear elements C_{gs} and R_i, a case which could cause trouble in HB programs, is directly accommodated in our approach.

We have plotted selected sensitivities vs. LO power in Fig. 6. For example, as LO power is increased, conversion gain becomes less sensitive to changes in gate bias V_{GS}.

VII. CONCLUSIONS

This paper presents a unified theory for frequency domain simulation and sensitivity analysis of linear and nonlinear circuits. Our formula (16a) encompasses the adjoint network approach in the frequency domain [18,19], a standard for exact sensitivity analysis of linear circuits, as a special case. Since the simulation of nonlinear circuits is expensive, gradient approximations for nonlinear circuits using repeated simulation is very costly. Consequently, the adjoint sensitivity analysis becomes far more significant for nonlinear circuits than for linear ones.

The hierarchical approach widely used for circuit simulation is generalized for sensitivity analysis and for computing responses in any subnetwork at any level of the hierarchy. Therefore, important aspects of frequency domain circuit CAD such as simulation and sensitivity analysis, linear and nonlinear circuits, hierarchical and nonhierarchical approaches, voltage and current excitations, or open and short circuit terminations are unified in this general framework.

Our theory provides a key for the coming generation of microwave CAD software. It can take advantage of many existing and mature techniques such as the syntax-oriented hierarchical analysis, optimization and yield driven design, to handle linear as well as nonlinear circuits.

Our novel sensitivity analysis approach has been verified by a MESFET mixer example exhibiting 98% saving of CPU time over the prevailing perturbation method.

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APPENDIX A

Derivation of Equation (11)

Suppose

$$\overline{\mathbf{V}}_{out} = \overline{\mathbf{e}}_t^T \overline{\mathbf{V}}_t \,. \tag{A1}$$

The harmonic balance equations can be formulated w.r.t. all nodes of the circuit, i.e., without suppressing the internal nodes in a single level description of the circuit. In such a case the Jacobian matrix $\overline{\mathbf{J}}_t$ can be defined similarly to (5), and

$$\overline{\mathbf{J}}_t = \overline{\mathbf{Y}}_t + \mathbf{Q}\mathbf{D}^T\mathbf{P}^T \,, \tag{A2}$$

where $\mathbf{D}$ is a 2HN × 2HN matrix representing the contribution to $\overline{\mathbf{J}}$ from nonlinear components, i.e.,

$$\overline{\mathbf{J}} = \overline{\mathbf{Y}} + \mathbf{D}^T \,. \tag{A3}$$

Matrices $\mathbf{P}$ and $\mathbf{Q}$ are $2HN_t \times 2HN$ incidence matrices containing 0's and ±1's.

Let

$$\mathbf{T} = \overline{\mathbf{Y}}_t^T \,. \tag{A4}$$

Similarly to (9) and (10), based on (A1) the adjoint voltages at both internal and external nodes can be computed as

$$\hat{\overline{\mathbf{V}}}_t \triangleq (\overline{\mathbf{J}}_t^T)^{-1}\overline{\mathbf{e}}_t = (\mathbf{T} + \mathbf{P}\mathbf{D}\mathbf{Q}^T)^{-1}\overline{\mathbf{e}}_t \,. \tag{A5}$$

Applying the Householder formula [20] to (A5) we have

$$\hat{\overline{\mathbf{V}}}_t = \mathbf{T}^{-1}\overline{\mathbf{e}}_t - \mathbf{T}^{-1}\mathbf{P}\,(\mathbf{D}^{-1} + \mathbf{Q}^T\mathbf{T}^{-1}\mathbf{P})^{-1}\mathbf{Q}^T\mathbf{T}^{-1}\overline{\mathbf{e}}_t \,. \tag{A6}$$

Notice that

$$(\overline{\mathbf{Y}}^T)^{-1} = \mathbf{Q}^T\mathbf{T}^{-1}\mathbf{P} \,. \tag{A7}$$

Let

$$\mathbf{X} = \overline{\mathbf{Y}}^T \,, \tag{A8}$$

$$\hat{\overline{\mathbf{V}}}_L = \mathbf{Q}^T\mathbf{T}^{-1}\,\overline{\mathbf{e}}_t \,. \tag{A9}$$

Premultiplying (A6) by $\mathbf{Q}^T$ gives

$$\hat{\overline{\mathbf{V}}} \triangleq \mathbf{Q}^T\hat{\overline{\mathbf{V}}}_t = \hat{\overline{\mathbf{V}}}_L - \mathbf{X}^{-1}(\mathbf{D}^{-1} + \mathbf{X}^{-1})^{-1}\hat{\overline{\mathbf{V}}}_L \,. \tag{A10}$$

Again, using the Householder formula [20],

$$(\mathbf{D}^{-1} + \mathbf{X}^{-1})^{-1} = \mathbf{X} - \mathbf{X}(\mathbf{D} + \mathbf{X})^{-1}\mathbf{X} \tag{A11}$$

and substituting (A3) and (A8) into (A10) we get

$$\hat{\mathbf{V}} = (\overline{\mathbf{J}}^{T})^{-1}\overline{\mathbf{Y}}^{T}\hat{\mathbf{V}}_{L} \tag{A12}$$

or

$$\overline{\mathbf{J}}^{T}\hat{\mathbf{V}} = \overline{\mathbf{Y}}^{T}\hat{\mathbf{V}}_{L} \,. \tag{A13}$$

REFERENCES

[1] V. Rizzoli, A. Lipparini and E. Marazzi, "A general-purpose program for nonlinear microwave circuit design", *IEEE Trans. Microwave Theory Tech.*, vol. MTT-31, pp. 762-769, 1983.

[2] W.R. Curtice and M. Ettenberg, "A nonlinear GaAs FET model for use in the design of output circuits for power amplifiers", *IEEE Trans. Microwave Theory Tech.*, vol. MTT-33, pp. 1383-1394, 1985.

[3] W.R. Curtice, "Nonlinear analysis of GaAs MESFET amplifiers, mixers, and distributed amplifiers using the harmonic balance technique", *IEEE Trans. Microwave Theory Tech.*, vol MTT-35, pp. 441-447, 1987.

[4] W.R. Curtice, "GaAs MESFET modeling and nonlinear CAD", *IEEE Trans. Microwave Theory Tech.*, vol. MTT-36, pp. 220-230, 1988.

[5] R.J. Gilmore and F.J. Rosenbaum, "Modelling of nonlinear distortion in GaAs MESFET's", *IEEE Int. Microwave Symp. Digest* (San Francisco, CA), pp. 430-431, 1984.

[6] R. Gilmore, "Nonlinear circuit design using the modified harmonic balance algorithm", *IEEE Trans. Microwave Theory Tech.*, vol. MTT-34, pp. 1294-1307, 1986.

[7] C. Camacho-Penalosa and C.S. Aitchison, "Analysis and design of MESFET gate mixers", *IEEE Trans. Microwave Theory Tech.*, vol. MTT-35, pp. 643-652, 1987.

[8] K.S. Kundert and A. Sangiovanni-Vincentelli, "Simulation of nonlinear circuits in the frequency domain", *IEEE Trans. Computer-Aided Design*, vol. CAD-5, pp. 521-535, 1986.

[9] S. Egami, "Nonlinear, linear analysis and computer-aided design of resistive mixers", *IEEE Trans. Microwave Theory Tech.*, vol. MTT-22, pp. 270-275, 1974.

[10] F. Filicori, V.A. Monaco and C. Naldi, "Simulation and design of microwave class-C amplifiers through harmonic analysis", *IEEE Trans. Microwave Theory Tech.*, vol. MTT-27, pp. 1043-1051, 1979.

[11] R.G. Hicks and P.J. Khan, "Numerical analysis of subharmonic mixers using accurate and approximate models", *IEEE Trans. Microwave Theory Tech.*, vol. MTT-30, pp. 2113-2120, 1982.

[12] C. Camacho-Penalosa, "Numerical steady-state analysis of nonlinear microwave circuits with periodic excitation", *IEEE Trans. Microwave Theory Tech.*, vol. MTT-31, pp. 724-730, 1983.

[13] M.S. Nakhla and J. Vlach, "A piecewise harmonic balance technique for determination of periodic response of nonlinear systems", *IEEE Trans. Circuits Syst.*, vol. CAS-23, pp. 85-91, 1976.

[14] A. Ushida and L.O. Chua, "Frequency-domain analysis of nonlinear circuits driven by multi-tone signals", *IEEE Trans. Circuits Syst.*, vol. CAS-31, pp. 766-779, 1984.

[15] K.S. Kundert, G.B. Sorkin and A. Sangiovanni-Vincentelli, "Applying harmonic balance to almost-periodic circuits", *IEEE Trans. Microwave Theory Tech.*, vol. MTT-36, pp. 366-378, 1988.

[16] V. Rizzoli and A. Neri, "State of the art and present trends in nonlinear microwave CAD techniques", *IEEE Trans. Microwave Theory Tech.*, vol. MTT-36, pp. 343-365, 1988.

[17] R.H. Jansen, "Computer-aided design of hybrid and monolithic microwave integrated circuits - state of the art, problems and trends", *Proc. European Microwave Conf.*, (Nurnberg, West Germany), pp. 67-78, 1983.

[18] S.W. Director and R.A. Rohrer, "The generalized adjoint network and network sensitivities", *IEEE Trans. Circuit Theory*, vol. CT-16, pp. 318-323, 1969.

[19] L.O. Chua and P.M. Lin, *Computer-Aided Analysis of Electronic Circuits.* Englewood Cliffs, NJ: Prentice-Hall, 1975.

[20] A.S. Householder, "A survey of some closed methods for inverting matrices", *SIAM J.*, vol. 5, pp. 155-169, 1957.

TABLE I

NOTATION AND DEFINITION

Notation	Definition
N_t	total number of nodes (internal and external) of a linear subnetwork.
N	number of circuit nodes (or ports) used in harmonic analysis. Also, it is the number of external nodes for a typical subnetwork of Fig. 2.
H	number of harmonics, including DC.
k	harmonic index. k = 0 for DC, k = 1 for the fundamental harmonic, k = 2, 3, ..., H-1 for other harmonics.
$\mathbf{V}_t(k)$, $\mathbf{I}_t(k)$	complex N_t-vectors indicating kth harmonic voltages or currents at all nodes (both internal and external) of a linear subnetwork.
$\mathbf{V}(k)$, $\mathbf{I}(k)$	complex N-vectors indicating kth harmonic voltages or currents at all external nodes of any linear subnetwork (at the highest level of hierarchy the nodes or ports at which the harmonic balance equations are formulated).
$\overline{\mathbf{V}}_t$, $\overline{\mathbf{I}}_t$	real $2HN_t$-vectors containing real and imaginary parts of $\mathbf{V}_t(k)$ or $\mathbf{I}_t(k)$ at all harmonics k, k = 0, 1, ..., H-1.
$\overline{\mathbf{V}}$, $\overline{\mathbf{I}}$	real 2HN-vectors containing real and imaginary parts of $\mathbf{V}(k)$ or $\mathbf{I}(k)$ at all harmonics k, k = 0, 1, ..., H-1.
$\mathbf{Y}_t(k)$	N_t by N_t matrix representing the unreduced nodal admittance matrix of a linear subnetwork at harmonic k.
$\mathbf{Y}(k)$	N by N matrix representing the reduced nodal admittance matrix of a linear subnetwork at harmonic k.

TABLE I (continued)

NOTATION AND DEFINITION

Notation	Definition
$\overline{\mathbf{Y}}_t$	$2HN_t$ by $2HN_t$ real matrix obtained by splitting the real and imaginary parts of $\mathbf{Y}_t(k)$ for all harmonics k, k = 0, 1, ..., H-1.
$\overline{\mathbf{Y}}$	2HN by 2HN real matrix obtained by splitting the real and imaginary parts of $\mathbf{Y}(k)$ for all harmonics k, k = 0, 1, ..., H-1.
$\overline{\mathbf{J}}_t$	$2HN_t$ by $2HN_t$ real matrix representing the Jacobian defined in (A2).
$\overline{\mathbf{J}}$	2HN by 2HN real matrix representing the Jacobian defined by (5). The internal nodes of the linear subcircuit are suppressed.
$\bar{\mathbf{e}}_t$	$2HN_t$ real vector selecting the output voltage from the vector $\overline{\mathbf{V}}_t$.
$\bar{\mathbf{e}}$	2HN real vector selecting the output voltage from the vector $\overline{\mathbf{V}}$.
$\mathbf{A}(k)$	$\begin{bmatrix} \mathbf{Y}_t(k) & -\mathbf{U} \\ \mathbf{U}^T & \mathbf{0} \end{bmatrix}$ where $\mathbf{U}$ is $\begin{bmatrix} \mathbf{0} \\ \mathbf{1} \end{bmatrix}$ and $\mathbf{1}$ is an N by N identity matrix.
$\mathbf{Z}_s(k)$	n_E by n_E diagonal matrix whose diagonal entries are the terminating impedances Z_i, i = 1, 2, ..., n_E.
$\mathbf{Y}_s(k)$	n_I by n_I diagonal matrix whose diagonal entries are the terminating admittances Y_i, i = 1, 2, ..., n_I.
$\mathbf{V}_s(k)$	n_E-vector containing voltage excitations E_i, i = 1, 2, ..., n_E.
$\mathbf{I}_s(k)$	n_I-vector containing current excitations I_{si}, i = 1, 2, ..., n_I.

TABLE II

SENSITIVITY EXPRESSIONS AT THE ELEMENT LEVEL

Type of Element*	Expression for $G_b(k)$	Applicable Equation
linear conductor G	1	(16a)
linear resistor R	$-1/R^2$	(16a)
linear capacitor C	$j\omega_k$	(16a)
linear inductor L	$-1/(j\omega_k L^2)$	(16a)
nonlinear VCCS or nonlinear resistor described by $i = i(\mathbf{v}(t),x)$	[kth Fourier coefficient of $\partial i/\partial x$]	(16b)
nonlinear capacitor described by $q = q(\mathbf{v}(t),x)$	ω_k [kth Fourier coefficient of $\partial q/\partial x$]	(16c)
current driving source	1	(16b) or (16c)+
voltage driving source	1/(source impedance)	(16b) or (16c)+

* the element is located in branch b and contains the variable x.

\+ (16b) is used if x is the real part of the driving source.
(16c) is used if x is the imaginary part of the driving source.

ω_k is the kth harmonic frequency used in the harmonic equation (3)

TABLE III

GRADIENTS OF MIXER CONVERSION GAIN

Variable x	Gradient Expression
RF power	$c\ \mathrm{Real}\{(\partial V_{out}/\partial x)/V_{out}\} - 1$
$R_g(f_{RF})$	$c\ \mathrm{Real}\{(\partial V_{out}/\partial x)/V_{out}\} + c/(2R_g(f_{RF}))$
$R_d(f_{IF})$	$c\ \mathrm{Real}\{(\partial V_{out}/\partial x)/V_{out}$
	$- 1/(R_d(f_{IF}) + jX_d(f_{IF}))\} + c/(2R_d(f_{IF}))$
$X_d(f_{IF})$	$c\ \mathrm{Real}\{(\partial V_{out}/\partial x)/V_{out}$
	$- j/(R_d(f_{IF}) + jX_d(f_{IF}))\}$
any parameter other than above	$c\ \mathrm{Real}\{(\partial V_{out}/\partial x)/V_{out}\}$

$c = 20/\ell n10$

R and X represent the real and the imaginary parts of the impedance terminations, respectively. Subscripts g and d represent the gate and the drain terminations, respectively.

complex quantity $\partial V_{out}/\partial x$ is obtained by solving (9), (10) and (16) twice, once for the real part and the other for the imaginary part. The LU factors of $\bar{J}$ and the Fourier transforms of element sensitivities are common between the two operations.

TABLE IV

NUMERICAL VERIFICATION OF SENSITIVITIES OF THE MIXER

Location of Variables	Variable	Exact Sensitivity	Numerical Sensitivity	Difference (%)
linear	C_{ds}	2.23080	2.23042	0.02
subnetwork	C_{gd}	-29.44595	-29.44659	0.00
	C_{de}	0.00000	0.00000	0.03
	R_g	3.17234	3.17214	0.01
	R_d	6.42682	6.42751	0.01
	R_s	11.50766	11.50805	0.00
	R_{de}	-0.02396	-0.02412	0.66
	L_g	-0.50245	-0.50346	0.20
	L_d	-0.20664	-0.20679	0.07
	L_s	1.15334	1.15333	0.00
nonlinear	C_{gs0}	-6.17770	-6.17786	0.00
subnetwork*	τ	0.49428	0.49414	0.03
	V_ϕ	-20.85730	-20.85758	0.00
	V_{p0}	-26.48210	-26.48041	0.01
	V_{dss}	0.01064	0.01028	3.33
	I_{dsp}	9.93696	9.93680	0.00
bias and	V_{GS}	-31.62080	-31.62423	0.01
driving	V_{DS}	-2.17821	-2.17823	0.00
sources	P_{LO}	2.76412	2.76412	0.00
	P_{RF}	-0.05401	-0.05392	0.16

TABLE IV (continued)

NUMERICAL VERIFICATION OF SENSITIVITIES OF THE MIXER

Location of Variables	Variable	Exact Sensitivity	Numerical Sensitivity	Difference (%)
termina-tions	$R_g(f_{LO})$	0.06671	0.06657	0.22
	$X_g(f_{LO})$	0.37855	0.37854	0.00
	$R_g(f_{RF})$	0.78812	0.78798	0.02
	$X_g(f_{RF})$	0.45120	0.45119	0.00
	$R_d(f_{IF})$	0.71451	0.71436	0.02
	$X_d(f_{IF})$	0.10886	0.10871	0.14

* Nonlinear elements are characterized by

$$C_{gs}(v_1) = C_{gs0} \ / \ \sqrt{1-v_1/V_\phi},$$

$$R_i(v_1)C_{gs}(v_1) = \tau$$

and the function for $i_m(v_1, v_2)$ is shown in Fig. 5, whose mathematical expression is consistent with [7]. V_ϕ, V_{p0}, V_{dss} and I_{dsp} are parameters in the function $i_m(v_1, v_2)$.

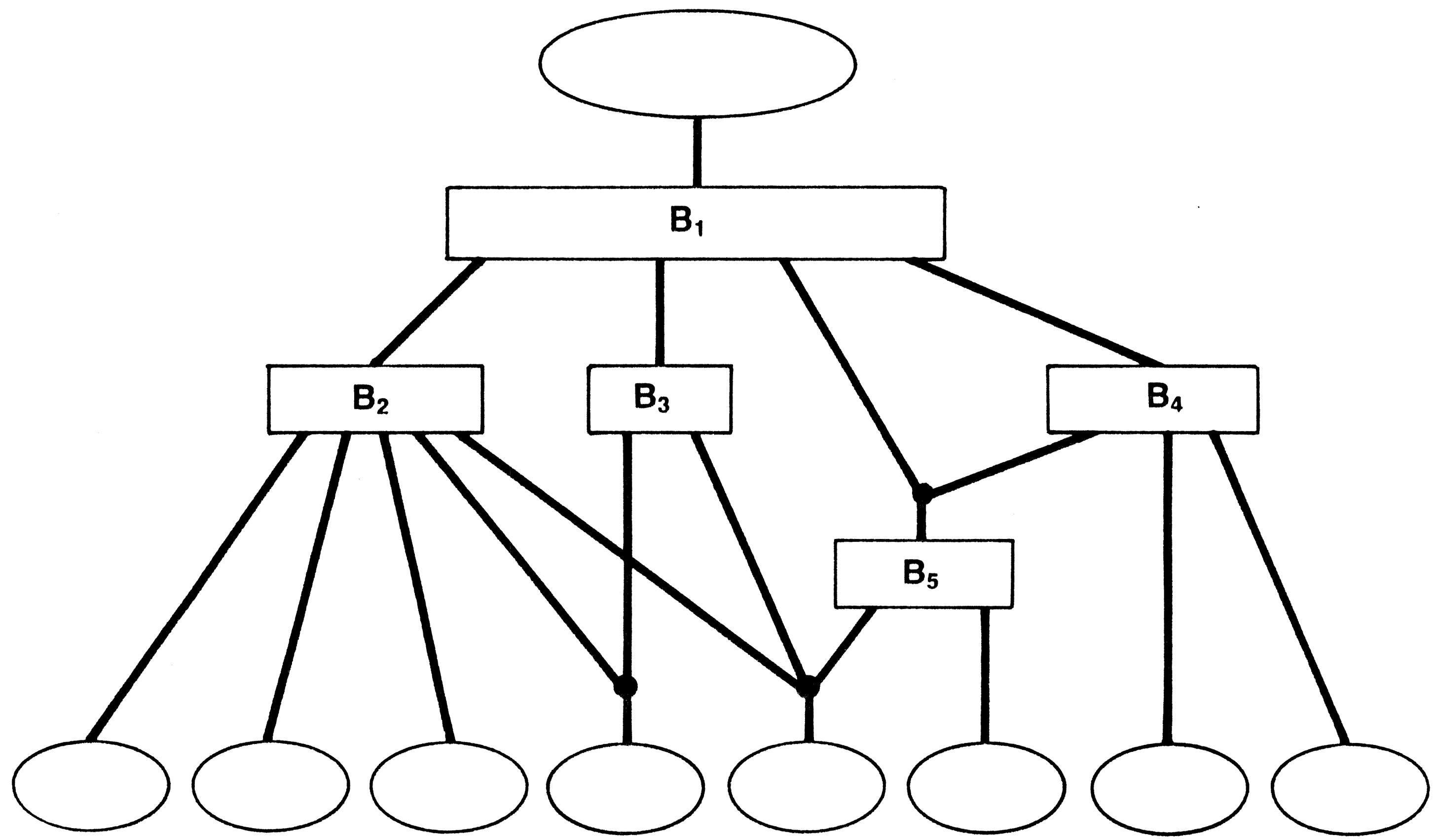
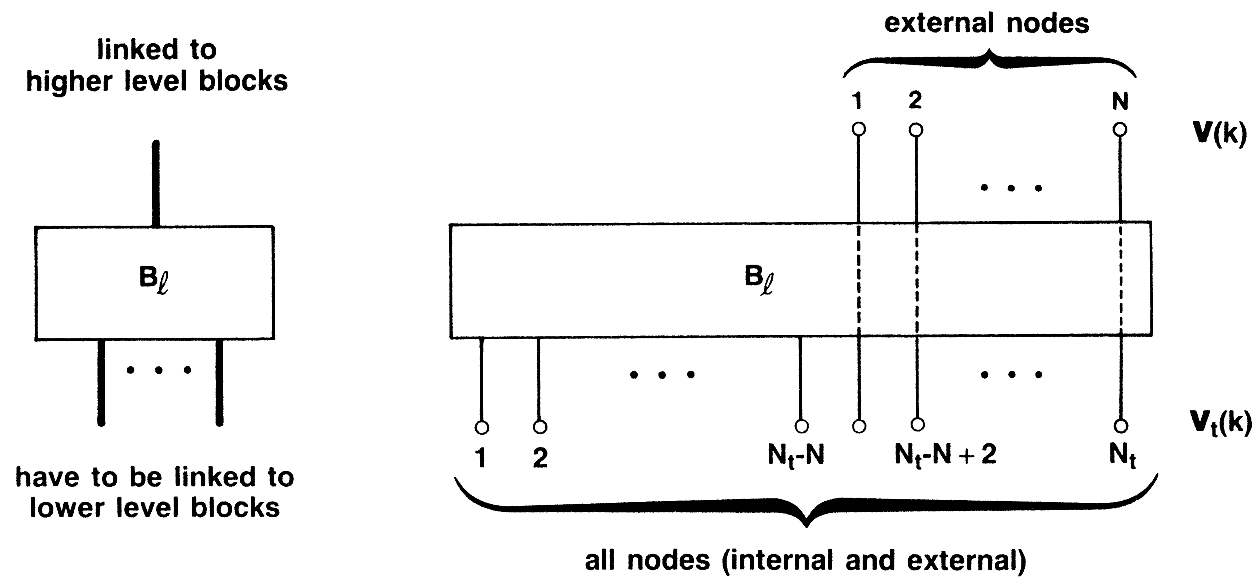


Fig. 1 An arbitrary circuit hierarchy. Each thick line represents a group of nodes. Each rectangular box represents a connection block for a subcircuit. Each bottom circular box represents a circuit element and the top circular box represents the sources and loads.



(a) (b)

Fig. 2 A typical subcircuit connection block: (a) as seen from Fig. 1, (b) detailed representation of all the nodes of the subnetwork. Nodes at the top (bottom) of the rectangular box are the external (external and internal) nodes of the subnetwork.

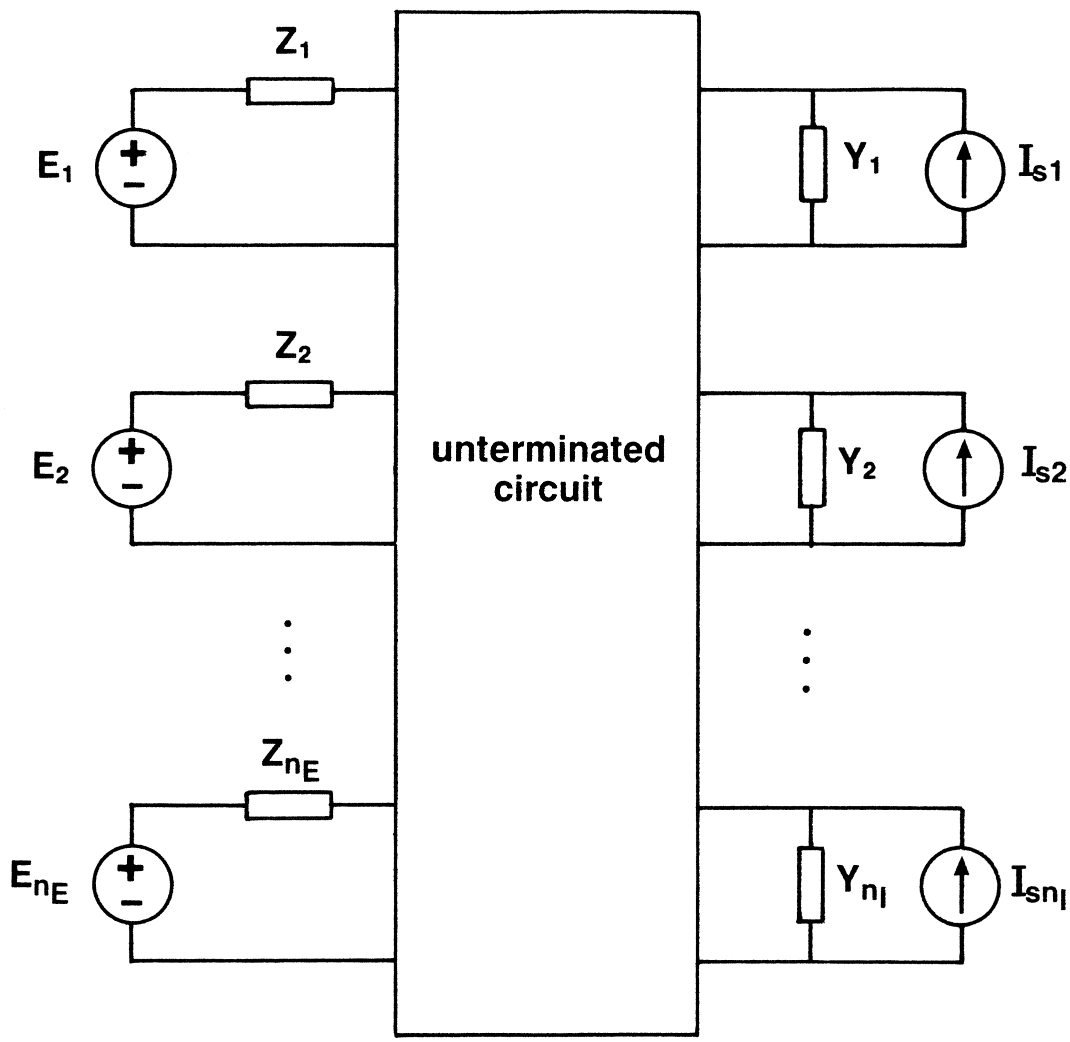


Fig. 3 A representation of a terminated subnetwork. Both current and voltage sources can be accommodated. The overall port sequence is such that ports 1, 2, ..., n_E correspond to voltage sources and ports n_E+1, n_E+2, ..., n_E+n_I correspond to current sources. The total number of ports is N, i.e., $N = n_E+n_I$.

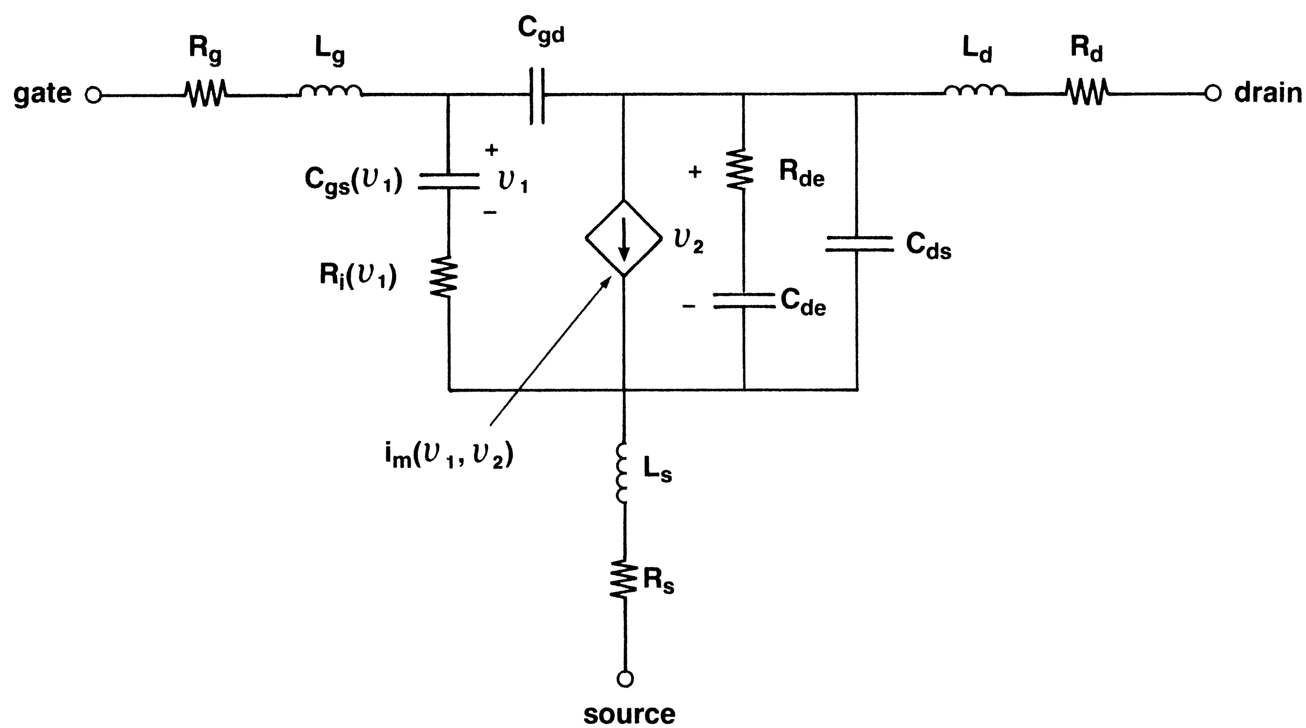


Fig. 4 A large signal MESFET model. All parameter values are consistent with [7].

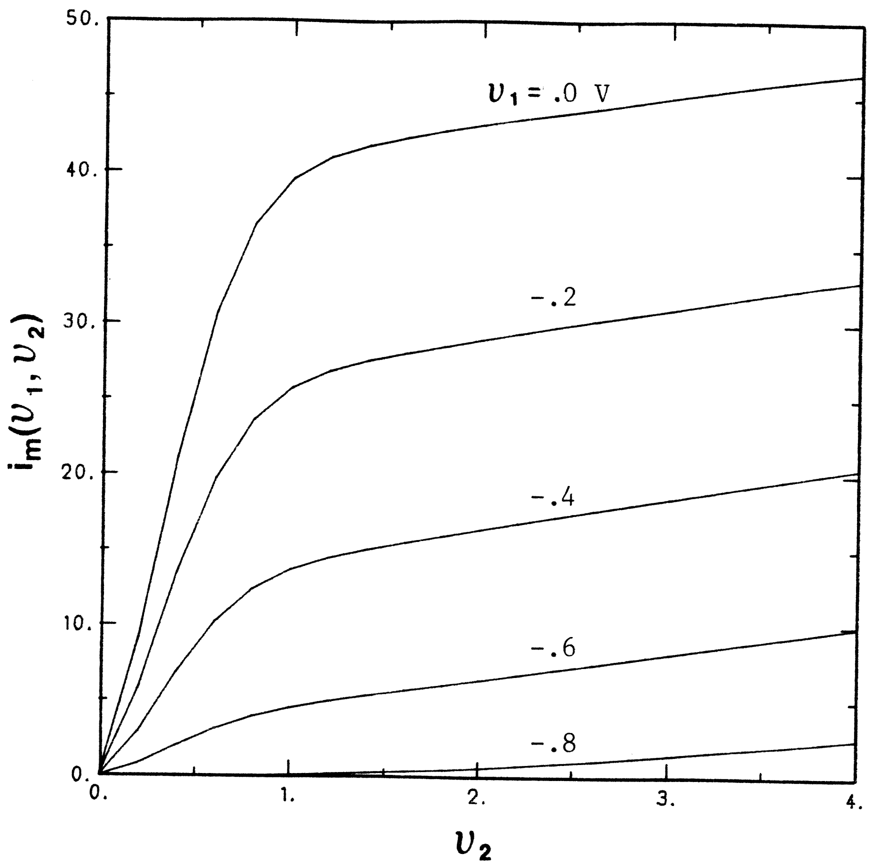


Fig. 5 The DC characteristics of the MESFET model.

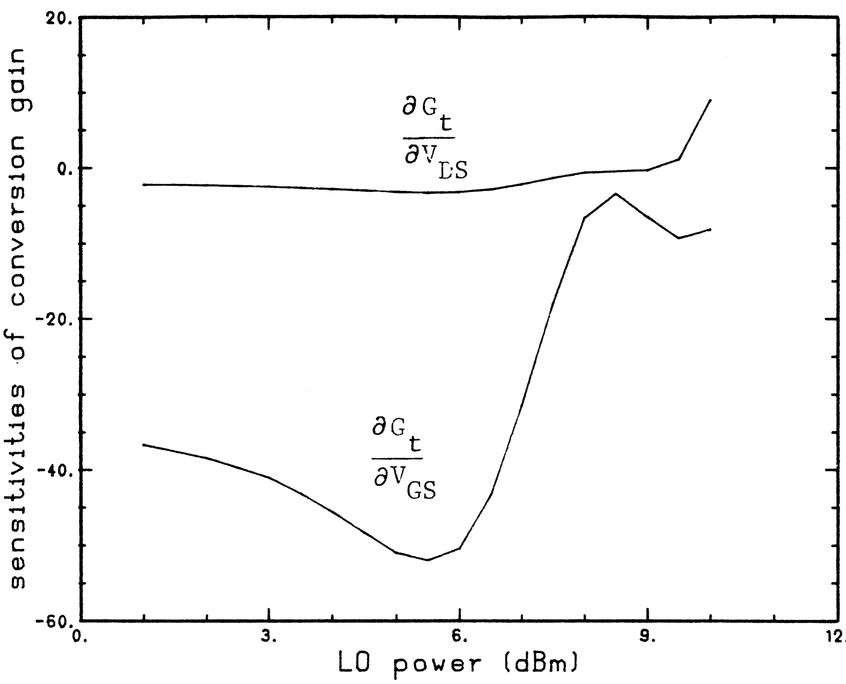
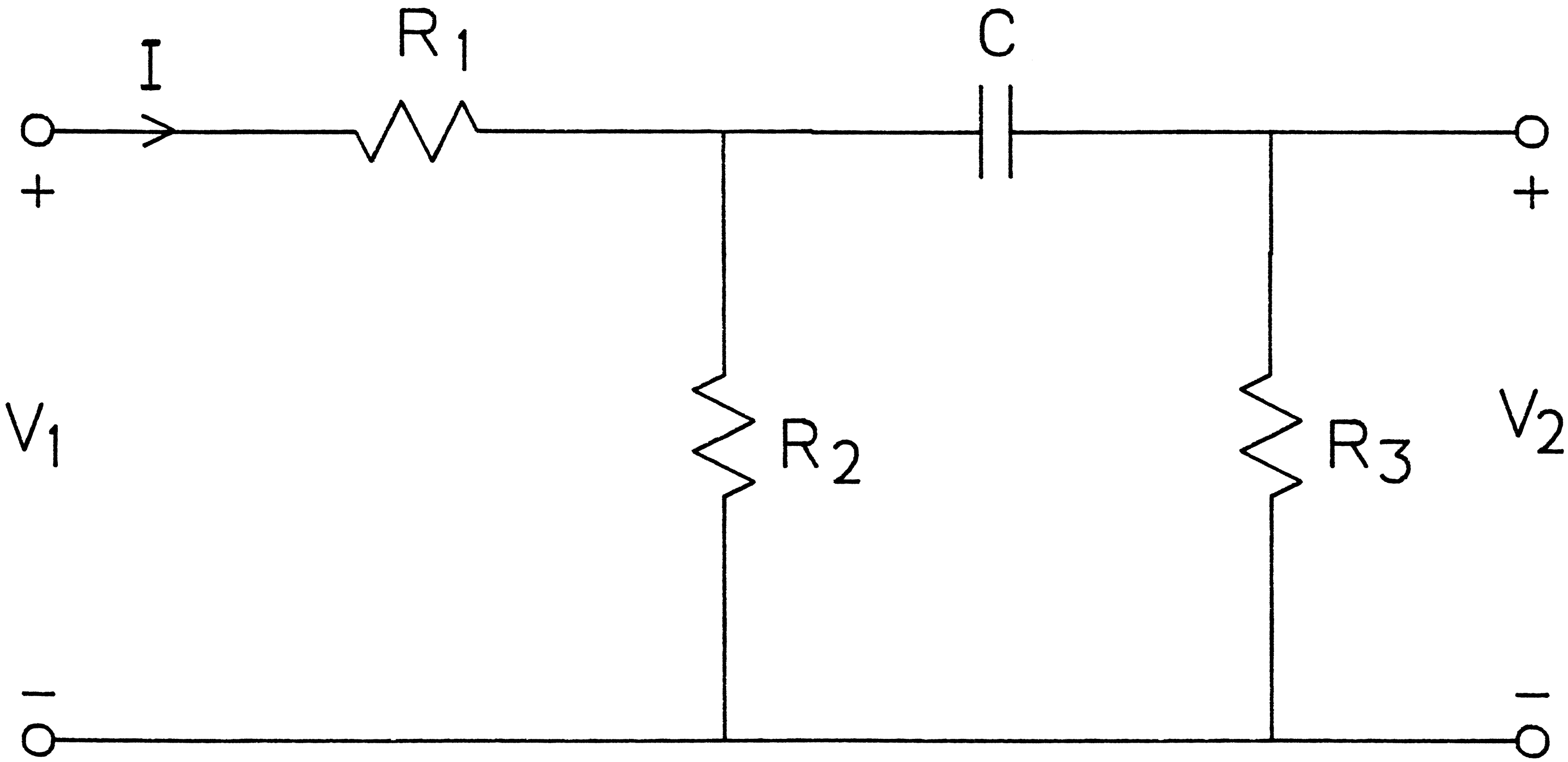


Fig. 6 Sensitivities of conversion gain w.r.t. bias voltages as functions of LO power.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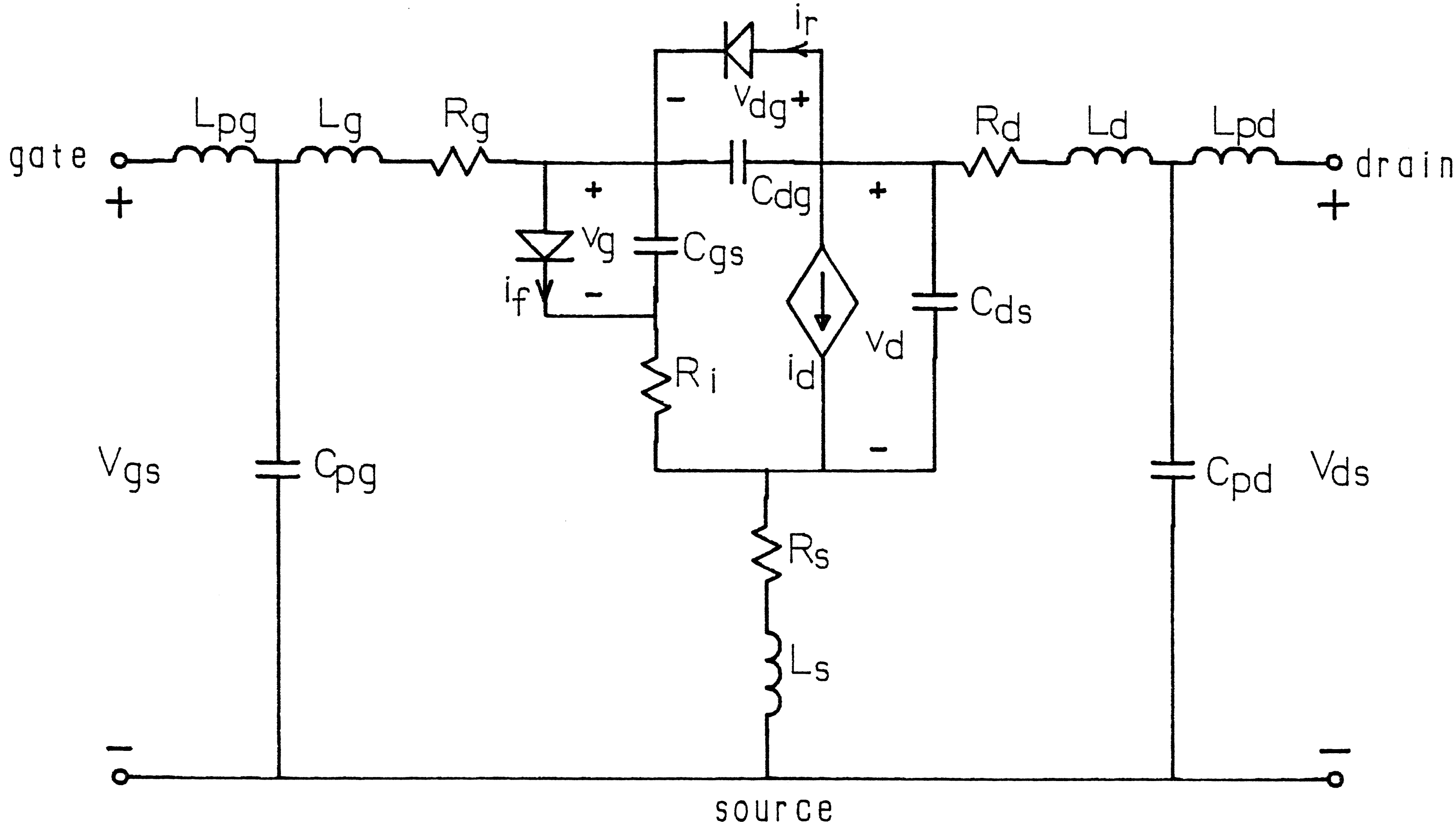
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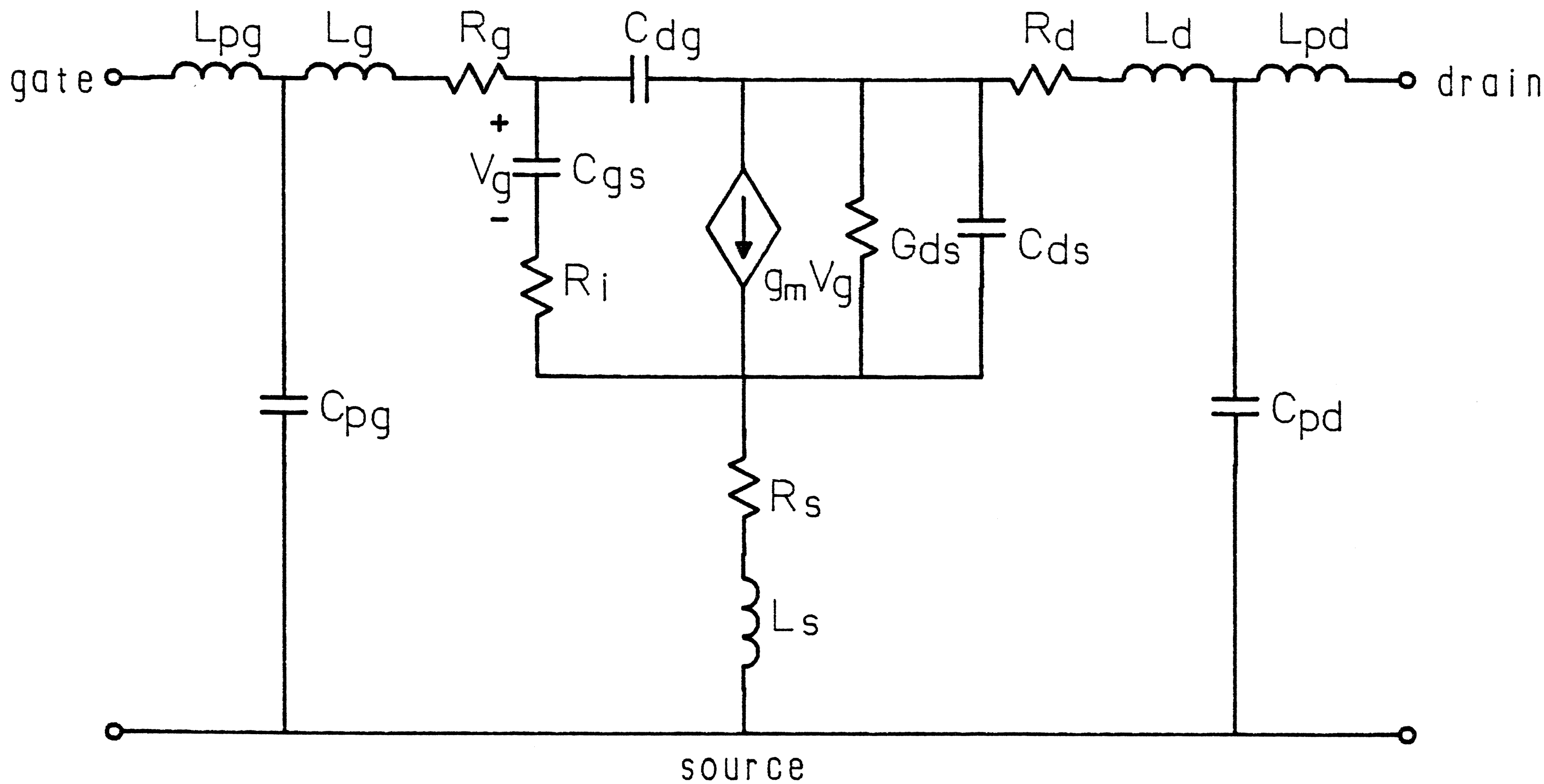

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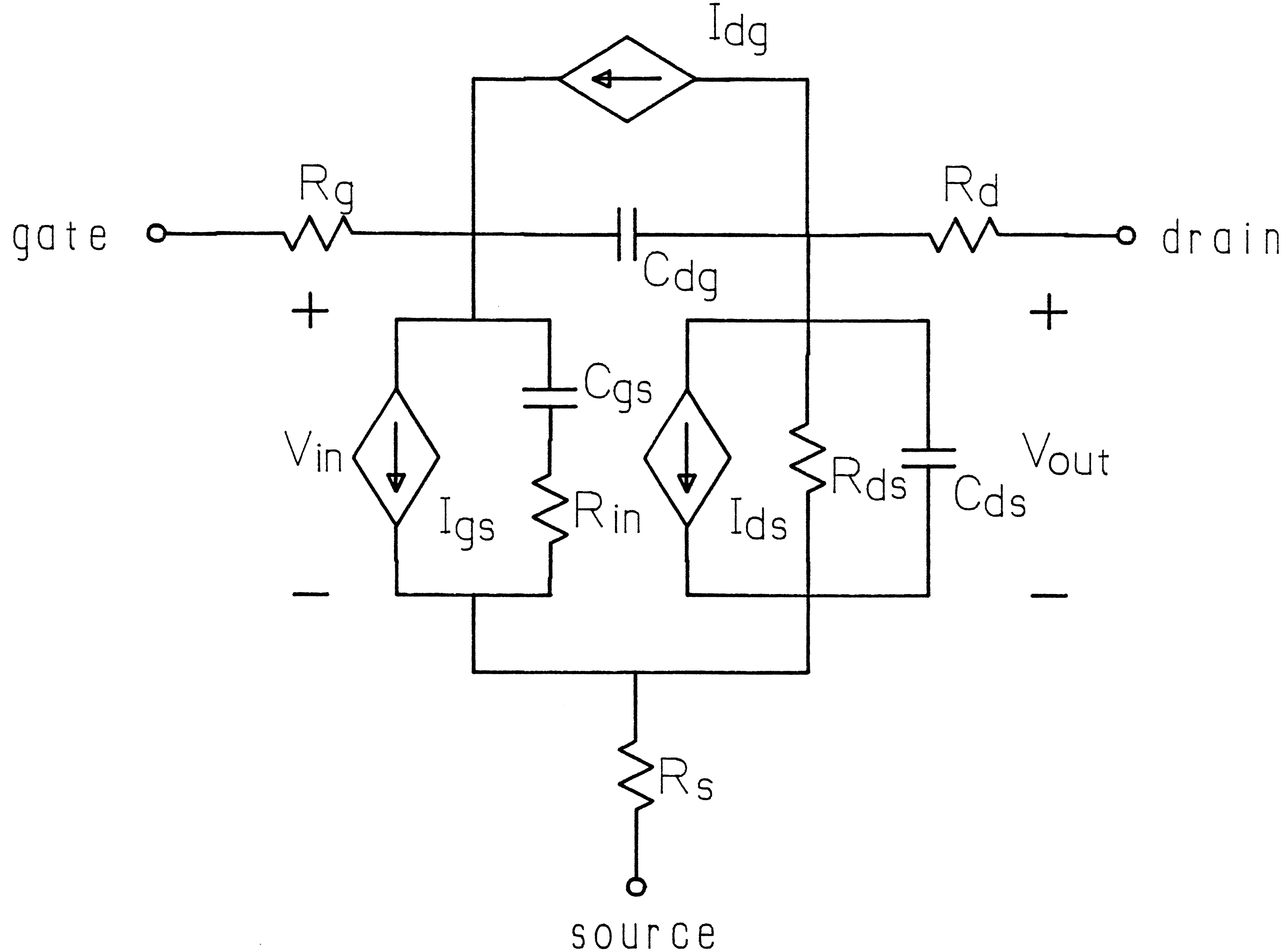
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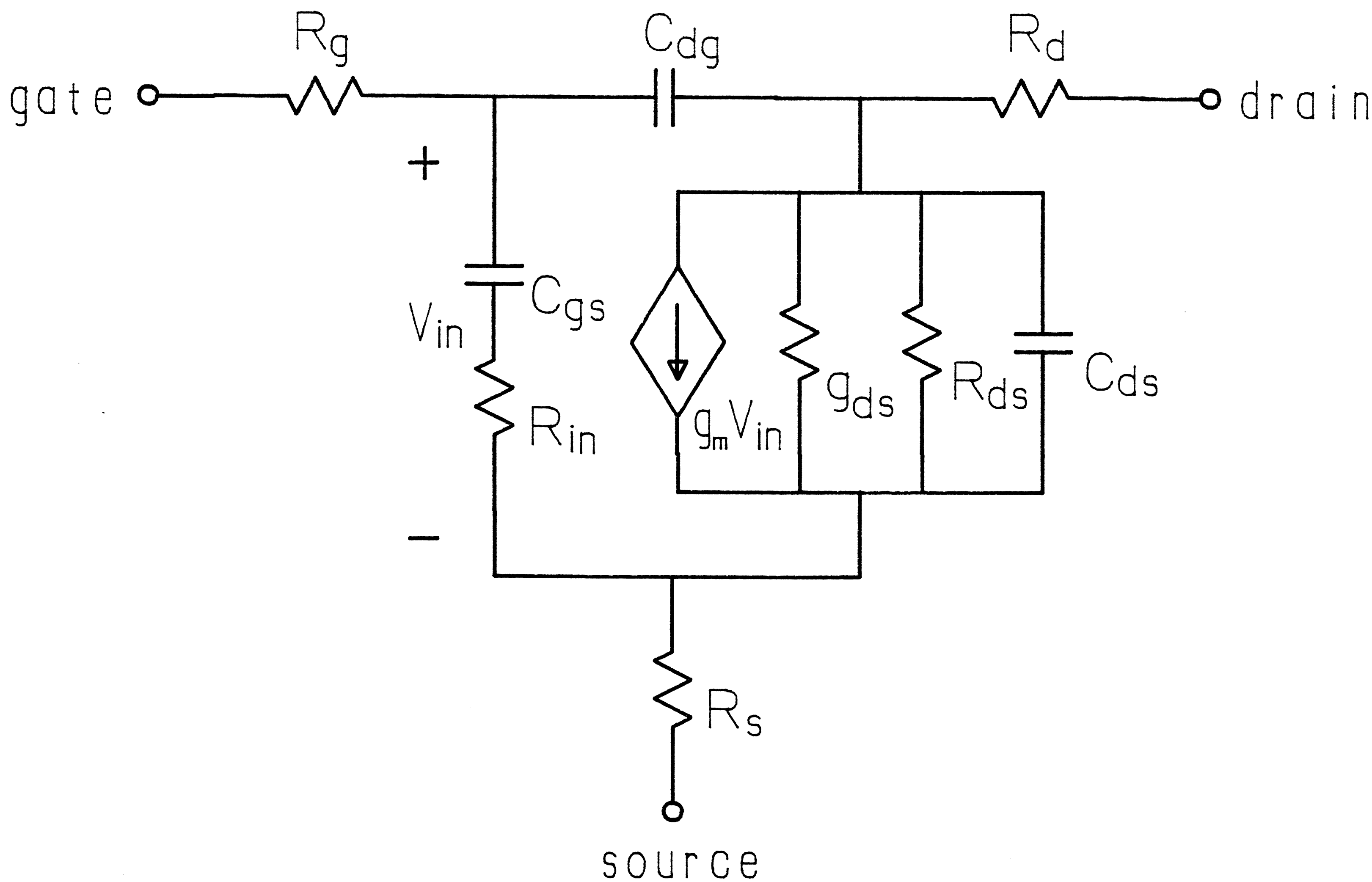
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