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YIELD OPTIMIZATION OF LARGE SCALE MICROWAVE CIRCUITS

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ABSTRACT

In this paper we demonstrate for the first time the feasibility of yield optimization of large scale microwave circuits. A combined strategy to attack this difficult problem is proposed, which includes the use of supercomputers, efficient approximation to the circuit responses, and the use of fast, dedicated simulation techniques. We have successfully accomplished the yield optimization of a 5 channel multiplexer with 75 design and toleranced variables, 124 constraints and up to 200 statistically perturbed circuits. No microwave circuit design of this type and on this scale has ever been reported.

INTRODUCTION

Due to various kinds of fluctuations inherent in the manufacturing process, any circuit outcome can not be guaranteed to have exact nominal parameter values. The outcomes will present variations of responses from one another. The merit of a design is no longer measured by the performance of the circuit with nominal values. Thus, yield driven design is becoming an indispensible tool in the microwave CAD area [1].

Yield optimization takes a variety of fluctuations into account, aiming at a circuit design with satisfactory yield. Unlike digital circuits, microwave circuits often have a very large number of independent parameters, thus creating very large problems. Application of the concepts of yield optimization to large scale circuits is of primary importance. There are two major difficulties faced by existing circuit design methods: (1) the cost and time of simulation increases with the size of the circuit, and (2) algorithms capable of handling large optimization problems are needed.

In this paper we discuss yield optimization of large scale microwave circuits, both tunable and nontunable. We attack this difficult problem here by: (1) the use of supercomputers, (2) efficient approximation to the circuit responses, and (3) the use of fast, dedicated simulation techniques.

An example of a 5 channel multiplexer with 75 design and toleranced variables, 124 constraints and up to 200 statistically perturbed outcomes, is used to demonstrate the feasibility of yield optimization of large scale problems using our combined strategy.

STATISTICAL DESIGN

Manufacturing yield is simply the ratio

$$N_{pass}/N_t \,, \tag{1}$$

where N_{pass} is the number of circuit outcomes meeting the design specifications and N_t is the total number of circuit outcomes. If tuning is involved, an outcome may be considered before or after tuning. The purpose of tuning is to increase yield.

Let x^0 denote the nominal design parameter vector. The *k*th tunable outcome x^k may be described by

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$$x^k = x^0 + r^k, \quad r^k = s^k + t^k + s_t^k, \quad k = 1, 2, \ldots, N_t, \tag{2}$$

where s^k represents deviations due to the model uncertainties and tolerances, t^k denotes possible postproduction tuning adjustments, and s_t^k represents tuning imprecisions, which may remain after actual tuning. For ideally accurate tuning ($s_t^k = 0$) we can obtain $r^k = 0$ provided that the tuning ranges are large enough to accommodate the spreads due to the manufacturing tolerances. Then, for realistic (imprecise) tuning we obtain $r^k = s_t^k$. Outcomes of nontunable circuits can be considered as a special case of (2), where $r^k = s^k$.

For both tunable and nontunable circuit design, each sample circuit is associated with an acceptance index given by

$$I_a(x^k) = \begin{cases} 1, & \text{if } x^k \text{ satisfies the specifications} \\ 0, & \text{otherwise.} \end{cases} \tag{3}$$

Then, yield is estimated by

$$Y \approx \left[\sum_{k=1}^{N_t} I_a(x^k) \right] \Big/ K. \tag{4}$$

In this paper we focus our attention on the case of fixed manufacturing tolerances and assumed tuning tolerances. Consequently, our problem of circuit optimization is stated as

$$\underset{x^0}{\text{maximize}}\ Y. \tag{5}$$

The design of tunable circuits using (5) has two goals. One is to drive up the probability of obtaining circuits that exhibit good initial responses for the tuning process. The other is to increase the possibility of the circuit outcomes satisfying specifications after tuning easy-to-tune elements. In this case we assign larger tuning tolerances to more difficult-to-tune elements. This should have an impact on the overall effort of tuning.

Most approaches to yield optimization proposed in the literature have difficulties dealing with large scale problems. Our approach to yield optimization follows a novel multi-circuit approach [2]. A number of circuits are sampled according to probability density functions of tolerances [3], and then they are simultaneously forced to meet design specifications. Several successive optimizations can be used if necessary, each of which may use different numbers of outcomes. The one-sided ℓ_1 objective function is used to perform the centering of these circuit outcomes.

APPROXIMATION TO CIRCUIT RESPONSES

For a large scale circuit and due to repeated simulations required for multiple circuits, the computational cost of yield optimization can be prohibitively high, and the CPU time can be unacceptably long. In order to speed up the design we use quadratic approximation to the circuit responses as proposed in [4].

A quadratic polynomial to approximate a given response $f(x)$, $x = [x_1\ x_2\ \ldots\ x_n]^T$, can be written as

$$q(x) = a_0 + \sum_{i=1}^{n} a_i(x_i - x_i^0) + \sum_{\substack{i,j=1 \\ i \geq j}}^{n} a_{ij}(x_i - x_i^0)(x_j - x_j^0), \tag{6}$$

where x^0 is the reference point. The function $f(x)$ is evaluated at m $(m > n + 1)$ points, x^k, $k = 0, 1, 2, \ldots, (m - 1)$. These points are called base points. Using the function values $f(x^k)$, we set up a system of linear equations

$$\begin{bmatrix} Q_{11} & Q_{12} \\ Q_{21} & Q_{22} \end{bmatrix} \begin{bmatrix} \mathbf{a} \\ \mathbf{v} \end{bmatrix} = \begin{bmatrix} \mathbf{f}_1 \\ \mathbf{f}_2 \end{bmatrix}, \tag{7}$$

where the vectors $\mathbf{a}$ and $\mathbf{v}$ contain a_i and a_{ij}, respectively, and the vectors $\mathbf{f}_1$ and $\mathbf{f}_2$ contain $f(x^k)$. The model coefficients can be solved as

$$\mathbf{v} = \mathbf{C}^T(\mathbf{C}\mathbf{C}^T)^{-1}\mathbf{e} \tag{8a}$$

and

$$\mathbf{a} = Q_{11}^{-1}\mathbf{f}_1 - Q_{11}^{-1}Q_{12}\mathbf{v}, \tag{8b}$$

where

$$\mathbf{C} = Q_{22} - Q_{21}Q_{11}^{-1}Q_{12}$$

and

$$\mathbf{e} = \mathbf{f}_2 - Q_{21}Q_{11}^{-1}\mathbf{f}_1.$$

Here, we arrange the first $(n + 1)$ base points as x^0 and

$$x^i = x^0 + [0\ 0\ \ldots\ 0\ \beta_i\ 0\ \ldots\ 0]^T, \quad i = 1, 2, \ldots, n, \tag{9}$$

where β_i is a certain perturbation. This arrangement results in very simple forms of $\mathbf{Q}_{11}$ and $\mathbf{Q}_{11}^{-1}\mathbf{Q}_{12}$ so that they do not have to be computed and stored. After these first $(n + 1)$ base points, a sequence of other base points follows with no particular restriction on their locations. When x^k $(k > n)$ is added as a new point, the components of the $(k - n)$th row of $\mathbf{C}$ are simply either

$$c_{k-n,(ii)} = (x_i^k - x_i^0)^2 - \beta_i(x_i^k - x_i^0) \tag{10a}$$

or

$$c_{k-n,(ij)} = (x_i^k - x_i^0)(x_j^k - x_j^0), \quad \text{for } i \neq j, \tag{10b}$$

where (ii) and (ij) indicate the column indices, which correspond to the positions of a_{ii} and a_{ij} in $\mathbf{v}$.

Using (10), the computational effort required by the original approach of [4] can be substantially reduced, thus making this kind of approximation even more attractive.

YIELD OPTIMIZATION OF A 5-CHANNEL MULTIPLEXER

A 5-channel 12 GHz contiguous band microwave multiplexer, consisting of multicavity filters distributed along a waveguide manifold, has been designed by applying yield optimization techniques. The ultimate specifications, after complete tuning, are 20dB for the common port return loss and 20dB for the individual channel stopband insertion losses. At the frequency points considered, 124 nonlinear constraint functions are composed. Design variables for each channel include 12 couplings, input and output transformer ratios and the waveguide spacings.

Careful and time-consuming tuning is essential for multiplexers. Any adjustments involving physical disconnection of the structure is particulary expensive. For the sake of illustration we focus attention in this example on the waveguide spacings as being expensive adjustments to make. Therefore, the larger tuning tolerances could be assumed for the spacings. We considered total tolerances of 5% for the spacings, and 0.5% for the couplings and the transformer ratios.

In tunable circuit design, target specifications for yield optimization may be different from those of tuning. In this example, we relaxed the specifications from 20dB to 10dB for the return and stopband insertion losses. We use the term yield index to denote the ratio of the number of circuits satisfying the relaxed specifications to the total number of outcomes.

The starting point was the solution of the conventional minimax nominal design w.r.t. the ultimate specifications. The corresponding responses are shown in Fig. 1, which exhibit typical responses of a multiplexer. The yield index at this point was 75%.

Yield optimization was carried out on the CRAY X-MP/22 using the generalized ℓ_p centering algorithm [2], the approximation scheme described in this paper and utilizing a dedicated multiplexer simulation program [5]. The entire process consisted of 4 optimization phases as shown in Table I. At the beginning of each phase a set of quadratic models was constructed by exact simulation of the circuit at 151 base points. Then the models were used in the entire phase to evaluate the approximate circuit responses and their gradients. This approach allowed us to handle this extremely large optimization problem (75 toleranced variables, 124 constraints and up to 200 statistically perturbed outcomes at each iteration) in acceptable cpu time.

After yield optimization the yield index increased to 90%. The statistical properties at the final solution are well illustrated by two envelopes containing the return losses of all 3000 statistically perturbed circuits and the acceptable circuits, shown in Figs. 2 and 3, respectively.

CONCLUSIONS

Using supercomputers and very efficient approximation techniques we have demonstrated the feasibility of yield optimization of large scale microwave circuits. The problem of yield optimization for both tunable and nontunable circuits has been discussed.

We have successfully accomplished the yield optimization of a 5 channel multiplexer with 75 design and toleranced variables, 124 constraints and up to 200 statistically perturbed circuits. No microwave circuit design of this type and on this scale has ever been reported.

For nonlinear microwave circuit design, yield optimization will face problems on an even larger scale. Our approach using supercomputers, and accurate and efficient approximation techniques will make yield optimization of nonlinear circuits affordable.

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TABLE I

STATISTICAL DESIGN OF A 5-CHANNEL MULTIPLEXER USING QUADRATIC APPROXIMATION

		Phase 1	Phase 2	Phase 3	Phase 4
Initial Yield index	*	75.00%	(81.00%)	(84.33%)	(90.00%)
	**	56.33%	69.00%	69.33%	92.00%
Final Yield Index	*	81.00%	84.33%	90.00%	90.33%
	**	77.33%	77.33%	91.33%	94.00%
No. of Outcomes in Design		50	100	150	200
No. of Iterations		4	6	6	4
CPU Time (CRAY X-MP/22)		16.5s	17.6s	17.8s	17.6s

CPU times do not include yield index estimation based on actual simulation.
All yield indices are estimated from 300 outcomes.
* The yield index is estimated by actual simulation.
** The yield index is estimated by maximally flat approximation.

Fig 1. Optimized return and insertion loss vs. frequency for the 5-channel multiplexer.

Fig 2. The envelope containing return loss responses of all 3000 Monte-Carlo samples.

Fig 3. The envelope containing return loss responses of acceptable circuits among 3000 Monte-Carlo samples.