DESIGN CENTERING, YIELD MAXIMIZATION

AND THE TOLERANCE PROBLEM

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ABSTRACT

This report is oriented towards electronic and microwave engineering design problems in which a large volume of production of circuits or devices is envisaged. Designs are considered subject to manufacturing tolerances, process and material uncertainties, environmental uncertainties and model uncertainties. The reduction of cost by increasing tolerances, the determination and optimization of production yield, and the problem of design centering subject to fixed tolerances are discussed. Nonlinear optimization approaches to solving these problems are considered.

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INTRODUCTION

This report deals principally with electronic and microwave engineering design problems in which a large volume of production is envisaged, e.g., integrated circuits. In this context designs are considered subject to possible processing imprecision, manufacturing tolerances, material uncertainties, environmental uncertainties, model uncertainties, and so on. For example, manufacturing tolerances may be considered on physical dimensions, material uncertainties may be on dielectric constants, environmental uncertainties may involve temperature, and model uncertainties may be on equivalent circuits.

Undesirable effects which deteriorate performance may be due to electromagnetic coupling between elements and impedance mismatches between them and terminations. The main objective is the reduction of cost by increasing tolerances, maximizing production yield with respect to an assumed probability distribution function, and optimally utilizing available design margins and windows in the performance specifications.

The related optimization problem is generically referred to as design centering. Its principal aim is the optimal determination of a set of nominal design parameter values. Production yield, which needs to be both estimated and enhanced by optimization, may be simply defined as the ratio of the number of actual manufactured outcomes which satisfy the specifications to the total number of manufactured outcomes.

The material presented in this report is based on a paper by Bandler [1] and on an article in preparation by Bandler and Chen [2].

References

[1] J.W. Bandler, "Engineering modelling and design subject to model uncertainties and manufacturing tolerances," in Methodology in Systems Modelling and Simulation, B.P. Zeigler, et al. Eds. North Holland, 1979, pp. 399-421.

[2] J.W. Bandler and S.H. Chen, "Circuit optimization: state-of-the-art", to be submitted to IEEE Trans. Microwave Theory and Techniques.

REVIEW OF OPTIMIZATION ORIENTED CIRCUIT CAD

Introduction

We describe in this section typical problems in modern optimization oriented computer-aided circuit design. We focus, in particular, on problems within the domain of the application of formal mathematical simulation and optimization appropriate to analog electronic and microwave circuits and systems.

Figure 1 shows some typical design situations. The concept of upper and lower specifications on a response function of an independent variable ψ, e.g., frequency or time, implies a constraint region in the space of designable variables $\boldsymbol{\phi}$. This concept is easily generalized to response functions of a number of independent variables $\boldsymbol{\psi}$.

Error functions involved in a classical minimax or Chebyshev approximation problem expressed along a sampled ψ axis can be represented in terms of ϕ by contour diagrams of the maximum, with its distinctive discontinuous derivatives.

A family of possible responses produced by the many outcomes of actual circuits with independent designable parameters lying within a tolerance region around a nominal design is shown also.

Nominal Design

Nominal design is the conventional approach used by microwave engineers. In nominal design we seek a single point in the space of designable variables which best meets a given set of performance specifications and design constraints. A suitable scalar measure of the deviation between responses and specifications which forms the objective function to be minimized is the ubiquitous least squares measure, the more esoteric generalized least pth objective [1] or the

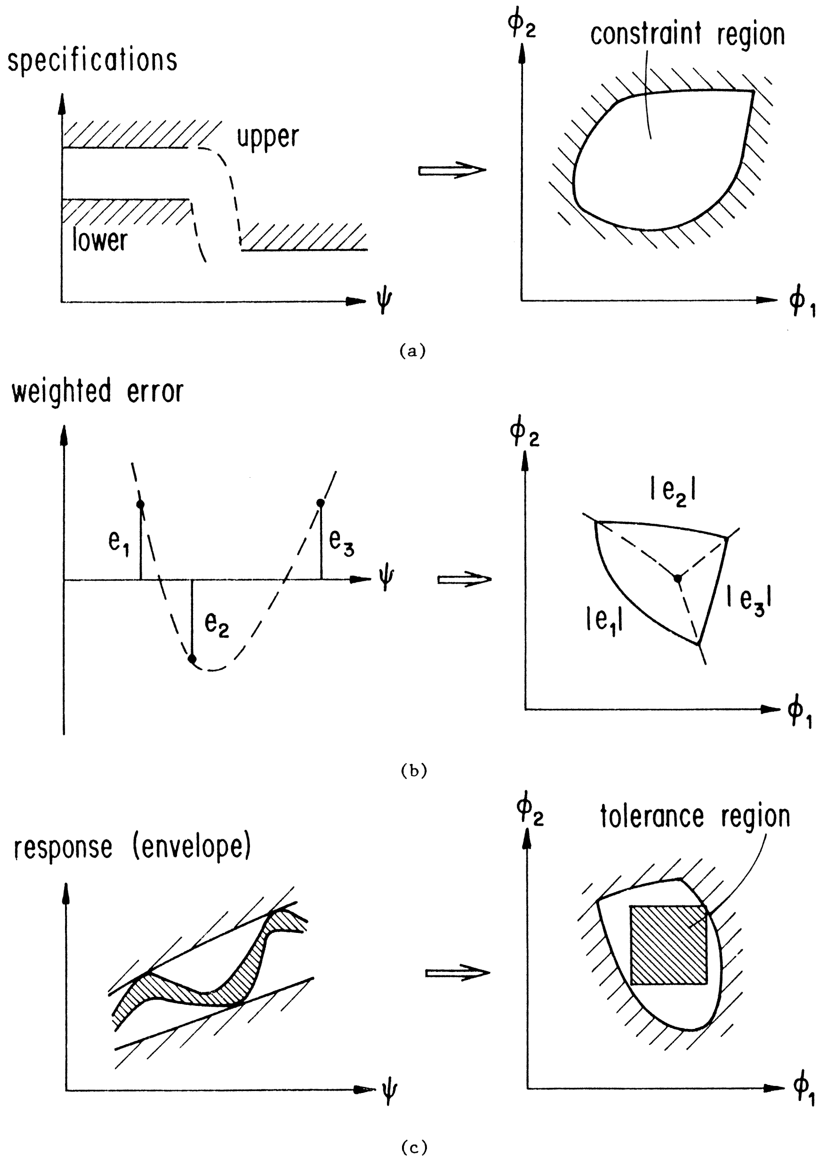


Fig. 1 Some typical design situations. In (a) we have upper and lower specifications on the response function of one independent variable implying a constraint region with respect to the designable parameters. In (b) is shown a weighted error function sampled at three points giving rise to minimax contours. In (c) we have a toleranced design satisfying all performance specifications.

minimax objective.

Nonlinear minimax optimization, a special case of which is the classical analytically oriented Chebyshev approximation, has been traditionally favored by filter designers, whereas the least squares approach has been more favored for a wider range of circuit design problems. For example, both Touchstone and Super-Compact have hitherto provided designers soley the least squares objective.

Sensitivity Minimization

In the so-called sensitivity minimization approach it is recognized that an actual realization of the solution point corresponding to a single simulated performance optimized design is subject to fluctuation or deviation. Traditionally, this is dealt with by defining a measure of sensitivity, usually involving first-order sensitivities of responses w.r.t. design parameters, and including it in the objective function.

Tolerance Design

When uncertainties and tolerances are considered explicitly, two important classes of problems emerge: statistical design and worst-case design.

In statistical design it is recognized that a production yield of less than 100% is likely. This approach has two principal aims. We attempt to minimize the overall cost of design, production, testing, tuning, etc. Alternatively, we orient the CAD process to maximize yield by optimizing the designable parameters of the circuit. A possible cost versus yield curve is shown in Fig. 2 [2].

In worst-case design we require that all units meet the specifications under all circumstances, with or without tuning, depending on what is practical.

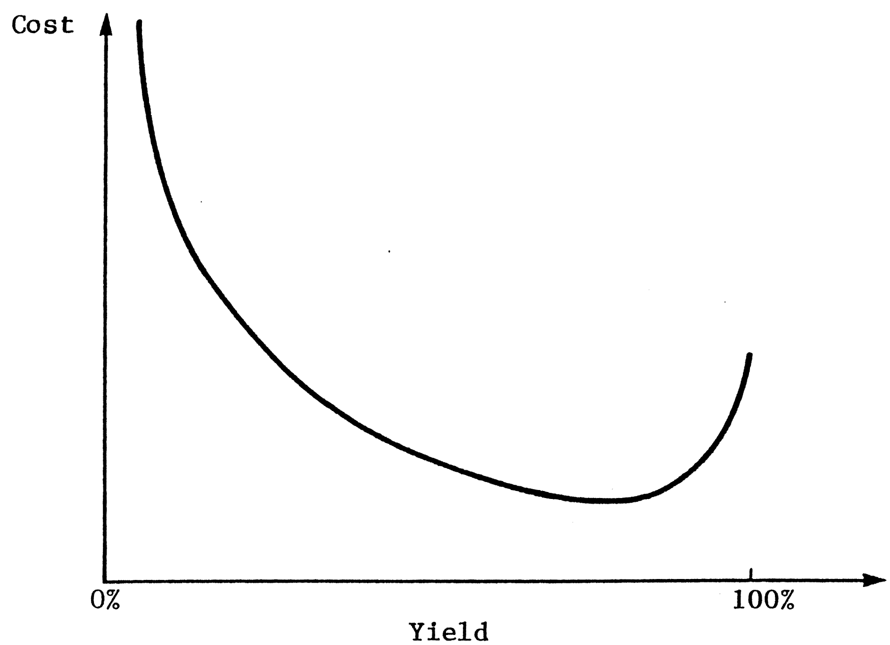


Fig. 2 A possible circuit cost vs. yield curve [2].

Both statistical design and worst-case design have the following features in common. Typically, we either attempt to center the design with fixed assumed tolerances (this is the fixed tolerance problem) or we attempt to optimally assign tolerances to reduce production cost (this is variously called tolerance optimization, tolerance assignment or, more formally, the variable tolerance problem).

What distinguishes all these problems from nominal designs or sensitivity minimization is the fact that a single point is no longer of interest: a (tolerance) region of multiple possible outcomes is to be optimally located with respect to the feasible (acceptable, constraint) region.

References

[1] J.W. Bandler and M.R.M. Rizk, "Optimization of Electrical Circuits," Mathematical Programming Study 11, 1979, pp. 1-64.

[2] K. Singhal and J.F. Pinel, "Statistical design centering and tolerancing using parametric sampling," IEEE Trans. Circuits and Systems, vol. CAS-28, 1981, pp. 692-702.

THE TRADITIONAL CAD APPROACH

Microwave designers are typically performance oriented. Their aim has been to produce a good set of design parameters corresponding to a single circuit. If they can show that a single simulated outcome satisfies the requirements of performance they have basically demonstrated that a feasible circuit is possible.

Traditionally, microwave designers have placed very strong reliance on postproduction tuning of customized products to attempt to realize on the bench the satisfactory response they observed for their simulation model on the computer. In volume production of integrated circuits, however, with high overhead costs and lengthy prototype production cycles this individual attention to an outcome and subsequent tuning or alignment is not cost effective.

In conventional microwave circuit design a nontunable circuit presumably implies that every unit has to be individually tested and each violating outcome discarded. On the other hand, a tunable design implies that at least one variable can be adjusted after testing in an effort to meet performance specifications. The presence of tuning tends to increase cost, not only in arranging for the availablity of tuning but in having to have it actually implemented.

MODERN DESIGN WITH TOLERANCES

Some Obstacles

Setting any or all of the aforementioned problems up as nonlinear optimization problems poses numerous difficulties. There is the problem of identifying a suitable objective (cost) function. Very little hard data is available in the open literature about production cost as a function of the variables entering into a design. Hence, highly simplified intuitive points of view are usually taken: abstract functions which force the expansion of a tolerance orthotope within the constraint region, the optimal location of a sphere within the region and so on.

The matter is complicated by unknown correlations between variables, empirical assumptions about models and model parameter uncertainties and unreliable or unknown distributions of outcomes of component values between tolerance extremes. The number of constraints and even variables that could be chosen for an otherwise deceptively simple design problem is virtually unlimited.

The direct use of the Monte Carlo method of tolerance analysis using assumed probability distributions within the optimization loop can be extremely computationally intensive when there is a large number of statistical variables. Approaches have been suggested in the literaure to avoid repeated use of the Monte Carlo method for estimating yield such as the method of parametric sampling or to employ multidimensional approximations (linear, quadratic, simplicial) of the responses, constraints or constraint boundaries.

The Monte Carlo Method

The Monte Carlo method consists of applying a numerical process on random numbers. Random numbers can be constructed by means of a physical process or arithmetical algorithms. Those random numbers which are generated by arithmetical algorithms are called pseudorandom numbers. In the most commonly used method for generating uniform pseudorandom numbers, a sequence of numbers is generated according to some recursive formula. This sequence is actually completely deterministic.

To carry out a Monte Carlo analysis we may need to construct random numbers from a given distribution. We can employ a simple rejection technique to carry this out. We choose a pair of random numbers from a uniform distribution on [0, 1]. According to a straightforward criterion the pair is accepted as representing a random outcome from the distribution or it is rejected and a new pair of random numbers is generated and the process repeated. After appropriate transformations of variables, simulated multiple circuit outcomes used in a design optimization process may be generated according to this scheme.

The basic Monte Carlo approach does not, unfortunately, provide accurate estimates of yield without considerable cost. Convergence is only proportional to the square root of N, the number of samples, e.g., a tenfold improvement in precision requires a hundred fold increase in the number of samples taken to represent the circuit outcomes.

Response Approximations and Data Bases

The most costly phase of the statistical approach to design is the circuit response simulation. Consequently, approaches to yield maximization frequently resort to the creation of circuit parameter and response data bases containing the results of many hundreds of complete network analyses. When yield estimation or design optimization are carried out a data base may be used to avoid the repeated expensive circuit simulations. The accuracy of the yield estimate is, however, likely to deteriorate as the optimization proceeds and the nominal point, or design center, moves out of the useful range of the data base.

Some proposals use multiple quadratic models derived from a data base to reduce the cost of simulations. Yield estimates are then computed from these models. It is recommended that such quadratic polynomials are fitted individually to the many nonlinear constraint or response functions and updated during the optimization process. Under these circumstances the very costly method of parameter perturbations adopted by such CAD systems as Touchstone and Super-Compact to produce gradient estimates for their built-in gradient based optimizer(s) might be obviated. The reason is that gradients required for efficient optimization are readily available from the analytical approximation formulas.

A PROPOSED MULTI-CIRCUIT APPROACH

Nominal circuit optimization, described earlier, focuses attention on a certain kind of idealized situation. In reality uncertainties may enter the problem at different levels, including parameter tolerances, model uncertainty and measurement errors. The approximate nature of an equivalent circuit, for example, may render the result of modeling unreliable. In such cases, a single nominal point can not satisfactorily represent all the possible outcomes.

An effective solution to this problem is to consider several sets of parameters, i.e., multiple circuits, simultaneously. We use

$$\boldsymbol{\Phi} = \begin{bmatrix} \boldsymbol{\phi}^0 \\ \boldsymbol{\phi}^1 \\ \cdot \\ \cdot \\ \boldsymbol{\phi}^K \end{bmatrix}$$

to denote K+1 sets of parameters. The multiple sets of parameters are not arbitrarily generated. Their relationship can be expressed symbolically as

$$\boldsymbol{\phi}^k = \boldsymbol{\phi}^0 + \mathbf{r}^k, \quad k = 1, 2, \ldots, K.$$

It should be noted that not necessarily all these parameters are designated as separate variables for optimization. In fact, some components of each $\boldsymbol{\phi}^k$ may have the same value as those of $\boldsymbol{\phi}^0$ and some may be fixed at constant values. In general, we use $\mathbf{x}$ to denote the vector of n optimization variables, as distinct from $\boldsymbol{\phi}^k$ or $\boldsymbol{\Phi}$.

For each circuit we have a set of error functions $\mathbf{e}(\boldsymbol{\phi}^k)$. We denote the overall error functions by

$$\mathbf{f}(\mathbf{x}) = \begin{bmatrix} \mathbf{e}(\boldsymbol{\phi}^0) \\ \mathbf{e}(\boldsymbol{\phi}^1) \\ \cdot \\ \cdot \\ \mathbf{e}(\boldsymbol{\phi}^K) \end{bmatrix} .$$

It can be shown [1] that the problems of design centering, optimal tolerancing, optimal tuning, yield optimization and robust modeling can all be stated using the unified formulation of multi-circuit optimization.

In the present context the goal of multi-circuit design is to maximize yield in the presence of simulated tolerance effects. Theoretically, we define the yield by a n_ϕ-fold integral over the constraint region, where n_ϕ is the dimensionality of $\boldsymbol{\phi}$. To approximate this in practice we consider K randomly selected circuits. Based on the error functions $\mathbf{e}(\boldsymbol{\phi}^k)$, we define an acceptance index

$$I_a(\boldsymbol{\phi}) = \begin{cases} 1 & \text{if} \quad \mathbf{e}(\boldsymbol{\phi}) \leqslant \mathbf{0} \\ 0 & \text{otherwise} \end{cases} .$$

Then

$$K_{pass} = \sum_{k=1}^{K} I_a(\boldsymbol{\phi}^k)$$

is the total number of circuits that meet the specifications. An estimate of yield is given by

$$Y \simeq K_{pass} / K.$$

Different aspects of the problem can be studied by specifying the vectors $\mathbf{r}^k$. If they are samples from a predetermined distribution we have a fixed tolerance problem which is also known as a design centering. Here, only the nominal point $\boldsymbol{\phi}^0$ is considered as variables to be optimized. Hence, $\mathbf{x} = \boldsymbol{\phi}^0$.

If a 100% yield is not attainable, we look for a solution where the specifications are met by as many points (out of K circuits) as possible. The approach we intend to investigate involves the specification, for each $\boldsymbol{\phi}^k$, of a scalar function which will indicate directly whether $\boldsymbol{\phi}^k$ satisfies or violates the specifications and by how much. For this purpose, we choose a set of generalized least pth functions as

$$v_k(\mathbf{x}) = H_p(\mathbf{e}(\boldsymbol{\phi}^k)), \qquad k = 1, 2, \ldots, K.$$

The sign of v_k indicates the acceptability of $\boldsymbol{\phi}^k$ while the magnitude of v_k is related to the distance between $\boldsymbol{\phi}^k$ and the boundary of the acceptable region. For example, with $p = \infty$ the distance is measured in the worst-case sense whereas for $p = 2$ it will be closer to a Euclidean measure.

Without going into details in this brief report, we intend to exploit the centering problem as a special case of the form

$$\underset{\mathbf{x}}{\text{minimize}}\ U(\mathbf{x}) = H_p(\mathbf{u}(\mathbf{x})),$$

where $\mathbf{u}(\mathbf{x})$ is related generally to the $v_k(\mathbf{x})$ in a similar generalized least pth sense.

We can define several cost functions representing separate tradeoffs in a complex environment. Each cost function may eventually be then be added as a separate term to an overall function. The resulting problem will then be similar to the so-called multiple objective optimization found in the literature. The ultimate aim is a tradeoff between satisfying performance and meeting target costs.

We may investigate the utility of a recently proposed multidimensional, dynamic constraint approximation scheme [2] to avoid the large number of base points required for complete quadratic interpolations and also the promising parametric sampling approach [3].

References

[1] J.W. Bandler and S.H. Chen, "Circuit optimization: state-of-the-art", to be submitted to IEEE Trans. Microwave Theory and Techniques.

[2] R.M. Biernacki and M.A. Styblinski, "Statistical circuit design with a dynamic constraint approximation scheme," Proc. IEEE Int. Symp. Circuits and Systems (San Jose, CA, 1986), pp. 976-979.

[3] K. Singhal and J.F. Pinel, "Statistical design centering and tolerancing using parametric sampling," IEEE Trans. Circuits and Systems, vol. CAS-28, 1981, pp. 692-702.

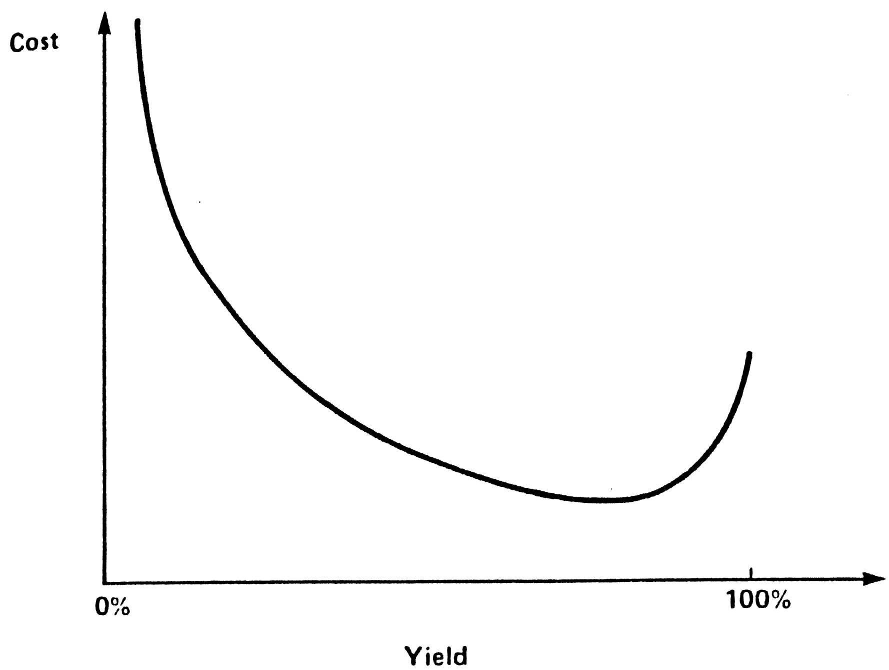
DISCUSSION

Generally speaking, the accuracy and computational complexity (but not the cost of computation) of statistical approaches are independent of dimensionality. One of the important features of statistical approaches is that they are easy to implement. On the other hand, this kind of method does not yield high accuracy, and the significant amount of computer time is a frequently mentioned drawback.

The deterministic approaches tend to be more difficult to implement. They suffer from the curse of dimensionality. They are generally considered computationally modest (i.e., comparable to the effort for a nominal design) only when the dimensionality of the space of designable parameters is not very high.

While the anticipated immediate application of yield maximization techniques by microwave designers is to design problems involving linear systems of equations (small-signal, linear, time-invariant circuit analysis), nonlinear circuits (analyzed in the frequency or time domains) are of particular interest. It is, therefore, expected that considerable effort will be devoted to such systems in the near future. Fortunately, all the mathematical descriptions and formulations of the tolerance design problem are directly and profitably applicable to nonlinear integrated analog circuits. The foregoing discussion on response approximation and data bases is particularly useful in this case.

The multiple circuit approach which we propose to implement is actually a very uniform extension to the existing performance oriented features of Super-Compact. The complexity of microwave integrated circuits is generally moderate compared with current VLSI circuits. This fact together with the continuing trends towards drastic reduction in the cost of mass computation: array processors, mass memory, special purpose processors, etc. and the increasing efficiency and reliability of the new generation of simulation and optimization algorithms makes us optimistic that the approach we are proposing will be both viable and cost effective.


Cost
0%
100%
Yield