YIELD MAXIMIZATION

FOR MICROWAVE CIRCUITS

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This report reviews important concepts relevant to past, present and possible future trends in the CAD of microwave circuits. It is based on material principally from two papers, one by Bandler [1] and one by Bandler and Chen [2]. Other background can be found in the review paper by Bandler and Rizk [3]. Some additional ideas and points of view, related particularly to MMIC design, are based on Pucel [4].

Microwave CAD has, traditionally, been performance oriented. The aim is a good set of design parameters corresponding to a single circuit. If a designer can show that a single simulated outcome exists which satisfies the requirements of performance he has, however, only demonstrated that a feasible circuit is theoretically possible.

There has been, and still is, very strong reliance on post-production tuning of customized products to realize on the bench the satisfactory response observed by simulation. In volume production of integrated circuits, however, with high overhead costs and lengthy prototype production cycles this individual attention to an outcome and subsequent tuning or alignment is not cost effective. It is essential that low yields be predicted and circuit topology and element types be reconfigured before costly fabrication is initiated.

For nontunable circuits every unit violating the specifications may be discarded. On the other hand, a tunable design implies that at least one variable can be adjusted after testing in an effort to meet performance specifications.

The presence of tuning tends to increase cost, not only in arranging for the availablity of tuning but in having to have it actually implemented. MMICs, in particular, should not require on-chip or in-process trimming and/or tuning, except possibly, bias adjustments [4].

Integrated circuit manufacture involves a large volume of production. In this context, a complete study must consider processing imprecision, manufacturing tolerances, material uncertainties, environmental uncertainties, model uncertainties, etc.

Undesirable effects which deteriorate performance may also be due to electromagnetic coupling between elements and impedance mismatches between them and terminations. The objective must be to reduce cost by increasing tolerances, maximizing production yield with respect to an assumed probability distribution function, and optimally utilizing available design margins and windows in the performance specifications.

The related optimization problem is generically referred to as design centering. Its principal aim is the optimal determination of a set of nominal design parameter values. Tolerances may be fixed or also optimized.

Production yield, which needs to be both estimated and enhanced by optimization, may be simply defined as the ratio of the number of actual manufactured outcomes which satisfy the specifications to the total number of manufactured outcomes.

Commercial microwave CAD software, at best, considers tolerance effects as a post-optimization analysis. Clearly, if tolerances were not explicitly accounted for during optimization, there can be no guarantee that the optimization result has minimum cost or maximum yield. In fact, both Touchstone and Super-Compact have hitherto provided designers soley the least squares objective for optimizing a single zero tolerance set of circuit parameters.

In statistical design it is recognized that a production yield of less than 100% is likely. This approach has two principal aims. We attempt to minimize the overall cost of design, production, testing, tuning, etc. Alternatively, we orient the CAD process to maximize yield by optimizing the designable parameters of the circuit. A widely assumed cost versus yield trend is shown in Fig. 1 [5].

In worst-case design we require that all units meet the specifications under all circumstances, with or without tuning, depending on what is practical.

Both statistical design and worst-case design have the following features in common. Typically, we either attempt to center the design with fixed assumed tolerances (this is the fixed tolerance problem) or we attempt to optimally assign tolerances to reduce production cost (this is variously called tolerance optimization, tolerance assignment or, more formally, the variable tolerance problem).

What distinguishes all these problems from conventional performance driven design is the fact that a single point is no longer of interest: a (tolerance) region of multiple possible outcomes is to be optimally located with respect to the acceptable region.

Figure 2 shows a typical design situation. The concept of upper and lower window type specifications on a simulated frequency response is depicted. The response clearly satisfies the specifications.

In Fig. 2, corresponding to the response, there is a set (which defines a point in the space) of equivalent circuit model parameter values. Notice that the point lies in the interior of a region. This region is directly related to the interaction of the design specifications with the fixed circuit structure and topology chosen by the designer. A different topology and different elements would produce a different region.

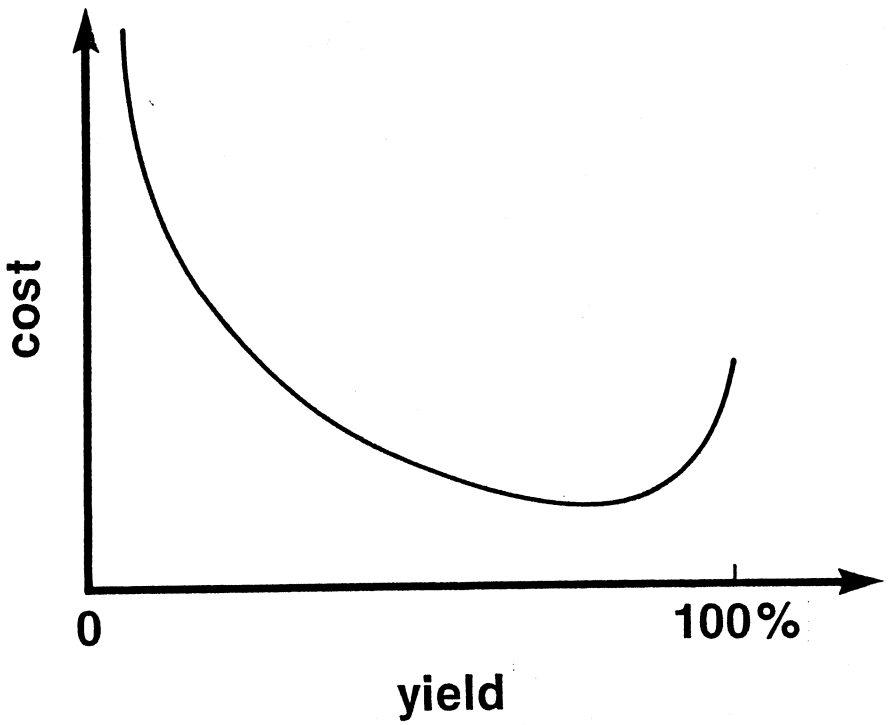

Fig. 1 A possible circuit cost vs. yield curve [5].

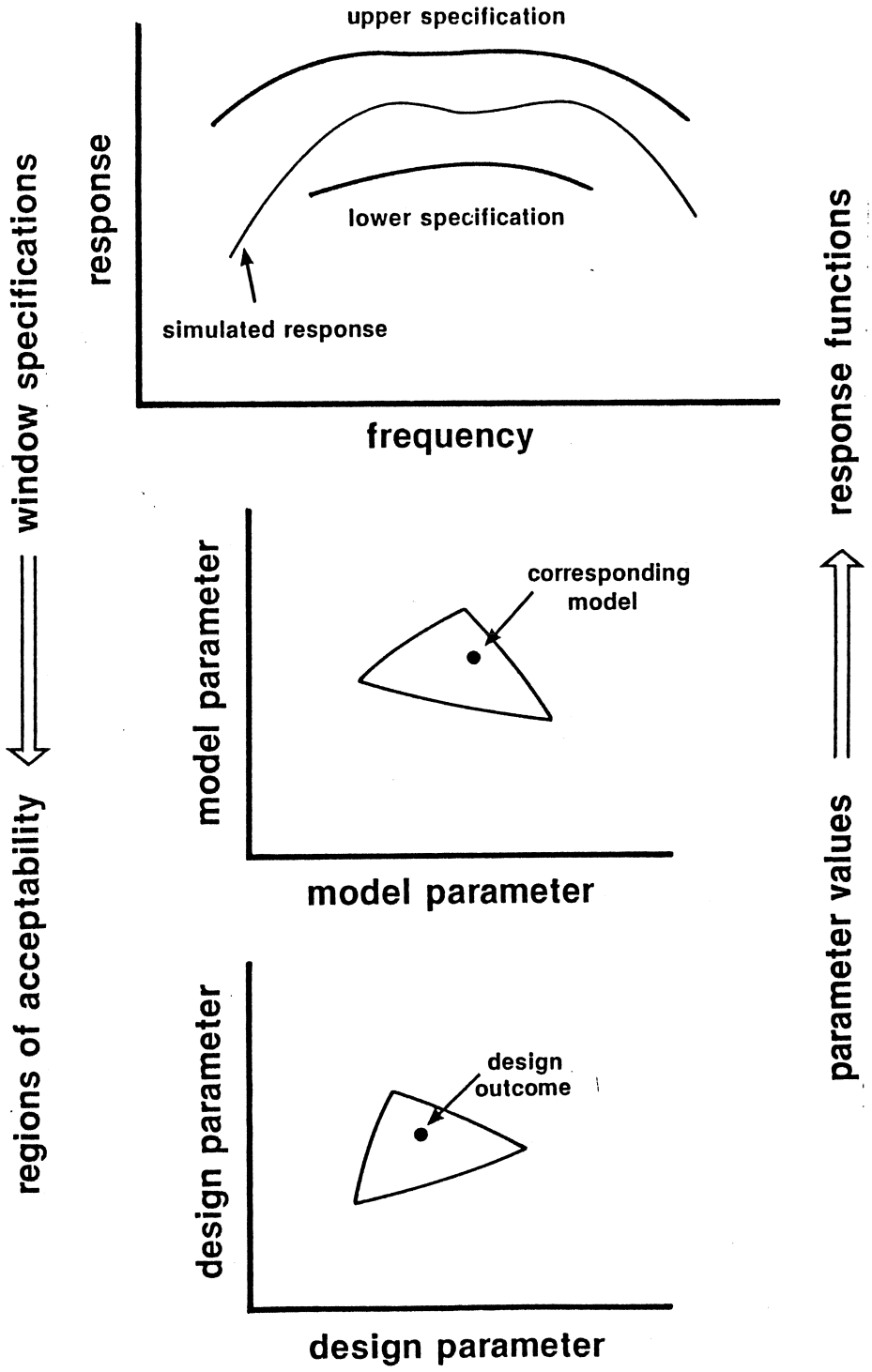

Fig. 2 Upper and lower specifications on frequency response and a corresponding satisfactory circuit outcome in the frequency domain, the model and design parameter spaces.

At a lower level, in Fig. 2, there may be independent physical parameters which are to be determined. The outcome corresponding to the satisfactory response is also an interior point of a region. Starting at the bottom of Fig. 3, the aforementioned region is called a region of acceptable designs R_a. The region of corresponding equivalent circuit models is shown immediately above. At the top of Fig. 3 we see an envelope of acceptable responses within the response window. Notice that the entire window is not filled. This emphasizes the interaction between the relatively arbitrary specifications and the chosen circuit, i.e., realizations of the latter will not generally fill the window.

Figure 4 depicts the consequences of a design outcome lying directly on the boundary of R_a. Here, we notice that the response just touches one of the specifications at a frequency point. In the past, commercial CAD packages could not distinguish between points in R_a because the objective function they employed was programmed to produce a zero value everywhere in R_a. Optimizers could "die" as soon as they hit or crossed the boundary of R_a.

A family of possible responses produced by assumed uniformly distributed outcomes of actual circuits with independent designable physical parameters lying within a rectangular tolerance region around a nominal design is shown in Fig. 5. In particular, the yield is 100 percent and could have been produced by a worst-case tolerance optimization algorithm, not currently available in commercial microwave CAD systems. Notice the corresponding distorted region of acceptable models. The distortions are, of course, due to the nonlinear dependence of typical equivalent circuit parameters on lower-level physical parameters.

Figure 6 shows the case when the yield is less than 100 percent. For such problems it is necessary for the manufacturer to create a data base for components from which statistical distributions can be inferred and used.

We see that if the specifications for the case of Fig. 5 are tightened without any reoptimization then the yield drops from 100 percent. If the specifications of Fig. 6 are relaxed then the yield will increase without any optimization.

Performance driven nominal design, as has been mentioned earlier, is the conventional approach used by microwave engineers. In nominal design we seek a single point in the space of designable variables which best meets a given set of performance specifications and design constraints. Suitable scalar measures of deviation between responses and specifications, namely objective functions to be minimized, are the least squares measure, the generalized least pth objective or the minimax objective.

Figure 7 shows a possible starting point (labelled a) in a parameter space which violates the specifications, a barely acceptable solution (labelled b) on the boundary of R_a and an interior optimized solution (labelled c).

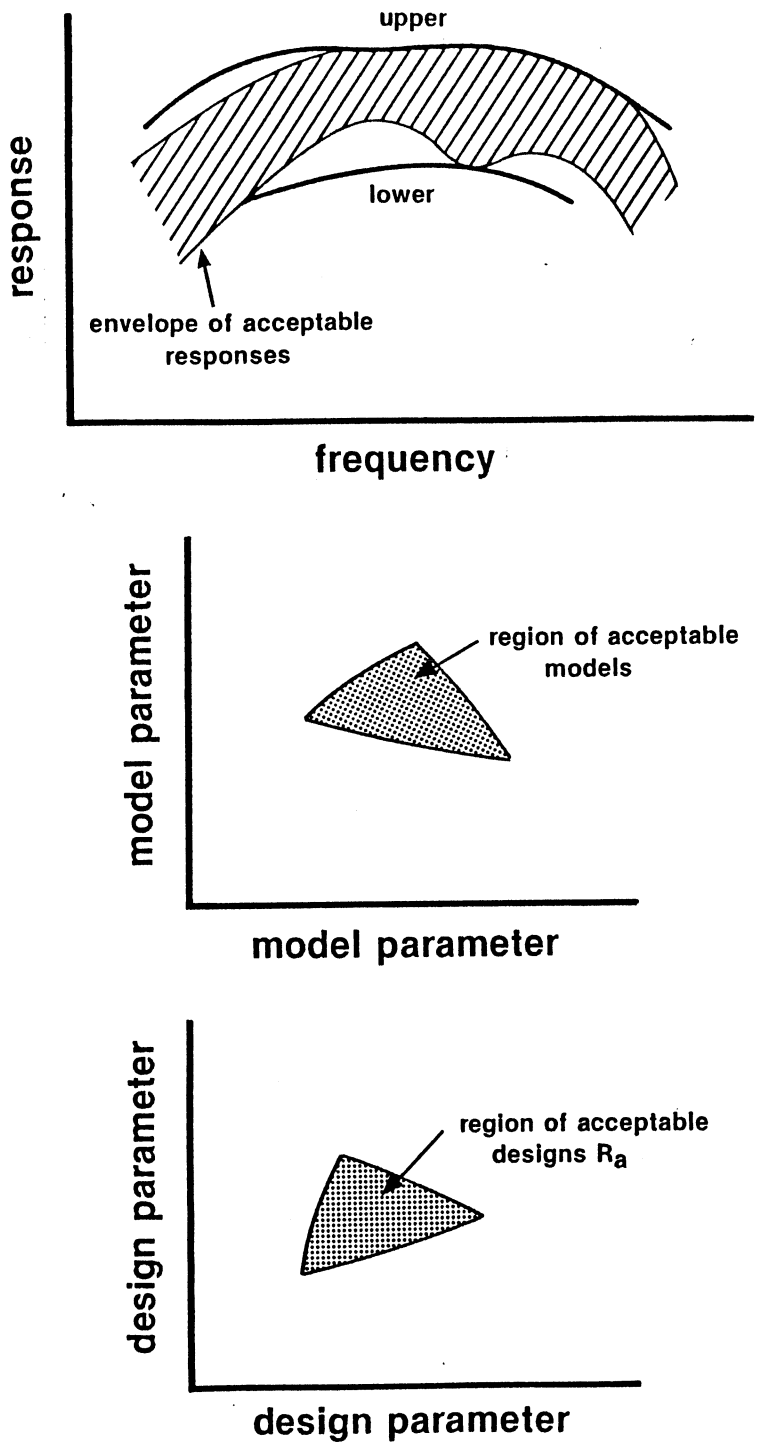

Fig. 3 The region of acceptable designs R_a, the region of corresponding equivalent circuit models and an envelope of acceptable responses.

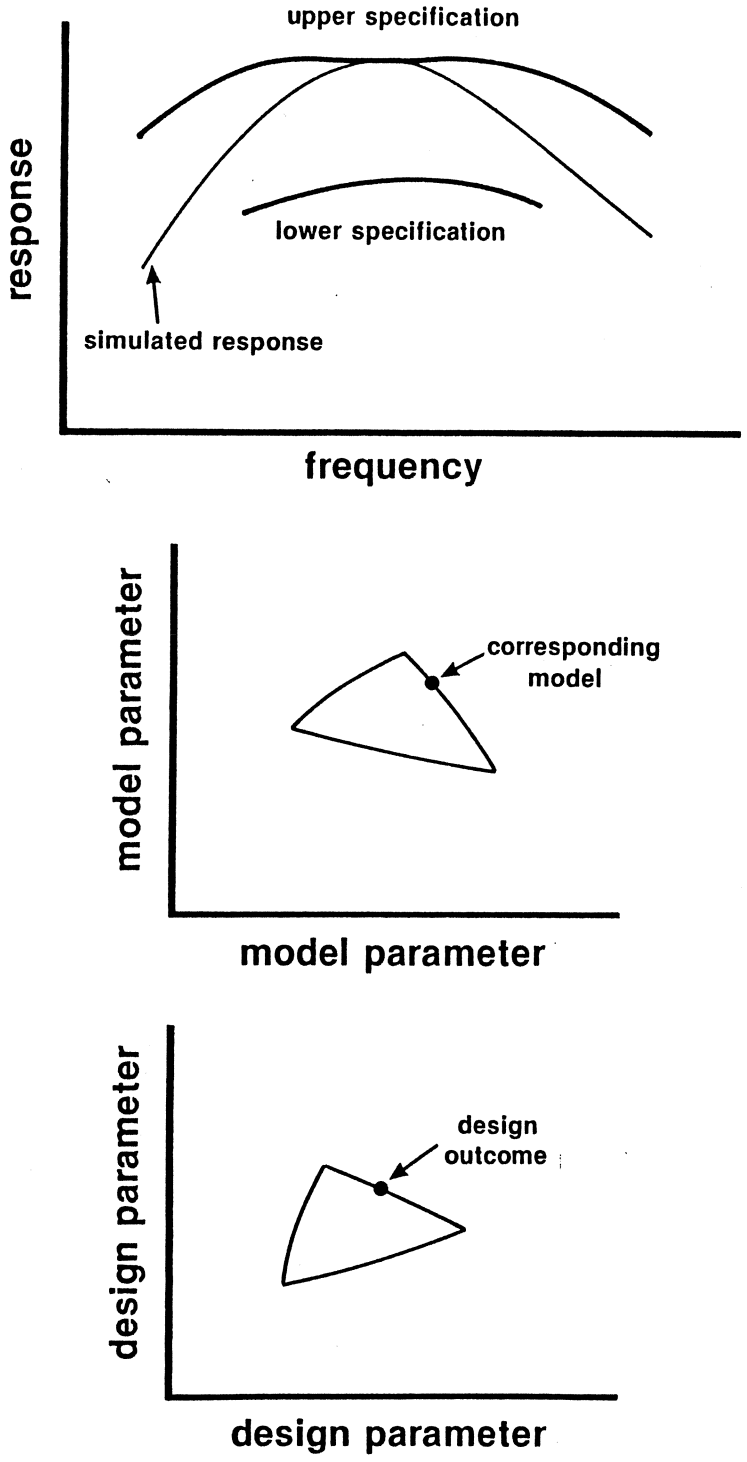

Fig. 4 An outcome lying directly on the boundary of R_a and its response. Compare with Fig. 2.

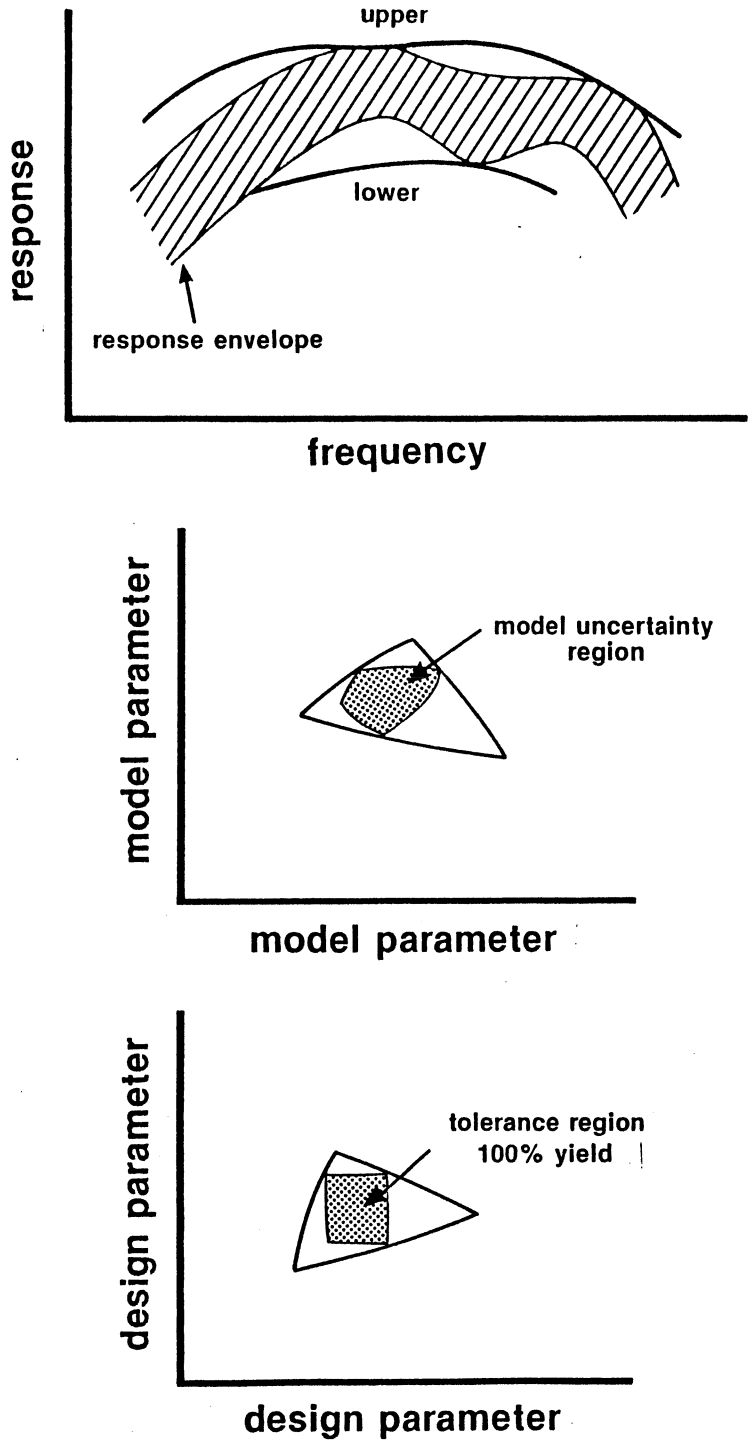

Fig. 5 A family of possible responses produced by assumed uniformly distributed outcomes of actual circuits with independent designable physical parameters lying within a rectangular tolerance region. The example is for 100 percent yield.

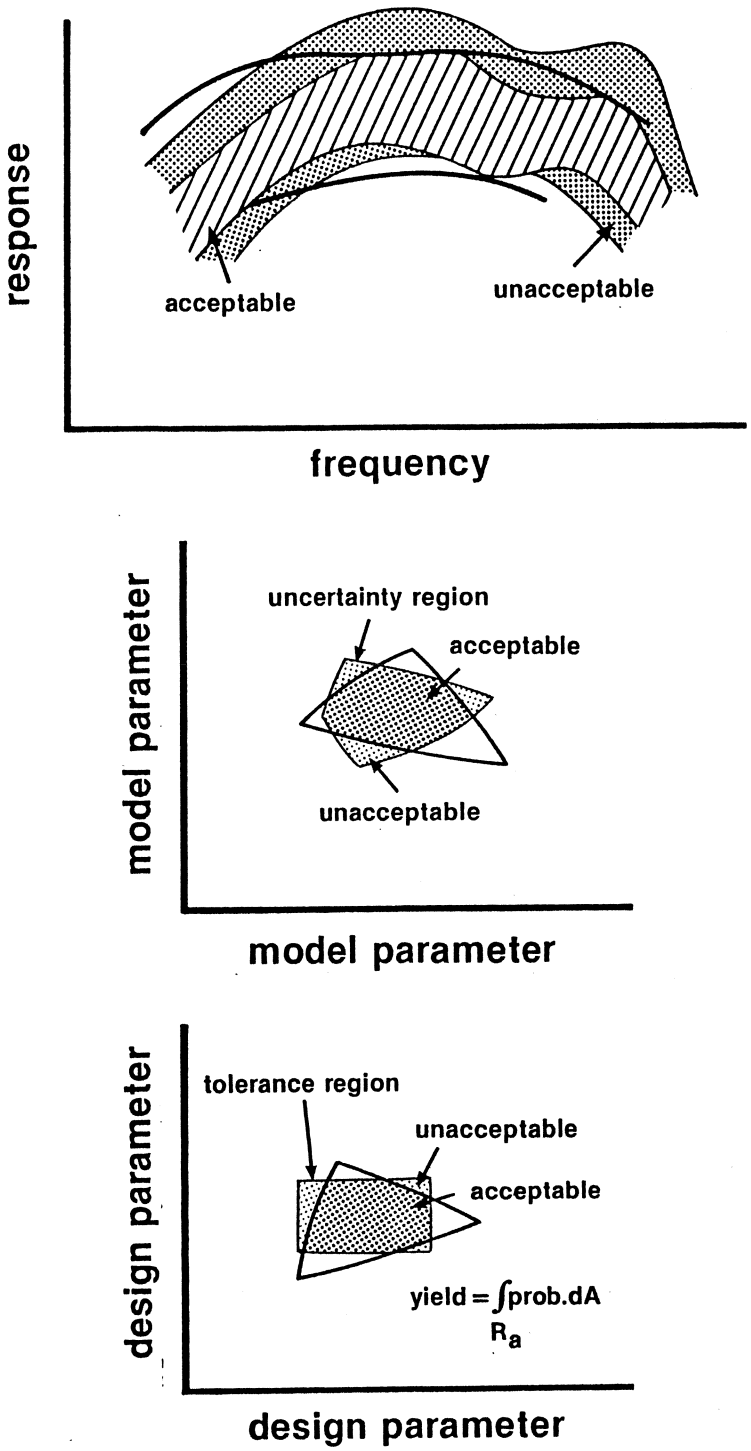

Fig. 6 A situation similar to that of Fig. 5, but when the yield is less than 100 percent.

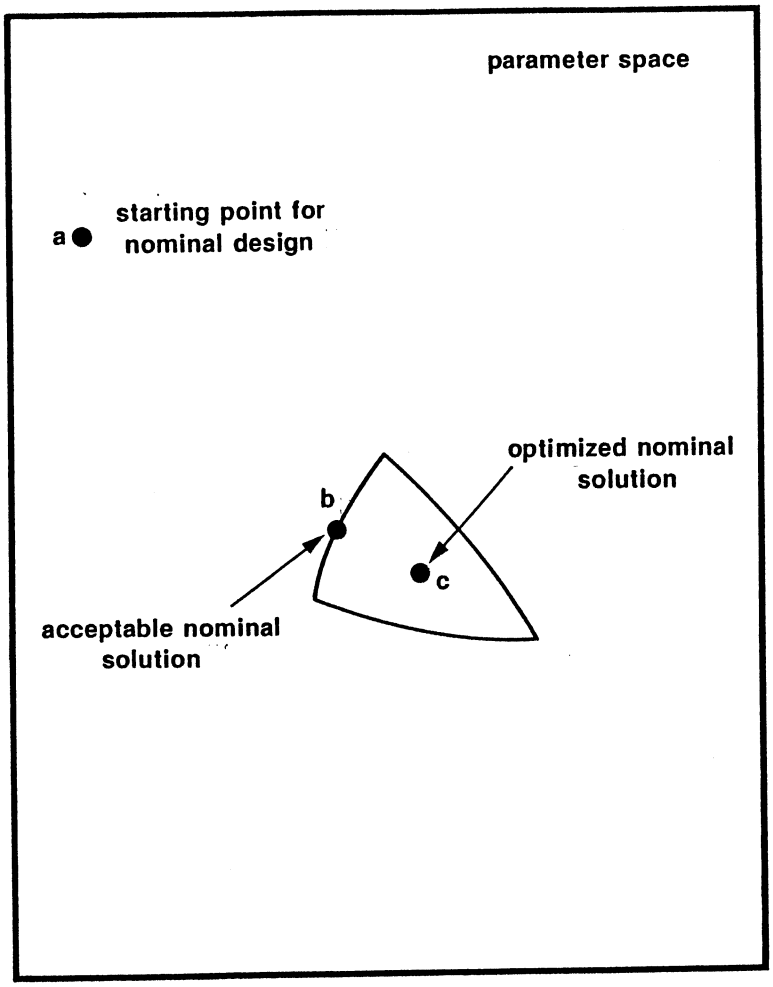

Fig. 7 A starting point for optimization (labelled a) which violates the specifications, a barely acceptable solution (labelled b) on the boundary of R_a and an interior optimized solution (labelled c).

Figure 8 attempts to illustrate the consequences of considering yield at the three points: initiating any yield analysis or optimization prematurely at a is a waste of effort, initiating a yield analysis or optimization at b is too early, whereas c provides an excellent point from which to initiate yield optimization.

Figure 9 shows a 100 percent yield optimized solution as well as a minimum cost solution with yield less than 100 percent.

While tuning is not desirable in MMICs, the concept of tuning is widespread and needs theoretical interpretation. Figure 10 illustrates the case when the yield (optimized or not) may be so low that tuning is essential. Here, one variable is tunable and the other is taken as untunable. Tunable points are cleary seen. These points are all regarded as contributing positively to yield. Nontunable points are also depicted. They do not contribute to yield. If the yield, even after tuning is still too low the designer may need to consider a new topology, more tuning variables, a different manufacturing process, etc.

In certain customized products, e.g., manifold multiplexers, the design situation is of the type shown in Fig. 11. Here, the probability that an untuned outcome meets the specifications may be inestimably low. Very costly, labour intensive tuning of nearly every manufactured variable (perhaps hundreds) may need to be undertaken. Any optimized single point, in this case, obviously represents mere feasibility. A yield analysis has no relevance. Virtually total reliance on production alignment is necessary.

Microwave CAD activity seems to be spanned by the two extremes: desirably untunable MMICs on the one hand and almost totally tuned discrete component circuits.

While the anticipated immediate application of yield maximization techniques by microwave designers is to design problems involving linear systems of equations (small-signal, linear, time-invariant circuit analysis), nonlinear circuits (analyzed in the frequency or time domains) are of particular interest. It is, therefore, expected that considerable effort will be devoted to such systems in the near future. Fortunately, all the mathematical descriptions and formulations of the tolerance design problem are directly and profitably applicable to nonlinear integrated analog circuits.

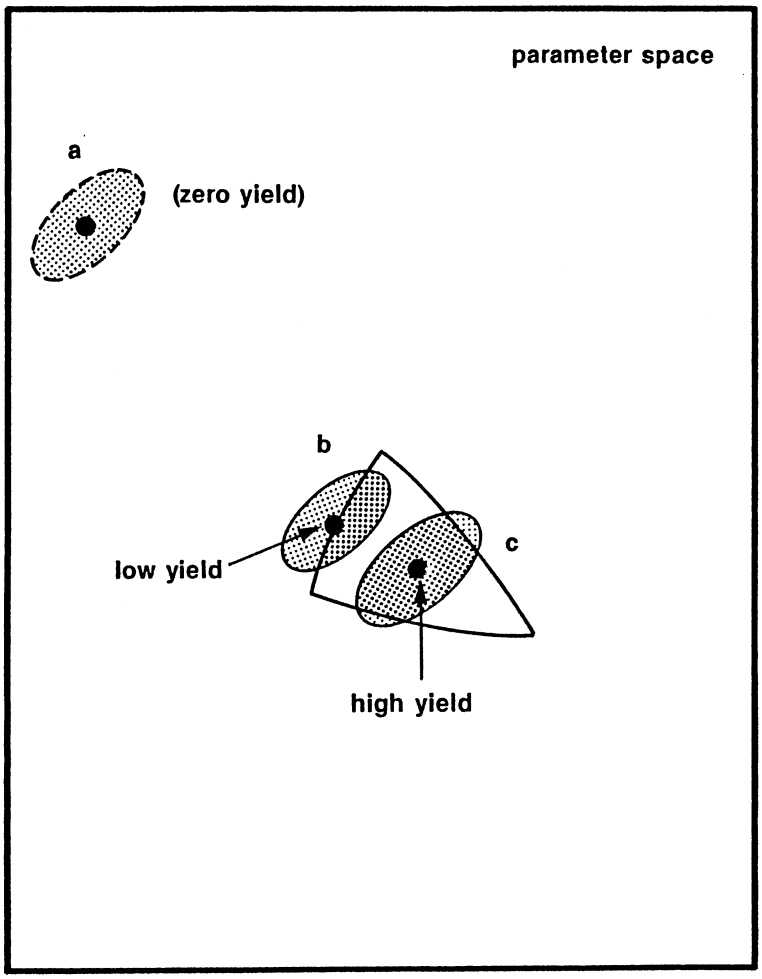

Fig. 8 The consequences of considering yield at the three points of Fig. 7: initiating any yield analysis or optimization at a is a waste of effort, initiating one at b is too early, whereas c provides an excellent starting point for yield optimization.

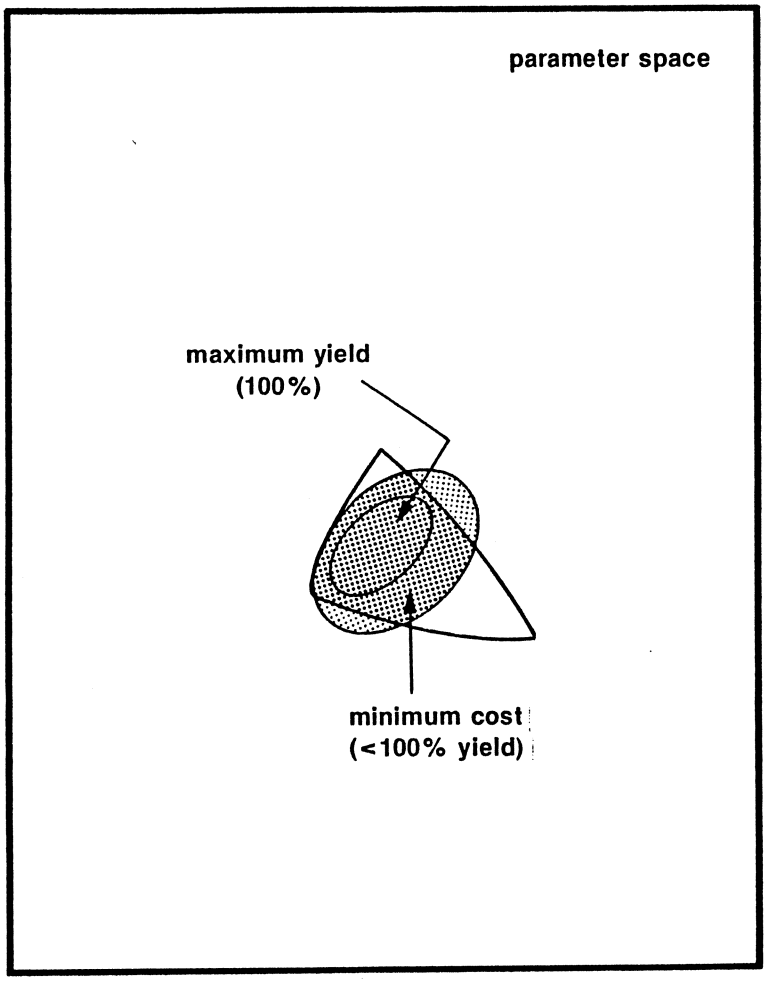

Fig. 9 A 100 percent yield optimized solution as well as a possible minimum cost solution with yield less than 100 percent.

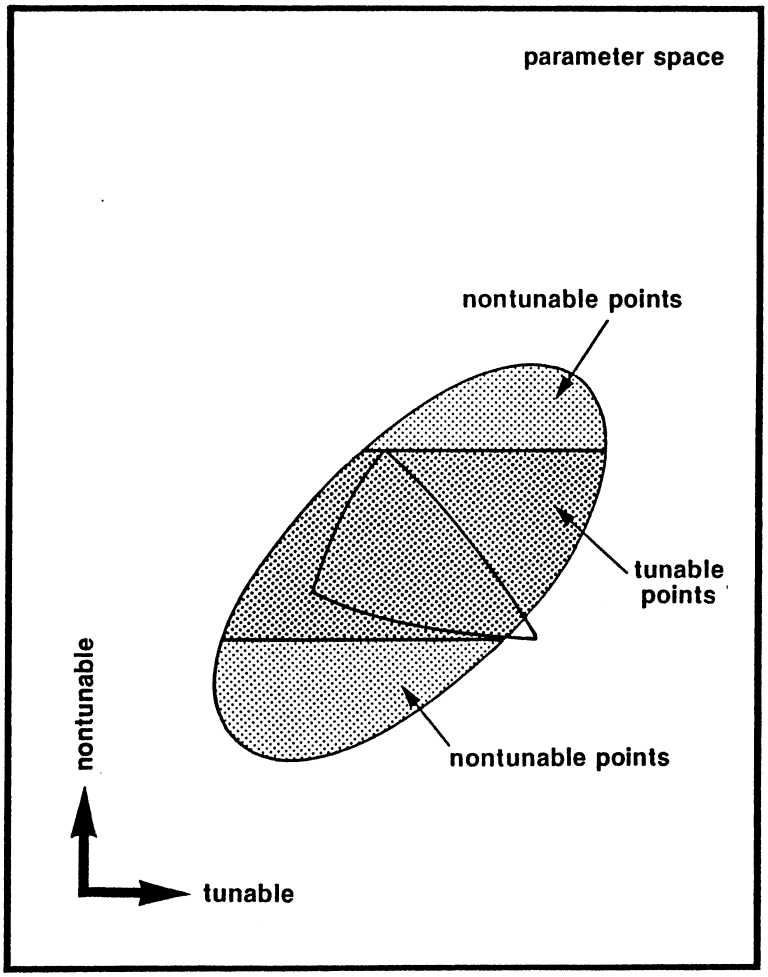

Fig. 10 An example for the case when the yield (optimized or not) is considered to be so low that tuning of a variable is essential. Tunable points regarded as contributing positively to yield are cleary seen.

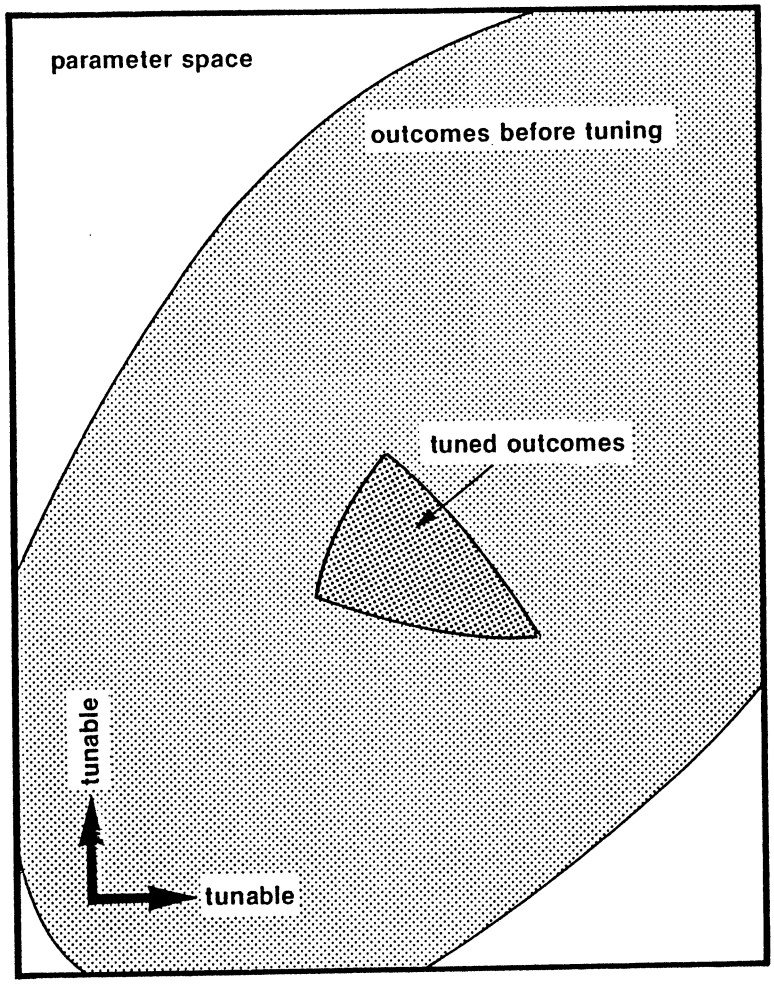

Fig. 11 A design situation in which the probability that an untuned outcome meets the specifications is very low. In such cases tuning of (nearly) every manufactured variable (perhaps hundreds) may need to be undertaken.

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