SIMULATION OPTIMIZATION SYSTEMS
Research Laboratory

CAD WITH TOLERANCES

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SOS-98-2-V

March 1998

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presented at

WORKSHOP ON COMPUTER-AIDED DESIGN FOR MANUFACTURABILITY

1998 IEEE MTT-S Int. Microwave Symposium, Baltimore, MD, June 12, 1998

Introduction

design with tolerances, yield-driven design, design centering: methodologies indispensable for today's RF, wireless and microwave CAD

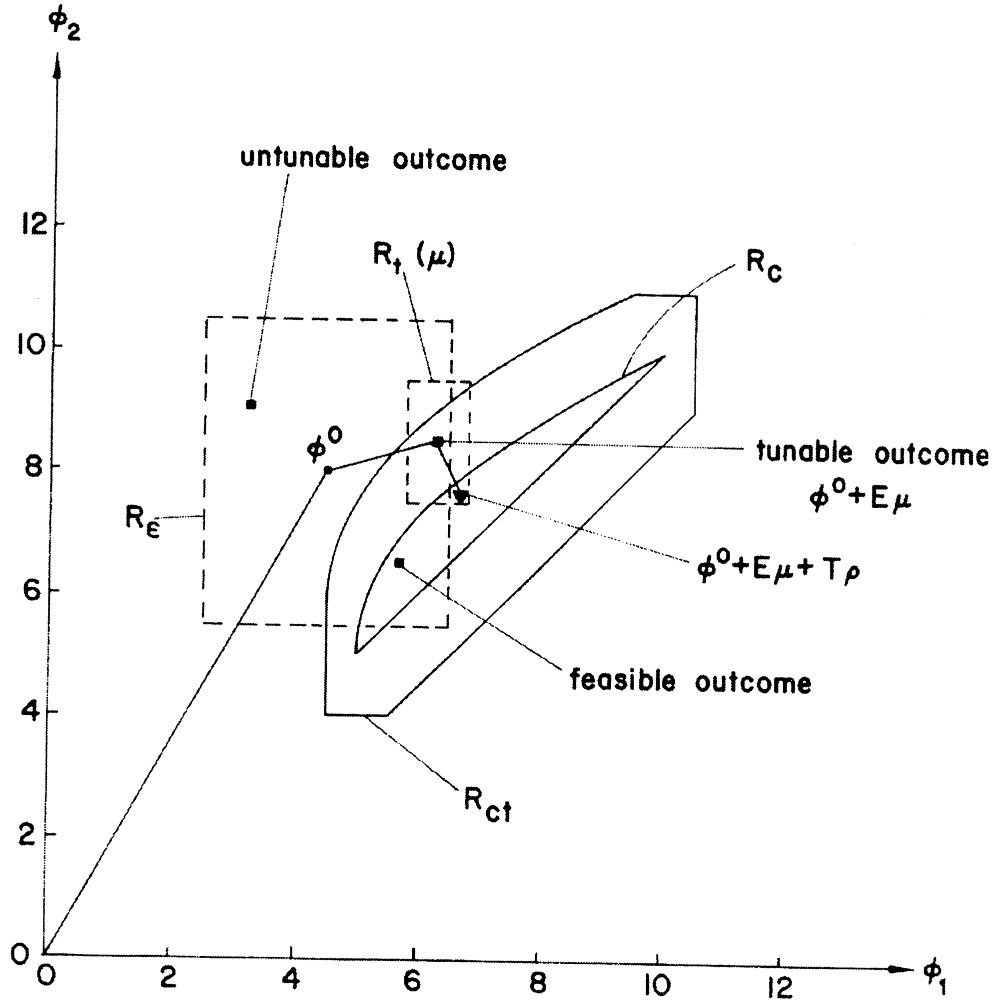
suitably integrated design methodologies take into account manufacturing tolerances and model uncertainties

microwave designers continue to use different CAD systems to address different aspects of their designs; may be tedious and time consuming because of incompatible user interfaces and data formats

we suggest a flexible approach to mixed-domain, multi-simulator yield-driven design

we integrate time-domain, frequency-domain and EM simulations into a versatile optimization environment with tolerances

Design Centering, Tolerancing and Tuning using Mathematical Optimization



Increasing Sophistication of Design Methodology with Tolerances

DCTT: Design Centering, Tolerancing and Tuning using mathematical optimization (*1970s*)

deterministic (*Bandler et al., 1976*)

performance-driven design

fixed tolerance worst-case design

variable tolerance worst-case design

full DCTT

statistical (*see Bandler and Chen, 1988*)

fixed tolerance yield-driven design

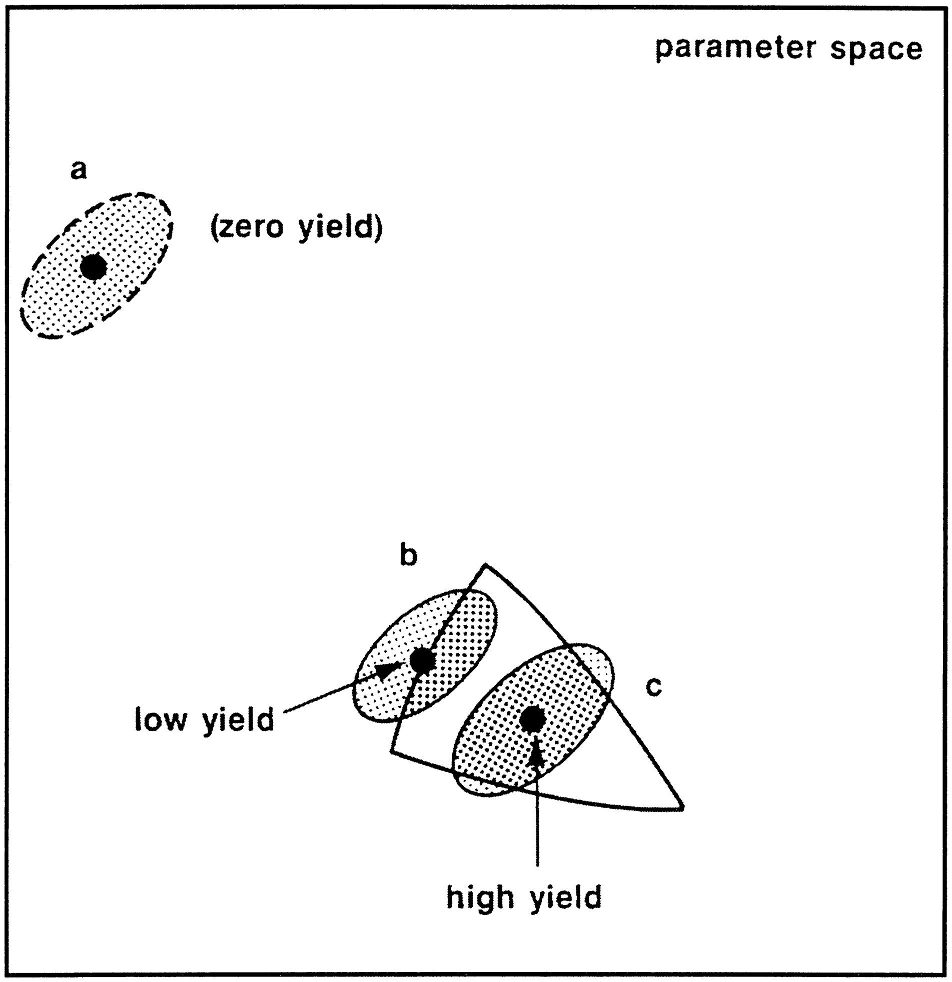
correlated tolerances

variable tolerance cost-driven design

CAD goal: first-pass success design, however...

role of tuning: tunable designs may be considered in which tunable variables are assigned possible ranges at the design stage; followed by postproduction testing and tuning

Yield Interpretation in the Parameter Space



Overview of Presentation

historical perspective (early work at Bell Labs, *Karafin 1971*)

the need for physics-based yield optimization of integrated circuits

the role of electromagnetic (EM) optimization

yield optimization of a distributed attenuator using distributed (parallel) computations

mixed-domain multi-simulator yield-driven design using SPICE, OSA90/hope, and Sonnet's ***em***

tolerance optimization of waveguide multiplexers

Space Mapping (SM) optimization

SM optimization using hybrid mode-matching (MM) /network theory and finite-element (FEM) models

Monte Carlo analysis of manufacturing tolerances using SM

Physics-Based Yield Optimization of MMICs

random variations in manufacturing process may lead to some circuits failing to meet design specifications

production tuning of MMICs is restricted

component replacement is not possible

circuits are manufactured in batches rather than individually

the cost is directly affected by yield

the ability to predict and enhance production yield is critical

accurate EM simulations of passive elements and physical simulations of active devices enhanced by Space Mapping optimization

Yield Optimization of a Three-Stage MMIC Amplifier
(*Bandler et al., 1992*)

the three-stage X-band MMIC amplifier is based on the circuit topology and fabrication layout originally designed by Thomson-Semiconductors (*Kermarrec and Rumelhard, 1988*)

intended as a gain block for phased-array antennas

the amplifier contains three GaAs MESFETs using an interdigitated structure with two gate fingers of dimensions 150 μm × 1.0 μm

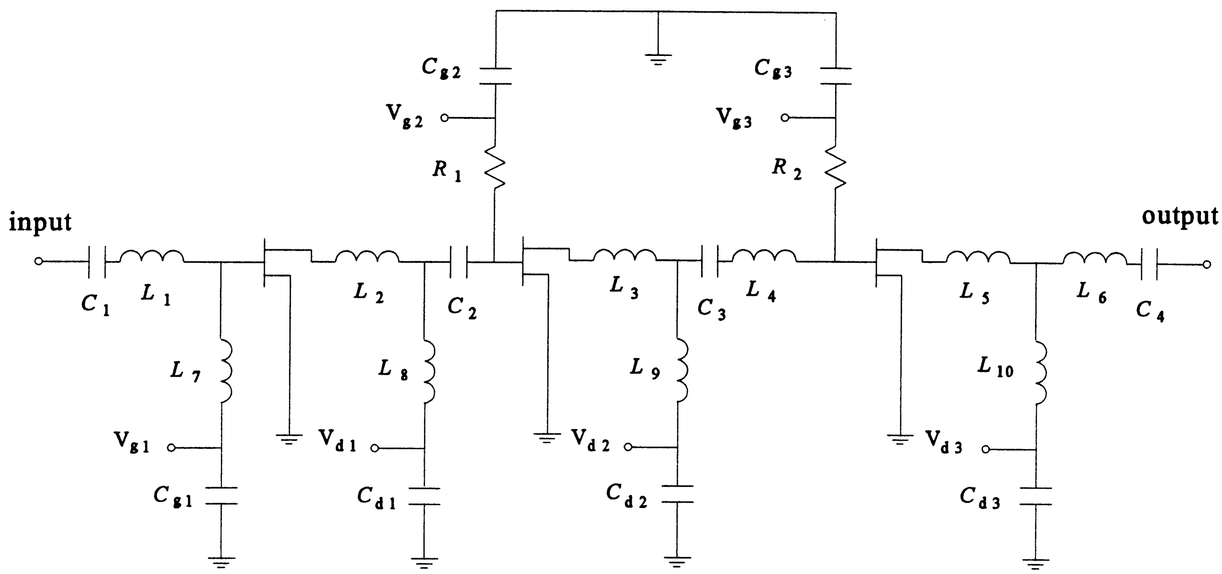
all passive elements are realized using lumped MMIC elements: spiral inductors, MIM capacitors and bulk resistors

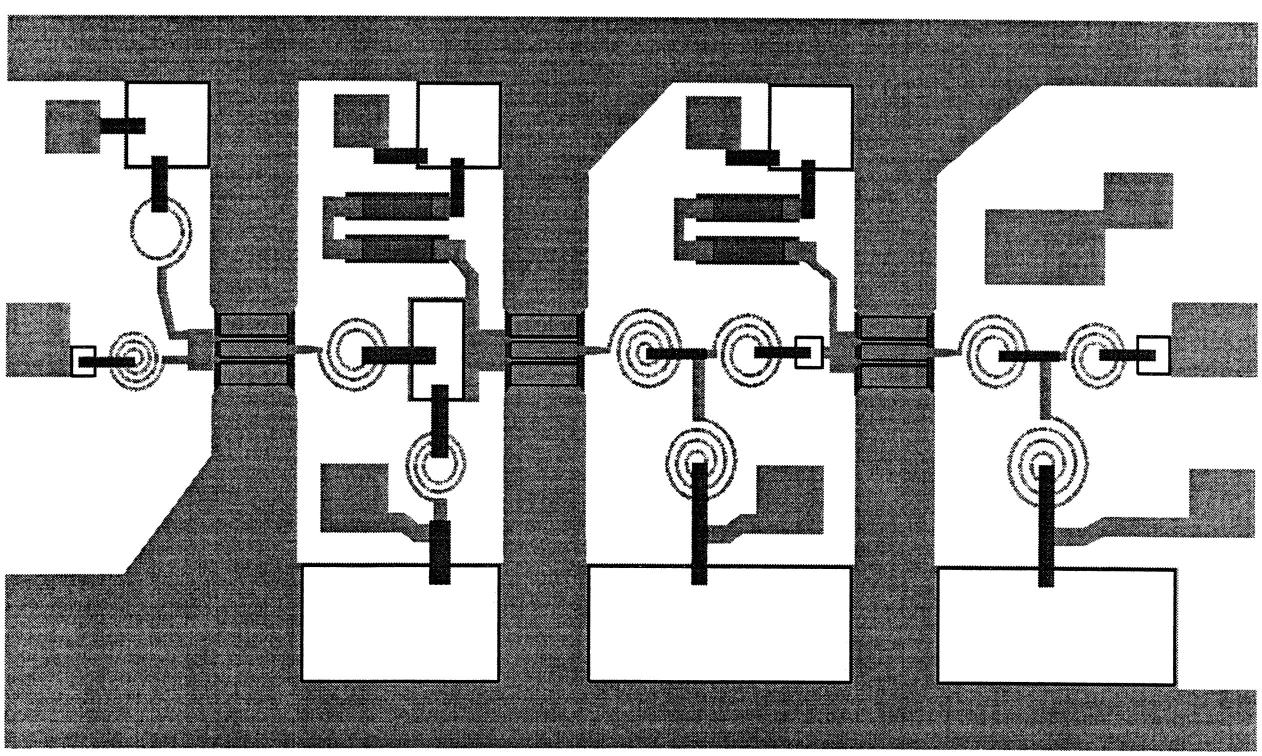
37 statistical variables with correlations and 16 design variables

yield optimization carried out by OSA90/hope

yield is improved from 26% at the nominal design to 69%

Circuit Schematic and Layout of the Three-Stage Amplifier





Predictable Yield-Driven Circuit Optimization
(*Bandler et al., 1992*)

usefulness of yield-driven design depends on the accuracy of yield estimated using the statistical model

yield predicted by Monte Carlo simulation using the model should be consistent with the yield predicted directly from the device measurement data

the advantage of a statistical model over the measurement data is that the model provides for convenient interpolation

the selection of device parameters for yield optimization can be assisted by yield sensitivity analyses

the yield can be significantly increased by simultaneous circuit-device optimization

design of a small-signal broadband amplifier is investigated using OSA90/hope with the KTL model w.r.t. a number of specifications

the predicted yield is verified using the device data

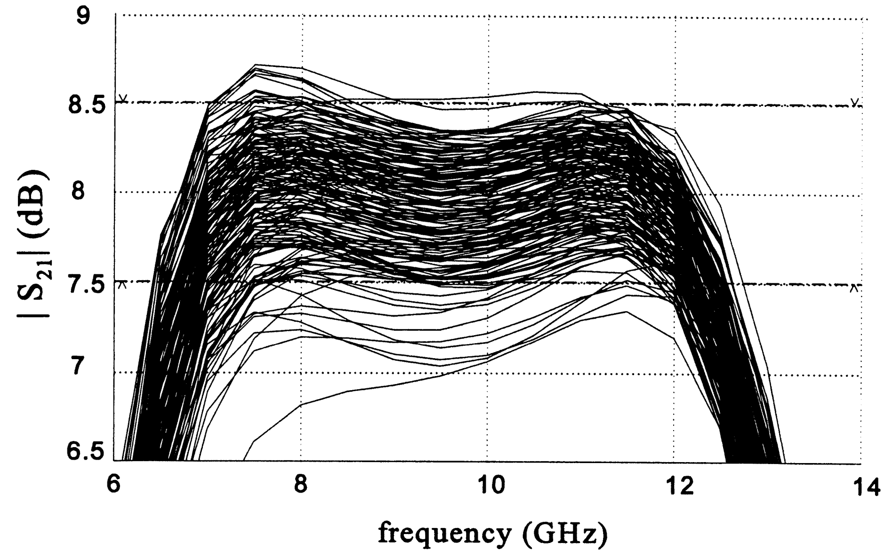
YIELD VERIFICATION

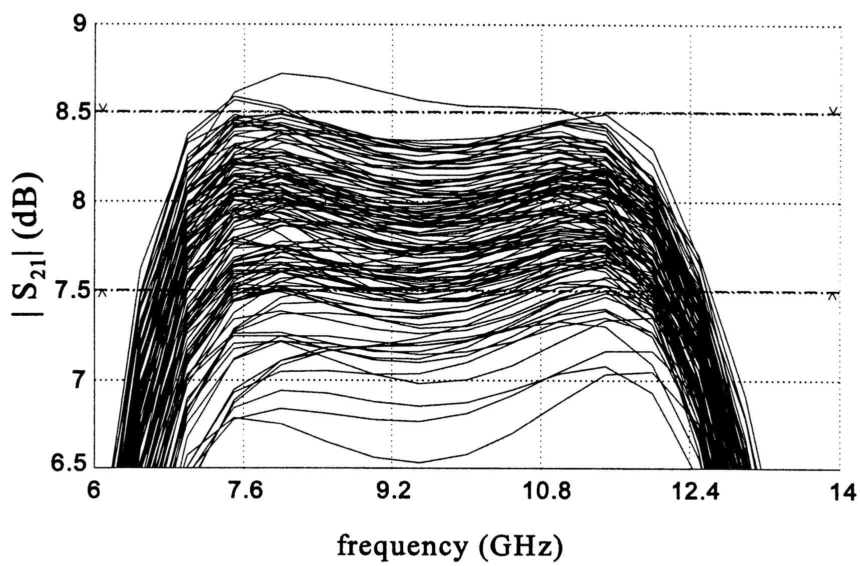
	Before Yield Optimization		After Yield Optimization	
	Predicted Yield (%)	Verified Yield (%)	Predicted Yield (%)	Verified Yield (%)
Spec. 1	17.5	15.7	67	57.9
Spec. 2	21	20	83	75.7
Spec. 3	44	37.1	98	93.6

Spec. 1: $7.5\text{dB} < |S_{21}| < 8.5\text{dB}$, $|S_{11}| < 0.5$, $|S_{22}| < 0.5$
Spec. 2: $6.5\text{dB} < |S_{21}| < 7.5\text{dB}$, $|S_{11}| < 0.5$, $|S_{22}| < 0.5$
Spec. 3: $6.0\text{dB} < |S_{21}| < 8.0\text{dB}$, $|S_{11}| < 0.5$, $|S_{22}| < 0.5$

200 Monte Carlo outcomes are used for predicted yield, 140 for verified yield

Gain After Optimization from Model and from Data





Physics-Based Cost-Driven Design
(*Bandler et al., 1995*)

yield optimization maximizes the yield by adjusting the nominal values of the design variables keeping tolerances fixed

the cost for obtaining small tolerances may be very high

there is a trade-off between the yield and the cost

cost-driven design minimizes the cost while maintaining the required yield

cost-driven optimization

$$\underset{\boldsymbol{x}}{\textit{minimize}} \quad C(\boldsymbol{x})$$

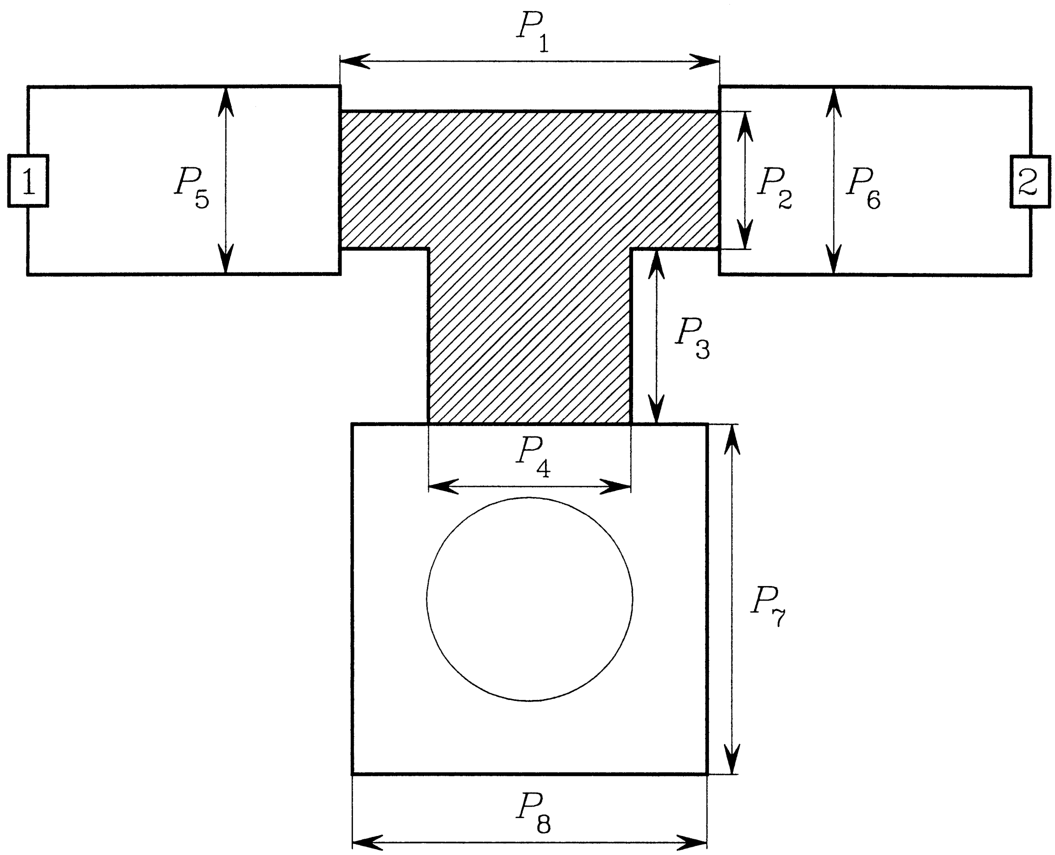
$$\textit{subject to} \;\; Y \geq Y_S$$

$\boldsymbol{x}$ vector of parameter tolerances
Y design yield
Y_S specified yield
$C(\boldsymbol{x})$ cost function, e.g.,

$$C(\boldsymbol{x}) = \sum_{i=1}^{m} \frac{c_i}{x_i}$$

10 dB Distributed Attenuator Design

(*Bandler et al., 1995*)



built on a 15 mil thick substrate with relative dielectric constant of 9.8

metallization of a high resistivity (50 Ω/sq)

the feed lines and the grounding pad are assumed lossless

Statistical Design of the Attenuator

design specifications (from 2 GHz to 18 GHz)

$$9.5 \text{ dB} \leq \text{insertion loss} \leq 10.5 \text{ dB}$$
$$\text{return loss} \geq 10 \text{ dB}$$

the structure, treated as a whole, has 8 geometrical parameters

designable: 4 parameters describing the resistive area

statistical: 8 parameters (with a standard deviation of 0.25 mil)

em simulation at a single frequency requires about 7 CPU minutes on a Sun SPARCstation 1+

Distributed (Parallel) Computing

nominal design: 30 ***em*** analyses with an average of 3.8 analyses run in parallel

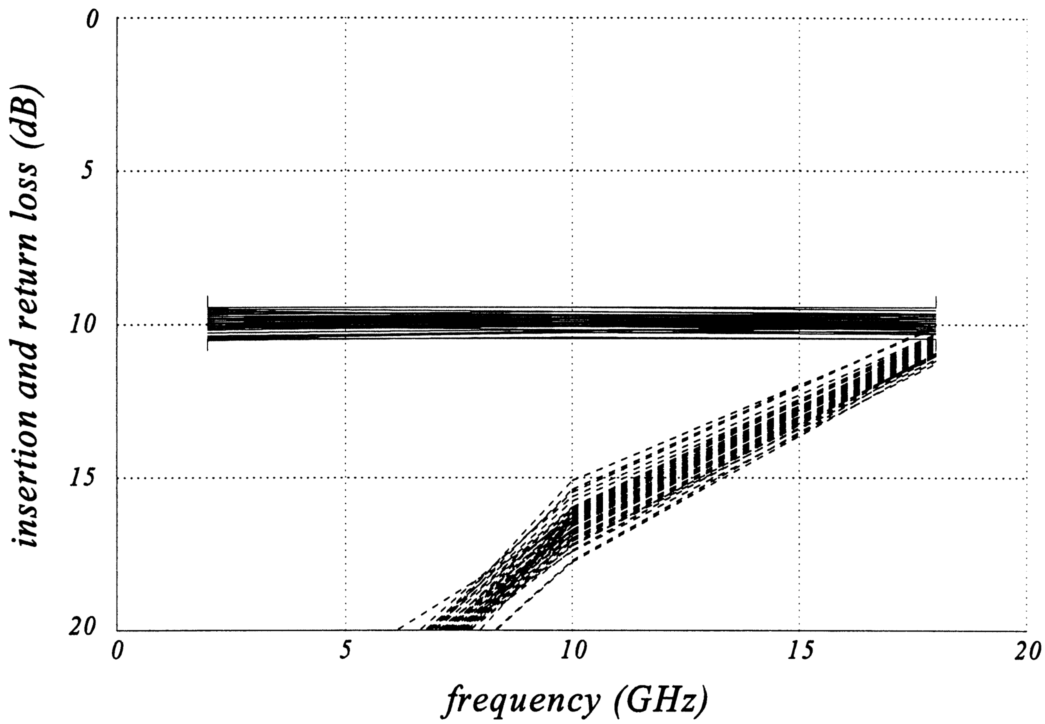
about 168 minutes on the network of Sun SPARCstations 1+

time is reduced by 75%

statistical design: additional 113 ***em*** analyses with an average of 2.5 analyses run in parallel

time is reduced by 60%

Monte Carlo Sweeps of the Attenuator Responses



yield (estimated from 250 Monte Carlo outcomes) is increased from 82% to 97%

Mixed-Domain Multi-Simulator Yield-Driven Design
(*Bandler et al., 1997*)

n_o outcomes are used in yield optimization

for all outcomes $\boldsymbol{\phi}^i$ the parent integrates the results returned from each child and performs the circuit-level simulation

$$R_P(\boldsymbol{\phi}^i) = R_P(\boldsymbol{\phi}^i, R_{C_1}(\boldsymbol{\phi}^i), R_{C_2}(\boldsymbol{\phi}^i), \ldots, R_{C_m}(\boldsymbol{\phi}^i))$$

where

R_P	circuit-level responses simulated by the parent
R_{C_k}	subcircuits simulated by the *k*th child

in general

$$R_{C_k}(\boldsymbol{\phi}^i) = R_{C_k}(R^t_{C_k}(\boldsymbol{\phi}^i), R^f_{C_k}(\boldsymbol{\phi}^i), R^e_{C_k}(\boldsymbol{\phi}^i))$$

where

$R^t_{C_k}$	time-domain responses
$R^f_{C_k}$	frequency-domain responses
$R^e_{C_k}$	EM responses

each child is usually devoted to only one type of simulation

Formulation for Yield-Driven Design

error functions

$$e_j(\boldsymbol{\phi}^i) = R_{P_j}(\boldsymbol{\phi}^i) - S_j \qquad \text{upper specifications}$$

$$e_j(\boldsymbol{\phi}^i) = S_j - R_{P_j}(\boldsymbol{\phi}^i) \qquad \text{lower specifications}$$

for all outcomes $\boldsymbol{\phi}^i$ and all specifications S_j, $j = 1, 2, ..., n_s$

outcome $\boldsymbol{\phi}^i$ is acceptable if all $e_j(\boldsymbol{\phi}^i)$, $j = 1, 2, ..., n_s$, are nonpositive (all design specifications are satisfied)

design yield

the ratio of acceptable outcomes to the total number of outcomes considered

yield-driven design formulation

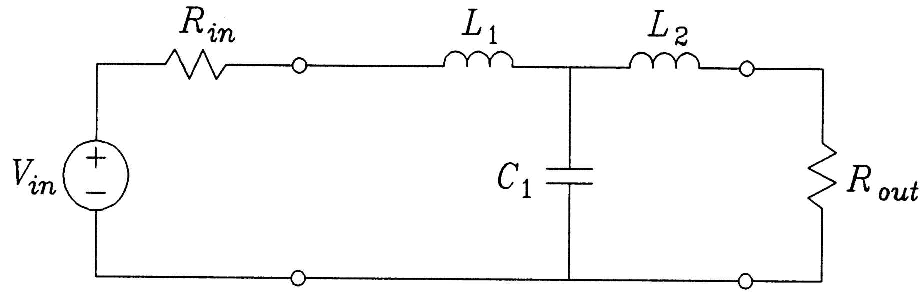
$$\underset{\boldsymbol{\phi}^0}{minimize} \quad U(\boldsymbol{\phi}^0) = \sum_{i=1}^{n_o} H[\alpha_i v(\boldsymbol{\phi}^i)]$$

where

α_i	positive multipliers
$v(\boldsymbol{\phi}^i)$	the generalized ℓ_p function
H	one-sided ℓ_1 or one-sided Huber

Mixed-Domain Multi-Simulator Yield-Driven Design: Example

a simple low-pass filter



specifications defined in the frequency domain

insertion loss $\leq$ 1.5 dB for $0 < \omega < 1$
insertion loss $\geq$ 25 dB for $\omega > 2.5$

and in the time domain

$0.45 \text{ V} \leq V_{out} \leq 0.55 \text{ V}$ for $3.5 \text{ s} < t < 20 \text{ s}$

design variables: L_1, L_2 and C_1 with a uniform distribution within a 10% tolerance

time-domain simulation performed by SPICE

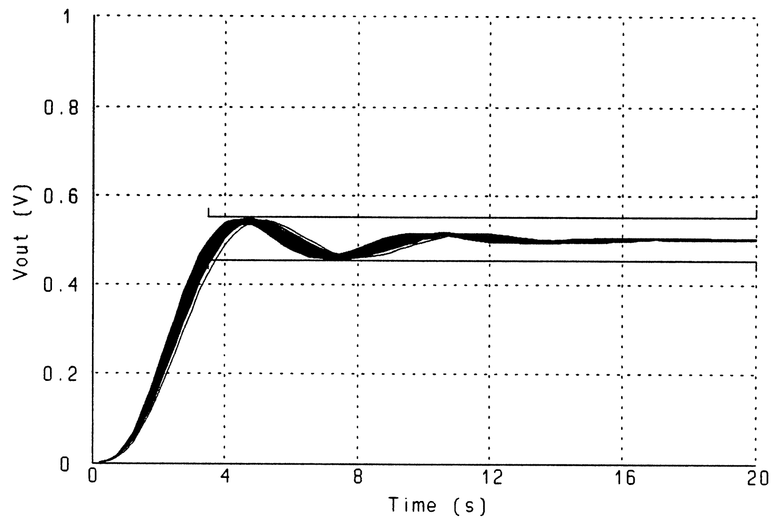
frequency-domain simulation performed by OSA90/hope

mixed-domain optimization performed by OSA90/hope

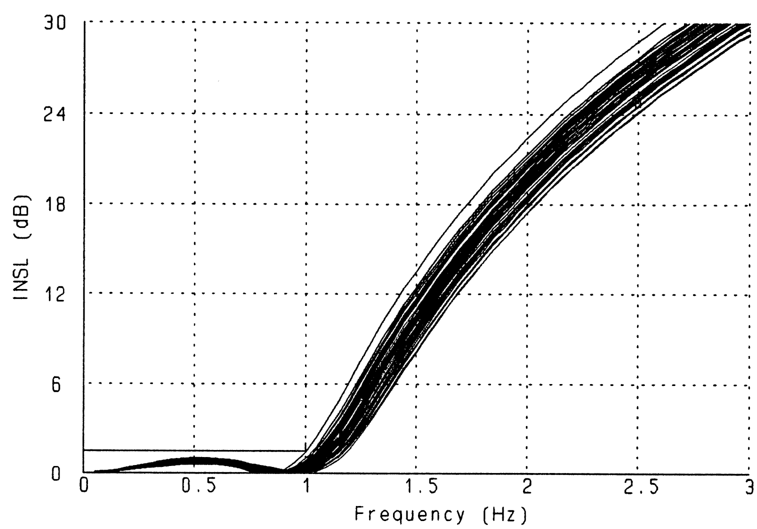
nominal design followed by yield optimization

Statistical Responses of the Low-Pass Filter

time-domain Monte Carlo sweep



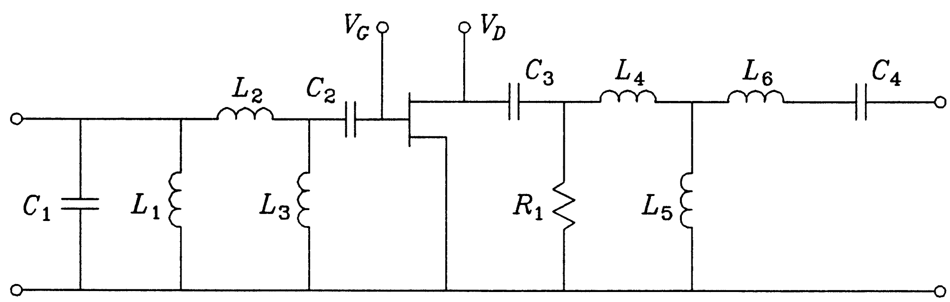
frequency-domain Monte Carlo sweep



yield is increased from 29% at the nominal design to 67% after optimization

Yield-Driven Design of an Amplifier

a small-signal amplifier



design specifications (for frequencies from 8 to 12 GHz)

$7.25 \text{ dB} < |S_{21}| < 8.75 \text{ dB}$
$|S_{11}| < 0.5$
$|S_{22}| < 0.5$

design variables

the matching circuit elements $L_1, L_2, L_3, L_4, L_5, L_6, C_1, C_2, C_3, C_4$ and R_1

28 statistical parameters

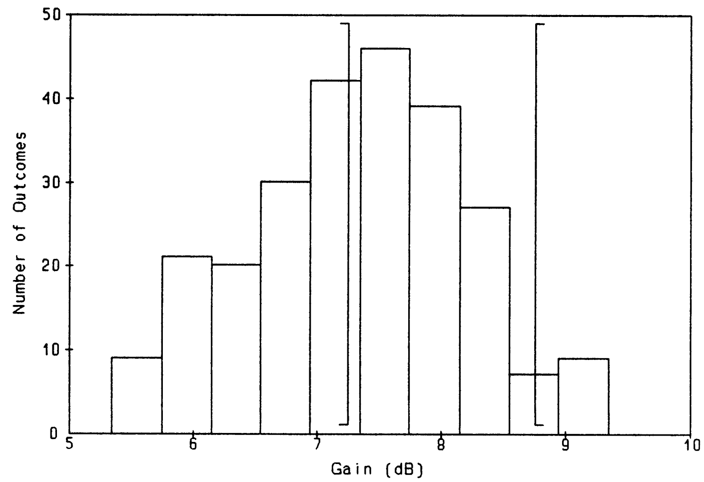
uniform distribution within a 5% tolerance

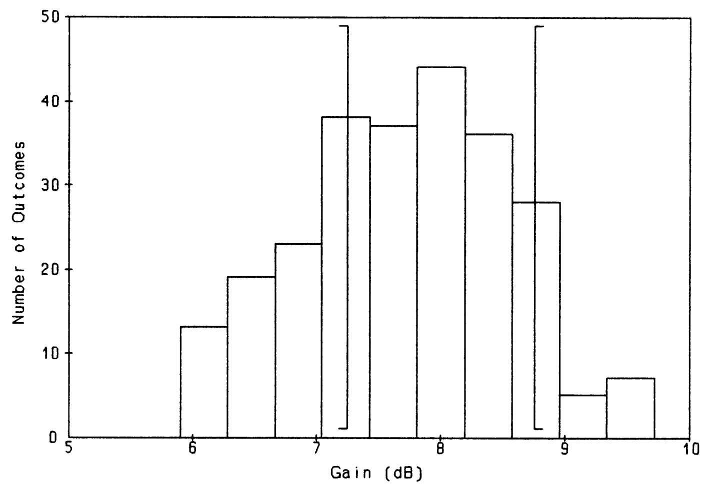
the MESFET is simulated in SPICE

SPICE results are returned to OSA90/hope through Spicepipe for circuit-level simulation and optimization

Histograms Before and After Yield Optimization

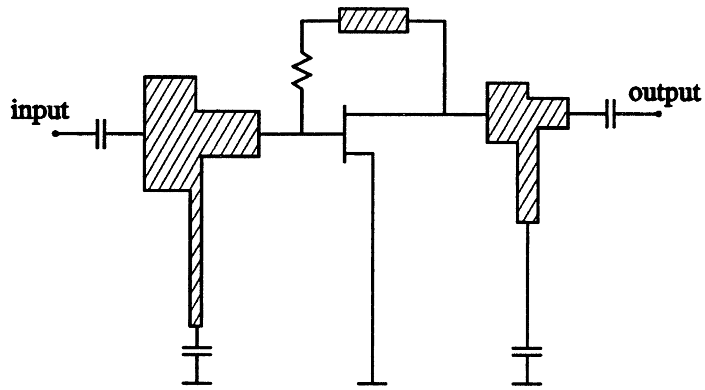
$|S_{21}|$ at 12 GHz



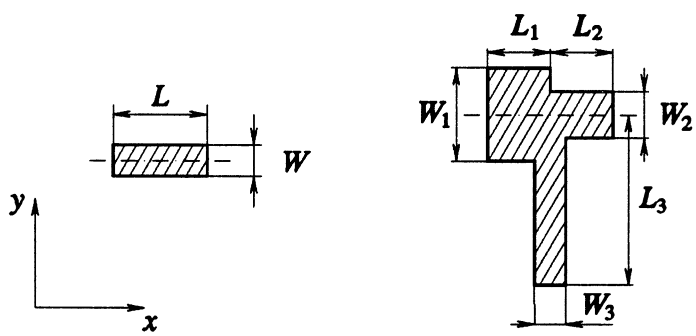


yield is increased from 16% at the nominal design to 52% after optimization

A Broadband Small-Signal Amplifier



parameters of the feedback microstrip line and the microstrip T-structures



design specifications

$$7 \text{ dB} \leq |S_{21}| \leq 8 \text{ dB} \quad \text{for} \quad 6 \text{ GHz} \leq f \leq 18 \text{ GHz}$$

design variables

gate T-structure: $W_{g1}, L_{g1}, W_{g2}, L_{g2}$

drain T-structure: $W_{d1}, L_{d1}, W_{d2}, L_{d2}$

Combined *em*/SPICE Yield-Driven Design
(*Bandler et al., 1997*)

the MESFET simulated by SPICE

microstrip components accurately simulated by Sonnet's *em*

the line and the *T*-structure primitives of the Empipe library are invoked

circuit-level simulation and optimization carried out by OSA90/hope

uniform distribution within a 0.5 mil tolerance for all geometrical parameters

yield at the nominal minimax solution is 43%

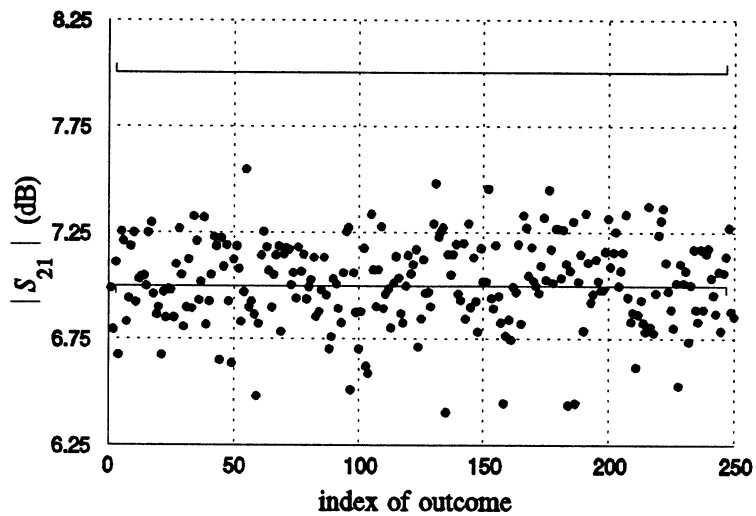
yield is increased to 74% after yield optimization

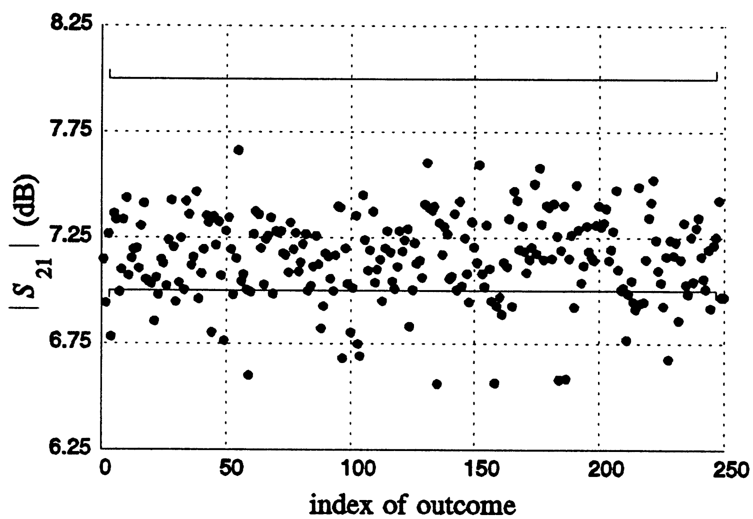
50 outcomes used for yield optimization

Run Charts Before and After Yield Optimization

$|S_{21}|$ at 18 GHz

250 outcomes

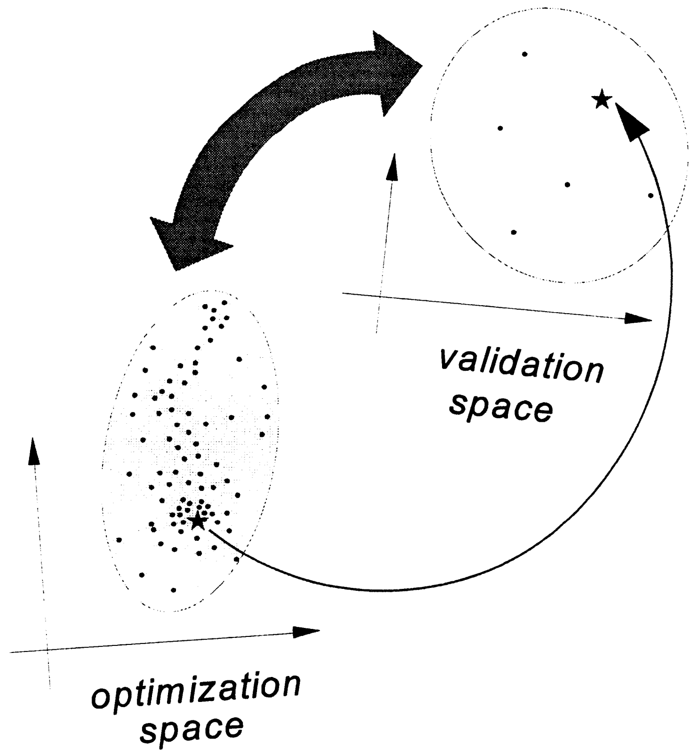




clearly, many more outcomes meet the specification after yield optimization

Space Mapping

(*Bandler et al., 1994*)



optimization or "coarse" model: $\boldsymbol{R}_{os}(\boldsymbol{x}_{os})$

EM, validation or "fine" model: $\boldsymbol{R}_{em}(\boldsymbol{x}_{em})$

Space Mapping: $\boldsymbol{x}_{os} = \boldsymbol{P}(\boldsymbol{x}_{em})$

such that $\boldsymbol{R}_{os}(\boldsymbol{P}(\boldsymbol{x}_{em})) \approx \boldsymbol{R}_{em}(\boldsymbol{x}_{em})$

Space Mapped solution: $\overline{\boldsymbol{x}}_{em} = \boldsymbol{P}^{-1}(\boldsymbol{x}_{os}^{*})$

fast response evaluation
for tolerance analysis: $\boldsymbol{R}_{os}(\boldsymbol{P}(\boldsymbol{x}_{em}))$

The Concept of Space Mapping

(*Bandler et al., 1994*)

we wish to find a mapping $\boldsymbol{P}(\boldsymbol{x}_{em})$ from the EM space $\boldsymbol{X}_{em}$ to the optimization space $\boldsymbol{X}_{os}$ such that

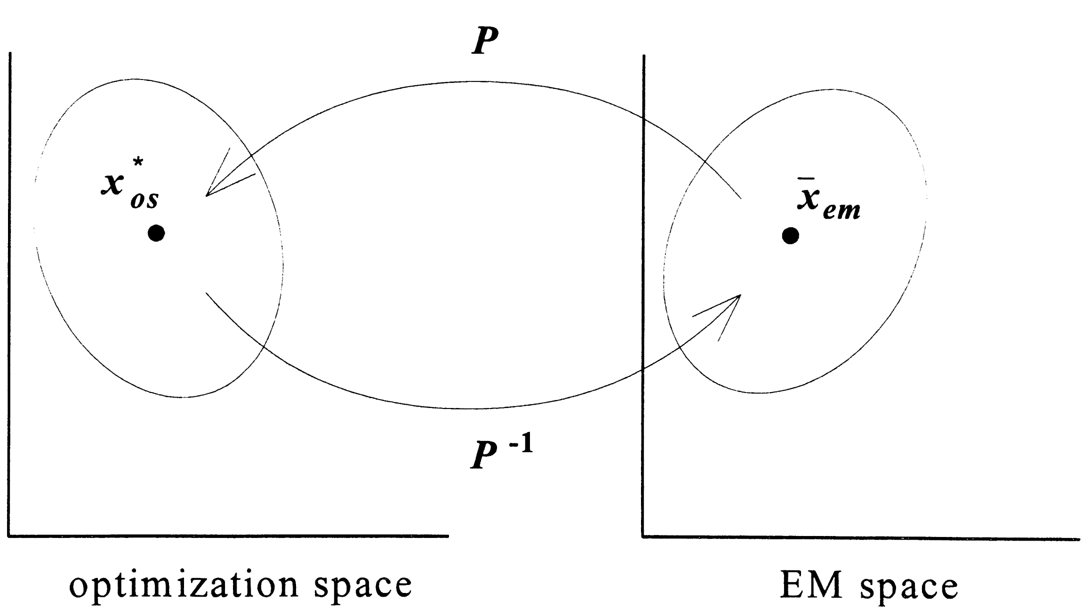
$$\| \boldsymbol{R}_{os}(\boldsymbol{P}(\boldsymbol{x}_{em})) - \boldsymbol{R}_{em}(\boldsymbol{x}_{em}) \| \leq \varepsilon$$

where $\boldsymbol{R}_{os}$ and $\boldsymbol{R}_{em}$ are the circuit responses simulated by the OS and EM simulators, respectively

starting from the optimal design $\boldsymbol{x}^*_{os}$ (in $\boldsymbol{X}_{os}$) we use SM to find the mapped solution in $\boldsymbol{X}_{em}$ as

$$\bar{\boldsymbol{x}}_{em} = \boldsymbol{P}^{-1}(\boldsymbol{x}^*_{os})$$

assuming that $\boldsymbol{P}$ is invertible



Aggressive Space Mapping
(*Bandler et al., 1995*)

new algorithm aggressively exploits *every* EM simulation

avoids upfront EM analyses at many base points

applies the classical Broyden update to the mapping

quasi-Newton iteration

$$\boldsymbol{x}_{em}^{(i+1)} = \boldsymbol{x}_{em}^{(i)} - \boldsymbol{B}^{(i)^{-1}} \left(\boldsymbol{P}^{(i)} (\boldsymbol{x}_{em}^{(i)}) - \boldsymbol{x}_{os}^{*} \right)$$

Broyden update:

$$\boldsymbol{B}^{(i+1)} = \boldsymbol{B}^{(i)} + \frac{\left(\boldsymbol{P}^{(i+1)} (\boldsymbol{x}_{em}^{(i+1)}) - \boldsymbol{x}_{os}^{*}\right) \boldsymbol{h}^{(i)^T}}{\boldsymbol{h}^{(i)^T} \boldsymbol{h}^{(i)}}$$

where

$$\boldsymbol{h}^{(i)} = \boldsymbol{x}_{em}^{(i+1)} - \boldsymbol{x}_{em}^{(i)}$$

Space Mapping Optimization

to avoid direct optimization of computationally intensive models

the multi-simulator approach is particularly relevant and suitable for Space Mapping

automatic alignment of two distinct models of different accuracy and computational efficiency

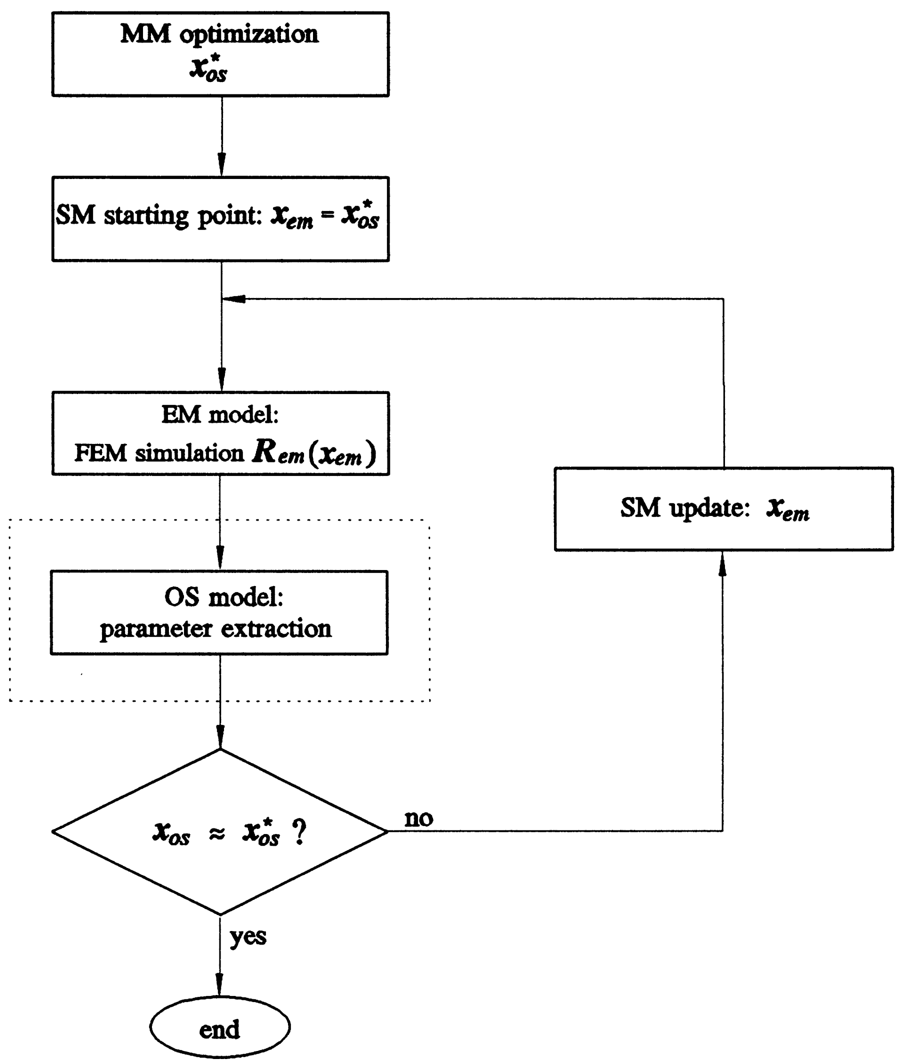
such models would normally be facilitated by two disjoint simulators

two different EM simulators are used here

> EM space or "fine" model - 3D FEM-based field simulator Maxwell Eminence (*Ansoft Corporation*)
>
> optimization space (OS) or "coarse" model - the RWGMM library of waveguide mode-matching (MM) models connected by network theory (*Fritz Arndt*)

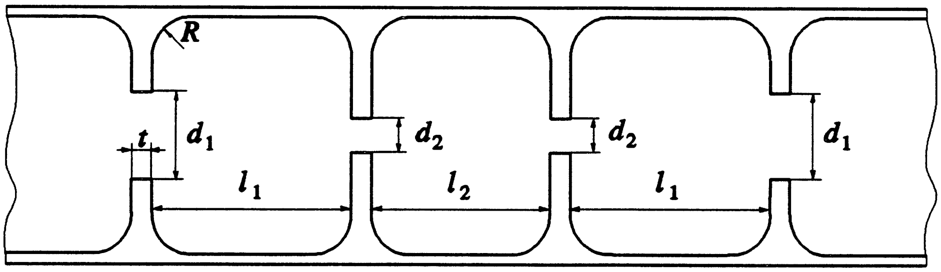
Space Mapping Using MM/Network Theory and FEM
(Bandler et al., 1997)

flow diagram of Space Mapping concurrently exploiting the hybrid MM/network theory and FEM simulation techniques



two-level Datapipe architecture

Optimization of an H-Plane Resonator Filter



the waveguide cross-section: 15.8×7.9 mm

iris and corner radius: $t = 0.4$ mm, $R = 1$ mm

design variables

d_1, d_2, l_1 and l_2

design specifications

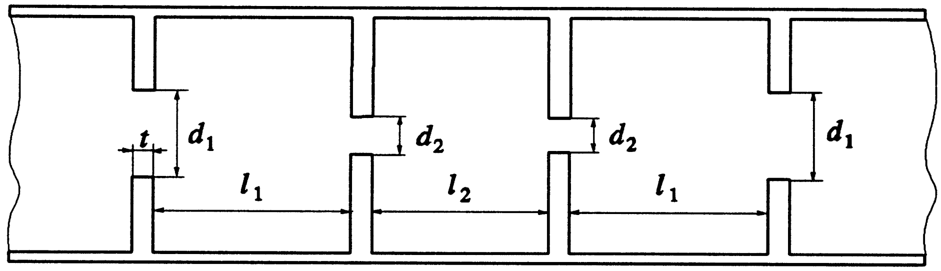
$|S_{21}| < -35$ dB for $13.5 \leq f \leq 13.6$ GHz
$|S_{11}| < -20$ dB for $14.0 \leq f \leq 14.2$ GHz
$|S_{21}| < -35$ dB for $14.6 \leq f \leq 14.8$ GHz

FEM analysis - fine (or EM) model for Space Mapping

capable of analyzing arbitrary shapes

computationally very intensive

Coarse Model for Space Mapping Optimization



OS model (coarse model) for Space Mapping

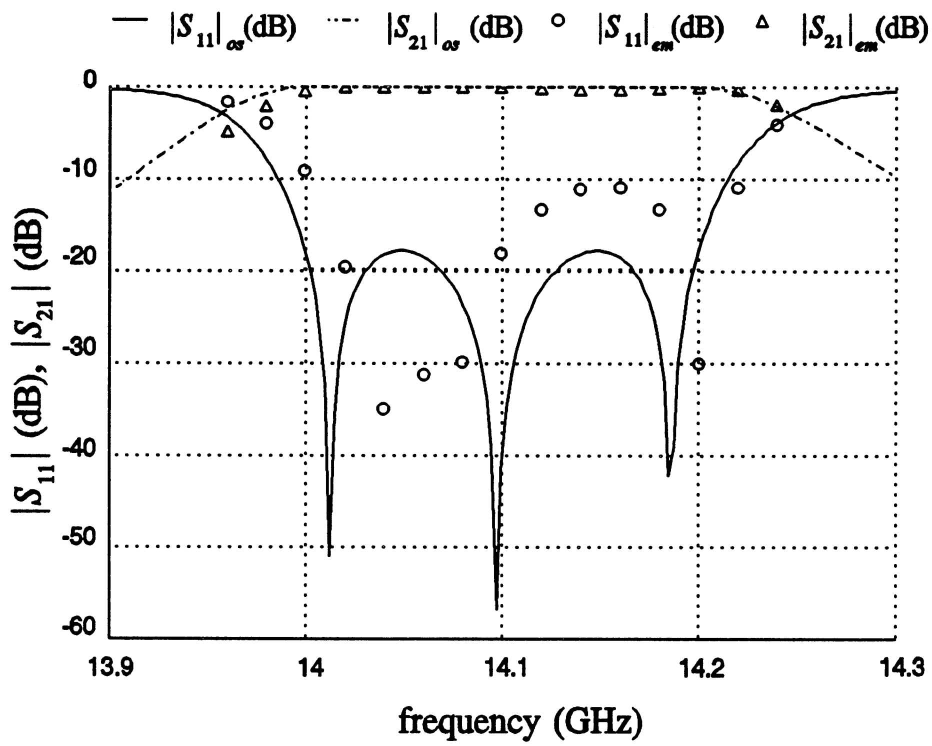
sharp corners

hybrid MM/network theory simulation

- computationally efficient
- accurately treats a variety of predefined geometries
- ideally suited for modeling complex waveguide structures decomposable into available library building blocks

minimax optimization of the OS model gives the starting point for Space Mapping

Responses at the Starting Point



focus on the passband: 13.96 to 14.24 GHz

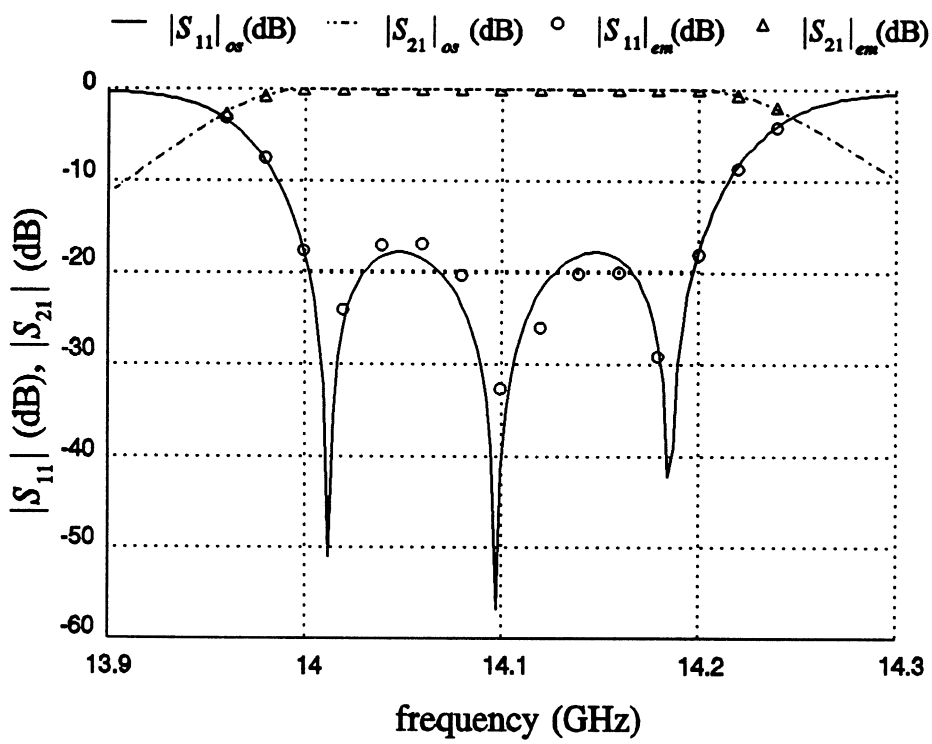
RWGMM (curves) and Maxwell Eminence (points)

discrepancy is evident

$d_1 = 6.04541, d_2 = 3.21811, l_1 = 13.0688$ and $l_2 = 13.8841$

the minimax solution in the OS space, x^*_{os}, yields the target response for Space Mapping

SM Optimized FEM Responses



only 4 Maxwell Eminence simulations

RWGMM (curves) and Maxwell Eminence (points)

very good match

$d_1 = 6.17557$, $d_2 = 3.29058$, $l_1 = 13.0282$ and $l_2 = 13.8841$

direct optimization using Empipe3D confirms that the Space Mapping solution is indeed optimal

Tolerance Simulation Using SM

first, the mapping is established during nominal SM optimization

statistical outcomes in the EM space are mapped to the corresponding points in the OS space

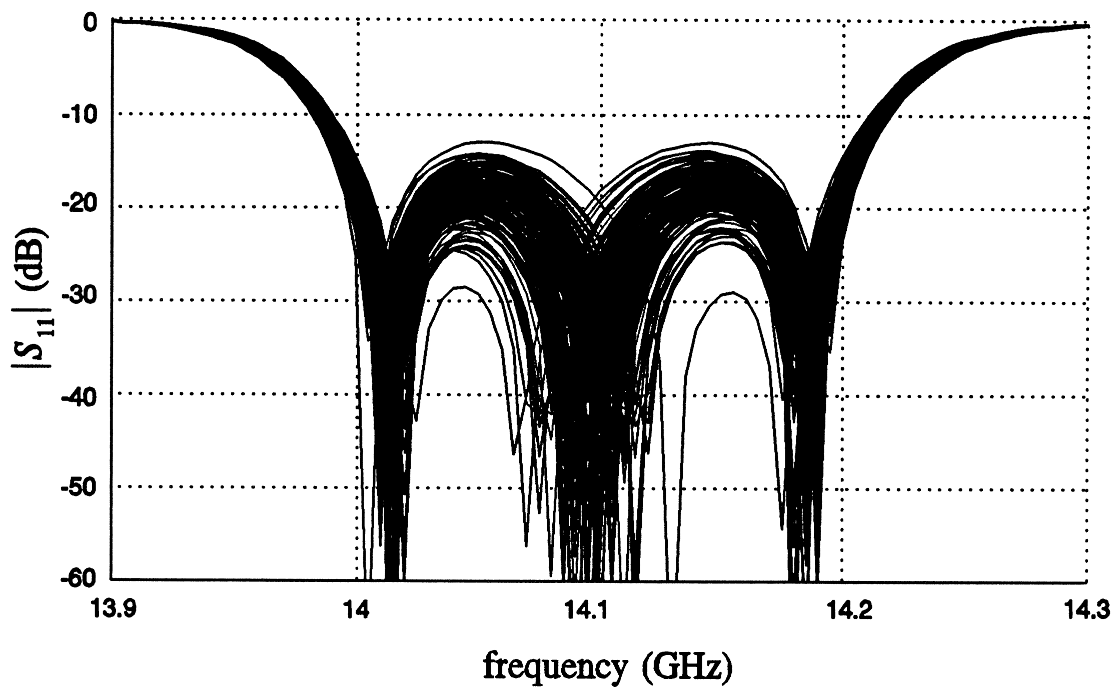
we are able to rapidly estimate the effects of manufacturing tolerances, benefitting from

- the accuracy of the FEM model

- the speed of the hybrid MM/network theory simulations

the CPU time required for the Monte Carlo analysis is comparable to just a single full FEM simulation

Monte Carlo Analysis of the H-Plane Filter



the statistical outcomes were randomly generated from normal distribution with a standard deviation of 0.0333%

the yield estimated from 200 outcomes is 88.5% w.r.t. the specification of $|S_{11}|$ < -15 dB in the passband

increasing the standard deviation to 0.1% results in yield dropping to 19% for 200 outcomes

Trust Region Aggressive Space Mapping Algorithm

(*Bakr et al., 1998*)

using $\boldsymbol{f}^{(i)} = \boldsymbol{P}(\boldsymbol{x}_{em}^{(i)}) - \boldsymbol{x}_{os}^{*}$

solve $(\boldsymbol{B}^{(i)T}\boldsymbol{B}^{(i)} + \lambda \boldsymbol{I})\,\boldsymbol{h}^{(i)} = -\boldsymbol{B}^{(i)T}\boldsymbol{f}^{(i)}$ for $\boldsymbol{h}^{(i)}$

this corresponds to minimizing $\left\|\boldsymbol{f}^{(i)} + \boldsymbol{B}^{(i)}\boldsymbol{h}^{(i)}\right\|_2^2$ subject to $\left\|\boldsymbol{h}^{(i)}\right\|_2 \le \delta$ where δ is the size of the trust region

λ, which correlates to δ, can be determined (*Moré et al., 1983)*

single point parameter extraction is performed at the new point $\boldsymbol{x}_{em}^{(i+1)} = \boldsymbol{x}_{em}^{(i)} + \boldsymbol{h}^{(i)}$ to get $\boldsymbol{f}^{(i+1)}$

if $\boldsymbol{f}^{(i+1)}$ satisfies a certain success criterion for the reduction in the l_2 norm of the vector $\boldsymbol{f}$, the point $\boldsymbol{x}_{em}^{(i+1)}$ is accepted and the matrix $\boldsymbol{B}^{(i)}$ is updated using Broyden's update

otherwise a temporary point is generated using $\boldsymbol{x}_{em}^{(i+1)}$ and $\boldsymbol{f}^{(i+1)}$ and is added to the set of points to be used for multi-point parameter extraction

a new $\boldsymbol{f}^{(i+1)}$ is obtained through multi-point parameter extraction

Trust Region Aggressive Space Mapping Algorithm

(*Bakr et al., 1998*)

the last three steps are repeated until a success criterion is satisfied or the step is declared a failure

step failure has two forms

(1) f may approach a limiting value without satisfying the success criterion or
(2) the number of fine model points simulated since the last successful step reaches n+1

Case (1): the parameter extraction is trusted but the linearization used is suspect; the size of the trust region is decreased and a new point $\boldsymbol{x}_{em}^{(i+1)}$ is obtained

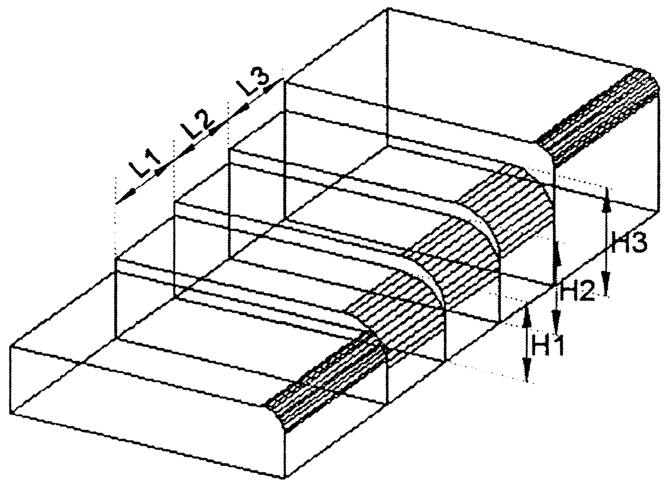
Case (2): sufficient information is available for an approximation to the Jacobian of the fine model responses w.r.t. the fine model parameters used to predict the new point $\boldsymbol{x}_{em}^{(i+1)}$

the mapping between the two spaces is exploited in the parameter extraction step by solving

$$\underset{\boldsymbol{x}_{os}}{minimize} \left\| \boldsymbol{R}_{os}(\boldsymbol{x}_{os} + \boldsymbol{B}^{(i)}(\boldsymbol{x} - \boldsymbol{x}_{em}^{(i+1)})) - \boldsymbol{R}_{em}(\boldsymbol{x}) \right\|$$

simultaneously for a set of points $\boldsymbol{x}$

Three-Section Waveguide Transformer, Rounded Corners
(*Empipe3D manual, 1997*)



impedance matching between WR-75 half height and WR-75 full height waveguides

designable variables: the height and length of each section

fine (EM) model: HP HFSS

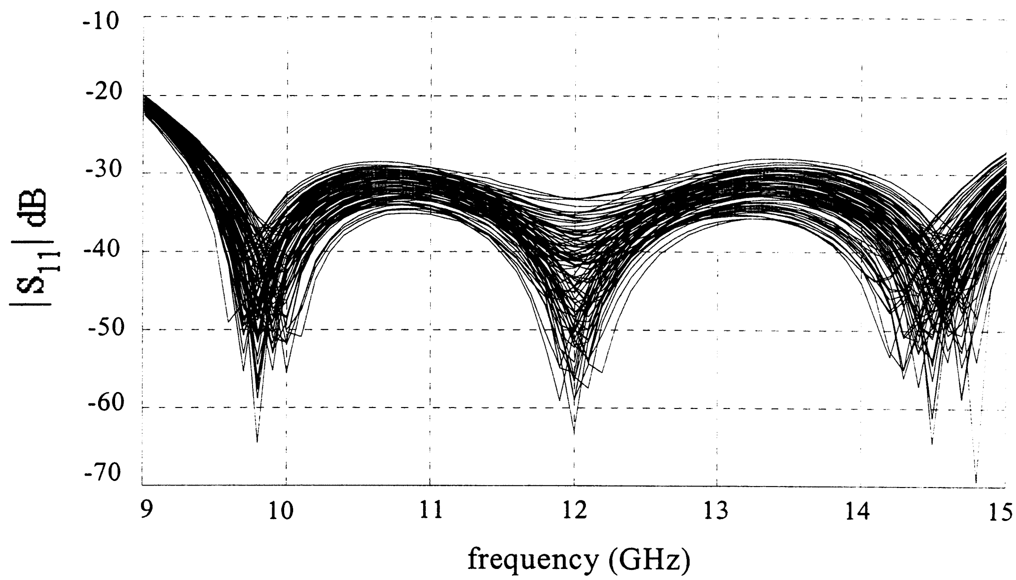
coarse model: ideal analytical model (*Bandler, 1969*)

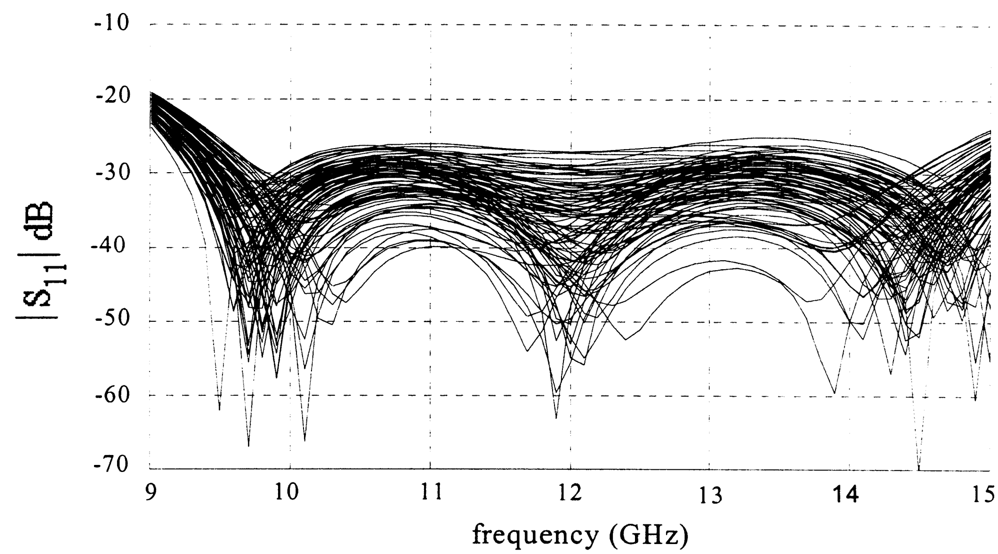
the optimal design was obtained in 3 iterations, requiring 7 fine model simulations by HP HFSS

design specifications

$$|S_{11}| \leq -30\,\text{dB} \text{ for } 9.5 \text{ GHz} \leq f \leq 15 \text{ GHz}$$

Three-Section Waveguide Transformer, Rounded Corners



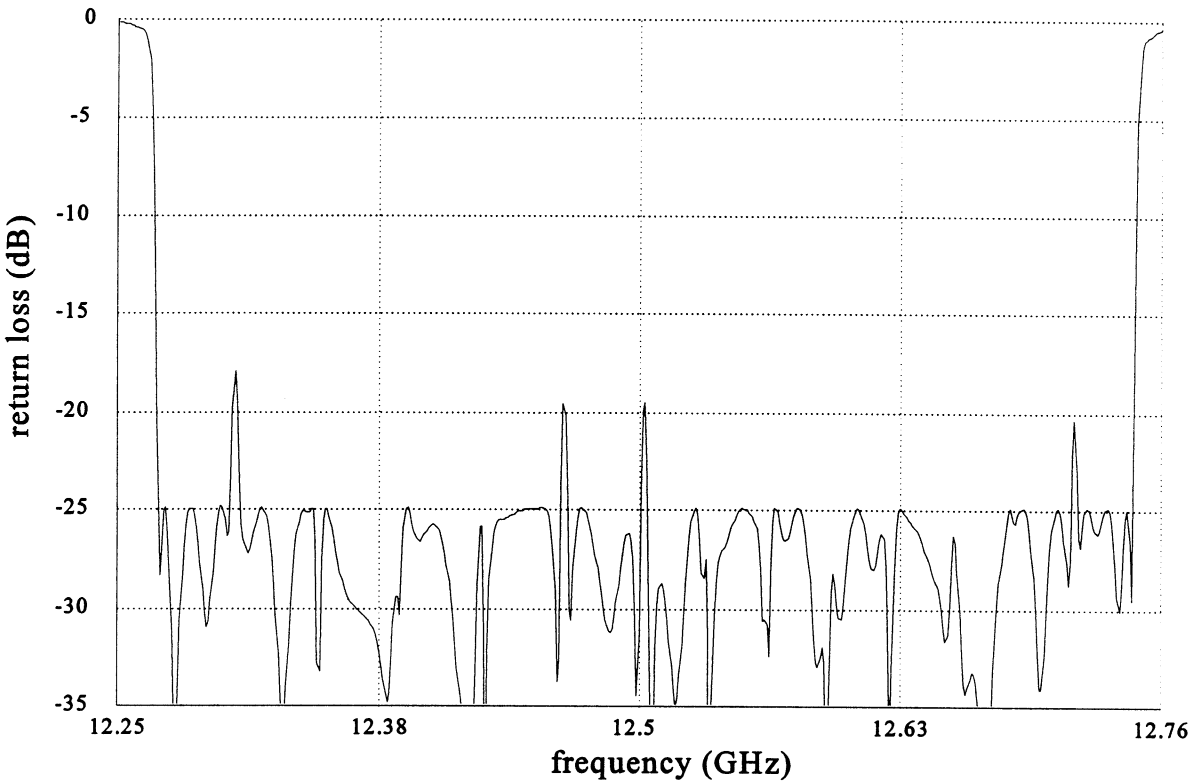


parameters uniformly distributed with tolerances of 1% and 2%

Monte Carlo analysis uses 100 coarse model simulations only

yield is 39% and 4%, respectively

14 Channel Multiplexer Tolerance Optimization



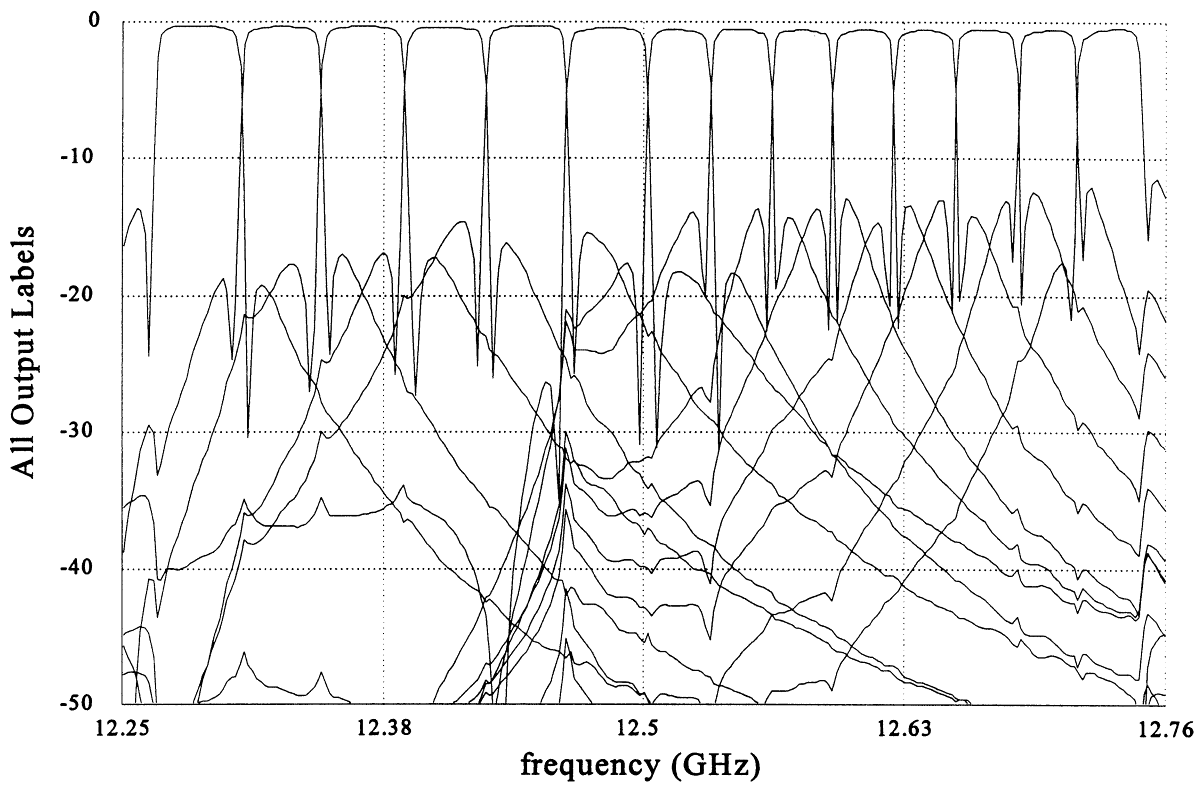
Common port return loss after nominal optimization

14 channel multiplexer

112 variable optimized

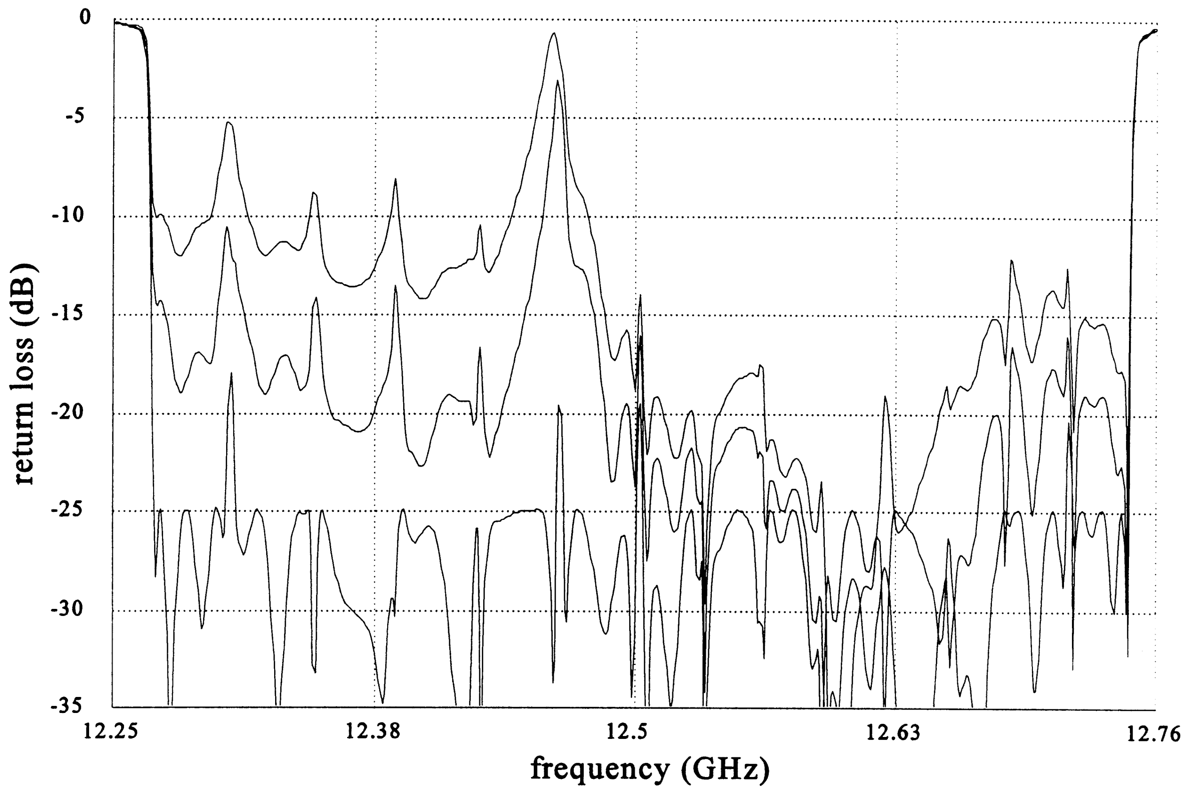
511 frequency points

14 Channel Multiplexer Tolerance Optimization



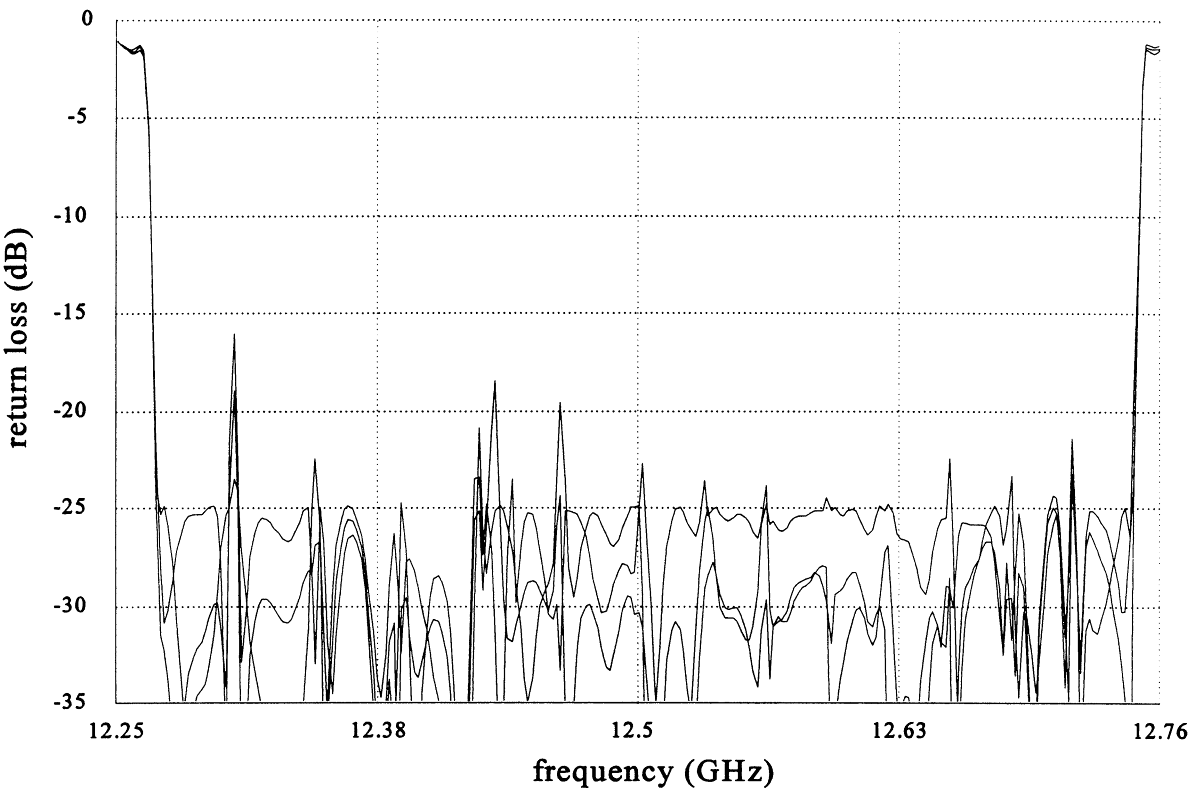
Channel insertion loss after nominal optimization

14 Channel Multiplexer Tolerance Optimization



Common port return loss with tolerances

14 Channel Multiplexer Tolerance Optimization



Common port return loss after optimization with tolerances

a total of 280 CPU hours on a SPARCstation 10

Conclusions

possibilities in microwave CAD with tolerances are presented

active and passive, linear and nonlinear, lumped and distributed, circuit-oriented and EM-oriented designs are considered

brief historical perspective of DCTT is provided

intelligent computational interfaces combine and enhance the features of otherwise disjoint simulators based on OSA's Datapipe open architecture

the role of distributed or parallel computing is exemplified

mixed time-domain, frequency-domain and EM simulations are integrated for efficient statistical design

optimization using OSA90/hope of a broadband amplifier with microstrip components: the MESFET is simulated by SPICE and the microstrip components are analyzed by ***em***

tolerance design of a 14 channel waveguide multiplexer is presented

Space Mapping and its advantages in design with tolerances is reviewed

further advantages of the multi-simulator approach are exemplified by Space Mapping optimization with two different EM simulators: mode-matching and finite element

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