OPTIMIZATION OF A CLASS B FREQUENCY DOUBLER ENHANCED BY ELECTROMAGNETIC SIMULATION

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ABSTRACT

A class B frequency doubler is optimized, Circuit simulation is enhanced by the electromagnetic simulation of critical components. The FET in the circuit is modeled by the Curtice and Ettenberg model. The couplings between the third harmonic stubs situated at the gate and drain ports of the FET and between the bias pads and the radial stubs are simulated by an electromagnetic simulator. The results are imported into OSA90/hope for circuit-level simulation. Minimax optimization is performed for the complete circuit with large-signal harmonic balance simulation. The circuit performance is significantly improved after optimization.

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SUMMARY

Introduction

Large-signal circuit optimization with the harmonic balance (HB) technique has been significantly advanced during the last decade (e.g., [1-4]). The computational time is greatly reduced due to the efficiency of the HB simulation and the elegant sensitivity calculation [2,3]. Optimization using the FAST sensitivity technique has been applied in the performance-driven design of a frequency doubler with a physics-based model [5] and yield-driven design of a frequency doubler with an equivalent circuit model [6].

In this paper we present performance-driven design of a class B frequency doubler [7] augmented by the electromagnetic simulation. The single FET chip (NE71000) used in the circuit is modeled by the Curtice and Ettenberg model [8] extracted from the typical DC and S parameters [9] using HarPE [10]. The third harmonic stubs situated at the gate and drain ports of the FET and the bias pads together with the radial stubs are simulated by ***em*** [11]. The ***em*** results of these three subcircuits are then imported into OSA90/hope [12] for the overall circuit-level simulation. This reflects the couplings within these three subcircuits (the third harmonic stubs, the gate biasing circuit, and the drain biasing circuit).

The minimax optimizer of OSA90/hope is used to carry out the performance-driven design of this frequency doubler. Significant improvement of the circuit performance is obtained after optimization.

FET Parameter Extraction

The class B frequency doubler [7] consists of a single FET chip (NE71000) and a number of microstrip components, including two third harmonic stubs situated at the gate and drain ports of the FET, two bias pads and two radial stubs as shown in Fig. 1. It is designed for applications at 7 GHz.

Since no large-signal model of the FET was available from the manufacturer, we used

HarPE to perform parameter extraction to create the large-signal FET model. The data that we utilized for parameter extraction contains typical DC characteristics and typical S parameters from 2 GHz to 26 GHz with 1 GHz step at two bias [9]. The built-in Curtice and Ettenberg model together with the "Extrinsic4" linear subcircuit is chosen to model the FET. The parameter extraction is performed by fitting simultaneously the DC curves at 12 points, and the S parameters at the two bias points and 25 frequencies. Very good DC match and reasonable S-parameter match are obtained.

Electromagnetic Simulation

Due to the geometrical structure of the circuit there are couplings between the microstrip elements, in particular between the third harmonic stubs situated at the gate and drain ports of the FET and between the bias pads and radial stubs. The effects of these couplings may significantly affect the circuit performance. Therefore, it is very important to include these couplings in circuit simulation.

In order to consider these couplings we use an electromagnetic simulator. The two third harmonic stubs situated at the gate and drain ports of the FET are considered as one four-port element. Each bias pad together with the adjacent radial stub is regarded as one two-port element. These three subcircuits are simulated by ***em*** [11] individually. The ***em*** results are then imported to OSA90/hope for circuit-level simulation. This reflects the couplings within these three subcircuits.

Harmonic Balance Simulation and Optimization

HB simulation and optimization are carried out by OSA90/hope augmented by the ***em*** simulation results for the three aforementioned subcircuits. The conversion gain is calculated by

conversion gain = output power at the second harmonic / available input power.

The spectral purity is computed by

$$\text{spectral purity} = P_2 / (P_1 + P_3 + P_4)$$

where P_i is the output power at the *i*th harmonic.

The specifications for optimization are

$$\text{conversion gain} > 3 \text{ dB}$$
$$\text{spectral purity} > 20 \text{ dB}$$

at 7 GHz and 9 dBm input power.

The frequency doubler design is carried out by minimax optimization with a total of 15 variables as indicated in Fig. 1. The parameter values given in [7] are chosen as the starting point for optimization. All specifications are satisfied after optimization. The values of the variables before and after optimization are listed in Table I. From Table I we can see that the most influencing variables are ML1, ML3 and ML12.

The output power versus input power at 7 GHz before and after optimization are shown in Figs. 2 and 3, respectively. The conversion gain and spectral purity versus input power at 7 GHz before and after optimization are shown in Figs. 4 and 5, respectively. The 3D view of conversion gain versus frequency and input power before and after optimization are given in Figs. 6 and 7, respectively. The source and output voltage waveforms at 7 GHz and 9 dBm input power before and after optimization are plotted in Fig. 8. We can see that significant improvement of the circuit performance is achieved after optimization.

Conclusions

We have presented optimization of a class B frequency doubler enhanced by ***em*** simulations to consider the couplings between the circuit components. Our optimization significantly improves the circuit performance.

References

[1] J.W. Bandler, Q.J. Zhang, S. Ye and S.H. Chen, "Efficient large-signal FET parameter extraction using harmonics," *IEEE Trans. Microwave Theory Tech.*, vol. 37, 1989, pp. 2099-2108.

[2] J.W. Bandler, Q.J. Zhang and R.M. Biernacki, "A unified theory for frequency domain simulation and sensitivity analysis of linear and nonlinear circuits," *IEEE Trans. Microwave Theory Tech.*, vol. 36, 1988, pp. 1661-1669.

[3] J.W. Bandler, Q.J. Zhang and R.M. Biernacki, "Practical, high-speed gradient computation for harmonic balance simulators," *IEEE Int. Microwave Symp. Dig.* (Long Beach, CA), 1989, pp. 363-366.

[4] J.W. Bandler, R.M. Biernacki, S.H. Chen, J. Song, S. Ye and Q.J. Zhang, "Analytically unified DC/small-signal/large-signal circuit design," *IEEE Trans. Microwave Theory Tech.*, vol. 39, 1991, pp. 1076-1082.

[5] Q. Cai, "Physics-based microwave device modeling and circuit optimization," *Ph.D. Thesis*, Department of Electrical and Computer Engineering, McMaster University, Hamilton, Ontario, Canada.

[6] J.W. Bandler, Q.J. Zhang, J. Song and R.M. Biernacki, "FAST gradient based yield optimization of nonlinear circuits", *IEEE Trans. Microwave Theory Tech.*, vol. 38, 1990, pp. 1701-1710.

[7] P. Jackson, Ed., *Microwave Engineering Europe*, Morgan-Grampian (Technical Press) Ltd., 30 Calderwood Street, London SE18 6QH, U.K., private communication, March 1, 1994.

[8] W.R. Curtice and M. Ettenberg, "A nonlinear GaAs FET model for use in the design of output circuits for power amplifiers," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-33, 1985, pp. 1383-1394.

[9] "RF and Microwave Semiconductors," *NEC Data Book*, California Eastern Laboratories, 1994.

[10] *HarPE*™, Optimization Systems Associates Inc., P.O. Box 8083, Dundas, Ontario, Canada L9H 5E7, 1993.

[11] *Em* Version 2.4, Sonnet Software, Inc., Suite 203, 135 Old Cove Road, Liverpool, NY 13090-3774, 1993.

[12] *OSA90/hope*™, Optimization Systems Associates Inc., P.O. Box 8083, Dundas, Ontario, Canada L9H 5E7, 1993.

TABLE I
VARIABLE VALUES BEFORE AND AFTER OPTIMIZATION

Variable	Before Optimization	After Optimization
ML1	2.0	1.691
ML2	1.0	0.901
ML3	7.95	6.792
ML4	1.55	1.759
ML5	5.75	5.182
ML6	2.11 + 0.38	1.601 + 0.38
ML7	2.5	2.842
ML8	3.99	3.903
ML9	3.87	3.698
ML10	1	0.994
ML11	20	17.35
ML12	3.395	4.500
ML13	7.68	7.510
ML14	7.85	7.903
ML15	3.82	3.804

All dimensions are in mm.

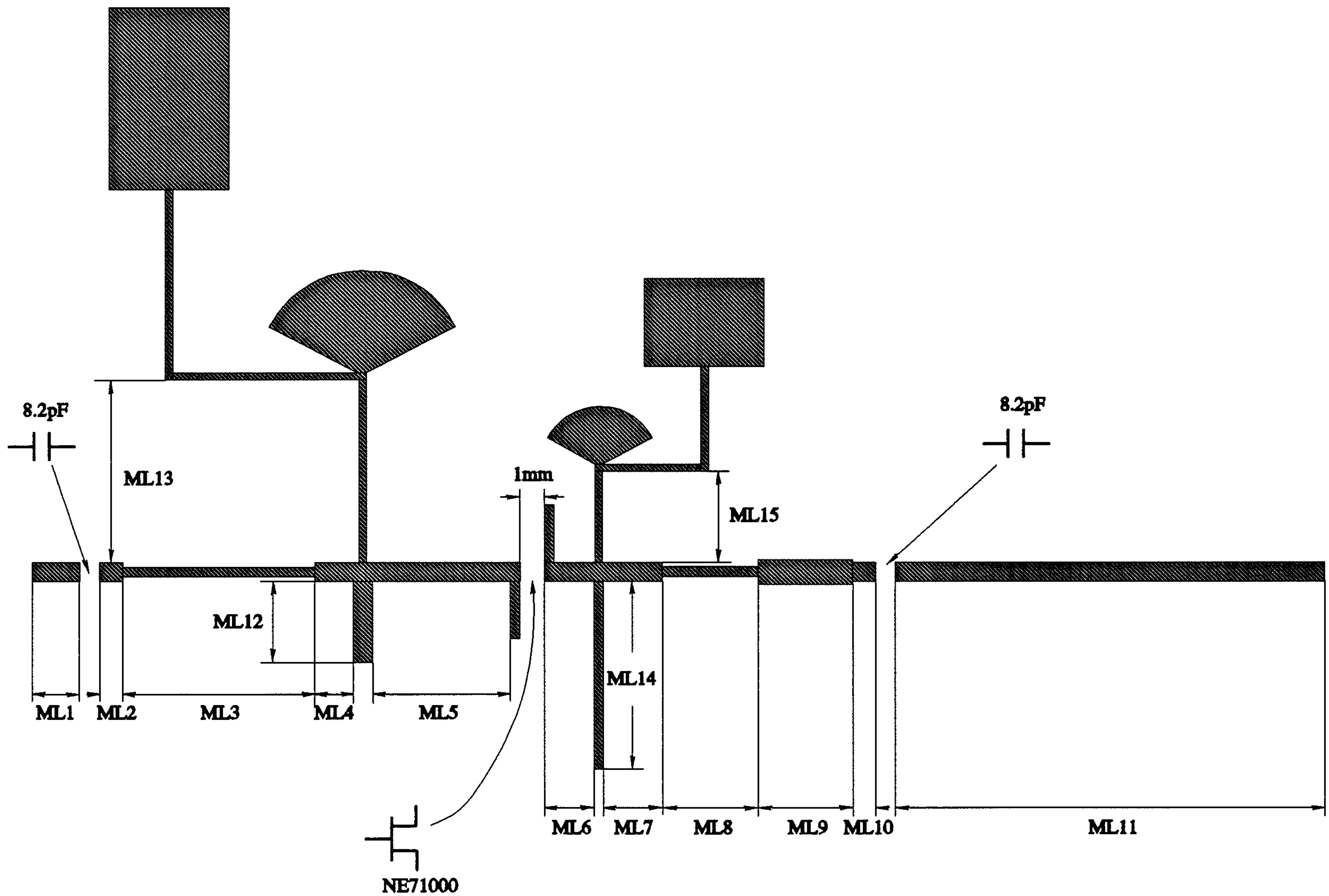

Fig. 1 The class B frequency doubler circuit.

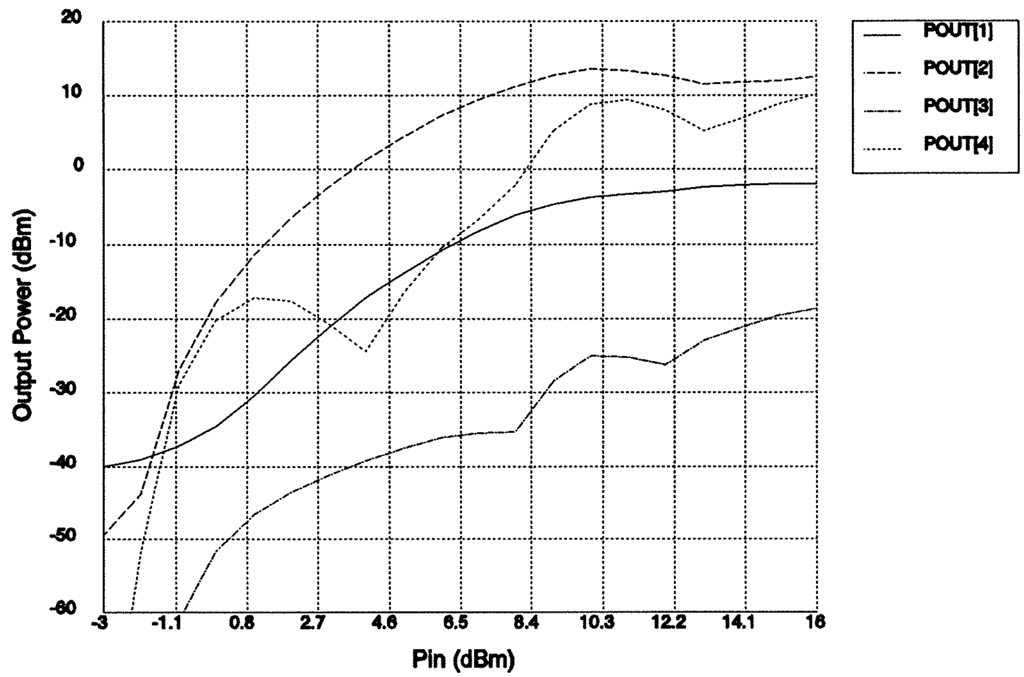

Fig. 2 Output power versus input power at 7 GHz before optimization.

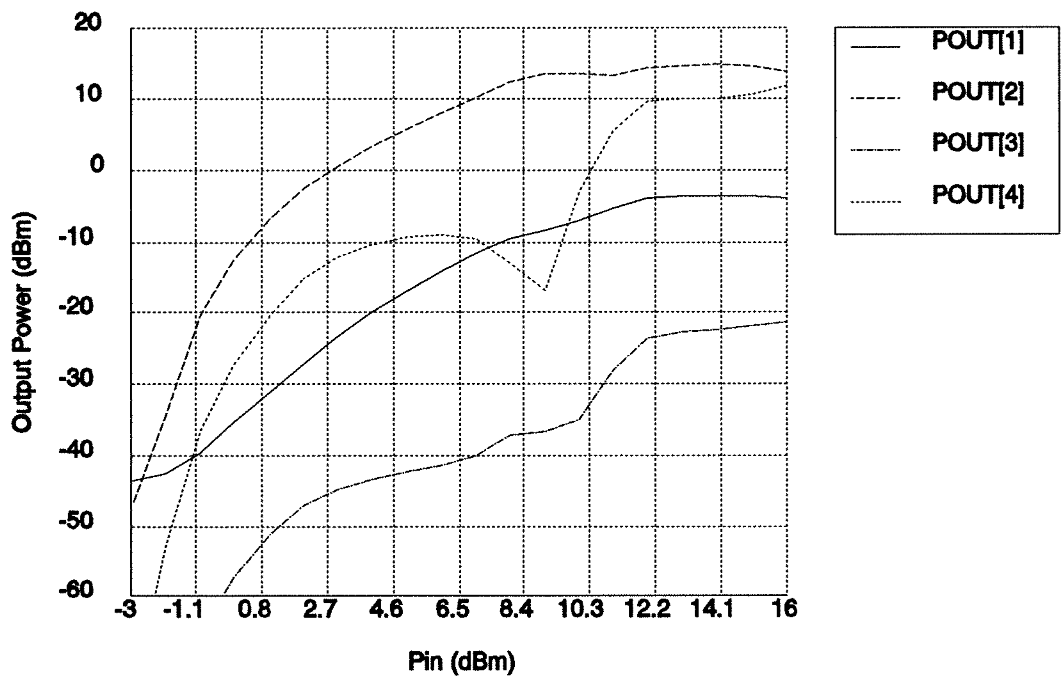

Fig. 3 Output power versus input power at 7 GHz after optimization.

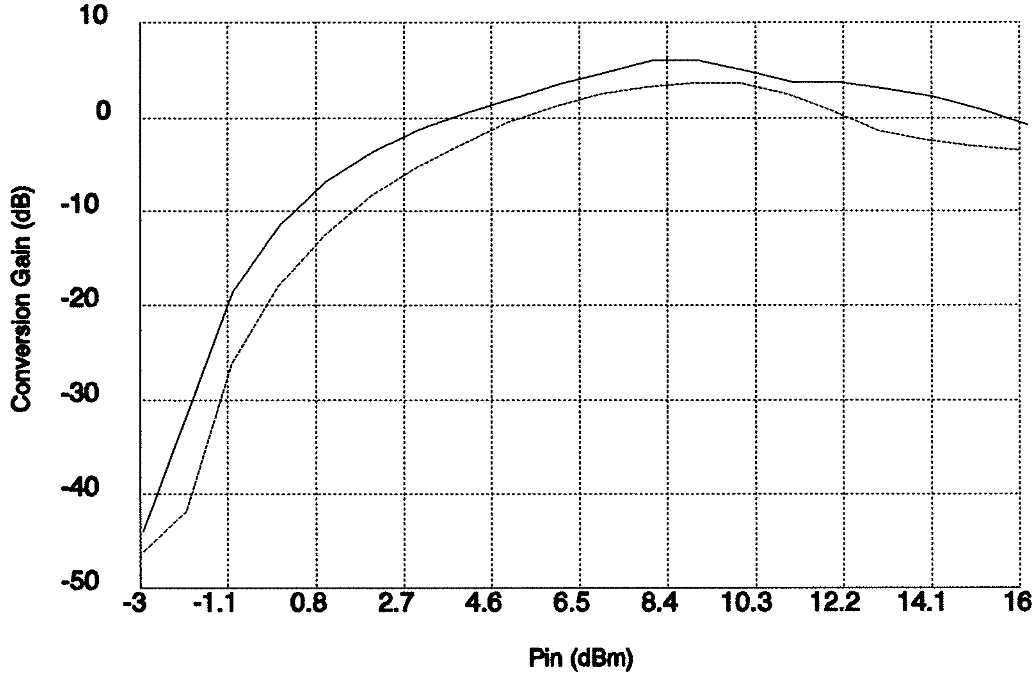

Fig. 4 Conversion gain versus input power at 7 GHz before (---) and after (—) optimization.

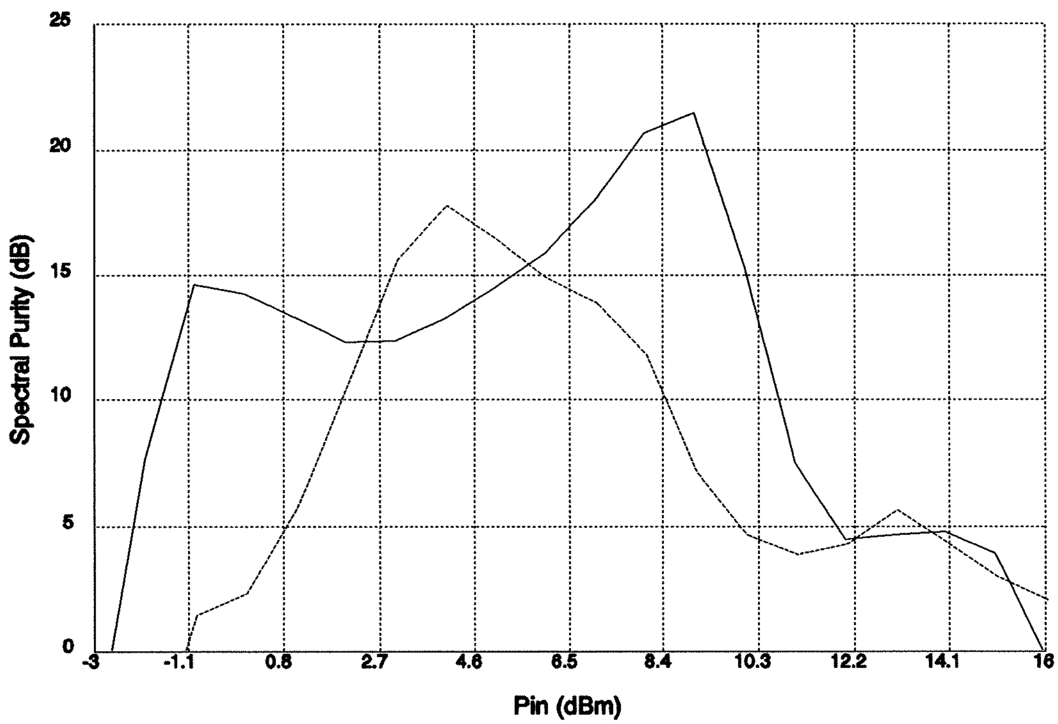

Fig. 5 Spectral purity versus input power at 7 GHz before (---) and after (—) optimization.

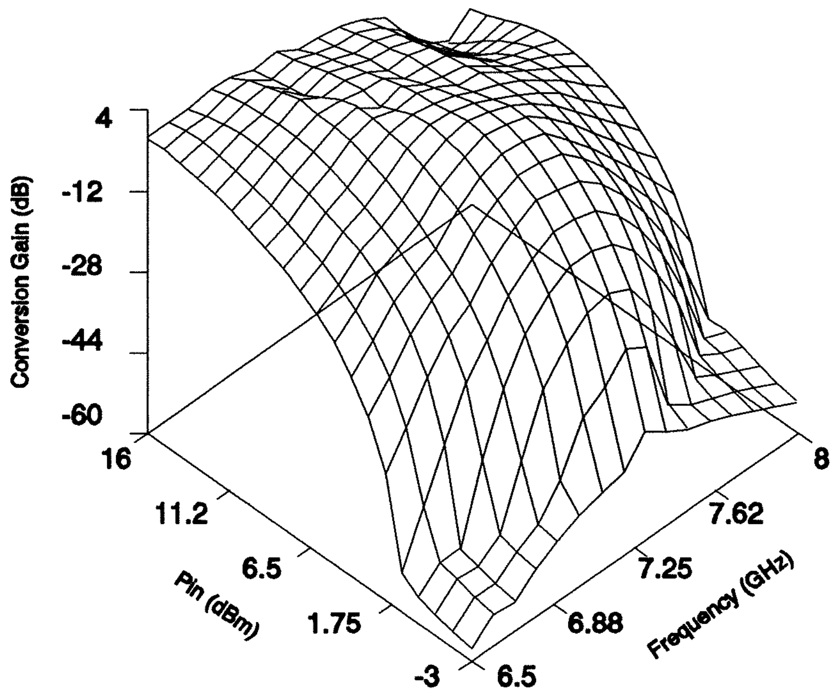

Fig. 6 3D view of conversion gain versus input power and frequency before optimization.

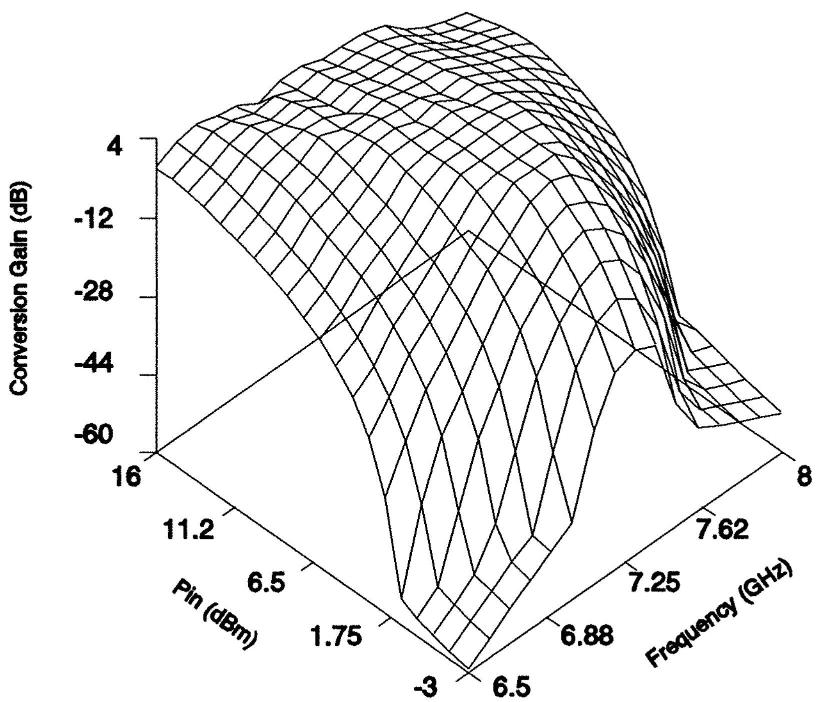

Fig. 7 3D view of conversion gain versus input power and frequency after optimization.

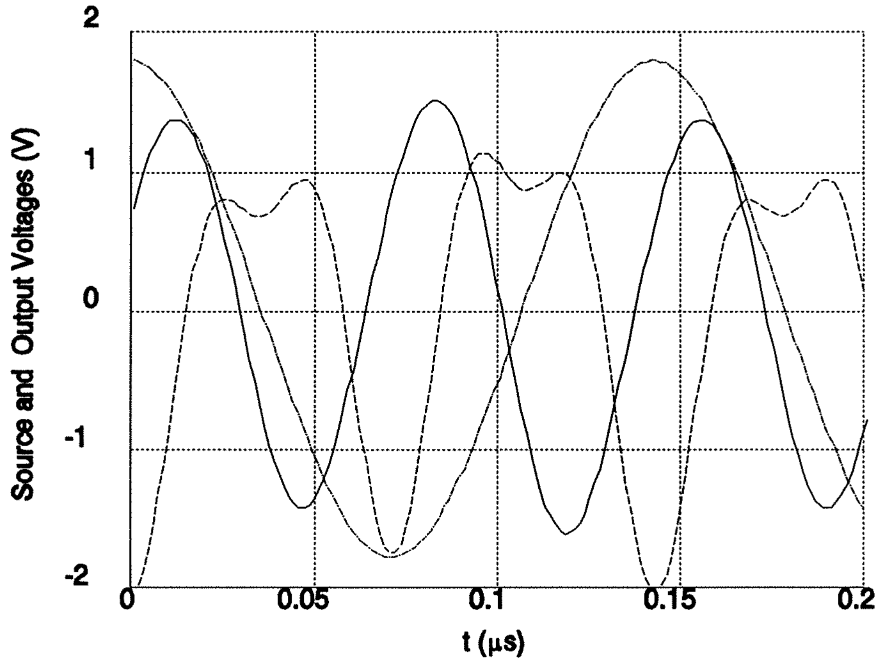

Fig. 8 Source (-·-) and output voltage waveforms at 7 GHz and 9 dBm input power before (---) and after (——) optimization.