COMPUTER ENGINEERING 4KC3: SIMULATION AND OPTIMIZATION

LABORATORY MANUAL

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INTRODUCTION

This set of laboratory experiments was developed during the Fall semester of the 1992/93 academic year for the senior level computer engineering course 4KC3 "Simulation and Optimization" offered by the Department of Electrical and Computer Engineering, McMaster University. It is an elective course for which the prerequisite is to complete the third year course on numerical techniques: 3KB3 "Computational Methods II".

For the first time the undergraduate students could gain hands-on experience with practical implementation of advanced concepts of computer-aided circuit design. Some of the techniques covered in the laboratory were hot research topics just a few years ago. It was made possible by the availability of OSA90/hope™ [1] - a state-of-the-art software system from Optimization Systems Associates Inc., in particular due to its user friendliness. Without extensive and very tedious programming the students could generate results directly related circuit design while, invisibly, employing some of the most advanced numerical techniques. This helped them to concentrate on concepts rather than on implementation.

The students had already been exposed to OSA90/hope when it was experimentally adopted for the laboratory associated with 3KB3 during the second semester of the 1991/92 academic year. That laboratory, however, covered only the basic concepts of simulation and optimization of linear passive circuits. In contrast, this set of experiments was devised to cover nonlinear and active circuits, the subjects not only more difficult, but obviously of much higher practical importance. The scope of engineering problems has also been widened to include device modeling and statistical design.

The purpose of the first experiment was to introduce some newly developed features of OSA90/hope such as X-Windows environment, HPGL plotter file generation, Graphical Views and Control Block. The main body of the laboratory consisted of four experiment: "Nonlinear Memoryless Circuits: DC and Time-Domain Simulation", "Performance-Driven Design of Nonlinear Circuits", "Device Modeling from Experimental Data" and "Statistical Design Centering". Particularly, the last two experiments allowed the students to perform tasks too complex to be included in undergraduate level material so far.

There were 20 students in the class and their reaction to this new lab was overwhelmingly positive. Some of their opinions included statements such as: "A very useful course with good applications towards research and thesis", "... 'high-end' technical labs", "... labs are very well written and clear and fun", the latter most likely reflecting the ease with which the students could carry out the experiments.

COMPUTER ENGINEERING 4KC3:
SIMULATION AND OPTIMIZATION

Introduction to OSA90/hope™ Version 2.0

Lab #1

Objectives

This introductory lab is intended to refresh your familiarity with OSA90/hope™ and to bring to your attention several new features available in Version 2.0. It is also intended to resolve any organizational problems.

Software

OSA90/hope™ on Sun SPARCstations (JHE 215, Monday, Sept. 21, 1992, 2:30 - 4:00 pm.)

Procedure

Getting Started

(1) Log into one of the 16 SPARCstations. Your initial password is "monday". Do not select SunView, but select X11 after login. Change your password using the command "passwd".

(2) Create symbolic link to OSA90/hope™ by executing the command

"ln -s /home/engine/ee761/osa90"

Subsequently, you will be able to invoke OSA90/hope™ by simply typing "osa90" without the full path.

(3) Copy OSA90/hope™ Demo Examples 1 and 9 files to your directory using the commands

"cp /home/engine/ee761/demo01.ckt ex1.ckt"
"cp /home/engine/ee761/demo09_o.ckt ex9.ckt"
"cp /home/engine/ee761/lcfilter ./"

Basic Experiments with X-Windows

X options are available by pressing mouse buttons outside the windows. Keep holding the button down and move mouse to select one of the options. To execute the selected option move pointer to the window to which the option is to be applied. The centre mouse button is for "drag".

(1) Open two or three concurrent windows. Move and resize a selected window.

(2) Execute two different commands such as "more ex9.ckt" and "vi ex1.ckt" simultaneously from within two different windows. (To leave vi type ":q" or ":q!".)

(3) Close the windows opened in Step 1.

Start OSA90/hope™

(1) Invoke OSA90/hope™ by entering "osa90" at the system prompt "%".

(2) Press **<ENTER>**, select the file "ex9.ckt" and press **<ENTER>** again. You are now in the OSA90/hope's editor.

In OSA90/hope the left-hand mouse button is used for "select" or "yes" and the right-hand mouse button is for "escape" or "no".

Use On-line Manual

(1) Invoke the on-line User's Manual from the editor pull-down menu. View the description of: Control Block in Chapter 3 (Input File); matrices, Tables 4.3 and 4.4 in Chapter 4 (Expressions); HPGL files in Chapter 9 (Simulation); and Graphical Views, Chapter 10.

(2) Mark Section 9.15 in Chapter 9 (Simulation) on Graphics Hardcopy and save it in the file "hpgl.man".

Control Block

(1) Remove all units (NH, NF and GHZ) from the current file (ex9.ckt).

(2) Exit the editor (parse the input file), simulate the circuit (display option), and invoke View 2 from XSWEEP display option. Note the frequency scale.

(3) Add "Non_Microwave_Units;" flag to the Control block and repeat Step 2.

(4) Without saving the modified file read in the file "ex9.ckt" again. This time remove "GHZ" only. Repeat Steps 2 and 3 and note the difference.

HPGL Plotter Files for Graphics Hardcopies

(1) Read in the file "ex1.ckt".

(2) Exit the editor, invoke the display option and then press the **<PRSC>** key. Select the "Printer" option as "HPGL for WP" and exit the pop-up window. This will generate the HPGL file for the first, and only for the first graphics display following this selection.

(3) Invoke View 1 of the Parametric display option (several circles).

(4) Open another window and view the newly generated HPGL file "osa90.plt" using "more". Close the window.

Graphical Views

(1) Study the view definitions in "ex1.ckt" and "ex9.ckt".

(2) Make simple modifications by adding display attributes such as ".red", ".green", ".cream" for colour, and ".point", ".square", "triangle" for shape. Invoke the corresponding displays.

Exit OSA90/hope™

(1) Exit OSA90/hope™. Remove the files "ex*.*" and "lcfilter". Log out.

(2) Before the next lab period on October 5, use "ftp" utility to transfer the files "osa90.plt" and "hpgl.man" to a PC. Experiment with incorporating the plot into WordPerfect.

R.M. Biernacki, September 1992

COMPUTER ENGINEERING 4KC3:
SIMULATION AND OPTIMIZATION

Nonlinear Memoryless Circuits: DC and Time-Domain Simulation

Lab #2

Objectives

This lab is intended to familiarize you with DC and time-domain simulations of nonlinear memoryless circuits (i.e., containing no dynamic components such as capacitance or inductance) using built-in simulators of OSA90/hope™. It is also intended to refresh your theoretical knowledge of frequency-domain representation of periodic signals (Fourier series).

Software

OSA90/hope™ on Sun SPARCstations (JHE 215, Monday, Oct. 5, 1992, 2:30 - 5:30 pm.)

Circuit Diagram and Parameter Values

A circuit with the diode bridge (full-wave rectifier) will be used throughout this lab. It is shown in Figure 2-1.

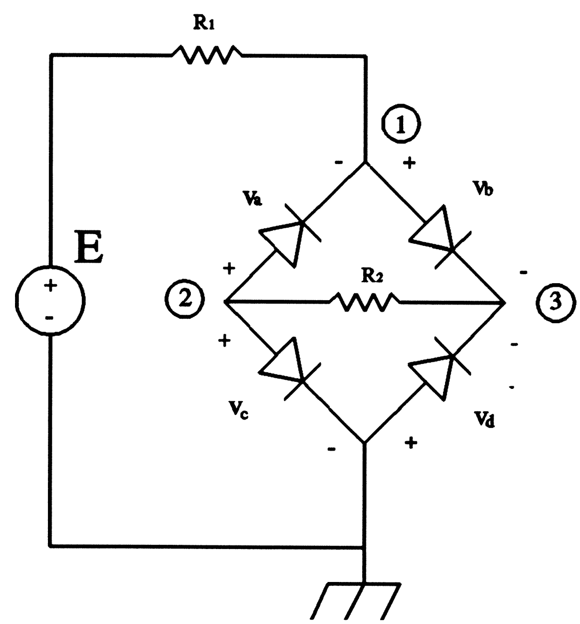

Figure 2-1.

The diodes are assumed memoryless, i.e., their capacitances are neglected. All diodes are identical and are fully described by the IV characteristic given by the nonlinear equation

i_d = IS * [exp(v_d*q/(N*k*TEMP)) - 1].

IS, the saturation current, is such that the diodes are so called "10mA" diodes: i_d is 10mA for V_d = 0.7V (you will have to find the value of IS). N, the emission coefficient, is 1, and TEMP, the temperature, is 298°K. The parameters q and k in the above equation are the electron charge and the Boltzmann constant, respectively. The expression k*TEMP/q is denoted by v_t and is called *thermal voltage.* Its value in this lab is constant and equals 25.67 mV. The aforementioned diode equation is implied when you define a diode within OSA90/hope™ using the keyword "DIODE". You can use the default values for all parameters except for IS. Other parameters in the circuit are:

R1 = R2 = 1kΩ, and various values for E.

Procedure

Preliminary Calculations

(1) Derive the expression to find the saturation current IS for a "10mA" diode.

The result is: IS = ____________________.

(2) Derive the expression to find the conductance of a linearized (companion) model of the diode at a given v_d = VD. The result is: g_d = ____________________.

Create the OSA90/hope™ Input File

(1) Create the Model block. Describe circuit elements and topology using "VSOURCE" (Manual Chapter 6 - "Circuit Models"), "RES" (Manual Chapter 8 - "Linear Elements"), and "DIODE" (Manual Chapter 7 - "Nonlinear Elements"). Define nodal voltages v1, v2 and v3 using *Voltage Labels* (Manual Chapter 6 - "Circuit Models"). Complete circuit description using the CIRCUIT statement (Manual Chapter 6 - "Circuit Models"). Define all parameters either as constants or by labels.

(2) Create the Sweep block (Manual Chapter 9 - "Simulation"). Define the simulation type as "DC". Select E as the sweep parameter, initially with three values: 10V, 1V and -10V. Define the responses to be simulated as the node voltages: v1, v2 and v3.

(3) Show your input file to the instructor.

Simulation Experiment 1

(1) Exit the file editor and parse the circuit file by pressing <F7>. Press <D> to choose the "Display" option. Press <X> to choose "Xsweep" option. Use "Numerical" option to obtain the numerical output (Manual Chapter 9 - "Simulation). Complete the following Table

Table 2.1

E(V)	v1(V)	v2(V)	v3(V)
10			
1			
-10			

(2) In the space below comment on the values of v2 and v3 at E = 10V and E = -10V.

(3) Show your results to the instructor.

Simulation Experiment 2

(1) Augment your input file to calculate the "output" voltage Vout = v3 - v2, and the conductance g_d of the linearized diode model for the diode denoted by the voltage V_b in Figure 2-1. Resimulate the circuit and complete the following Table

Table 2.2

E(V)	Vout(V)	$g_d(1/\Omega)$
10		
1		
-10		

(2) In the space below comment on your results.

(3) Show your results to the instructor.

Simulation Experiment 3

(1) Define a new sweep parameter T (time) and sweep it through 51 points (N = 50) in one period of the sinusoidal source voltage

$$E(t) = E_m \sin(2\pi f T)$$

where E_m = 10V and f = 50Hz. Define the source voltage as a function of the sweep parameter T using the above shown expression. Set up your sweep definition to display Vout together with the source voltage E(t). Use repetitive DC simulations to obtain results. In the space below sketch the time domain waveforms generated by the program on the screen.

(3) Show your results to the instructor.

Harmonic Analysis of the Rectified Voltage

(1) Invoke "Numerical" display option for the results of time domain analysis performed in "Simulation Experiment 3". Select Vout for the output. Edit the numerical output by removing any text and the values of time points, leaving only the numerical values of Vout. Save the results in a file "waveform.inc".

(2) Create a new simple input file for OSA90/hope™ consisting of the Expression and Sweep blocks. Define an array with the time domain samples saved in the file "waveform.inc". Use the DFT_TF built-in transformation to generate the frequency domain spectrum of Vout. Use RI2MP built-in transformation to generate the magnitude spectrum of Vout. Display the magnitude spectrum using "OSA90.Display>Array" menu option. In the space below sketch the results generated by the program on the screen.

(3) Show your results to the instructor.

Team: ____________________

Name: ____________________ Student ID ____________________

Name: ____________________ Student ID ____________________

Deadline: The Afternoon of Laboratory

R.M. Biernacki, October 1992

COMPUTER ENGINEERING 4KC3:
SIMULATION AND OPTIMIZATION

Performance-Driven Design of Nonlinear Circuits

Lab #3

Objectives

This lab is intended to familiarize you with performance-driven design of nonlinear circuits using built-in optimizers and simulators of OSA90/hope™. It is also intended to show you how to formulate and optimize user-defined responses derived from the basic built-in responses of OSA90/hope™.

Software

OSA90/hope™ on Sun SPARCstations (JHE 215, Monday, Oct. 19, 1992, 2:30 - 5:30 pm.)

Circuit Diagram and Parameter Values

A simple single-stage amplifier will be used throughout this lab. It is shown in Figure 3-1.

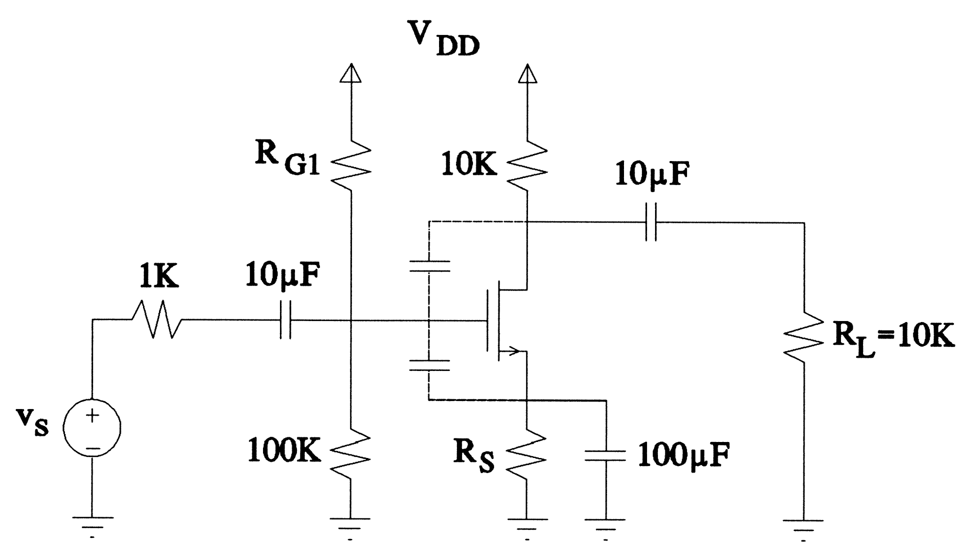

Figure 3-1.

The amplifier is to be designed with a depletion type *n*-channel MOSFET with I_{DSS} = 4mA and the pinch-off voltage V_P = -4V. The parasitic capacitances of the FET are assumed as C_{gd} = 10pF and C_{gs} = 0.1μF. Other parasitic effects are neglected. The DC power supply is fixed at V_{DD} = 20V. The resistances R_{G1}, R_S and the capacitance C_{gs} will be optimizable.

Procedure

Create the OSA90/hope™ Input File

(1) Define the Control block to use "Non_Microwave_Units".

(2) Create the Model block. Describe the circuit elements and topology using "RES", "CAP" and/or "PRC" (Manual Chapter 8 - "Linear Elements"), "FETM" (Manual Chapter 7 - "Nonlinear Elements"), "VSOURCE" (Manual Chapter 6 - "Circuit Models"), and "PORT" (Manual Chapter 6 - "Circuit Models"). Complete the circuit description using the CIRCUIT statement (Manual Chapter 6 - "Circuit Models"). The following hints should be helpful in setting up the circuit description.

   (a) Use two separate DC bias sources: one for the gate and the other for the drain. Define a label such as VDD and apply it to both sources. This will have the same effect as defining one source only. The advantage is that you will be able to calculate and optimize the gate and drain currents.

   (b) Include the input source resistance in the "PORT" definition. Define the amplitude of the input voltage v_s through a label. This will allow you to sweep its value. The input source generates a sinusoidal voltage.

   (c) The load resistance R_L may or may not be included in the output "PORT" definition. For some experiments it might be advantageous to include R_L in the 2-port while for others it might be better to define it as the terminating impedance.

(3) Create the Sweep block (Manual Chapter 9 - "Simulation"). Initially define one sweep set with the simulation type of "DC". No sweep parameters will be needed, so only numerical output will be available. Define the currents through the DC sources as the responses to be simulated.

(4) Show your input file to the instructor.

Experiment 1: Design of the FET Biasing Circuit

(1) Assume the following values for the unknown resistances: R_{G1} = 100kΩ and R_S = 1kΩ, and perform DC simulation. Your results are

I_G = ______________________ and I_D = ______________________

(2) Define R_{G1} and R_S as optimization variables. Create the Specification block (Manual Chapter 11 - "Optimization"). Define one specification set of "DC" simulation type with the gate and drain currents as the responses to be optimized. Optimize the biasing circuit to get $I_G < 17\mu A$ and $I_D = 1mA$. Use the ℓ_1 optimizer. Your results are

R_{G1} = ______________________ and R_S = ______________________

(3) Resimulate the circuit and save the input file. Now, your results are

I_G = ______________________ and I_D = ______________________

(4) Show your results to the instructor.

Experiment 2: Small-Signal Simulation of the Amplifier

(1) Augment your Model block of the input file to calculate the voltage gain Vgain = V_{out}/V_s where V_{out} is the voltage across R_L. Vgain can be calculated from the *S* parameters in the following way. If you select the reference resistance for the calculation of *S* parameters as the input resistance $R_{ref} = R_{in}$ and if you include R_L in the 2-port then the voltage gain can be expressed as

$$\text{Vgain} = S_{21} / (1 - S_{22})$$

Alternatively, if R_L is excluded from the 2-port then (again for $R_{ref} = R_{in}$)

$$\text{Vgain} = S_{21} / [(1 - S_{22}) + (1 + S_{22})*R_{ref}/R_L]$$

You can implement either of the two formulas, but be careful of how you define R_L. In any case remember that the *S* parameters are complex numbers. Since only the magnitude of Vgain will be of interest define Vgain as the absolute value of the corresponding expression. Also, define a new label, say "K", to be used in an exponential frequency sweep.

(2) Define a new sweep set in the Sweep block. The simulation type should be "AC". Define the exponential frequency sweep from 10Hz to 10kHz, 3 points per decade. You will need to define an expression "FREQ=(10^((K+2)/3))" where "K" is swept linearly. The corresponding display, linear in "K", will produce a logarithmic scale for frequency. Define an appropriate "RREF" and specify Vgain as the response to be simulated. Also specify "FREQ" as a response label in order to make it available for display.

(3) Simulate the circuit and complete the following Table.

Table 3.1

K	1	4	7	10
f				
Vgain				

(3) Show your results to the instructor.

Experiment 3: Optimization of the Frequency Response

Your previous experiment indicates that the 3dB bandwidth does not extend to 10kHz. It is known that the parasitic capacitances of the FET are responsible for the high frequency drop of the response. The question to answer through this experiment is: What is the largest allowable value of the parasitic capacitance C_{gs} for the 3dB bandwidth to be extended to 10kHz?

(1) Designate C_{gs} as the optimization variable. Modify the Specification block by commenting out the existing "DC" specification set and creating a new "AC" specification set. Define only one specification at 10kHz in the form "Vgain > ...". Do not forget to specify "RREF".

(2) Optimize the circuit using the ℓ_2 optimizer. Your result is

$$C_{gs} < \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_$$

(3) Resimulate the circuit and save the input file. Now, the frequency response is

Table 3.2

K	1	4	7	10
f				
Vgain				

(4) Show your results to the instructor.

Experiment 4: Large-Signal Simulation of the Amplifier

(1) Define a new sweep set in the Sweep block. The simulation type should be "HB". Define the amplitude of the input source voltage as the sweep parameter and specify the sweep range from 0.2V to 2V with the step of 0.3V. Set the frequency of the input source to 1kHz. The output port must now include R_L, so it should be excluded from the 2-port. Define MVout and PVout as the response labels. Define a graphical view to display simultaneously two periods of the output voltage waveforms corresponding to all values of V_s.

(2) *Optional:* Define the output power spectrum in an array POUT[0:N_Spectra] (N_Spectra is a built-in label, which in our case defaults to 4). Create an expression for the harmonic distortion h which is defined as the square root of the ratio of the power at all higher harmonics ($P_2+P_3+...$) to the power at the fundamental frequency (P_1). Include POUT and h in the sweep set.

(3) Simulate the circuit and, in the space below, sketch the output voltage waveforms.

(4) *Optional:* Complete the following Table.

Table 3.3

V_s (V)	MVout[1] (V)	POUT[1] (mW)	*h* (%)
0.2			
0.8			
1.4			
2.0			

(4) Show your results to the instructor.

Team: ____________________

Name: ____________________ Student ID ____________________

Name: ____________________ Student ID ____________________

<u>Deadline:</u> November 2, 1992

R.M. Biernacki, October 1992

COMPUTER ENGINEERING 4KC3:
SIMULATION AND OPTIMIZATION

Device Modeling from Experimental Data

Lab #4

Objectives

This lab is intended to familiarize you with device modeling using built-in optimizers and simulators of OSA90/hope™. At the completion of this lab you should be able to better understand the concepts of different models: small-signal, large-signal, linear, bias dependent and nonlinear, and to apply optimization for extracting model parameters from measurement data.

Software

OSA90/hope™ on Sun SPARCstations (JHE 215, Monday, Nov. 2, 1992, 2:30 - 5:30 pm.)

Measurement Setup and Device Data

A microwave Schottky barrier FET (MESFET) has been measured in the setup shown in Figure 4-1. Measurements of S parameters with respect to 50Ω were taken at the input and output reference planes for 17 frequencies in the range from 2GHz to 18GHz and for three values of the gate bias voltage V_G: 0, -1.74 and -3.1 volts. The drain bias voltage V_D was fixed at 4V. The blocking capacitors of 1nF and inductors of 10μH were used to decouple the DC biasing circuit from the RF (or AC) circuit. The resulting S parameters are contained in an ASCII file generated by MicroCAT™ Test Executive system from Cascade Microtech. Make your own copy of that file by executing the command "cp /home/engine/ee761/cascade.dat ./"

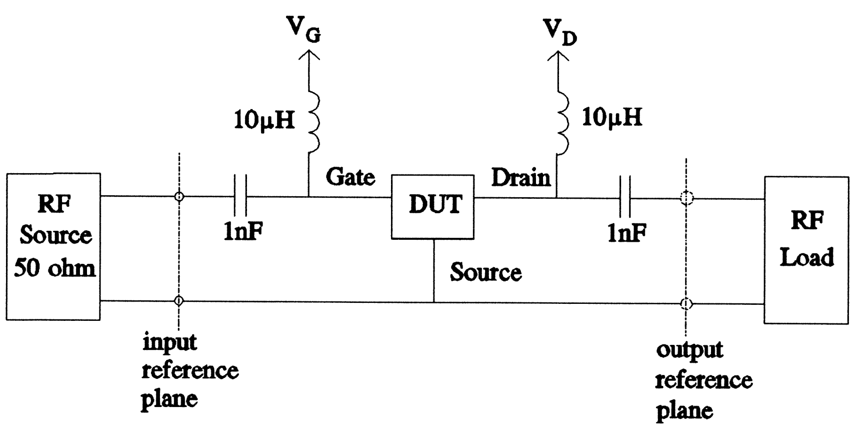

Figure 4-1.

Throughout this lab you will investigate two models for the FET. The first one is a simple small-signal model which may be suitable for simulating the FET around a specific operating point, determined and established separately. This model is shown in Figure 4-2. It consists of a voltage-controlled current source and three lumped linear components. If the biasing of the FET is dropped out of the picture the resulting circuit is linear. The second model, shown in Figure 4-3, is a global, large-signal nonlinear model which accounts for all nonlinearities, including biasing. In this lab you will use the Materka and Kacprzak built-in intrinsic nonlinear model (FETM) together with a built-in super-component "Extrinsic2" which consists of a number of linear elements connected internally in a predefined manner (Manual Chapters 7 and 8 - "Nonlinear Elements" and "Linear Elements").

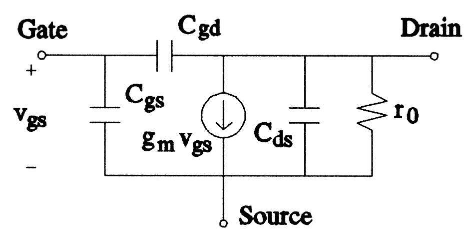

Figure 4-2.

Procedure

Experiment 1: Small-Signal FET Modeling

(1) Create the OSA90/hope™ Input File. It is recommended that you use default microwave units. Define the Model block. Describe the circuit of Figure 4-1 with the model of Figure 4-2 put in place of the device under test (DUT). Use "CAP", "VCCS" and "RES". You do not need to include the bias sources in this experiment, and you may exclude the blocking capacitors and inductors (if so, the overall circuit will simply reduce to that of Figure 4-2). Define the ports using "PORT" statements. Assume the following values for model parameters.

$C_{gs} = C_{gd} = C_{ds} = 1\text{pF}$ $\qquad$ $g_m = 10$ mA/V $\qquad$ $r_0 = 50\Omega$

All these parameters are to be optimizable. Be careful when you define the "VCCS". The orientation of the source in Figure 4-2 is opposite to that in the Manual. After completing the circuit description with the "CIRCUIT" statement define the array "SP_SIM[8]" of simulated S parameters in the following order: Re(S_{11}), Im(S_{11}), Re(S_{21}), Im(S_{21}), Re(S_{12}), Im(S_{12}), Re(S_{22}), Im(S_{22}), which is the order of the data in each row in the file "cascade.dat".

(2) Define the array "SP_DATA[8]" and initialize it with the S parameters for V_G = -1.74V at 2GHz (copy the corresponding row, without the first number, from the data). Define the

error functions in the array "SP_ERROR[8]" as the difference between the arrays "SP_SIM" and "SP_DATA". Close the Model block with the "End" statement.

(3) Define the Sweep block with one sweep set of the "AC" type to simulate the circuit at a single frequency of 2GHz (only numerical output will be available). The responses of interest are "SP_SIM" and "SP_ERROR". Define the Specification block with one specification set of the "AC" type. Define a single specification of 0 for the whole array "SP_ERROR" at 2GHz. Save your file.

(4) Perform simulation and then invoke the ℓ_1 optimizer. After optimization is completed, perform circuit simulation again, go to the file editor and save the back-annotated file under a different name. Complete the following Table.

Table 4.1

	S_{11}	S_{21}	S_{12}	S_{22}
Measurement Data				
Model Before Optimization				
Model After Optimization				

The extracted parameters of the model are

C_{gs} = ________ C_{gd} = ________ C_{ds} = ________ g_m = ________ r_0 = ________

(5) Show your results to the instructor.

Experiment 2: Checking Validity of the Small-Signal FET Model

In this experiment you will investigate whether the model established in Experiment 1 is suitable for simulating device behaviour at a different operating point or in the whole frequency range.

(1) In the file saved after optimization performed in Experiment 1 replace the contents of the array "SP_DATA" with the S parameters for V_G = -3.1V at 2GHz (copy another row, without the first number, from the data). Repeat Step 4 of Experiment 1 without saving the resulting file. In the space below comment on the suitability of the model at different bias points.

(2) Retrieve the file saved after optimization performed in Experiment 1. Redefine your "SP_DATA" array to make it a two-dimensional array "SP_DATA[17,8]" and initialize it with the whole subset of the measurement data corresponding to V_G = -1.74V. Do not forget to remove the first column of the data (frequencies). Define a new array "FREQs[17]" and initialize it with the frequencies at which the data was taken. If you use default microwave units enter the values in GHz but do not specify units (i.e., 2.0, 3.0, etc.). Now, the measurement data must be selected from the matrix "SP_DATA". You can do it by defining a frequency index "L", which will be swept, and selecting one row of the data for each specific value of "L" using the matrix function "ROW" (Manual, p. 4-20) to create a new array "SELECT_SP_DATA[8]". You will also need to redefine "SP_ERROR". Finally, extend the sweep and specification sets from a single frequency to all points by sweeping "L" from 1 to 17 and setting "FREQ" to the corresponding element of the array "FREQs". Repeat Step 4 of Experiment 1. Save the files before and after optimization. In the space below comment on how the model fits the measurement data at 2GHz and at all frequencies before and after optimization.

(3) Show your results to the instructor.

Experiment 3: Large-Signal FET Modeling

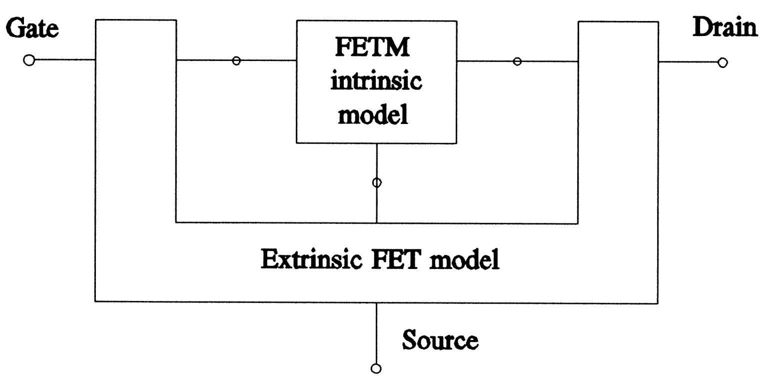

Figure 4-3.

The preceding experiments indicate that a small-signal linear model is not capable of covering a large range of operating conditions, even for small-signal simulations. A linear model should at least have the parameter values that are bias dependent (bias dependent model). While such a model could be suitable for small-signal simulations under different bias conditions, only a true nonlinear model can be used as a global model. In this experiment you will use optimization to extract parameters of the Materka and Kacprzak model to fit simultaneously all measurement data.

(1) Retrieve either of the files used in Experiment 2, Step 2. Go to the secondary window of the editor. Read in the file "/home/engine/ee761/lab4model.inc". Mark the whole contents of the file and copy it to the primary file. This is the model shown in Figure 4-3 to be put in place of DUT in Figure 4-1 and should replace the description of the small-signal model used in preceding experiments. You may have to adjust the node numbers. You also need to include the blocking capacitors and inductors of Figure 4-1, and, using "VSOURCE", to define DC bias sources. When defining V_G, introduce a new array "VGS[3]" and a new bias index "K", which will be swept, and select the value of V_G using "VDC=VGS[K]". Adjust the number of rows of the matrix "SP_DATA" to accommodate all 51 lines of data from the file "cascade.dat". It is recommended that you edit that file (do not forget to delete the first column), save it under a different name such as "sp_data.inc" and use the "#include" directive in the input file. Now, to select the row of the data which corresponds to the Kth bias point and the Lth frequency you need the selector index "KL = (K-1)*17 + L". Finally, you need to define a double sweep in the Sweep and Specification blocks. Make "K" as the outer sweep label and "L" as the inner sweep label. Save your file and show it to the instructor.

(2) *Optional:* Define the parameter "NAME" for the drain bias source. Define the array "Ids_DATA[3]" and initialize it with the measured values of the current I_{ds} contained in the file "cascade.dat". Define the array "ID_ERROR" as the difference between the Kth element of "Ids_DATA" and the simulated DC current through the V_D source, multiplied by 50, the weighting factor for optimization. Include "ID_ERROR" in the Sweep and Specification blocks.

(3) Perform simulation and view the error functions. Invoke the ℓ_1 optimizer. After optimization is completed, perform circuit simulation again, go to the file editor and save the back-annotated file under a different name. Again, view the error functions. Complete the following table with approximate values (order of magnitude).

Table 4.2

	Average Error	Maximum Error
Model Before Optimization		
Model After Optimization		

(4) *Optional:* Define a graphical view to display the fit of S_{21} for all frequencies and all bias conditions. Use continuous curves for displaying the simulated responses and "circles" to display measured data. You can define either a rectangular plot or polar plot. Sketch your results in the space below.

You can also generate the HPGL file. Before the next lab period you can transfer the file to your PC, produce a hardcopy of the plot and hand it in.

(5) Show your results to the instructor.

Team: ____________________

Name: ____________________ Student ID ____________________

Name: ____________________ Student ID ____________________

Deadline: November 16, 1992

R.M. Biernacki, October 1992

COMPUTER ENGINEERING 4KC3:
SIMULATION AND OPTIMIZATION

Statistical Design Centering

Lab #5

Objectives

This lab is intended to familiarize you with characterization of statistical variations of circuit parameters, Monte Carlo analysis and yield-driven design of nonlinear circuits using OSA90/hope™.

Software

OSA90/hope™ on Sun SPARCstations (JHE 215, Monday, Nov. 16, 1992, 2:30 - 5:30 pm.)

Procedure

Experiment 1: Monte Carlo Analysis of a Simple Voltage Divider

(1) Create the OSA90/hope™ input file for a simple voltage divider consisting of two resistors $R_1 = R_2 = 50\Omega$ connected in series. The input DC voltage source of 1V is applied to both resistors and the output voltage is taken across R_2. Create the Model block using "VSOURCE", "RES", "VLABEL" and "CIRCUIT" statements. Define statistical variation of R_1 and R_2 using "UNIFORM" distribution within ±5% interval with respect to the nominal values ("TOL=5%"). Create the MonteCarlo block with one sweep set of the DC type. Specify "N_outcomes = 100" and the output voltage as the response label.

(2) Invoke OSA90.MonteCarlo menu item. After Monte Carlo analysis is finished view the Run Chart of the simulated output voltage. The spread of the output voltage is

min V_{out} = ________, max V_{out} = ________ and variation of V_{out} = ± ________%

(3) Show your results to the instructor.

Experiment 2: Statistical Design Centering of a Small-Signal Amplifier (Figure 5-1)

(1) Retrieve the input file generated during Experiment 3 of Lab #3 "Performance-Driven Design of Nonlinear Circuits". Assume that the nominal value of C_{gs} is 10nF, which satisfies the specification Vgain > 3.5. Define statistical variations of "NORMAL" distribution with the standard deviation of 5% ("SIGMA=5%") for all four resistors R_{G1}, R_{G2}, R_D and R_S, and for the capacitor C_{gs}. You should have 5 statistical variables.

(2) Create the MonteCarlo block with one sweep set of the AC type by copying the existing sweep set from the Sweep block. Leave Vgain as the only response label. Use "N_outcomes = 100". Define design specifications Vgain > 3.5 and Vgain < 5 for yield estimation.

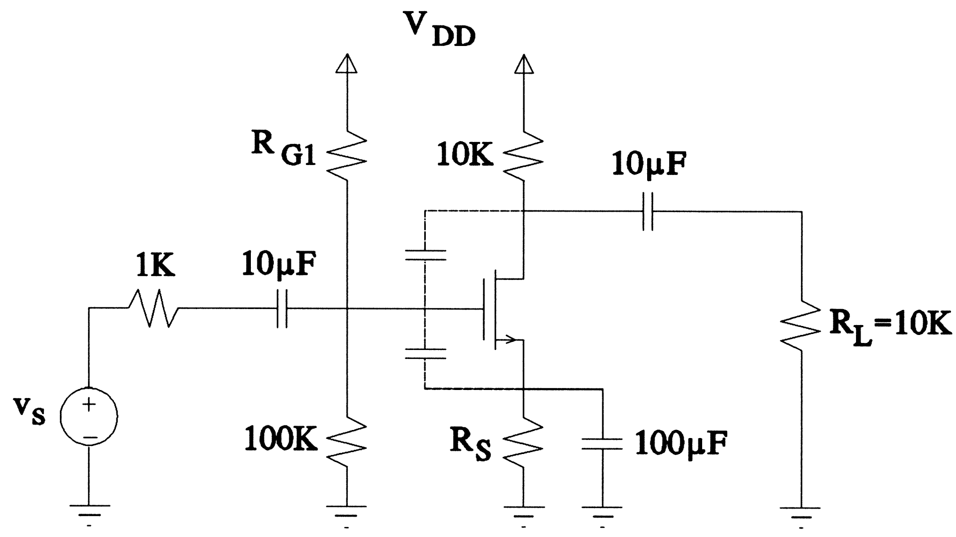

Figure 5-1.

(3) Perform Monte Carlo analysis and invoke OSA90.MonteCarlo.Xsweep menu item to simultaneously view all the responses corresponding to the 100 circuit outcomes generated according to the statistical distribution (statistical response). In the space below sketch the statistical response together with design specifications.

initial yield = __________%

(4) Show your results to the instructor.

(5) Define the nominal values of R_{G1} and R_S as optimization variables. Modify the Specification block to define design specifications consistently with the MonteCarlo block (Vgain > 3.5 and Vgain < 5 for all 10 frequencies swept exponentially from 10Hz to 10kHz).

(6) Invoke OSA90.Optimize menu item. Select "yield" as the optimizer. Once "yield" is selected the pop-up window allows you to choose the number of outcomes to be involved in yield optimization. Select 50 outcomes. Accept defaults for all other options. Perform yield optimization. Then go back to the file editor and change the number of outcomes for Monte Carlo analysis to 300. Perform Monte Carlo analysis and view the statistical response. In the space below sketch the statistical response after yield optimization and report final yield and the values of optimization variables.

yield after optimization = __________%

The values of the optimization variables after yield optimization are

R_{G1} = __________________________ and R_S = __________________________

(7) Show your results to the instructor.

Team: ____________________

Name: ____________________ Student ID ____________________

Name: ____________________ Student ID ____________________

Deadline: The Afternoon of Laboratory

R.M. Biernacki, November 1992

REFERENCES

[1] *OSA90/hope™ Version 2.0 User's Manual*, Optimization Systems Associates Inc., P.O. Box 8083, Dundas, Ontario, Canada L9H 5E7, 1992.

[2] J.W. Bandler, *Electrical Engineering 3K4 Simulation and Optimization I*, Simulation Optimization Systems Research Laboratory, Department of Electrical and Computer Engineering, McMaster University, Hamilton, Canada L8S 4L7, 1988.

Appendix A

Input File "demo01.ckt"

```
!  Example  demo01.ckt
!  a simple example for OSA90
!  Xsweep displays X and Y as functions of Angle
!  Parametric plots of circles

Expression
   Angle: 0;     ! sweep label
   Center: 0;    ! center of the circles

   X: cos(Angle) + Center;    ! X coordinates of points on a circle
   Y: sin(Angle) - Center;    ! Y coordinates
end

Sweep
   Center: 0 1 2 3 4 5
   Angle: from 0 to (2 * PI) N=100  X  Y
   { Parametric  P=Angle  Center=ALL  Title="PARAMETRIC VIEW OF CIRCLES"
     X=X  X_title="cos(Angle) + Center"  Xmin=-4  Xmax=8  NXticks=12
     Y=Y  Y_Title="sin(Angle) - Center"  Ymin=-7  Ymax=2  NYTicks=9 };
end
```

Appendix B

Input File "demo09_o.ckt"

```
!  Example  demo09.ckt
!  optimization with external simulator and FDF via datapipe
!  11-element LC low-pass filter
!  This example takes advantage of user-supplied gradients
!  minimax optimization

! flags for calling the child program

#define  SIMULATION  0  ! SIM protocol, output insertion loss
#define  PASSBAND    1  ! FDF protocol, output Insertion_loss - SPEC
#define  STOPBAND    2  ! FDF protocol, output SPEC - Insertion_loss

Expression
   L1=?0.220272NH?;
   L2=?0.234602NH?;
   L3=?0.250828NH?;
   L4=?0.2679NH?;
   L5=?0.235759NH?;
   C1=?0.217537NF?;
   C2=?0.380367NF?;
   C3=?0.395219NF?;
   C4=?0.359733NF?;
   C5=?0.338273NF?;
   C6=?0.203821NF?;

   X[11] = [C1, L1, C2, L2, C3, L3, C4, L4, C5, L5, C6];

   Omega = 2 * PI * FREQ;

   Passband_Spec: 0.32;  ! dB on Insertion_loss
   Stopband_Spec: 52;    ! dB on Insertion_loss

   Datapipe: FDF  FILE="lcfilter"  NAME=Passband_Error
                  N_INPUT=14  INPUT=(X, PASSBAND, Omega, Passband_Spec)
                  N_OUTPUT=1;

   Datapipe: FDF  FILE="lcfilter"  NAME=Stopband_Error
                  N_INPUT=14  INPUT=(X, STOPBAND, Omega, Stopband_Spec)
                  N_OUTPUT=1;

   Datapipe: SIM  FILE="lcfilter"
                  N_INPUT=13  INPUT=(X, SIMULATION, Omega)
                  N_OUTPUT=1  OUTPUT=(Insertion_loss);
end

Sweep
   FREQ: from 0.01GHZ to 1GHZ step 0.01GHZ
         from 1.025GHZ to 1.4GHZ step=0.025GHZ  Insertion_loss
      {Xsweep  Title="Passband Insertion Loss Of LC Filter"
       Y=Insertion_loss  Ymin=0  Ymax=0.5  NYTicks=5
       Xmin=0  Xmax=1 NXTicks=5}
      {Xsweep  Title="Insertion Loss Of LC Low-Pass Filter"
       Y=Insertion_loss  Xmin=0  Xmax=1.4  NXTicks=7};
end

Specification
   Datapipe:  FREQ: FROM 0.02GHZ TO 1GHZ STEP 0.02GHZ
              Passband_Error;
   Datapipe:  FREQ: 1.3GHZ  Stopband_Error;
end

Control
   Optimizer=Minimax;
end
```

Appendix C

Data File "cascade.dat"

```
NOTE  FET S-parameter measurement for test with HarPE
NOTE  simulating the format by CASCADE MICROTECH
DATE  Nov 22, 1989
NOTE  the first bias
BIAS Vgs=0.0
BIAS Vds=4.0
BIAS Ids=0.177
S2RITABLE 17
 2.00E9     0.5952    -0.7405    -3.351     2.731    0.01574    0.02555     0.5699    -0.2847
 3.00E9     0.2782    -0.8682    -2.258     3.095    0.02697    0.02913      0.507    -0.3408
 4.00E9   0.003826    -0.8774    -1.332     3.088    0.03631    0.02841      0.448    -0.3896
 5.00E9    -0.2089    -0.8241   -0.6258     2.884    0.04307    0.02552     0.3927    -0.4319
 6.00E9     -0.367    -0.7442   -0.1137     2.599    0.04756    0.02184     0.3398    -0.4698
 7.00E9    -0.4831    -0.6561    0.2496     2.296    0.05027     0.0181     0.2879    -0.5043
 8.00E9    -0.5686    -0.5686    0.5039     2.002    0.05169    0.01465     0.2358    -0.5355
 9.00E9    -0.6318    -0.4851    0.6789     1.729    0.05217    0.01162     0.1829    -0.5634
10.00E9    -0.6788    -0.4068    0.7962     1.481    0.05197   0.009091      0.129    -0.5876
11.00E9    -0.7138    -0.3338    0.8709     1.258    0.05129   0.007052    0.07406    -0.6079
12.00E9    -0.7396    -0.2658     0.914      1.06     0.0503   0.005494    0.01827     -0.624
13.00E9    -0.7584    -0.2023    0.9333    0.8828     0.0491   0.004388   -0.03809    -0.6358
14.00E9    -0.7716    -0.1428    0.9347    0.7262    0.04779   0.003704   -0.09467    -0.6432
15.00E9    -0.7804   -0.08692    0.9226    0.5878    0.04644   0.003405    -0.1511    -0.6462
16.00E9    -0.7854   -0.03419    0.9002    0.4659    0.04512   0.003455     -0.207    -0.6448
17.00E9    -0.7874    0.01571    0.8703    0.3588    0.04386   0.003816    -0.2621    -0.6391
18.00E9    -0.7868    0.06306    0.8349    0.2652    0.04271    0.00445    -0.3159    -0.6294
ENDTABLE
NOTE  the second bias
BIAS Vgs=-1.74
BIAS Vds=4.0
BIAS Ids=0.08896
S2RITABLE 17
 2.00E9     0.7854    -0.5682    -2.667     1.616    0.01656     0.0352     0.5055    -0.2722
 3.00E9      0.577    -0.7439    -2.102     2.017    0.03109    0.04451     0.4452    -0.3342
 4.00E9     0.3559    -0.8389    -1.518     2.222    0.04608     0.0479     0.3823    -0.3876
 5.00E9     0.1491    -0.8697   -0.9818     2.265    0.05947    0.04668     0.3197    -0.4302
 6.00E9   -0.03086    -0.8564   -0.5255     2.195    0.07038    0.04242     0.2593    -0.4636
 7.00E9    -0.1815    -0.8155   -0.1548     2.058    0.07865    0.03644     0.2018    -0.4903
 8.00E9     -0.305    -0.7591    0.1372     1.885     0.0845    0.02968     0.1469    -0.5119
 9.00E9    -0.4053    -0.6947    0.3619     1.697    0.08829    0.02276    0.09385    -0.5294
10.00E9    -0.4864     -0.627    0.5311     1.507    0.09038    0.01605    0.04223    -0.5436
11.00E9    -0.5519    -0.5587    0.6554     1.322    0.09111   0.009802  -0.008427    -0.5546
12.00E9    -0.6049    -0.4915    0.7435     1.147    0.09076   0.004127   -0.05839    -0.5626
13.00E9    -0.6476    -0.4261    0.8028    0.9831    0.08957 -0.0009067    -0.1078    -0.5675
14.00E9    -0.6819    -0.3629    0.8389    0.8321    0.08775  -0.005273    -0.1567    -0.5695
15.00E9    -0.7093     -0.302    0.8566    0.6939    0.08546  -0.008975     -0.205    -0.5684
16.00E9    -0.7309    -0.2435    0.8596    0.5685    0.08284   -0.01203    -0.2527    -0.5643
17.00E9    -0.7476    -0.1873    0.8509    0.4553       0.08   -0.01447    -0.2995    -0.5571
18.00E9    -0.7601    -0.1332    0.8332    0.3539    0.07705   -0.01632    -0.3453    -0.5469
ENDTABLE
```

```
NOTE  the third bias point
BIAS Vgs=-3.1
BIAS Vds=4.0
BIAS Ids=0.0408
S2RITABLE 17
 2.00E9      0.835   -0.5042     -1.85     1.044   0.01928    0.04435    0.4908    -0.269
 3.00E9     0.6659   -0.6806    -1.509     1.335   0.03699    0.05763    0.4335    -0.333
 4.00E9     0.4752   -0.7942    -1.136     1.514   0.05638    0.06387    0.3715   -0.3904
 5.00E9     0.2856   -0.8521   -0.7732     1.587   0.07485    0.06398    0.3074   -0.4368
 6.00E9     0.1106   -0.8665   -0.4468     1.577   0.09087    0.05948    0.2439    -0.473
 7.00E9   -0.04368   -0.8502   -0.1682     1.511    0.1038    0.05193    0.1825   -0.5008
 8.00E9    -0.1762   -0.8135   0.06073     1.408    0.1136    0.04263    0.1235   -0.5221
 9.00E9    -0.2881   -0.7641    0.2435     1.285    0.1204    0.03251    0.0668   -0.5382
10.00E9     -0.382   -0.7073    0.3858     1.154    0.1247    0.02227   0.01213   -0.5501
11.00E9    -0.4604   -0.6467    0.4936      1.02    0.1268    0.01233  -0.04087   -0.5583
12.00E9    -0.5257   -0.5845    0.5727    0.8895    0.1272   0.002983  -0.09248   -0.5632
13.00E9    -0.5801    -0.522    0.6279     0.765    0.1261  -0.005595   -0.1429   -0.5649
14.00E9    -0.6251   -0.4603    0.6637     0.648    0.1239   -0.01331   -0.1922   -0.5636
15.00E9    -0.6624   -0.3997    0.6837    0.5396    0.1208   -0.02011   -0.2404   -0.5593
16.00E9     -0.693   -0.3405    0.6908    0.4402    0.1171     -0.026   -0.2875   -0.5521
17.00E9    -0.7179   -0.2829    0.6875    0.3497    0.1128   -0.03098   -0.3334   -0.5421
18.00E9    -0.7379    -0.227    0.6761    0.2681    0.1082   -0.03509    -0.378   -0.5294
ENDTABLE
```

Appendix D

Include File "lab4model.inc"

```
Extrinsic2  1 2 3 4 5
   RG: 0.0119   RD: 0.0006   RS: 0.33   CX: 1.5PF
   LG: ?0.1NH?
   LD: ?0.1NH?
   GDS: ?0.004?
   LS: ?0.1NH?
   CDS: ?0.1PF?;

FETM  1 2 3
   GAMMA: -0.1  KE: 0          SL: 0.2
   KG: -0.25    SS: 0          E: 2
   C10: 0.67PF  CF0: 0.023PF   KF: -0.12
   IG0: 5E-10   ALPHAG: 20     IB0: 8e-12
   ALPHAB: 1    VBC: 20        R10: 5.2
   KR: 0        K1: 1          C1S: 0.0048PF
   IDSS: ?0.2?
   VP0: ?-4?
   TAU: ?3PS?;
```