PREDICTABLE YIELD-DRIVEN CIRCUIT DESIGN EXPLOITING A NOVEL STATISTICAL GaAs MESFET MODEL

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Abstract

This paper presents a comprehensive approach to *predictable* yield optimization of microwave circuits exploiting an analytical statistical model. We utilize a novel small-signal bias-dependent physics-oriented statistical GaAs MESFET model which integrates the DC Khatibzadeh and Trew model for DC simulation with the Ladbrooke formulas for small-signal analysis (KTL). Accuracy of the statistical KTL model is demonstrated by good agreement between Monte Carlo simulations using the model and corresponding simulations using device measurement data. Statistical extraction and postprocessing of device physical parameters are carried out by HarPE. Yield optimization with the statistical KTL model is carried out by OSA90/hope. The yield of a broadband amplifier is significantly improved after optimization. Predicted yield over a range of specifications is verified by device data. The benefits of simultaneous circuit-device yield optimization assisted by yield sensitivity analysis are also demonstrated.

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I. INTRODUCTION

In IC manufacturing, fabricated circuits and devices exhibit parameter values deviating randomly from their nominal (or designed) values. These random variations result in statistical spreads of circuit responses and directly affect production yield, as some manufactured circuits violate design specifications. Therefore, yield optimization is now accepted as an indispensable component of circuit design methodology (e.g., [1–4]). Needless to say, the practical usefulness of yield-driven circuit design depends on the accuracy of the statistical models and the predictability of the design yield.

Statistical modeling is needed to characterize device statistics to provide accurate models for statistical analysis and yield optimization. Purviance *et al.* [5–7] proposed various FET statistical modeling techniques based on equivalent circuit models (ECMs), abstract models and data bases. Bandler *et al.* [1,8,9] investigated statistical modeling of GaAs MESFETs using both ECMs and physics-based models (PBMs) and demonstrated that PBMs are capable of providing better estimates of device statistics than ECMs.

We promote PBMs because they allow characterization of device statistics directly at the geometrical/material parameter level where the statistics originate. Also, for a given process, the nominal values of physical parameters as well as their probable ranges of deviations may be known, providing useful information for numerical techniques employed in statistical modeling.

In this paper we present a novel GaAs MESFET statistical PBM for small-signal applications which we call the KTL (Khatibzadeh/Trew/Ladbrooke) statistical model. It combines the advantages of the Khatibzadeh and Trew model [10,11] and the small-signal Ladbrooke model [12] while overcoming their respective shortcomings. The new model has been implemented in the statistical environment of HarPE [13] and OSA90/hope [14].

We used HarPE to carry out statistical characterization of a GaAs MESFET from wafer measurements provided by Plessey Research Caswell [15]. Statistical modeling requires data for different, but supposedly identical, devices to be taken under identical measurement conditions. Measurement data, unless specifically collected for statistical modeling, may not satisfy this

requirement. Then a meaningful preprocessing of data is needed. We call it alignment of the measured data. Deterministic models are extracted for individual manufactured outcomes and these models are used to generate "pseudo-measured" responses at some other "measurement conditions". We apply the Materka and Kacprzak model [16] to this end.

Employing the new model, we present a comprehensive approach to predictable yield-driven physics-based circuit optimization. We demonstrate for the first time that yield predicted by Monte Carlo simulation using a PBM can be consistent with yield predicted directly from device measurement data [17]. Yield optimization of a broadband small-signal amplifier was carried out using OSA90/hope. Our experiments show that the statistical KTL model is the first analytical model to provide reliable and predictable results in yield optimization.

Finally, we discuss potential benefits of including some active device parameters as design variables. Although device adjustment in IC manufacturing may be expensive to implement, it may be justified if it significantly increases the yield and therefore reduces the production cost. Device optimization may also become more attractive with further advances in technology. We show that a significantly higher yield can be achieved by simultaneous circuit and device optimization when suitable FET parameters such as the gate length and channel thickness are included as design variables. The selection of device parameters for yield optimization can be assisted by yield sensitivity analyses.

II. A NEW STATISTICAL GaAs MESFET MODEL

The KTL small-signal equivalent circuit follows the Ladbrooke model [12] and is shown in Fig. 1. Its attractive statistical properties have already been noticed in [9]. The model includes elements whose values are derived from device physical/geometrical parameters and intrinsic voltages at the DC operating point. These intrinsic voltages may be assumed, as is the case in traditional design: the biasing circuit is designed to attain the desired operating point, or they must be determined separately. If the intrinsic voltages are to be determined by simulation it is important that the same physical parameters are used, thus leading to a consistent model.

In our investigations into statistical PBMs we have seriously considered the Khatibzadeh and Trew model [10,11]. It is an analytical physics-based large-signal (or global) model exhibiting reasonable efficiency for small scale yield optimization problems. However, for small-signal applications, in particular statistical modeling, it is not as accurate as the Ladbrooke model [1]. Details of the Khatibzadeh and Trew approach and the Ladbrooke formulas, including our modifications, can be found in [1,9–14].

To provide for complete DC/small-signal device simulations we combine the Ladbrooke model with the Khatibzadeh and Trew model. The latter is employed to solve for the DC operating point needed in establishing the former. Both models share the same physical parameters, therefore the resulting combined, or integrated, model is consistently defined. The statistical KTL model is then obtained by extracting the statistics of the model parameters from multi-device measurement data.

The model includes the intrinsic FET parameters

$$\{L,\ Z,\ a,\ N_d,\ V_{b0},\ v_{sat},\ E_c,\ \mu_0,\ \varepsilon,\ L_{G0},\ a_0,\ r_{01},\ r_{02},\ r_{03}\} \tag{1}$$

and the linear extrinsic elements

$$\{L_g,\ R_g,\ L_d,\ R_d,\ L_s,\ R_s,\ G_{ds},\ C_{ds},\ C_{ge},\ C_{de}\} \tag{2}$$

where L is the gate length, Z the gate width, a the channel thickness, N_d the doping density, V_{b0} the zero-bias barrier potential, v_{sat} the saturation value of electron drift velocity, E_c the critical electric field, μ_0 the low-field mobility of GaAs, ε the dielectric constant, L_{G0} the inductance from gate bond wires and pads, a_0 the proportionality coefficient, and r_{01}, r_{02} and r_{03} are fitting coefficients [9]. The DC blocking capacitor C_x in Fig. 1 is fixed at 2pF.

The bias-dependent small-signal parameters, namely, g_m, C_{gs}, C_{gd}, R_i, L_g, r_0 and τ, as shown in Fig. 1, are derived using the modified Ladbrooke formulas once the DC operating point is solved for. For instance,

$$\begin{aligned} g_m &= \varepsilon v_{sat} Z/d, \\ \tau &= (0.5X - 2d)L/(v_{sat}(L+2X)), \\ R_i &= L/(Z\mu_0 q N_d (a-d)), \\ C_{gd} &= 2\varepsilon Z/(1+2X/L), \end{aligned} \tag{3}$$

$$r_0 = r_{01} V_{D'S'} (r_{02} - V_{G'S'}) + r_{03}$$

where $V_{D'S'}$ and $V_{G'S'}$ are DC intrinsic voltages from D' to S' and from G' to S', respectively, as shown in Fig. 1. The equivalent depletion depth d and the space-charge layer extension X are defined by

$$\begin{aligned} d &= [2\varepsilon(-V_{G'S'}+V_{b0})/(qN_d)]^{0.5}, \\ X &= a_0\{2\varepsilon/[qN_d(-V_{G'S'}+V_{b0})]\}^{0.5}(V_{D'G'}+V_{b0}). \end{aligned} \tag{4}$$

Following our discrete/normal approach to statistical modeling [8], device statistics are represented by a multidimensional normal distribution characterized by the means, standard deviations and the correlation matrix, with additional one-dimensional mapping employing discrete distribution functions (DDFs) for the marginal distributions.

III. MEASUREMENT DATA INTERPOLATION

We have performed statistical modeling from a sample of GaAs MESFET measurements from Plessey Research Caswell [15]. 69 individual devices (data sets) from two wafers were used. Each device represents a four finger 0.5μm gate length GaAs MESFET with equal finger width of 75μm. Each data set contains small-signal S parameters measured at frequencies from 1GHz to 21GHz with 0.4GHz step and under three different bias conditions (V_{DS} at 5V and V_{GS} approximately at 0V, -0.7V and -1.4V, respectively). DC drain bias currents are also included in the measurements.

The measurement bias conditions vary slightly from device to device, thus we align the different data sets to provide consistent bias points for statistical modeling. It is also desirable to interpolate measured data at some other bias points. The Materka and Kacprzak model is a suitable interpolator for this purpose, because of its excellent single device fitting accuracy for these devices. For each individual device we fit the Materka and Kacprzak model to its corresponding data set. The resulting models are used to interpolate data for each device at two bias points (gate bias -0.5V and -0.7V, drain bias 5V). In this way we generated data sets for 69 devices including DC responses and S parameters from 1GHz to 21GHz with 2GHz step under the two bias conditions.

IV. STATISTICAL MODELING AND VERIFICATION

Our statistical modeling technique consists of two stages: multi-device parameter extraction and postprocessing. The two stages, leading to a concise model described by the means, standard deviations, correlation matrix and DDFs, were carried out by HarPE [13]. After alignment of the measurement data described in the preceding section, KTL model parameters were extracted for each device by fitting the model responses to the corresponding S-parameter data and drain bias currents at gate bias -0.5V and -0.7V and drain bias 5V. The 69 (deterministic) models corresponding to the 69 measured devices were then postprocessed to obtain the parameter statistics. The resulting mean values and the standard deviations are listed in Table I. Histograms of channel thickness and doping density are shown in Fig. 2.

For verification, 400 Monte Carlo outcomes were generated using the statistical KTL model. The statistics of the simulated S parameters for those 400 outcomes were compared with the statistics of the data. The mean values and standard deviations from the data and the simulated S parameters at both bias points and at frequency 11GHz are listed in Table II. Note that the statistics of the data and simulated S parameters are consistent. This validates the statistical properties of KTL.

It should be pointed out that statistical verification of the models is of utmost importance, and virtually every paper on statistical modeling tries to address it. While first and second order statistical moments are frequently considered inadequate (e.g., [7]), full verification of joint probability density functions may not be feasible. We discuss this subject further in Section VI.

V. YIELD OPTIMIZATION

We consider the small-signal broadband amplifier shown in Fig. 3. The specifications for yield optimization are: $|S_{21}|$ = 8dB ± 0.5dB, $|S_{11}| < 0.5$ and $|S_{22}| < 0.5$ for the frequency range 8GHz-12GHz. The matching network elements, namely, L_1, L_2, L_3, L_4, L_5, L_6, C_1, C_2, C_3, C_4 and R, are chosen as design variables. They are also assigned random variations of uniform distribution with a 5% tolerance. Adding these to the FET parameters, we have a total of 28 statistical variables. The optimization was carried out using OSA90/hope [14] on a Sun SPARCstation 1.

First, a nominal minimax design was obtained (after 133 iterations and about 12 minutes CPU time). The yield of the nominal design is estimated as 17.5% by Monte Carlo simulation with 200 outcomes. Using the nominal design as the starting point, yield optimization was performed with 100 outcomes. After 30 iterations (145 minutes CPU time), the yield was increased to 67% as estimated by Monte Carlo simulation with 200 outcomes.

The Monte Carlo sweeps of $|S_{21}|$ before and after yield optimization are shown in Fig. 4. Table III lists the values of the design variables before and after yield optimization.

VI. YIELD VERIFICATION

The significance of yield optimization will be much more convincing if the yield predicted by statistical models can be shown to be consistent with actual device data. To demonstrate that this indeed can be the case, we substitute the KTL model with device data and compare the Monte Carlo yields for both cases. Because the wafer measurements contain small variations in bias conditions between different devices, we use the Materka and Kacprzak model [16] to interpolate individual device data at the same bias point (V_{GB} = -0.7V and V_{DB} = 5V), as discussed in Section III.

The yield predicted by Monte Carlo simulation using the device data and 140 outcomes was 15.7% (nominal design) and 57.9% (after yield optimization). This verifies very well the yields predicted by our model (which are 17.5% and 67%, respectively). The Monte Carlo sweeps of $|S_{21}|$ using the device data are shown in Fig. 5, which are in excellent agreement with those produced by the statistical model (Fig. 4).

To show that the good result is not a singular exception, we varied the design specifications over a range and applied the same procedure. As shown in Table IV, the yields predicted by the model and the device data are in very good agreement in all cases.

We feel that the procedure outlined in this section is suitable for statistical validation of the KTL model. Yield, similarly to mean value or standard deviation, can be considered as a statistical parameter, whose estimate is determined from a sample. It is better qualified to validate the model for the simple reason that yield estimation is what the model is intended for.

VII. YIELD SENSITIVITY ANALYSIS

Yield is a function of device parameters, circuit elements, parameter statistics and design specifications. To select a proper set of variables for yield optimization can be a delicate task. We use OSA90/hope to calculate the sensitivities of yield w.r.t. circuit and design parameters. This analysis reveals the influence of different parameters on yield, and this information can assist us in selecting variables for yield optimization.

To illustrate, we performed yield sensitivity analysis w.r.t. two parameters which were not included in the optimization of the matching network, namely, one design specification and one device parameter (the FET gate length).

Fig. 6 depicts the yield sensitivity w.r.t. the lower specification on the gain (the upper specification was fixed). It shows, for instance, that if the lower specification is relaxed from 7.5dB to 7.3dB, the yield would increase from 67% to 74.5%. Fig. 7 depicts the yield sensitivity w.r.t. the FET gate length. It clearly shows that the gate length has a strong influence on yield and therefore merits inclusion as a variable for yield optimization.

VIII. SIMULTANEOUS DEVICE-CIRCUIT DESIGN

Representing devices by statistical PBMs has a clear advantage over direct use of the measured S parameters: the model can interpolate device behaviour at frequency and bias points not contained in the data, and an unlimited number of outcomes can be generated for Monte Carlo analysis. Also, the use of PBMs presents us with the opportunity of optimizing the parameters of active devices, which is not possible if the devices are represented by S parameters. Although device optimization can be expensive to implement, it may be justified when stringent specifications result in very low yield which cannot be sufficiently improved by optimizing the matching circuit alone.

Consider again the small-signal broadband amplifier. We tighten the upper specification on $|S_{11}|$ from 0.5 to 0.4 in the passband, while the other specifications remain the same. Two separate cases of optimization were constructed as follows. In Case I, only the matching circuits are optimized. In Case II, we include the GaAs MESFET gate length and channel thickness as design variables in

addition to the matching circuits.

In both cases, we first performed a minimax nominal optimization and then a yield optimization. In Case I, at the nominal solution the yield predicted by Monte Carlo simulation using 200 outcomes is only 7.5%. After yield optimization the yield is improved to 27.5%.

In Case II, the yield at the nominal solution is 12.5%, and is increased to 64.5% after yield optimization. Compared with Case I, this drastic improvement in the optimized yield requires relatively small changes in the device parameters: the gate length changed from 0.5μm to 0.4μm and the channel thickness from 0.163μm to 0.14μm.

IX. CONCLUSIONS

A comprehensive approach to yield-driven circuit optimization has been presented. We have addressed various stages of yield-driven CAD: statistical modeling, nominal design optimization, yield optimization, yield verification and device optimization.

We have presented the statistical KTL model: a novel, accurate physics-oriented model for GaAs MESFETs, particularly suitable for statistical device characterization. Our experiments demonstrate its ability to accurately represent the statistical properties of MESFETs. The KTL model is suitable for both nominal design and yield optimization of small-signal circuits. Model accuracy is demonstrated by good agreement between Monte Carlo S-parameter simulations and the statistical parameters of the measurement S-parameter data.

From our experience, the statistical KTL model is the first analytical model to provide reliable and predictable results in yield optimization. Through a broadband small-signal amplifier, we have demonstrated for the first time that yield predicted by Monte Carlo simulation using an analytical PBM can be consistent with yield predicted directly from device mesurement data. Excellent results have been obtained for a variety of design specifications.

Simultaneous device and circuit optimization assisted by yield sensitivity analyses further champions the relevance and benefits of our physics-based technique for MMICs. We believe that device optimization will become more attractive with continuing advances in technology.

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FIGURE CAPTIONS

Fig. 1. Small-signal equivalent circuit where $I_d = g_m V_g e^{-j\omega\tau}$.

Fig. 2. Histograms of (a) channel thickness and (b) doping density obtained from statistical postprocessing of extracted parameters.

Fig. 3. Small-signal broadband amplifier.

Fig. 4. Monte Carlo sweeps of $|S_{21}|$ using the statistical KTL model, (a) before yield optimization and (b) after yield optimization.

Fig. 5. Monte Carlo sweeps of $|S_{21}|$ using device data (140 outcomes), (a) before yield optimization and (b) after yield optimization.

Fig. 6. Yield versus the lower specification on the gain.

Fig. 7. Yield versus the FET gate length.

TABLE I

MESFET MODEL PARAMETERS

Parameter	Mean	Std. Dev. (%)
$L(\mu m)$	0.4997	4.76
$a(\mu m)$	0.1630	5.78
$N_d(m^{-3})$	2.475×10^{23}	4.21
$V_{b0}(V)$	0.2661	34.6
$L_{G0}(nH)$	0.0299	9.02
$r_{01}(\Omega/V^2)$	0.0779	0.17
$r_{02}(V)$	7.7855	0.17
$r_{03}(\Omega)$	534.44	4.86
$R_d(\Omega)$	0.4905	1.42
$R_s(\Omega)$	3.9345	1.29
$R_g(\Omega)$	7.7811	0.34
$L_d(nH)$	6.21×10^{-2}	5.88
$L_s(nH)$	2.15×10^{-2}	7.31
$G_{ds}(1/\Omega)$	2.34×10^{-3}	4.19
$C_{ds}(pF)$	5.89×10^{-2}	2.33
$C_{ge}(pF)$	4.61×10^{-2}	6.12
$C_{de}(pF)$	2.00×10^{-4}	0.05
$Z(\mu m)$	300	*
$v_{sat}(m/s)$	9.5×10^{4}	*
$E_c(V/m)$	1.9×10^{5}	*
$\mu_0(m^2/Vns)$	5×10^{-10}	*
ε	12.5	*
a_0	1.0	*

* Assumed fixed (non-statistical) parameters.

The bias-dependent linear extrinsic element L_g is computed using the Ladbrooke formula [12] with modifications given in [9].

TABLE II

MEAN VALUES AND STANDARD DEVIATIONS OF
DATA AND SIMULATED S PARAMETERS AT 11GHZ

	Bias 1				Bias 2			
	Data		KTL		Data		KTL	
	Mean	Dev.(%)	Mean	Dev.(%)	Mean	Dev.(%)	Mean	Dev.(%)
$\lvert S_{11} \rvert$	0.771	0.67	0.765	0.74	0.775	0.65	0.776	0.72
$\angle S_{11}$	-103.5	1.53	-104.2	1.62	-100.1	1.60	-100.5	1.54
$\lvert S_{21} \rvert$	1.760	2.26	1.707	2.84	1.657	3.23	1.668	2.78
$\angle S_{21}$	97.21	0.72	98.26	0.84	98.10	0.70	100.3	0.73
$\lvert S_{12} \rvert$	0.091	4.10	0.092	4.32	0.097	4.27	0.097	3.85
$\angle S_{12}$	35.59	1.74	35.04	2.13	36.20	1.63	35.45	2.12
$\lvert S_{22} \rvert$	0.576	1.57	0.577	1.66	0.577	1.78	0.579	1.66
$\angle S_{22}$	-39.48	1.42	-39.61	1.37	-39.96	1.26	-40.18	1.24

Bias 1: V_{GS} = -0.5V, V_{DS} = 5V.
Bias 2: V_{GS} = -0.7V, V_{DS} = 5V.

TABLE III

MATCHING CIRCUIT OPTIMIZATION

Design Variable	Before Yield Optimization	After Yield Optimization
C_1(pF)	0.6161	0.4372
C_2(pF)	5.2556	6.1365
C_3(pF)	0.2606	0.2757
C_4(pF)	0.1385	0.1570
$R(\Omega)$	589.00	708.08
L_1(nH)	0.5947	0.9110
L_2(nH)	0.9916	0.9430
L_3(nH)	1.9203	1.6395
L_4(nH)	1.5754	1.7516
L_5(nH)	2.0039	2.3933
L_6(nH)	1.0085	0.7537

TABLE IV

YIELD PREDICTED BY MODEL AND VERIFIED BY DATA

Specification	Before Yield Optimization		After Yield Optimization	
	KTL Predicted Yield (%)	Data Verified Yield (%)	KTL Predicted Yield (%)	Data Verified Yield (%)
Spec. 1	17.5	15.7	67	57.9
Spec. 2	21	20	83	75.7
Spec. 3	44	37.1	98	93.6

Spec. 1: $7.5\text{dB} < |S_{21}| < 8.5\text{dB}$, $|S_{11}| < 0.5$, $|S_{22}| < 0.5$.
Spec. 2: $6.5\text{dB} < |S_{21}| < 7.5\text{dB}$, $|S_{11}| < 0.5$, $|S_{22}| < 0.5$.
Spec. 3: $6.0\text{dB} < |S_{21}| < 8.0\text{dB}$, $|S_{11}| < 0.5$, $|S_{22}| < 0.5$.

200 outcomes are used for yield prediction by the statistical KTL model, 140 for yield verification using the device data.

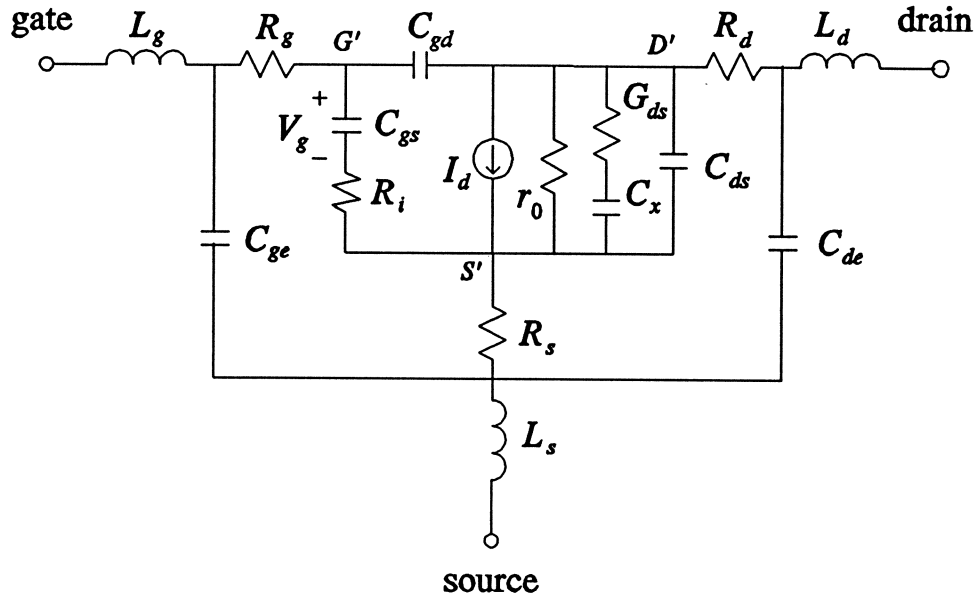
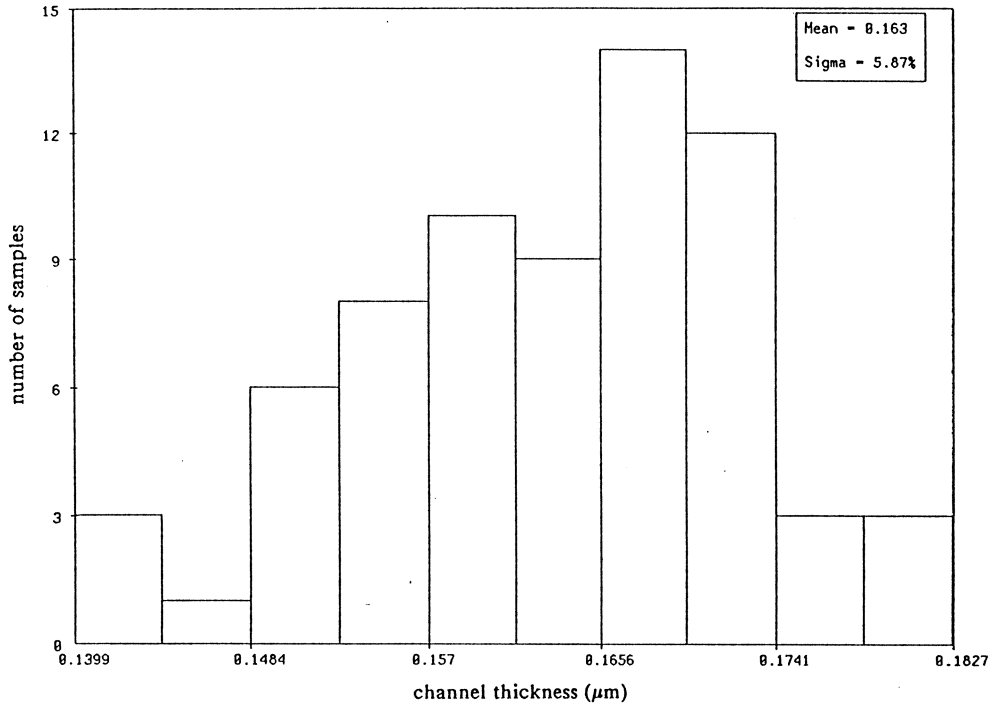
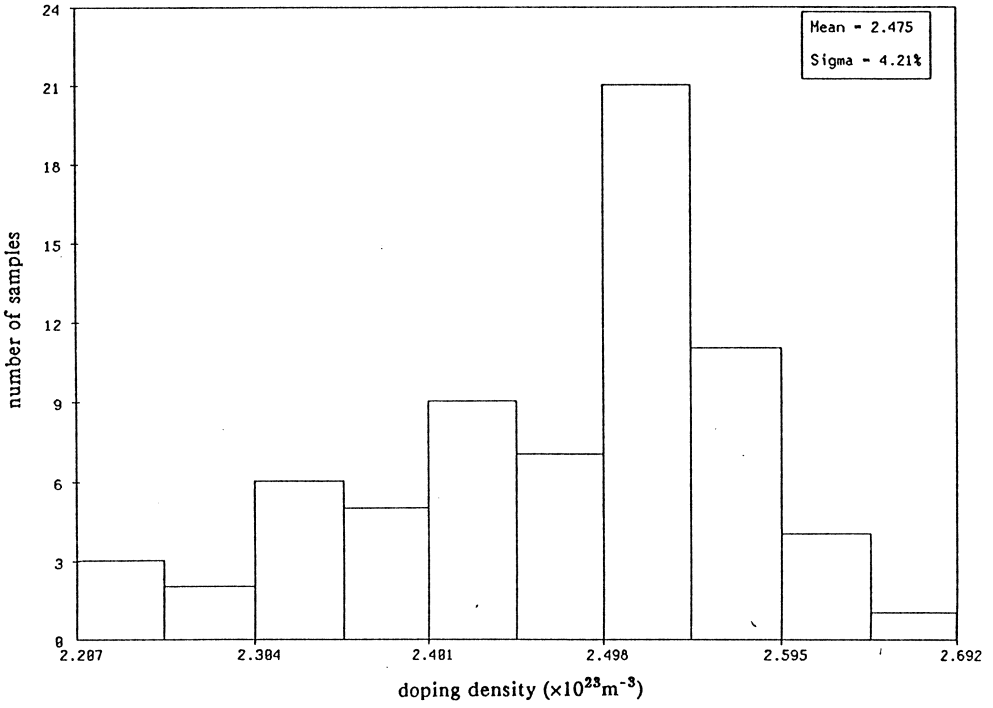


Fig. 1. Small-signal equivalent circuit where $I_d = g_m V_g e^{-j\omega\tau}$.



(a)



(b)

Fig. 2. Histograms of (a) channel thickness and (b) doping density obtained from statistical postprocessing of extracted parameters.

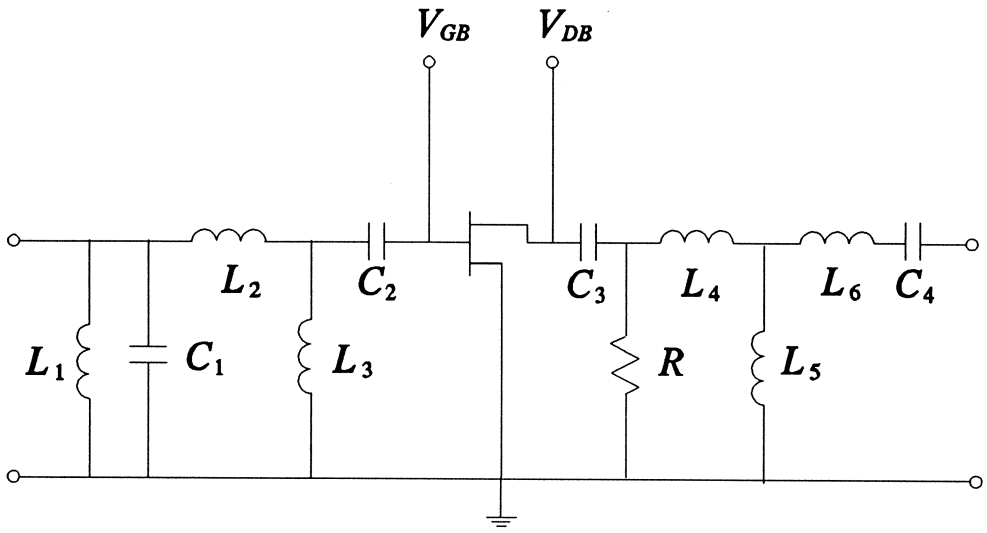
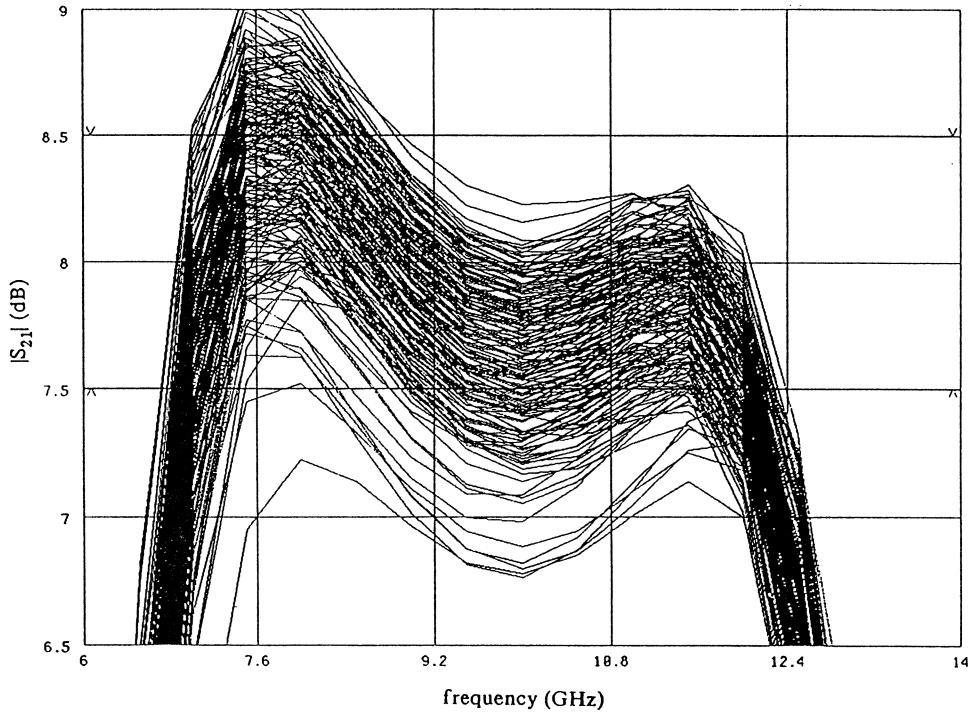
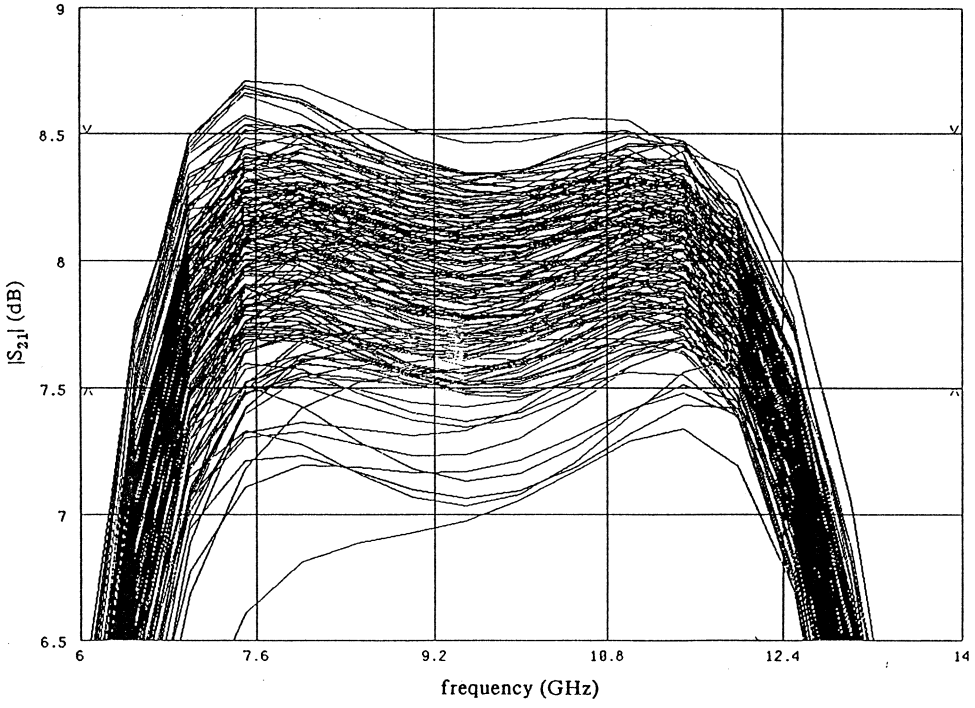


Fig. 3. Small-signal broadband amplifier.

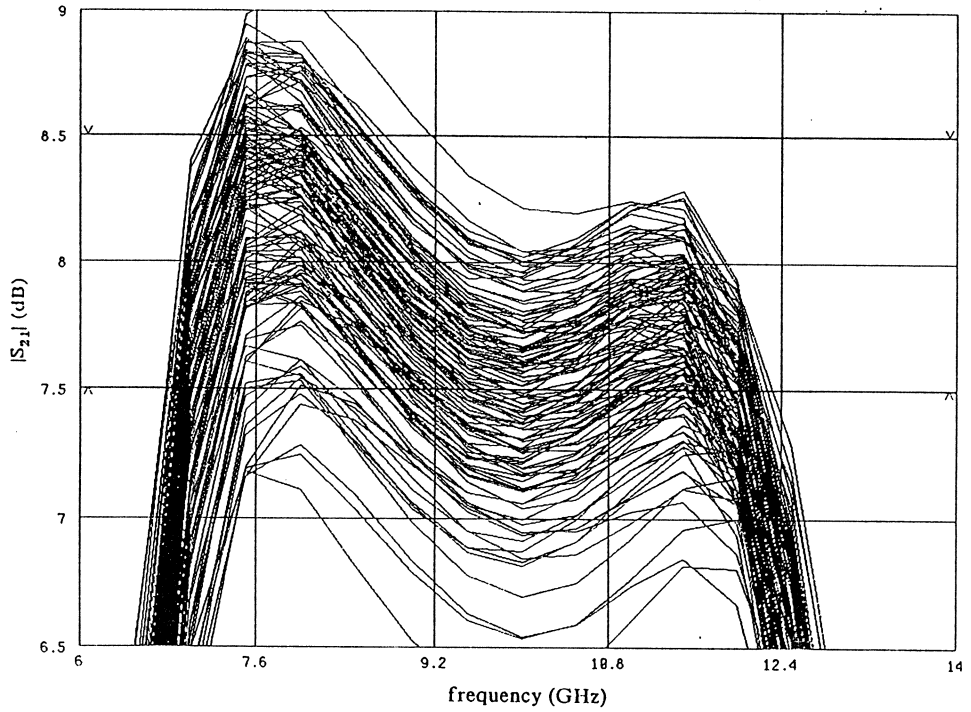


(a)

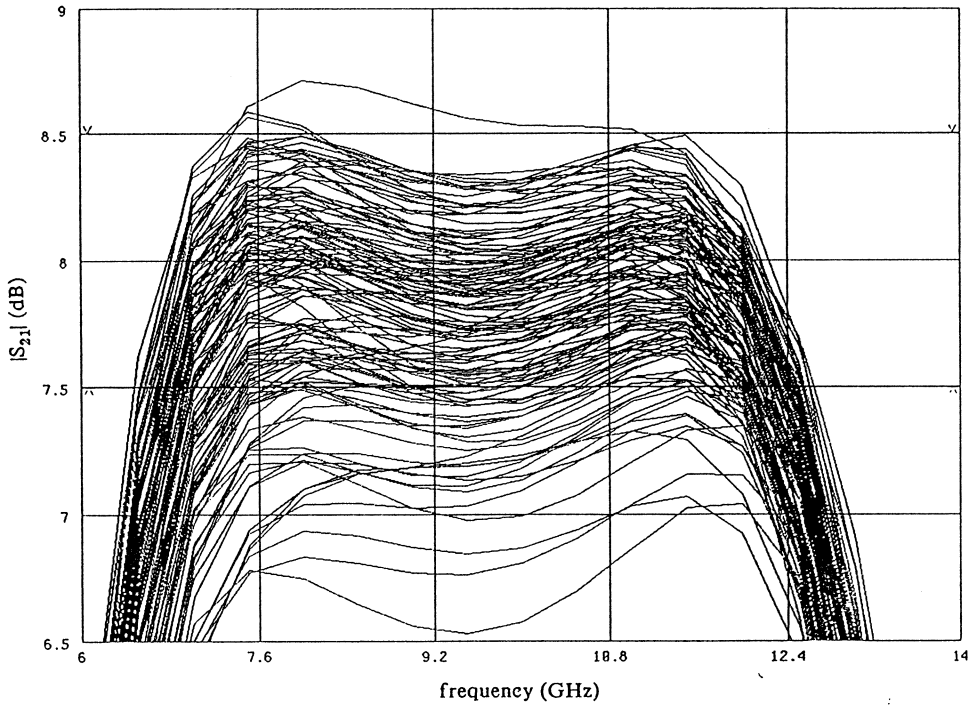


(b)

Fig. 4. Monte Carlo sweeps of $|S_{21}|$ using the statistical KTL model, (a) before yield optimization and (b) after yield optimization.



(a)



(b)

Fig. 5. Monte Carlo sweeps of $|S_{21}|$ using device data (140 outcomes), (a) before yield optimization and (b) after yield optimization.

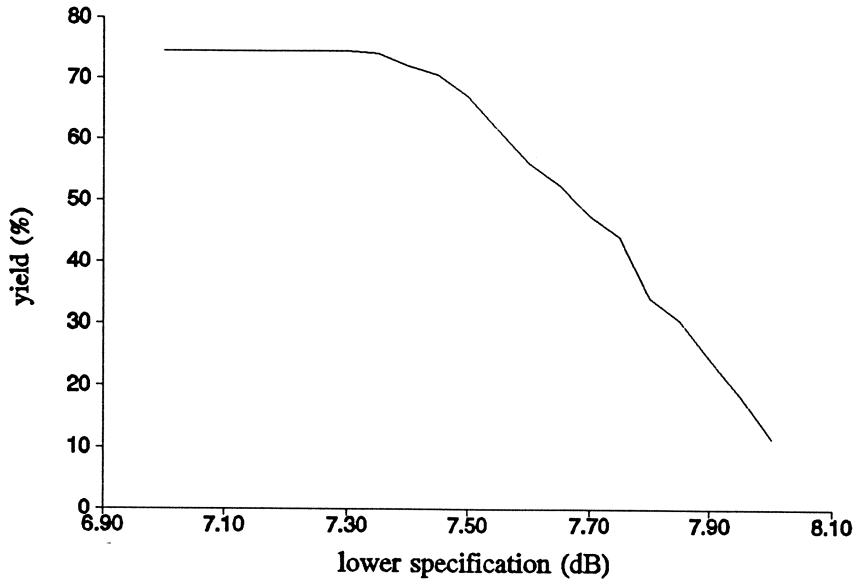


Fig. 6. Yield versus the lower specification on the gain.

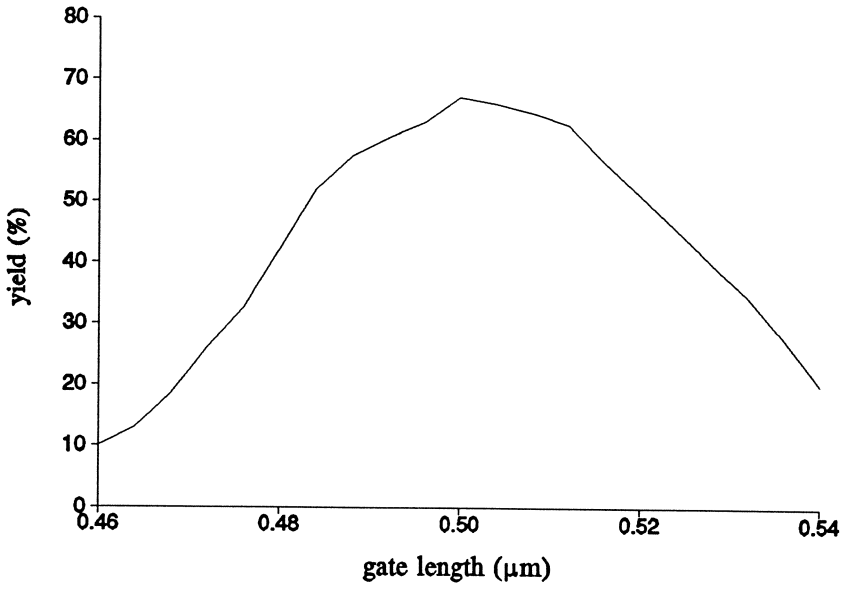


Fig. 7. Yield versus the FET gate length.