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PREDICTABLE YIELD-DRIVEN CIRCUIT OPTIMIZATION

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Abstract

We present a comprehensive approach to yield optimization exploiting PhorsFET, the first reliable statistical GaAs MESFET model. The yield of a broadband amplifier is significantly improved after optimization. Predicted yield over a range of specifications is verified by device data. Yield sensitivity analysis assists simultaneous circuit-device yield optimization.

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SUMMARY

Introduction

Yield optimization of microwave circuits is now widely accepted [1-3]. FET statistics can be represented by equivalent circuit models (ECMs), physics-based models (PBMs) or direct data. The validity of ECM and PBM statistical models and the predictability of the optimized yield need verification.

This paper addresses predictable yield-driven statistical circuit optimization. The new physics-oriented GaAs MESFET model PhorsFET [4] is extracted from statistical data. PhorsFET combines the advantages of the Khatibzadeh and Trew model [5] for DC simulations and the Ladbrooke model [6] for small-signal simulations. Using OSA90/hope™ [7], we perform yield optimization of a broadband small-signal amplifier over a range of design specifications.

PhorsFET allows us to demonstrate for the first time that yield predicted by Monte Carlo simulation based on device statistical models can be consistent with yield predicted directly from measurement data. The advantages of using a model instead of direct data are clear: the model can interpolate device behaviour at frequency and bias points not present in the data and permits variation of device parameters.

The benefits of simultaneous optimization of circuit and device parameters are also demonstrated. Higher yield can be achieved by including suitable FET parameters such as the gate length, gate width and doping density as designable parameters. The significance of device physical parameters in yield optimization is confirmed by yield sensitivity analyses.

The PhorsFET Model

PhorsFET [4] is used for yield optimization. The model includes the intrinsic parameters

$$\{L, Z, a, N_d, V_{b0}, v_{sat}, E_c, \mu_0, \varepsilon, L_{g0}, a_0, r_{01}, r_{02}, r_{03}\} \quad (1)$$

and the linear extrinsic elements

$$\{L_g, R_g, L_d, R_d, L_s, R_s, G_{ds}, C_{ds}, C_{ge}, C_{de}\}. \quad (2)$$

Extracted from the measurements, the statistics of PhorsFET are described by their mean values,

standard deviations, correlation coefficients between model parameters and discrete distribution functions (DDF) [8].

Yield Optimization

Yield optimization of a small-signal broadband amplifier is considered. The circuit schematic of the amplifier is shown in Fig. 1. The specifications for the amplifier are: $|S_{21}| = 8dB \pm 0.5dB$, $|S_{11}| < 0.5$ and $|S_{22}| < 0.5$ for the frequency range 8GHz–12GHz. The matching network elements, namely, L_1, L_2, L_3, L_4, L_5, L_6, C_1, C_2, C_3, C_4 and R, are chosen as design variables. They are also considered as statistical variables uniformly distributed with fixed tolerances of 5%. There is a total of 28 statistical variables including the FET parameters and the elements of the matching circuits. The design was carried out using OSA90/hope [7] on a Sun SPARCstation 1.

First, a nominal design with 11 variables was obtained using minimax optimization. The solution was reached after 133 iterations (about 12 minutes CPU time). The yield at the nominal solution as estimated by Monte Carlo simulation with 200 outcomes is 17.5%. The nominal solution was then used as the starting point for yield optimization with 100 outcomes. The design process finished after 30 iterations (about 2 hours and 25 minutes CPU time) and the yield was improved to 67% as estimated by Monte Carlo simulation with 200 outcomes.

Table I lists the values of the design variables before and after yield optimization. The Monte Carlo sweeps of $|S_{21}|$ before and after yield optimization are shown in Fig. 2.

Yield Verification

To verify the predicted yield we substitute PhorsFET with the device data and compare the Monte Carlo simulations for both cases. We use the Materka and Kacprzak model [9] as an intermediate vehicle to interpolate individual device data. 69 accurate (Materka and Kacprzak) models extracted from the device data were used as sample outcomes by the Monte Carlo simulator to predict yield based on data. The bias point of the amplifier was chosen as V_{GB}=–0.7V and V_{DB}=5V, which is close to the actual bias point at which the measurements were taken. This yield verification process was performed by HarPE™ [10].

140 Monte Carlo outcomes were generated for yield verification. The verified yields before and after yield optimization are 15.7% and 57.9%, respectively. They exhibit excellent agreement with the yields predicted by PhorsFET. The Monte Carlo sweeps of $|S_{21}|$ before and after yield optimization are plotted in Fig. 3. Excellent agreement between Figs. 2(a) and 3(a) and between Figs. 2(b) and 3(b) is observed.

We further performed yield optimization using the same procedure over a range of design specifications. All the results were verified, as shown in Table II. We have achieved a very good match between predicted yield and verified yield.

Yield Sensitivity Analysis

The yield sensitivity analysis feature in OSA90/hope provides insight into the selection of variables in yield optimization. Yield is a complicated function of device parameters, circuit elements, design specifications, and their statistics. The sensitivities of yield w.r.t. these parameters reveal their influence on yield and their relative significance as variables for yield optimization.

To illustrate, we performed yield sensitivity analysis w.r.t. a design specification and w.r.t. a device parameter (the FET gate length). This was done at the solution of yield optimization as listed in Table I.

In Fig. 4, the upper bound of the design specification on the gain was fixed at 8.5dB, and the yield sensitivity w.r.t. the lower bound is shown. For instance, if we relax the lower bound from 7.5dB to 7.3dB, the yield increases from 67% to 74.5%. Fig. 5 depicts the yield sensitivity w.r.t. the FET gate length. It clearly shows that the gate length has a strong influence on yield and therefore merits inclusion as a designable parameter for yield optimization.

Simultaneous Device-Circuit Design

Yield optimization using FET ECMs or direct device data addresses matching circuit design only, since the physical parameters of FETs are not directly accessible through ECMs or data. PBMs directly treat geometrical, material and process-related parameters. They provide an opportunity for designers to optimize device parameters and matching circuits simultaneously.

To demonstrate the potential of using PBMs for yield optimization, we perform yield optimization for two cases. In Case I, only the matching circuits are optimized. In Case II, we include the GaAs MESFET gate length and channel thickness to be design variables in addition to the matching circuits. For better illustration, the specification for $|S_{11}|$ is altered to $|S_{11}| < 0.4$ in the passband, while the other specifications are unchanged.

In Case I, the yield predicted by Monte Carlo (PhorsFET) simulation using 200 outcomes at the solution of the nominal design is 7.5%. After yield optimization the yield is improved to 27.5%. In Case II, we have 12.5% yield at the nominal solution. The yield is increased to 64.5% after yield optimization. The improvement is significant, and the gate length is only reduced from 0.5μm to 0.4μm and the channel thickness from 0.163μm to 0.14μm.

Conclusions

Yield optimization of a broadband small-signal amplifier has been conducted using a new physics-oriented statistical GaAs MESFET model (PhorsFET). Our results demonstrate, for the first time, predictable yield: excellent agreement between PhorsFET yield estimates and yield estimates obtained by utilizing data. Yield sensitivity analyses and simultaneous device-circuit optimization further enhances the relevance of this physics-based technique for MMICs.

References

[1] J.W. Bandler, Q.J. Zhang, J. Song and R.M. Biernacki, "FAST gradient based yield optimization of nonlinear circuits," *IEEE Trans. Microwave Theory Tech.*, vol. 38, 1990, pp. 1701–1710.

[2] R.J. Gilmore, M. Eron and T. Zhang, "Yield optimization of a MMIC distributed amplifier using physically-based device models," *IEEE Int. Microwave Symp. Dig.* (Boston, MA), 1991, pp. 1205–1208.

[3] J.W. Bandler, Q. Cai, R.M. Biernacki, S.H. Chen and Q.J. Zhang, "Physics-based design and yield optimization of MMICs," *Proc. European Microwave Conf.* (Stuttgart, Germany), 1991, pp. 1515–1520.

[4] J.W. Bandler, R.M. Biernacki, Q. Cai, S.H. Chen and S. Ye, "PhorsFET: a new physics-oriented statistical GaAs MESFET model," submitted to 1992 *IEEE Int. Microwave Symp.*

[5] M.A. Khatibzadeh and R.J. Trew, "A large-signal, analytic model for the GaAs MESFET," *IEEE Trans. Microwave Theory Tech.*, vol. 36, 1988, pp. 231–238.

[6] P.H. Ladbrooke, *MMIC Design: GaAs FETs and HEMTs*. Norwood, MA: Artech House, 1989.

[7] *OSA90/hope*™, Optimization Systems Associates Inc., P.O. Box 8083, Dundas, Ontario, Canada L9H 5E7, 1991.

[8] J.W. Bandler, R.M. Biernacki, S.H. Chen, J.F. Loman, M.L. Renault and Q.J. Zhang, "Combined discrete/normal statistical modeling of microwave devices," *Proc. 19th European Microwave Conf.* (London), 1989, pp. 205-210.

[9] A. Materka and T. Kacprzak, "Computer calculation of large-signal GaAs FET amplifier characteristics," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-33, 1985, pp. 129-135.

[10] *HarPE*™, Optimization Systems Associates Inc., P.O. Box 8083, Dundas, Ontario, Canada L9H 5E7, 1991.

TABLE I

MATCHING CIRCUIT DESIGN VARIABLES FOR YIELD OPTIMIZATION

Design Variable	Before Yield Optimization	After Yield Optimization
C_1(pF)	0.6161	0.4372
C_2(pF)	5.2556	6.1365
C_3(pF)	0.2606	0.2757
C_4(pF)	0.1385	0.1570
R(Ω)	589.00	708.08
L_1(nH)	0.5947	0.9110
L_2(nH)	0.9916	0.9430
L_3(nH)	1.9203	1.6395
L_4(nH)	1.5754	1.7516
L_5(nH)	2.0039	2.3933
L_6(nH)	1.0085	0.7537

TABLE II

PREDICTED AND VERIFIED YIELD
FOR DIFFERENT SPECIFICATIONS

	Before Yield Optimization		After Yield Optimization	
Specification	Predicted Yield (%)	Verified Yield (%)	Predicted Yield (%)	Verified Yield (%)
Spec. 1	17.5	15.7	67	57.9
Spec. 2	21	20	83	75.7
Spec. 3	44	37.1	98	93.6

Spec. 1: $7.5dB < |S_{21}| < 8.5dB$, $|S_{11}| < 0.5$, $|S_{22}| < 0.5$.
Spec. 2: $6.5dB < |S_{21}| < 7.5dB$, $|S_{11}| < 0.5$, $|S_{22}| < 0.5$.
Spec. 3: $6.0dB < |S_{21}| < 8.0dB$, $|S_{11}| < 0.5$, $|S_{22}| < 0.5$.

200 Monte Carlo outcomes are used for predicted yield, 140 for verified yield.

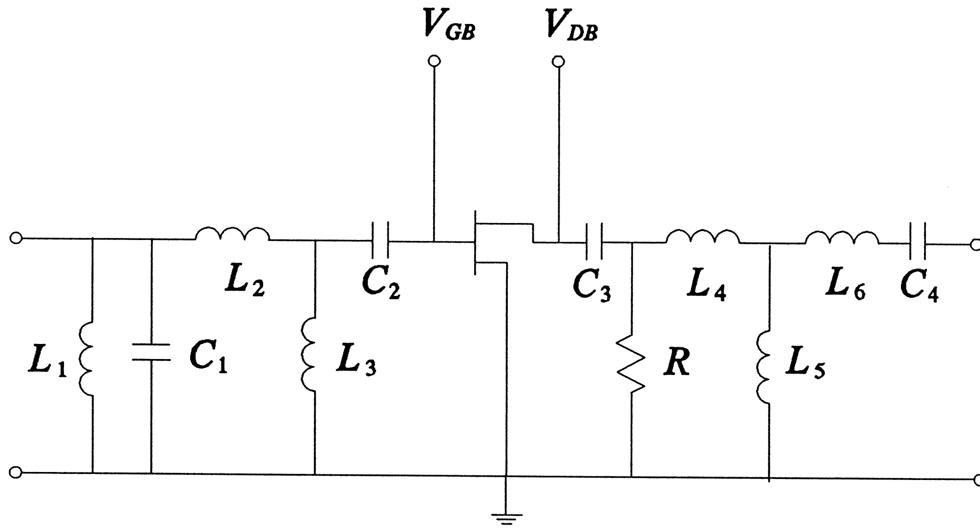
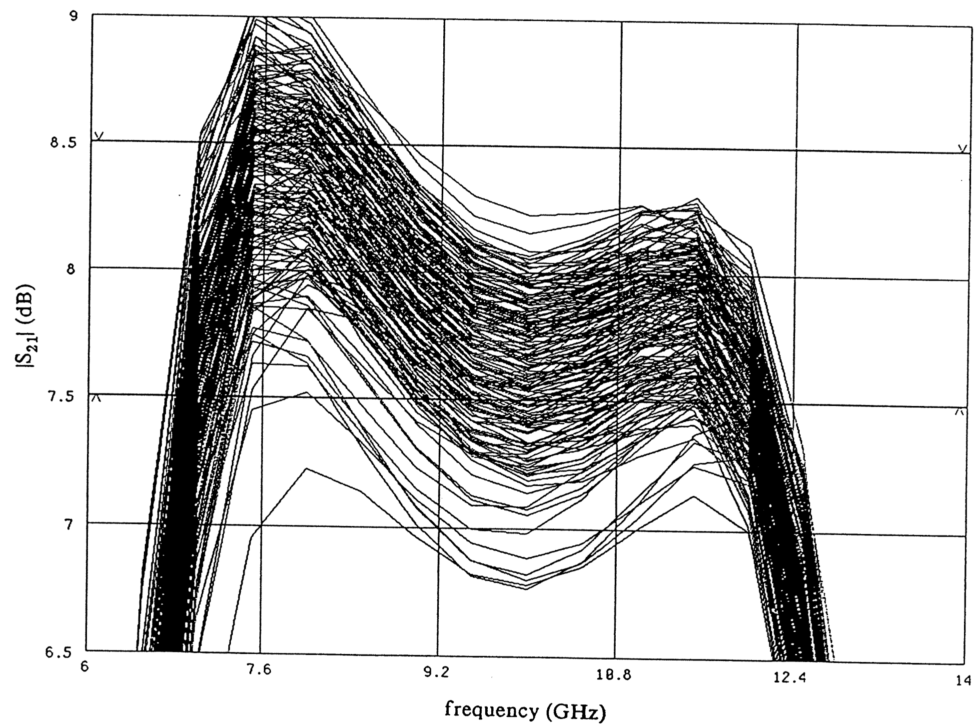
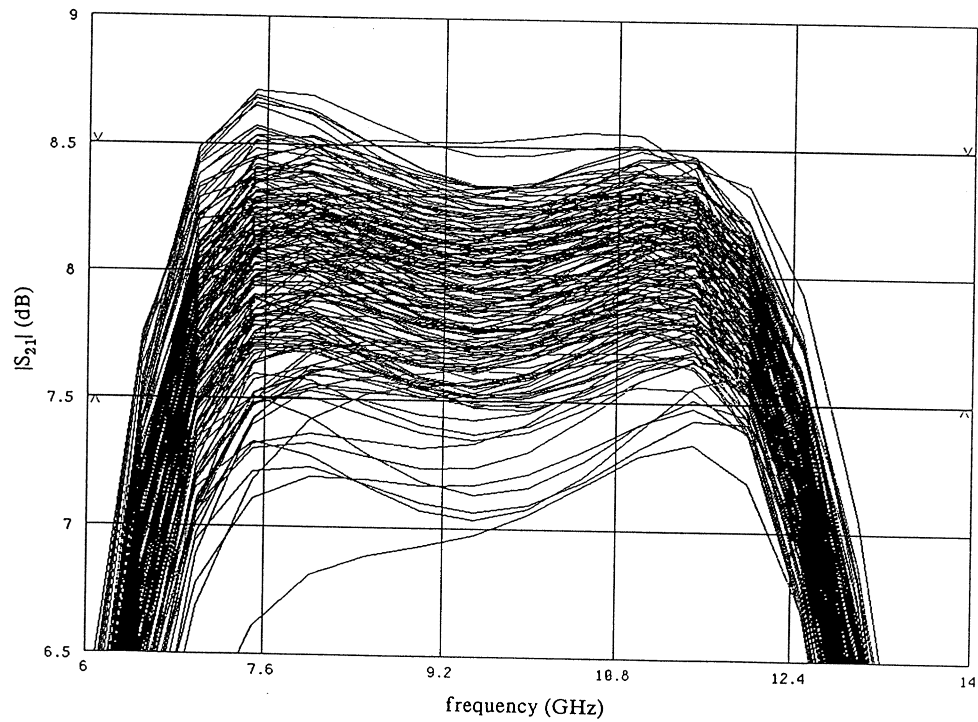


Fig. 1. Circuit diagram of the small–signal broadband amplifier.

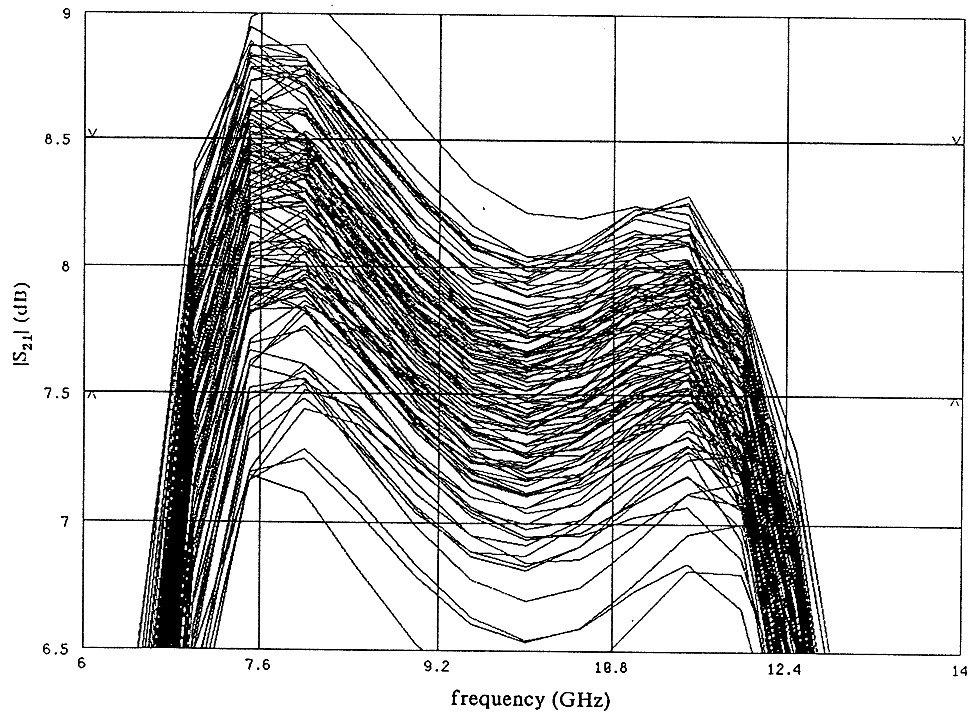


(a)

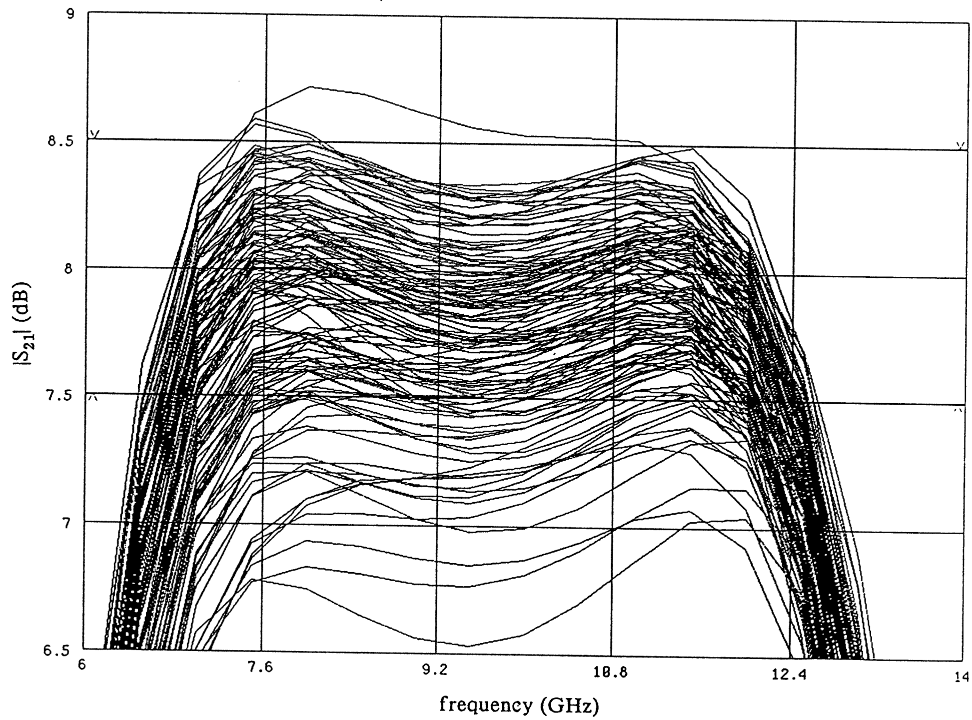


(b)

Fig. 2. Monte Carlo sweep of $|S_{21}|$ using PhorsFET, (a) before yield optimization and (b) after yield optimization.



(a)



(b)

Fig. 3. Monte Carlo sweep of $|S_{21}|$ using device data with the same matching circuits as for Fig. 2, (a) before yield optimization and (b) after yield optimization.

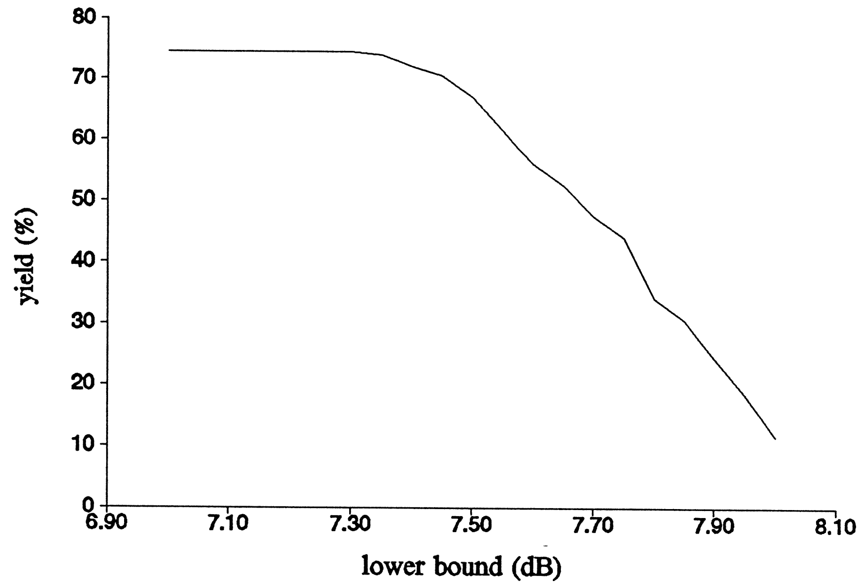


Fig. 4. Yield versus the lower bound of the design specification on the gain.

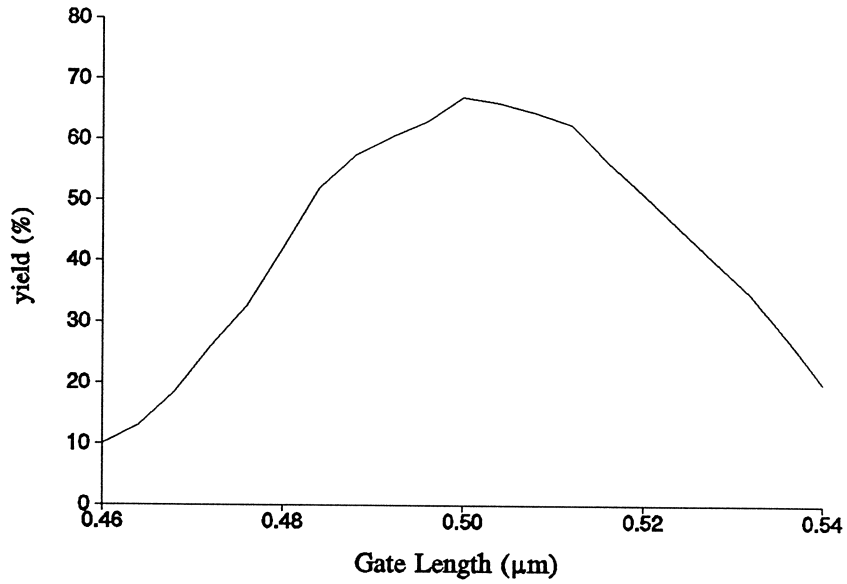


Fig. 5. Yield versus the FET gate length.

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