YIELD DRIVEN OPTIMIZATION
OF INTEGRATED CIRCUITS

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ABSTRACT

We review the concept of yield driven optimization of integrated circuits such as (monolithic) microwave integrated circuits, (M)MICs. Statistical variations of circuit parameters are taken into account at the design stage in order to maximize yield. We stress the importance of dealing with basic physical/process/geometrical parameters. We also present a novel and powerful approach to CAD software architecture suitable for distributed calculations and interactions between independent programs. This approach is particularly useful for independent software development and for maintenance of large software systems such as those dedicated to integrated circuit design and yield optimization.

INTRODUCTION

Yield optimization has been recognized as an indispensable design tool for modern CAD of integrated circuits [1-3]. Manufactured circuits are spread over a region determined by nominal design and statistical distribution of parameters. Statistical variations originate in process fluctuations or can be attributed to model uncertainties. A number of algorithms for yield driven optimization have been proposed in the last fifteen years (e.g., see [1-3]). Here we briefly review the approach employing the one-sided ℓ_1 optimization technique proposed by Bandler and Chen [3].

Yield driven optimization, especially of nonlinear circuits, is extremely computationally intensive: many circuits have to be simulated repeatedly and each circuit simulation involves CPU intensive iterations to solve nonlinear equations. Efficiency of the algorithms as well as organization of software are of utmost importance. Software modularity must be facilitated and modules of different origin need to be accommodated. To this end we discuss some of our new developments in design of open architecture software systems.

YIELD OPTIMIZATION

Due to various fluctuations inherent in the manufacturing process, the circuit outcomes exhibit variations of their responses w.r.t the nominal design response. Manufacturing yield is simply the ratio of the number of circuit outcomes meeting all design specifications to the total number of outcomes. Formally, yield driven optimization is formulated as

$$\underset{\phi^0}{\text{maximize}} \ \{ \ Y(\phi^0) = \int_{\Re^n} I_a(\phi) f_\phi(\phi^0, \phi) d\phi \ \}, \tag{1}$$

where $\phi^0 \in \Re^n$ is the vector of nominal circuit parameters, ϕ is the vector of actual circuit outcome parameters, $f_\phi(\phi^0, \phi)$ is the probability density function

(pdf) of ϕ around ϕ^0, $I_a(\phi) = 1$ if $\phi \in A$, the acceptability region in the ϕ space where all design specifications are satisfied, and $I_a(\phi) = 0$, otherwise.

There are two main difficulties in evaluating yield $Y(\phi^0)$ in (1). First, an infinite number of outcomes is involved since ϕ is a continuous random variable. To overcome this difficulty a number of Monte Carlo outcomes, ϕ^i, $i = 1,2,\ldots,K$, is sampled around ϕ^0 according to $f_\phi(\phi^0,\phi)$. Then, yield can be estimated by

$$Y(\phi^0) \simeq (\sum_{i=1}^{K} I_a(\phi^i)) \Big/ K. \qquad (2)$$

Secondly, the actual joint pdf $f_\phi(\phi^0,\phi)$ is difficult or even impossible to estimate. The problem of determining this pdf is a subject of statistical modeling and will be briefly discussed in the next section.

The one-sided ℓ_1 objective function for yield driven optimization [3] is formulated as follows. For each of K circuit outcomes ϕ^i the corresponding error vector $e(\phi^i) = [e_1(\phi^i) \; e_2(\phi^i) \; \ldots \; e_M(\phi^i)]^T$ is determined as

$$e_j(\phi^i) = R_j(\phi^i) - S_{uj} \qquad \text{or} \qquad e_j(\phi^i) = S_{\ell j} - R_j(\phi^i), \qquad (3)$$

where $R_j(\phi^i)$ is the jth response of the ith circuit outcome and S_{uj} or $S_{\ell j}$ is the jth (upper or lower, respectively) design specification. Then the generalized ℓ_1 function [4] $v(\phi^i)$ is calculated, which has the property that it is positive if at least one specification is violated, i.e., $\phi^i \notin A$, and it is negative if all design specifications are satisfied. The final one-sided ℓ_1 objective function is defined from $v(\phi^i)$ as

$$u(\phi^0) = \sum_{i \in J} \alpha_i v(\phi^i), \qquad (4)$$

where $J = \{ i \mid v(\phi^i) > 0, i=1,2,\ldots,K \}$ and α_i are properly chosen non-zero multipliers. The function (4) naturally imitates the percentage of outcomes violating design specifications and, therefore, its minimization leads to yield improvement.

Finally, it is worth mentioning that there exist efficient, gradient based algorithms, for example [5], suitable for solving (4). The problem of gradient evaluation, or approximation, is outside the scope of this short version of the paper, but will be addressed during paper presentation [6].

STATISTICAL MODELING

The purpose of statistical modeling is to determine or approximate the probability density function $f_\phi(\phi^0,\phi)$ in (1) from a sample of measurement data. Circuit simulation can be performed at different levels of primary parameters depending on available software tools or desired efficiency, e.g., timing analysis, cell or device simulations. Therefore, the vector ϕ^0 of designable parameters in (1) as well as the pdf must be considered at the same level as available or desired simulation.

Conventionally, the equivalent circuit parameters have been considered as adequate for design optimization. Consequently, attempts have been made

to perform statistical modeling at that level [7,8]. Unfortunately, it has been noticed that parameters at the equivalent circuit level exhibit somewhat unpredictable correlations and, quite frequently, distributions substantially different from Gaussian. This is because such parameters are complicated functions of certain physical and process parameters to which the original statistical variations, typically Gaussian, apply.

We have recently studied [9] statistical modeling of GaAs MESFETs at the equivalent circuit level as well as in terms of physical parameters. The parameters were extracted from GaAs MESFET wafer measurements provided by Plessey Research Caswell. The measurements consisted of DC bias data and multi-bias S parameters from a sample of GaAs MESFET devices. The parameter extraction and statistical postprocessing were automated by the statistical modeling features of HarPE™ [10]. Our results show that modeling at the physical parameter level can provide a much better estimate of the statistical spread of the measurements.

OPEN ARCHITECTURE OPTIMIZATION SOFTWARE SYSTEMS

We will now present a recent, advanced technique for open software architecture called IPPC (inter-program pipe communication) facilitating high speed numerical interaction between independent programs. It allows highly repetitive data communication between totally independent programs. It also allows an unlimited number of non-predetermined and new software modules to be added to existing software systems with no modification, no re-compilation and no re-linking of the existing systems. Therefore, a software user can add new modules to an existing IPPC-based system, allowing the existing system's optimizers, statistical drivers, etc., to interact iteratively with his own modules. The user's modules are separate executables programs. Thus, independent development, testing and execution of new code are facilitated. The confidentiality of the user's program is also totally secured.
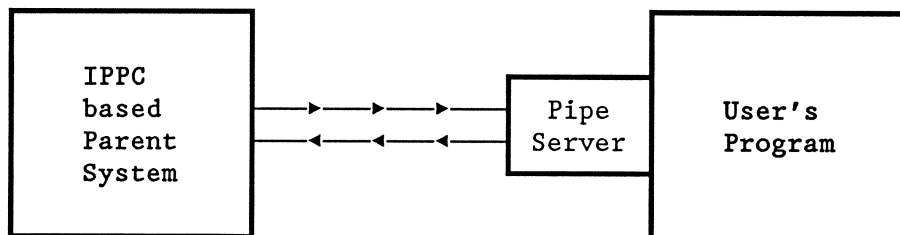

Fig. 1. Schematic diagram of IPPC between two independent programs

The communication, in its basic form, allows the user to combine two application programs: the parent and the child. It requires only minor modification to the child program and no modification to the IPPC-based parent program. A small IPPC server is the vehicle for communication between the two programs. As shown in Fig. 1, the user attaches the IPPC server to his or her program to generate a pipe-ready version. During simulation or optimization involving the child, the parent executes the child as a separate process. In

forking the child process, two inter-process pipes are created. The two-way communication is established by using each pipe to transfer data one-way. Communication between one parent and several children and grandchildren is possible. Experiments have been conducted on our new CAD system OSA90™ [11]. The overhead CPU cost in practical situations is found to be negligible - it typically adds only about 1% to the conventional approach of subroutine calls.

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