SIMULATION OPTIMIZATION SYSTEMS
Research Laboratory

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DC/SMALL-SIGNAL/LARGE-SIGNAL CIRCUIT DESIGN

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Abstract

We unify DC, small-signal and large-signal circuit design concepts and techniques. Circuits are optimized to simultaneously meet DC/small-signal/large-signal specifications. Unified FET model parameter extraction provides consistent bias dependent device models suitable for both small- and large-signal simulations. In a FET broadband amplifier design example the dynamic operating range is extended. Optimization of bias circuits is illustrated.

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SUMMARY

Introduction

It is traditional in microwave circuit design to focus upon a small-signal equivalent circuit after a separate DC analysis is performed to determine an operating point. Optimization is then limited to the parameters of the linearized circuit.

The harmonic balance (HB) technique offers efficient simulation of nonlinear circuits operating under large-signal steady state conditions [1,2]. Logically, it should be possible to design a nonlinear circuit which meets specifications for both small- and large-signal operation. Available CAD software, however, separates small-signal from large-signal circuit design, making optimum, consistent results tedious to attain.

This paper verifies and exploits the analytical relationship between small-signal analysis and HB analysis for sufficiently small input signals (HBSS). The circuit design problem is proved to converge to a single unified optimization problem, which, we believe, must be a distinctive feature of the next generation of microwave CAD software. Consistent device models can then be used and other factors affecting the behaviour of circuits such as bias, temperature, etc., can be simultaneously taken into account during optimization.

Examples demonstrate that consistent results can be reached which meet design specifications both for large and small signals. Our approach offers superior results w.r.t. those obtained by considering small- and large-signal operations independently from each other.

Consistency of DC/Small-Signal/Large-Signal Analysis

We use the same notation as in [1]. Boldface letters are used to indicate vectors or matrices, and superscript T denotes transposition.

Assume that the HB equation for a nonlinear circuit is

$$F(V) = I(V) + j\Omega Q(V) + YV + I_s = 0 \ , \tag{1}$$

where $V = [V^T(0) \ \ V^T(1) \ ... \ V^T(H)]^T$ is the variable vector to be solved for, usually the node voltages at the nodes connecting the linear and nonlinear parts of the circuit, H is the number of harmonics considered in the simulation, I(V) represents the current of nonlinear resistive elements and voltage controlled nonlinear current sources in the circuit, Q(V) the charges of nonlinear capacitors, $\Omega = \text{diag}\{\Omega(0), \Omega(1), ..., \Omega(H)\}$ with $\Omega(k) = \text{diag}\{\omega_k, \omega_k, ..., \omega_k\}$, Y is the admittance matrix describing the linear part of the circuit, and I_s contains the equivalent current excitation sources.

Using Fourier series, we have

$$v(t) = \sum_{\ell=-H}^{H} V(\ell) e^{j\ell\omega_0 t}.$$

The time invariant and variant parts can be briefly expressed as

$$v(t) = V(0) + \Delta v(t) \ . \tag{2}$$

Let the current of nonlinear resistive elements and voltage controlled nonlinear current sources in the time domain be i(v(t)). The corresponding frequency domain expression is

$$I(V,k) = \frac{1}{T_0} \int_0^{T_0} i(v(t)) e^{-jk\omega_0 t} dt \ . \tag{3}$$

Under small-signal operation, i.e., $\Delta v(t) \approx 0$, we have

$$\frac{\partial i^T(v(t))}{\partial v(t)} \approx \left. \frac{\partial i^T(v(t))}{\partial v(t)} \right|_{V(0)} = \text{constant.}$$

It can be shown that

$$\frac{\partial I^T(V,k)}{\partial V(m)} = \frac{1}{T_0} \int_0^{T_0} \frac{\partial i^T(v(t))}{\partial v(t)} \ e^{jm\omega_0 t} \ e^{-jk\omega_0 t} \ dt$$

$$\approx \begin{cases} \left.\dfrac{\partial i^T(v(t))}{\partial v(t)}\right|_{V(0)} & k=m,\ k,m = 0,1,\ ...,\ H \\ 0 & k\neq m,\ k,m = 0,1,\ ...,\ H \end{cases}$$

Similar derivations can be applied to Q(V). Therefore, under small-signal conditions, the Jacobian matrix of (1) tends to be block diagonal. From the Newton iteration method, it is not difficult to derive that (1) can be solved by first solving the nonlinear equation

$$F(V(0)) = I(V(0)) + Y(0)V(0) + I_s(0) = 0 \tag{4}$$

and then a set of linear equations

$$\left(\left[\frac{\partial I^T(V,k)}{\partial V(k)}\right]_{V(0)}^{T} + j\Omega(k) \left[\frac{\partial Q^T(V,k)}{\partial V(k)}\right]_{V(0)}^{T} + Y(k) \right) V(k) + I_s(k) = 0 \qquad k=1,...,H, \tag{5}$$

where V(0) is the solution of (4).

Equations (4) and (5) verify that DC/small-signal circuit analysis is a special case of HB analysis. This leads to a specialized HB technique for small-signal analysis which we call HBSS. It should be emphasized, however, that while there exist techniques for DC/small-signal simulation that do not require explicit AC excitations, an AC excitation is indispensable to HBSS simulation.

The numerical verification of our derivation is illustrated in Fig. 1, where a single FET circuit, shown in Fig. 2, is simulated by DC/small-signal analysis and by HB analysis, respectively. The Curtice nonlinear FET model [3] is employed. The result in Fig. 1 shows that when the input signal is sufficiently small HB is almost the same as DC/small-signal analysis, except when the input signal is too small, in which case numerical errors become dominant.

Seamless DC/Small-Signal/Large-Signal Circuit Design and Optimization

Using the consistency between DC/small-signal/large-signal analysis, general circuit design can be formulated into one optimization problem with error functions expressed as

$$e(\phi) = \begin{bmatrix} e_{dc}(\phi) \\ e_{ss}(\phi) \\ e_{ls}(\phi) \end{bmatrix}, \tag{6}$$

where $e_{dc}/e_{ss}/e_{ls}$ stand for error functions in the DC/small-signal/large-signal domain, ϕ represents circuit optimization variables common to DC/small-signal/large-signal circuits. Because of our unification, ϕ can include not only usual variables such as resistors, capacitors, FET parameters, and so on, but also other parameters such as bias voltages.

CAD systems, such as Libra [4] and Microwave Harmonica [5], have adopted simulation with uncoupled DC, small-signal and large-signal analyses. For combined specifications, manual manipulations have to be involved.

Examples

Both parameter extraction and design optimization examples are presented employing the McCAE research system running on an Apollo workstation.

Example 1 We extract FET model parameters by simultaneously matching DC, small-signal and large-signal measurements [6,7]. The circuit diagram is shown in Fig. 2 with the Curtice nonlinear FET model. Totally, 27 variables are considered, including all parameters in the intrinsic FET model and all elements in the extrinsic circuits.

Measurement sets used are listed in Table I. Corresponding to (6), e_{dc} represents the 2 errors between measured and modeled DC drain bias currents, e_{ss} the 128 errors between measured and modeled S-parameters, and e_{ls} the 48 errors between measured and modeled harmonic output powers. Then we have 178 error

functions. Least-squares optimization is applied to simultaneously minimize all error functions. From the same initial guess of parameter values two parameter extractions were performed by matching (1) large-signal measurements only, and (2) DC, small-signal and large-signal measurements simultaneously.

Fig. 3 illustrates the match in large-signal responses at solutions reached by the two different approaches. A bias-fundamental frequency point not used in the optimization is selected to illustrate the model prediction. Both give reasonably good matches. However, as shown in Fig. 4, the small-signal S-parameter matches reached by the two approaches are quite different. Very good agreement is observed at the solution obtained by simultaneous DC/small-signal/large-signal optimization, yielding considerable improvement over the results by matching large-signal data alone.

Example 2 We design a small-signal broadband amplifier [8]. The circuit diagram is shown in Fig. 5, where the FET model is taken from the result of Example 1. We assume the specifications for the amplifier to be

$$\begin{aligned} \text{GAIN} &= 8 \pm 0.5\text{dB} \\ |S_{11}| &\le 0.4 \\ |S_{22}| &\le 0.4 \\ |S_{12}| &\le 0.15 \end{aligned}$$

at frequencies 4, 5, 6, 7 and 8GHz. The design variables are 11 element parameters in the matching network and 2 resistor values in the bias network. Minimax optimization [9] is used.

First, we design the amplifier by the conventional small-signal approach at a predetermined bias point selected approximately in the middle of the FET DC I-V curve. All the specifications can be met at the optimal solution under small-signal conditions. Then, we exploit our new design strategy to include the dynamic

range of the amplifier in addition to the small-signal specifications. Specifically, we add specifications to extend the gain of the amplifier at input available power levels -10, -5 and 0dBm, and enforce second and third harmonic output power levels to be at least 40dB below the fundamental output power level. All small- and large-signal specifications result in 85 error functions. We also allow the bias circuits to be optimized. All small-signal/large-signal specifications are met at the solution.

Figs. 6 and 7 show the results. In Fig. 6, the gain response surfaces are depicted over fundamental frequency 2 to 10GHz and input available power -35 to 5dBm. It can be seen that the gain surface in Fig. 6(b) is flatter and provides a wider area which meets the gain specification.

Fig. 7 depicts the second harmonic error surface over the same range. Any excursion above the flat part of the surface means that the second harmonic output power is less than 40dB below the fundamental output power. From Fig. 7(a), we can see that the error becomes nonzero when the input power becomes higher than -10dBm, while in Fig. 7(b) the zero error area extends to 0dBm input power, the area where we have imposed additional specifications.

Conclusions

We present a unified theory to simultaneously optimize DC, small-signal and large-signal performance. Our approach enjoys the following distinctions.

(1) The inherent consistency of small- and large-signal analyses and unified optimization guarantees designs which simultaneously meet DC/small-signal/large-signal specifications.

(2) A much wider range of design variable selections is permitted. Besides linear elements, design variables can include nonlinear elements, controllable operating parameters, such as bias, and possibly process parameters. Therefore, the nonlinearity of the circuit at different levels can be

effectively exploited.

(3) Design specifications can be expanded from the traditional frequency dimension into a multidimensional space [10]. For example, specifications can be imposed at different input power levels in a small-signal circuit design to increase the dynamic operating range.

(4) For parameter extraction, the DC, small-signal and large-signal data are explicitly traded off resulting in a model suitable for both small-signal and large-signal applications.

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TABLE I

MEASUREMENT SETS USED FOR PARAMETER EXTRACTION IN EXAMPLE 1

DC measurements	
Response type	drain current
Bias conditions	V_{GB}=-0.361V V_{DB}=2V V_{GB}=-1.062V V_{DB}=6V
Small-signal measurements	
Response types	magnitudes and phases of 4 S-parameters
Bias conditions	V_{GB}=-0.361V V_{DB}=2V V_{GB}=-1.062V V_{DB}=6V
Frequencies (GHz)	1, 3, 5, 7, 9, 11, 13, 15
Large-signal measurements	
Response types	DC drain current, output powers at the fundamental, second and third harmonics
Bias conditions	V_{GB}=-0.373V V_{DB}=2V V_{GB}=-1.072V V_{DB}=6V
Input power (dBm)	-15, -5, 5
Fundamental frequencies (GHz)	0.2, 6

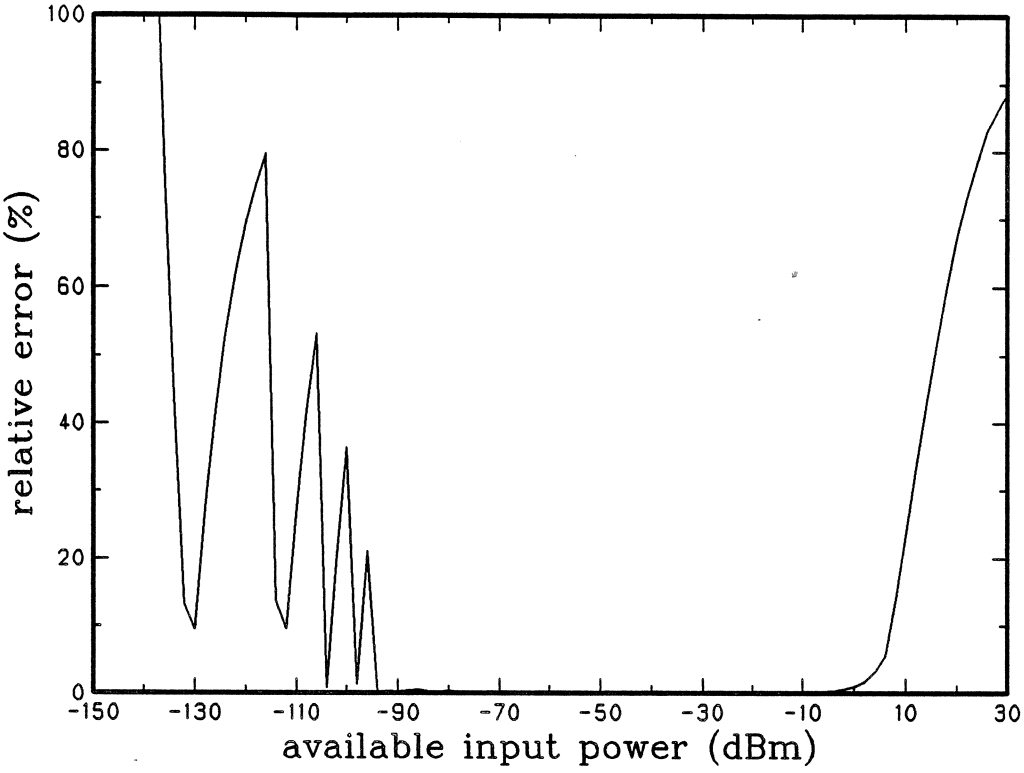


Fig. 1. Relative errors between the voltage gain calculated by HB and $|S_{21}|$ by small-signal analysis with respect to different available input power levels.

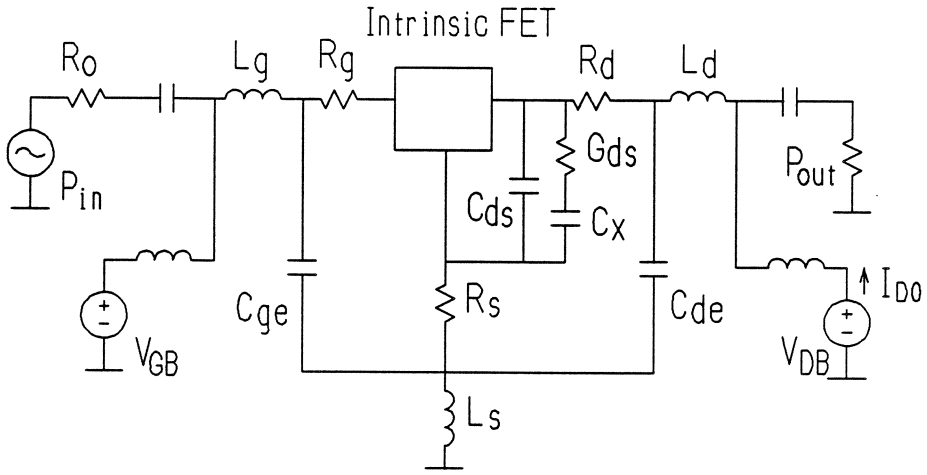


Fig. 2. Single FET circuit with the Curtice nonlinear intrinsic FET model.

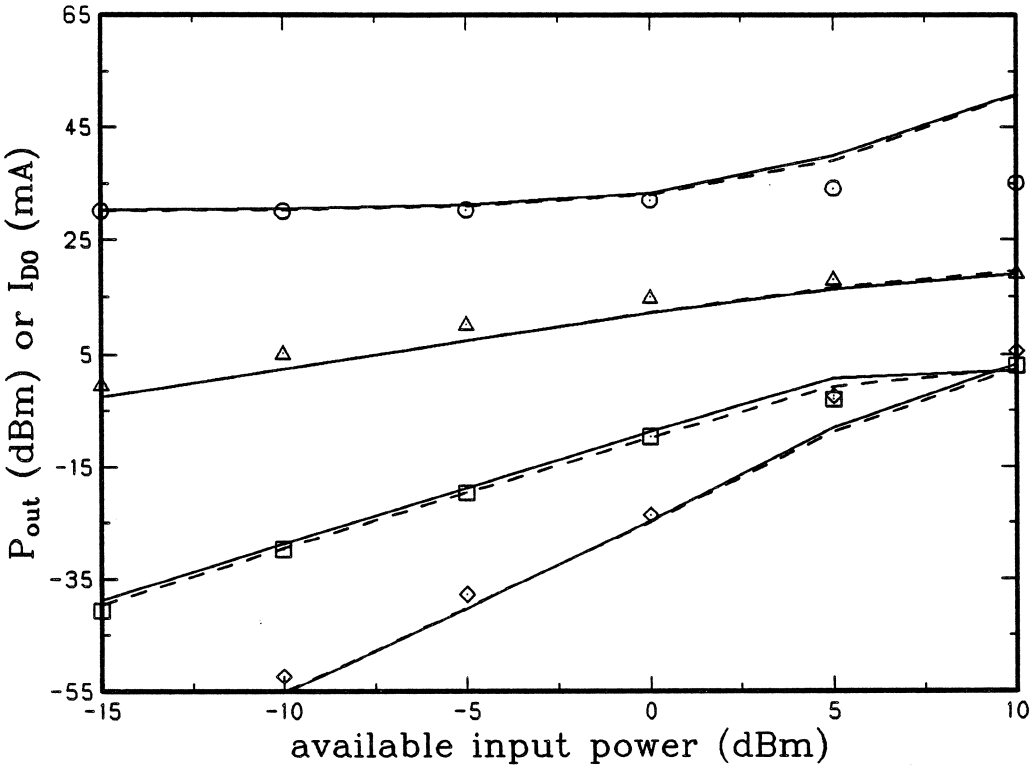
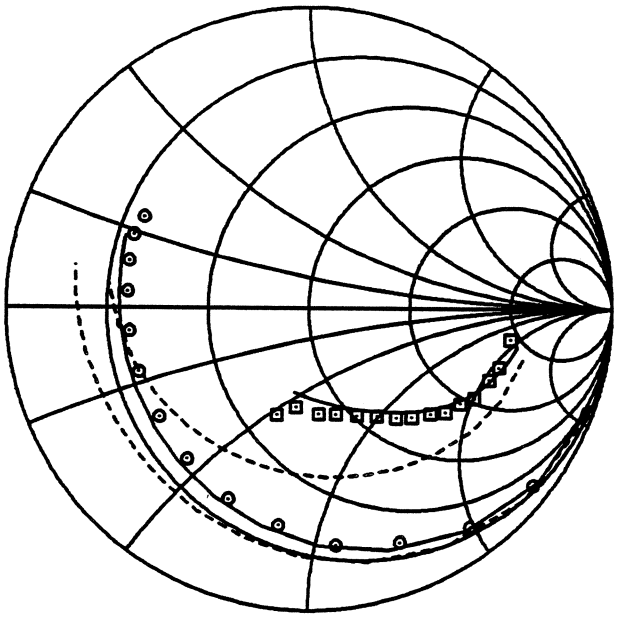
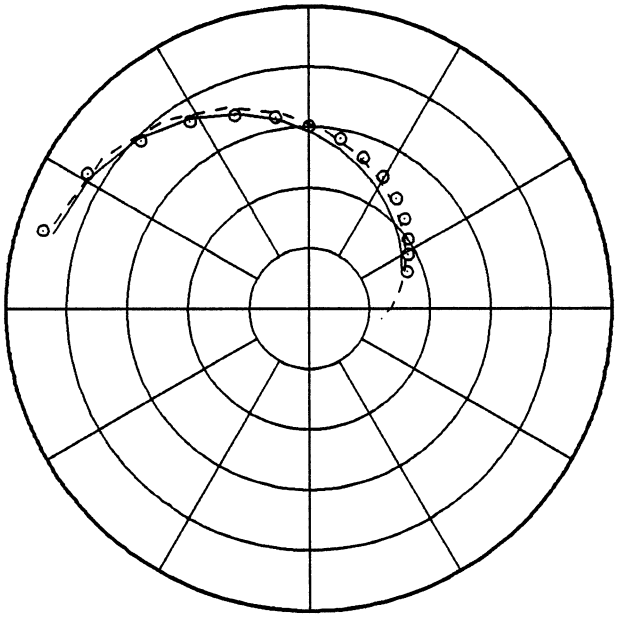


Fig. 3. Agreement between model responses and large-signal measurements at fundamental frequency 2GHz and bias V_{GB}=-0.667V and V_{DB}=4V. Solid lines represent responses of the model extracted from both small- and large-signal matching. Dashed lines represent responses of the model extracted only from large-signal fitting. Circles, triangles, squares, and diamonds stand for DC, fundamental, second, and third harmonic measurements, respectively.



(a)



(b)

Fig. 4. Agreement between model responses and S-parameter measurements at bias V_{GB}=-0.667V and V_{DB}=4V. Solid lines represent responses of the model determined from both small- and large-signal matching. Dashed lines represent responses of the model determined only from large signal fitting. (a) S_{11} and S_{22} fitting, where circles and squares represent S_{11} and S_{22} measurements, respectively. (b) S_{21} fitting, where circles are from S_{21} data.

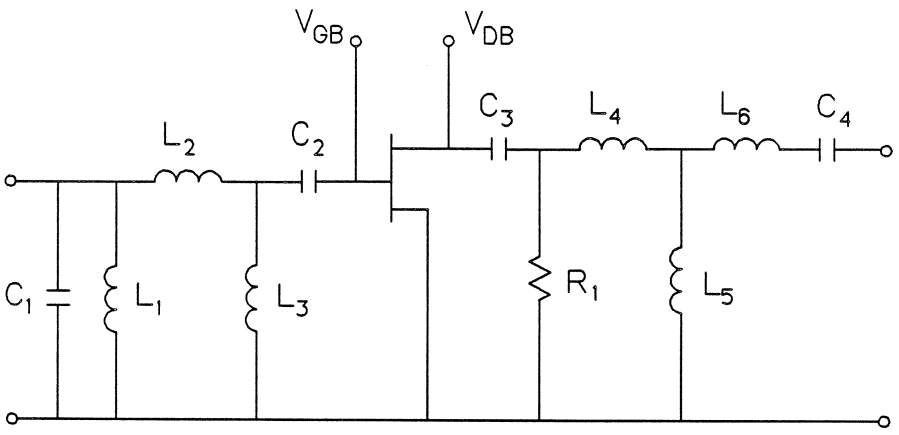
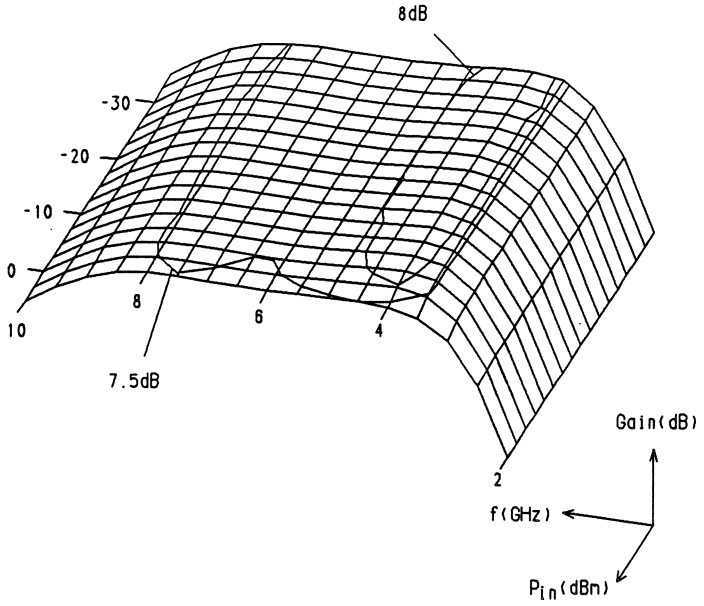
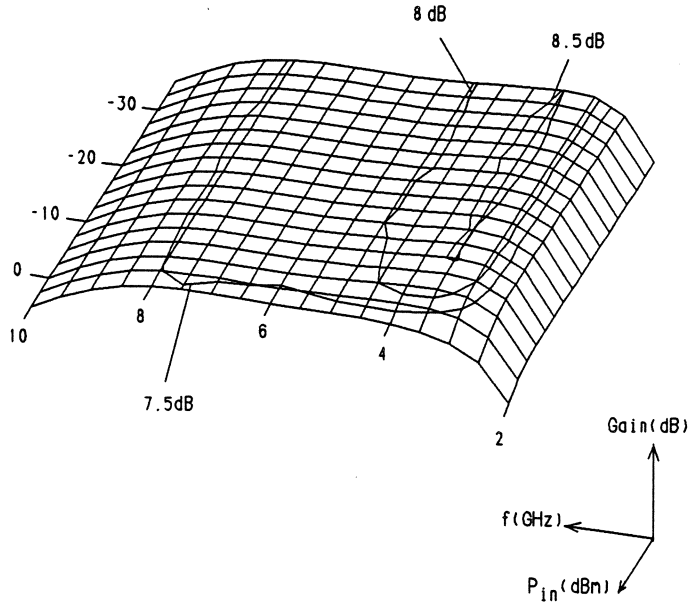


Fig. 5. 4-8GHz broadband small-signal amplifier.

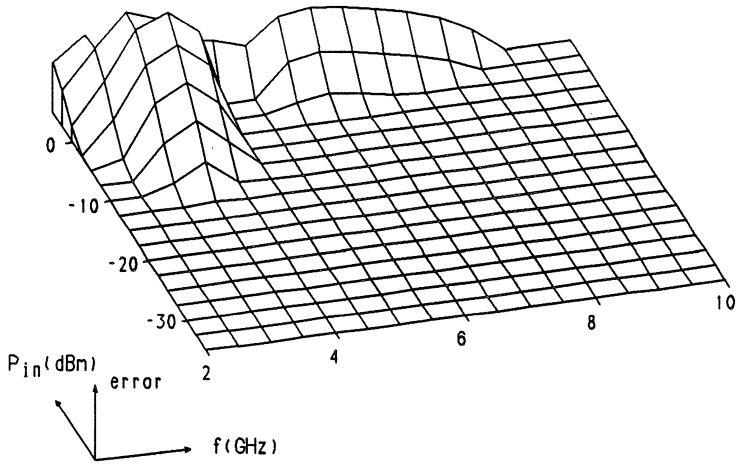


(a)

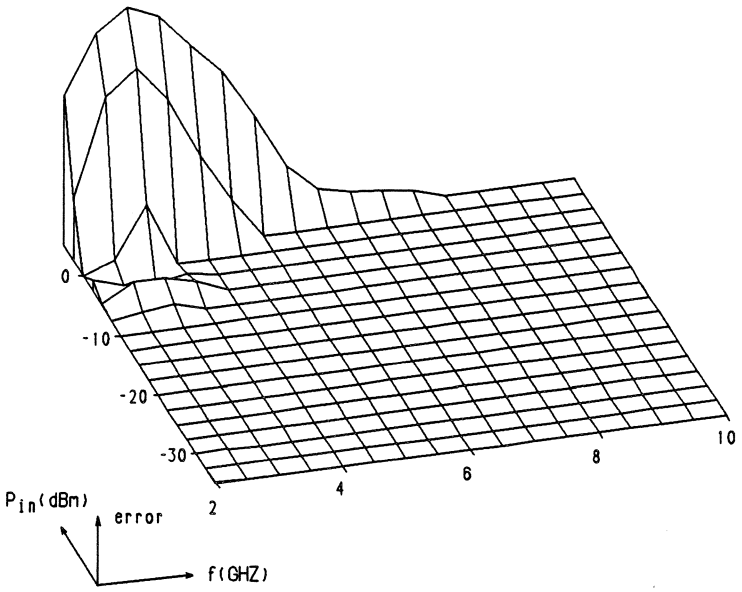


(b)

Fig. 6. (a) The gain response surface simulated at the solution obtained by small-signal design. (b) The gain response surface simulated at the solution obtained by simultaneous small- and large-signal design. Contours indicate the specification of 8±0.5dB.



(a)



(b)

Fig. 7. The error surfaces of the second harmonic output power with respect to the design specification. (a) Simulation at the solution obtained by conventional small-signal design. (b) Simulation at the solution by simultaneous small- and large-signal design. The specifications are from 4 to 8GHz on the fundamental frequency and from -10dBm to 0dBm on the input power. The flat part of the surface indicates zero error.