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ANALYSIS OF A CURRENT SWITCH EMITTER FOLLOWER
USING THE COMPANION NETWORK APPROACH

M.R.M. Rizk

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FACULTY OF ENGINEERING
McMASTER UNIVERSITY
HAMILTON, ONTARIO, CANADA



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ANALYSIS OF A CURRENT SWITCH EMITTER FOLLOWER
USING THE COMPANION NETWORK APPROACH

M.R.M. Rizk

Abstract

This report demonstrates, in a tutorial fashion, the transient analysis of a nonlinear circuit, namely a current switch emitter follower [1]. The response obtained was checked against other responses obtained by a program which uses the state space formulation for the analysis [2] and by SPICE2 [3].

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The author is with the Group on Simulation, Optimization and Control and Department of Electrical Engineering, McMaster University, Hamilton, Canada L8S 4L7.

I. INTRODUCTION

A transient analysis of a CSEF was performed using the companion network approach [4-6]. The report discusses briefly the companion networks which replace the original elements of a nonlinear circuit resulting in a linear resistive circuit which is repeatedly solved to obtain the transient response. The method implies two loops, the first is concerned with the convergence of the nonlinear algebraic equations which are linearized by the companion network, and the second is concerned with the discretization of the time derivatives. To start the analysis a D.C. (steady state) analysis is performed to supply the initial conditions for the transient analysis. The response obtained was verified by SPICE2 [3]. Some of the elements which could not be handled by SPICE2 were modeled by some additional circuits. The listings of the analysis subroutines and the input data to SPICE2 are given in Appendices A and B, respectively.

II. THE COMPANION NETWORK APPROACH

In the transient analysis of nonlinear circuits the equations describing the circuits are algebraic and differential equations. These equations are linearized and discretized according to the integration scheme used for solving these equations. In the companion network approach the linearization and discretization are performed at the branch (element) level. Each element can be represented by a combination of

- (1) resistors
- (2) independent current sources
- (3) voltage - controlled current sources.

Hence the resultant new circuit will be a linear resistive circuit.

Linearization

Consider the diode shown in Fig. 1.a, with the current i_d passing through it and v_d the voltage across its terminals. The current i_d is given by

$$i_d = I_S (e^{\theta v_d} - 1), \quad (1)$$

where

I_S is the saturation current

θ is the inverse of thermal potential.

Linearizing the nonlinear characteristic around a given point i_d^0 (taking the linear part only of the Taylor expansion) the current can be expressed as

$$i_d = i_d^0 + \left. \frac{\partial i_d}{\partial v_d} \right|_{v_d=v_d^0} (v - v^0). \quad (2)$$

In general, this expression is substituted in the circuit equations which will have to be solved iteratively. So (2) is written as

$$i_d^{m+1} = i_d^m + \left. \frac{\partial i_d}{\partial v_d} \right|_{v_d=v_d^m} (v_d^{m+1} - v_d^m) \quad (3)$$

where $m+1$ is the present iteration. Equation (3) can be represented or modeled by the companion network shown in Fig. 1.b.

Discretization

The differential equations will contain derivatives w.r.t. time which can be approximated in many different ways according to the integration algorithm used in solving the equations. In the Backward

Euler algorithm, for example, the derivative of a voltage can be approximated by

$$\left. \frac{dv}{dt} \right|_{t=t^{n+1}} = \frac{v^{n+1} - v^n}{T} \quad (4)$$

where $T = t^{n+1} - t^n$ is the time step of the integration, and n is the time iteration counter. Using this approximation the current passing through a linear capacitor

$$i_C = C \frac{dv}{dt}, \quad (5)$$

would be

$$i_C^{n+1} = C \frac{v_C^{n+1} - v_C^n}{T}. \quad (6)$$

This equation can be represented by a companion network as shown in Fig. 2.b. Using higher order, or any different, integration algorithm will result in a different companion network. For example if Gear's integration algorithm (a predictor corrector algorithm [6]) is used the capacitance current is expressed by [4]

$$i_C^{n+1,m+1} = \left(-\frac{C}{a_1 T} \right) v_C^{n+1,m+1} + \left[C \left(\frac{\partial v_C}{\partial t} \right)^{n+1,0} + \frac{C}{a_1 T} v_C^{n+1,0} \right] \quad (7)$$

where a_1 is a constant coefficient, and m is the corrector iteration counter. The linear capacitor will have the companion network shown in Fig. 2.c. For a nonlinear capacitance (Fig. 3.a) the companion network can be as the one shown in Fig. 3.b (Backward Euler).

III. ANALYSIS OF THE CSEF CIRCUIT

With the Companion Network Approach

The CSEF [1] shown in Fig. 4 was analyzed using the companion network approach. The transistor model was the one given in Fig. 5.a. The decoupled equivalent circuit of the lossless transmission line shown in Fig. 5.b was used in the analysis. The circuit parameters, the diode model, the transistor model and the transmission line parameters are given in Tables 1, 2, 3 and 4 respectively.

The circuit initially at equilibrium with input voltage $E_1 = -0.776V$ was analyzed to obtain the initial capacitance voltages. In this case (D.C. or steady state) all the capacitances were removed and the other elements were replaced by their companion networks. The resultant circuit is the one shown in Fig. 6. This linear resistive circuit was analyzed using its nodal equations shown in Fig. 7. This set of equations was solved by the CDC library subroutine GELG [7], where we start with all node voltages $\underline{v}^0 = 0$ and find \underline{v}^1 and so on, iteratively, until convergence is achieved. The values of \underline{v} obtained are the initial voltages of the transient analysis.

The circuit shown in Fig. 8 represents the CSEF after replacing the elements and the transistor models by the appropriate companion networks. The nodal admittance matrix of this circuit is given in Fig. 9. At each time step the set of equations is solved (starting with the voltages obtained from the previous time step, iteratively until convergence.

The analysis subroutines for the D.C. and transient cases are given in Appendix A. In the transient analysis a step T of 0.0025 nsec was

used and it took 40 sec to perform the analysis, while having T as 0.025 nsec it took 6 sec only and the results were indistinguishable.

The Analysis Using SPICE2

The general analysis program SPICE2 [3] was used to verify the responses obtained. In order to overcome the problem of handling the nonlinear capacitance in the form of the one given in the transistor model (Fig. 5.a) the current passing through the nonlinear part of the capacitance was represented by the current i_1 of a two dimensional current controlled current source. The currents controlling this source are i_2 and i_3 in two small additional networks as shown in Fig. 10. The coefficients of the polynomial representing i_1 are all zero except the coefficient of the cross terms has the value one. In the circuit where i_2 is passing $P_0 = P_1 I_S$ so as to let i_2 be equal to $P_1 I_S \exp(\theta V_{BE})$. The current i_3 will represent dV_{BE}/dt .

The analysis was also performed by SPICE2 using the built-in models. The parameters of these models were fed in the data to match the model as close as possible to the given model (Fig. 5.a). Responses obtained by the state equations [2], the companion network and by SPICE2 are shown in Fig. 11. Note that the two responses obtained by SPICE2 were almost identical.

The running time of SPICE2, where we modeled the nonlinear capacitance, was 92 sec, while using the built-in models the running time was only 7 sec. This difference is mainly due to the additional elements we have introduced in modeling the nonlinear capacitance which resulted in having 12 additional nodes and node voltages. The data supplied to SPICE2 in the two cases are given in Appendix B.

IV. ACKNOWLEDGEMENT

Thanks are due to Dr. J.W. Bandler for useful discussion, and to Dr. H.L. Abdel-Malek for checking the results with the state-space approach and to Dr. S. Chisholm for useful discussions concerning the use of SPICE2.

V. REFERENCES

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- [5] D.A. Calahan, Computer-Aided Network Design (Revised Edition). New York: McGraw Hill, 1972.
- [6] L.O. Chua and P.M. Lin, Computer-Aided Analysis of Electronic Circuits. Englewood Cliffs, NJ: Prentice-Hall, 1975.
- [7] Subroutine GELG, System/360 Scientific Subroutine Package, Version III, IBM Programmer's Manual Number 360A-CM-03x, p. 121.

TABLE 1
CIRCUIT PARAMETER VALUES

R_1	281.33 Ω
R_2	75.00 Ω
R_3	78.24 Ω
R_4	45.53 Ω
E_2	4.03 V
E_3	1.13 V
E_4	1.66 V
C_0	1.25 pF

TABLE 2
DIODE MODEL PARAMETERS

I_{SD}	diode saturation current	$0.6 \times 10^{-9} \text{ A}$
C_{JD}	depletion layer capacitance	0.12 pF
τ_{TD}	transit time	0.01 ns
θ	inverse of thermal potential	38.668 V^{-1}

$$I_D = I_{SD} (\exp(\theta V_D) - 1)$$

$$C_D = C_{JD} + \tau_{TD} \frac{dI_D}{dV_D}$$

TABLE 3
TRANSISTOR MODEL PARAMETERS

I_S	saturation current	$0.6 \times 10^{-9} \text{ A}$
α	common base current gain	0.99
R_B	base resistance	50.0Ω
C_C	collector junction capacitance	0.5 pF
C_{JE}	emitter junction depletion layer capacitance	0.12 pF
TT	base transit time	0.01 ns
θ	inverse of thermal potential	38.668 V^{-1}

$$I_E = I_S (\exp(\theta V_{BE}) - 1)$$

$$I_C = \alpha I_E$$

$$C_E = C_{JE} + TT \frac{dI_E}{dV_{BE}}$$

R_B and C_C are assumed zero for transistor T_3

TABLE 4
TRANSMISSION LINE PARAMETERS

Z_0	characteristic impedance	92.004Ω
τ	delay time	0.25 ns

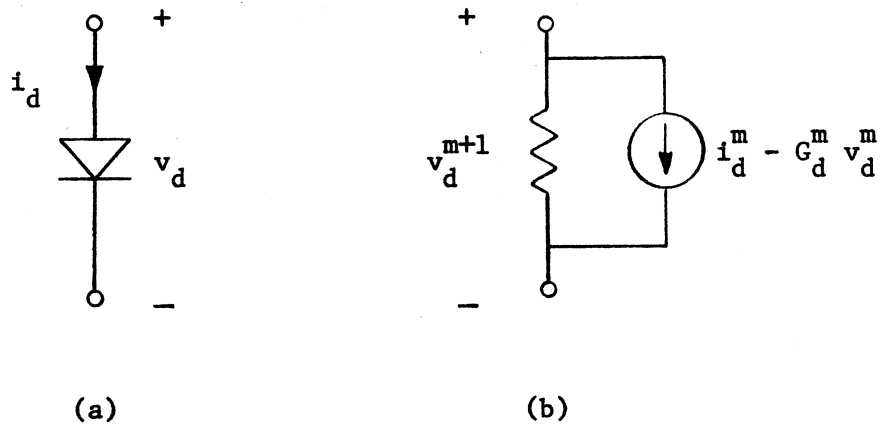


Fig. 1. a) A diode, b) its companion network.

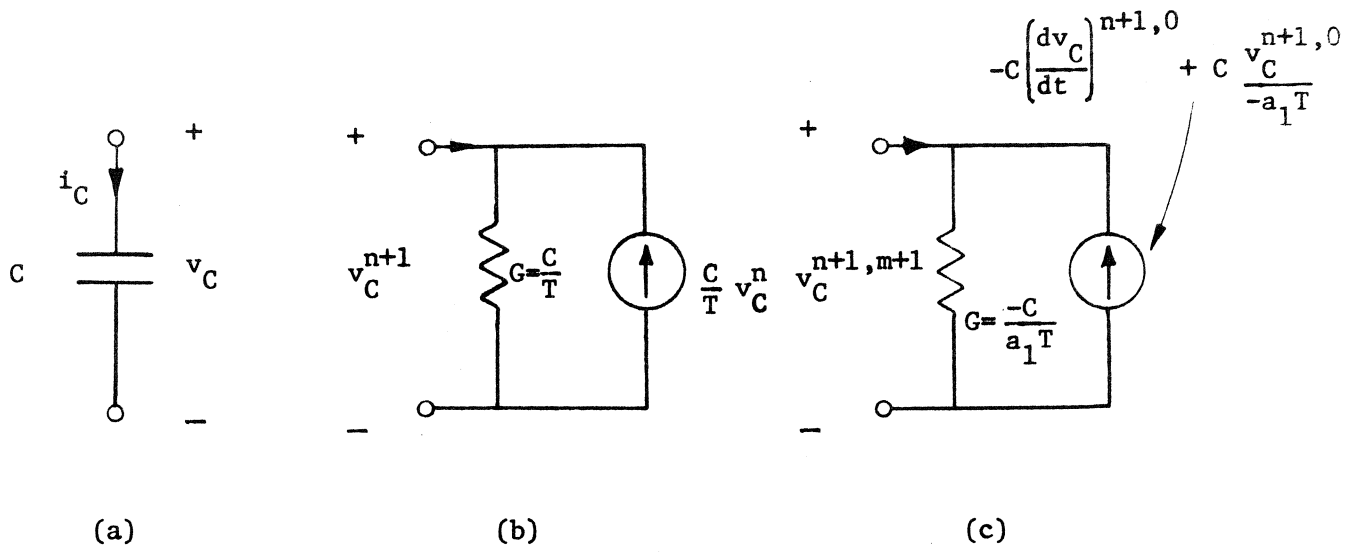


Fig. 2. a) A linear capacitor, b) its companion network using backward-Euler formula, c) its companion network using Gear's formula.

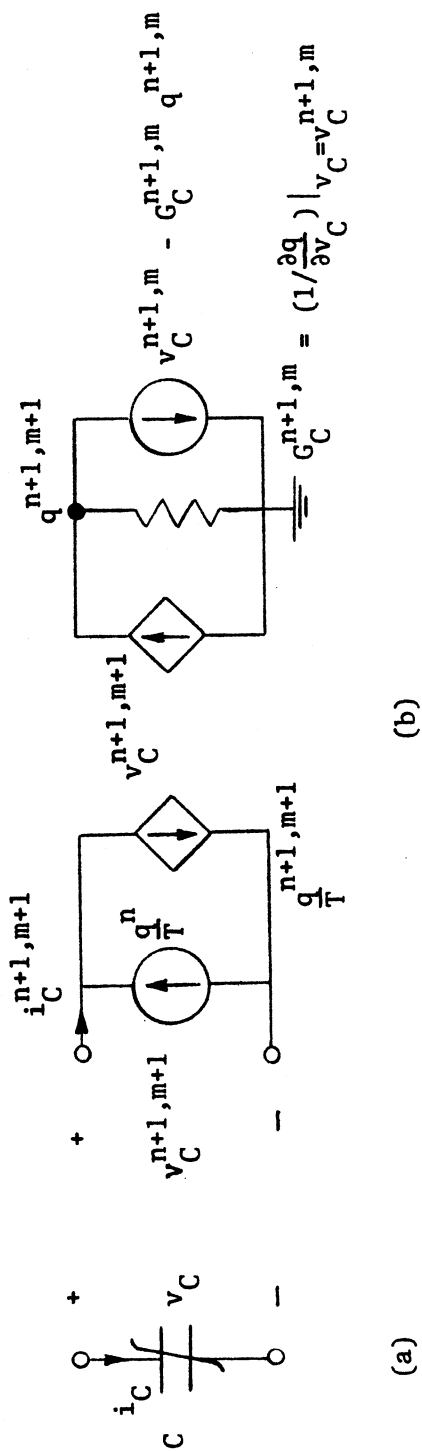


Fig. 3. a) A nonlinear capacitance, b) its companion network (note $q^{n+1,m+1}$ represents the node voltage).

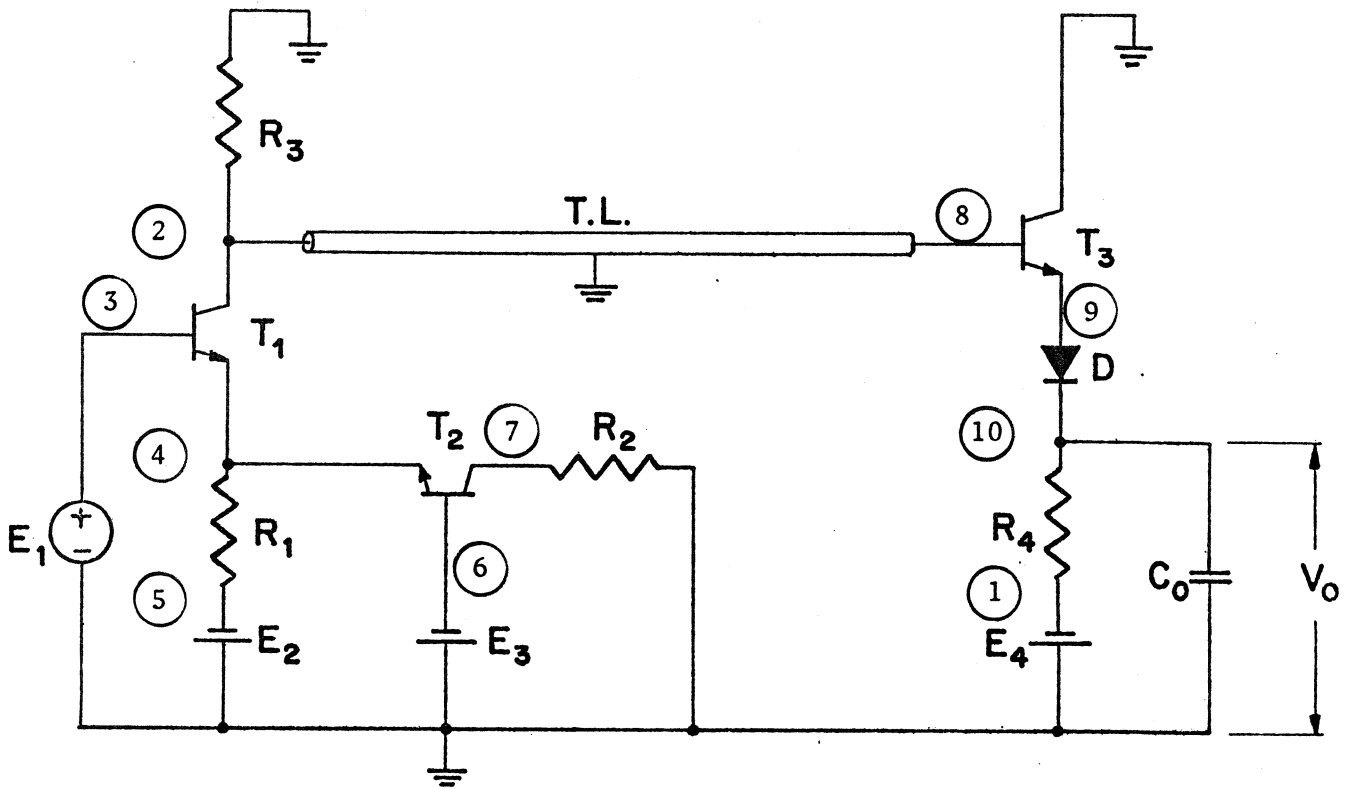


Fig. 4. The CSEF circuit [1].

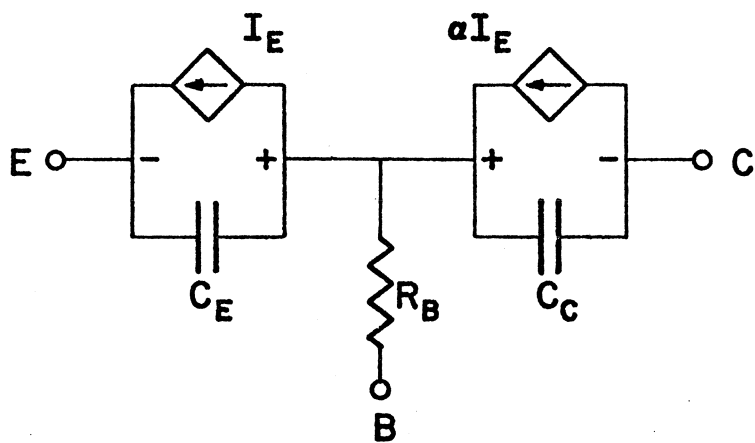
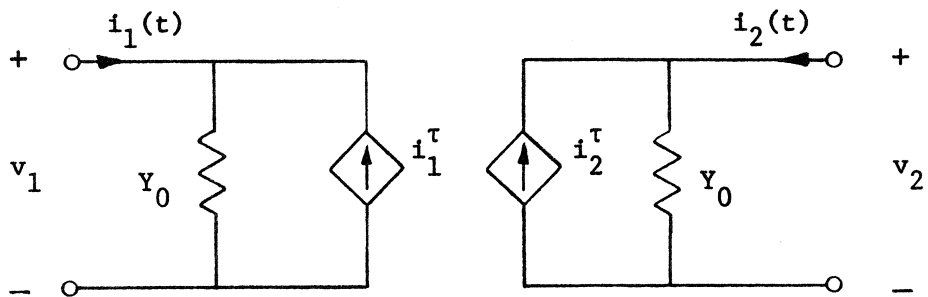


Fig. 5.a. The transistor model.



$$i_1^\tau = Y_0 v_1(t-\tau) + i_1(t-\tau)$$

$$i_2^\tau = Y_0 v_2(t-\tau) + i_2(t-\tau)$$

Fig. 5.b. The equivalent circuit of the transmission-line used in the nodal admittance analysis.

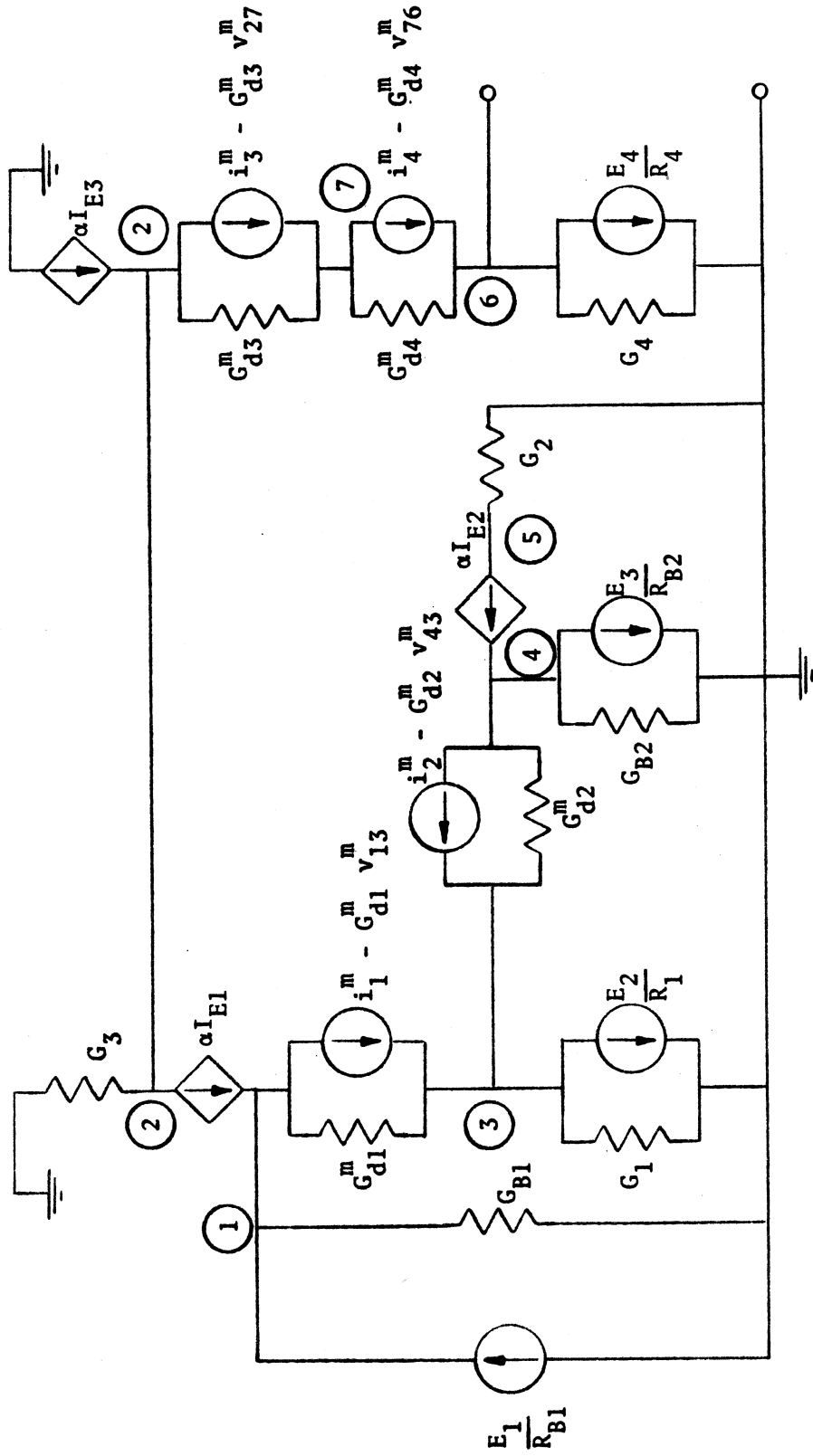


Fig. 6. The CSEF with the transistor and diode model elements (with capacitors removed) replaced by their companion networks for the D.C. analysis.

$$\begin{bmatrix} G_{B1} + (1-\alpha)G_{d1}^m \\ \alpha G_{d1}^m \\ -G_{d1}^m \end{bmatrix}
 \begin{bmatrix} (\alpha-1)G_{d1}^m \\ -\alpha G_{d1}^m \\ G_1 + G_{d1}^m + G_{d2}^m - G_{d2}^m \end{bmatrix}
 +
 \begin{bmatrix} (1-\alpha)G_{d3}^m \\ -\alpha G_{d3}^m \\ G_2 + (1-\alpha)G_{d2}^m \\ \alpha G_{d2}^m \\ G_2 \\ \alpha G_{d2}^m \\ -G_{d3}^m \end{bmatrix}
 \begin{bmatrix} v_1^{m+1} \\ v_2^{m+1} \\ v_3^{m+1} \\ v_4^{m+1} \\ v_5^{m+1} \\ v_6^{m+1} \\ v_7^{m+1} \end{bmatrix}
 =
 \begin{bmatrix} \frac{E_1}{R_{B1}} + (\alpha-1)(i_1^m - G_{d1}^m v_{13}^m) \\ -\alpha(i_1^m - G_{d1}^m v_{13}^m) + (\alpha-1)(i_3^m - G_{d3}^m v_{27}^m) \\ \frac{E_2}{R_1} + (i_1^m - G_{d1}^m v_{13}^m) + (i_2^m - G_{d2}^m v_{43}^m) \\ -\frac{E_3}{R_{B2}} + (\alpha-1)(i_2^m - G_{d2}^m v_{43}^m) \\ -\alpha(i_2^m - G_{d2}^m v_{43}^m) \\ \frac{E_4}{R_4} + (i_4^m - G_{d4}^m v_{76}^m) \\ -(i_4^m - G_{d4}^m v_{76}^m) + (i_3^m - G_{d3}^m v_{27}^m) \end{bmatrix}$$

Fig. 7. Nodal equations of the circuit shown in Fig. 6.

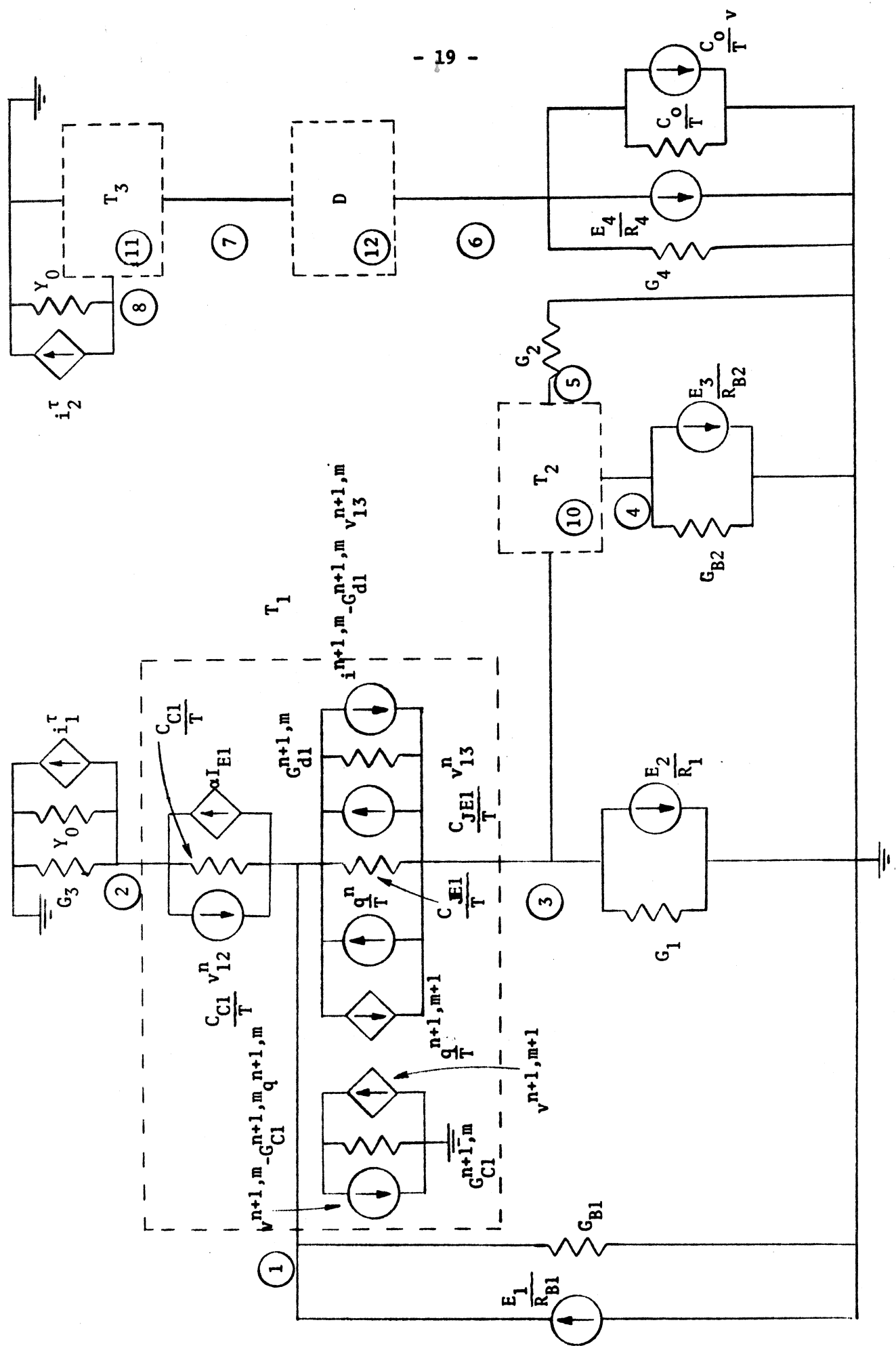


Fig. 8. The CSEF equivalent circuit. T₂ is exactly like T₁, T₃ is T₁ with C_C removed and D is T₁ without the collector junction.

$$\begin{array}{r}
 G_{E1} \frac{C_{JE1}}{T} + \frac{C_{C1}}{T} + (1-\alpha)G_{d1}^{n+1,m} - \frac{C_{JE1}}{T} + (\alpha-1)G_{d1}^{n+1,m} \\
 - \frac{C_{C1}}{T} + G_{d1}^{n+1,m} - \alpha G_{d1}^{n+1,m} \\
 G_3 + \frac{C_{C1}}{T} + Y_0 \\
 \frac{C_{JE1}}{T} + G_{d1}^{n+1,m} + \frac{C_{JE2}}{T} + G_{d2}^{n+1,m} \\
 G_1 + \frac{C_{JE1}}{T} + G_{d1}^{n+1,m} + \frac{C_{JE2}}{T} + G_{d2}^{n+1,m} \\
 - \frac{C_{JE1}}{T} + (\alpha-1)G_{d2}^{n+1,m} \\
 - \alpha G_{d2}^{n+1,m} \\
 G_{B2} + \frac{C_{C2}}{T} + \frac{C_{JE2}}{T} + (1-\alpha)G_{d2}^{n+1,m} - \frac{C_{C2}}{T} \\
 G_2 + \frac{C_{C2}}{T} \\
 G_4 + \frac{C_1}{T} + \frac{C_{JE4}}{T} + G_{d4}^{n+1,m} - \frac{C_{JE4}}{T} + G_{d4}^{n+1,m} \\
 - \frac{C_{JE4}}{T} + G_{d4}^{n+1,m} \\
 \frac{C_{JE3}}{T} + \frac{C_{JE4}}{T} + G_{d3}^{n+1,m} - \frac{C_{JE3}}{T} + G_{d3}^{n+1,m} \\
 + G_{d4}^{n+1,m} \\
 - \frac{C_{JE3}}{T} + (\alpha-1)G_{d3}^{n+1,m} - \frac{C_{JE3}}{T} + (1-\alpha)G_{d3}^{n+1,m} + Y_0 \\
 -1 \qquad \qquad \qquad 1 \\
 1 \qquad \qquad \qquad -1 \\
 \qquad \qquad \qquad 1 \qquad \qquad \qquad -1
 \end{array}$$

Fig. 9. L.H.S. part of the nodal equations of the circuit shown in Fig. 8.

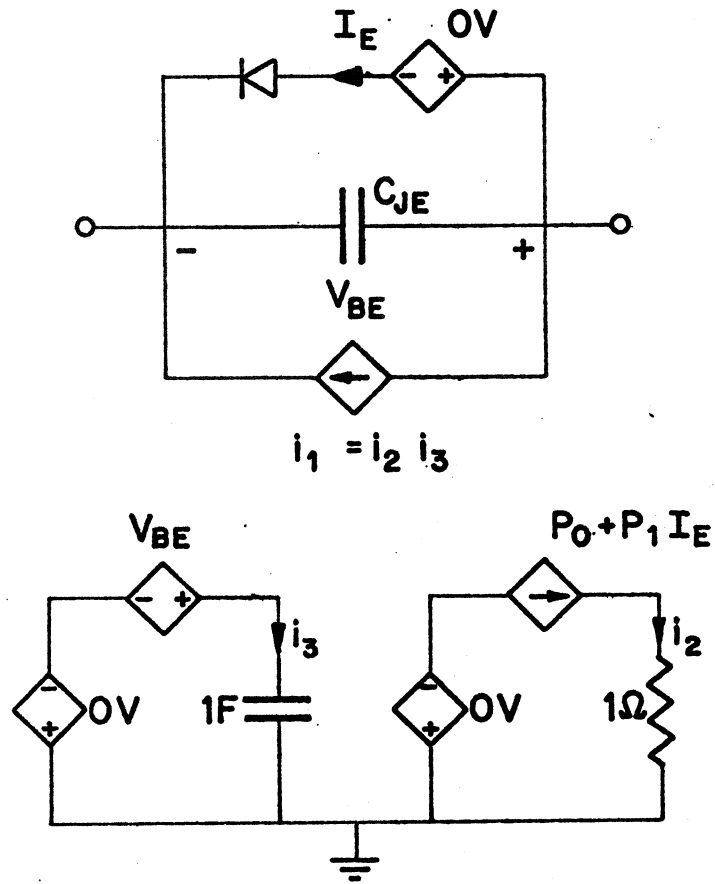


Fig. 10. An equivalent circuit for the transistor emitter junction supplied to SPICE2.

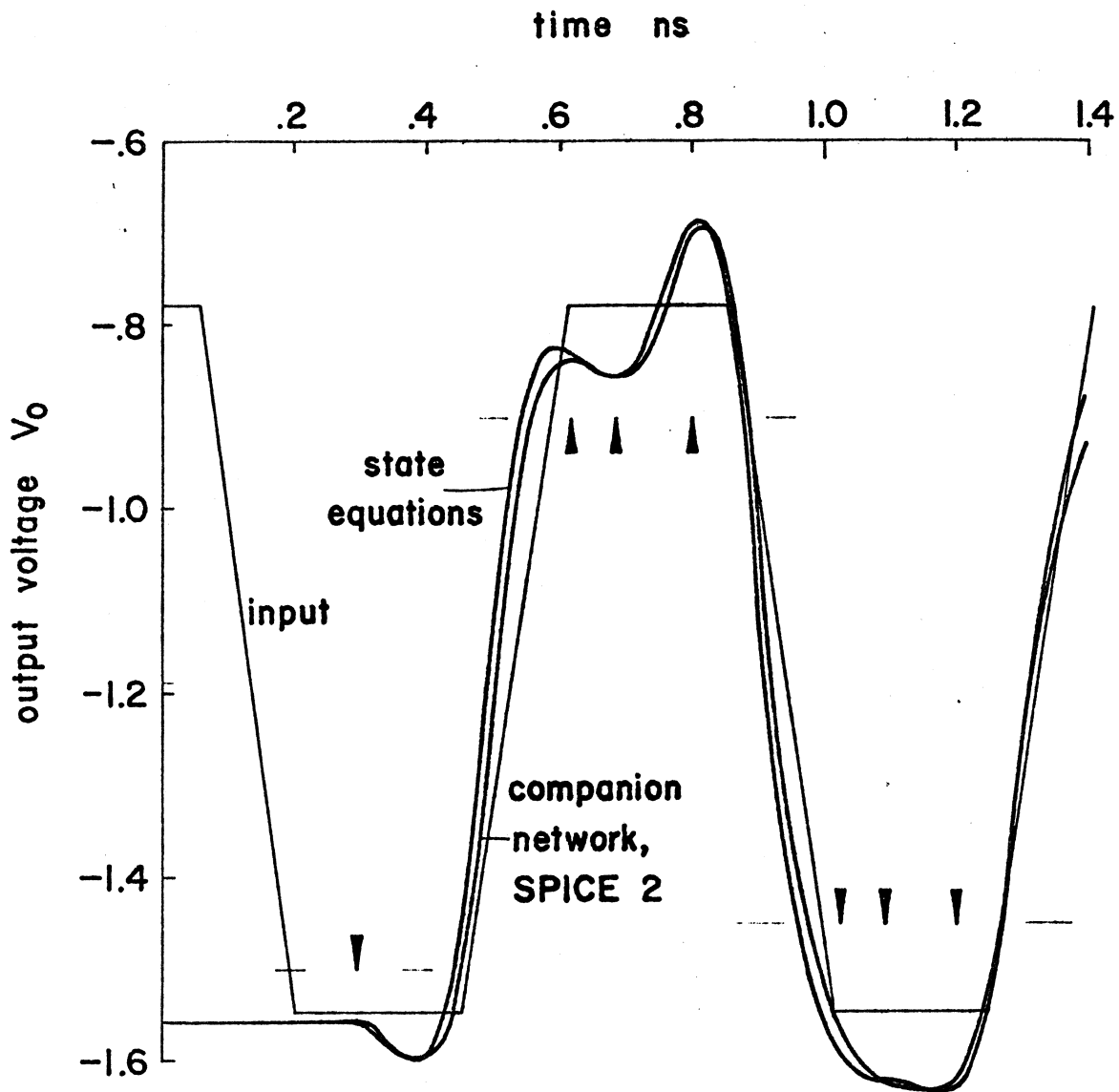


Fig. 11. Response of the CSEF circuit obtained by the companion network approach, SPICE2 and the state equations approach with the parameter values given in Tables 1,2,3 and 4.

Appendix A

Listing of the analysis programs of the CSEF circuit

A1) in the steady-state case (the capacitors removed)

A2) in the transient case.

```
PROGRAM TST ( INPUT, OUTPUT, TAPE5=INPUT, TAPE6=OUTPUT)      10
DIMENSION G(7,7), V(7), C(7), Y(7,7)                          20
C                                                                30
C  DEFINE TRANSISTOR AND DIODE PARAMETERS                       40
C                                                                50
CSAT= .6E-9                                                    60
SAT2=CSAT                                                       70
AL=38.668                                                       80
ALCS=2.32008E-8                                                90
ALCS2=ALCS                                                      100
ALPH= .99                                                       110
A= .01                                                          120
B=-A                                                            130
C                                                                140
C  DEFINE NETWORK PARAMETER VALUES                             150
C                                                                160
CB= 1./50.                                                       170
G1=1./281.33                                                    180
G2=1./75.                                                        190
G3=1./78.24                                                      200
G4=1./45.533                                                     210
CUR1=-.776*CB                                                    220
CUR2=G1*4.03                                                     230
CUR3=CB*1.13                                                     240
CUR4=G4*1.655                                                    250
C                                                                260
DO 1 I=1,7                                                       270
DO 1 J=1,7                                                       280
C(I,J)=0.                                                        290
1  CONTINUE                                                       300
DO 2 I=1,7                                                       310
V(I)=0.                                                           320
2  CONTINUE                                                       330
V(1)=-.781                                                       340
V(2)=-.7782                                                       350
V(3)=-1.211                                                       360
V(4)=-1.13                                                       370
V(5)=-1.177E-5                                                    380
V(6)=-1.57                                                       390
V(7)=-1.175                                                       400
M=0                                                               410
20 M=M+1                                                         420
V13=V(1)-V(3)                                                    430
V43=V(4)-V(3)                                                    440
V27=V(2)-V(7)                                                    450
V76=V(7)-V(6)                                                    460
E1=EXP(AL*V13)                                                    470
E2=EXP(AL*V43)                                                    480
E3=EXP(AL*V27)                                                    490
E4=EXP(AL*V76)                                                    500
GD1=ALCS*E1                                                       510
GD2=ALCS*E2                                                       520
GD3=ALCS*E3                                                       530
GD4=ALCS2*E4                                                      540
G(1,1)=CB+A*GD1                                                  550
G(1,3)=B*GD1                                                      560
Z1=ALPH*GD1                                                       570
G(2,1)=Z1                                                         580
G(2,2)=G3+A*GD3                                                  590
G(2,3)=-Z1                                                        600
G(2,7)=B*GD3                                                      610
C                                                                620
G(3,1)=-GD1                                                       630
G(3,3)=G1+GD1+GD2                                                640
G(3,4)=-GD2                                                       650
C                                                                660
G(4,3)=B*GD2                                                       670
G(4,4)=CB+A*GD2                                                  680
Z3=-ALPH*GD2                                                      690
C(5,3)=Z3                                                         700
C(5,4)=-Z3                                                        710
C(5,5)=G2                                                         720
G(6,6)=G4+GD4                                                     730
G(6,7)=-GD4                                                       740
```

	G(7,2)=-GD3	750
	G(7,6)=-GD4	760
	G(7,7)=GD4+GD3	770
C		780
C	LOAD CURRENT VECTOR	790
C	DEFINE CURRENT SOURCES WITH SUPERSCRIPT N+1, M	800
C		810
	C1=CSAT*(E1-1.)-GD1*V13	820
	C2=CSAT*(E2-1.)-GD2*V43	830
	C3=CSAT*(E3-1.)-GD3*V27	840
	C4=SAT2*(E4-1.)-GD4*V76	850
	C(1)=CUR1+B*C1	860
	C(2)=-ALPH*C1+B*C3	870
	C(3)=-CUR2+C1+C2	880
	C(4)=-CUR3+B*C2	890
	C(5)=-ALPH*C2	900
	C(6)=-CUR4+C4	910
	C(7)=-C4+C3	920
		930
C		940
C		950
C	STORE THE G MATRIX BEFORE GAUSS ELIMINATION	960
		970
	DO 3 I=1,7	980
	DO 3 J=1,7	990
	Y(I,J)=G(I,J)	1000
3	CONTINUE	1010
	CALL GELG(C,G,7,1,1.E-3,IER)	1020
	ERR=0.	1030
	DO 4 I=1,7	1040
	W=V(I)-C(I)	1050
	ERR=ERR+W*W	1060
4	V(I)=C(I)	1070
C		1080
C	TEST CONVERGENCE AND RESTORE THE G MATRIX	1090
C		1100
	DO 5 I=1,7	1110
	DO 5 J=1,7	1120
	G(I,J)=Y(I,J)	1130
5	CONTINUE	1140
	WRITE(6,500) M	1150
500	FORMAT(50X, I5)	1160
	IF(ERR.GT.1.E-16.AND.M.LT.25) GO TO 20	1170
		1180
C	PRINT OUTPUT	1190
C	WRITE(6,50) (V(I), I=1,7)	1200
50	FORMAT(5X,7E16.8)	1210
	STOP	1220
	END	

```

PROGRAM TST ( INPUT, OUTPUT, TAPE5=INPUT, TAPE6=OUTPUT)
DIMENSION G( 12, 12), V( 12), C( 12), Y( 12, 12), VV1( 100), VV2( 100), AI1( 100)
$, AI2( 100), E( 2)
LOGICAL IND1
DATA EU, EB, SL/0.776, 1.552, -5.17333333/

C
C NK IS THE NUMBER OF NODES
C T IS THE TIME STEP
C KF IS THE TAU OF THE TRANSMISSION LINE/T
C
NK=12
KF=100
MR=0
K=0
KK=0
DO 400 I=1, KF
AI1(I)=0.
AI2(I)=0.
VV1(I)=0.
VV2(I)=0.
400 CONTINUE
C
IND1=.TRUE.
TIM=0.
T=.25E-11
CX1=0.
CX2=0.

C
C DEFINE PARAMETERS OF THE TRANSISTORS AND DIODE
C
CSAT=.6E-9
SAT2=CSAT
AL=38.668
ALCS=2.32008E-8
ALCS2=ALCS
TT=.01E-9
TX1=TT*CSAT
TZ=TX1/T
TX2=TT*SAT2
TZ2=TX2/T
TMAX=1.4E-9

C
C DEFINE THE CONSTANT ELEMENTS VALUES
C
ALPH=.99
A=.01
B=-A
GB=1./50.
X1=.12E-12/T
X2=.5E-12/T
X3=1.248E-12/T
XP=X1+X1
G1=1./281.33
G2=1./75.
G3=1./78.24
G4=1./45.533
YO=1./92.004
CUR2=G1*4.03
CUR3=GB*1.13
CUR4=G4*1.655

C
DO 1 I=1, NK
DO 1 J=1, NK
C(I, J)=0.
1 CONTINUE
X4=GB+X1+X2
X5=G1+X1
X6=X4+X1
X7=G4+X3
X8=X1+YO
X9=1./T

C
C CONSTANT ELEMENTS IN THE G MATRIX
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	G(1,2)=-X2	750
	G(1,9)=X9	760
	G(2,2)=G3+X2+Y0	770
	G(3,9)=-X9	780
	G(3,10)=-X9	790
	G(4,5)=-X2	800
	G(4,10)=X9	810
	G(5,5)=G2+X2	820
	G(6,12)=-X9	830
	G(7,11)=-X9	840
	G(7,12)=X9	850
	G(8,11)=X9	860
	G(9,1)=-1.	870
	G(9,3)=1.	880
	G(10,3)=1.	890
	G(10,4)=-1.	900
	G(11,7)=1.	910
	G(11,8)=-1.	920
	G(12,6)=1.	930
	G(12,7)=-1.	940
C		950
C	INITIAL CONDITIONS (OBTAINED FROM STEADY STATE ANALYSIS)	960
C		970
	DO 2 I=1,NK	980
	V(I)=0.	990
2	CONTINUE	1000
	V(1)=-.78100994	1010
	V(2)=-.77778347	1020
	V(3)=-1.2111048	1030
	V(4)=-1.1300	1040
	V(5)=-.9807813E-6	1050
	V(6)=-1.557929	1060
	V(7)=-1.1678564	1070
	V(8)=V(2)	1080
	CX1=V(2)*Y0	1090
	CX2=CX1	1100
C		1110
	M=0	1120
10	TIM=TIM+T	1130
	K=K+1	1140
	NR=NR+1	1150
C		1160
C	SET UP VARIABLES WITH N, AND CONSTANT WITH M	1170
C		1180
	VN13=V(1)-V(3)	1190
	VN12=V(1)-V(2)	1200
	VN43=V(4)-V(3)	1210
	VN76=V(7)-V(6)	1220
	VN45=V(4)-V(5)	1230
	VN87=V(8)-V(7)	1240
	VN6=-V(6)	1250
	CUR5=X1*VN13	1260
	CUR6=X2*VN12	1270
	CUR7=X1*VN43	1280
	CUR8=X2*VN45	1290
	CUR9=X3*VN6	1300
	CUR10=X1*VN87	1310
	CUR11=X1*VN76	1320
	Q1N=TZ*(EXP(AL*VN13)-1.)	1330
	Q2N=TZ*(EXP(AL*VN43)-1.)	1340
	Q3N=TZ*(EXP(AL*VN87)-1.)	1350
	Q4N=TZ2*(EXP(AL*VN76)-1.)	1360
	IF(IND1) GO TO 7	1370
	J=K-KK	1380
	CX1=Y0*VV1(J)+A11(J)	1390
	CX2=Y0*VV2(J)+A12(J)	1400
7	CONTINUE	1410
C		1420
C	DEFINE INPUT VOLTAGE	1430
C		1440
	IF(K.GT.20) GO TO 221	1450
	E(1)=EU	1460
	GO TO 229	1470
221	IF(K.GT.80) GO TO 222	1480

	E(1)=EU-SL*(TIM-0.05E-9)/1.E-9	1490
	GO TO 229	1500
222	IF(K.GT.180) GO TO 223	1510
	E(1)=EB	1520
	GO TO 229	1530
223	IF(K.GT.240) GO TO 224	1540
	E(1)=EB+SL*(TIM-0.45E-9)/1.E-9	1550
	GO TO 229	1560
224	IF(K.GT.340) GO TO 225	1570
	E(1)=EU	1580
	GO TO 229	1590
225	IF(K.GT.400) GO TO 226	1600
	E(1)=EU-SL*(TIM-0.85E-9)/1.E-9	1610
	GO TO 229	1620
226	IF(K.GT.500) GO TO 227	1630
	E(1)=EB	1640
	GO TO 229	1650
227	E(1)=EB+SL*(TIM-1.25E-9)/1.E-9	1660
229	CONTINUE	1670
	CUR1=-E(1)*GB	1680
C		1690
C	SET UP THE REST OF G MATRIX(VARIABLE ENTRIES)	1700
C	WITH SUPERSCRIPT N+1,M	1710
C		1720
20	M=M+1	1730
	V13=V(1)-V(3)	1740
	V43=V(4)-V(3)	1750
	V76=V(7)-V(6)	1760
	V87=V(8)-V(7)	1770
	E1=EXP(AL*V13)	1780
	E2=EXP(AL*V43)	1790
	E3=EXP(AL*V87)	1800
	E4=EXP(AL*V76)	1810
	GD1=ALCS*E1	1820
	GD2=ALCS*E2	1830
	GD3=ALCS*E3	1840
	GD4=ALCS*E4	1850
	GC1=1./(TT*GD1)	1860
	GC2=1./(TT*GD2)	1870
	GC3=1./(TT*GD3)	1880
	GC4=1./(TT*GD4)	1890
C		1900
	G(1,1)=X4+A*GD1	1910
	G(1,3)=-X1+B*GD1	1920
	Z1=ALPH*GD1	1930
	G(2,1)=-X2+Z1	1940
	G(2,3)=-Z1	1950
	G(3,1)=-X1-GD1	1960
	G(3,3)=G1-G(3,1)+X1+GD2	1970
	G(3,4)=-X1-GD2	1980
	Z2=A*GD2	1990
	G(4,3)=-X1-Z2	2000
	G(4,4)=X4+Z2	2010
	Z3=-ALPH*GD2	2020
	G(5,3)=Z3	2030
	G(5,4)=-X2-Z3	2040
	G(6,6)=X7+GD4+X1	2050
	G(6,7)=-GD4-X1	2060
	G(7,6)=-GD4-X1	2070
	G(7,7)=XP+GD3+GD4	2080
	G(7,8)=-X1-GD3	2090
	Z4=A*GD3	2100
	G(8,7)=-X1-Z4	2110
	G(8,8)=Y0-G(8,7)	2120
	G(9,9)=GC1	2130
	G(10,10)=GC2	2140
	G(11,11)=GC3	2150
	G(12,12)=GC4	2160
C		2170
C	LOAD CURRENT VECTOR	2180
C	DEFINE CURRENT SOURCES WITH SUPERSCRIPT N+1,M	2190
C		2200
	C1=CSAT*(E1-1.)-GD1*V13	2210
	C2=CSAT*(E2-1.)-GD2*V43	2220

	C3=CSAT*(E3-1.)-GD3*VB7	2230
	C4=SAT2*(E4-1.)-GD4*V76	2240
C		2250
	C(1)=CUR5+Q1N-A*C1+CUR6+CUR1	2260
	C(2)=-CUR6-ALPH*C1+CX2	2270
	C(3)=-CUR2-Q1N-CUR5+C1-Q2N-CUR7+C2	2280
	C(4)=-CUR3+CUR7-A*C2+Q2N+CUR8	2290
	C(5)=-CUR8-ALPH*C2	2300
	C(6)=-CUR4-CUR9+C4-Q4N-CUR11	2310
	C(7)=-C4+C3-CUR10-Q3N+Q4N+CUR11	2320
	C(8)=Q3N+CUR10-A*C3+CX1	2330
C		2340
	C(9)=-V13+GC1*TX1*(E1-1.)	2350
	C(10)=-V43+GC2*TX1*(E2-1.)	2360
	C(11)=-V87+GC3*TX1*(E3-1.)	2370
	C(12)=-V76+GC4*TX2*(E4-1.)	2380
C		2390
C	STORE THE G MATRIX BEFORE GAUSS ELIMINATION	2400
C		2410
	DO 3 I=1,NK	2420
	DO 3 J=1,NK	2430
	Y(I,J)=G(I,J)	2440
3	CONTINUE	2450
	CALL GELG(C,G,NK,1,1.E-3,IER)	2460
	ERR=0.	2470
	DO 4 I=1,NK	2480
	W=V(I)-C(I)	2490
	ERR=ERR+W*W	2500
4	V(I)=C(I)	2510
C		2520
C	TEST CONVERGENCE AND RESTORE THE G MATRIX	2530
C		2540
	DO 5 I=1,NK	2550
	DO 5 J=1,NK	2560
	G(I,J)=Y(I,J)	2570
5	CONTINUE	2580
	IF(ERR.GT.1.E-12.AND.M.LT.15) GO TO 20	2590
C		2600
	VV1(MR)=V(2)	2610
	VV2(MR)=V(8)	2620
	AI1(MR)=YO*V(2)-CX2	2630
	AI2(MR)=YO*V(8)-CX1	2640
C	PRINT OUTPUT	2650
	MK=MOD(K,5)	2660
	IF(MK.NE.0) GO TO 22	2670
	WRITE(6,40) TIM,M,V(6)	2680
22	IF(K.GE.KF) IND1=.FALSE.	2690
	IF(TIM.GE.TMAX) STOP	2700
	M=0	2710
	MM=MOD(K,KF)	2720
	IF(MM.NE.0) GO TO 10	2730
	KK=KK+KF	2740
	MR=0	2750
	GO TO 10	2760
C		2770
40	FORMAT(20X,E16.8,10X,I5,10X,E16.8,/)	2780
50	FORMAT(5X,11E10.4)	2790
101	FORMAT(E16.8)	2800
500	FORMAT(50X,I5)	2810
	END	2820

Appendix B

Data, supplied to SPICE2, for the CSEF circuit

B1) with the equivalent circuit of the emitter junction

B2) with built-in transistor models.

```

CURRENT SWITCH EMITTER FOLLOWER
R1 4 5 281.33
R2 7 0 75.
R3 2 0 78.24
R4 10 1 45.533
CO 10 0 1.248E-12
T1 2 0 8 0 Z0=92.004 TD=.25NS
VE2 0 5 DC 4.03
VE3 0 6 DC 1.13
VE4 0 1 DC 1.655
VE1 3 0 PWL(0 -.776 .05NS -.776 .2NS -1.55 .45NS -1.55 .6NS
+-.776 .85NS -.776 1.NS -1.55 1.25NS -1.55 1.4NS -.776)
D1 9 10 DMOD
D2 13 4 DMOD
D3 14 4 DMOD
D4 15 9 DMOD
CE1 11 4 0.12P
CC1 11 2 0.5P
CE2 12 4 0.12P
CC2 12 7 0.5P
CE3 8 9 0.12P
RB1 3 11 50.
RB2 12 6 50.
RT1 17 0 1.
RT2 20 0 1.
RT3 23 0 1.
CT1 25 0 1.E-8
CT2 26 0 1.E-8
CT3 27 0 1.E-8
VT1 11 13 DC 0.
VT2 12 14 DC 0.
VT3 8 15 DC 0.
VT4 16 17 DC 0.
VT5 19 20 DC 0.
VT6 22 23 DC 0.
VT7 18 25 DC 0.
VT8 21 26 DC 0.
VT9 24 27 DC 0.
E1 18 0 13 4 1
E2 21 0 14 4 1
E3 24 0 15 9 1
F1 2 11 VT1 0.99
F2 7 12 VT2 0.99
F3 0 8 VT3 0.99
F4 0 16 VT1 2.3200E-10 3.8668E-2
F5 0 19 VT2 2.3200E-10 3.8668E-2
F6 0 22 VT3 2.3200E-10 3.8668E-2
F7 11 4 POLY(2) VT4 VT7 0 0 0 0 1
F8 12 4 POLY(2) VT5 VT8 0 0 0 0 1
F9 8 9 POLY(2) VT6 VT9 0 0 0 0 1
.TRAN 0.0125NS 1.4NS
.PRINT TRAN V(10,0)
.PLOT TRAN V(10,0)
.MODEL DMOD D IS=.6E-9
.END

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CURRENT SWITCH EMITTER FOLLOWER
R1  4  5 281.33      10
R2  7  0  75.      20
R3  2  0  78.24     30
R4  10 1  45.533    40
CQ  10 0  1.248E-12 50
T1  2  0  8  0 Z0=92.004 TD=.25NS 60
VE2  0  5  DC 4.03  70
VE3  0  6  DC 1.13  80
VE4  0  1  DC 1.655 90
VE1  3  0  PWL(0 -.776 .05NS -.776 .2NS -1.55 .45NS -1.55 .6NS 100
+-.776 .85NS -.776 1.NS -1.55 1.25NS -1.55 1.4NS -.776) : 110
D1  9  10  DMOD 120
QT1  2  3  4  QMOD 130
QT2  7  6  4  QMOD 140
QT3  0  8  9  QM1 150
.TRAN 0.0125NS 1.4NS 160
.PRINT TRAN V(10,0) 170
.PLOT  TRAN V(10,0) 180
.MODEL DMOD D IS=.6E-9 190
.MODEL QMOD NPN BF=99. IS=.6E-9 RB=50. TF=.01NS CJE=0.12PF CJC=0. 200
+ MC=0. ME=0. 210
.MODEL QM1 NPN BF=99. IS=.6E-9 TF=.01NS CJE=0.12PF ME=0. MC=0. 220
.END 230
      240

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SOC-193

ANALYSIS OF A CURRENT SWITCH EMITTER FOLLOWER USING THE COMPANION NETWORK APPROACH

M.R.M. Rizk

April 1978, No. of Pages: 33

Revised:

Key Words: Nonlinear circuit analysis, companion network formulation, integration methods

Abstract: This report demonstrates, in a tutorial fashion, the transient analysis of a nonlinear circuit, namely a current switch emitter follower. The response obtained was checked against other responses obtained by a program which uses the state space formulation for the analysis and by SPICE2.

Description: Contains Fortran listing, user's manual.
The listing contains 336 cards, of which 68 are comment cards.
There are also 79 lines of data for SPICE2.

Related Work: SOC-182, SOC-185, SOC-192, SOC-194.

Price: \$15.00.

