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STATE EQUATION ANALYSIS AND COMPUTER PROGRAM  
FOR A CURRENT SWITCH EMITTER FOLLOWER

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Abstract

The analysis of a current switch emitter follower (CSEF) circuit originally given by Ho is described. State equations in conjunction with Gear's integration method are used to obtain the output response.

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## I. INTRODUCTION

A current switch emitter follower circuit which was previously investigated by Ho [1] in the context of sensitivity calculation is described in detail.

The circuit is depicted in Fig. 1. The decoupled equivalent circuit of the transmission line is used [2]. Considering a lossless transmission line and the charge-control model of the transistors as well as the diode the equivalent circuit is shown in Fig. 2. The definitions of the model parameters are given in Table I.

The following two equations are used for the transmission line model, taking  $Z_0$  as characteristic impedance and  $\tau$  as delay time:

$$u_i(t) = [e_o(t-\tau) + Z_0 i_o(t-\tau)]U(t-\tau) + \phi_i(t), \quad (1)$$

$$u_r(t) = [e_l(t-\tau) + Z_0 i_l(t-\tau)]U(t-\tau) + \phi_r(t), \quad (2)$$

where  $U$  is the step function given by

$$U(t-\tau) = \begin{cases} 0 & t < \tau, \\ 1 & t \geq \tau. \end{cases} \quad (3)$$

The parameter  $\phi$  represents the initial voltage distribution stored on the transmission line. Thus, we take

$$\phi_i(t) = \phi_r(t) = 0 \quad \text{for } t \geq \tau. \quad (4)$$

The steady state solution is obtained using the Newton-Raphson algorithm as shown in Section II. The state equations are formulated in Section III. The subroutine DVOGER [3] based on Gear's integration algorithm [4] is used. The algorithm has a variable step and hence interpolation was used to find the values of  $u_i(t)$  and  $u_r(t)$  if  $t-\tau$  falls between time steps. Alternatively,  $\tau/n$ , where  $n$  is an integer can

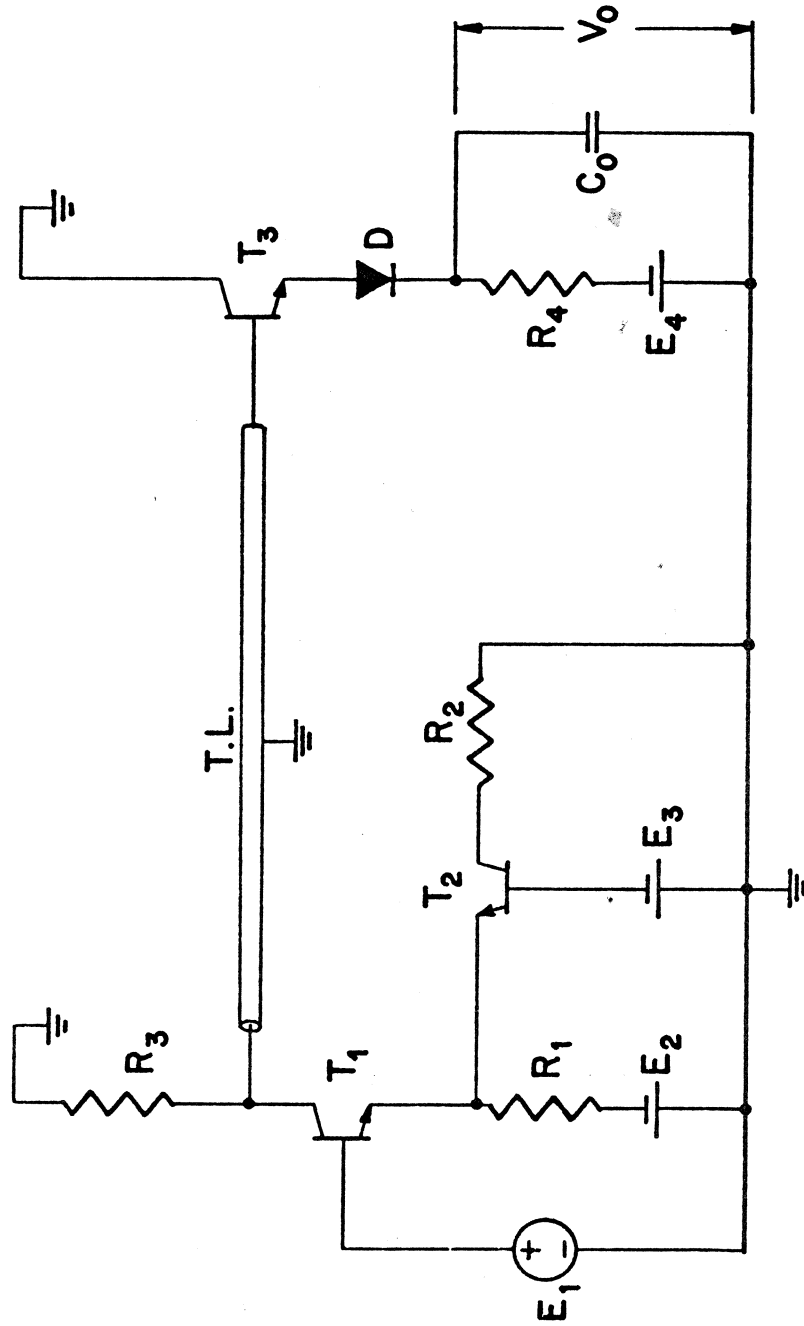


Fig. 1 The CSEF circuit [1].

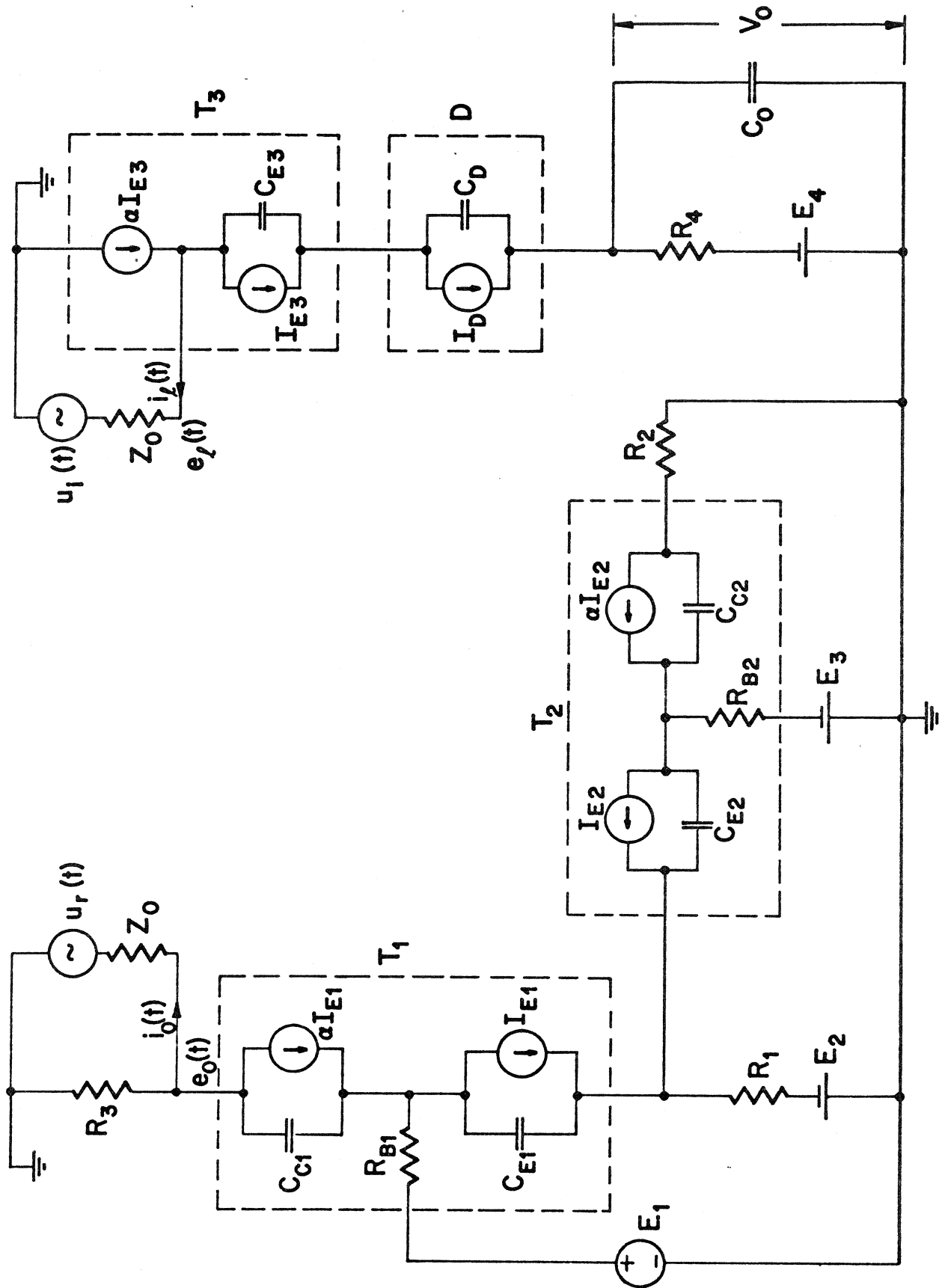


Fig. 2 The CSEF equivalent circuit used, indicating transmission-line, transistor and diode models.

TABLE I(a)  
DIODE MODEL PARAMETERS

---

$I_{SD}$	diode saturation current
$C_{JD}$	depletion layer capacitance
$TT_D$	transit time
$\theta$	inverse of thermal potential

---

$$I_D = I_{SD}(\exp(\theta V_D) - 1)$$

$$C_D = C_{JD} + TT_D \frac{dI_D}{dV_D}$$

---

TABLE I(b)  
TRANSISTOR MODEL PARAMETERS

---

$I_S$	saturation current
$\alpha$	common base current gain
$R_B$	base resistance
$C_C$	collector junction capacitance
$C_{JE}$	emitter junction depletion layer capacitance
$TT$	base transit time
$\theta$	inverse of thermal potential

---

$$I_E = I_S (\exp(\theta V_{BE}) - 1)$$

$$I_C = \alpha I_E$$

$$C_E = C_{JE} + TT \frac{dI_E}{dV_{BE}}$$

$R_B$  and  $C_C$  are assumed zero for transistor  $T_3$

---

be used as a fixed step, however, integration will be expensive.

A FORTRAN listing of the program is given in the appendix. Library subroutines DVOGER [3] and GELG [5] are used.

## II. DC ANALYSIS OF THE CSEF CIRCUIT

The DC equivalent circuit is shown in Fig. 3. Loops 1 and 2 will lead to the following two KVL equations.

$$V_{BE1} + I_{E1}(R_1 + R_{B1}) + I_{E2}R_1 - E_2 - E_1 = 0 , \quad (5)$$

$$V_{BE2} + I_{E2}(R_1 + R_{B2}) + I_{E1}R_1 - E_2 + E_3 = 0 , \quad (6)$$

where

$$I_{E1} = I_{S1} (\exp(\theta V_{BE1}) - 1) , \quad (7)$$

$$I_{E2} = I_{S2} (\exp(\theta V_{BE2}) - 1) . \quad (8)$$

The two simultaneous nonlinear equations (5) and (6) in  $V_{BE1}$  and  $V_{BE2}$  are solved using the Newton-Raphson algorithm.

Knowing that the transmission line will have zero length for DC analysis, the base voltage of the output transistor  $T_3$  is

$$V_{B3} = - R_3 (\alpha I_{E1} + (1 - \alpha) I_{E3}) . \quad (9)$$

Since

$$I_{E3} = I_D = I_{SD} (\exp(\theta V_D) - 1) , \quad (10)$$

then

$$V_D = \ln(1 + I_{E3}/I_D) / \theta , \quad (11)$$

where

$$I_{E3} = I_{S3} (\exp(\theta V_{BE3}) - 1) . \quad (12)$$

But

$$V_{B3} = V_{BE3} + V_D + I_{E3} R_4 - E_4 . \quad (13)$$

Accordingly, (9) and (13) lead to the nonlinear equation



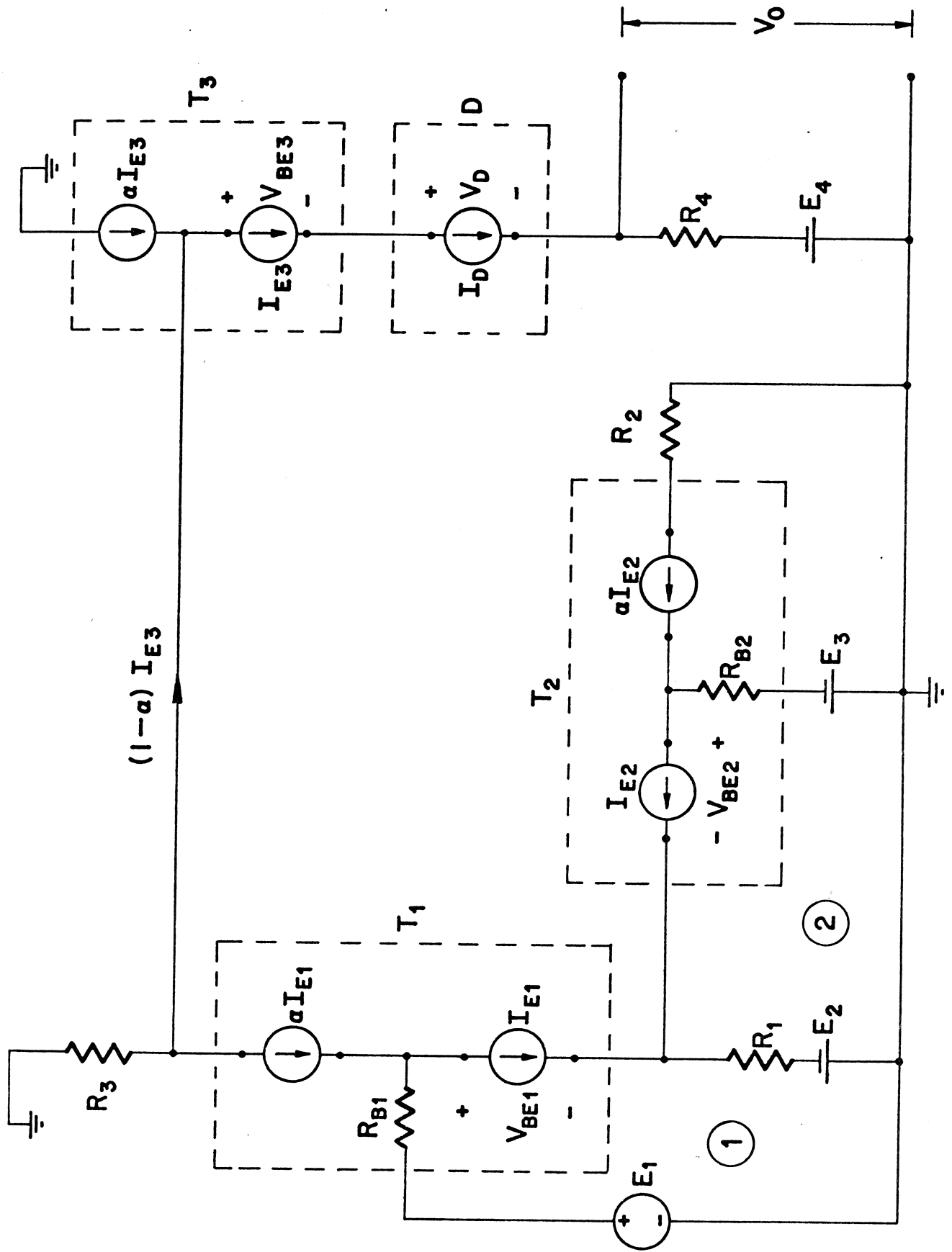


Fig. 3 The DC equivalent circuit of the CSEF.

$$V_{BE3} + \frac{1}{\theta} \ln\left(1 + \frac{I_{E3}}{I_{SD}}\right) + I_{E3} R_4 - E_4 + R_3 [\alpha I_{E1} + (1-\alpha) I_{E3}] = 0 \quad (14)$$

in  $V_{BE3}$ , where  $I_{E3}$  is given by (12).

Having  $V_{BE1}$ ,  $V_{BE2}$  and  $V_{BE3}$  all other potentials can be obtained in a simple manner.

### III. TOPOLOGICAL FORMULATION OF THE STATE EQUATIONS

The basic steps required in the formulation of the state equations for nonlinear networks are sketched out. For further details see Chua and Lin [6].

#### Step 1 Formation and characterization of network branches

This step involves the characterization of linear and nonlinear elements, controlled and independent sources and tree and cotree (link) branches. The choice of the tree branches is based upon

- (i) all independent and controlled voltage sources,
- (ii) as many capacitors as possible,
- (iii) as many resistors as possible,
- (iv) as few inductors as possible,
- (v) no independent current sources.

#### Step 2 Solving the resistive nonlinear subnetwork

We solve for the voltages across the nonlinear resistors in the tree as well as the currents in the nonlinear resistors in the cotree.

#### Step 3 Solving the loops which include capacitors only and the cutsets which include inductors only

In this step we express the currents in the cotree capacitors and the voltages across the tree inductors in terms of the derivatives (w.r.t. time) of the tree capacitor voltages and the cotree inductor currents. Also, they may well be functions of the derivatives of voltages of the tree independent voltage sources and derivatives of currents of cotree independent current sources (if these derivatives exist).

Step 4 Collecting relationships derived so far to formulate the state equations.

Regarding the CSEF circuit shown in Fig. 2, the input and output circuits can be treated independently.

#### Formulation of the State Equations for the Input Circuit

The tree chosen according to the priorities mentioned before is shown in Fig. 4. According to this tree, the set of independent KCL equations is

$$D \tilde{i} = 0, \quad (15)$$

where

$$\tilde{i} = \begin{bmatrix} I_{\sim ET} \\ I_{\sim CT} \\ I_{\sim RT} \\ I_{\sim RL} \\ I_{\sim JL} \end{bmatrix}, \quad (16)$$

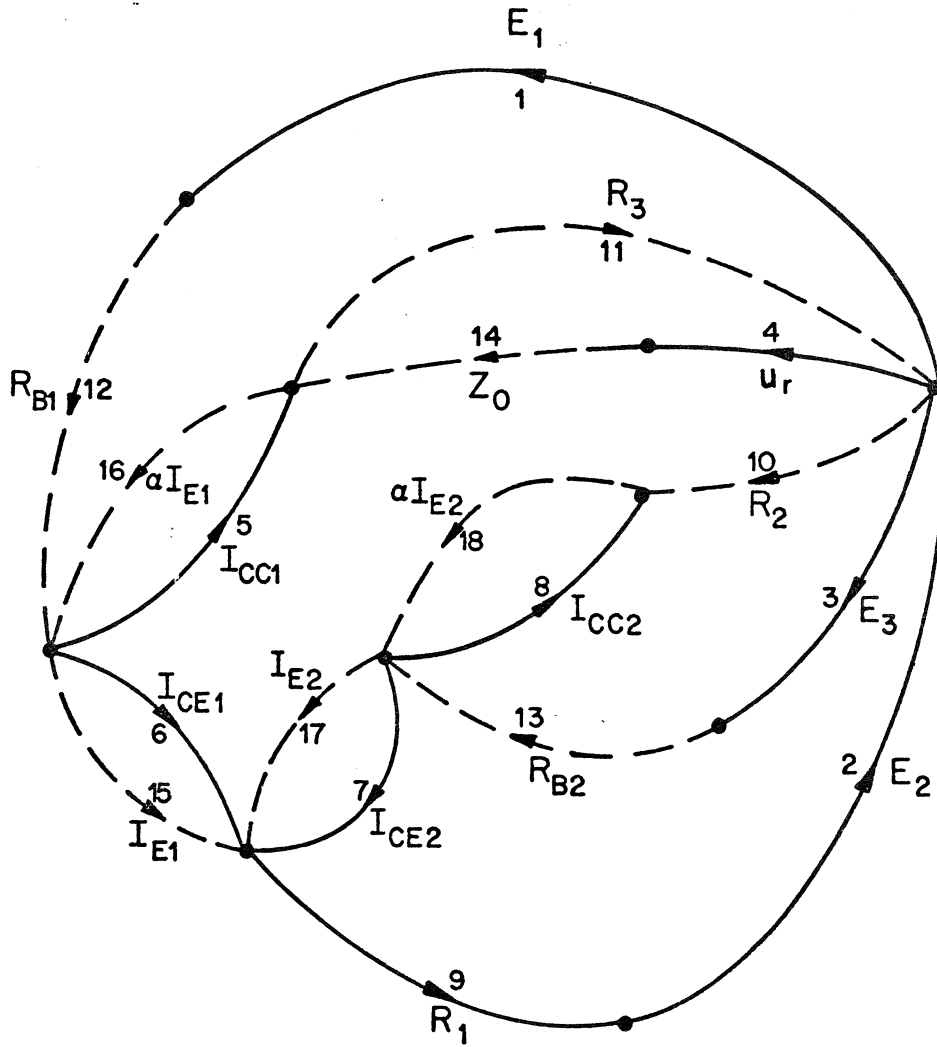


Fig. 4 Directed graph of the input circuit and branch numbering.

- Tree chosen
- Corresponding link



Hence, we can write (15) as

$$\left[ \begin{array}{c|cc} \mathbb{I}_9 & D_{11} & D_{12} \\ & D_{21} & D_{22} \\ & D_{31} & D_{32} \end{array} \right] \begin{bmatrix} I_{ET} \\ I_{CT} \\ I_{RT} \\ I_{RL} \\ I_{JL} \end{bmatrix} = \underline{\underline{0}}, \quad (23)$$

where

$$D_{11} = \begin{bmatrix} -1 & 1 & -1 & -1 & -1 \\ -1 & & -1 & & -1 \\ & & & -1 & -1 \\ & & & & -1 \end{bmatrix}, \quad (24)$$

$$D_{12} = \underline{\underline{0}}, \quad (25)$$

$$D_{21} = \begin{bmatrix} -1 & 1 & -1 & -1 & -1 \\ -1 & & & & -1 \\ 1 & & & & \end{bmatrix}, \quad (26)$$

$$D_{22} = \begin{bmatrix} 1 & -1 & & & \\ & & 1 & & \\ & & & 1 & \\ & & & & -1 \end{bmatrix}, \quad (27)$$

$$D_{31} = [-1 \quad 1 \quad -1 \quad -1 \quad -1], \quad (28)$$

$$D_{32} = \underline{\underline{0}}. \quad (29)$$

and  $\mathbb{I}_9$  is the identity matrix of order 9. The KVL equations can be written as

$$\left[ \begin{array}{ccc|c} D_{11}^T & D_{21}^T & D_{31}^T & -\mathbb{I}_9 \\ D_{12}^T & D_{22}^T & D_{32}^T & \end{array} \right] \begin{bmatrix} V_{ET} \\ V_{CT} \\ V_{RT} \\ V_{RL} \\ V_{JL} \end{bmatrix} = \underline{\underline{0}}, \quad (30)$$

where superscript T denotes transposition.

It is required to represent the link currents  $\underline{I}_{RL}$  in terms of  $\underline{V}_{ET}$  and  $\underline{V}_{CT}$ . We have

$$\begin{aligned}\underline{V}_{RL} &= \underline{R}_L \underline{I}_{RL} \\ &= \underline{D}_{11}^T \underline{V}_{ET} + \underline{D}_{21}^T \underline{V}_{CT} + \underline{D}_{31}^T \underline{V}_{RT},\end{aligned}\quad (31)$$

where

$$\underline{R}_L = \begin{bmatrix} R_2 & & & & & & \\ & R_3 & & & & & \\ & & R_{B1} & & & & \\ & & & R_{B2} & & & \\ & & & & Z_0 & & \\ & & & & & & \end{bmatrix}.$$
 (32)

Using (23) and (29) we can write

$$\begin{aligned}\underline{I}_{RT} &= -\underline{D}_{31} \underline{I}_{RL} - \underline{D}_{32} \underline{I}_{JL} \\ &= -\underline{D}_{31} \underline{I}_{RL}.\end{aligned}\quad (33)$$

Thus,

$$\underline{V}_{RT} = \underline{R}_T \underline{I}_{RT} = -\underline{R}_T \underline{D}_{31} \underline{I}_{RL},\quad (34)$$

where

$$\underline{R}_T = [\underline{R}_1].\quad (35)$$

Substituting for  $\underline{V}_{RT}$  in (31) and with some manipulations, we obtain

$$\underline{I}_{RL} = \underline{R}^{-1} [\underline{D}_{11}^T \underline{V}_{ET} + \underline{D}_{21}^T \underline{V}_{CT}],\quad (36)$$

where

$$\underline{R} = \underline{R}_L + \underline{D}_{31}^T \underline{R}_T \underline{D}_{31}.\quad (37)$$

From (23), we have

$$\underline{I}_{CT} = -D_{21} \underline{I}_{RL} - D_{22} \underline{I}_{JL} . \quad (38)$$

Substituting for  $\underline{I}_{RL}$  from (36), the state equations are

$$\underline{I}_{CT} = -D_{21} \underline{R}^{-1} [D_{11}^T \underline{V}_{ET} + D_{21}^T \underline{V}_{CT}] - D_{22} \underline{I}_{JL} . \quad (39)$$

More explicitly, they can be written as

$$\begin{bmatrix} C_{C1} & dV_{C1}/dt \\ C_{E1} & dV_{BE1}/dt \\ C_{E2} & dV_{BE2}/dt \\ C_{C2} & dV_{C2}/dt \end{bmatrix} = -D_{21} \underline{R}^{-1} \begin{bmatrix} D_{11}^T \\ D_{21}^T \end{bmatrix} \begin{bmatrix} E_1 \\ E_2 \\ E_3 \\ u_r \end{bmatrix} + D_{21}^T \begin{bmatrix} V_{C1} \\ V_{BE1} \\ V_{BE2} \\ V_{C2} \end{bmatrix} + \begin{bmatrix} I_{16} \\ -I_{15} \\ -I_{17} \\ I_{18} \end{bmatrix} , \quad (40)$$

where

$$C_{E1} = C_{JE} + TT \theta I_S \exp(\theta V_{BE1}) , \quad (41)$$

$$C_{E2} = C_{JE} + TT \theta I_S \exp(\theta V_{BE2}) , \quad (42)$$

$$I_{15} = I_S (\exp(\theta V_{BE1}) - 1) , \quad (43)$$

$$I_{16} = \alpha I_{15} , \quad (44)$$

$$I_{17} = I_S (\exp(\theta V_{BE2}) - 1) , \quad (45)$$

$$I_{18} = \alpha I_{17} . \quad (46)$$

#### Formulation of the State Equations for the Output Circuit

Fig. 5 shows the chosen tree and branch numbering. The set of independent KCL equations is

$$\underline{D} \underline{i} = \underline{0} , \quad (47)$$



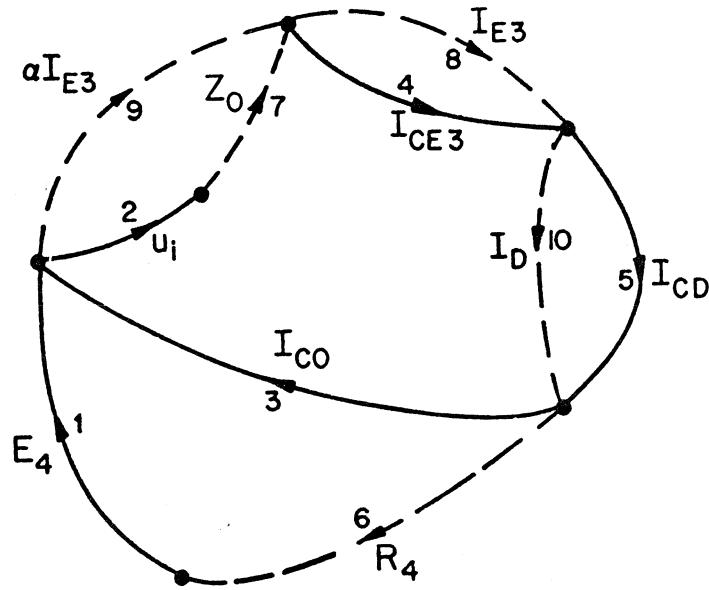


Fig. 5 Directed graph of the output circuit and branch numbering.

— Tree chosen

--- Corresponding link

where

$$\tilde{D} = \left[ \begin{array}{cccc|cccc} 1 & & & & -1 & & & \\ & 1 & & & & -1 & & \\ & & 1 & & & & -1 & \\ & & & 1 & & & & -1 \\ & & & & 1 & & & \\ & & & & & 1 & & \\ & & & & & & 1 & \\ & & & & & & & 1 \end{array} \right], \quad (48)$$

$$\tilde{i} = \begin{bmatrix} I_{\tilde{ET}} \\ I_{\tilde{CT}} \\ I_{\tilde{RL}} \\ I_{\tilde{JL}} \end{bmatrix}, \quad (49)$$

$$I_{\tilde{ET}} \triangleq \text{Tree voltage source currents} = \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}, \quad (50)$$

$$I_{\tilde{CT}} \triangleq \text{Tree capacitor currents} = \begin{bmatrix} I_3 \\ I_4 \\ I_5 \end{bmatrix}, \quad (51)$$

$$I_{\tilde{RL}} \triangleq \text{Link resistor currents} = \begin{bmatrix} I_6 \\ I_7 \end{bmatrix}, \quad (52)$$

$$I_{\tilde{JL}} \triangleq \text{Link current sources} = \begin{bmatrix} I_8 \\ I_9 \\ I_{10} \end{bmatrix}. \quad (53)$$

The KVL equations are

$$\left[ \begin{array}{cccc|cccc} -1 & & & & -1 & & & \\ & -1 & -1 & -1 & & -1 & & \\ & & 1 & -1 & & & -1 & \\ & & & 1 & & & & \\ & & & & -1 & & & \\ & & & & & -1 & & \\ & & & & & & -1 & \\ & & & & & & & 1 \end{array} \right] \begin{bmatrix} V_{\tilde{ET}} \\ V_{\tilde{CT}} \\ V_{\tilde{RL}} \\ V_{\tilde{JL}} \end{bmatrix} = \tilde{0}, \quad (54)$$

Hence,

$$\begin{aligned} \underline{V}_{RL} &= \underline{R}_L \underline{I}_{RL} \\ &= \underline{D}_{11}^T \underline{V}_{ET} + \underline{D}_{21}^T \underline{V}_{CT}, \end{aligned} \quad (55)$$

where

$$\underline{R}_L = \begin{bmatrix} R_4 & \\ & Z_0 \end{bmatrix}, \quad (56)$$

$$\underline{D}_{11} = \begin{bmatrix} -1 & \\ & -1 \end{bmatrix}, \quad (57)$$

$$\underline{D}_{21} = \begin{bmatrix} 1 & -1 \\ & -1 \\ & -1 \end{bmatrix}. \quad (58)$$

Thus,

$$\underline{I}_{RL} = \underline{R}_L^{-1} [\underline{D}_{11}^T \underline{V}_{ET} + \underline{D}_{21}^T \underline{V}_{CT}]. \quad (59)$$

From (47), we have

$$\underline{I}_{ET} = -\underline{D}_{11} \underline{I}_{RL} \quad (60)$$

and

$$\underline{I}_{CT} = -\underline{D}_{21} \underline{I}_{RL} - \underline{D}_{22} \underline{I}_{JL}. \quad (61)$$

Substituting for  $\underline{I}_{RL}$  from (59) into (60), the state equations are

$$\underline{I}_{CT} = -\underline{D}_{21} \underline{R}_L^{-1} [\underline{D}_{11}^T \underline{V}_{ET} + \underline{D}_{21}^T \underline{V}_{CT}] - \underline{D}_{22} \underline{I}_{JL}. \quad (62)$$

Or, more explicitly, the state equations are

$$\begin{bmatrix} C_0 & dV_0/dt \\ C_{E3} & dV_{BE3}/dt \\ C_D & dV_D/dt \end{bmatrix} = -D_{21} \begin{bmatrix} 1/R_4 \\ 1/Z_0 \end{bmatrix} \begin{bmatrix} D_{11}^T & D_{21}^T \end{bmatrix} \begin{bmatrix} E_4 \\ u_i \\ V_0 \\ V_{BE3} \\ V_D \end{bmatrix} + \begin{bmatrix} I_9 \\ I_9 - I_8 \\ I_9 - I_{10} \end{bmatrix}, \quad (63)$$

where

$$C_{E3} = C_{JE} + TT \theta I_S \exp(\theta V_{BE3}), \quad (64)$$

$$C_D = C_{JD} + TT_D \theta I_{SD} \exp(\theta V_D), \quad (65)$$

$$I_8 = I_S (\exp(\theta V_{BE3}) - 1), \quad (66)$$

$$I_9 = \alpha I_8, \quad (67)$$

$$I_{10} = I_{SD} (\exp(\theta V_D) - 1). \quad (68)$$

If the diode is similar to the transistor base emitter junction, then

$$V_D = V_{BE3} \quad (69)$$

and

$$I_{10} = I_8. \quad (70)$$

Hence, the three state equations (63) can be reduced to the following two equations

$$\begin{bmatrix} C_0 & dv_0/dt \\ C_{E3} & dv_{BE3}/dt \end{bmatrix} = \begin{bmatrix} -1 & 1 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1/R_4 & \\ & 1/Z_0 \end{bmatrix} + \begin{bmatrix} -1 & & 1 \\ & -1 & -1 & -2 \end{bmatrix} \begin{bmatrix} E_4 \\ u_i \\ v_0 \\ v_{BE3} \end{bmatrix} + \begin{bmatrix} I_9 \\ I_9 - I_8 \end{bmatrix} . \quad (71)$$

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- [2] D.A. Calahan, Computer-aided Network Design (Revised Edition). New York: McGraw-Hill, 1972.
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- [5] Subroutine GELG, System/360 Scientific Subroutine Package, Version III, IBM Programmer's Manual Number 360A-CM-03x, p. 121.
- [6] L.O. Chua and P.M. Lin, Computer-aided Analysis of Electronic Circuits. Englewood Cliffs, NJ: Prentice-Hall, 1975.

APPENDIX

FORTRAN LISTING OF THE CSEF ANALYSIS SUBROUTINES

The subroutine CSEF supplies the values of the output response  $V_0$  in the array F(121) for a given value of the parameter vector

$$\tilde{x} = \begin{bmatrix} E_4 \\ Z_0 \\ R_4 \\ C_0 \\ \alpha_3 \\ I_{S3} \\ C_{JE3} \\ TT_3 \end{bmatrix} .$$

The parameter vector  $\tilde{x}$  may be scaled by values given in the array SCALE(8).

For program notation and associated text notation, see Table A.

TABLE A  
RELATION BETWEEN TEXT AND PROGRAM NOTATIONS

Description	Text Notation	Program Notation	
Circuit Parameters	$R_1$	R1	*
	$R_2$	R2	*
	$R_3$	R3	*
	$R_4$	R4	*
	$E_1$	E(1)	***
	$E_2, E_3$ and $E_4$	E(I), I = 2,3,4	*
	$C_0$	CO	*
Diode Parameters	$V_D$	VD	**
	$I_{SD}$	SATD	*
	$\theta I_{SD} TT_D$	TSD	**
	$TT_D$	TTD	*
	$C_{JD}$	CD	*
Transistor Parameters	$I_S$	SATC(I), I = 1,2,3	*
	TT	TT	*
	$\theta$	THETA	*
	$\alpha$	ALPHA(I), I = 1,2,3	*
	$\theta I_S TT$	TST(I), I = 1,2,3	**
	$\alpha I_S$	ASAT(I), I = 1,2,3	**
	$C_{JE}$	CEJ(I), I = 1,2,3	*
	$C_C$	CC(I), I = 1,2,3	*
$R_B$	RB(I), I = 1,2	*	
Transmission-Line Parameters	$Z_0$	Z0	*
	$\tau$	TD	*

\* Supplied by user.

\*\* Working variable.

\*\*\*  $E_1$  is defined as a function of time in Subroutine DFUNI.

SUBROUTINE CSEF(X,F)	CSE 10
=====	
* * * * *	CSE 20
* * * * *	CSE 30
* * * * *	CSE 40
* * * * *	CSE 50
* * * * *	CSE 60
* * * * *	CSE 70
* * * * *	CSE 80
* * * * *	CSE 90
--SUBROUTINES CALLED	
DVOGER  AN IMSLIB  SUBROUTINE	CSE 100
GEARSI  IS THE SAME AS DVOGER BUT WITH DIFFERENT NAME	CSE 110
GELG   AN SSPLIB SUBROUTINE FOR SOLVING SYSTEMS OF LINEAR	CSE 120
EQUATIONS	CSE 130
DCAN   A SUBROUTINE WHICH FINDS THE DC STEADY STATE SOLUTION	CSE 140
	CSE 150
DFUNI AND DFUNO ARE THE TWO SUBROUTINES SUPPLYING THE	CSE 160
DERIVATIVES OF THE INPUT AND OUTPUT STATE VARIABLES NECESSARY	CSE 170
FOR INTEGRATION	CSE 180
	CSE 190
X = ARRAY OF VARIABLES THEY ARE SCALED BY THE VECTOR SCALE	CSE 200
IN THIS SUBROUTINE THEY ARE E(4), ZO, R4, CO, ALPHA(3),	CSE 210
SATC(3), CEJ(3) AND TT(3)	CSE 220
	CSE 230
F = ARRAY OF RESPONSE AT EQUAL TIME STEPS GIVEN BY TMAX/120	CSE 240
	CSE 250
FF = ARRAY IN WHICH THE RESPONSE IS STORED AND THE MAXIMUM	CSE 260
NUMBER OF THE INTEGRATION STEPS IS LIMITED TO 1500	CSE 270
	CSE 280
R = WORKING AREA TO STORE THE R MATRIX	CSE 290
	CSE 300
YI, YIMAX, ERI AND WKI ARE THE WORKING ARRAYS REQUIRED BY	CSE 310
THE INTEGRATION SUBROUTINE FOR THE 4 STATE VARIABLES INPUT	CSE 320
CIRCUIT	CSE 330
	CSE 340
YO, YOMAX, ERO AND WKO ARE CORRESPONDING ARRAYS FOR THE 3	CSE 350
STATE VARIABLES OUTPUT CIRCUIT	CSE 360
	CSE 370
ID1 = D21(IN TEXT)                  ARE DEFINED IN	CSE 380
ID2 = D11(IN TEXT)                  THE FOLLOWING	CSE 390
ID3 = D31(IN TEXT)                  DATA STATEMENTS	CSE 400
	CSE 410
AV, AC, B AND V ARE WORKING ARRAYS	CSE 420
	CSE 430
UI = WORKING ARRAY TO STORE INCIDENT VOLTAGES FOR THE T.L.	CSE 440
UR = WORKING ARRAY TO STORE REFLECTED VOLTAGES FOR THE T.L.	CSE 450
UITD AND URTD ARE CORRESPONDING VALUES OBTAINED BY LINEAR	CSE 460
INTERPOLATION BETWEEN THE DISCRETE VALUES IN UI AND UR	CSE 470
AT CERTAIN TIMES DETERMINED BY THE DELAY TIME TD	CSE 480
TIME AND TIMEI ARE ARRAYS TO STORE THE TIMES FOR THE OUTPUT	CSE 490
AND INPUT CIRCUITS, RESPECTIVELY, AT WHICH THE RESPONSES ARE	CSE 500
OBTAINED	CSE 510
	CSE 520
/MIMC/  CIRCUIT PARAMETERS	CSE 530
	CSE 540
/MIMT/  TRANSISTOR PARAMETERS	CSE 550
	CSE 560
/MIMD/  DIODE PARAMETERS	CSE 570
	CSE 580
/MIMTL/ TRANSMISSION-LINE PARAMETERS	CSE 590
	CSE 600
	CSE 610
	CSE 620
/MIME/  VOLTAGES DEFINING THE SHAPE OF THE INPUT E(1)	CSE 630
EU      UPPER VALUE OF E(1)	CSE 640
EB      LOWER VALUE OF E(1)	CSE 650
SL      SLOPE	CSE 660
	CSE 670
/MIMINT/ VARIABLES REQUIRED FOR THE INTEGRATION	CSE 680
HI      INPUT CIRCUIT INTEGRATION STEP	CSE 690
HO      OUTPUT CIRCUIT INTEGRATION STEP	CSE 700
HMIN    MINIMUM STEP ALLOWED	CSE 710
HMAX    MAXIMUM STEP ALLOWED	CSE 720
EPSI    AN ERROR CRITERION TO CHANGE THE ORDER OF	CSE 730



C		THE STEP IN THE INTEGRATION	CSE 740
C	SCALE	A VECTOR OF SCALING FACTORS FOR THE X VECTOR	CSE 750
C	TMAX	THE UPPER BOUND ON TIME UNTIL WHICH OUTPUT	CSE 760
C		RESPONSE IS REQUIRED	CSE 770
C	MOI	MAXIMUM ORDER ALLOWED TO BE USED IN THE	CSE 780
C		INTEGRATION	CSE 790
C		-----	CSE 800
C			CSE 810
C	*****	E X A M P L E	*****
C			CSE 820
C		THIS EXAMPLE ILLUSTRATES THE EVALUATION AND PLOTTING OF	CSE 830
C		OUTPUT RESPONSE	CSE 840
C			CSE 850
C		PROGRAM MIM ( INPUT, OUTPUT, TAPE5= INPUT, TAPE6=OUTPUT)	CSE 860
C		DIMENSION X(8), F(121)	CSE 870
C		COMMON/MIMT/ SATC(3), TT(3), THETA, TST(3), ALPHA(3), ASAT(3), CEJ(3)	CSE 880
C		+ , CC(3), RB(2)	CSE 890
C		COMMON/MIMC/ R1, R2, R3, R4, E(4), CO	CSE 900
C		COMMON/MIMTL/ Z0, TD, M, MS, MK, MI, MSI, MKI	CSE 910
C		COMMON/MIMD/ VD, SATD, TSD, TTD, CD	CSE 920
C		COMMON/MIME/ EU, EB, SL	CSE 930
C		COMMON/MIMINT/ HI, HO, HMIN, HMAX, EPSI, SCALE(8), TMAX, MOI	CSE 940
C		DATA SATD, TTD, CD/0.6E-9, 1.E-11, 0.12E-12/	CSE 950
C		DATA SATC(1), SATC(2), TT(1), TT(2), THETA, ALPHA(1), ALPHA(2), CEJ(1),	CSE 960
C		+CEJ(2), CC, RB/2*0.6E-9, 2*1.E-11, 38.668, 0.99, 0.99, 2*0.12E-12,	CSE 970
C		+3*0.5E-12, 2*50.0/	CSE 980
C		DATA R1, R2, R3, E(2), E(3)/281.33, 75., 78.24, -4.03, 1.13/	CSE 990
C		DATA EU, EB, SL/0.776, 1.552, -5.173333333333E9/	CSE1000
C		DATA TD/0.25E-9/	CSE1010
C		DATA SCALE/-1.7, 50., 50., 1.5E-12, 0.99, 0.6E-9, 0.12E-12, 1.E-11/	CSE1020
C		DATA X/0.97377, 1.8401, 0.910653, 0.832065, 4*1.0/	CSE1030
C		MOI=2	CSE1040
C		TMAX=1.44E-9	CSE1050
C		EPSI=0.005	CSE1060
C		HMAX=1.E-11	CSE1070
C		HMIN=1.E-17	CSE1080
C		HI=1.E-13	CSE1090
C		CALL CSEF(X, F)	CSE1100
C		DDT=TMAX/120.	CSE1110
C		WRITE(6, 100) (F(I), I=1, 121)	CSE1120
C		DO 50 I=1, 121	CSE1130
C		T=DDT*FLOAT(I)	CSE1140
C		ZZ=F(I)	CSE1150
C		CALL PLOTPT(T, ZZ, 4)	CSE1160
C	50	CONTINUE	CSE1170
C		CALL OUTPLT	CSE1180
C	100	FORMAT(10(2X, F8.4))	CSE1190
C		STOP	CSE1200
C		END	CSE1210
C			CSE1220
C			CSE1230
C			CSE1240
C		-----	CSE1250
C		EXTERNAL DFUNI, DFUNO	CSE1260
C			CSE1270
C		DIMENSION X(8), F(121), FF(1500)	CSE1280
C			CSE1290
C		DIMENSION R(5,5), YI(8,4), YO(8,3), YIMAX(4), YOMAX(3), ERI(4), ERO(3),	CSE1300
C		+WKI(84), WKO(60)	CSE1310
C			CSE1320
C		COMMON/MIMA/ ID1(4,5), ID2(4,5), ID3(5),	CSE1330
C		+ AV(4,4), AC(4,4), B(5,4), V(5),	CSE1340
C		+ UI(1500), UR(1500), UITD, URTD, TIME(1500), TIMEI(1500)	CSE1350
C			CSE1360
C		COMMON/MIMC/ R1, R2, R3, R4, E(4), CO	CSE1370
C			CSE1380
C		COMMON/MIMT/ SATC(3), TT(3), THETA, TST(3), ALPHA(3), ASAT(3), CEJ(3)	CSE1390
C		+ , CC(3), RB(2)	CSE1400
C			CSE1410
C		COMMON/MIMD/ VD, SATD, TSD, TTD, CD	CSE1420
C			CSE1430
C		COMMON/MIMTL/ Z0, TD, M, MS, MK, MI, MSI, MKI	CSE1440
C			CSE1450
C		COMMON/MIME/ EU, EB, SL	CSE1460
C			CSE1470





C	65 MKI=MSI	CSE2960
	MI=MI+1	CSE2970
	TIMEI(MI)=TI	CSE2980
	IF(IERI.EQ.34.OR.IERI.EQ.35) CALL EXIT	CSE2990
	JI=1	CSE3000
	CALL GEARS1(DFUNI, YI, TI, NI, MTI, MOI, JI, HI, HMIN, HMAX,	CSE3010
	+ EPSI, YIMAX, ERI, WKI, IERI)	CSE3020
	GO TO 60	CSE3030
C		CSE3040
C	---	CSE3050
C	LINEAR INTERPOLATION TO FIND RESPONSE AT INTERMEDIATE TIMES	---
C	TIME POINTS ARE EQUALLY SPACED BY DDT = TMAX/120	CSE3060
C		CSE3070
	70 MS=2	CSE3080
	M=M+1	CSE3090
	TIME(M)=TO	CSE3100
	FF(M)=YO(1,1)	CSE3110
	DDT=TMAX/120.	CSE3120
	DO 90 I=1,121	CSE3130
	T=DDT*(I-1)	CSE3140
	DO 75 J=MS,M	CSE3150
	JMS=J	CSE3160
	IF(TIME(J).GT.T) GO TO 80	CSE3170
	75 CONTINUE	CSE3180
	80 MS=JMS-1	CSE3190
	F(I)=(FF(JMS)*(T-TIME(MS))+FF(MS)*(TIME(JMS)-T))/	CSE3200
	+ (TIME(JMS)-TIME(MS))	CSE3210
	90 CONTINUE	CSE3220
C		CSE3230
	RETURN	CSE3240
	END	CSE3250
		CSE3260

C  
C  
C  
C  
C  
C  
C  
C  
C  
C

SUBROUTINE DFUNI(Y, T, MZM, DY, PW, IND)  
=====

DFU 10

THIS SUBROUTINE IS CALLED BY GEARS INTEGRATION SUBROUTINE  
IT SUPPLIES THE VALUES OF THE DERIVATIVES (DY) THE JACOBIAN  
(PW) FOR A POINT(Y, T) FOR THE INPUT CIRCUIT

DFU 20  
DFU 30  
DFU 40  
DFU 50

FOR FURTHER DETAILS, SEE COMMENTS IN THE INTEGRATION SUBROUTINE

DFU 60  
DFU 70

-----  
DIMENSION Y(8,4), DY(4), W(2,4), PW(MZM, MZM)  
COMMON/MIMA/ ID1(4,5), ID2(4,5), ID3(5),  
+ AV(4,4), AC(4,4), B(5,4), V(5),  
+ UI(1500), UR(1500), UITD, URTD, TIME(1500), TIMEI(1500)  
COMMON/MIMT/ SATC(3), TT(3), THETA, TST(3), ALPHA(3), ASAT(3), CEJ(3)  
+, CC(3), RB(2)  
COMMON/MIMC/ R1, R2, R3, R4, E(4), CO  
COMMON/MIME/ EU, EB, SL  
COMMON/MIMTL/ Z0, TD, M, MS, MK, MI, MSI, MKI

DFU 80  
DFU 90  
DFU 100  
DFU 110  
DFU 120  
DFU 130  
DFU 140  
DFU 150  
DFU 160  
DFU 170  
DFU 180  
DFU 190

W(1,1)=THETA\*Y(1,2)  
W(2,1)=THETA\*Y(1,3)  
DO 10 I=1,2  
W(I,2)=EXP(W(I,1))  
W(I,3)=SATC(I)\*W(I,2)-1.0  
W(I,4)=CEJ(I)+TST(I)\*W(I,2)  
10 CONTINUE  
PT=T-TD  
IF(PT.LT.0.0) GO TO 55  
DO 50 I=MK, M  
IMS=I  
IF(TIME(I).GT.PT) GO TO 52  
50 CONTINUE  
52 MS=IMS-1  
RATIO=(PT-TIME(MS))/(TIME(IMS)-TIME(MS))  
URTD=RATIO\*(UR(IMS)-UR(MS))+UR(MS)

DFU 200  
DFU 210  
DFU 220  
DFU 230  
DFU 240  
DFU 250  
DFU 260  
DFU 270  
DFU 280  
DFU 290  
DFU 300  
DFU 310  
DFU 320  
DFU 330  
DFU 340  
DFU 350  
DFU 360

--- THE INPUT VOLTAGE E(1) ---

DFU 370  
DFU 380

55 IF(T.LE.0.05E-9) E(1)=EU  
IF(T.GT.0.05E-9.AND.T.LT.0.2E-9) E(1)=EU-SL\*(T-0.05E-9)  
IF(T.GE.0.2E-9.AND.T.LE.0.45E-9) E(1)=EB  
IF(T.GT.0.45E-9.AND.T.LT.0.6E-9) E(1)=EB+SL\*(T-0.45E-9)  
IF(T.GE.0.6E-9.AND.T.LE.0.85E-9) E(1)=EU  
IF(T.GT.0.85E-9.AND.T.LT.1.E-9) E(1)=EU-SL\*(T-0.85E-9)  
IF(T.GE.1.E-9.AND.T.LE.1.25E-9) E(1)=EB  
IF(T.GT.1.25E-9.AND.T.LT.1.4E-9) E(1)=EB+SL\*(T-1.25E-9)  
IF(T.GE.1.4E-9) E(1)=EU

DFU 390  
DFU 400  
DFU 410  
DFU 420  
DFU 430  
DFU 440  
DFU 450  
DFU 460  
DFU 470  
DFU 480  
DFU 490

DO 20 I=1,3  
V(I)=E(I)  
20 CONTINUE  
V(4)=-URTD  
DO 30 I=1,4  
DY(I)=0.0  
DO 30 J=1,4  
DY(I)=DY(I)+AV(I,J)\*V(J)+AC(I,J)\*Y(1,J)

DFU 500  
DFU 510  
DFU 520  
DFU 530  
DFU 540  
DFU 550

30 CONTINUE  
DY(1)=DY(1)+ALPHA(1)\*W(1,3)  
DY(2)=DY(2)-W(1,3)  
VL=-Y(1,1)-RB(1)\*((1.-ALPHA(1))\*W(1,3)+DY(1)+DY(2))-E(1)  
CIZ=VL/R3+ALPHA(1)\*W(1,3)-DY(1)  
UI(MI)=VL-CIZ\*Z0

DFU 560  
DFU 570  
DFU 580  
DFU 590  
DFU 600  
DFU 610  
DFU 620

C

DY(1)=DY(1)/CC(1)  
DY(2)=DY(2)/W(1,4)  
DY(3)=(DY(3)-W(2,3))/W(2,4)  
DY(4)=(DY(4)+ALPHA(2)\*W(2,3))/CC(2)  
IF(IND.NE.1) RETURN  
PW(1,1)=AC(1,1)/CC(1)  
PW(1,2)=(AC(1,2)+ASAT(1)\*THETA\*W(1,2))/CC(1)  
PW(1,3)=AC(1,3)/CC(1)  
PW(1,4)=AC(1,4)/CC(1)  
PW(2,1)=AC(2,1)/W(1,4)

DFU 630  
DFU 640  
DFU 650  
DFU 660  
DFU 670  
DFU 680  
DFU 690  
DFU 700  
DFU 710  
DFU 720  
DFU 730

PW(2,2)=(AC(2,2)-THETA*W(1,2)*(SATC(1)+TST(1)*DY(2)))/W(1,4)	DFU 740
PW(2,3)=AC(2,3)/W(1,4)	DFU 750
PW(2,4)=AC(2,4)/W(1,4)	DFU 760
PW(3,1)=AC(3,1)/W(2,4)	DFU 770
PW(3,2)=AC(3,2)/W(2,4)	DFU 780
PW(3,3)=(AC(3,3)-THETA*W(2,2)*(SATC(2)+TST(2)*DY(3)))/W(2,4)	DFU 790
PW(3,4)=AC(3,4)/W(2,4)	DFU 800
PW(4,1)=AC(4,1)/CC(2)	DFU 810
PW(4,2)=AC(4,2)/CC(2)	DFU 820
PW(4,3)=(AC(4,3)+ASAT(2)*THETA*W(2,2))/CC(2)	DFU 830
PW(4,4)=AC(4,4)/CC(2)	DFU 840
RETURN	DFU 850
END	DFU 860

C  
C  
C  
C  
C  
C  
C  
C  
C  
C  
C

SUBROUTINE DFUNO(Y, T, MZM, DY, PW, IND) DFU 10  
=====

THIS SUBROUTINE IS CALLED BY GEARS INTEGRATION SUBROUTINE DFU 20  
IT SUPPLIES THE VALUES OF THE DERIVATIVES (DY) THE JACOBIAN DFU 30  
(PW) FOR A POINT(Y, T) FOR THE OUTPUT CIRCUIT DFU 40  
DFU 50  
DFU 60

FOR FURTHER DETAILS, SEE COMMENTS IN THE INTEGRATION SUBROUTINE DFU 70

-----  
DIMENSION Y(8, 3), DY(3), W(4), PW(MZM, MZM, WD(4)) DFU 100  
COMMON/MIMA/ ID1(4, 5), ID2(4, 5), ID3(5), DFU 110  
+ AV(4, 4), AC(4, 4), B(5, 4), V(5), DFU 120  
+ UI(1500), UR(1500), UITD, URTD, TIME(1500), TIMEI(1500) DFU 130  
COMMON/MIMT/ SATC(3), TT(3), THETA, TST(3), ALPHA(3), ASAT(3), CEJ(3) DFU 140  
+ , CC(3), RB(2) DFU 150  
COMMON/MIMC/ R1, R2, R3, R4, E(4), CO DFU 160  
COMMON/MIMTL/ Z0, TD, M, MS, MK, MI, MSI, MKI DFU 170  
COMMON/MIMD/ VD, SATD, TSD, TTD, CD DFU 180  
DFU 190

W(1)=THETA\*Y(1, 2) DFU 200  
W(2)=EXP(W(1)) DFU 210  
W(3)=SATC(3)\*(W(2)-1.0) DFU 220  
W(4)=CEJ(3)+TST(3)\*W(2) DFU 230  
WD(1)=THETA\*Y(1, 3) DFU 240  
WD(2)=EXP(WD(1)) DFU 250  
WD(3)=SATD\*(WD(2)-1.0) DFU 260  
WD(4)=CD+TSD\*WD(2) DFU 270

PT=T-TD DFU 280  
IF(PT.LT.0.0) GO TO 30 DFU 290  
DO 10 I=MKI, MI DFU 300  
IMS=I DFU 310  
IF(TIMEI(I).GT.PT) GO TO 20 DFU 320

10 CONTINUE DFU 330  
20 MSI=IMS-1 DFU 340  
RATIO=(PT-TIMEI(MSI))/(TIMEI(IMS)-TIMEI(MSI)) DFU 350  
UITD=UI(MSI)+RATIO\*(UI(IMS)-UI(MSI)) DFU 360  
DFU 370

30 V(1)=E(4) DFU 380  
V(2)=-UITD DFU 390  
V(3)=Y(1, 1) DFU 400  
V(4)=Y(1, 2) DFU 410  
V(5)=Y(1, 3) DFU 420  
DY(1)=ALPHA(3)\*W(3) DFU 430  
CIZ=W(3)-DY(1) DFU 440  
DY(2)=-CIZ DFU 450  
DY(3)=DY(1)-WD(3) DFU 460  
DO 40 I=1, 3 DFU 470  
DO 40 J=1, 5 DFU 480  
DY(I)=DY(I)+B(J, I)\*V(J) DFU 490

40 CONTINUE DFU 500  
VL=V(3)+V(4)+V(5) DFU 510  
CIZ=CIZ+DY(2) DFU 520  
UR(M)=VL-CIZ\*Z0 DFU 530  
DY(1)=DY(1)/CO DFU 540  
DY(2)=DY(2)/W(4) DFU 550  
DY(3)=DY(3)/WD(4) DFU 560  
DFU 570  
IF(IND.NE.1) RETURN DFU 580

C PW(1, 1)=B(3, 1)/CO DFU 590  
PW(1, 2)=(B(4, 1)+ASAT(3)\*THETA\*W(2))/CO DFU 600  
PW(1, 3)=B(5, 1)/CO DFU 610  
PW(2, 1)=B(3, 2)/W(4) DFU 620  
PW(2, 2)=(B(4, 2)-THETA\*W(2)\*(SATC(3)-ASAT(3)+TST(3)\*DY(2)))/W(4) DFU 630  
PW(2, 3)=B(5, 2)/W(4) DFU 640  
PW(3, 1)=B(3, 3)/WD(4) DFU 650  
PW(3, 2)=(B(4, 3)+ASAT(3)\*THETA\*W(2))/WD(4) DFU 660  
PW(3, 3)=(B(5, 3)-THETA\*WD(2)\*(SATD+TSD\*DY(3)))/WD(4) DFU 670  
RETURN DFU 680  
END DFU 690  
DFU 700

```

SUBROUTINE DCAN(VE1,VE2,VE3,VC1,VC2,VO,UI,UR)
=====
THIS SUBROUTINE EVALUATES THE STEADY STATE VALUES OF
VE1,VE2,VE3, VC1,VC2, VO, UI, UR.

AN INITIAL GUESS FOR VE1, VE2 AND VE3 SHOULD BE SUPPLIED
ALL CIRCUIT AND MODEL PARAMETERS ARE ALSO SUPPLIED THROUGH
THE COMMON STATEMENTS
THEY ARE CIRCUIT PARAMETERS IN /MIMC/, TRANSISTOR PARAMETERS IN
/MIMT/, TRANS. LINE PARAMETERS IN /MIMTL/ AND DIODE PARAMETERS
IN /MIMD/
-----
DIMENSION TX(2),EX(2),G(2,2),GINV(2,2),DX(2)
COMMON/MIMT/ SATC(3),TT(3),THETA,TST(3),ALPHA(3),ASAT(3),CEJ(3)
+,CC(3),RB(2)
COMMON/MIMC/ R1,R2,R3,R4,E(4),CO
COMMON/MIMTL/ Z0,TD,M,MS,MK,MI,MSI,MKI
COMMON/MIMD/ VD,SATD,TSD,TTD,CD

STEADY STATE SOLUTION FOR INPUT

B1=SATC(1)*R1
B2=SATC(2)*R1
A1=B1+(1.-ALPHA(1))*SATC(1)*RB(1)
A2=B2+(1.-ALPHA(2))*SATC(2)*RB(2)
NIT=0
10 TX(1)=THETA*VE1
TX(2)=THETA*VE2
DO 20 I=1,2
EX(I)=EXP(TX(I))
20 CONTINUE
F1=A1*(EX(1)-1.)+B2*(EX(2)-1.)+VE1+E(2)+E(1)
F2=A2*(EX(2)-1.)+B1*(EX(1)-1.)+VE2+E(2)+E(3)
G(1,1)=A1*THETA*EX(1)+1.0
G(1,2)=B2*THETA*EX(2)
G(2,1)=B1*THETA*EX(1)
G(2,2)=A2*THETA*EX(2)+1.0
DET=G(1,1)*G(2,2)-G(1,2)*G(2,1)
GINV(1,1)=G(2,2)/DET
GINV(2,1)=-G(2,1)/DET
GINV(1,2)=-G(1,2)/DET
GINV(2,2)=G(1,1)/DET
DO 30 I=1,2
DX(I)=-GINV(I,1)*F1-GINV(I,2)*F2
30 CONTINUE
VE1=VE1+DX(1)
VE2=VE2+DX(2)
NIT=NIT+1
IF(NIT.GT.1000) GO TO 90
IF(ABS(DX(1)).GT.1.E-10.OR.ABS(DX(2)).GT.1.E-10) GO TO 10
GO TO 100
90 WRITE(6,300)
CALL EXIT
100 CONTINUE
CE1=SATC(1)*(EXP(THETA*VE1)-1.0)
CC1=ALPHA(1)*CE1
CE2=SATC(2)*(EXP(THETA*VE2)-1.0)
CC2=ALPHA(2)*CE2
VC2=R2*CC2-E(3)-RB(2)*(CE2-CC2)

STEADY STATE SOLUTION FOR OUTPUT

A=R4+R3*(1.-ALPHA(3))
B=R3*CC1+E(4)
NIT=0
CT=SATC(3)/SATD
Y=VE3
40 EY=EXP(THETA*Y)
CE3=SATC(3)*(EY-1.0)
VD=ALOG(CT*(EY-1.0)+1.0)/THETA

```

DCA 10  
DCA 20  
DCA 30  
DCA 40  
DCA 50  
DCA 60  
DCA 70  
DCA 80  
DCA 90  
DCA 100  
DCA 110  
DCA 120  
DCA 130  
DCA 140  
DCA 150  
DCA 160  
DCA 170  
DCA 180  
DCA 190  
DCA 200  
DCA 210  
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DCA 590  
DCA 600  
DCA 610  
DCA 620  
DCA 630  
DCA 640  
DCA 650  
DCA 660  
DCA 670  
DCA 680  
DCA 690  
DCA 700  
DCA 710  
DCA 720  
DCA 730



```
DY=- (A*CE3+B+Y+VD)/(A*THETA*EY*SATC(3)+1.+CT*(EY*EXP(-THETA*VD))) DCA 740
Y=Y+DY DCA 750
NIT=NIT+1 DCA 760
IF(NIT.GT.1000) GO TO 190 DCA 770
IF(ABS(DY).GT.1.E-10) GO TO 40 DCA 780
GO TO 200 DCA 790
190 WRITE(6,400) DCA 800
CALL EXIT DCA 810
200 CONTINUE DCA 820
EY=EXP(THETA*Y) DCA 830
VE3=Y DCA 840
CE3=SATC(3)*(EY-1.) DCA 850
C DCA 860
C CALCULATION OF VC1, VC2, VO, UI, AND UR DCA 870
C DCA 880
VD=ALOG(CT*(EY-1.)+1.)/THETA DCA 890
VO=R4*CE3+E(4) DCA 900
VR=Y+VD+VO DCA 910
VI=VR DCA 920
DELTA=Z0*(1.-ALPHA(3))*CE3 DCA 930
UI=VI+DELTA DCA 940
UR=VR-DELTA DCA 950
VC1=- (1.-ALPHA(1))*RB(1)*CE1-E(1)-VI DCA 960
300 FORMAT(//,5X,*DC SOLUTION ONE WAS NOT OBTAINED*) DCA 970
400 FORMAT(//,5X,*DC SOLUTION TWO WAS NOT OBTAINED*) DCA 980
RETURN DCA 990
END DCA1000
```



SOC-192

STATE EQUATION ANALYSIS AND COMPUTER PROGRAM FOR A CURRENT SWITCH  
EMITTER FOLLOWER

H.L. Abdel-Malek and J.W. Bandler

April 1978,           No. of Pages: 31

Revised:

Key Words:           Nonlinear circuit analysis, state equation formulation,  
                          integration methods

Abstract:    The analysis of a current switch emitter follower (CSEF)  
circuit originally given by Ho is described. State equations in  
conjunction with Gear's integration method are used to obtain the output  
response.

Description:        Contains Fortran listing, user's manual.  
                          The listing contains 586 cards, of which 235 are  
                          comment cards.

Related Work:       SOC-182, SOC-184, SOC-185.

Price:             \$15.00.

