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YIELD OPTIMIZATION FOR ARBITRARY STATISTICAL DISTRIBUTIONS

PART II: IMPLEMENTATION

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Abstract A suggested test problem for proposed algorithms in yield optimization is described in detail. The problem is a current switch emitter follower (CSEF) circuit originally described by Ho, which includes a transmission line. The ideas presented in Part I of this paper [1] are applied to this circuit in order to obtain an optimal statistical design. Production yield is maximized taking into consideration statistical distributions of circuit parameters and realistic correlations between transistor model parameters. Nonlinear programming employing the analytical formulas for yield and its sensitivities is used to provide optimal nominal values for the circuit parameters. Different design specifications are assumed and corresponding optimal designs are obtained.

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I. INTRODUCTION

Need is growing for test problems in the area of yield optimization. Several test problems, such as the Karafin filter [2-5], the LC lowpass filter [6,7] and the two-section transmission-line transformer [6,8], have been used by researchers both for demonstrating and for comparing proposed algorithms for tolerance assignment, design centering, yield analysis and optimization techniques. However, no such problem has been developed in the available literature in sufficient detail for comparing proposed techniques which take explicitly into account statistical distributions and possible correlations in providing an optimal design center.

Yield optimization has been considered by Elias [9] and by Becker and Jensen [10] using the Monte Carlo method of yield analysis. It was also considered by Bandler and Abdel-Malek [8] using linear cuts but for uniform distribution of outcomes between tolerance extremes. It has been recently considered indirectly by Brayton, Hachtel and Director [11] using the simplicial approximation.

A current switch emitter follower circuit which was previously investigated by Ho [12] in the context of sensitivity calculations is chosen for implementing the ideas presented in Part I [1] of this paper. A detailed description of the circuit is given in Section II. Felt to be a worthwhile preliminary exercise to statistical design, an optimal worst-case design is carried out in Section III [8]. Sparsity is exploited in developing the quadratic models for the constraints.

Correlations between transistor model parameters through formulas based on work published by Balaban and Golembeski [13] are established

in Section IV. According to these correlations, weights to be assigned to the orthocells are computed (see Part I of this paper). Production yield is maximized employing analytical formulas for yield and its sensitivities as well as the quadratic approximations to the design constraints. It is shown how different design specifications can be investigated and corresponding optimal yields obtained without any additional circuit simulations.

An appendix (to aid future work by other researchers) describing the derivation of the state equations used in analyzing the CSEF circuit is provided.

II. ANALYSIS OF THE CSEF

The circuit is shown in Fig. 1. The decoupled equivalent circuit of the transmission line is used [14]. Considering a lossless transmission line and the charge-control model of the transistors as well as the diode the circuit is shown in Fig. 2. The following two equations are used for the transmission-line model.

$$u_i(t) = [e_0(t-\tau) + Z_0\, i_0(t-\tau)]\, U(t-\tau) + \Phi_i(t),$$
$$u_r(t) = [e_\ell(t-\tau) + Z_0\, i_\ell(t-\tau)]\, U(t-\tau) + \Phi_r(t),$$

where Z_0 and τ are the characteristic impedance and the delay time of the transmission line, respectively, U is the step function given by

$$U(t-\tau) = \begin{cases} 0 & t < \tau\ , \\ 1 & t \geq \tau\ . \end{cases}$$

The parameter Φ represents the initial voltage distribution stored on the transmission line. Thus, we take

$$\Phi_i(t) = \Phi_r(t) = 0 \quad \text{for } t \geq \tau \ .$$

The original circuit parameters and model parameters are given in Table I. The state equations are formulated as described in the Appendix.

The subroutine CSEF [15] solves for the equilibrium, steady state solution which supplies initial values of the states in the subsequent integration. The subroutine DVOGER [16], based on Gear's integration algorithm [17], called from CSEF, is used for solving the state equations. The algorithm has a variable step and hence interpolation was used to find the values of $u_i(t)$ and $u_r(t)$ if $t - \tau$ falls between time steps. Alternatively, τ/n, where n is an integer can be used as a fixed step, however, integration will be expensive. Our analysis has been verified independently by the companion network approach [18].

III. WORST-CASE DESIGN OF THE CSEF

The parameter vector considered for a worst-case design (see Fig. 2) is

$$\underset{\sim}{\phi} = \begin{bmatrix} E_4 \\ Z_0 \\ R_4 \\ C_0 \end{bmatrix} .$$

The corresponding tolerances are denoted by ϵ_1, ϵ_2, ϵ_3 and ϵ_4. Fig. 3 shows the input voltage E_1 and the time point constraints used. The response obtained with the parameter values in Table I are also shown.

The circuit is initially at equilibrium with $E_1 = -0.776$ V.

Starting at the nominal parameter values given in Table I, the approximation to the design constraints was carried out by solving the system of equations (36) of Part I using the program MODEL4 [19]. The base points were obtained by equation (30) of Part I with

$$\underset{\sim}{\bar{\phi}} = \begin{bmatrix} 1.7 \\ 50.0 \\ 50.0 \\ 1.5 \end{bmatrix}, \qquad \underset{\sim}{\delta} = \begin{bmatrix} 0.17 \\ 5.00 \\ 5.00 \\ 0.15 \end{bmatrix}$$

and

$$\underset{\sim}{B} = \left[\begin{array}{ccc|cc|c} -0.2 & 0.6 & 0.5 & 0 & 0 & 0 \\ \hline -0.3 & 0 & 0 & -1.0 & -0.5 & 0 \\ 0 & -0.5 & 0 & 1.0 & 0 & 0.2 \\ 0 & 0 & 0.5 & 0 & 0.4 & 0.4 \end{array}\right].$$

The values of the constraints g_i are obtained from the circuit response and the specifications shown in Fig. 3 using the program CSEF [15]. Each constraint g_i is described by a quadratic polynomial P_i having 15 coefficients.

The nonlinear program formulated to solve the worst-case design problem [8] is

$$\underset{\underset{\sim}{\phi}^0,\ \underset{\sim}{\varepsilon}}{\text{minimize}}\ E_4^0/\varepsilon_1 + Z_0^0/\varepsilon_2 + R_4^0/\varepsilon_3 + C_0^0/\varepsilon_4$$

subject to

$$P_i(\underset{\sim}{\phi}^r) \geq 0,\ r = 1, 2, \ldots, 2^4,$$

$$i = 1, 2, \ldots, 7,$$

where $\underset{\sim}{\phi}^r$ indicates a vertex of the tolerance orthotope as given by

equation (8) of Part I. The output capacitor C_0 was constrained such that

$$C_0^0 - \epsilon_4 \geq 1.0 \text{ pF}.$$

This constraint was designed to prevent an unrealistic nominal value.

This nonlinear program was transformed into a minimax problem using the Bandler-Charalambous technique [20]. The program FLOPT4 [21] was used to solve the resulting minimax problem and the program QPE [19] was used for calculating the quadratic polynomials at the vertices. The optimum nominal point obtained was far from the center of interpolation $\bar{\underset{\sim}{\phi}}$. In order to have a reliable approximation, the time point constraints were reapproximated around the obtained nominal $\underset{\sim}{\phi}^0$, i.e., the new center of interpolation is

$$\bar{\underset{\sim}{\phi}} = \underset{\sim}{\phi}^0 = \begin{bmatrix} 1.70 \\ 95.00 \\ 45.00 \\ 1.35 \end{bmatrix}.$$

Again, the base points were obtained by equation (30) of Part I using the same $\underset{\sim}{B}$ matrix given before and with

$$\underset{\sim}{\delta} = \begin{bmatrix} 0.17 \\ 14.25 \\ 9.0 \\ 0.3375 \end{bmatrix}.$$

The nonlinear program was solved employing the updated approximations. The optimal worst-case nominal parameters and

tolerances are shown in Table II. The nominal design response as well as the responses for the critical vertices, numbered according to equation (9) of Part I, are shown in Fig. 3.

A single interpolation region was found to be satisfactory. The difference between the predicted responses at vertices according to the approximations and the actual responses subsequently checked by integration was, over the sample points used, less than 2%.

For the worst-case design obtained the power dissipated in the output circuit is 0.1854 mW at the nominal solution. It is 0.365 mW for the original design at equilibrium when $E_1 = -0.776$. This saves power and limits fluctuations in chip temperature.

IV. STATISTICAL DESIGN OF THE CSEF

The output section of the CSEF circuit was optimally designed to provide maximum yield. The statistical distributions of the circuit parameters and the transistor model parameters were assumed to be fixed. The nominal values of the output circuit parameters were optimized in order to obtain maximum yield.

The statistical distributions of the transistor T_3 model parameters are based upon results published by Butler [22] and by Balaban and Golembeski [13]. The transistor current gain β was assumed to have a triangular probability distribution function with a peak at $\beta = 60$ and $40 \leq \beta \leq 100$, as illustrated in Fig. 4. Correlation between transistor model parameters (see Table I(c)) was established according to the following equations

$$I_S = 0.0061\ \beta\ (1 + 0.3516\ X_{r1})\ x\ 10^{-9}\ A\ ,$$
$$C_{JE} = (0.144 - 0.242\ x\ 10^{-3}\beta)\ (1 + 0.2\ X_{r2})\ pF\ ,$$
$$TT = 0.01\ (1 + 0.2\ X_{r3})\ ns,$$

where X_{ri} are independent uniformly distributed random numbers over the range

$$-1 \leq X_{ri} \leq 1,\ i = 1, 2, 3.$$

The discretized joint probability density functions of the common base current gain $\alpha = \beta/(\beta+1)$ and I_S and that of α and C_{JE} are shown in Fig. 5 and Fig. 6, respectively. The numerical coefficients in each of these equations were obtained by preserving the ratios of the corresponding coefficients of Balaban and Golembeski [13] and, at the same time, ensuring that they lead to the same nominal values we have. According to these distributions the weights and intervals for the discretized distribution were determined and are shown in Table III. As a matter of fact the weights should be available from the sampled data used in formulating these equations.

The circuit parameters were assumed to have the distributions

$$E_4 = E_4^0 + 0.1632\ X_{r4}\ ,$$
$$Z_0 = Z_0^0 + 9.5\ X_{r5}\ ,$$
$$R_4 = R_4^0 + 4.4\ X_{r6}\ ,$$
$$C_0 = C_0^0 + 0.27\ X_{r7}\ ,$$

where, again,

$$-1 \leq X_{ri} \leq 1\ ,\quad i = 4, 5, 6, 7\ .$$

The nonlinear programming problem to be solved is

$$\underset{\underset{\sim}{\phi}^0}{\text{maximize}} \quad Y$$

subject to

$$C_0^0 \geq 1.27 \text{ pF},$$

$$Z_0^0 \leq Z_{0u},$$

where Z_{0u} is an upper bound on the characteristic impedance of the transmission line and

$$\underset{\sim}{\phi}^0 = \begin{bmatrix} E_4^0 \\ Z_0^0 \\ R_4^0 \\ C_0^0 \end{bmatrix}.$$

The production yield Y is calculated using equations (61) and (53) of Part I. The linear cuts are obtained from the quadratic approximations to the design constraints

$$V_0(t) \leq -1.45 \text{ V}, \quad t = 0.3 \text{ ns},$$

$$V_0(t) \geq -0.85 \text{ V}, \quad t = 0.62, \ 0.69, \ 0.8 \text{ ns},$$

$$V_0(t) \leq -1.40 \text{ V}, \quad t = 1,02, \ 1.09, \ 1.2 \text{ ns},$$

using equation (42) of Part I, where

$$\underset{\sim}{\phi}^{a} = \begin{bmatrix} \underset{\sim}{\phi}^{0} \\ \alpha_3 \\ I_{S3} \\ C_{JE3} \\ TT_3 \end{bmatrix} .$$

The value of $\underset{\sim}{\phi}^{0}$ is varying as determined during the optimization process while the remaining parameters have the fixed values given in Table IV.

A single quadratic approximation to the design constraints was carried out at the interpolation region defined by the center and size shown in Table IV. The base points are obtained from equation (30) of Part I, where $\underset{\sim}{B}$ is given by equation (31) of Part I and where

$$\underset{\sim}{u}_7 = \begin{bmatrix} -0.2 \\ -0.5 \\ 0.5 \\ -0.7 \\ 0.2 \\ -0.6 \\ 0.8 \end{bmatrix}, \quad \underset{\sim}{T}_7 = \begin{bmatrix} -0.3 & & & & & & \\ & 0.6 & & & & & \\ & & 0.5 & & & & \\ & & & 0.5 & & & \\ & & & & 0.3 & & \\ & & & & & 0.4 & \\ & & & & & & -0.6 \end{bmatrix},$$

$$\underset{\sim}{u}_6 = \begin{bmatrix} -1.0 \\ -0.5 \\ 0.2 \\ 0.3 \\ -0.5 \\ -0.7 \end{bmatrix}, \quad \underset{\sim}{T}_6 = \begin{bmatrix} 1.0 & & & & & & \\ & 0.4 & & & & & \\ & & 0.8 & & & & \\ & & & 0.8 & & & \\ & & & & 0.5 & & \\ & & & & & -0.5 & \end{bmatrix},$$

$$\underset{\sim}{u}_5 = \begin{bmatrix} 0.2 \\ 0.3 \\ 0.6 \\ -0.7 \\ 0.8 \end{bmatrix}, \quad \underset{\sim}{T}_5 = \begin{bmatrix} 0.4 & & & & \\ & -0.5 & & & \\ & & -0.7 & & \\ & & & 0.6 & \\ & & & & -1.0 \end{bmatrix},$$

$$\underset{\sim}{u}_4 = \begin{bmatrix} 0.2 \\ -0.6 \\ 0.5 \\ 0.8 \end{bmatrix}, \quad \underset{\sim}{T}_4 = \begin{bmatrix} 0.6 & & & \\ & 0.7 & & \\ & & -0.6 & \\ & & & 0.3 \end{bmatrix},$$

$$\underset{\sim}{u}_3 = \begin{bmatrix} 1.0 \\ -1.0 \\ 1.0 \end{bmatrix}, \quad \underset{\sim}{T}_3 = \begin{bmatrix} -0.8 & & \\ & -1.0 & \\ & & 1.0 \end{bmatrix},$$

$$\underset{\sim}{u}_2 = \begin{bmatrix} 1.0 \\ -0.9 \end{bmatrix}, \quad \underset{\sim}{T}_2 = \begin{bmatrix} 0.6 & \\ & -1.0 \end{bmatrix},$$

$$\underset{\sim}{u}_1 = [1.0], \quad \underset{\sim}{T}_1 = [-1.0] \quad .$$

The number of response evaluations required in order to obtain these approximations is 45. This is the same as the number of coefficients of the quadratic polynomial, see equation (20) of Part I, for this 8-dimensional problem.

The weight assigned for each orthocell is obtained by multiplying the corresponding weight resulting from the correlations between the transistor model parameters, given in Table III, by the weights for the remaining uniformly distributed independent parameters. For a uniformly distributed parameter we have

$$w_i(0) = w_i(2) = 0.0,$$
$$w_i(1) = 1.0 \ .$$

The yield sensitivities required during optimization are evaluated using equation (69) of Part I.

The results obtained for two different upper bounds on the characteristic impedance Z_0 are shown in Table V. These results may be compared with those obtained from 1000 Monte Carlo points, generated according to the assumed statistical distribution in conjunction with the quadratic approximations. The resulting yields are also tabulated in Table V and the nominal responses at the starting point and at the optimal solution are shown in Fig. 7.

In order to further demonstrate the benefits of having an approximation, different specifications were assumed and the corresponding yield optimiztions were carried out. The specified switching levels were varied as tabulated in Table VI and hence the corresponding constraints are simply generated by changing the constant term in the quadratic approximations. The resulting optimum yields and corresponding nominal values for the circuit parameters are given in Table VI.

The design constraints at t = 1.02 ns and at t = 1.09 ns were found to be overlapping. This is simply discovered by checking the reference vertices and the corresponding distances from them to the points of intersection of the linear cuts with the orthotope edges which are given by equations (43) and (45) of Part I, respectively. The constraint at t = 1.02 ns was removed from the optimization process since it has the same reference vertex as the constraint at t = 1.09 and its contribution to the weighted nonfeasible hypervolume is negligible.

V. CONCLUSIONS

Yield optimization of the CSEF circuit has been successfully performed. It has been demonstrated how small a number of simulations

is required: 75 integrations for the whole investigation. A summary of the effort is shown in Table VII. This number of simulations is much smaller than the number of Monte Carlo analyses, used in such a case, to provide even a single yield estimate let alone a complete optimization. Less than one second was required to carry out a complete yield and yield sensitivity evaluation, while more than 1.5 seconds are generally required for only one numerical integration using Gear's method.

Having approximations to the design constraints allowed us to consider different design specifications without any additional circuit simulations as seen from Table VII. Furthermore, different statistical distributions can be investigated. Similar transistors manufactured under different physical conditions, for example, can be readily investigated for optimum yield without additional integrations.

Finally, the reader may be interested in a recent review [23] of the authors' approach involving linear cuts based on quadratic approximations with the simplicial approximation approach originally devised by Director and Hachtel [24,25].

APPENDIX

TOPOLOGICAL FORMULATION OF THE STATE EQUATIONS FOR THE CSEF CIRCUIT

The basic steps required in the formulation of the state equations for nonlinear networks are sketched out. For further details see Chua and Lin [26].

Step 1 Formation and characterization of network branches

This step involves the characterization of linear and nonlinear elements, controlled and independent sources and tree and cotree (link) branches. The choice of the tree branches is based upon

(i) all independent and controlled voltage sources,

(ii) as many capacitors as possible,

(iii) as many resistors as possible,

(iv) as few inductors as possible,

(v) no independent current sources.

Step 2 Solving the resistive nonlinear subnetwork

We solve for the voltages across the nonlinear resistors in the tree as well as the currents in the nonlinear resistors in the cotree.

Step 3 Solving the loops which include capacitors only and the cutsets which include inductors only

In this step we express the currents in the cotree capacitors and the voltages across the tree inductors in terms of the derivatives (w.r.t. time) of the tree capacitor voltages and the cotree inductor currents. Also, they may well be functions of the derivatives of voltages of the tree independent voltage sources and derivatives of currents of cotree independent current sources (if these derivatives exist).

Step 4 Collecting relationships derived so far to formulate the state equations.

Regarding the CSEF circuit shown in Fig. 2, the input and output circuits can be treated independently.

A.1 Formulation of the State Equations for the Input Circuit

The tree chosen according to the priorities mentioned before is shown in Fig. A.1. According to this tree, the set of independent KCL equations is

$$\underset{\sim}{D}\ \underset{\sim}{i} = \underset{\sim}{0}\ , \tag{A.1}$$

where

$$\underset{\sim}{i} = \begin{bmatrix} \underset{\sim}{I}_{ET} \\ \underset{\sim}{I}_{CT} \\ \underset{\sim}{I}_{RT} \\ \underset{\sim}{I}_{RL} \\ \underset{\sim}{I}_{JL} \end{bmatrix}, \tag{A.2}$$

$$\underset{\sim}{I}_{ET} \triangleq \text{Tree voltage source currents} = \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix}, \tag{A.3}$$

$$\underset{\sim}{I}_{CT} \triangleq \text{Tree capacitor currents} = \begin{bmatrix} I_5 \\ I_6 \\ I_7 \\ I_8 \end{bmatrix}, \tag{A.4}$$

$$\underset{\sim}{I}_{RT} \triangleq \text{Tree resistor currents} = [I_9]\ , \tag{A.5}$$

$$\underset{\sim}{I}_{RL} \triangleq \text{Link resistor currents} = \begin{bmatrix} I_{10} \\ I_{11} \\ I_{12} \\ I_{13} \\ I_{14} \end{bmatrix}, \tag{A.6}$$

$$\underset{\sim}{I}_{JL} \triangleq \text{Link current sources} = \begin{bmatrix} I_{15} \\ I_{16} \\ I_{17} \\ I_{18} \end{bmatrix} \tag{A.7}$$

and where

$$\underset{\sim}{D} = \left[\begin{array}{ccccc|ccccc|cc} 1 & & & & & & & -1 & & & & \\ & 1 & & & & -1 & 1 & -1 & -1 & -1 & & \\ & & \cdot & & & & & & -1 & & & \\ & & & \cdot & & & & & & -1 & & \\ & & & & \cdot & & & & & & & \\ \hline & & & & & & -1 & & & 1 & -1 & \\ & & & & & & 1 & -1 & & -1 & 1 & \\ & & & & & -1 & & & -1 & & & 1 \\ & & & & & 1 & & & & & & -1 \\ \hline & & & & 1 & -1 & 1 & -1 & -1 & -1 & & \end{array}\right] . \tag{A.8}$$

Hence, we can write (A.1) as

$$\left[\begin{array}{ccc|cc} & & & \underset{\sim}{D}_{11} & \underset{\sim}{D}_{12} \\ & \underset{\sim}{\mathbb{1}}_9 & & \underset{\sim}{D}_{21} & \underset{\sim}{D}_{22} \\ & & & \underset{\sim}{D}_{31} & \underset{\sim}{D}_{32} \end{array}\right] \begin{bmatrix} \underset{\sim}{I}_{ET} \\ \underset{\sim}{I}_{CT} \\ \underset{\sim}{I}_{RT} \\ \underset{\sim}{I}_{RL} \\ \underset{\sim}{I}_{JL} \end{bmatrix} = \underset{\sim}{0} , \tag{A.9}$$

where

$$\underset{\sim}{D}_{11} = \begin{bmatrix} & & -1 & & \\ -1 & 1 & -1 & -1 & -1 \\ & & & -1 & \\ & & & & -1 \end{bmatrix} , \tag{A.10}$$

$$\underset{\sim}{D}_{12} = \underset{\sim}{0} , \tag{A.11}$$

$$\underset{\sim}{D}_{21} = \begin{bmatrix} & -1 & & & 1 \\ & 1 & -1 & & -1 \\ -1 & & & -1 & \\ 1 & & & & \end{bmatrix} , \tag{A.12}$$

$$\underset{\sim}{D}_{22} = \begin{bmatrix} & -1 & & \\ 1 & & & \\ & & 1 & \\ & & & -1 \end{bmatrix} , \tag{A.13}$$

$$\underset{\sim}{D}_{31} = [-1 \quad 1 \quad -1 \quad -1 \quad -1] , \tag{A.14}$$

$$\underset{\sim}{D}_{32} = \underset{\sim}{0} . \tag{A.15}$$

and $\underset{\sim}{1}_9$ is the identity matrix of order 9.

The KVL equations can be written as

$$\left[\begin{array}{ccc|c} \underset{\sim}{D}_{11}^T & \underset{\sim}{D}_{21}^T & \underset{\sim}{D}_{31}^T & \\ \underset{\sim}{D}_{12}^T & \underset{\sim}{D}_{22}^T & \underset{\sim}{D}_{32}^T & -\underset{\sim}{1}_9 \end{array}\right] \begin{bmatrix} \underset{\sim}{V}_{ET} \\ \underset{\sim}{V}_{CT} \\ \underset{\sim}{V}_{RT} \\ \underset{\sim}{V}_{RL} \\ \underset{\sim}{V}_{JL} \end{bmatrix} = \underset{\sim}{0} , \tag{A.16}$$

where superscript T denotes transposition.

It is required to represent the link currents $\underset{\sim}{I}_{RL}$ in terms of $\underset{\sim}{V}_{ET}$ and $\underset{\sim}{V}_{CT}$. We have

$$\underset{\sim}{V}_{RL} = \underset{\sim}{R}_L \, \underset{\sim}{I}_{RL}$$

$$= \underset{\sim}{D}_{11}^T \, \underset{\sim}{V}_{ET} + \underset{\sim}{D}_{21}^T \, \underset{\sim}{V}_{CT} + \underset{\sim}{D}_{31}^T \, \underset{\sim}{V}_{RT} , \tag{A.17}$$

where

$$\underset{\sim}{R}_L = \begin{bmatrix} R_2 & & & & & \\ & R_3 & & & & \\ & & R_{B1} & & & \\ & & & R_{B2} & & \\ & & & & Z_0 & \end{bmatrix} . \tag{A.18}$$

Using (A.9) and (A.15) we can write

$$\underset{\sim}{I}_{RT} = -\underset{\sim}{D}_{31}\ \underset{\sim}{I}_{RL} - \underset{\sim}{D}_{32}\ \underset{\sim}{I}_{JL}$$

$$= -\underset{\sim}{D}_{31}\ \underset{\sim}{I}_{RL} \ . \qquad \text{(A.19)}$$

Thus,

$$\underset{\sim}{V}_{RT} = \underset{\sim}{R}_T\ \underset{\sim}{I}_{RT} = -\ \underset{\sim}{R}_T\ \underset{\sim}{D}_{31}\ \underset{\sim}{I}_{RL} \ , \qquad \text{(A.20)}$$

where

$$\underset{\sim}{R}_T = [R_1] \ . \qquad \text{(A.21)}$$

Substituting for $\underset{\sim}{V}_{RT}$ in (A.17) and with some manipulations, we obtain

$$\underset{\sim}{I}_{RL} = \underset{\sim}{R}^{-1}\ [\underset{\sim}{D}_{11}^T\ \underset{\sim}{V}_{ET} + \underset{\sim}{D}_{21}^T\ \underset{\sim}{V}_{CT}] \ , \qquad \text{(A.22)}$$

where

$$\underset{\sim}{R} = \underset{\sim}{R}_L + \underset{\sim}{D}_{31}^T\ \underset{\sim}{R}_T\ \underset{\sim}{D}_{31} \ . \qquad \text{(A.23)}$$

From (A.5), we have

$$\underset{\sim}{I}_{CT} = -\underset{\sim}{D}_{21}\ \underset{\sim}{I}_{RL} - \underset{\sim}{D}_{22}\ \underset{\sim}{I}_{JL} \ . \qquad \text{(A.24)}$$

Substituting for $\underset{\sim}{I}_{RL}$ from (A.22), the state equations are

$$\underset{\sim}{I}_{CT} = -\underset{\sim}{D}_{21}\ \underset{\sim}{R}^{-1}\ [\underset{\sim}{D}_{11}^T\ \underset{\sim}{V}_{ET} + \underset{\sim}{D}_{21}^T\ \underset{\sim}{V}_{CT}] - \underset{\sim}{D}_{22}\ \underset{\sim}{I}_{JL} \ . \qquad \text{(A.25)}$$

More explicitly, they can be written as

$$\begin{bmatrix} C_{C1} & dV_{C1}/dt \\ C_{E1} & dV_{BE1}/dt \\ C_{E2} & dV_{BE2}/dt \\ C_{C2} & dV_{C2}/dt \end{bmatrix} = -\underset{\sim}{D}_{21}\ \underset{\sim}{R}^{-1} \left[\underset{\sim}{D}_{11}^T \begin{bmatrix} E_1 \\ E_2 \\ E_3 \\ u_r \end{bmatrix} + \underset{\sim}{D}_{21}^T \begin{bmatrix} V_{C1} \\ V_{BE1} \\ V_{BE2} \\ V_{C2} \end{bmatrix} \right] + \begin{bmatrix} I_{16} \\ -I_{15} \\ -I_{17} \\ I_{18} \end{bmatrix}, \qquad \text{(A.26)}$$

where

$$C_{E1} = C_{JE} + TT\ \theta\ I_S \exp(\theta\ V_{BE1}) \ , \tag{A.27}$$

$$C_{E2} = C_{JE} + TT\ \theta\ I_S \exp(\theta\ V_{BE2}) \ , \tag{A.28}$$

$$I_{15} = I_S(\exp(\theta\ V_{BE1})-1) \ , \tag{A.29}$$

$$I_{16} = \alpha\ I_{15} \ , \tag{A.30}$$

$$I_{17} = I_S(\exp(\theta\ V_{BE2})-1) \ , \tag{A.31}$$

$$I_{18} = \alpha\ I_{17} \ . \tag{A.32}$$

A.2 Formulation of the State Equations for the Output Circuit

Figure A.2 shows the chosen tree and branch numbering. The set of independent KCL equations is

$$\underset{\sim}{D}\ \underset{\sim}{i} = \underset{\sim}{0} \ , \tag{A.33}$$

where

$$\underset{\sim}{D} = \left[\begin{array}{ccccc|cccc} 1 & & & & & -1 & & & \\ & 1 & & & & & -1 & & \\ & & 1 & & & 1 & -1 & -1 & \\ & & & 1 & & & -1 & 1 & -1 \\ & & & & 1 & & -1 & -1 & 1 \end{array}\right] , \tag{A.34}$$

$$\underset{\sim}{i} = \left[\begin{array}{c} \underset{\sim}{I}_{ET} \\ \underset{\sim}{I}_{CT} \\ \underset{\sim}{I}_{RL} \\ \underset{\sim}{I}_{JL} \end{array}\right] , \tag{A.35}$$

$$\underset{\sim}{I}_{ET} \triangleq \text{Tree voltage source currents} = \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}, \tag{A.36}$$

$$\underset{\sim}{I}_{CT} \triangleq \text{Tree capacitor currents} = \begin{bmatrix} I_3 \\ I_4 \\ I_5 \end{bmatrix}, \tag{A.37}$$

$$\underset{\sim}{I}_{RL} \triangleq \text{Link resistor currents} = \begin{bmatrix} I_6 \\ I_7 \end{bmatrix}, \tag{A.38}$$

$$\underset{\sim}{I}_{JL} \triangleq \text{Link current sources} = \begin{bmatrix} I_8 \\ I_9 \\ I_{10} \end{bmatrix}. \tag{A.39}$$

The KVL equations are

$$\left[\begin{array}{cccc|ccccc} -1 & & 1 & & & -1 & & & \\ & -1 & -1 & -1 & -1 & & -1 & & \\ & & & 1 & & & & -1 & \\ & & -1 & -1 & -1 & & & & -1 \\ & & & & 1 & & & & -1 \end{array}\right] \begin{bmatrix} \underset{\sim}{V}_{ET} \\ \underset{\sim}{V}_{CT} \\ \underset{\sim}{V}_{RL} \\ \underset{\sim}{V}_{JL} \end{bmatrix} = \underset{\sim}{0}, \tag{A.40}$$

Hence,

$$\begin{aligned} \underset{\sim}{V}_{RL} &= \underset{\sim}{R}_L \, \underset{\sim}{I}_{RL} \\ &= \underset{\sim}{D}_{11}^T \, \underset{\sim}{V}_{ET} + \underset{\sim}{D}_{21}^T \, \underset{\sim}{V}_{CT}, \end{aligned} \tag{A.41}$$

where

$$\underset{\sim}{R}_L = \begin{bmatrix} R_4 & \\ & Z_0 \end{bmatrix}, \tag{A.42}$$

$$\underset{\sim}{D}_{11} = \begin{bmatrix} -1 & \\ & -1 \end{bmatrix}, \tag{A.43}$$

$$\underset{\sim}{D}_{21} = \begin{bmatrix} 1 & -1 \\ & -1 \\ & -1 \end{bmatrix} . \tag{A.44}$$

Thus,

$$\underset{\sim}{I}_{RL} = \underset{\sim}{R}_L^{-1} \left[\underset{\sim}{D}_{11}^T \underset{\sim}{V}_{ET} + \underset{\sim}{D}_{21}^T \underset{\sim}{V}_{CT}\right] . \tag{A.45}$$

From (A.33), we have

$$\underset{\sim}{I}_{ET} = -\underset{\sim}{D}_{11} \underset{\sim}{I}_{RL} \tag{A.46}$$

and

$$\underset{\sim}{I}_{CT} = -\underset{\sim}{D}_{21} \underset{\sim}{I}_{RL} - \underset{\sim}{D}_{22} \underset{\sim}{I}_{JL} . \tag{A.47}$$

Substituting for $\underset{\sim}{I}_{RL}$ from (A.45) into (A.47), the state equations are

$$\underset{\sim}{I}_{CT} = -\underset{\sim}{D}_{21} \underset{\sim}{R}_L^{-1} \left[\underset{\sim}{D}_{11}^T \underset{\sim}{V}_{ET} + \underset{\sim}{D}_{21}^T \underset{\sim}{V}_{CT}\right] - \underset{\sim}{D}_{22} \underset{\sim}{I}_{JL} . \tag{A.48}$$

Or, more explicitly, the state equations are

$$\begin{bmatrix} C_0 & dV_0/dt \\ C_{E3} & dV_{BE3}/dt \\ C_D & dV_D/dt \end{bmatrix} = -\underset{\sim}{D}_{21} \begin{bmatrix} 1/R_4 & \\ & 1/Z_0 \end{bmatrix} \left[\underset{\sim}{D}_{11}^T \underset{\sim}{D}_{21}^T\right] \begin{bmatrix} E_4 \\ u_i \\ V_0 \\ V_{BE3} \\ V_D \end{bmatrix} + \begin{bmatrix} I_9 \\ I_9 - I_8 \\ I_9 - I_{10} \end{bmatrix}, \tag{A.49}$$

where

$$C_{E3} = C_{JE} + TT\ \theta\ I_S \exp(\theta\ V_{BE3}) , \tag{A.50}$$

$$C_D = C_{JD} + TT_D\ \theta\ I_{SD} \exp(\theta\ V_D) , \tag{A.51}$$

$$I_8 = I_S\ (\exp(\theta\ V_{BE3}) - 1) , \tag{A.52}$$

$$I_9 = \alpha\ I_8 , \tag{A.53}$$

$$I_{10} = I_{SD} \, (\exp(\theta \, V_D)-1) \, . \qquad (A.54)$$

If the diode is similar to the transistor base emitter junction, then

$$V_D = V_{BE3} \qquad (A.55)$$

and

$$I_{10} = I_8 \, . \qquad (A.56)$$

Hence, the three state equations (A.49) can be reduced to the following two equations

$$\begin{bmatrix} C_0 & dV_0/dt \\ C_{E3} & dV_{BE3}/dt \end{bmatrix} = \begin{bmatrix} -1 & 1 \\ & 1 \end{bmatrix} \begin{bmatrix} 1/R_4 & \\ & 1/Z_0 \end{bmatrix} + \begin{bmatrix} -1 & & 1 & \\ & -1 & -1 & -2 \end{bmatrix} \begin{bmatrix} E_4 \\ u_i \\ V_0 \\ V_{BE3} \end{bmatrix} + \begin{bmatrix} I_9 \\ I_9 - I_8 \end{bmatrix} \, . \qquad (A.57)$$

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TABLE I(a)

CIRCUIT PARAMETER VALUES

R_1	281.33 Ω
R_2	75.00 Ω
R_3	78.24 Ω
R_4	50.00 Ω
E_2	4.03 V
E_3	1.13 V
E_4	1.70 V
C_0	1.50 pF

TABLE I(b)

DIODE MODEL PARAMETERS

I_{SD}	diode saturation current	0.6×10^{-9} A
C_{JD}	depletion layer capacitance	0.12 pF
TT_D	transit time	0.01 ns
θ	inverse of thermal potential	38.668 V^{-1}

$$I_D = I_{SD}(\exp(\theta V_D)-1)$$

$$C_D = C_{JD} + TT_D \frac{dI_D}{dV_D}$$

TABLE I(c)

TRANSISTOR MODEL PARAMETERS

I_S	saturation current	0.6×10^{-9} A
α	common base current gain	0.99
R_B	base resistance	50.0 Ω
C_C	collector junction capacitance	0.5 pF
C_{JE}	emitter junction depletion layer capacitance	0.12 pF
TT	base transit time	0.01 ns
θ	inverse of thermal potential	$38.668\ V^{-1}$

$$I_E = I_S\ (\exp(\theta V_{BE})-1)$$

$$I_C = \alpha\ I_E$$

$$C_E = C_{JE} + TT\ \frac{dI_E}{dV_{BE}}$$

R_B and C_C are assumed zero for transistor T_3

TABLE I(d)

TRANSMISSION LINE PARAMETERS

Z_0	characteristic impedance	50 Ω
τ	delay time	0.25 ns

TABLE II

WORST-CASE DESIGN FOR THE CSEF CIRCUIT

E_4^0 (V)	Z_0^0 (Ω)	R_4^0 (Ω)	C_0^0 (pF)	ε_1/E_4^0 (%)	ε_2/Z_0^0 (%)	ε_3/R_4^0 (%)	ε_4/C_0^0 (%)
1.655	92.004	45.533	1.248	4.46	8.29	13.77	14.00

Objective cost function $\sum_{i=1}^{4} \phi_i^0/\varepsilon_i$

Number of complete response evaluations = 30

CDC modeling time = 48 s

CDC time (approximation and optimization) = 103 s

TABLE III

RESULTING WEIGHTS DUE TO CORRELATION BETWEEN β, I_S AND C_{JE}

β		α*		I_S $\epsilon^{**}_{I_S,i} = 0.221\times10^{-9}$ A			C_{JE} $\epsilon^{**}_{C_{JE},i} = 0.0218$ pF		
ϵ_{β,i_β}	w	$\epsilon_{\alpha,i_\alpha}$	w	w_1	w_2	w_3	w_1	w_2	w_3
20.0	0.3333	0.0080	0.3333	0.8320	0.1680	0.0000	0.2345	0.4084	0.3571
20.0	0.5000	0.0041	0.5000	0.3599	0.6113	0.0288	0.3174	0.4258	0.2568
20.0	0.1667	0.0024	0.1667	0.0744	0.5731	0.3525	0.4059	0.4472	0.1469

* $\alpha = \beta/(\beta+1)$

** Equal intervals for I_S and C_{JE} are considered

Lower extremes of the parameters are $\beta = 40.0$, $\alpha = 0.9756$, $I_S = 0.1582\times10^{-9}$ A and $C_{JE} = 0.0958$ pF

TABLE IV

INTERPOLATION REGION SIZE AND CENTER

FOR THE CSEF EXAMPLE

	E_4 (V)	Z_0 (Ω)	R_4 (Ω)	C_0 (pF)	α_3	I_{S3} (10^{-9}A)	C_{JE3} (pF)	TT_3 (ns)
$\bar{\phi}$	1.632	95.0	44.0	1.35	0.98285	0.49135	0.1285	0.0100
δ	0.170	15.0	10.0	0.45	0.00786	0.34400	0.0380	0.0025

TABLE V

RESULTS FOR THE MAXIMIZATION OF YIELD

FOR THE CSEF CIRCUIT

Description	E_4^0 (V)	Z_0^0 (Ω)	R_4^0 (Ω)	C_0^0 (pF)	Optimization time (s)	Yield (%)	
						Linear Cut	M.C.
Starting values	1.632	95.00	44.00	1.35	-	25.7	39.4
Optimum for Z_{Ou} = 100 Ω	1.595	100.00	51.15	1.27	67.8	58.6	68.9
Optimum for Z_{Ou} = 105 Ω	1.638	105.00	53.07	1.27	40.6	85.6	89.1

CDC modeling time = 74 s

CDC time required for M.C. employing approximation ≈ 5 s

TABLE VI

YIELD OPTIMIZATION FOR DIFFERENT SPECIFICATIONS

Specifications		E_4^0	Z_0^0	R_4^0	C_0^0	Yield (%)
a	b	(V)	(Ω)	(Ω)	(pF)	Linear Cut
-1.450	-0.900	1.657	90.00	51.84	1.27	65.1
-1.425	-0.925	1.652	90.00	48.95	1.27	91.4
-1.400	-0.950	1.637	90.00	44.91	1.27	99.7

$V_0(t) \leq$ a V, t = 0.3, 1.02, 1.09, 1.2 ns

$V_0(t) \geq$ b V, t = 0.62, 0.69, 0.8 ns

Z_{0u} = 90 Ω

TABLE VII

SUMMARY OF EFFORT FOR THE CSEF

Optimization problem	Number of simulations	Number of yield evaluations	CDC time	
			modeling	optimization
worst-case	30	0	48 s	55 s
yield	75	49	122 s	96 s
perturbed constraints and specifications	0	~ 50	0	~ 45 s

FIGURE CAPTIONS

Fig. 1 The CSEF circuit [12].

Fig. 2 The CSEF equivalent circuit used, indicating transmission line, transistor and diode models.

Fig. 3 Original, nominal and worst-case responses of the CSEF.

Fig. 4 Assumed distribution for the transistor current gain β.

Fig. 5 Illustration of the assumed discretized joint distribution of the transistor common base current gain α and the saturation current I_S. Appropriate weights of Table III divided by the corresponding cell area give the values of the PDF.

Fig. 6 Illustration of the assumed discretized joint distribution of the transistor common base current gain α and the emitter junction depletion layer capacitance C_{JE}. Appropriate weights of Table III divided by the corresponding cell area give the values of the PDF.

Fig. 7 Nominal responses of the CSEF corresponding to the 39% yield and 89% yield entries of Table V.

Fig. A.1 Directed graph of the input circuit and branch numbering.

____ Tree chosen

---- Corresponding link

Fig. A.2 Directed graph of the output circuit and branch numbering.

____ Tree chosen

---- Corresponding link

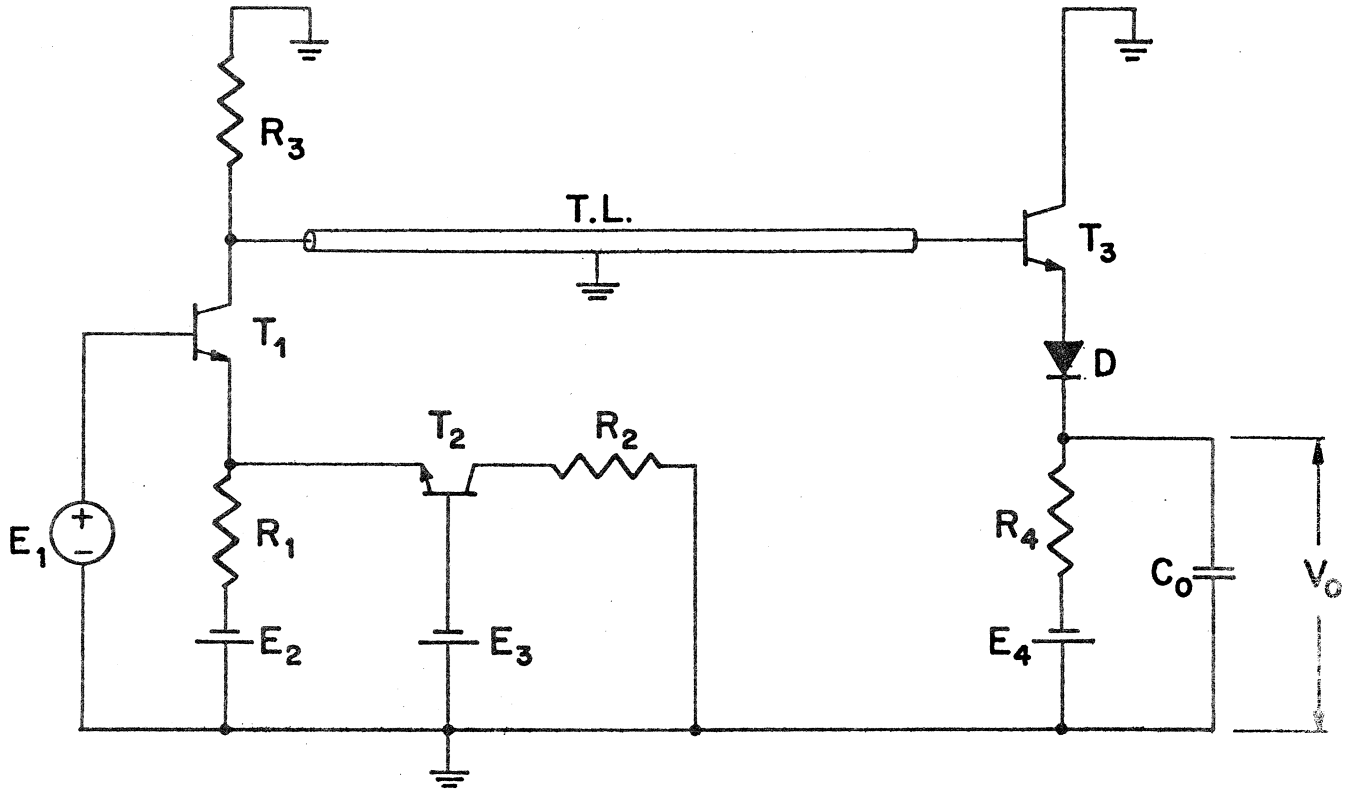


Fig. 1

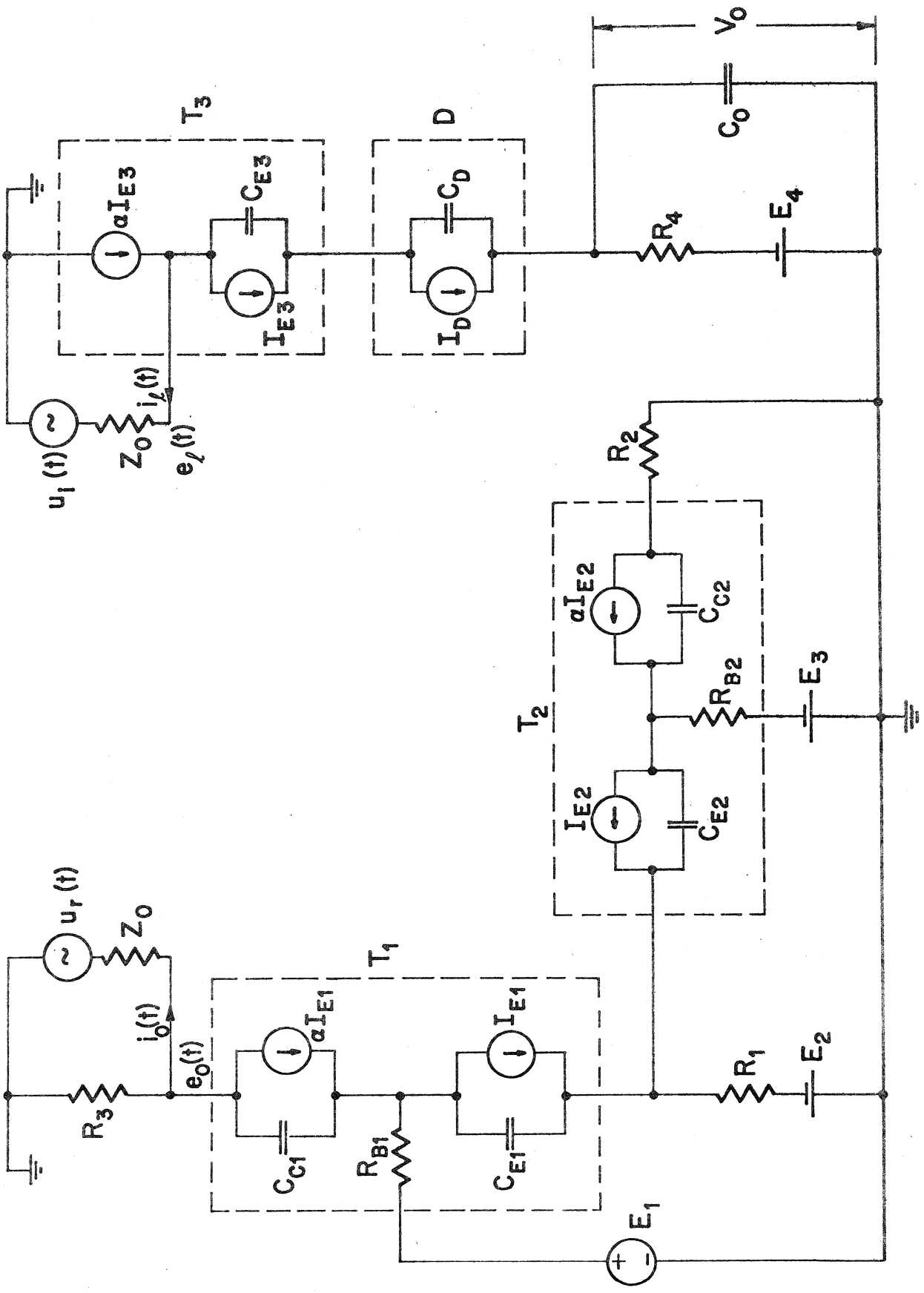
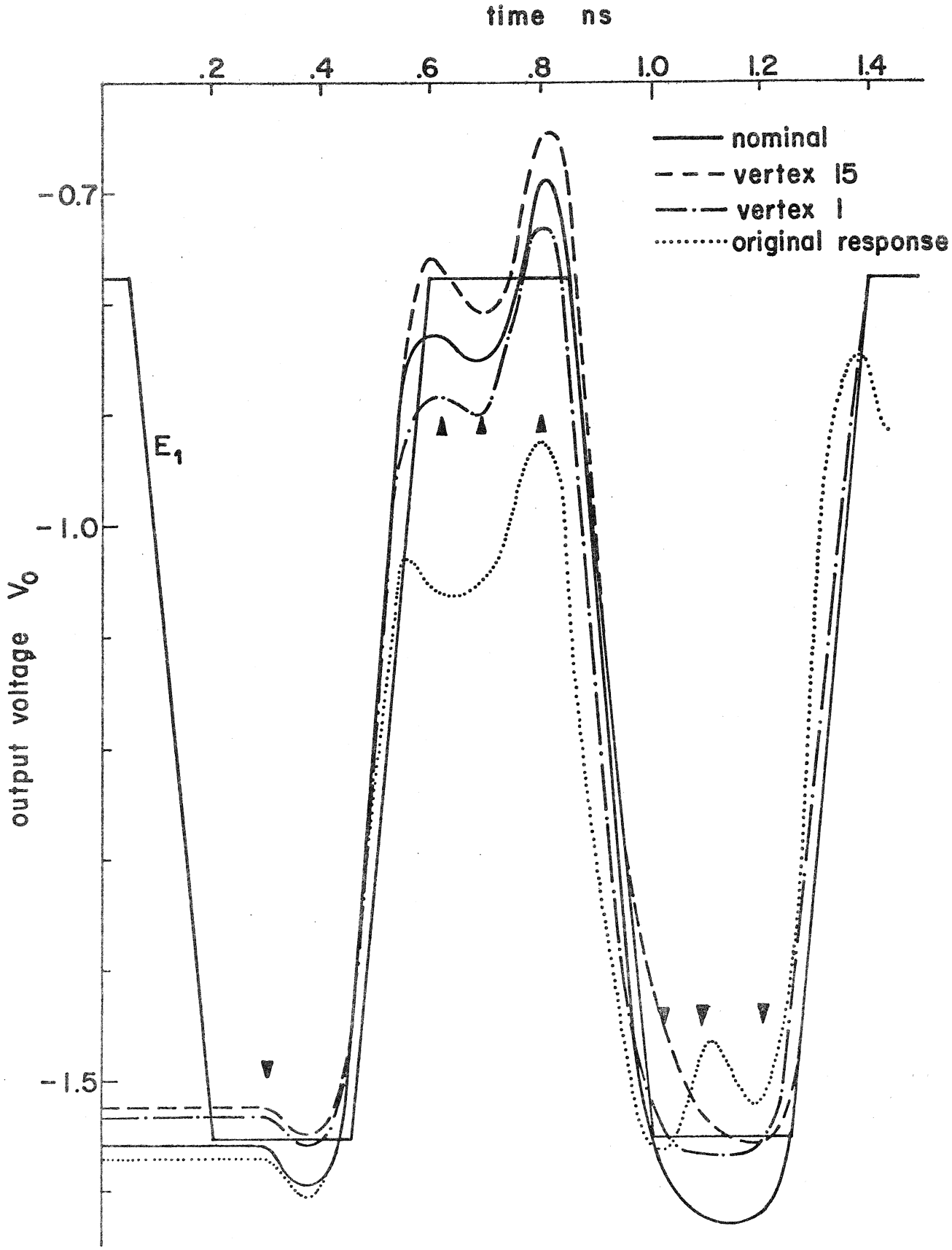

V_o
C_o
T_3
D
αI_{E3}
C_{E3}
I_{E3}
C_D
I_D
R_4
E_4
$u_l(t)$
Z_o
$i_l(t)$
$e_l(t)$
R_2
αI_{E2}
C_{C2}
T_2
R_{B2}
E_3
I_{E2}
C_{E2}
$u_r(t)$
Z_o
T_1
$i_o(t)$
$e_o(t)$
αI_{E1}
I_{E1}
R_3
C_{C1}
R_{B1}
C_{E1}
R_1
E_2
E_1

Fig. 2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.4
.6
.8
1.0
1.2
1.4
nominal
vertex 15
vertex 1
original response
-0.7
-1.0
-1.5
E1
output voltage Vo

Fig. 3

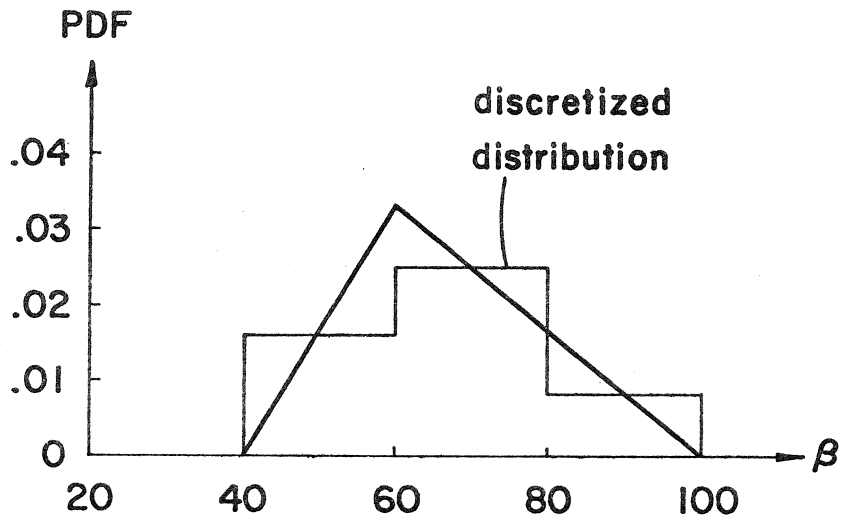


Fig. 4

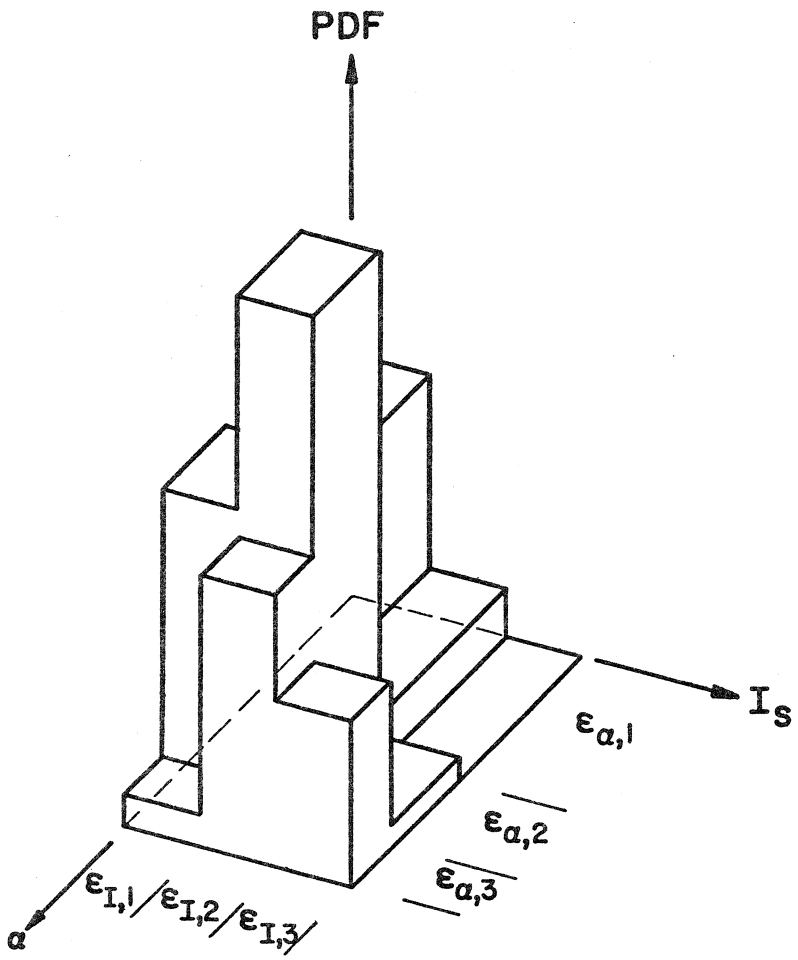

PDF
I_S
$\varepsilon_{\alpha,1}$
$\varepsilon_{\alpha,2}$
$\varepsilon_{\alpha,3}$
α
$\varepsilon_{I,1}$ $\varepsilon_{I,2}$ $\varepsilon_{I,3}$

Fig. 5

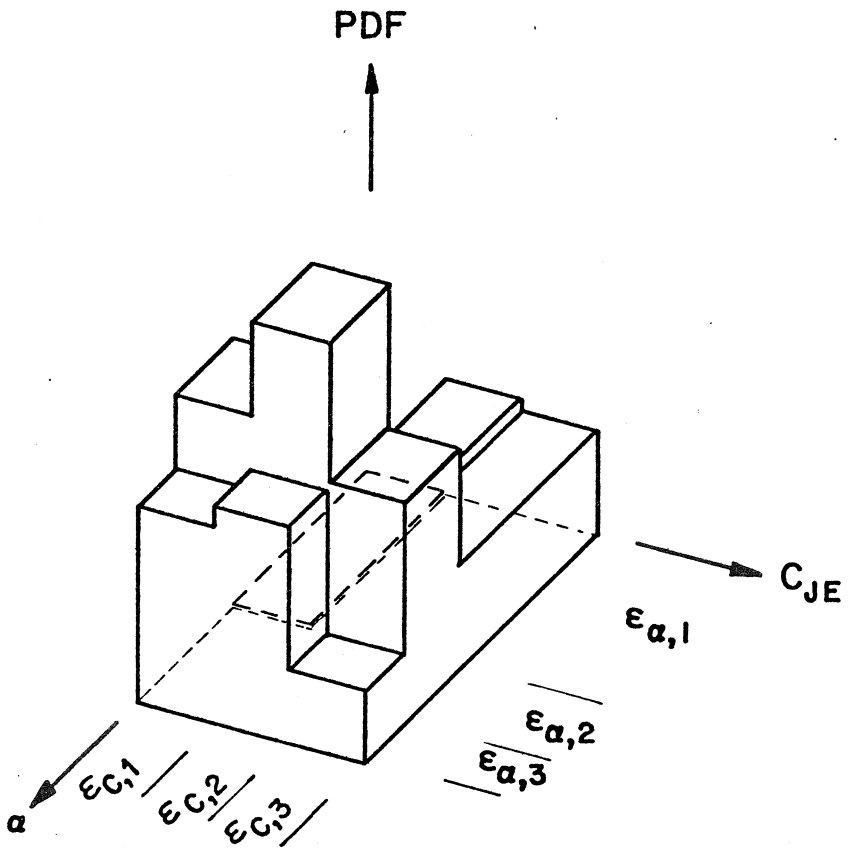

PDF
C_{JE}
$\varepsilon_{\alpha,1}$
$\varepsilon_{\alpha,2}$
$\varepsilon_{\alpha,3}$
α
$\varepsilon_{C,1}$
$\varepsilon_{C,2}$
$\varepsilon_{C,3}$

Fig. 6

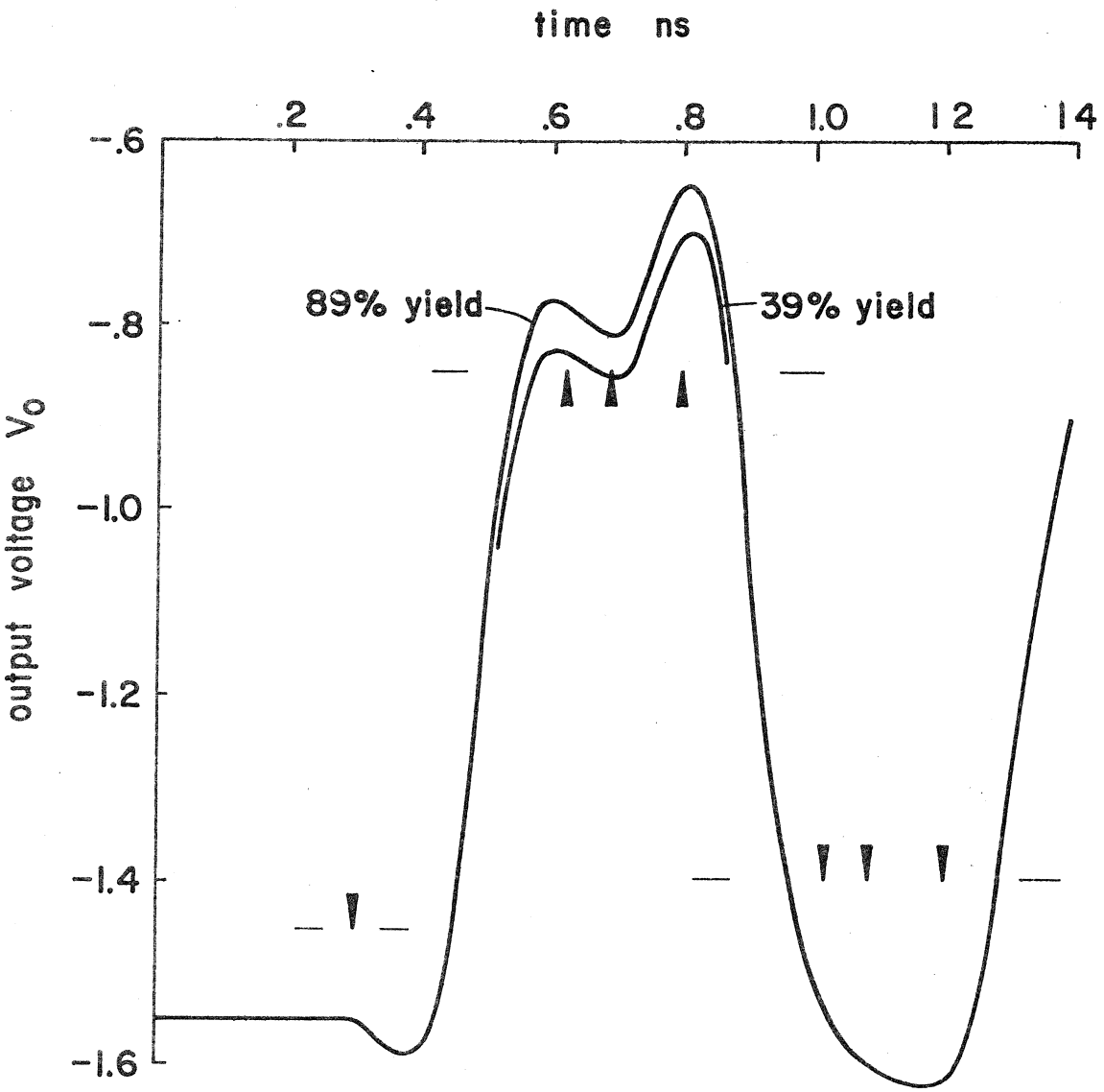
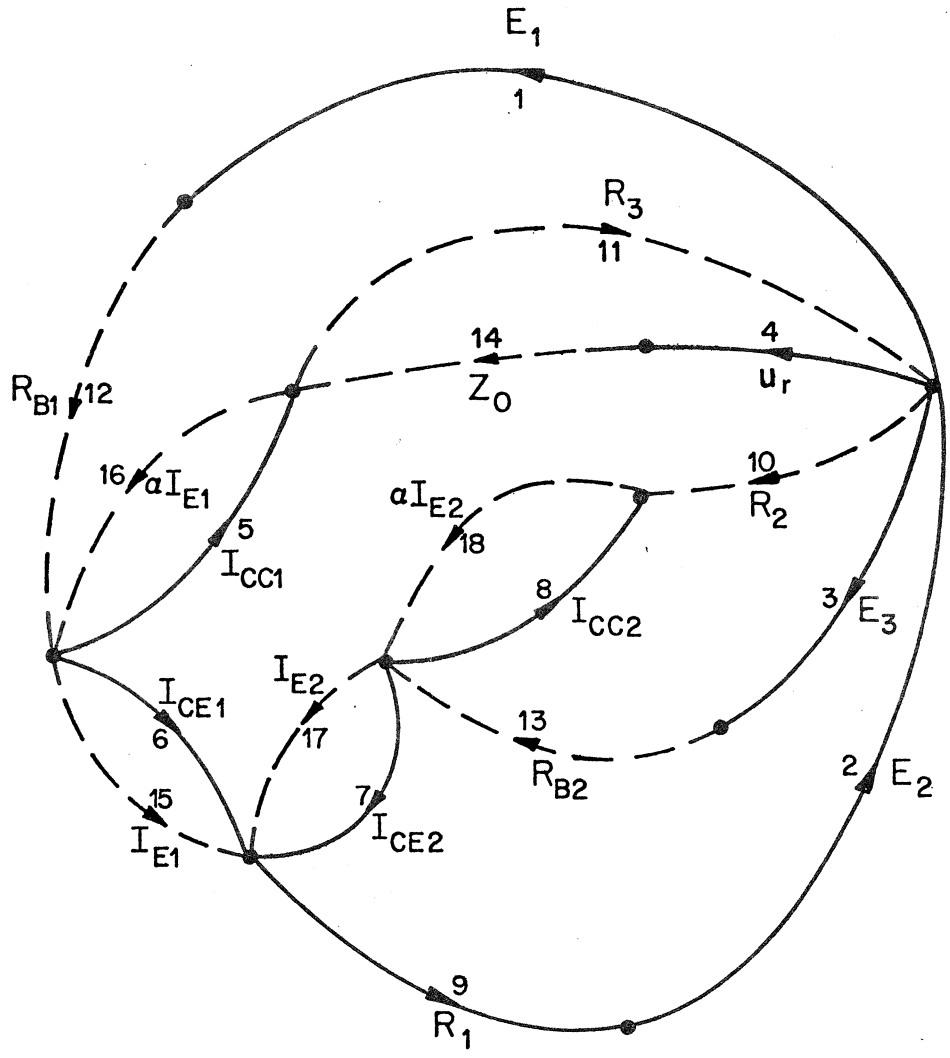

time ns
.2
.4
.6
.8
1.0
1.2
1.4
-.6
-.8
-1.0
-1.2
-1.4
-1.6
output voltage V_o
89% yield
39% yield

Fig. 7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R3
11
14
Z0
4
ur
RB1
12
16
αIE1
5
ICC1
αIE2
18
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8
ICC2
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E2
15
IE1
7
ICE2
9
R1

Fig. A.1

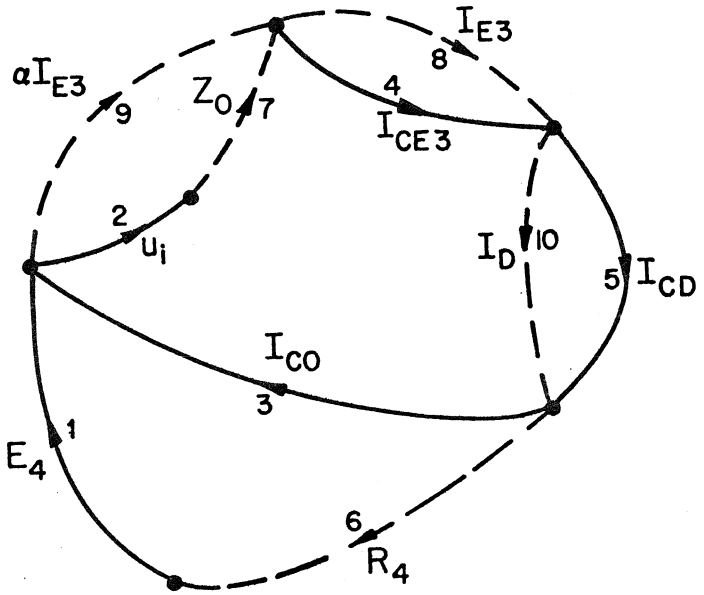

Fig. A.2

SOC-185

YIELD OPTIMIZATION FOR ARBITRARY STATISTICAL DISTRIBUTIONS PART II: IMPLEMENTATION

H.L. Abdel-Malek and J.W. Bandler

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Revised: June 1978, March 1979

Key Words: Yield analysis, design centering, tolerance assignment, numerical integration, nonlinear network design

Abstract: A suggested test problem for proposed algorithms in yield optimization is described in detail. The problem is a current switch emitter follower (CSEF) circuit originally described by Ho, which includes a transmission line. The ideas presented in Part I of this paper are applied to this circuit in order to obtain an optimal statistical design. Production yield is maximized taking into consideration statistical distributions of circuit parameters and realistic correlations between transistor model parameters. Nonlinear programming employing the analytical formulas for yield and its sensitivities is used to provide optimal nominal values for the circuit parameters. Different design specifications are assumed and corresponding optimal designs are obtained.

Description: Presented at the IEEE International Symposium on Circuits and Systems (New York, May 1978). See the symposium proceedings, pp. 670-674.

Related Work: SOC-182, SOC-184, SOC-191, SOC-192, SOC-193, SOC-194.

Price: $ 6.00.