PHASE NOISE ANALYSIS OF VOLTAGE-CONTROLLED OSCILLATOR

Phase Noise Analysis of

Voltage-Controlled Oscillator

By

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Abstract

In modern wireless communication technology, designing low power, high frequency transceivers while exhibiting low noise is still one of the challenging topics in RF systems. Compared to other technologies, CMOS VCO has a poorer performance at phase noise measurements. Therefore, improving phase noise becomes a very important issue in designing a high quality VCO.

This work describes and compares the available models to realize low phase noise oscillators. On this basis, the possible criteria for reducing phase noise are discussed.

In this thesis, we explore phase noise fluctuations at the offset range of 10 kHz to 100K Hz for six 2.4 GHz LC-tuned VCOs, fabricated in 0.18μm standard mixed-signal CMOS process. We compare the phase noise performance of all six circuits and draw conclusions about reducing phase noise.

The measurement results show that the Q factor of the inductor has the most significant effect on reducing phase noise fluctuations. The next important parameter is the capacitor. The resistors in the VCO do not affect phase noise fluctuations.

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List of Symbols and Acronyms

Symbols

f	Frequency in Hertz
F	Noise factor
g_m	Transconductance
g_{d0}	Drain conductance at zero drain-to-source voltage
I_{DC}	DC current
k	Boltzmann's constant
P_{DD}	DC power
P_{in}	Input power
P_{out}	Output power
q	Electron charge
Q	Quality factor
γ	bias-dependent noise parameter
R_{eff}	Effective resistance
T	Temperature
V_{CUR}	Tail current source voltage
V_{DD}	DC voltage
V_{VAR}	Varactor Bias
ω	Frequency in radians
W/L	Width over length ratio

η	Drain efficiency
μ	Electron mobility

Acronyms

ADC	Analog-to-digital converter
AGC	Automatic gain control
AM	Amplitude modulation
BJT	Bipolar junction transistor
BPF	Band-pass filter
BW	Bandwidth
CMOS	Complementary metal oxide semiconductor
DAC	Digital-to-analog converter
DC	Direct current
DNW	Deep n-well
DSB	Double side band
FoM	Figure-of-merit
IC	Integrated circuit
I/O	Input/Output
ISF	Impulse sensitivity function
IRMIX	Image-rejection mixer
LNA	Low-noise amplifier
LO	Local oscillator
LP	Loop filter

MOSFET	Metal-oxide semiconductor field effect transistor
NMOS	N-type metal-oxide semiconductor
PA	Power amplifier
PD	Phase detector
PLL	Phase-locked loop
PFD	Phase frequency detector
PM	Phase modulation
PMOS	P-type metal-oxide semiconductor
PSD	Power spectral density
RF	Radio frequency
RMS	Root mean square
Si	Silicon
SiGe	Silicon germanium
SPA	Semiconductor parameter analyzer
SSB	Single side band
SSCR	Single-sideband-to-carrier ratio
VCO	Voltage-controlled oscillator

Chapter 1

INTRODUCTION

Recent years have seen significant progress in wireless communication technologies. Better performance at lower cost and power consumption is the main motivation for Radio Frequency (RF) designer to develop new products.

For microwave frequency (gigahertz), CMOS is the dominant technology for semiconductor applications. This is due to two main reasons. First, power consumption is lower compared to other technologies. Second, in recent years the increase in the unity current gain frequency f_T of modern deep submicrometer MOS devices makes CMOS more competitive compared to other technologies. [1] However, noise in CMOS is a challenging issue in RF technology because it could affect the performance to a large extent.

1.1 CMOS Technology

CMOS circuits were first introduced in 1963 by Frank Wanlass. The first CMOS integrated circuits were made by RCA (Radio Corporation of America) in 1968 by a group led by Albert Medwin.[2] In less than half a century, CMOS has already become a widely used technology in RF applications because of its low cost and low power consumption.

CMOS technology has enabled the semiconductor industry to continually reduce device area for over 30 years. Figure 1.1 depicts the dramatic growth in capability of the microprocessor chip since the early 1970s. The regular exponential increase in transistors per chip was forecast in 1965 by Gordon Moore, whose prediction is known as "Moore's Law". When more transistors could be developed on one chip, the cost per function drops. According to Moore's Law, the number of transistors on a single chip is doubled every 18 months and the cost is therefore reduced by 25% every year.

Ubiquitous in our daily lives, CMOS technology has now reached every corner in the home. Figure 1.2 and Figure 1.3 show two example devices whose transceivers based on CMOS technology. Bluetooth technology is a short-range communication system whose objective is to remove the cables connecting two portable and/or fixed electronic devices. The key features of Bluetooth technology are low power consumption and low cost. [3] Therefore, CMOS is a promising solution for wireless devices.

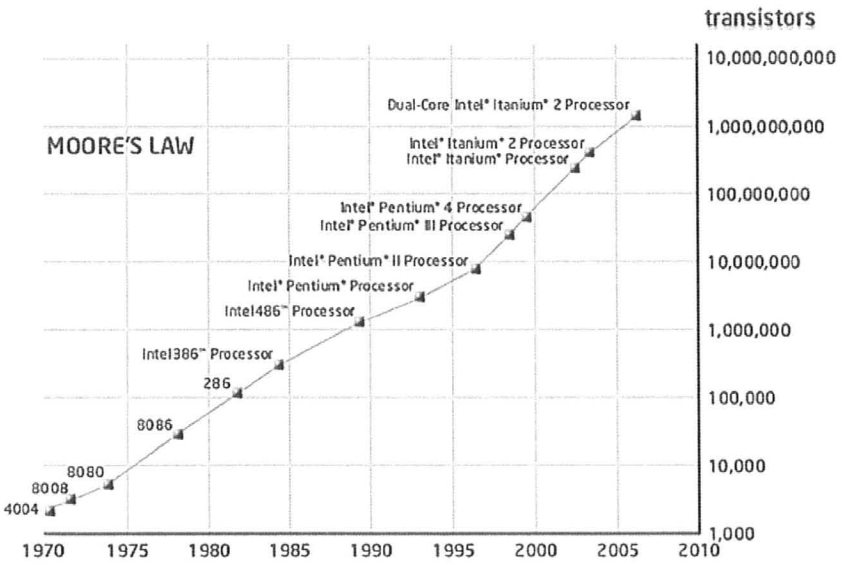


Fig 1.1: The steady progression of Moore's Law continues to double microprocessor capability with each generation [4]

Fig 1.2: Wireless Internet Camera [5]

Fig 1.3: Bluetooth technology connects many electronic devices [6]

1.2 VCO Applications

Frequency generator is an essential part in most electrical systems, especially in wireless telecommunications systems. CMOS VCO, a tuneable frequency oscillator, is the major component in the frequency generator. VCO is widely used in cell phones, satellites, radars, and many other electronic systems. It is a key component in transceivers, phase-locked loop (PLL), frequency synthesizers, and other applications. VCO has a huge impact on the performance, size, weight and cost of these devices. The size reduction of the commercial VCO module since 1980's is shown in Figure 1.4. Obviously, these changes eventually lower the cost.

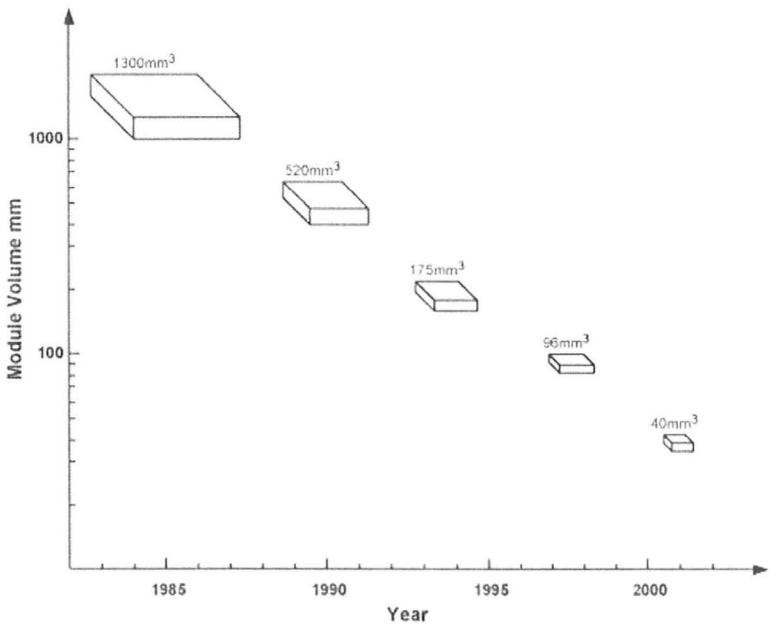


Fig 1.4: VCO module size reduction [7]

1.2.1 Transceiver

Transceiver is a short term for transmitter-receiver; it is a device that combines both a transmitter and a receiver. Figure 1.5 shows a transceiver block diagram used in

Bluetooth technology. Signal is received by the antenna, passes through a switch and a filter to get the desired frequency, and enters the transceiver. Through the transceiver, the signal is passed to a base-band (B.B.) processor via the I/O. The main parts of the receiver are the low-noise amplifier (LNA), image-rejection mixer (IRMIX), band-pass filter (BPF), automatic gain control (AGC), and analog-to-digital converter (ADC). The main parts of the transmitter are Gaussian filter, digital-to-analog converter (DAC), power amplifier (PA), VCO, and PLL.

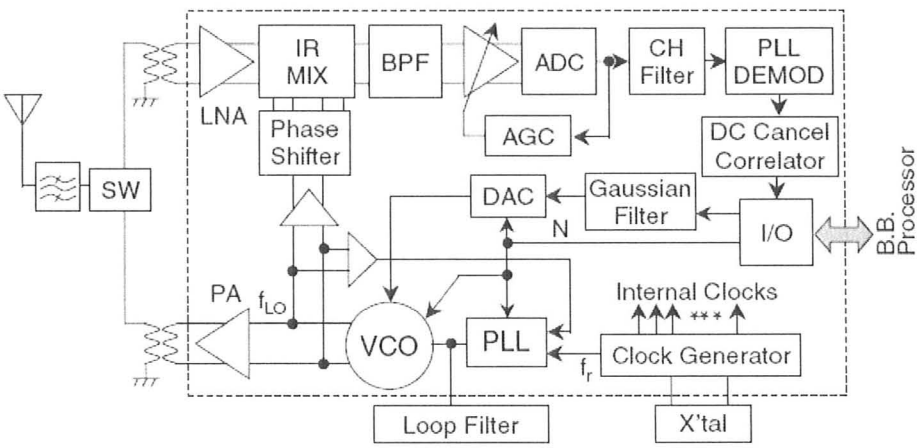


Fig 1.5: Transceiver block diagram [8]

Among the RF blocks in a transceiver, the CMOS LC-tuned VCO usually has poorer phase noise than other technologies such as SiGe HBT, thus making it difficult to meet commercial requirements. Therefore, improving phase noise in VCO is a very important issue in designing a well-performed VCO. Figure 1.6 shows an example of a wireless transceiver; the phase noises in both cases are shown in Figure 1.7 and Figure 1.8.

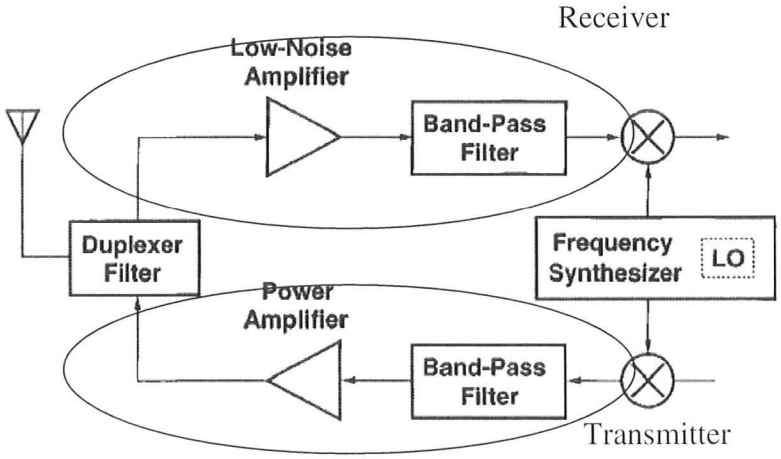


Fig 1.6: A wireless transceiver [9]

In the receiver, the signal of interest has a large interference in the adjacent channel. When these two signals are convolved with the local oscillator (LO) output, which has phase noise, the downconverted signals have a very large noise due to the interferer. In the transmitter, if the wanted signal is too weak compared to the nearby transmitter which has a significant phase noise, then the wanted signal can no longer be detected.[9] This example shows the importance of minimizing phase noise to improve the performance of a transceiver design.

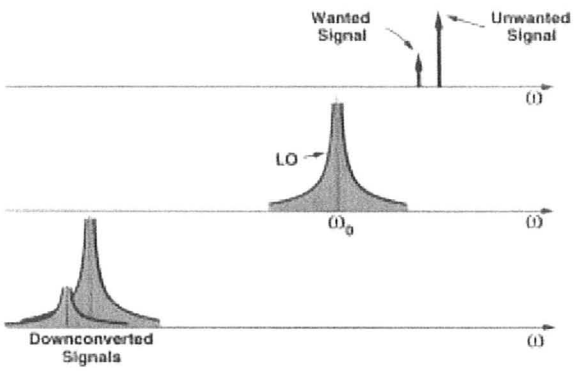


Fig 1.7: Phase noise in the receiver [9]

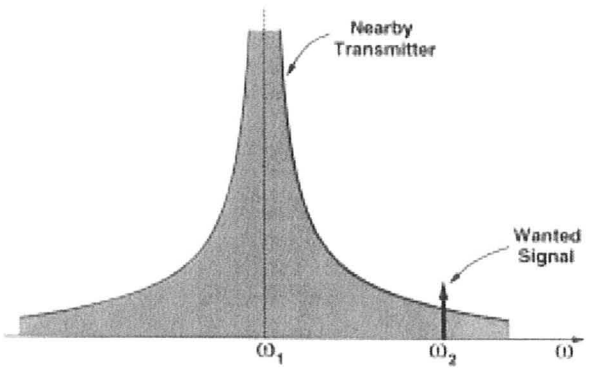


Fig 1.8: Phase noise in the transmitter [9]

1.2.2 Phase-Locked Loop (PLL)

PLL is a closed loop frequency control system the functioning of which is based on the phase sensitive detection of phase difference between the input signal and the output signal of the controlled oscillator. From a historical point of view, the PLL is not a new invention. PLL has been in use since the early 1930s.

In the 1940s, the first widespread use of phase-locked loop was in the synchronization of the horizontal and vertical sweep oscillators in television receivers to the transmitted sync pulses. Such circuits carried the names "Synchro-Lock" and "Synchro-Guide." Since then, the electronic phase-locked loop principle has been extended to other applications. For example, radio telemetry data from satellites using narrow-band, phase-locked loop receivers to recover low-level signals in the presence of noise.

The first PLL ICs appeared around 1965 and were purely analog devices. An analog multiplier (four-quadrant multiplier) was used as the phase detector, the loop filter was built from a passive or active RC filter, and the well-known voltage controlled

oscillator (VCO) was used to generate the output signal of the PLL. This type of PLL is referred to as the "linear PLL"(LPLL) today.

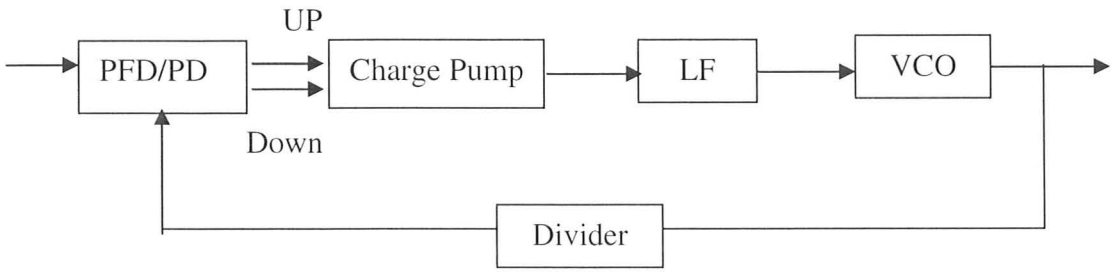


Fig 1.9: Basic analog phase-locked loop diagram

Analog PLL (phase-locked loop) is a type of PLL used to synchronize analog signals. The diagram of the analog PLL is shown in Figure 1.9. The whole circuit consists of five main parts:

- Phase Detector (PD) or Phase Frequency Detector (PFD)
- Charge Pump
- Loop Filter (LP)
- Voltage Controlled Oscillator (VCO)
- Divider

The left-hand block is the phase detector of phase frequency detector, which compares the phases and frequencies of its two input waves and produces an output that is proportional to the difference. There are two outputs from the PFD: up and down, which inform the VCO to either increase or decrease the frequency and phase. The charge pump current charges and discharges the loop filter to produce the VCO control voltage. The output of the phase detector is usually in the form of pulses that have to be low-pass filtered by the loop filter. This signal is then applied to the voltage-controlled

oscillator or VCO, the block on the right, which can generate a frequency that matches the reference signal. The output from the VCO is fed back to the divider, which helps to reduce the frequency from the VCO and makes the signal comparable to the reference signal. A low-pass filter smooths out abrupt changes in the control voltage; it can be demonstrated that some filtering is required for a stable system.

The VCO is a crucial component in the PLL and it can produce the necessary frequency output of the PLL.

1.2.3 Other VCO Applications

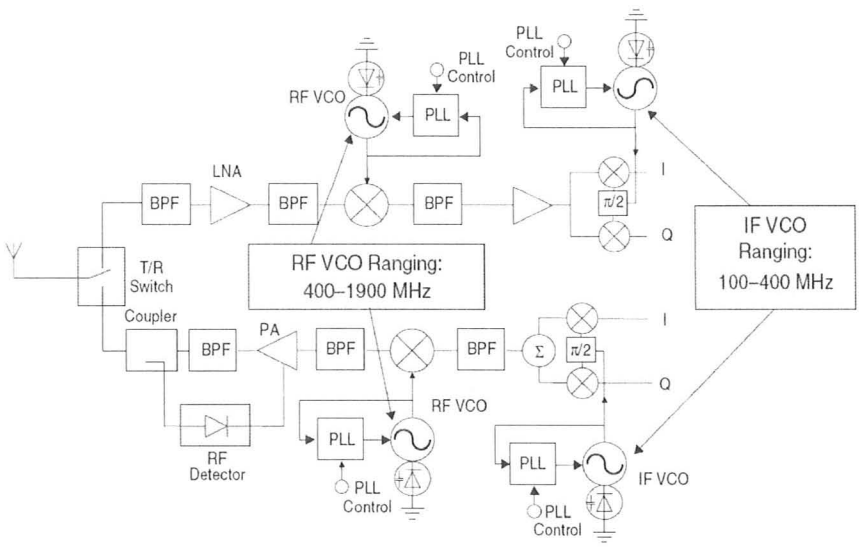


Fig 1.10: *VCO* application in a digital wireless phone [10]

Figure 1.10 shows a VCO application in a wireless handset phone with dual bands (900 MHz cellular band and 1.8GHz PCS band). In this application, 8 different VCO are used to solve the multi-band problem.

1.3 Thesis Scope and Organization

There are several reports in the literature that consider VCO phase noise performance [see, e.g., Refs11,12,13]. In several of these reports, ripples appear in the magnitude of the phase noise at offset of 10kHz-100kHz. This ripple is not predicted through simulation and the underlying cause is seldom discussed in the literature. Figure 1.11 shows a typical phase noise curve with such ripple.

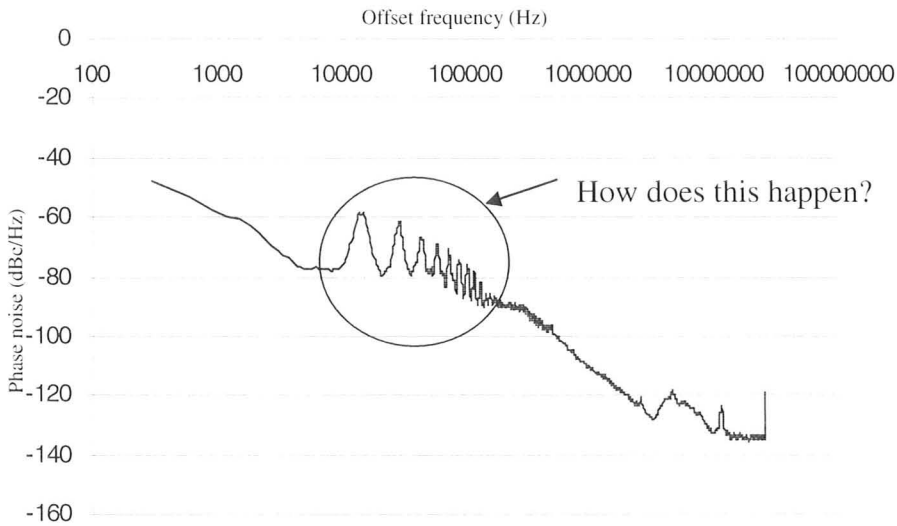


Fig 1.11: A typical phase noise measurement result

The focus of this thesis is to investigate phase noise ripple in the LC-tuned VCO. The contents of this thesis are as follows:

In Chapter 2, a brief introduction to noise is presented. Four main sources of noise in semiconductor devices are discussed: thermal noise, shot noise, flicker noise, and generation-degeneration noise.

Chapter 3 is concerned with the phase noise models of the LC-tuned VCO in previous works. The advantages and disadvantages of each model are summarized in this chapter.

Chapter 4 summarizes the design parameter of a VCO to optimize the phase noise performance. The phase noise fluctuation problem is also discussed here.

We fabricated six different variations of the same circuit to explore the underlying cause of phase noise ripple. Chapter 5 provides the measurement results of the fabricated circuits. Both DC measurements and phase noise measurements are discussed in this chapter.

Finally, chapter 6 describes the conclusions and future work.

Chapter 2

INTRODUCTION TO NOISE

Initially noise is considered as electronic signal that are created by audio devices, such as radios. Today not all noise is related to sound. The 'snow' image seen on a degraded television is also a type of noise. In general, noise could be considered as any unwanted signal in micro-electronic circuits, whether it affects the performance or not. For example, an RF signal, at a specific frequency, is the desired signal for certain receivers that need this signal, but is considered as noise by other receivers.

The first thing that we need to know about noise is that it is impossible to be removed, but what we could do is to decrease the noise level and render it so that it is not considered as interference. There are some types of noise, like thermal noise and shot noise, that are inherent in micro-electronic systems.

Noise is generated when electric current flows through resistive objects. An antenna picks up the desired signal and couples it into a transceiver system. In practice the received waveform is made up of the desired signal plus noise. Since the received signal is weak, amplification is needed before it is processed. It would not be beneficial if the noise is amplified as much as the desired signal and this leads to the invention of Low Noise Amplifier (LNA). LNA not only amplifies desired signal level but also suppresses noise signal level. This rather 'clean' signal could increase the performance of the system without introducing any additional interference. Filters such as LPF and BPF in transceivers are also designed to remove the noise and retain wanted signals.

The noise performance of a system could be measured by the noise factor (F) or noise figure (NF). The noise factor is defined as the ratio of

$$F = \frac{\text{total output noise power}}{\text{output noise due to input source}} \tag{2.1}$$

at a standard temperature of 290K.

The signal-to-noise ratio (SNR) is defined as the power ratio between the signal and the noise, which means:

$$SNR = \frac{P_{signal}}{P_{noise}} \tag{2.2}$$

Therefore, noise factor could also be expressed as:

$$\begin{aligned} F &= \left(\frac{\text{total output noise power}}{\text{total output signal power}}\right) \cdot \left(\frac{\text{total output signal power}}{\text{output noise due to input source}}\right) \\ &= \frac{1}{SNR_{out}} \cdot SNR_{in} \\ &= \frac{SNR_{in}}{SNR_{out}} \end{aligned} \tag{2.3}$$

The noise factor represents the degradation of the signal-to-noise ratio when signals pass through the system. In an ideal situation, the noise factor is equal to unity since the output noise is entirely due to the input source.

Noise figure (NF) is the noise factor expressed in decibels, and the relationship is defined as follows:

$$NF = 10\log(F),\ F = 10^{NF/10} \tag{2.4}$$

$$NF = SNR_{in} - SNR_{out} \tag{2.5}$$

Since noise is random, it is difficult and meaningless to be presented in its absolute value. People usually use noise power to express noise, the root mean square (rms) value of noise power is:

$$V_{rms} = \sqrt{|V|^2} \tag{2.6}$$

Noise power spectral density (PSD) expresses noise power distribution over a frequency band, usually in the bandwidth of 1Hz. It indicates at which bands the noise is strong and at which bands the noise is weak.

Noise occurs when current flows in objects, the random motions of electrons make the voltage and current fluctuate. Noise can come from many different sources. Here we will discuss four main sources of noise in semiconductor devices: thermal noise, shot noise, flicker noise and generation-recombination noise. There are also some other sources of noise, but the impact of those sources is ordinarily negligible compared with the major components discussed here.

2.1 Noise

2.1.1 Thermal noise

Thermal noise was first measured by John B. Johnson in 1928 and then explained by Harry Nyquist, so it is also called Johnson-Nyquist noise. It is generated when thermal energy causes free electrons to move randomly in a resistive material. This type of noise occurs even when there is no external power supply. Thermal noise exists in any passive resistor above absolute zero temperature.

As shown in Figure 2.1, a resistor's thermal noise can be modeled by a noiseless resistor in series with a voltage source. The open-circuit thermal noise voltage mean square value across a resistor is $\overline{v_n^2} = 4kTR\Delta f$, and the power spectral density (PSD) is $4kTR$, where k is Boltzmann's constant which is equal to 1.38×10^{-23} J/K, T is the absolute temperature, and Δf is the bandwidth (BW) in hertz over which the noise is measured $\Delta f = f_{\max} - f_{\min}$. It is known that the power in thermal noise is proportional to $\overline{v_n^2}$. When the power has no frequency dependence for a fixed bandwidth, this kind of noise is said to have a uniform or flat power distribution and is called white noise. [14] [15] A 50Ω resistor has a thermal noise about $1nV/\sqrt{Hz}$.

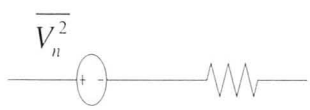


Fig 2.1: Resistor's thermal noise model

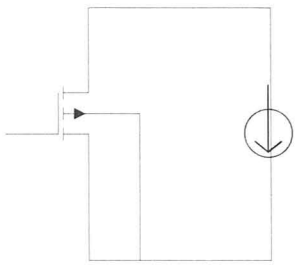


Fig 2.2: MOSFET's thermal noise model

In MOSFET, thermal noise is generated in the channel and its noise spectral density S could be expressed as:

$$S_{I_d}(f) = 4kT\gamma g_{d0} \tag{2.7}$$

where g_{d0} is the drain conductance at zero drain-to-source voltage and γ is the bias-dependent noise parameter. The thermal noise model of MOSFET is shown in Figure 2.2. At zero drain-to-source voltage, γ is equal to unity and decreases to 2/3 as the device enters the saturation regime. Also 2/3 is for lightly doped substrate, the value increases for higher substrate doping. [16] Klaassen and Prins extended this equation to describe all MOSFET thermal noise research. The equation is [17]:

$$S_{I_d}(f) = \frac{4kT}{I_{DS}L^2}\int_0^{V_{DS}} g^2(V)dV \tag{2.8}$$

where I_{DS} is the drain-to-source current, L is the electrical channel length, and $g(V)$ is the local channel conductance.

2.1.2 Shot noise

Shot noise is caused by the random emission of electrons or photons, or the random passage of carriers across potential barriers. [18] It is generated when a DC

current flows across a potential barrier. The current has the random fluctuation about its average value, which results in a lot of independent current pulse. [14][15]

The root mean square (rms) shot noise current is given by:

$$I_{sn}^2 = 2qI_{dc}\Delta f \tag{2.9}$$

and the PSD is given by:

$$S_{I_{sn}} = 2qI_{dc} \tag{2.10}$$

where q is the electronic charge, I_{dc} is the average DC current and Δf is the frequency band. For a fixed frequency bandwidth, the shot noise current does not have frequency dependence, i.e., it is white noise.

There are two conditions for shot noise to occur:

- there is a direct current flow in the circuit;

- there must be a potential barrier for the charge carrier.

Shot noise could not be distinguished from thermal noise since both processes happen simultaneously and resulted in white noise. Therefore, the existence of shot noise is defined for the above two reasons. Thermal noise could also happen when there is no direct current. And the linear resistors could not generate shot noise since there are no potential barriers in them. In MOSFET, shot noise is generated by the DC gate leakage current. Because this current is small, shot noise is not a big contribution in MOSFET.

2.1.3 Flicker noise

The imperfect contact between conducting materials causes the conductivity to fluctuate in the presence of a DC current. This is called flicker noise and it occurs in any

device where two conductors are joined together. This noise was first observed in vacuum tubes, and gets its name from the anomalous "flicker" that was seen in the plate current. Flicker noise is a quantitatively more accurate way to describe the type of noise that occurs specifically at low frequencies.

The rms flicker noise current is given by:

$$I_{fn} = \sqrt{\frac{k_f I^m \Delta f}{f^n}} \tag{2.11}$$

where I is the DC current, n is an exponent that is usually close to 1. k_f is the flicker noise coefficient, and m is the flicker-noise exponent whose value is between 0.5 and 2. Since the power in flicker noise is proportional to the square of I_f which is inversely proportional to the frequency, usually flicker noise is also called 1/f noise. [14]

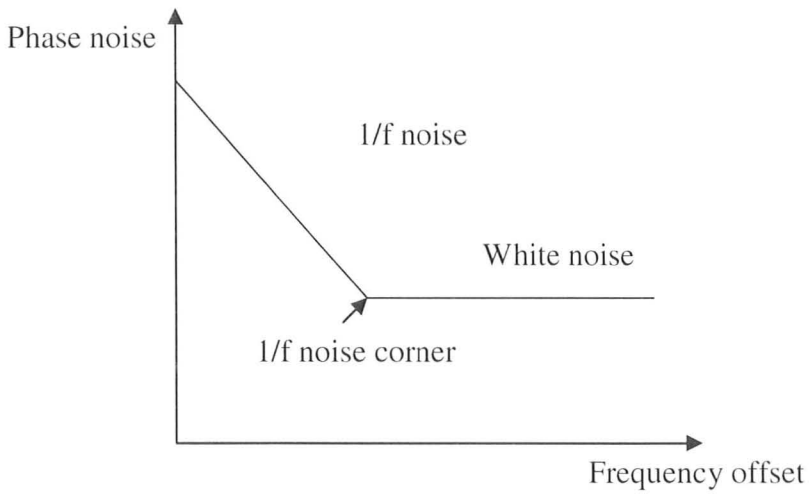


Fig 2.3: Flicker noise corner

Here is an important thing to note, flicker noise is also called the low-frequency noise. That's because the PSD of low frequency noise is extremely small in linear RF circuits. In nonlinear RF circuits, this noise can be converted to RF by the unwanted

mixing processes of frequencies around the signal. But eventually, the resulting upconverted noise can be eliminated by using feedback in the form of PLLs. That is why we usually do not discuss flicker noise in high frequency range.

Flicker noise for MOSFET is much more than that in bipolar devices since flicker noise is sensitive to the surface phenomena. For the MOSFET devices, flicker noise is equal to:

$$I_{fn} = \frac{g_m}{C_{ox}} \sqrt{\frac{k_f}{f} \frac{1}{WL} \Delta f} \tag{2.12}$$

$$\approx \sqrt{\frac{k_f}{f} \cdot \omega_T^2 \cdot A \cdot \Delta f} \tag{2.13}$$

where g_m is the device conductance, C_{ox} is the gate capacitance per unit area, W is the channel width , L is the channel length and A is the area of the gate. [16] k_f is estimated at about $10^{-28} C^2/m^2$ for PMOS devices while the value is about $5\times10^{-27} C^2/m^2$ for NMOS devices.

2.1.4 Generation-recombination noise (GR noise)

GR noise is caused by the random generation and recombination of hole-electron pairs, the random generation of carriers from traps, or the random recombination of carriers with empty traps. [18] The spectral density of resistance fluctuation is [19]:

$$S_R = \frac{\overline{(\Delta N)^2}}{N^2} \frac{4\tau R^2}{1+\omega^2\tau^2} \tag{2.14}$$

where τ is a relaxation time, called a Lorentzian characteristic, usually in the range of 10^{-6} s to 10^{-3} s. The variance $\overline{(\Delta N)^2}$ is given by

$$\frac{1}{\overline{(\Delta N)^2}} = \frac{1}{N} + \frac{1}{X_n} + \frac{1}{X_p} \tag{2.15}$$

where X_n is the average number of occupied traps and X_p the average number of empty traps.

In MOSFET, current spectral density is expressed as:

$$S_I(f) = \frac{4q\mu IV}{L^2} \frac{\tau}{1+\omega^2\tau^2} \tag{2.16}$$

where q is the electronic charge, μ is the electron mobility, L is the sample length, I is the current, and V is the channel potential.

2.2 MOSFET Noise Model

After the discussion of the four major noise sources in semiconductor devices, we could then move on to the analysis of noise in MOSFETs. In order to do this, Figure 2.4 shows a cross section of a MOSFET that could help to get a better understanding.

Since MOSFETs have four terminals (gate, source, drain and body), each terminal generates its own thermal noise from the parasitic gate (R_G), source (R_S), drain (R_D) and body (R_B) resistances. The value is:

$$\sqrt{\overline{v_{nx}^2}} = \sqrt{4kTR_x} \tag{2.17}$$

$$\sqrt{\overline{i_{nx}^2}} = \sqrt{\frac{4kT}{R_x}} \tag{2.18}$$

where X indicates G, S, D and B terminals.

$$\sqrt{\overline{i_{shot}^2}} = \sqrt{\frac{8kTg_m}{3}} \tag{2.19}$$

$$\sqrt{\overline{i_{1/f}^2}} = \sqrt{\frac{KF \cdot I_D^{AF}}{COX \cdot}} \tag{2.20}$$

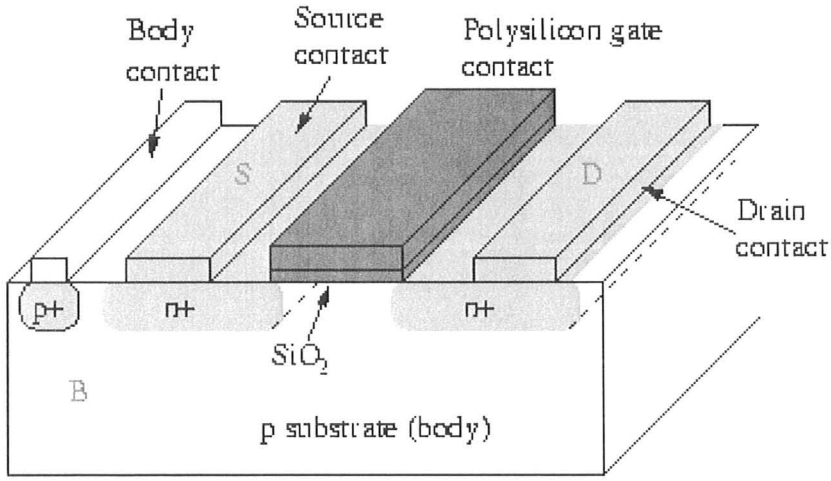


Fig 2.4: Cross Section of a MOSFET[20]

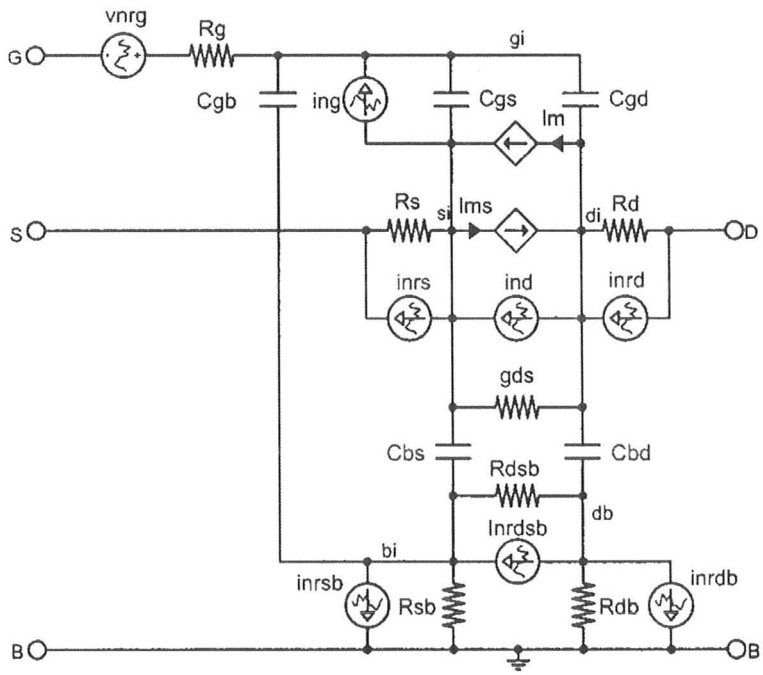


Fig 2.5: MOSFET noise sources in saturation region [21]

In [21], noise sources are categorized in three main groups:

1. Thermal noise of resistances.

These resistances include gate resistance S_{vnrg}, source resistance S_{inrs}, drain resistance S_{inrd}, source-body resistance S_{inrsb}, drain-body resistance S_{inrdb}, and drain-source-body resistance S_{nch}.

2. Drain noise S_{ind}.

Drain noise is the combination of two noise sources: channel thermal noise and flicker noise.

3. Induced gate noise S_{ing}.

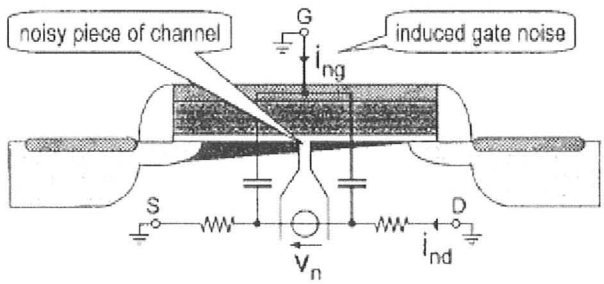


Fig 2.6: Induced gate noise. [21]

At high frequencies, the thermal effect generates voltage fluctuations at the gate channel (see Figure 2.6). Voltage couples with oxide capacitance C_{gs} and generates induced gate noise. The value of this noise is:

$$S_{ing} = 4kT\delta\frac{(\omega C_{gs})^2}{5g_{d0}} \qquad (2.21)$$

where gate noise coefficient δ is equal to 4/3 for a long-channel device in saturation. [22]

2.3 Summary

A basic introduction to noise is given in this chapter. Four different noise sources are discussed followed by MOSFET noise models. These concepts could offer a better understanding of phase noise which will be studied in the next chapter.

Chapter 3

PHASE NOISE

Short term and long term stability plays a crucial role in designing an oscillator. Frequency and phase fluctuations caused by random noise are classified as short-term frequency stability while signal variation caused by temperature and time progression is classified as long term stability. The term phase noise is widely used for describing short-term frequency stability. Phase noise is a product of up-conversion of low-frequency noise to higher (carrier) frequency, and increases the required channel spacing in RF applications, thereby limiting the number of channels in communication systems. [23]

The ideal output of a sinusoidal oscillator could be expressed as:

$$V_{out}(t) = A\sin(\omega_0 t + \phi) \tag{3.1}$$

where A is the amplitude, ω_0 is the frequency and ϕ is the fixed phase reference. In reality, the output is represented by

$$V_{out}(t) = A(t) f(\omega_0 t + \phi(t)) \tag{3.2}$$

where $A(t)$ and $\phi(t)$ include the amplitude and phase fluctuations of the signal respectively and f is a periodic function of 2π. In general, phase noise can affect both the amplitude and phase of the oscillator output. However, all practical oscillators have some amplitude limiting mechanisms which will eventually attenuate the amplitude fluctuations. Thus, phase fluctuation dominates in the design of oscillators.

Phase noise can be measured as either single sideband (SSB) or double sideband (DSB). Phase noise is typically expressed in units of dBc/Hz at various offsets from the carrier frequency. The relation between SSB spectral density and DSB spectral density is:

$$S_{SSB}(f) = 2S_{DSB}(f), \text{ for } 0 \le f < \infty, \text{ otherwise zero} \qquad (3.3)$$

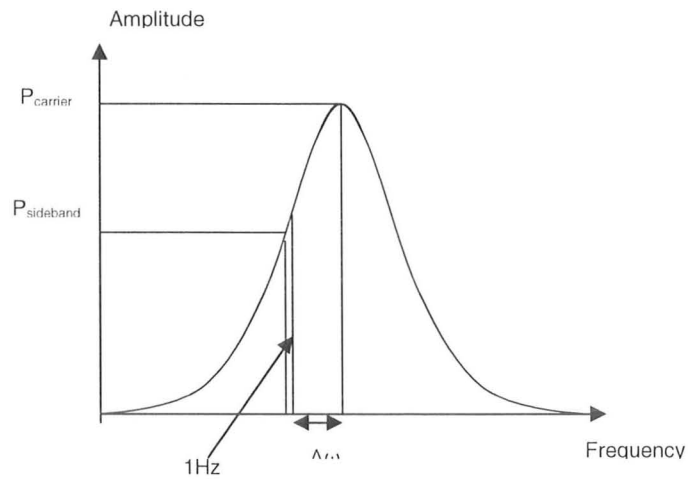


Fig 3.1: The typical phase noise plot

More precisely, the DSB spectral density is defined for $-\infty < f < \infty$, while the SSB spectral density is only defined for the positive frequencies. The SSB phase noise $L(\Delta\omega)$ is defined as the ratio of noise power in a bandwidth of 1Hz at frequency deviation $\Delta\omega$ from the oscillation frequency ω_0 and the signal power at the oscillation

frequency ω_o.[24] It is usually expressed in units of decibel carrier per Hertz (dBc/Hz) and defined as: [25]

$$L(\Delta\omega) = 10 \cdot \log\left(\frac{P_{sideband}(\omega_0 + \Delta\omega, 1Hz)}{P_{carrier}}\right) \tag{3.4}$$

When using spectral analyzer, phase noise is defined by the following equation, which will be explained later section 3.5.1:

$$L(\Delta\omega) = 10 \cdot \log\left(\frac{P_{sideband}}{P_{total\ in\ full\ band}}\right) - 10 \cdot \log(resolution\ bandwidth) \tag{3.5}$$

The phase noise performance of different oscillators is usually compared by figure of merit (FoM), which is defined by [26]:

$$FoM = 10\log\left(\left(\frac{f_o}{\Delta f}\right)^2 \frac{1}{L(\Delta f)P}\right) \tag{3.6}$$

where f_o is the oscillator frequency, Δf is the offset frequency, $L(\Delta f)$ is the phase noise at the offset frequency Δf, and P is the DC power consumption of the oscillator.

In this chapter, different phase noise models of VCO are discussed.

3.1 Leeson's Semi-Empirical Model

In 1966, D.B. Leeson proposed a semi-empirical model for phase noise measurement. In this model, a physical oscillator has two main sources of phase uncertainty:

1. from additive white noise at frequencies around center frequency and also noise at other frequencies mixed into the pass band;

2. from parameter variations at video frequencies which affect the phase. The power spectral density from this source usually varies inversely with the frequency, that is, 1/f spectrum.

To calculate the total power spectral, we need to discuss two regions

1. $\omega < \frac{\omega_0}{2Q}$, where noise is from both noise sources;

2. $\omega > \frac{\omega_0}{2Q}$, where noise is mainly from the first source.

$\frac{\omega_0}{2Q}$ is half of the resonator bandwidth.

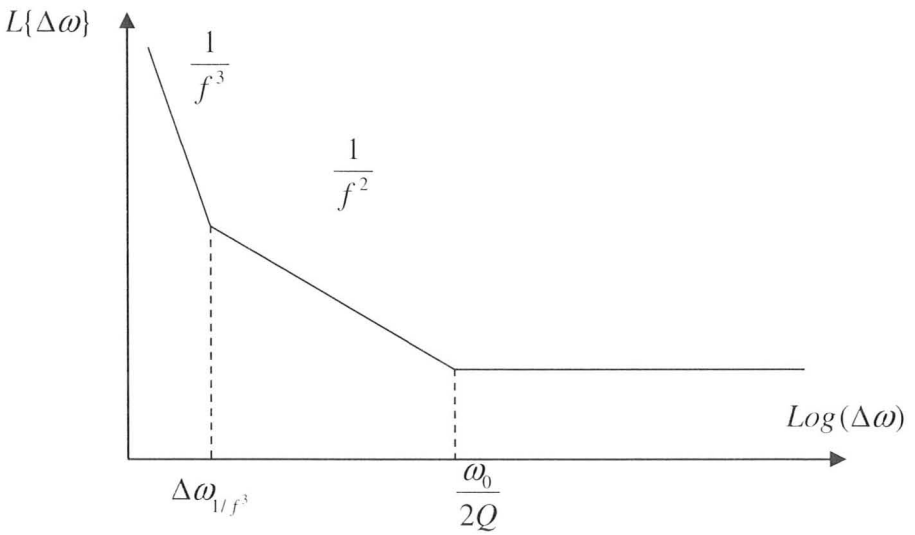


Fig 3.2: Leeson's semi-empirical phase noise model

Based on the above theories, the phase noise, shown in Figure 3.2, consists of three regions. The first region is $1/f^3$, which has a slope of 9dB/octave. This noise is derived from the 1/f variations and is very close to the carrier frequency. This is also known as the close-in phase noise. The phase noise in this region is expressed as:

$$L(\Delta\omega) = 10\log((\frac{\omega_0}{2Q})^2 \alpha(\frac{1}{\Delta\omega})^3) \tag{3.7}$$

where α is a constant value which is determined by the level of 1/f variations.

The second region of the phase noise model is the $1/f^2$ region, which has a slope of 6dB/octave. It is defined from the point where 1/f variations no longer dominates the noise and takes up to half of the resonator bandwidth. In this region, the spectrum is:

$$L(\Delta\omega) = 10\log[\frac{2FkT}{P_s}(\frac{\omega_0}{2Q\Delta\omega})^2] \tag{3.8}$$

The phase noise is determined by the F number (an empirical fitting number, which is also called the device excess noise number), P_s the average power dissipated in the resistive part of the tank can be also expressed as A^2/R_{eq} (where R_{eq} is the tank impedance), Q value and T the absolute temperature.

The phase noise in the last region has a constant value, which is:

$$L(\Delta\omega) = \frac{2FkT}{P_s} \tag{3.9}$$

In 2000, Rael proposed that the value of this noise factor F could be defined as [27]:

$$F = 1 + \frac{4\gamma IR}{\pi V_0} + \gamma\frac{4}{9} g_{mbias} R \tag{3.10}$$

where γ is the channel noise coefficient of the FET, I is the bias current, and g_{mbias} is the transconductance of the current-source FET.

3.2 Linear Time Invariant Estimation

Based on Leeson's model, Craninckx proposed a linear time invariant model. [25] The model assumes that the circuit is linear and only thermal noise is considered here, it neglects other noise sources, such as flicker noise.

Figure 3.3 shows a basic feedback LC-tuned oscillator where G_M is the transconductance, R_l is the series resistance of the inductor L, R_c is the series resistance of the capacitor C. The improvement of this model is that it considers the resistor R_p, which is the equivalent resistance of the output resistance and the parallel resistance across C and L.

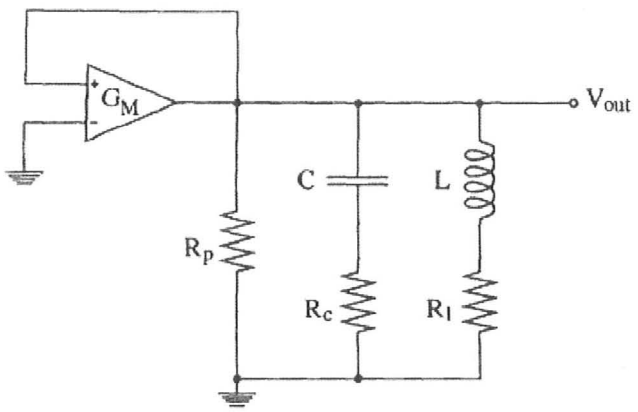


Fig 3.3: An LC-tuned oscillator as a feedback circuit

Total noise is the addition of every parasitic resistance noise: R_p, R_c and R_l. To achieve that, first we need to calculate the noise R_p.

Based on the Barkhausen criterion, the steady-state oscillation occurs only if:

1. The loop gain is equal to 1.
2. The loop phase delay is set to zero or an integer multiple of 2π.

For the LC-tuned oscillator, the loop transfer function is defined as:

$$H_{Rp}(j\omega) = \frac{V_{out}}{V_+} = G_M(R_p // j\omega L // \frac{1}{j\omega L})$$
$$= G_M \frac{j\omega L}{(1-\omega^2 LC) + j\omega \frac{L}{R_p}} \tag{3.11}$$

When the imaginary part of the loop transfer function is equal to zero,

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{3.12}$$

When the loop gain is equal to 1,

$$H(j\omega_0) = 1$$
$$G_M \frac{j\omega L}{j\omega \frac{L}{R_p}} = G_M \cdot R_p = 1$$

$$G_M = \frac{1}{R_P} \tag{3.13}$$

Then the transfer function from the current noise source $di_{R_p}^2$ to the output noise voltage V_{out} is:

$$H_{R_p}^2(j\omega) = \frac{dV_{out}^2}{di_{R_p}^2}$$
$$= (R_p // j\omega L // \frac{1}{j\omega C} // (-\frac{1}{G_M}))^2$$
$$= (\frac{j\omega L}{1 - j\omega L(G_M - \frac{1}{R_P}) - \omega^2 LC})^2 \tag{3.14}$$

At $\omega = \omega_0 + \Delta\omega$,

$$H_{R_p}(j\omega) = \frac{j(\omega_0 + \Delta\omega)L}{1 - j(\omega_0 + \Delta\omega)L(G_M - \frac{1}{R_P}) - (\omega_0 + \Delta\omega)^2 LC}$$

$$\approx 2j\sqrt{\frac{L}{C}}(\frac{\omega_0}{\Delta\omega}) \tag{3.15}$$

Then the noise density at frequencies very close to the center frequency is

$$\begin{aligned} dV^2_{out,R_p}(\omega_0+\Delta\omega) &= H^2_{R_p}(\omega_0+\Delta\omega)\cdot di^2_{R_p} \\ &= \left|2j\sqrt{\frac{L}{C}}(\frac{\omega_0}{\Delta\omega})\right|^2 \cdot \frac{4kT}{R_p}\cdot df \\ &= kT\frac{1}{R_p(\omega_0 C)^2}(\frac{\omega_0}{\Delta\omega})^2\cdot df \end{aligned} \tag{3.16}$$

Similarly, the noise densities come from current noise sources R_l *and* R_c are defined as:

$$dV^2_{out,R_l}(\omega_0+\Delta\omega) = kT\cdot R_l\cdot(\frac{\omega_0}{\Delta\omega})^2\cdot df \tag{3.17}$$

$$dV^2_{out,R_c}(\omega_0+\Delta\omega) = kT\cdot R_c\cdot(\frac{\omega_0}{\Delta\omega})^2\cdot df \tag{3.18}$$

When combining them together, the phase noise could be expressed as:

$$\begin{aligned} L(\Delta\omega) &= 10\log(\frac{\int_{\omega_0+\Delta\omega-1/2}^{\omega_0+\Delta\omega+1/2} dV^2_{out}}{P_{out}}) \\ &= 10\log(\frac{kT}{V^2_{\max}/2}R_{eff}\cdot(1+A)\cdot(\frac{\omega_o}{\Delta\omega})^2) \end{aligned} \tag{3.19}$$

where A is also an empirical fitting parameter and is equal to $\alpha\cdot F_{G_M}$, F_{G_M} is the noise factor of the amplifier, α is a factor, and $V_{\max}$ is the voltage amplitude. R_{eff} is the effective resistance which includes all three resistors, $R_{eff} = R_l + R_c + \frac{1}{R_p(\omega_0 C)^2}$.

From Craninckx's model, the phase noise can be improved by increasing the oscillation voltage and decreasing the effective resistance.

3.3 Nonlinear Time Invariant Estimation

In 1998, Samori presented a nonlinear phase noise theory based on differential LC-tuned oscillators. [28] The carrier signal is $V_o(t)$ with amplitude A_o , it is superimposed by a harmonic tone $V_t(t)$ at $\omega_o - \alpha$ and the amplitude of $V_t(t)$ is much less than A_o . This will create an amplitude modulation (AM) and a phase modulation (PM).

In Samori's model, the conductance of resistor R_p , as shown in Figure 3.3, is

$$g_p = g_{pC} + g_{pL} + \frac{(\omega_0 C)^2}{g_{sC}} + \frac{1}{(\omega_0 L)^2 + g_{sL}} \tag{3.20}$$

where g_{pc} and g_{pl} are the parasitic conductance in parallel with the capacitor and inductor, while g_{sc} and g_{sl} are those in series with the capacitor and inductor.

Q of the tank is defined as $Q = \frac{\omega_0 C}{g_p}$. The impedance at the frequency $\omega_0 + \Delta\omega$ could be written as:

$$\left|Z(\omega_0 + \Delta\omega)\right|^2 \approx \frac{1}{(2\Delta\omega C)^2} \tag{3.21}$$

And the noise power at offset $\Delta\omega$ is:

$$\begin{aligned} P_{nv} = S_{ni} \times \left|Z(\omega_0 + \Delta\omega)\right|^2 &= \frac{S_{ni}}{4\Delta\omega^2 C^2} \\ &= \frac{S_{ni}}{4\Delta\omega^2 C \times C} \\ &= \frac{S_{ni}\omega_0}{4\Delta\omega^2 C g_p Q} \\ &= \frac{1}{4}\frac{S_{ni}}{g_p C}\frac{\omega_0}{Q}\frac{1}{\Delta\omega^2} \end{aligned} \tag{3.22}$$

where S_{ni} is the overall current noise source and it can be expressed as:

$$S_{ni} = 2kTg_p(1+F) \tag{3.23}$$

The phase noise at a frequency offset $\Delta\omega$ from the carrier is:

$$L(\Delta\omega) = 10\log(\frac{kT}{V_{\max}^2 C}\frac{\omega_o}{Q}\left(\frac{1}{\Delta\omega}\right)^2(1+F)) \tag{3.24}$$

with the F given by

$$F = 2r_{bb'}g_{ot}\eta + \frac{\sigma S_{nt}}{kTg_{ot}}$$

F is still an empirical fitting parameter.

3.4 Nonlinear Time Variant Estimation

In [29], Hajimiri and Thomas H. Lee points out that there are some drawbacks in Leeson's model:

1). F, $\Delta\omega_{1/f^3}$ are empirical fitting parameters, which are determined by the measurements.

2). The frequency where the noise flattens out is not always equal to $\frac{\omega_0}{2Q}$.

Therefore, they proposed a time variant model based on the impulse sensitivity function to predict phase noise. In this model, every oscillator is a system with n inputs and two outputs. Each input is associated with a noise source, and the two outputs are instantaneous amplitude and excess phase of the oscillator, $A(t)$ and $\phi(t)$ respectively. Noise inputs to this system are in the form of current sources injecting into circuit nodes and voltage sources in series with circuit branches.

The phase impulse response is expressed as:

$$h_{\phi}(t,\tau)=\frac{\Gamma(\omega_0\tau)}{q_{\max}}u(t-\tau) \tag{3.25}$$

where $u(t)$ is the unit step function and $q_{\max}$ is the maximum charge displacement in the tank. The quantity Γ is the ISF (impulse sensitivity function). ISF is essentially a transfer function between an arbitrary noise source and the excess phase at the output of the oscillator. ISF, whose example is shown in Figure 3.4, is calculated from the output waveform. It is not related to the oscillation frequency, and has a period of 2π :

$$\Gamma(\omega_0\tau)=\frac{c_0}{2}+\sum_{n=1}^{\infty}C_n\cos(n\omega_0\tau+\theta_n) \tag{3.26}$$

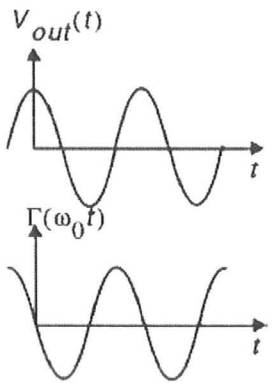


Fig 3.4: Illustration of the ISF [29]

From the ISF, the excess phase could be expressed as:

$$\phi(t)=\frac{1}{q_{\max}}[\frac{c_0}{2}\int_{-\infty}^{t}i(\tau)d\tau+\sum_{n=1}^{\infty}c_n\int_{-\infty}^{t}i_n(\tau)\cos(n\omega_0\tau)d\tau] \tag{3.27}$$

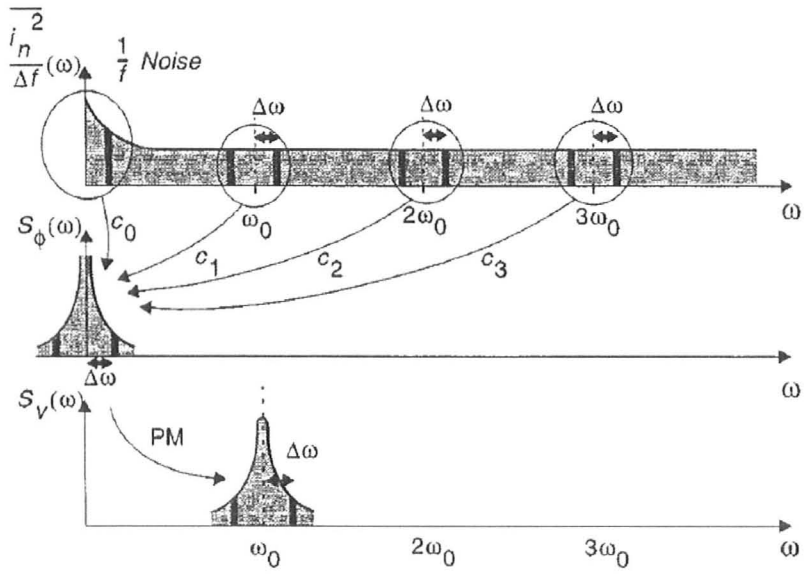


Fig 3.5: Illustration of noise converted to phase noise sidebands [29]

The phase noise spectrum of an oscillator in $1/f^2$ region of the phase noise spectrum, which is due to the thermal noise, is:

$$L(\Delta\omega) = 10\log(\frac{\Gamma_{rms}^2}{q_{\max}^2} \cdot \frac{\overline{i_n^2}/\Delta f}{4 \cdot \Delta\omega^2}) \tag{3.28}$$

The phase noise in the $1/f^3$ region of the phase noise spectrum, which is due to flicker noise, is:

$$L(\Delta\omega) = 10\log(\frac{c_0^2}{q_{\max}^2} \frac{\overline{i_n^2}}{8\Delta\omega^2} \frac{\omega_{1/f}}{\Delta\omega}) \tag{3.29}$$

The $1/f^3$ corner of the phase noise is not the same as the $1/f$ corner of the device noise spectrum:

$$\omega_{1/f^3} = \omega_{1/f} \cdot (\frac{\Gamma_{dc}}{\Gamma_{rms}})^2 \tag{3.30}$$

where Γ_{dc} is the DC value of the ISF and Γ_{rms} is the rms value of the ISF.

3.5 Phase Noise Measurements

3.5.1 Spectrum Analyzer

Phase noise is usually measured by using a spectrum analyzer. For this thesis, Agilent E4440A PSA Series Spectrum Analyzer with a frequency range from 3Hz to 26.5GHz is used.

Three main parameters need to be carefully selected before doing the measurement: span, resolution bandwidth (RBW) and reference level.

- Span is the maximum offset frequency from centre frequency.

- RBW determines the smallest frequency that can be resolved, in other words, it determines the sensitivities of the spectral analyzer.

- Reference level could introduce extra thermal noise to the tested circuit. This parameter is important in calculating the phase noise. It must be taken into consideration when calculating the phase noise equation, which will be introduced in the next chapter.

To improve the repeatability of the measurement, some methods could be used, for example, smoothing and averaging are two of them. [30]

- Averaging measures multiple traces for the same point and then calculates the average value. For this test, more than twenty traces are used for the same measurement.

- Smoothing averages adjacent trace points for a log plot measurement.

3.5.2 Frequency Discriminator Method

The frequency discriminator method converts the frequency fluctuations into phase fluctuations in the first stage, and then converts into voltage fluctuations which could be measured by the baseband analyzer, as shown in Figure 3.6. [31]

This method does not need a second reference source and is useful for measuring a source that is difficult to phase lock. However, this method could not be used to measure the close-in phase noise because it requires a delay line that is too long to be practically feasible.[30]

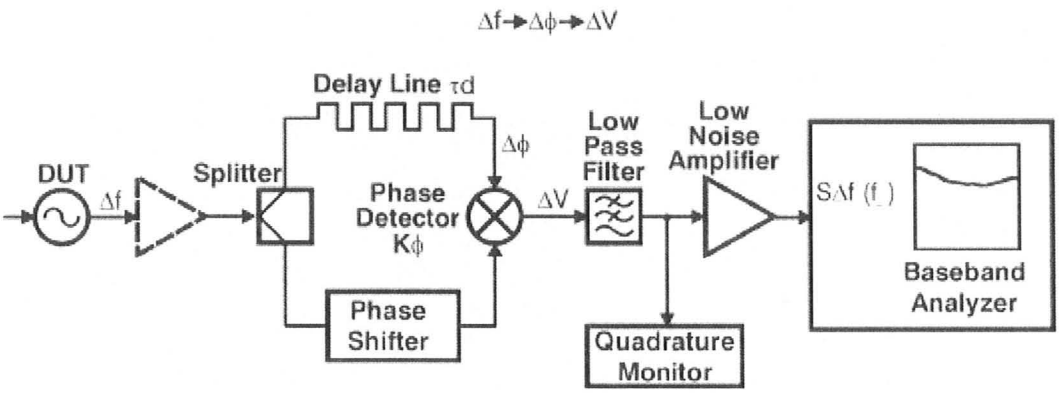


Fig 3.6: Basic frequency discriminator method. [31]

3.5.3 PLL-based Technique

PLL-based technique is another method which requires a second reference source. The phase of the oscillator under test (DUT) is compared with a reference oscillator or a VCO, which usually has a similar or better phase noise performance.

PLL-based technique is an accurate but complicated and expensive method. It requires an external reference source and the measurement sensitivity is limited by the noise floor of the reference source.

3.6 Phase Noise Fluctuations

In [32], Mossammaparast et al. observed phase noise fluctuations in the measurement of Low Noise Regenerative Dividers, as shown in Figure 3.7. They explained this phenomenon as a result of the electromagnetic effect associated with the cooling fans used in the Sapphire Loaded Cavity Oscillator.

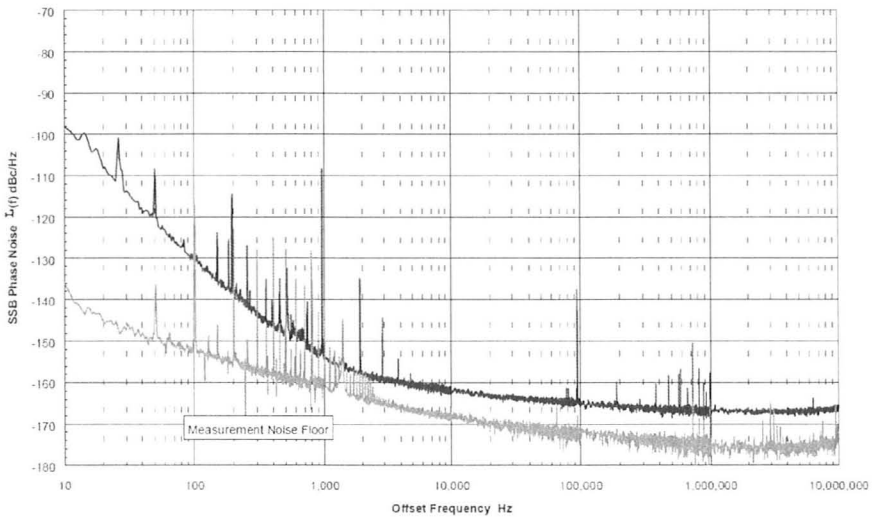


Fig 3.7: Illustration of Phase noise spurs in low noise regenerative divider [32]

Lance et al. [33] explain that the spurs appearing below 1000Hz come from the 60 Hz power line frequency and its harmonics. Their results are reproduced in Figure 3.8. According to this explanation, phase noise fluctuations do not contribute to the oscillator phase noise. Similarly, Nick et al [34] found the spurs at frequency offsets of 150Hz, 250Hz, 350Hz, etc. when they were measuring inter-injection-locked (IIL) oscillators. Leakage of the AC power line harmonics was again hypothesized to be the main cause of the phase noise spurs.

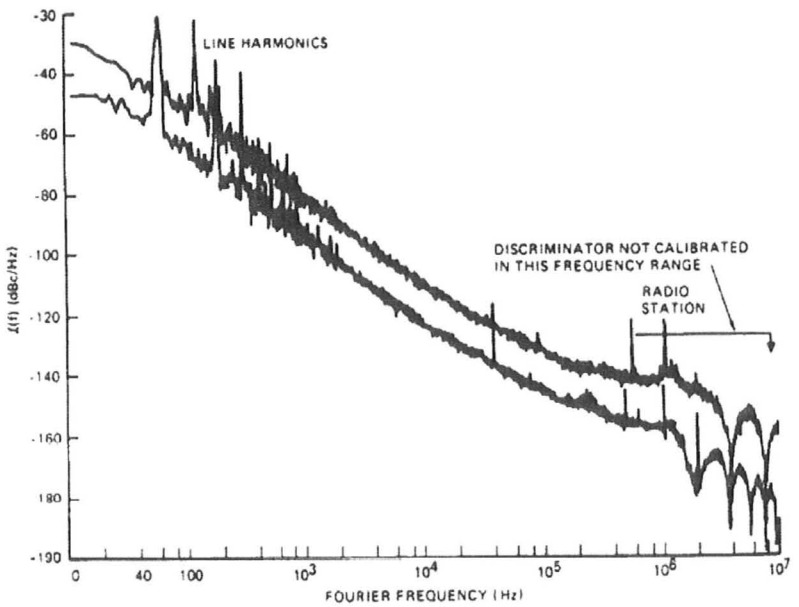


Fig 3.8: Phase noise measurements at 600MHz and 2.4GHz frequencies [33]

Mendez et al [35] explained the spurs observed in their measurements at an offset of 10Mz as coming from the harmonic component of the digital clock frequency. The substrate noise is generated by a digital circuit which is put below the VCO test chip. Figure 3.9 shows that when the digital circuit is not activated (turned off), the spurs at 10 MHz are largely improved.

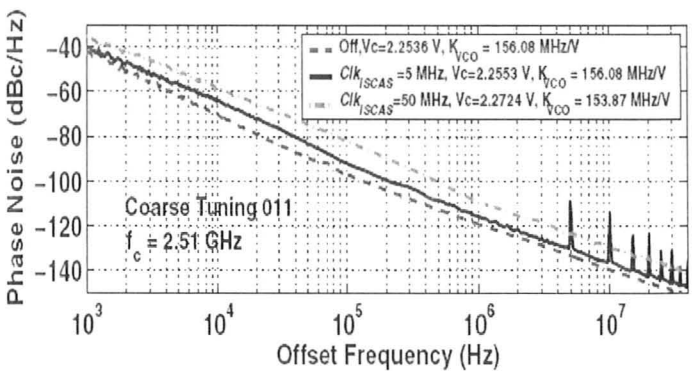


Fig 3.9: M.A. Mendez et al's phase noise measurement [35]

Maxim [36] proposed that the spurs in the phase noise measurements of LC-VCO could be improved by introducing partial metal cage inductor structure. This proposed inductor could reject the parasitic coupling digital noise.

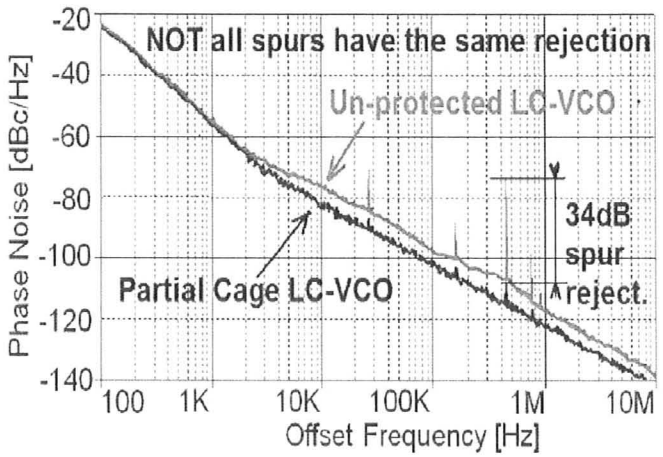


Fig 3.10: Comparison of caged and non-caged inductor VCOs [36]

These studies may then be classified into two main scenarios as pertains to phase noise fluctuations:

1. cases where the fluctuations are caused by noise sources outside of the chip: clock frequencies of the measurement instruments, power line interference, etc; and

2. cases where the fluctuations are caused by the noise inside the test chip: inductor structure, substrate noise, etc.

To filter wanted external noise from the first source, appropriate care in setting up the source measurement was taken. As the second source originates from the actual circuit design and device parasitic of the technology used, amending the design itself is needed to address phase noise of internal noise.

3.7 Summary

This chapter explained the definition of phase noise, followed by a brief introduction to different models.

Phase noise measurements are also discussed in this chapter. Literatures are summarized at the end which provides potential sources that could cause phase noise fluctuations.

Chapter 4

VCO

A voltage-controlled oscillator or VCO is an oscillator which is designed to control the oscillation frequency by changing the DC voltage input. There are many different topologies to realize an oscillator.

Figure 4.1 and Figure 4.4 illustrate two basic topologies. The first one is a three-stage ring oscillator, shown in Figure 4.1. The oscillation frequency is determined by:

$$f = \frac{1}{2 \cdot N \cdot t_d} \tag{4.1}$$

where N is the number of inverters in the ring oscillator and it must be an odd number, t_d is the propagation delay time for each inverter, which is equal to:

$$t_d = t_{PHL} + t_{PLH} \tag{4.2}$$

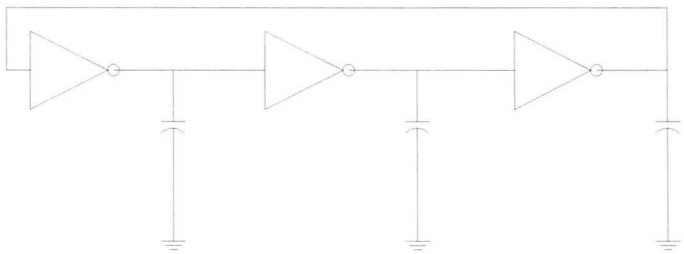


Fig 4.1: Basic topology of a three-stage ring oscillator

Consider this a single stage ring oscillator whose equivalent circuit is shown in Figure 4.2. Output of the circuit denoted as *out* is connected to the VCC (i.e., logic 1) when PMOS is ON and NMOS is OFF or connected to GND (i.e., logic 0) when PMOS is OFF and NMOS is ON.

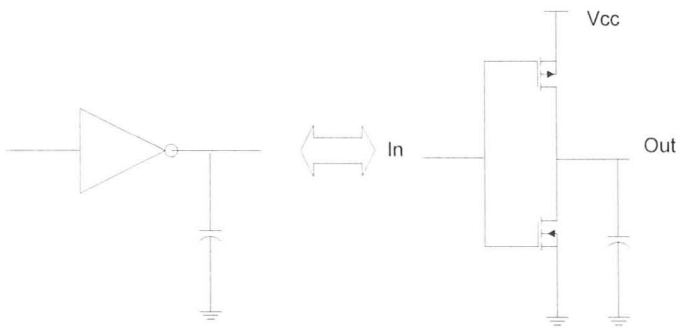


Fig 4.2: The equivalent circuit of a single stage of ring oscillator

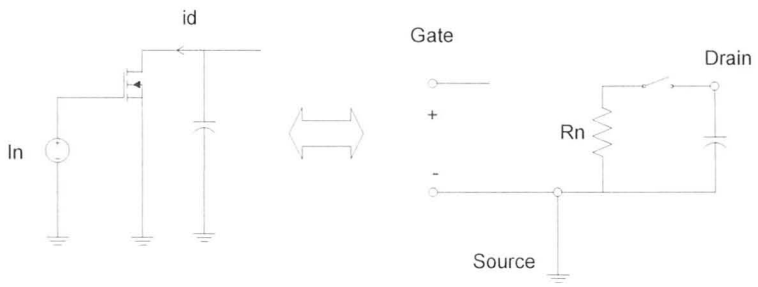


Fig 4.3: The equivalent circuit of a NMOS

An equivalent circuit is illustrated in Figure 4.3 when input is set to logic 1, neglecting the parasitic capacitance of MOSFETs. MOSFET is replaced with a series connection of a resistor and a switch. The switch opens when $V_{gs} < V_{CC}/2$ and closes when $V_{gs} > V_{CC}/2$. The effective resistance R_n is expressed as:

$$R_n = \frac{V_{CC}}{\frac{1}{2} * \mu_n * C_{ox}^{'} * \frac{W_n}{L_n}(V_{CC} - V_{thn})^2} \tag{4.3}$$

The time delay of the inverter could be expressed as:

$$t_{PLH} = R_n * C \tag{4.4}$$

Similarly, to analyze the falling time for the inverter, the input state is changed to logic 0. Then NMOS is turned off while PMOS is turned on. The delay time is

$$t_{PHL} = R_p * C \tag{4.5}$$

$$= \frac{V_{CC}}{\frac{1}{2} * \mu_p * C_{ox}^{'} * \frac{W_p}{L_p}(V_{cc} - V_{thp})^2} * C \tag{4.6}$$

Therefore, the delay time is

$$t_d = t_{PHL} + t_{PLH} \tag{4.7}$$

$$= R_p * C + R_n * C \tag{4.8}$$

$$= (R_n + R_p)C \tag{4.9}$$

The oscillation frequency of the ring oscillator is determined by the effective resistances of MOSFETs and the output capacitance C.

In comparison with ring oscillators, the LC-tuned VCOs usually have better phase noise performance. This is due to the increase in phase noise in a ring VCO as the number of stages rises.

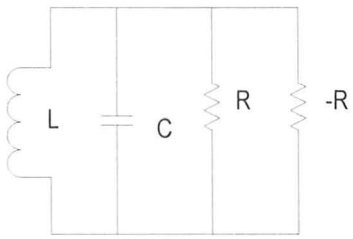


Fig 4.4: Parallel LC oscillator model

Figure 4.4 shows the model for a typical parallel LC oscillator, where R represents the tank loss and –R represents the effective negative resistance which could compensate the losses in R in the tank. From Kirchhoff's voltage law, voltage across the inductor L is equal to the voltage across the capacitor C and the resistors R and -R.

$$V_L = V_C = V_R = V_{-R} \tag{4.10}$$

And by Kirchhoff's current law,

$$i_L + i_C + i_R + i_{-R} = 0 \tag{4.11}$$

The impedance of the inductor L and the capacitor are $Z_L = j\omega L$ and $Z_C = \frac{1}{j\omega C}$, the equation could be written as:

$$\frac{V}{j\omega L} + \frac{V}{\frac{1}{j\omega C}} + \frac{V}{R} + \frac{V}{-R} = 0 \tag{4.12}$$

where frequency could be expressed as:

$$\omega = \sqrt{\frac{1}{LC}} \tag{4.13}$$

Therefore oscillation frequency in unit hertz is:

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{4.14}$$

Negative resistance can be generated using a pair of NMOS and PMOS, as illustrated in the following figures. The equivalent circuit for generating negative resistance is shown in Figure 4.5 (a) and (b). From Figure 4.5 (b):

$$I_{DC} = g_{m1}V_1 = -g_{m2}V_2 \tag{4.15}$$

Since $g_{m1} = g_{m2}$, $V_1 = -V_2$, which concludes that:

$$V_{DC} = V_2 - V_1 = -2V_1 \tag{4.16}$$

Therefore, the equivalent resistance of the cross-coupled pair is:

$$\frac{V_{DC}}{I_{DC}} = \frac{-2V_1}{g_{m1}V_1} = -\frac{2}{g_{m1}} = -\frac{2}{g_{m2}} \tag{4.17}$$

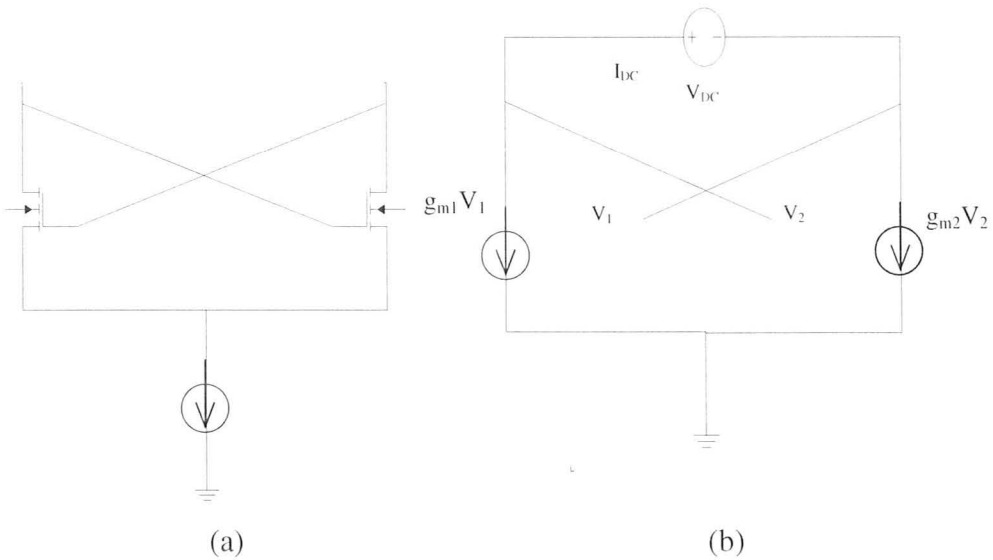


Fig 4.5: (a) An NMOS cross-coupled pair, and (b) The equivalent circuit of cross-coupled pair

It is well-known that MOSFET usually have better phase noise performance than BJT devices due to high linearity. Figure 4.6 shows the basic topologies of three different LC-tuned VCOs.

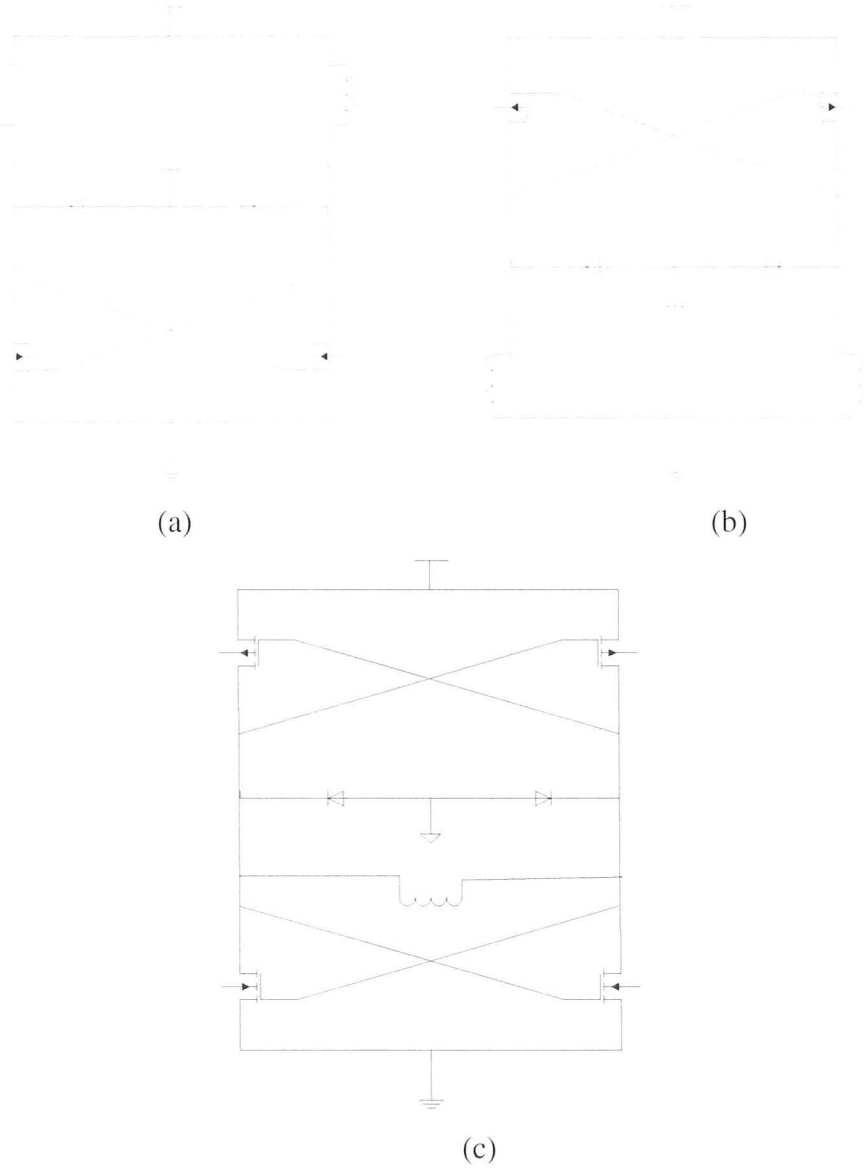


Fig 4.6: Three basic LC-tuned VCO topologies (a) NMOS cross-coupled, (b) PMOS cross-coupled, and (c) complementary cross-coupled

The advantages of NMOS cross-coupled VCO shown in Figure 4.6 (a) are:

- Requires smaller size to achieve equivalent gain as compared to PMOS cross-coupled topology and therefore, has less parasitic capacitance.
- Consumes less power as it requires fewer components as compared to complementary cross-coupled topology.

The advantages of PMOS cross-coupled VCO shown in Figure 4.6 (b) are:

- The flicker noise of PMOS is less than that of NMOS. [37]
- Since the size of PMOS is larger than NMOS, when achieving the same gain, the supply voltage could also be increased.
- Consumes less power as it requires less components as compared to complementary cross-coupled topology

The last topology uses both NMOS and PMOS to realize VCO.

- Both NMOS and PMOS cross-coupled pairs could provide negative resistance

The tuning range of an LC-tuned VCO is controlled by $1/\sqrt{L(C_b + C_{VAR})}$ since varactor is a voltage-controlled capacitor. C_b is the capacitance of the fixed capacitor or in some cases, the parasitic capacitance, C_{VAR} is the capacitance of the varactor. LC-tuned VCOs usually have higher phase noise than fixed-frequency oscillators because of the limitation of the resonator Q factor and the increased white noise induced by the varactors. [38]

4.1 LC-tuned VCO Phase Noise

Complementary cross-coupled LC-tuned VCO is used in this thesis to study phase noise performance. The negative resistances generated by cross-coupled NMOS and PMOS transistors pairs are denoted by $-R_{PMOS}$ and $-R_{NMOS}$ in Figure 4.7. Transistor M_5 provides the bias current; C_V represent varactors capacitors, and C_b represent fixed value capacitors. In the next few sections of this chapter, we will discuss several design

parameters that need to be taken into consideration to improve the phase noise performance of the VCO.

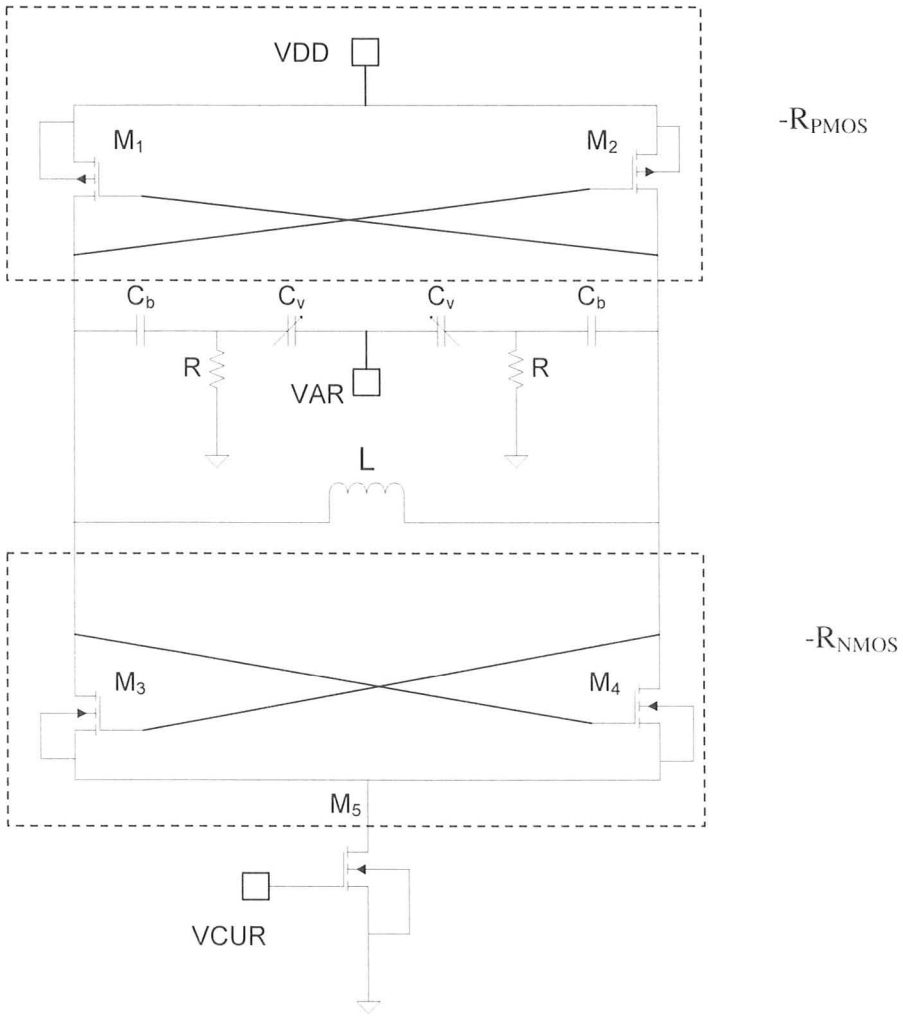


Fig 4.7: Schematic view of the LC-tuned VCO

4.1.1 Quality Factor

It is already shown that the overall Q of the circuits could determine the phase noise level of the VCO to a large extent. To design a low phase noise VCO, the Q factor of the resonator, the inductor and the varactor must be as high as possible.

The Q of a resonant circuit, can be expressed as

$$Q = \frac{f_o}{\Delta f} \tag{4.18}$$

where f_0 is the resonant frequency (center frequency). Δf is the bandwidth, which is the width of the range of frequencies where the energy is half of the peak value, see Figure 4.8.

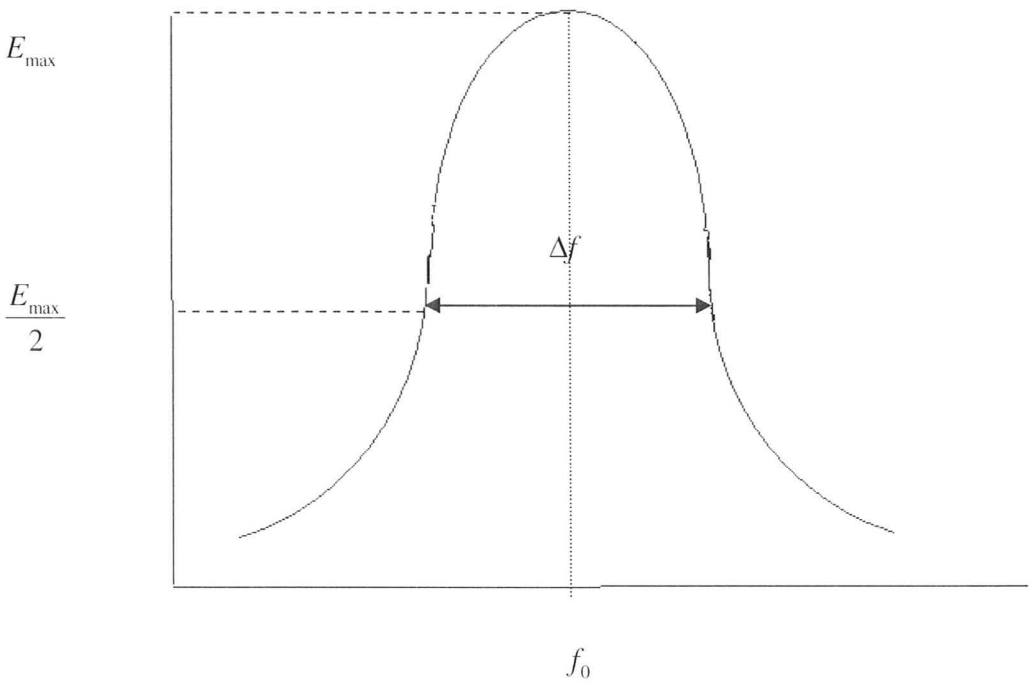


Fig 4.8: Energy versus frequency

In a high Q circuit design, the tuning bandwidth is small. Therefore a low phase noise VCO design must have a small tuning range. In a series or parallel RLC circuit, the Q factor is:

$$Q = \frac{1}{R}\sqrt{\frac{L}{C}} \tag{4.19}$$

From the expression for the resonant frequency of a tuned circuit,

$$\omega = \sqrt{\frac{1}{LC}} \tag{4.20}$$

we can derive the following formula:

$$Q = \frac{\omega L}{R} \tag{4.21}$$

The overall Q factor is inversely proportional to the effective resistance R_{eff} whose value is determined by all parasitic resistances. In order to have low phase noise and power consumption, the effective resistance must be kept low. That is, the overall Q must be as high as possible. [25]

The overall Q factor can be expressed as:

$$\frac{C_T}{Q_T} = \frac{C_L}{Q_L} + \frac{C_V}{Q_V} + \frac{C_b}{Q_b} \text{ with } C_T = C_b + C_V \tag{4.22}$$

where Q_T is the overall Q factor, Q_L is the Q factor of the inductor, Q_V is the varactor Q factor, Q_b is the fixed capacitor Q factor.[39]

From equation 4.22, the overall Q of the resonator is the "parallel" combination of the individual Q factors, and hence, the overall Q will be smaller than the smallest Q in the circuit. To maximize the overall Q of the resonator and improve the phase noise, the Q of the inductor must be as high as possible, that is, the series resistance of the inductor must be as low as possible to lower the phase noise and power consumption.

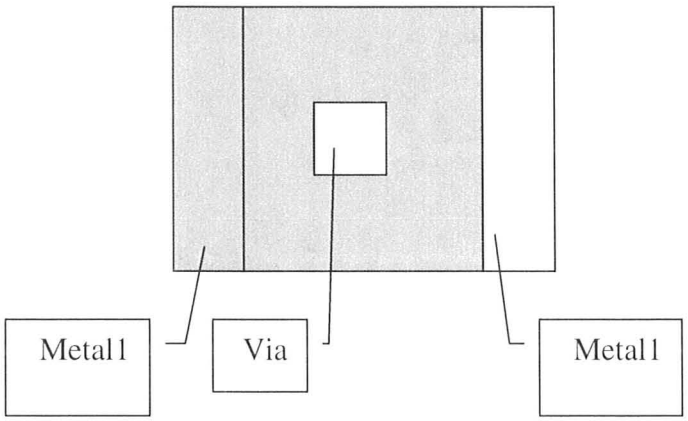
4.1.2 Layout design

From Lee and Hajamiri's model, the shape of the output waveform could change the DC value of the ISF, thus impacting the phase noise performance of the VCO. To optimize the phase noise, the circuit needs to be symmetrical and with the same

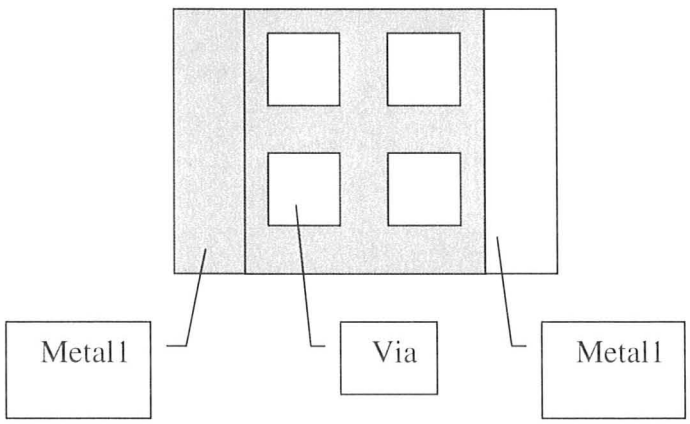
orientation. From MOSFETs to resistors, every cell in the VCO must be carefully laid out to be as symmetric as possible.

In some situations, it is difficult to have a fully symmetric inductor and capacitor layout. In these cases, two identical inductors or capacitors could be used separately in the tank.

From Craninckx's phase noise equation, one of the most important parameter to influence phase noise is the LC-tank's effective resistance, that is, the parasitic resistance of the VCO. IC designers must be careful with the layout so as to introduce as little parasitic elements into the circuits as possible. For example, Figure 4.9 shows two layout designs of the vias which is used to connect two metal layers. Figure 4.9(a) uses only 1 via and it is assumed that the resistance for 1 via is 1Ω and the maximum current flow is 1A. Compared to (a), Figure 4.9(b) includes more vias and shows 4 vias connected in parallel between the two metal layers. So the total resistance becomes 1Ω/4=0.25Ω, and the maximum current flow is increased to 1A*4=4A. From this example we could see that the layout design is very important in determining the parasitic resistance.



(a) 1 via between two metal layers



(b) 4 vias between two metal layers

Fig 4.9 Two layout designs of vias

4.1.3 Varactor design

There are three different kinds of varactors: inversion-mode MOS varactor (I-MOS), accumulation-mode MOS varactor (A-MOS), and diode varactor. In [40], the phase noise of different LC-tuned VCOs using these three varactors are measured at 1.8GHz carrier frequency. As shown in Figure 4.10, there is no significant difference in performance at offset frequencies below about 100 kHz. However, at higher offset frequencies, MOS varactors outperform diode varactors. Between I-MOS and A-MOS, the I-MOS VCO significantly performs better.

However, the data of Figure 4.10 consider VCOs with the same power supply voltage, same center frequency and tuning range. Since current consumption is different in each design, the total power is different. The Diode consumes the most power, while A-MOS consumes the least power. As shown in Figure 4.11, a comparison [41] between two CMOS VCOs tuned by a diode varactor and a MOS varactor, respectively, shows that diode varactor VCO produces lower phase noise than MOS varactor VCO when power consumptions are the same, that is, the layout of varactors design makes both supply voltage and current consumption the same.

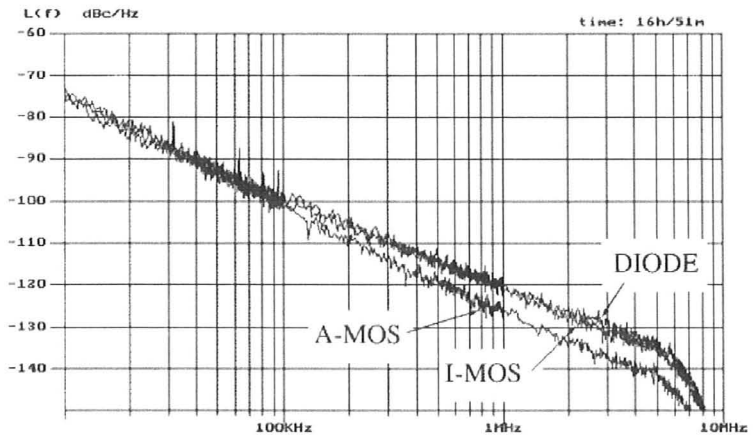


Fig 4.10: Phase noise performance of three VCOs with diode varactor, A-MOS varactor, and I-MOS varactor [40]

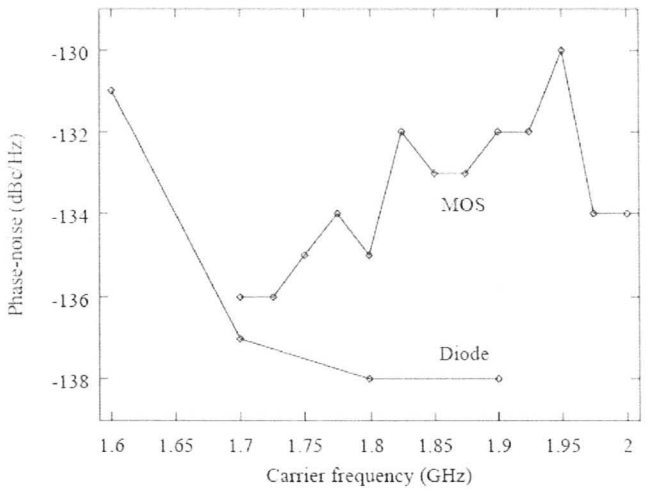


Fig 4.11: Phase-noise at 3MHz from the carrier as function of the carrier frequency [41]

In VCO, amplitude-modulation (AM) noise could be converted to frequency-modulation (FM) noise by using varactors. [42][43] This conversion is another source of phase noise. Single-sideband-to-carrier ratio (SSCR) can be expressed by the sensitivity coefficient

$$K_{AM-FM} = \frac{\partial \omega}{\partial A} = \frac{\partial}{\partial A}\left(\frac{1}{\sqrt{LC}}\right) = -\frac{1}{2}\frac{\omega_0}{C}\frac{\partial C}{\partial A} \tag{4.23}$$

which represents the sensitivity of the oscillation frequency to variation of the oscillation amplitude A. The resulting phase noise is given by:

$$L(\omega_0) = \frac{K_{AM-FM}^2 \cdot S_{AM}(\omega_0)}{2\omega_0^2} \tag{4.24}$$

where $S_{AM}(\omega_0)$ is the AM voltage spectral density on the oscillation envelope.

4.1.4 Flicker Noise Up-conversion

In a VCO, close-in phase noise is the phase noise at a small offset frequency caused by the upconversion of flicker noise. There are two mechanisms for the flicker noise to be upconverted to the $1/f^3$ phase noise.

The first mechanism is frequency doubling that occurs when the flicker noise from the tail current source enters MOSFETs. Then noise frequency becomes twice the oscillation frequency $2\omega_0$ at the common node of the differential VCO through the effect of channel length modulation due to the switching of the MOS differential pair. The noise at $2\omega_0$ will mix with the fundamental frequency when entering the LC tank. This is the main cause of the phase noise sidebands at the oscillation frequency. [44]Phase noise could be improved by suppressing the 2nd harmonic at the tail node. [45] proposed a harmonic tuning VCO to improve phase noise performance.

The second mechanism is due to the mixing action of the VCO. Flicker noise from the tail current source is upconverted to the oscillation frequency f_0 . [46] suggests

that this upconversion could be reduced by minimizing C_0, the DC value of the ISF. And since C_0 depends on the waveform, the choice of waveforms could improve the close-in phase noise. This can be done by making the g_m of NMOS and PMOS equal.

4.2 Phase Noise Fluctuations

In Section 1.3 we discussed the phenomenon of phase noise fluctuations along with possible causes and remedies. In previous work done in our research group at McMaster University, phase noise fluctuations at an offset of ~100kHz were observed in an LC-tuned VCO design [11], as shown in Figure 4.12. The objective of this thesis is to understand how such fluctuations may be reduced or eliminated.

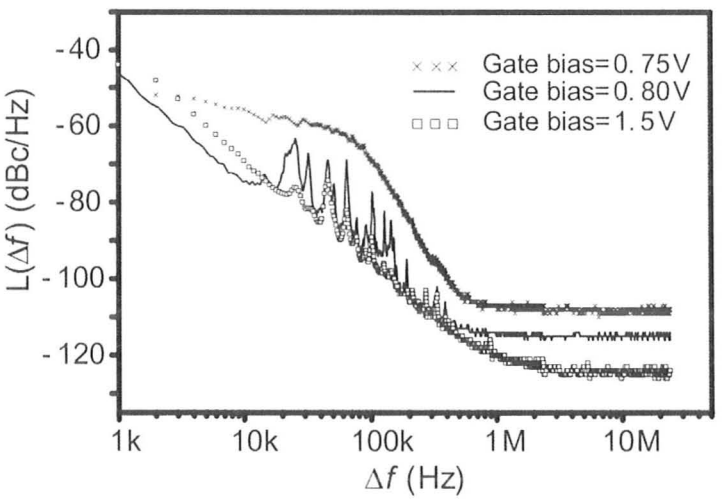


Fig 4.12: Munir's phase noise measurement results [11]

To achieve this goal, six versions of the 2.4GHz VCOs were fabricated. Each version makes one specific modification to the design or layout in order to isolate the underlying cause of the phase noise fluctuations. Fabrication was done by the TSMC (Taiwan Semiconductor Manufacturing Company) 6-metal layer, 0.18 μm standard

mixed-signal CMOS technology, with a 2 μm thick top-metal layer. The die-photograph of the fabricated chip is shown in Figure 4.13. The whole chip occupies an area of 5.5mm^2, while each circuit occupies an area of 0.7mm^2. Circuit simulation was carried out by the simulation tool Spectre-RF.

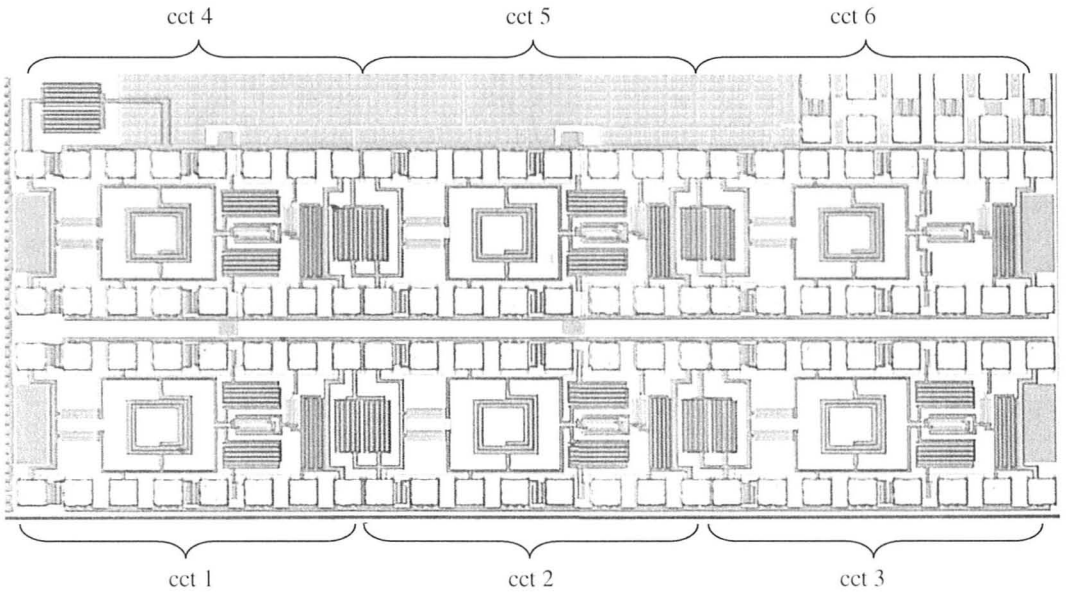


Fig 4.13: Photograph of the six circuits

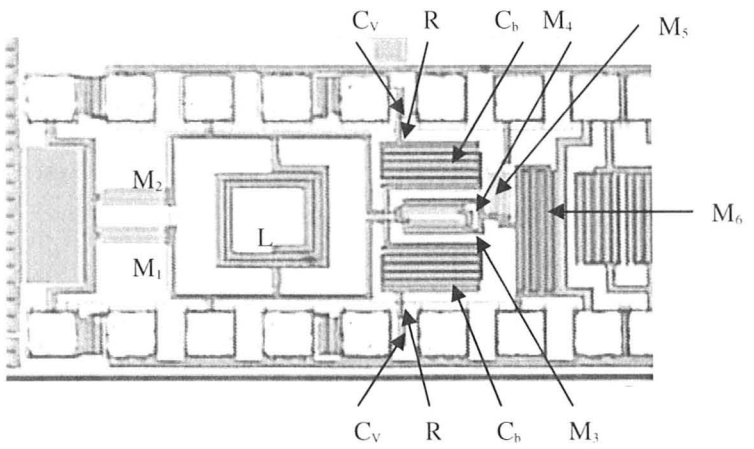


Fig 4.14: Photograph of fabricated VCO cct 1

For our discussion, we will conveniently name the different VCOs designs as cct 1 to cct 6. Figure 4.14 shows a photograph of cct 1. The PMOS devices (M_1 and M_2) each have 140 fingers, giving a total width of 350μm while the gate length is 0.18μm. The NMOS devices (M3 and M4) each have 70 fingers, with a total width of 175μm. The inductor L is 2.3nH with a quality factor of 8. The capacitors C_b are 12pF while resistors R are 50kΩ. Transistors M_5 and M_6 are tail current sources. M_5 has 100 fingers and an aspect ratio of 250μm/0.18μm. M_6 is a long channel device that has 500 fingers with an aspect ratio of 1250μm/1μm. Each of the RF outputs goes to the 50Ω load of the measurement equipment directly without a buffer. The cct 1 schematic of the 2.4GHz VCO is shown in Figure 4.15.

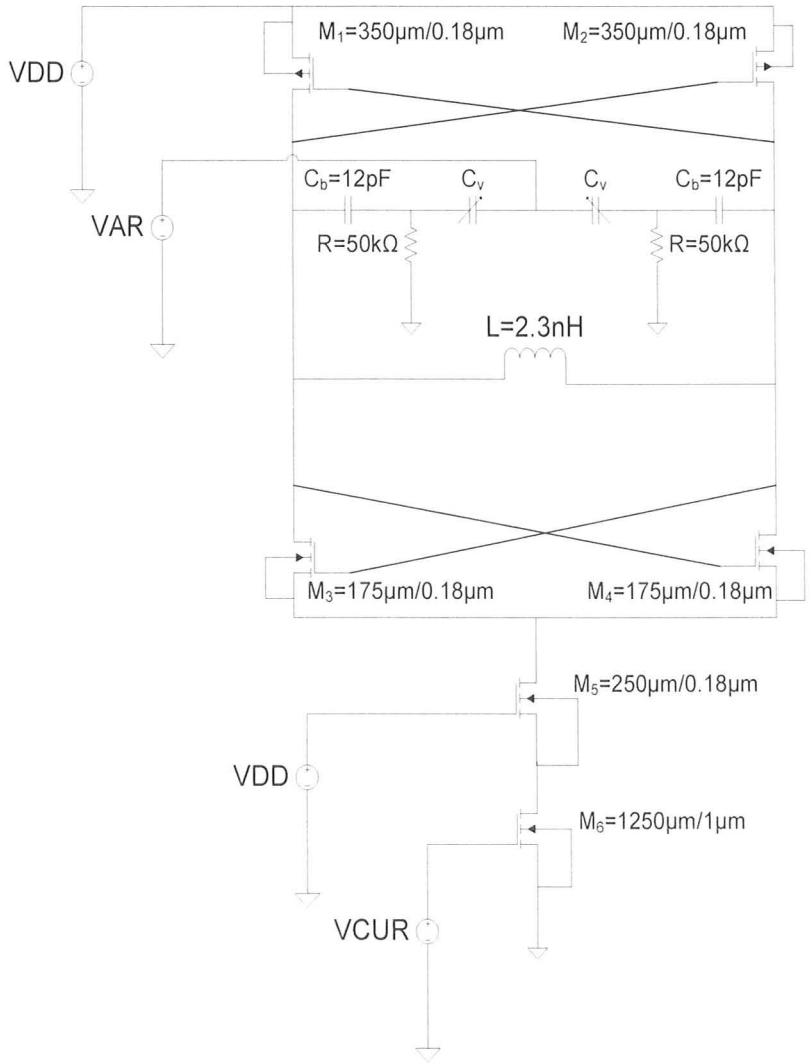


Fig 4.15: Schematic of the cct 1 VCO design

As mentioned earlier, five different versions of the circuit were designed and fabricated. The differences between the five designs (summarized in Table 4.1) are:

- Other than cct 1, all other five circuits have two large DC filter capacitors of 12pF between VDD and ground;
- Cct 3 and cct 5 have smaller bias resistors R, with a value of 30kΩ;
- Cct 4 and cct 5 have MOS varactors with a higher Q factor;

- Cct 5 has the inductor L enclosed in a deep n-well (DNW); and
- Cct 6 has a smaller blocking capacitor C_b.

	Large DC filter Capacitor	Bias Resistor R(k Ω)	Varactor with better Q factor	Deep n-well inductor L	Smaller Blocking Capacitor C_b
cct 1		50k			
cct 2	×	50k			
cct 3	×	30k			
cct 4	×	50k	×		
cct 5	×	30k	×	×	
cct 6	×	50k			×

Table 4.1: Comparison between the six presented VCO designs

The DC filter capacitors are used between the power supply and ground to filter out the uneven DC supply signal.

The DNW structure used in cct 5 should effectively isolate substrate coupling. By forming an n+ high conductive layer above the substrate, the substrate resistance and effective capacitance are largely reduced. [47][48] Since the Q factor is inversely proportional to the resistance and the capacitance, the quality factor of the proposed inductor should be increased.

In cct 4, a better Q varactor is designed. Compared to the other varactor, this one has wider metal interconnections between the multi fingers.

Theses different modifications account for possible sources of phase noise fluctuations identified in the literature and described in the previous chapter. In Chapter 5 we will analyze the measurements made on these circuits in an attempt to identify the dominant source of these fluctuations as well as the means to minimize such fluctuations.

Chapter 5

MEASUREMENT RESULTS

As stated earlier, our objective is to analyze phase noise fluctuations in a 2.4GHz LC-tuned VCO. Our approach was to (1) review the literature to understand the phenomenon of phase noise fluctuations, (2) identify possible sources of phase noise fluctuations in our design, and (3) fabricate modified circuits to test each of the components that potentially contribute to these fluctuations. In this chapter we describe our measurements and analyze the results.

Section 5.1 presents the measurement setup. We performed two sets of measurements: phase noise of the VCO as a function of frequency offset and DC measurements that characterize the performance of the VCO (including its oscillation behaviour) in response to the supplied DC bias voltage. Section 5.2 presents the DC measurement results and section 5.3 presents the phase noise measurement results.

5.1 Measurement Setup

Figure 5.1 illustrates the experiment setup for the measurements. The chip is set under a microscope to allow visual alignment with the probes. The probes are then placed securely onto respective contacts of the chip to connect the chip with the instruments. The HP-4145B semiconductor parameter analyzer (SPA) is used to provide the bias voltage for measuring DC power. A McMaster custom-made dry battery box is used to provide the bias voltage for phase noise measurements. The battery box provides constant voltage to minimize the noise generated from the parameter analyzer for more accurate measurements. An E4440A Series Spectrum Analyzer, with operating range from 3Hz to 26.5 GHz, is used for displaying output frequency spectrum and phase noise measurement.

In the context of this research thesis, six chips of each containing a different version of VCO circuit are carefully studied and examined (see Figure 4.13). We need to ensure that the same test is conducted three times or more for each experiment. There are two methods used to achieve this goal:

1. The series of measurements was conducted once on all the six chips.
2. Based on the results that we got from the first run, we selected for each circuit version a chip that had typical performance and ran the same experiments three times on it. In between these three experiments, the probes are lifted and lowered down again to avoid errors from different probe locations. An average of the three experiments is taken from the test data collected which will be used as the result for our discussion.

Three bias voltages are provided in this setup: VDD (DC Supply voltage), VAR (voltage to control the varactor), and VCUR (tail current source bias). Figure 4.15 shows that two bias voltages are needed for the tail current transistors. However, again with reference to the figure, one of them is already connected to the VDD supply voltage, and therefore we only have one variable, VCUR.

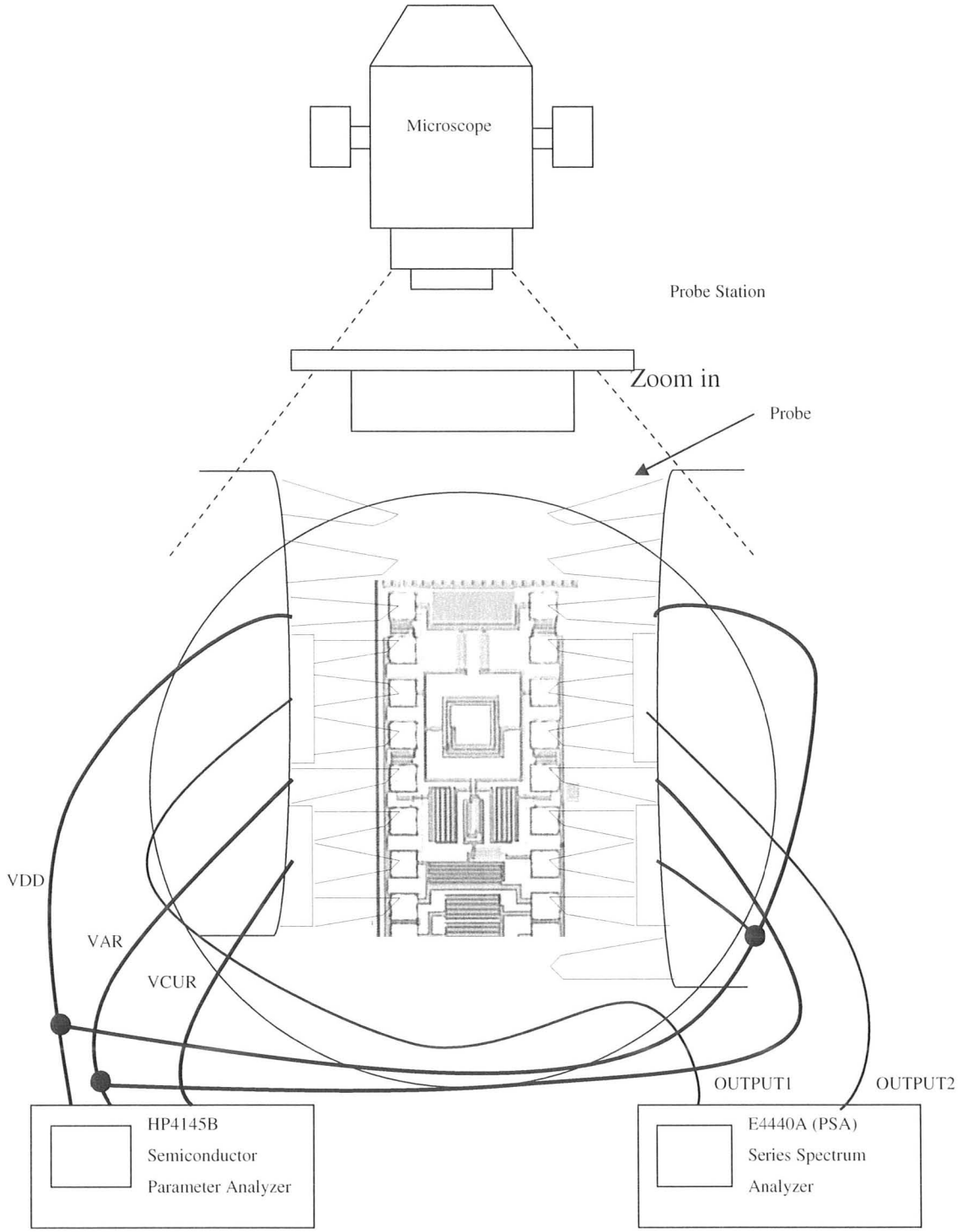


Fig 5.1: Experimental setup for phase noise measurement

5.2 DC Measurement Results

For the DC measurements we change the values of three bias voltages: VDD, VAR and VCUR. When one bias voltage is changed, the other two are kept at the nominal value of 1.5V. The primary performance parameters thus measured are the drain efficiency and oscillation frequency.

Drain efficiency is defined as the ratio of output power to the DC supply power:

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{P_{out}}{V_{DC} \times I_{DC}} \tag{5.1}$$

The supply current could be read directly from the semiconductor parameter analyzer (SPA).

Figure 5.2 and Table 5.1 show the measured drain efficiency as a function of the supply voltage VDD, with VAR and VCUR biased at 1.5V. The supply voltage is swept from 1.2V to 1.8V. Recall from Figure 4.15 that VDD is also the gate bias for M_5. Below 1.2V, M_5 would not turn on, there is no output power and the efficiency would be zero. From 1.3V to 1.8V, the output power is increased as the input power is increased. Cct 6 with a smaller blocking capacitor has the overall best efficiency performance among all the circuits. The original circuit without any of the modifications tried here has the worst performance.

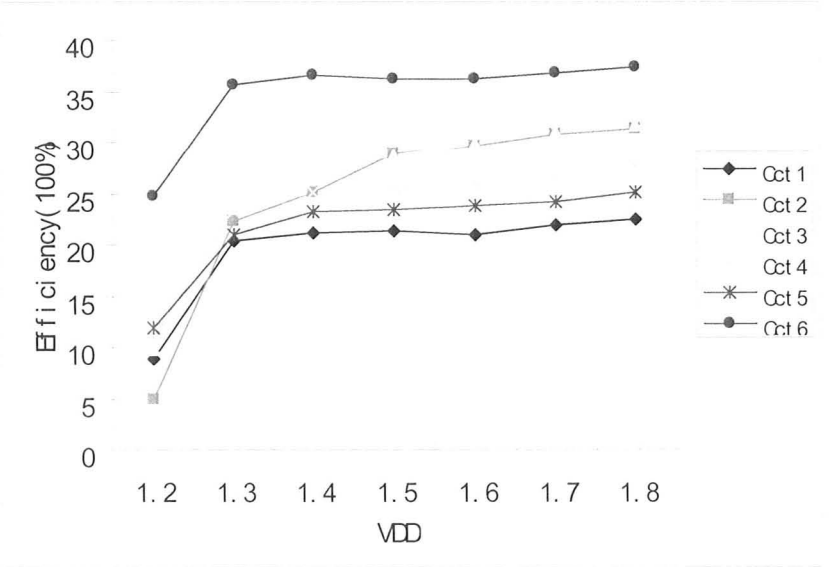


Fig 5.2: Measured drain efficiency, as a function of the supply voltage

	Supply Voltage		
	1.2V	1.5V	1.8V
Cct 1	8.872324	21.26996	22.45562
Cct 2	4.826281	28.78535	31.38336
Cct 3	9.80628	28.63389	31.70506
Cct 4	10.95986	25.47962	27.70673
Cct 5	11.80449	23.48193	25.05988
Cct 6	29.67629	36.23124	37.27694

Table 5.1: A summary of the measured efficiency

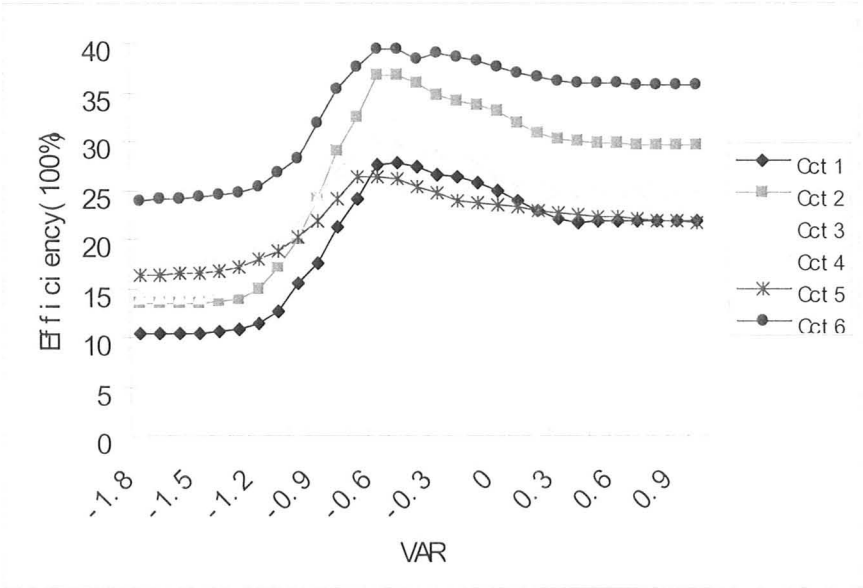


Fig 5.3: Measured drain efficiency, as a function of the varactor voltage

Figure 5.3 shows the measured drain efficiency as a function of the varactor voltage VAR, which was swept from -1.8V to 1.2V, with VDD and VCUR biased at 1.5V. When VAR is above 1V, the efficiency saturates and becomes independent of VAR. For all the circuits, peak efficiency occurs at a bias of VAR = -0.6V.

Figure 5.4 shows the measured drain efficiency as a function of the tail current source VCUR, which was swept from 0.6V to 1.8V with VAR and VDD held at 1.5V. When VCUR is below 0.6V, the tail current source MOSFET M_5 is not turned on and the drain efficiency is zero.

Based on all these measurements, cct 6 has the best drain efficiency, followed by cct 2, 3, 4, and 5. The original design, cct 1, has the worst drain efficiency performance. This illustrates the importance of the blocking capacitor to the efficiency of the circuit. The smaller blocking capacitor C_b, the higher efficiency is the circuit.

Cct 2&3 differ from 4&5 in the varactor design, cct 4&5 have a better Q varactor. The better Q is realized by enlarging the metal interconnections between the multi fingers.

Therefore, extra resistance is introduced to the varactor design. It causes the lower efficiency of the circuit design.

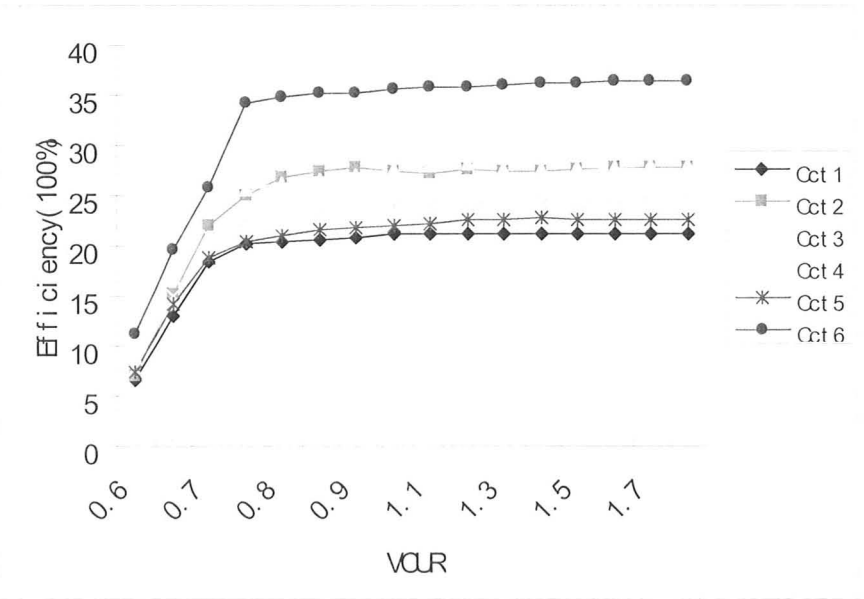


Fig 5.4: Measured drain efficiency, as a function of the tail current voltage

Figures 5.5– Fig 5.7 show the measured frequency as a function of the supply voltage VDD, varactor voltage VAR, and tail current source VCUR. Table 5.2 summarizes the measured frequency values as a function of VDD.

In Figure 5.5, cct 1 is closest to the design frequency 2.4GHz when VDD is below 1.3V. At VDD=1.3V, cct 3, 4&5 have the closest frequency. From 1.4V-1.8V, cct 6 is the closest. Overall, the entire supply voltage bias, cct 2, has the worst performance. Cct 4&5 have the largest tuning range 0.15GHz, followed by cct 1&3. Cct 2&6 have the minimum tuning range.

In Figure 5.6, the data only shows the varactor voltage only biased from -1.8V to 0.9V. That is because above 0.5V, the frequency shows very little changes. So it could be considered that the frequency is the same after VAR=0.5V.

For all three bias voltages, frequency drops as the increase of the supply voltage, and the tail current voltage. As the varactor voltage, there is a peak frequency that happens around VAR=-0.6V for cct 2, 3, 4&5. The performance of cct 1&2 is different from other four circuits, that is, the peak frequency happens at lower voltage.

Overall, cct 3, 4&5 are closer to the design frequency at all bias voltages than other three circuits. In Figure 5.5 and Figure 5.7, cct 6 has the highest frequencies at lower voltage and cct 2 has the lowest frequencies at higher voltage.

Care must be taken with the probe-pad contact during frequency measurements. A significant source of error in measurement is the poor contact between the probe tip and the I/O pads of the circuit. Our experimental setup and procedure have been carefully controlled to yield reliable measurements.

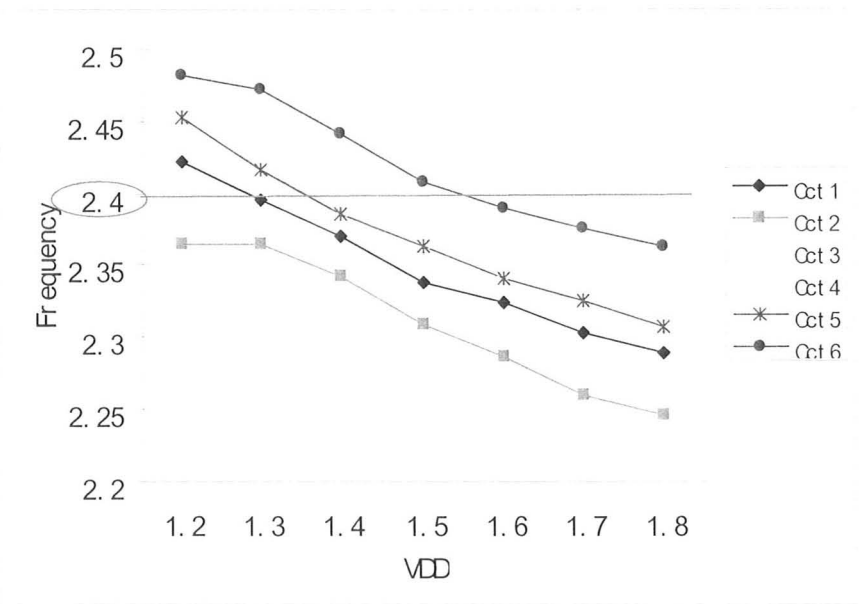


Fig 5.5: Measured frequency, as a function of the supply voltage

	Supply Voltage			Tuning Range
	1.2V	1.5V	1.8V	
Cct 1	2.42208	2.33866	2.2898	0.132
Cct 2	2.364225	2.30886	2.24594	0.118
Cct 3	2.45644	2.37164	2.3266	0.130
Cct 4	2.458667	2.3576	2.3027	0.156
Cct 5	2.45292	2.3637	2.30786	0.145
Cct 6	2.482267	2.402983	2.36283	0.119

Table 5.2: A summary of the measured frequency

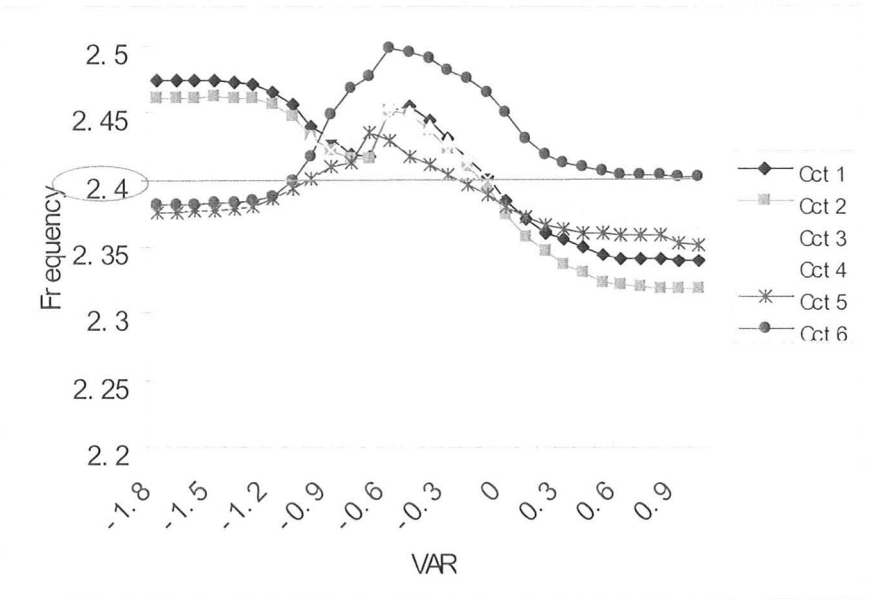


Fig 5.6: Measured frequency, as a function of the varactor voltage

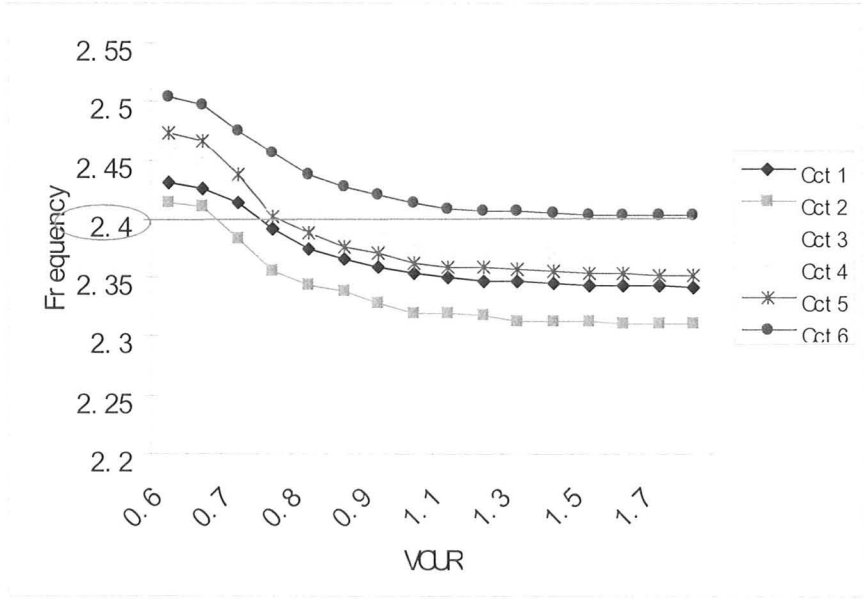


Fig 5.7: Measured frequency, as a function of the tail current voltage

5.3 Phase Noise Measurements

In making the phase noise measurements, we no longer use the HP4145B Semiconductor Parameter Analyzer to provide the DC bias. Here a McMaster custom-made dry battery box is used instead. The reason for this is to try to protect against noise generated from the Semiconductor Parameter Analyzer. All three voltage sources are biased at 1.5V. Finally, data presented here are averages from multiple measurements on at least two individual chips for each circuit.

Figure 5.8 shows a comparison between the phase noise measurements of the six circuits and the cadence simulation results. The cadence simulation uses cct 1 to be considered as a reference. Clearly, the simulation simply does not predict the observed phase noise fluctuations. For clarity, we have separately shown the measurement results for each of the different circuits in Figures 5.9-5.14.

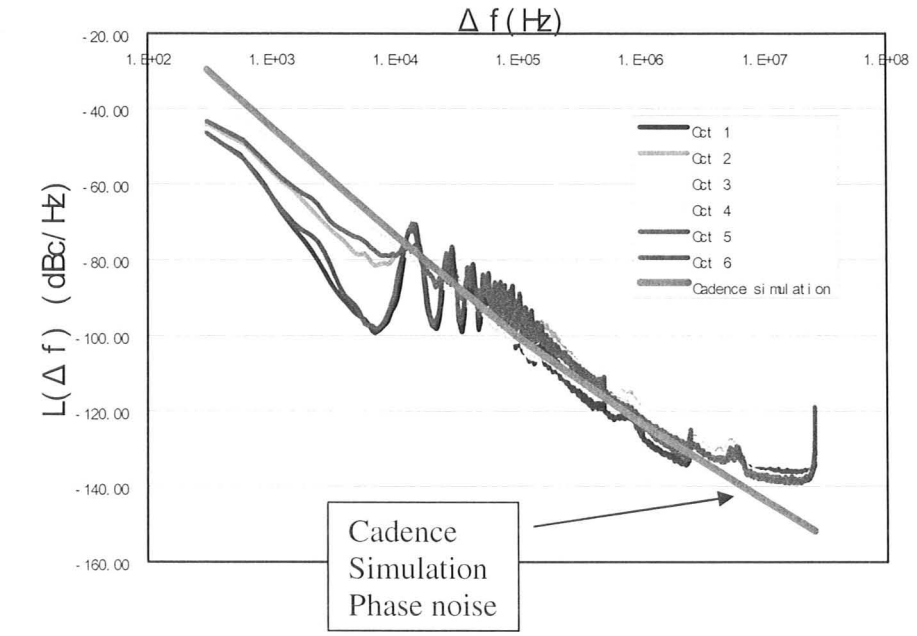


Fig 5.8: Comparison between simulated and measured phase noise

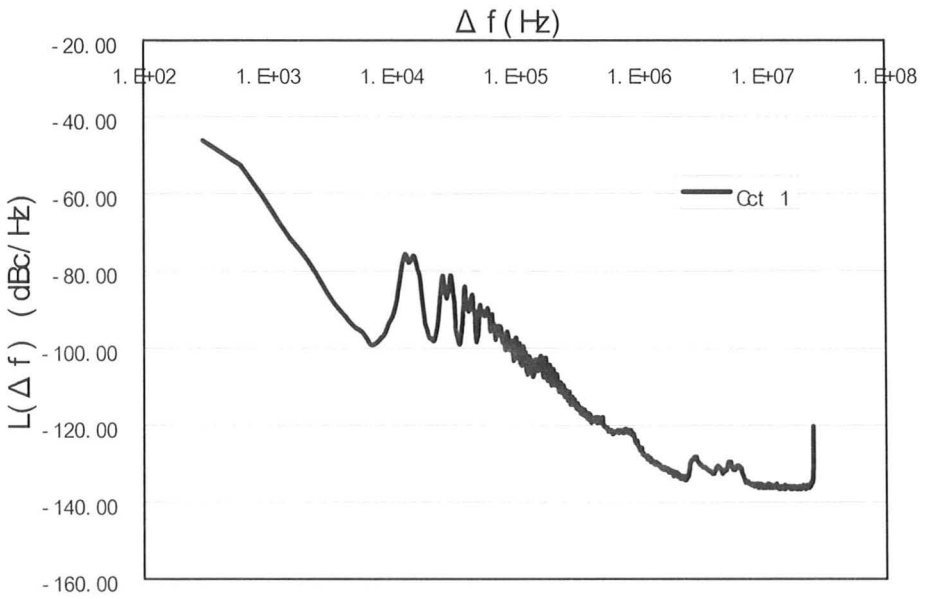


Fig 5.9: Measured phase noise of cct 1

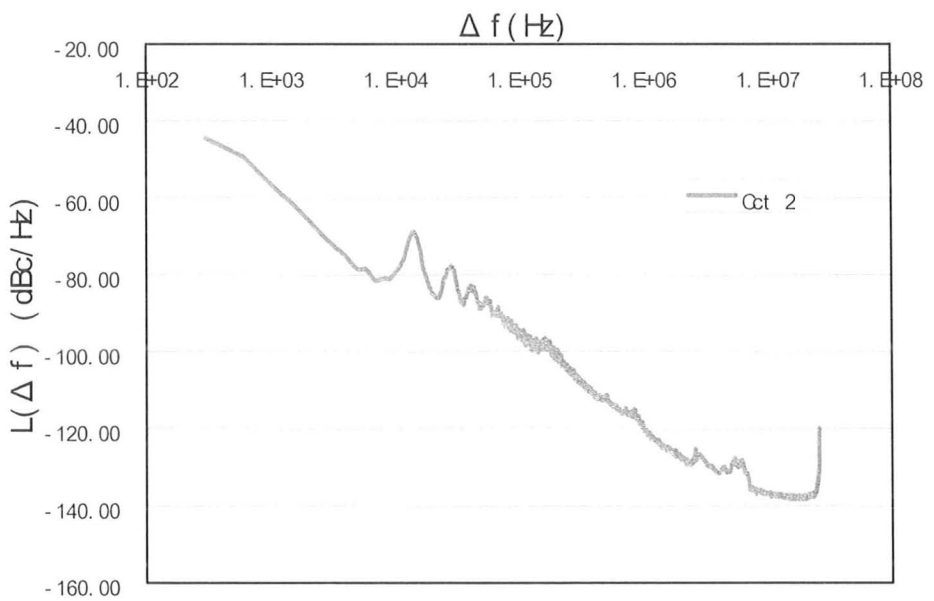


Fig 5.10: Measured phase noise of cct 2

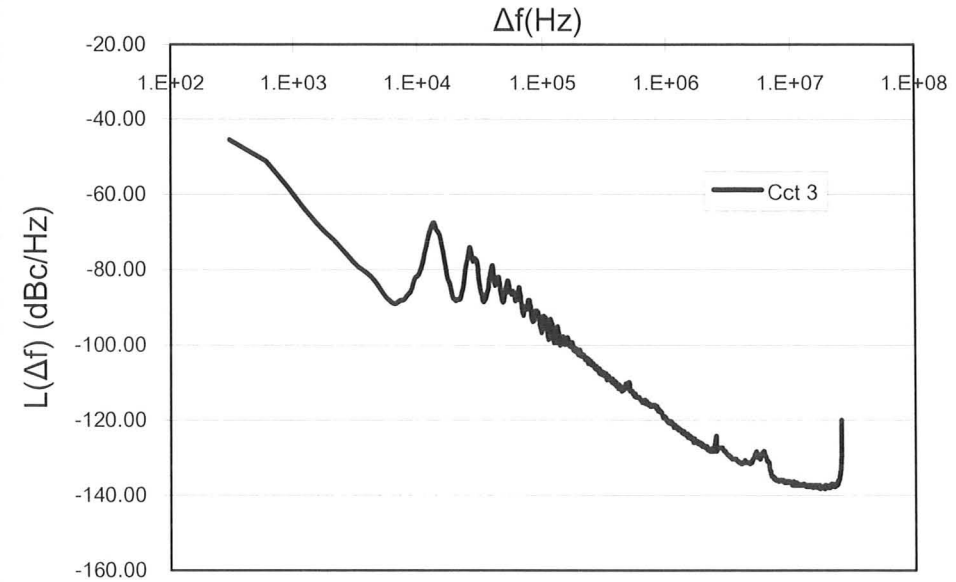


Fig 5.11: Measured phase noise of cct 3

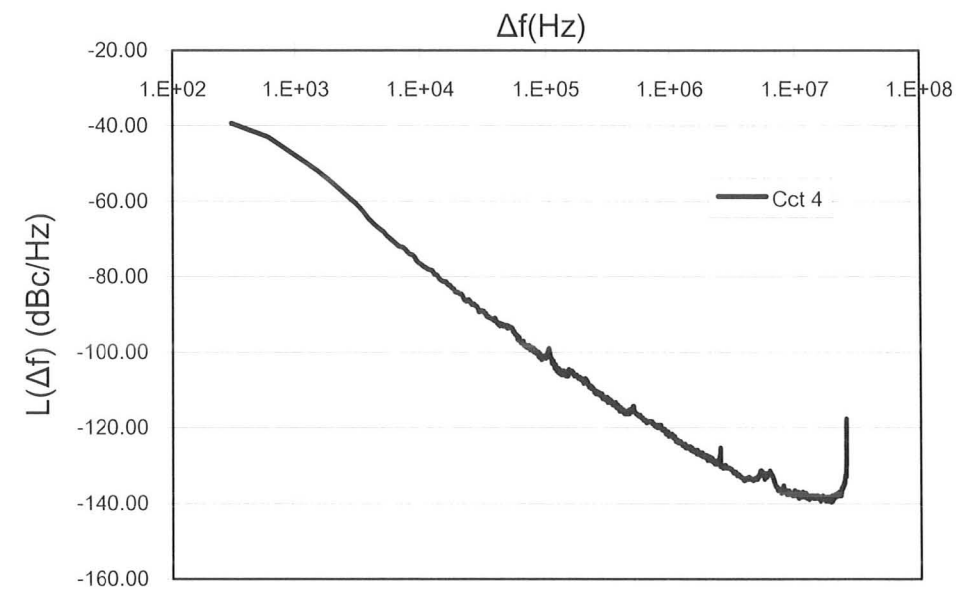


Fig 5.12: Measured phase noise of cct 4

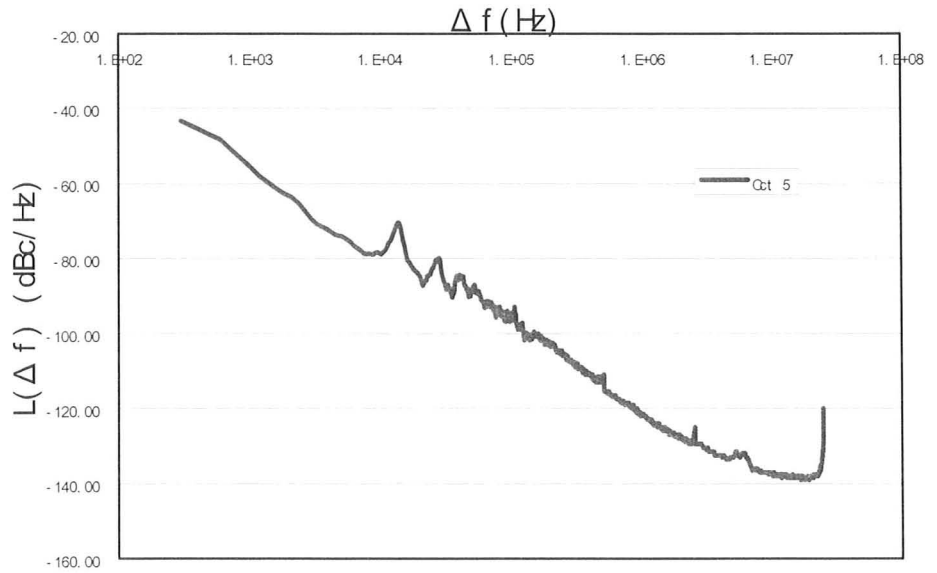


Fig 5.13: Measured phase noise of cct 5

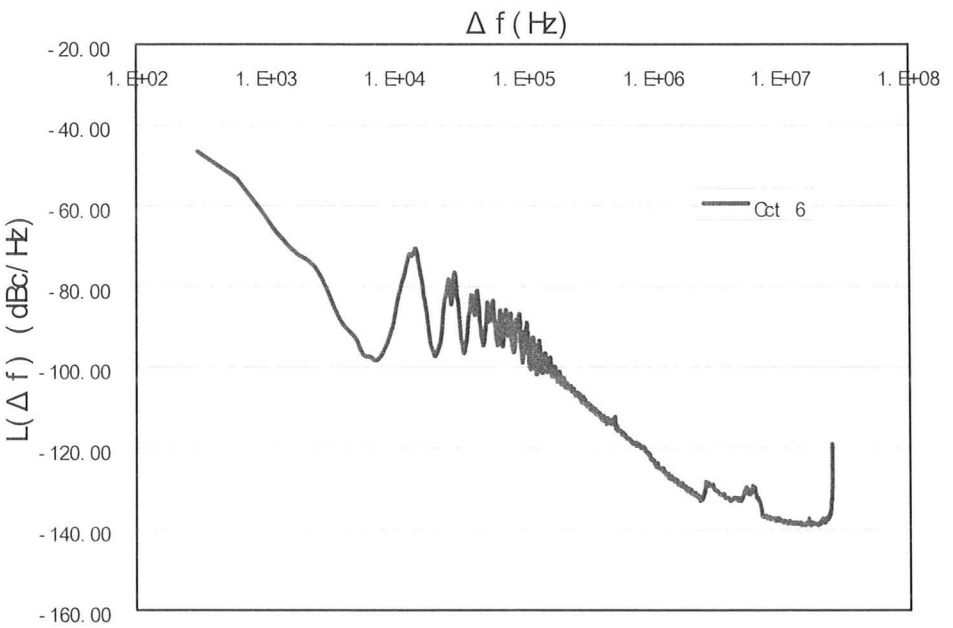


Fig 5.14: Measured phase noise of cct 6

Based on all the measurements that we have conducted, cct 4 has the least phase noise fluctuations with cct 5 also showing some improvement. From the circuit design, we know that cct 4 and 5 have the better Q varactor. From section 4.1.1, it is shown that Q of the varactor could affect overall Q of the circuit. The higher Q of the varactor, the higher is the overall Q. Therefore, we could conclude that Q factor has the largest influence on the phase noise fluctuations.

Between cct 4 and cct 5, the second circuit is not as favorable as compared to the first one. The only difference between these two designs is cct 5 has the DNW structure inductor. In our design, the DNW is formed by implanting a buried n-well under the inductor. From the test results, it is shown that the effect of the DNW will cancel out the effect of the better Q varactor and bring more fluctuations. It is assumed that the introduction of DNW brings in the parasitic effects between DNW and other layers, like parasitic resistors and capacitors. These parasitic effects would worsen the phase noise performance.

Among all other circuits, the cct 6 has the biggest phase noise fluctuations. The following assumption could be made: the capacitor could also influence the ripples. The bigger the capacitor, the better the phase noise ripples. This assumption could be further proved by other three circuits: cct 1, 4 and 5. Because cct 4&5 have the filter capacitor, the fluctuations are all better than that of cct 1. Of all the design changes that we experimented with, it appears that the bias resistance value has the least significance.

5.4 Summary

This chapter presents measurement setup and test results of six fabricated VCO chips and a comparison study of these chips sharing the same topology that uses a differential CMOS cross-coupled negative g_m architecture. The results in comparing DC and phase noise measurement lead to the conclusion that Q factor has the largest influence on phase noise fluctuation reduction.

Chapter 6

CONCLUSIONS AND FUTURE WORK

Phase noise is an important technical design parameter in many modern electronic systems and devices (such including radar, telecommunications devices, electronic navigation tools, electronic measurement equipment, etc.). This work presents the design, fabrication, and measurement of six low power 2.4-GHz LC-tuned VCO fabricated in a CMOS 0.18μm process. Phase noise fluctuation is carefully studied. Although the study of this phenomenon could be found in many papers, methods for improving phase noise performance is seldom touched upon.

To better understand phase noise fluctuations, the design parameters of LC-tuned VCO that improve phase noise performance are examined. Thus, possible parameters for improving the phase noise ripples between 10 kHz and 100 kHz are identified.

The improvement of the inductor's Q factor can significantly eliminate phase noise ripples while decrease in the blocking capacitance in the tank could enlarge the ripples.

In cct 5, we tried to determine whether a DNW could improve the quality factor of the inductor in order to improve the fluctuations, but the result is inconclusive. To further investigate the phase noise fluctuations of DNW, more circuits need to be designed, fabricated and measured. The effects of resistance also need to be further examined in future work with more design samples fabricated for measurement. In addition, more analysis needs to be made on the LC-tuned VCO to investigate phase noise ripples.

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