

Narrow-Band Receiver and Ultra-Wideband Low Noise Amplifier

NARROW-BAND RECEIVER AND ULTRA-WIDEBAND LOW
NOISE AMPLIFIER

BY
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Abstract

In past years, the evolution in communication technology has led to a need for highly-integrated, low-power, and low-cost circuit designs for wireless applications. The demand for radio frequency (RF) wireless transceiver operating at 2.4-GHz band has attracted considerable research interest. The performance of such transceivers depends heavily on that of each of the individual blocks such as low-noise amplifiers and mixers. However, there are very few designs that focus on connecting the single-ended output low-noise amplifier (LNA) to a double-balanced mixer without the use of on-chip transformer. This kind of receiver front-end is designed to achieve high integration and low power consumption.

In recent years, Ultra-Wideband (UWB) technology has developed very rapidly due to its high data transmitting rate and low power consumption. Meanwhile, the design of an Ultra-Wideband low-noise amplifier (LNA) has become an important challenge since it is normally the front-end of the radio frequency (RF) receiver system. Low power consumption of an UWB LNA is a critical requirement for UWB application such as portable devices or especially in biomedical systems. However, the design should not only focus on low power, but also focus on optimizing other performances at competitive levels over the entire bandwidth, where the Federal Communication Commission (FCC) has allocated 7.5 GHz of bandwidth from 3.1

GHz to 10.6 GHz for Ultra-Wideband.

This thesis focuses on the design of a fully-integrated RF receiver front-end including a narrow-band LNA followed by a double balanced mixer. The receiver operates at 2.4 GHz and produces an output signal at 300 MHz. The circuit is designed and fabricated using TSMC 0.18- μm CMOS technology. In order to translate the single-ended RF output signal from the LNA into the differential input pair of the mixer, a main novel idea of this design is to use one PMOS and one NMOS instead of two NMOS devices for the RF amplification stage of the double balanced mixer. The circuit achieves 16.3dB gain and 6.74mW power consumption while using 2.08 mm² chip area.

Another design presented in this thesis is a UWB LNA with special emphasize on low power consumption as well as on optimizing the overall performance. The circuit is designed using TSMC 0.13- μm CMOS technology. It achieves a very flat gain of 10.3-12.1 dB and 3.4-5.9 dB noise figure (NF) throughout the entire bandwidth of 3.1-10.6 GHz. The power consumption is 2.81 mW which is extremely low compared to other designs and the chip area is 0.48 mm². The overall performance is also competitive according to its figure of merit (FoM).

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List of Symbols and Acronyms

Symbols

C_{ox}	Oxide capacitance per unit gate area
ε_{ox}	Permittivity of the silicon oxide
t_{ox}	Oxide thickness
ε_0	Permittivity of free space
g_m	MOSFET transconductance
G_c	Conversion gain
G	Power gain
k'_n	Process transconductance parameter
μ_n	Mobility of electrons in the n channel
μ_p	Mobility of holes in the induced p channel
k	Boltzmann constant
T	Temperature in Kelvin
IIP ₃	Input Third-Order Intercept Point
IM ₃	Third-Order Intermodulation
IP ₃	Third-Order Intercept Point

OIP_3	Output Third-Order Intercept Point
P_{1dB}	1dB compression point
Γ_S	reflection coefficient seen looking toward the source
Γ_L	reflection coefficient seen looking toward the load
Γ_{in}	Input reflection coefficient
Γ_{out}	Output reflection coefficient
V_{DD}	DC voltage supply
S_{11}	Input return loss
S_{12}	The reverse transmission (or leakage) factor
S_{21}	Power gain
S_{22}	Output return loss
Z_S	Source impedance
Z_L	Load impedance
Z_{in}	Input impedance
Z_{out}	Output impedance
Z_0	Characteristic impedance

Acronyms

AC	Alternating Current
CMOS	Complementary Metal-Oxide Semiconductor
dB	Decibel

DC	Direct Current
DSB	Double-Sideband
DUT	Device Under Test
FCC	Federal Communication Commission
FoM	Figure of Merit
GPS	Global Positioning System
IF	Intermediate Frequency
KCL	Kirchhoff's Current Law
LNA	Low Noise Amplifier
LO	Local Oscillator
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NF	Noise Figure
NMOS	n -channel MOSFET
PMOS	p -channel MOSFET
PSD	Power Spectral Density
RMS	Root Mean Square
RF	Radio Frequency
SNR	Signal-to-Noise Ratio
SoC	System-on-a-Chip
SSB	Single-Sideband
TSMC	Taiwan Semiconductor Manufacturing Company
UWB	Ultra-Wideband
VLSI	Very Large-Scale Integration
WLANs	Wireless Local Area Networks

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Chapter 1

Introduction

1.1 Narrow-Band Receiver

1.1.1 Introduction to Narrow-Band Receiver Systems

The design of radio frequency receiver integrated circuits requires a combination of expertise in the areas of circuit design, system architecture, and IC process technology [1]. One of the most important receiver types is the 2.4-GHz narrow-band receiver since many wireless networking architectures are based on it. Therefore, the demand for wireless transceivers operating in the 2.4-GHz band has led to extensive research on the relevant system architectures as well as integrated circuit designs that implement specific transceiver functions [2–4]. The performance of such transceivers depends heavily on that of each of the individual blocks. Also, the quality and range of the communication link is determined by the electrical performance of the transmitter and receiver [1]. These qualities, as well as the cost, and the system's marketability depend on the semiconductor technology and

design techniques used.

For the receiver front-end, both the Low-Noise Amplifier (LNA) and the mixer are key circuit blocks in its operation and performance. However, very few works focus on connecting the single-ended output LNA to the double balanced mixer without the use of on-chip transformer. Realizing such a connection is one of the fulfillment for compact implementation of RF applications. In this thesis, the design of a fully-integrated LNA and a double-balanced mixer on a single chip are described in detail.

1.1.2 Applications of Narrow-Band Receiver Systems

The traffic growth of audio- and video-based messages has led to the need for increasingly higher data rates for next-generation wireless communication applications [1]. Cellular telephony and wireless local area networks (WLANs) are the two primary directions and in recent years, fully integrated system-on-a-chip (SoC) realization become a major interest in receiver front-end designs while maintaining low cost [1]. This is the reason that Complementary Metal-Oxide Semiconductor (CMOS) technology is very popular in RF circuit designs.

The 2.4-GHz narrow-band receiver can also be used in a wide variety of applications, including industrial control and monitoring, public safety, vehicular sensor, etc [5]. In addition, one of the largest application areas is for home automation and networking including wireless mice, keyboards, and radio or television remote controls [5], as shown in Figure 1.1. The characteristics of such a home network are shown in Figure 1.2. Note that the typical transceiver range is on the order of 10-20 m, and the individual channel bandwidths are around 800-900 MHz.

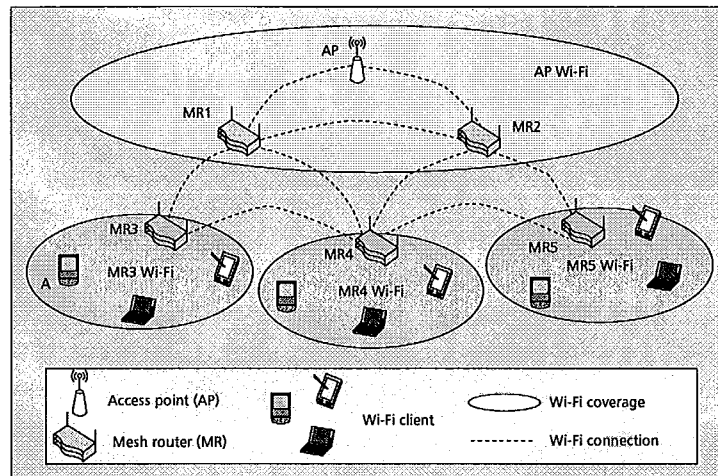


Figure 1.1: Home network system architecture [6].

Property	Range
Raw data rate	868 MHz: 20 kb/s; 915 MHz: 40 kb/s; 2.4 GHz: 250 kb/s
Range	10–20 m
Latency	Down to 15 ms
Channels	868/915 MHz: 11 channels 2.4 GHz: 16 channels
Frequency band	Two PHYs: 868 MHz/915 MHz and 2.4 GHz
Addressing	Short 8-bit or 64-bit IEEE
Channel access	CSMA-CA and slotted CSMA-CA
Temperature	Industrial temperature range –40 to +85 C

Figure 1.2: Home network characteristics [5].

Another application of the 2.4-GHz receiver is for use with Bluetooth technology such as cell phones, cordless headsets, cameras etc [7], as shown in Figure 1.3 [8]. This technology becomes attractive as low cost and low power, and this

points to CMOS technology as an important contender [4]. Nowadays, many researchers focus on low-power, highly-integrated, and low cost narrow-band receiver. In this thesis, we focus on low-power 2.4-GHz narrow-band receiver design while keep other performance parameters at competitive levels.

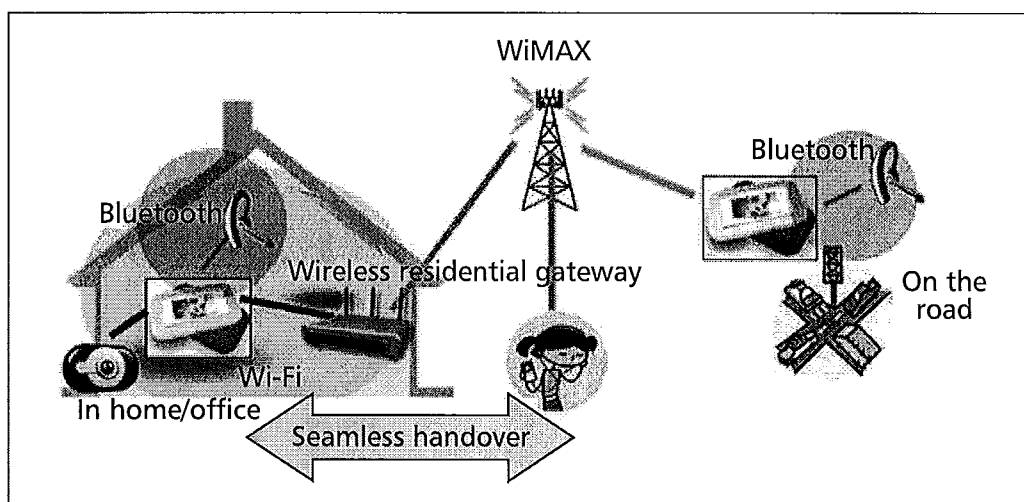


Figure 1.3: Bluetooth applications [8].

1.2 Ultra-Wideband Communications

1.2.1 Introduction to Ultra-Wideband Systems

In recent years, the rapid inroads that technology has made into our daily lives was made possible by the continuing evolution of wireless communication systems. Among the new challenges for the ongoing development of these systems, are the combined problems of high data transmitting rate, low interference, low complexity, low cost and low power consumption. One approach is to make use

of ultra-wideband (UWB) technologies, which have seen much improvement in recent years.

Ultra-Wideband Communications was first employed by Guglielmo Marconi in 1901 to transmit Morse code sequences across Atlantic Ocean using spark gap radio transmitters [9]. Approximately fifty years after Marconi, UWB technology was applied to impulse radars in military applications and this technology was restricted to military from 1960s to 1990s. However, ultra-wideband is now ready for commercial applications because of recent advancements in microprocessors stemming from the rapid development of semiconductor technology. Therefore, it is more appropriate to consider UWB as a new name for a long-existing technology [9].

The FCC has allocated 7.5 GHz bandwidth from 3.1-10.6 GHz frequency range for ultra-wideband technology [10]. The advantages of the UWB system are the following:

- High data transmission rate,
- simple transceiver architecture and low costs,
- large channel capacity and high performance in multipath channels, and
- low signal-to-noise ratio and low power.

UWB technology can be used in radar application, biomedical imaging systems, or positioning system, etc.

1.2.2 Applications of Ultra-Wideband Systems

As shown in Figure 1.4, ultra-wideband technology can be used in high data rate wireless personal area networks, intelligent wireless area networks, as well as sensor, positioning, and identification networks [11]. For example, intelligent wireless area networks are characterized by a high density of devices in a domestic or office environment with the main requirements for such devices being that they are of low cost and have a low power consumption.

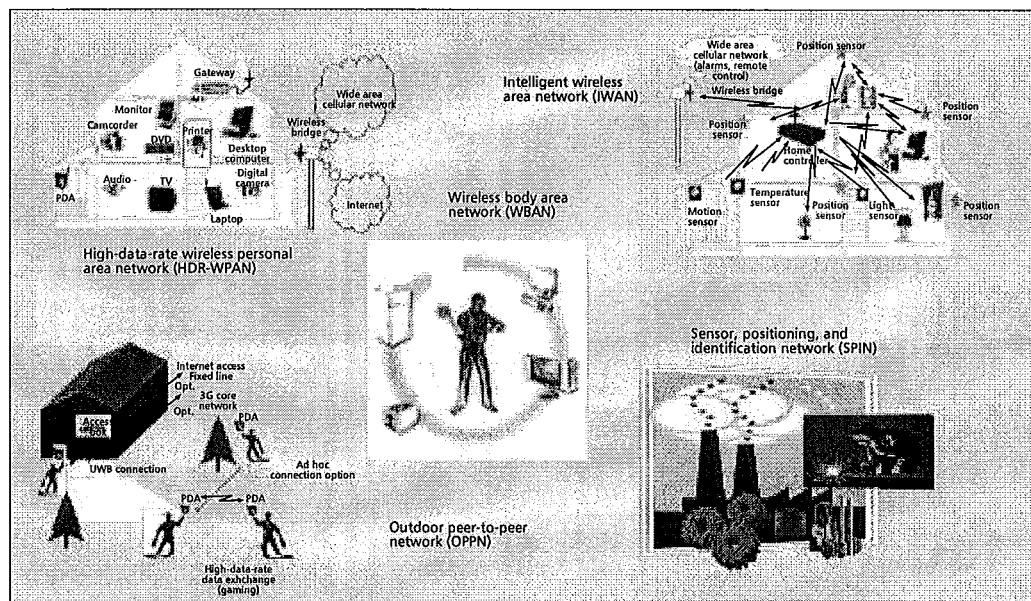


Figure 1.4: Envisaged scenarios for future UWB radio application [11].

In addition to the above networking applications, UWB technology has also been developed for biomedical applications. Ultra-wideband imaging systems have shown promising results for use in early breast cancer detection. Such systems have been found to have a good detection rate and a low false alarm rate [12]. In this system, wideband pulse is transmitted from an antenna toward the target

area. As the signal propagates through various tissues, reflections occur, and the backscattered signal can be used to map different layers of the body [12]. Figure 1.5 shows the general idea of this UWB application. A very significant advantage of this technique is that it is not harmful to the human body and can be easily repeated. UWB technology can also be used in some portable devices with low power consumption.

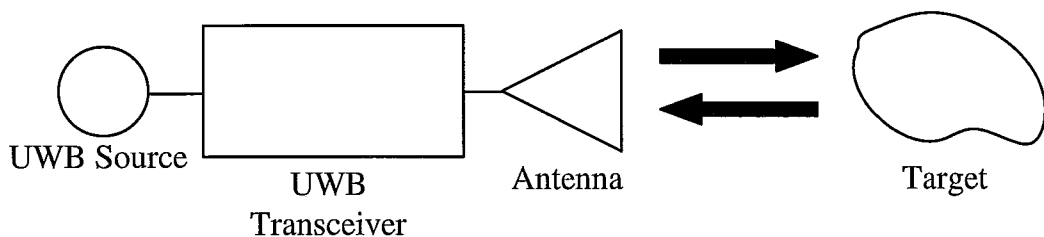


Figure 1.5: General configuration of a UWB imaging system.

1.3 CMOS Technology

Radio-frequency integrated circuits using Complementary Metal-Oxide Semiconductor (CMOS) technology are developing a strong presence in the commercial world such as wireless LAN and Bluetooth [13]. The main advantages of using CMOS for designing RF circuits is that it is high speed, low cost, and allows for a high level of compact integration on a single chip. This is the reason that CMOS is commonly used in very large-scale integration (VLSI) technology in which millions of transistors can be integrated on a single die or chip [14].

Of particular importance to RF designers is the high speed capability of CMOS. This allows CMOS technology to operate effectively in the GHz frequency range

[15] with great levels of integration on a single chip while keeping high performance and low cost [16]. The current need to exploit such regions of the radio spectrum, as well as the high signalling rates required by modern digital telecommunications, therefore make CMOS a very attractive technology choice.

1.4 Motivation

1.4.1 Narrow-Band Receiver

One important part of the narrow-band receiver front-end is the connection between the low noise amplifier (LNA) to the double balanced mixer. While there are severally different ways to realize such a receiver front-end as described in the current literature, these methods have their own drawbacks when fully-integrated on a single chip.

For example, one way to realize this front-end is to use a transformer that can convert the single RF output of the LNA to the differential input of mixer while another way to do this is to use a narrow-band two stage tuned differential LNA that can provide a differential output. However, the first approach is not very easy to implement as integrating an efficient transformer on chip is both difficult and area intensive, which degrades the performance and increases the cost of the chip. The second approach obviously requires a differential RF input. In addition, a two-stage tuned differential LNA has a high power consumption.

To overcome these two issues, we suggest a novel idea that can transform a single output signal from a single-ended LNA into a differential input signal for

a double balanced mixer. This scheme also allows all components to be fully-integrated on a single chip. In this work, we use an NMOS-PMOS pair of devices as the RF input amplification stage of a standard double balanced mixer, rather than using a conventional NMOS-NMOS configuration which will be discussed later in this thesis. This achieves the single-ended LNA to double balanced mixer connection without the need for an on-chip transformer while also keeping all the performance characteristics at competitive levels.

1.4.2 Ultra-Wideband LNA

Portable devices are required to operate for extended periods of time without need to charge or change the battery, a fact which highlights the importance of low-power circuits [2]. This leads to a major challenge for UWB LNA design. Obviously, low power consumption requires a low supply voltage. However, reduction of the supply voltage reduces the circuit's performance parameters such as the linearity or gain.

The target of this thesis is to improve the power consumption as well as optimize the overall performance of an ultra-wideband low noise amplifier. In order to obtain low power dissipation, a 1.2V supply voltage has been selected together with a reasonable bias voltage to provide a certain DC current. As a result, the power consumption can be optimized. The UWB LNA design in this thesis is built as inductive source degeneration cascode structure. Furthermore, the design also focus on optimizing the overall performance which can be measured using the figure of merit (FoM).

1.5 Thesis Organization

This thesis is divided into seven chapters beginning with Chapter 1 (this chapter).

In Chapter 2, a discussion of the fundamental theories of the receiver front-end is provided including some background information on MOSFET and CMOS technology, as well as a description of the desired performance characteristics for the narrow-band receiver. Furthermore, a review of the literature on narrow-band receivers and the relevant design targets is also provided.

In Chapter 3, the details of the narrow-band receivers containing narrow-band low-noise amplifier designs and downconversion double balanced mixer designs are discussed. The fundamental design theories, performance characteristics, and design topologies are reviewed and discussed for both LNAs and mixers.

In Chapter 4, the details of ultra-wideband low-noise amplifiers including fundamentals theories, performance characteristics, and different design topologies are explained. A brief literature review and discussion of the design targets for UWB LNA systems are also presented in this chapter.

Chapter 5 discusses the narrow-band receiver front-end design. The design theories and circuit implementation process are described. In addition, the simulation and implementation results are also discussed and compared with other results found in the published literature.

Chapter 6 describes the ultra-wideband low-noise amplifier design including the design theories, circuit implementation, simulation results, discussions, as well as comparisons to other existing published works.

Finally, Chapter 7 presents a summary of the entire thesis. Possible future work for improving the designs presented in this thesis is also discussed in this chapter.

Chapter 2

Narrow-Band Receivers

2.1 Narrow-Band Receiver Fundamentals

The purpose of the receiver system front-end is to receive a relatively weak signal from an antenna assembly and to perform the initial stages of amplification and frequency conversion while maintaining a good signal-to-noise ratio (SNR). The receiver front-end architecture is shown in Figure 2.1 where the input is an RF signal from the antenna and the output is an intermediate frequency (IF) signal [17].

The incoming RF signal is first amplified by a low-noise amplifier (LNA) and then is fed into the mixer stage to produce the IF output. The IF amplifier is designed to amplify the IF output if needed.

The receiver design in this thesis is focused on the narrow-band LNA and the downconversion double balanced mixer with particular emphasis on the double balanced Gilbert Mixer design. Normally, an upconversion mixer is used in transmitter design [18–21] while the downconversion mixer is used in receiver circuit.

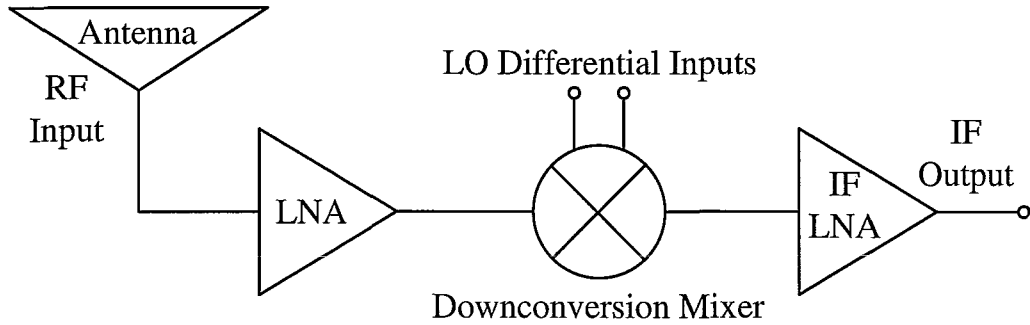


Figure 2.1: Block diagram of the receiver front-end [17].

2.2 Background of CMOS Technology

Complementary Metal-Oxide Semiconductor (CMOS) devices were first introduced in the mid-1960s, initiating a revolution in the semiconductor industry [22]. The low cost of fabrication and the possibility of greater improvements to the speed of MOSFETs have made it the technology of choice for the integrated circuit designs. A CMOS chip is fabricated with both the NMOS and PMOS transistors instead of NMOS transistors alone. Figure 2.2 shows a cross-sectional view of a CMOS device, where the NMOS transistor is implemented directly in the p -type substrate, and the PMOS transistor is fabricated in a special n region, known as an n well [23]. The two devices are isolated from each other by a thick region of oxide that functions as an insulator [23]. Indeed, CMOS is most widely used of all integrated circuits and our circuits are based on $0.18\text{-}\mu\text{m}$ and $0.13\text{-}\mu\text{m}$ CMOS technologies.

2.2.1 MOSFET Fundamentals

The metal-oxide-semiconductor field-effect transistor (MOSFET) is a major type of semiconductor device. The physical structure for the n -channel type (NMOS) is

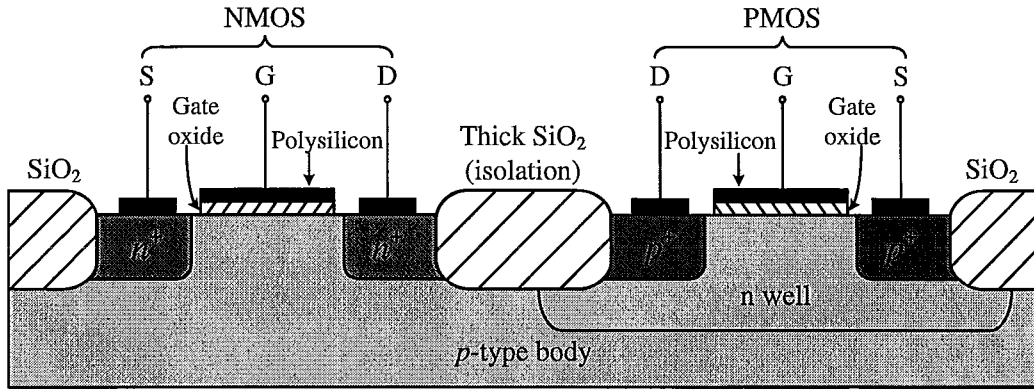


Figure 2.2: Cross-section of a CMOS integrated circuit [23].

shown in Figure 2.3 [23]. The device has a total of four terminals: the gate (G), source (S), drain (D), and substrate or body (B).

The value of V_{GS} at which a sufficient number of mobile electrons are induced in the channel region to form a conducting channel is called the threshold voltage and is denoted as V_t [23]. Normally, the threshold voltage is used to determine whether the transistor is on or off. For the *n*-channel MOSFET (NMOS), whose simplified circuit symbol is shown in Figure 2.4(a), there are three distinct regions of operation:

- when $V_{GS} < V_t$, the NMOS transistor is in the cutoff region since no current flows,
- when $V_{GS} \geq V_t$ and $V_{DS} < V_{GS} - V_t$, the NMOS transistor is in the triode

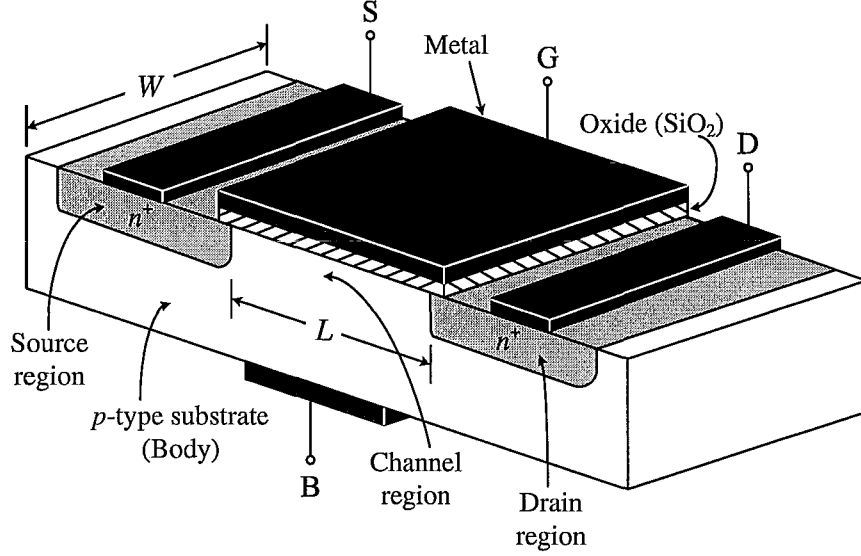


Figure 2.3: 3-D physical structure of the NMOS transistor [23].

region. In this case, the current flowing from drain to source ($I_D - V_{DS}$ characteristic) is calculated as [23]:

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right], \quad (2.1)$$

where μ_n is the mobility of electrons in the n channel, and $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$ is the oxide capacitance per unit gate area. The constant, ϵ_{ox} is the permittivity of the silicon oxide, where $\epsilon_{ox} = 3.9\epsilon_0$ and ϵ_0 is the permittivity of free space. The current I_D enters the drain terminal and leaves through the source terminal.

- When $V_{GS} \geq V_t$ and $V_{DS} \geq V_{GS} - V_t$, the NMOS transistor is in the saturation region. Current flowing in this operating region is calculated according to

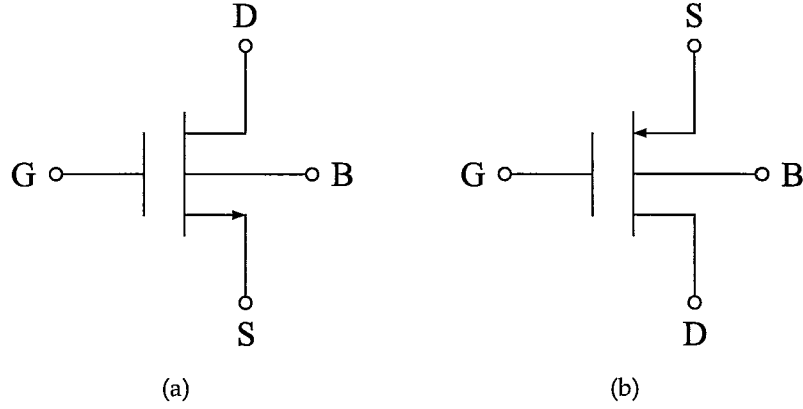


Figure 2.4: (a) Simplified circuit symbol for the n -channel MOSFET (NMOS), and (b) simplified circuit symbol for the p -channel MOSFET (PMOS) [23].

[23]:

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2. \quad (2.2)$$

In most analog circuit designs, the MOSFET needs to be biased, which means that the gate-to-source voltage V_{GS} must be fixed in order to provide the desired DC current I_D . In addition, the MOSFET is normally working in the saturation region which leads to the DC current I_D , which is calculated using equation (2.2).

When MOSFET is biased, it will provide a transconductance gain g_m , which is given by [23]:

$$g_m \equiv \frac{i_d}{v_{gs}} = k'_n \frac{W}{L} (V_{GS} - V_t), \quad (2.3)$$

where k'_n is the process transconductance parameter and is $k'_n = \mu_n C_{ox}$ [23]. Note that g_m is equal to the slope of the $i_D - v_{GS}$ characteristic at the bias point [23]:

$$g_m \equiv \frac{\partial i_D}{\partial v_{GS}}. \quad (2.4)$$

This is the formal definition of g_m , which can be shown to yield the expression given in equation (2.3) [23].

The small-signal equivalent circuit, shown in Figure 2.5, is a very important tool for analyzing MOSFET circuit. For example, applying this equivalent model

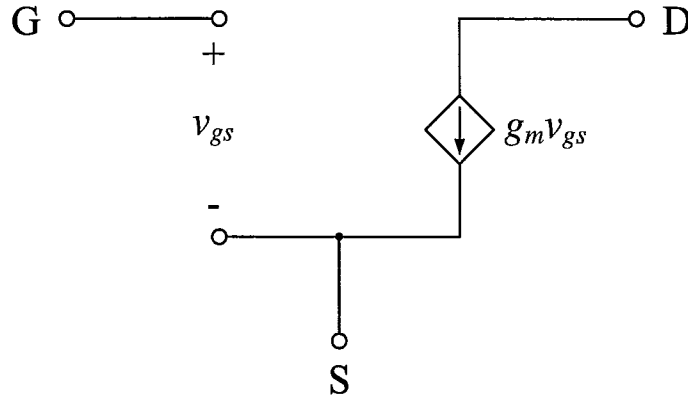


Figure 2.5: Small-signal equivalent circuit for the MOSFET [23].

to a basic circuit, Figure 2.6(a) can be modeled by its small-signal equivalent circuit as shown in Figure 2.6(b). Then the circuit performance such as gain, input impedance, or output impedance can be obtained easily.

To analyze the voltage gain from Figure 2.6(b), it is obvious that

$$v_o = -g_m v_{gs} R_L. \quad (2.5)$$

Furthermore, we know $v_{gs} = v_{in}$, this indicates that the voltage gain is

$$A_v \equiv \frac{v_o}{v_{in}} = \frac{v_o}{v_{gs}} = -g_m R_L. \quad (2.6)$$

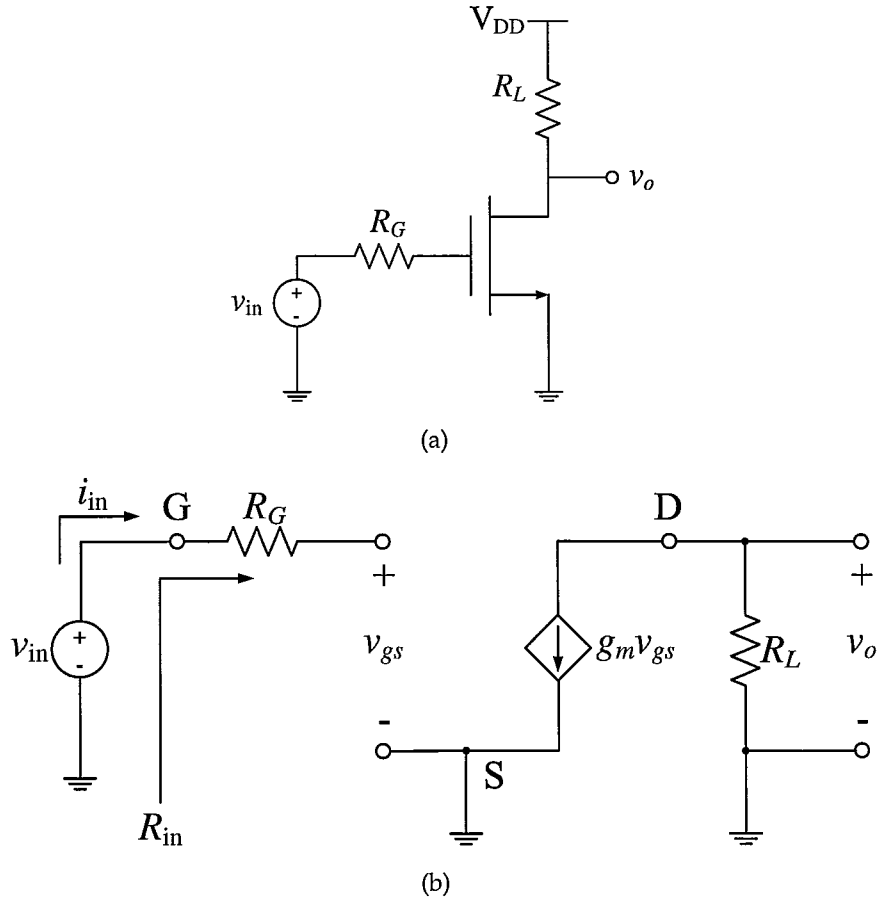


Figure 2.6: (a) Amplifier Circuit, and (b) small-signal equivalent circuit model.

This model can be applied to further complex circuits that includes more resistances, capacitances, or inductances.

2.2.2 MOSFET High-Frequency Model

The small-signal equivalent circuit of the high-frequency response is shown in Figure 2.7 [23]. At high frequencies, the internal capacitances in the MOSFET device

become significant and can not be neglected. In fact, this includes four capacitances C_{gs} , C_{gd} , C_{sb} and C_{db} . However, this becomes quite complex for hand analysis, and we usually neglect C_{sb} and C_{db} which results in a significant simplification of the model. The values of these internal capacitances can be calculated as follows [23]

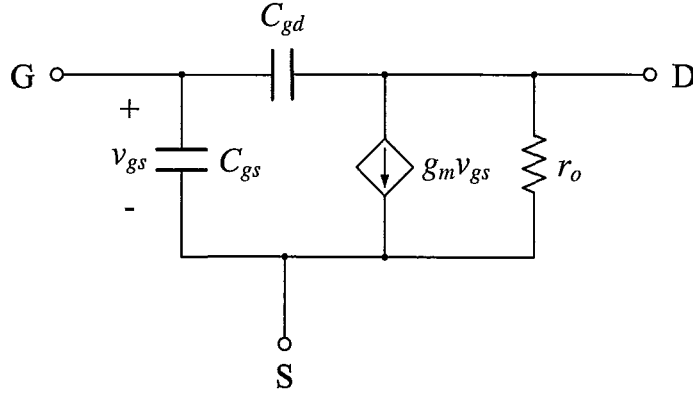


Figure 2.7: MOSFET High-frequency equivalent circuit model [23].

- In the cutoff region:

$$C_{gs} = C_{gd} = 0, \quad (2.7)$$

$$C_{gb} = WLC_{ox}, \quad (2.8)$$

- and in the triode region:

$$C_{gs} = C_{gd} = \frac{1}{2}WLC_{ox}, \quad (2.9)$$

- and in the saturation region:

$$C_{gs} = \frac{2}{3}WLC_{ox}, \quad (2.10)$$

$$C_{gd} = 0. \quad (2.11)$$

2.2.3 PMOS Characteristic

The p -channel MOSFET (PMOS), shown in Figure 2.4(b), operates in the same manner as the NMOS device except that v_{GS} and v_{DS} are negative and the threshold voltage V_t is also negative. In addition, the current i_D enters the source terminal and leaves through the drain terminal. Unlike NMOS, it is required that $v_{GS} \leq V_t$ to turn a PMOS transistor on. Otherwise, the PMOS transistor is off. Therefore, the two distinct regions when PMOS is on can be described accordingly:

- When $v_{GS} \leq V_t$ or equivalently $v_{SG} \geq |V_t|$ and $v_{DS} \geq v_{GS} - V_t$, the PMOS transistor is in triode region. The current i_D is the same as for NMOS from equation (2.1), except for replacing μ_n with μ_p ,

$$i_D = \mu_p C_{ox} \frac{W}{L} \left[(v_{GS} - V_t) v_{DS} - \frac{1}{2} v_{DS}^2 \right], \quad (2.12)$$

where μ_p is the mobility of holes in the induced p channel. Typically, $\mu_p = 0.25$ to $0.5\mu_n$, which depends on the specific process-technology.

- When $v_{GS} \leq V_t$ and $v_{DS} \leq v_{GS} - V_t$, the PMOS transistor is in saturation region. The current i_D can be obtained from equation (2.2) by replacing μ_n with μ_p .

$$i_D = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} (v_{GS} - V_t)^2. \quad (2.13)$$

In CMOS technology, PMOS originally dominated MOSFET manufacturing. However, the NMOS technology has now virtually replaced PMOS due to several

advantages. Usually, the mobility of holes is slower than the mobility of electrons, which means that NMOS devices are faster.

2.3 Receiver Performance Characteristics

2.3.1 Gain

Normally, voltage gain and power gain can be defined as [23]:

$$\text{Voltage gain } (A_v) \equiv \frac{v_O}{v_I}, \quad (2.14)$$

where v_O is the output voltage and v_I is the input voltage, and

$$\begin{aligned} \text{Power gain } (A_p) &\equiv \frac{\text{load power } (P_L)}{\text{input power } (P_I)} \\ &= \frac{v_O i_O}{v_I i_I}, \end{aligned} \quad (2.15)$$

and can be expressed in decibels (dB) as [23]:

$$\begin{aligned} \text{Voltage gain in decibels} &= 20 \log |A_v| \\ &= 20 \log \left| \frac{v_O}{v_I} \right|, \end{aligned} \quad (2.16)$$

$$\begin{aligned} \text{Power gain in decibels} &= 10 \log |A_p| \\ &= 10 \log \left| \frac{v_O i_O}{v_I i_I} \right|. \end{aligned} \quad (2.17)$$

Given $i_I = \frac{v_I}{R_{in}}$ and $i_O = \frac{v_O}{R_L}$, where R_{in} is the input resistance and R_L is the output (load) resistance, the input and output power can be obtained as:

$$P_I = v_I i_I = \frac{v_I^2}{R_{in}}, \quad (2.18)$$

$$P_L = v_O i_O = \frac{v_O^2}{R_L}. \quad (2.19)$$

Substituting equations (2.18) and (2.19) in equation (2.17), the power gain in decibels can be reformulated as

$$\text{Power gain in decibels} = 10 \log \left| \frac{v_O^2/R_L}{v_I^2/R_{in}} \right|. \quad (2.20)$$

If we assume the input impedance R_{in} is equal to the load impedance R_L and are both equal to the source impedance R_S ($R_{in} = R_L = R_S$), which is usually 50Ω , equation (2.20) can be expressed as:

$$\begin{aligned} \text{Power gain in decibels} &= 10 \log \left| \frac{v_O^2}{v_I^2} \right| \\ &= 20 \log \left| \frac{v_O}{v_I} \right|. \end{aligned} \quad (2.21)$$

This result is the same as equation (2.16). Therefore, under this situation, the voltage gain is equal to the power gain when expressed in decibels. This means if a good input and output matching network is achieved (the input and output resistances are matched), the voltage gain should be equal to the power gain in decibels

(dB). However, if the input and output resistances are not matched, the relationship between power gain and voltage gain is:

$$\begin{aligned}
 \text{Power gain in decibels} &= 10 \log \left| \frac{v_O^2/R_L}{v_I^2/R_{in}} \right| = 10 \log \left| \frac{v_O^2 R_{in}}{v_I^2 R_L} \right| \\
 &= 20 \log \left| \frac{v_O}{v_I} \right| + 10 \log \left| \frac{R_{in}}{R_L} \right| \\
 &= \text{Voltage gain in decibels} + 10 \log \left| \frac{R_{in}}{R_L} \right|. \quad (2.22)
 \end{aligned}$$

2.3.2 Noise

Noise in transistors is usually generated by the random motions of charges or charge carriers in devices and materials [24]. In RF front-end circuit designs, the noise is caused by the small current and voltage fluctuations that are generated within the devices themselves, and these various sources of noise are [24,25]:

- *Thermal Noise*, which basically arises due to the random thermally generated motion of electrons. It occurs in resistive devices and is proportional to the temperature.
- *Shot Noise* occurs in all energy barrier junctions, namely, in diodes and bipolar transistors. Actually, it happens whenever a flux of carriers (possessing potential energy) passes over an energy boundary.
- *Flicker Noise* or $1/f$ noise arises from random trapping of charge at the oxide-silicon interface of MOS transistors and in some resistive devices.
- *Additive Amplitude Noise* is described by noise adding to the amplitude of the desired signal.

- *Additive Phase Noise* is the noise adding to the phase of the desired signal.

The most basic type of noise is thermal noise, which is commonly used for noise estimation in RF circuit designs. For instance, the thermal noise of a resistor exists even when there is no current flowing through it. It has a flat power spectral density (PSD) which can be given as follows [25]:

$$\frac{\overline{v^2}}{\Delta f} = 4kTR \quad \text{or} \quad \frac{\overline{i^2}}{\Delta f} = 4kT \frac{1}{R}, \quad (2.23)$$

where $\overline{v^2}$ and $\overline{i^2}$ are the mean square noise voltage and current, respectively, k is the Boltzmann constant, T is the temperature in Kelvin, and Δf is the unit of bandwidth in Hertz. The unit of equation (2.23) is V^2/Hz or A^2/Hz .

A parameter called noise figure (NF) is a commonly used method of specifying the additive noise inherent in a circuit or system [25]. It describes how much the internal noise of an electronic element degrades the signal-to-noise ratio (SNR) [25]. Mathematically, the noise figure is defined as [24]

$$\begin{aligned} \text{NF} &= \frac{\text{SNR}_{\text{in}}}{\text{SNR}_{\text{out}}} = \frac{S_{\text{in}}/N_{\text{in}}}{S_{\text{out}}/N_{\text{out}}} \\ &= \frac{S_{\text{in}}N_{\text{out}}}{S_{\text{out}}N_{\text{in}}}, \end{aligned} \quad (2.24)$$

where S_{in} , N_{in} are the input signal power and the input noise power while S_{out} , N_{out} are the output signal power and the output noise power. In a single stage model with a power gain G , the NF can be expressed as

$$\text{NF} = \frac{N_{\text{out}}}{GN_{\text{in}}}. \quad (2.25)$$

In an RF receiver, the noise is mainly generated from the source resistance and the noisy devices which can be modeled as in Figure 2.8 [25].

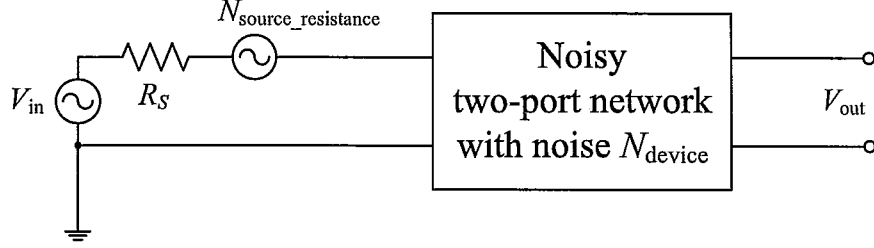


Figure 2.8: Model used in noise figure calculation [25].

The input noise generated from the source resistance can be modeled as [25]

$$N_{in} = N_{source_resistance}. \quad (2.26)$$

Assuming the power gain of this network is G , therefore, the output noise is given by [25]:

$$N_{out} = G \cdot N_{source_resistance} + N_{device}. \quad (2.27)$$

where N_{device} is the noise from the device at the output of the device. The noise figure of this network can be obtained by substituting equations (2.26) and (2.27) into (2.25), which is:

$$\begin{aligned} NF &= \frac{G \cdot N_{source_resistance} + N_{device}}{G \cdot N_{source_resistance}} \\ &= 1 + \frac{N_{device}/G}{N_{source_resistance}}. \end{aligned} \quad (2.28)$$

Denoting $N_{\text{device.input}} = N_{\text{device}}/G$, which means referring the noise to the input of the device. The noise figure can therefore be expressed as:

$$\text{NF} = 1 + \frac{N_{\text{device.input}}}{N_{\text{source.resistance}}}. \quad (2.29)$$

Note that this is input referred noise figure. Usually, the expression above is referred to as the noise factor in linear value, and the relationship between noise figure in decibels (dB) and the noise factor is [25]:

$$\text{NF}_{\text{dB}} = 10 \log_{10} (\text{NF}). \quad (2.30)$$

Considering Figure 2.9 where a cascade of noisy stages is shown, each individual block has an available power gain G_i , noise figure NF_i , device noise N_i , input noise $N_{\text{in},i}$ and output noise $N_{\text{out},i}$, where the letter i denotes the i th stage in the cascade. Assuming that the source impedance for each stage is the same, since this assures the input noise $N_{\text{in},i}$ is the same at each stage. The overall noise figure (NF) derivation consists of the following four steps [25]:

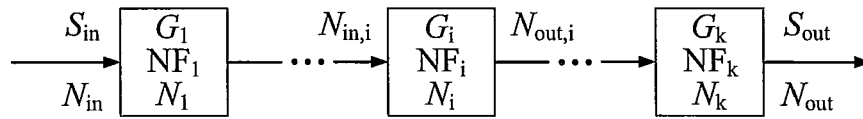


Figure 2.9: Cascade of k gain stages, each with noise [25].

1. The overall output signal power can be obtained from multiplying the input

signal power by the power gain of each stage.

$$S_{\text{out}} = S_{\text{in}}(G_1 G_2 \cdots G_k). \quad (2.31)$$

2. From equation (2.25), the noise figure of i th stage is:

$$\begin{aligned} \text{NF}_i &= \frac{S_{\text{in},i} N_{\text{out},i}}{S_{\text{out},i} N_{\text{in},i}} = \frac{(G_1 \cdots G_{i-1}) S_{\text{in}} N_{\text{out},i}}{(G_1 \cdots G_i) S_{\text{in}} N_{\text{in},i}} \\ &= \frac{N_{\text{out},i}}{G_i N_{\text{in},i}}, \end{aligned} \quad (2.32)$$

and applying equation (2.27), the output noise of i th stage is:

$$N_{\text{out},i} = N_i + G_i N_{\text{in},i}. \quad (2.33)$$

Furthermore, $N_{\text{in},i} = N_{\text{in}}$ since we assumed the input noise $N_{\text{in},i}$ is the same at each stage. Substituting this into equation (2.33), we have:

$$N_{\text{out},i} = N_i + G_i N_{\text{in}}. \quad (2.34)$$

Now substituting equation (2.34) into (2.32), yields:

$$\text{NF}_i = \frac{N_i + G_i N_{\text{in}}}{G_i N_{\text{in}}} = \frac{N_i}{G_i N_{\text{in}}} + 1. \quad (2.35)$$

Relating N_i to NF_i , equation (2.35) can be rearranged as:

$$N_i = (\text{NF}_i - 1) G_i N_{\text{in}}. \quad (2.36)$$

3. Including all k stages, the resulting overall output noise can be obtained by using equation (2.27) iteratively:

$$\begin{aligned} N_{\text{out}} = & (G_1 G_2 \cdots G_k) N_{\text{in}} + N_1 (G_2 \cdots G_k) \\ & + N_2 (G_3 \cdots G_k) + \cdots + N_{k-1} G_k + N_k. \end{aligned} \quad (2.37)$$

Substituting equation (2.36) into (2.37), yields:

$$\begin{aligned} N_{\text{out}} = & (G_1 G_2 \cdots G_k) N_{\text{in}} + (\text{NF}_1 - 1)(G_1 G_2 \cdots G_k) N_{\text{in}} \\ & + \cdots + (\text{NF}_k - 1) G_k N_{\text{in}}. \end{aligned} \quad (2.38)$$

4. Finally, the total noise figure of the cascaded stages in Figure 2.9 can be obtained by substituting equations (2.31) and (2.38) into (2.24). Therefore, the overall NF expression is:

$$\text{NF} = \text{NF}_1 + \frac{\text{NF}_2 - 1}{G_1} + \frac{\text{NF}_3 - 1}{G_1 G_2} + \cdots + \frac{\text{NF}_k - 1}{G_1 G_2 \cdots G_{k-1}}. \quad (2.39)$$

This equation is called the Friis formula. Equation (2.39) clearly indicates that the overall noise figure is dominated by the first stage of the entire system.

2.3.3 Linearity

In an ideal linear receiver system, the IF output signal is proportional to the RF input signal. However, in reality, there are higher-order non-linearities which results in intermodulation distortion. Typically, only nonlinearities of the third order and below are of interest to RF designers. Mathematically, these nonlinearities can be

represented in terms of third-order polynomial of the form [25]:

$$y(t) = \alpha_1 s(t) + \alpha_2 s^2(t) + \alpha_3 s^3(t), \quad (2.40)$$

where coefficients α_n are constants, $s(t)$ is the input signal, and $y(t)$ is the output signal.

In order to analyze this distortion, a so called "two-tone" test is applied since intermodulation arises if more than one tone appears at the input (ω_0). Therefore, we assume that two interference signals appear at the input, specified by [25]:

$$s(t) = A_1 \cos \omega_1 t + A_2 \cos \omega_2 t, \quad (2.41)$$

where ω_1 and ω_2 are the angular frequencies of the two interferers. Substituting equation (2.41) into (2.40), the intermodulation products can be obtained according to [25]:

$$\begin{aligned} y(t) = & \alpha_1 (A_1 \cos \omega_1 t + A_2 \cos \omega_2 t) + \alpha_2 (A_1 \cos \omega_1 t + A_2 \cos \omega_2 t)^2 \\ & + \alpha_3 (A_1 \cos \omega_1 t + A_2 \cos \omega_2 t)^3. \end{aligned} \quad (2.42)$$

For simplicity and clarity, only third-order intermodulation products are reproduced here [25]:

$$\begin{aligned} 2\omega_1 \pm \omega_2 : & \frac{3\alpha_3 A_1^2 A_2}{4} \cos(2\omega_1 + \omega_2)t + \frac{3\alpha_3 A_1^2 A_2}{4} \cos(2\omega_1 - \omega_2)t, \\ 2\omega_2 \pm \omega_1 : & \frac{3\alpha_3 A_2^2 A_1}{4} \cos(2\omega_2 + \omega_1)t + \frac{3\alpha_3 A_2^2 A_1}{4} \cos(2\omega_2 - \omega_1)t. \end{aligned} \quad (2.43)$$

Normally, the removal of the third order intermodulation products at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ requires a filter with very narrow bandwidth. This is impractical since ω_1 and ω_2 are too close to the desired signal at ω_0 . To quantify this distortion, the term IM_3 is defined as the ratio of the amplitude of the third-order intermodulation product to the amplitude of the fundamental output signal given by $y(t) = \alpha_1 A \cos \omega_0 t$. Mathematically, if we assume the amplitudes of the desired and unwanted signals are the same, $A=A_1=A_2$, IM_3 can be defined as [25]:

$$IM_3 = \frac{\frac{3}{4}\alpha_3 A^3}{\alpha_1 A} = \frac{3}{4} \frac{\alpha_3}{\alpha_1} A^2. \quad (2.44)$$

Now, we will define another performance metric, called the third-order intercept point (IP_3), shown in Figure 2.10 [25], where it is the intersection of the ideal first order and third order curves. Moreover, IIP_3 stands for Input referred Third-Order Intercept Point and OIP_3 stands for Output referred Third-Order Intercept Point.

Mathematically, the third-order intercept point, IP_3 is defined by the relation [25]:

$$20 \log(\alpha_1 A_{IP3}) = 20 \log \left(\frac{3}{4} \alpha_3 A_{IP3}^3 \right). \quad (2.45)$$

After solving for A_{IP3} , we have:

$$A_{IP3} = \sqrt{\frac{4}{3} \left| \frac{\alpha_1}{\alpha_3} \right|}. \quad (2.46)$$

If we assume the load is 50Ω , then the input third-order intercept point (IIP_3) is defined as [25]:

$$IIP_3 = A_{IP3}^2 / 50\Omega. \quad (2.47)$$

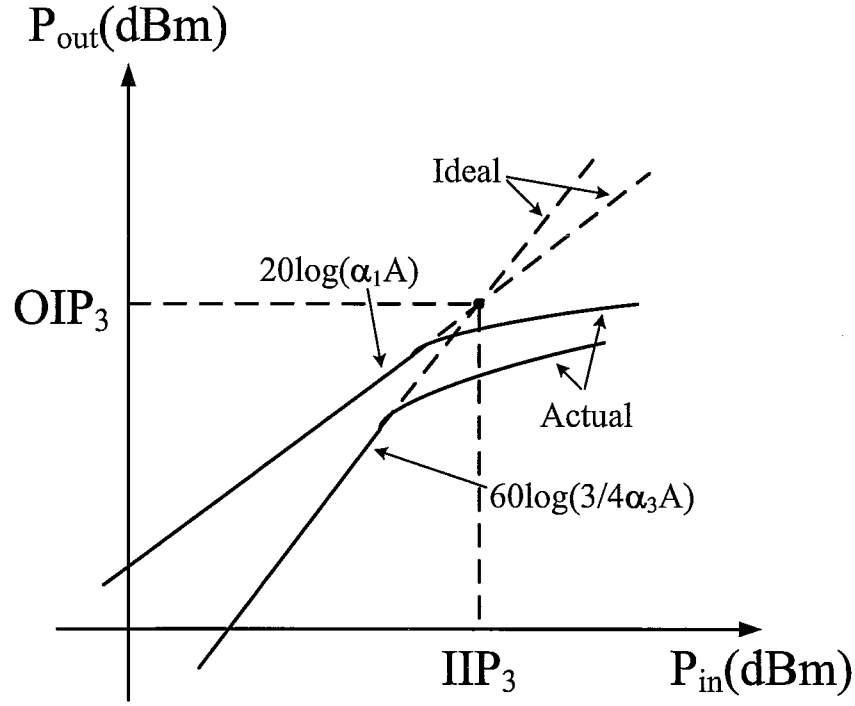


Figure 2.10: Graphical representation of the input and output referred third-order intercept points [25].

In turn, we define the output third-order intercept point (OIP_3) to be the multiplication of the IIP_3 by the gain of the fundamental signal, $OIP_3 = IIP_3 G$.

Another useful approximation of the overall IIP_3 of a cascaded nonlinear stages system, shown in Figure 2.11, can be expressed as [25]

$$\frac{1}{IIP_3} \approx \frac{1}{IIP_{3,1}} + \frac{G_1}{IIP_{3,2}} + \frac{G_1 G_2}{IIP_{3,3}} + \cdots + \frac{G_1 G_2 \cdots G_{n-1}}{IIP_{3,n}}, \quad (2.48)$$

where G_n is the power gain of the n th stage.

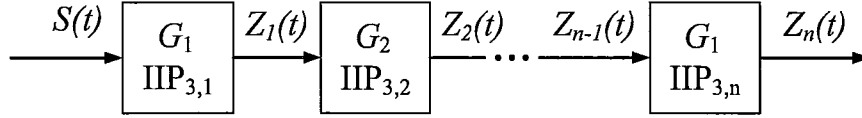


Figure 2.11: Cascade of n nonlinear stages, each with gain G [25].

2.3.4 Gain Compression

The nonlinearity of the receiver can cause gain compression, which is defined as a point at which the output curve drops from the ideal linear curve by 1 dB, and the point is defined as the 1dB compression point (P_{1dB}), shown in Figure 2.12.

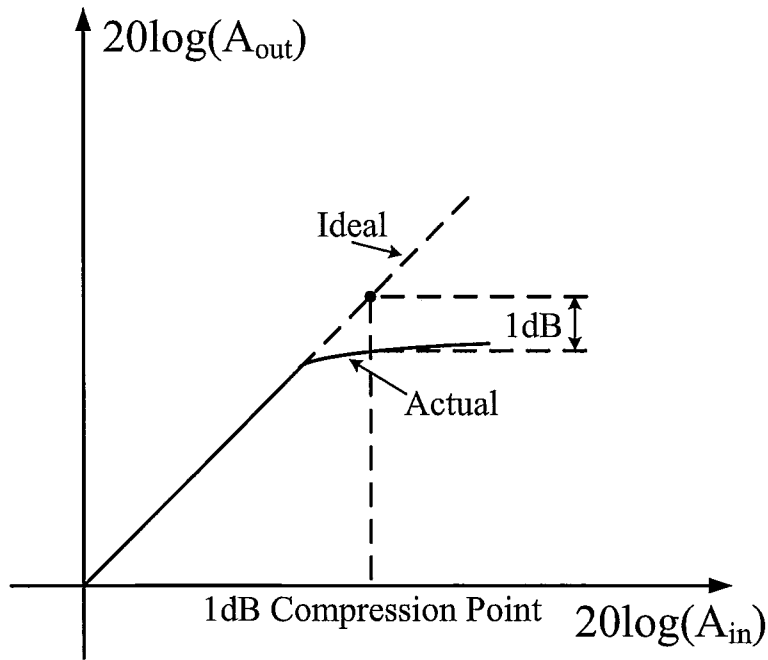


Figure 2.12: Illustration of the 1dB compression point [25].

From equation (2.40), if a single tone input is applied, which is $s(t) = A \cos \omega_0 t$,

the output can be expanded mathematically as:

$$\begin{aligned}
 y(t) &= \alpha_1 A \cos \omega_0 t + \alpha_2 A^2 \cos^2 \omega_0 t + \alpha_3 A^3 \cos^3 \omega_0 t \\
 &= \frac{\alpha_2 A^2}{2} + \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4} \right) \cos \omega_0 t \\
 &\quad + \frac{\alpha_2 A^2}{2} \cos 2\omega_0 t + \frac{\alpha_3 A^3}{4} \cos 3\omega_0 t.
 \end{aligned} \tag{2.49}$$

The frequency band of interest is at ω_0 which leads $y(t)$ to become:

$$y(t) = \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4} \right) \cos \omega_0 t = \left(\alpha_1 + \frac{3\alpha_3 A^2}{4} \right) A \cos \omega_0 t. \tag{2.50}$$

Applying the concept of 1dB compression point, $P_{1\text{dB}}$ is the point when the gain drops by 1 dB and it can be represented as the voltage amplitude $A_{1\text{dB}}$, which is expressed as:

$$\left(\alpha_1 + \frac{3\alpha_3 A_{1\text{dB}}^2}{4} \right) \Big|_{\text{dB}} = \alpha_1|_{\text{dB}} - 1\text{dB}. \tag{2.51}$$

Rearranging equation (2.51) in decibels, we have:

$$20 \log \left| \alpha_1 + \frac{3\alpha_3 A_{1\text{dB}}^2}{4} \right| = 20 \log |\alpha_1| - 20 \log 1.122. \tag{2.52}$$

Therefore, solving equation (2.52), the 1dB compression point appears at the voltage level $A_{1\text{dB}}$ given by:

$$A_{1\text{dB}} = \sqrt{0.145 \left| \frac{\alpha_1}{\alpha_3} \right|}. \tag{2.53}$$

2.4 Narrow-Band Receiver Literature Review

There are many published designs for 2.4 GHz narrow-band receiver front-ends and these focus on different aspects depending on the perceived demands of the application. However, this thesis will focus on the issue of how to connect a narrow-band low-noise amplifier to a double balanced mixer. From the existing literature, there are two principle approaches to solve this problem.

One possible solution is to design a differential low noise amplifier, which is designed to produce a differential output signal pair. Existing literature [26, 27] has presented such an approach by implementing the differential narrow-band LNA on-chip. The advantage of this design is that it can produce a differential output pair which can be used directly by the double balanced mixer. It is relatively simple to fabricate and presents good performance. One disadvantages however, is that it requires a differential RF input signal instead of a single input. This creates difficulties for practical application since normally an RF signal is single input. Another disadvantage is that it requires obviously one more stage in the LNA design since the two symmetric stages can produce two out-of-phase signals (the differential output pair). Therefore, the differential narrow-band LNA doubles the number of stages from the original LNA, which consumes twice the power, degrading the performance of the narrow-band receiver.

Another possible method for implementing a single input narrow-band LNA followed by a double balanced mixer is to design an on-chip transformer [28]. However, this solution also degrades the performance since many components need to be added in order to implement an on-chip transformer designed to translate the single RF signal into a differential signal. This results in greater power

dissipation and increases the physical complexity of the circuit design and fabrication.

Razavi [29] suggests another narrow-band receiver design that implements a single RF input narrow-band LNA connected to a single balanced mixer. The single balanced mixer requires a single RF input eliminating the problems discussed previously. However, as will be discussed in Chapter 3, the single balanced mixer has difficulties to reduce the RF and LO feedthroughs and meanwhile, the gain is only half that of the double balanced mixer. These disadvantages restrict this method. As a result, it is not a very popular design strategy in narrow-band receiver designs.

In summary, the designs discussed above have their own advantages and drawbacks. The problem of how to connect the narrow-band LNA to the double balanced mixer has therefore, not been satisfactorily solved, and remains a topic of active research. It is this problem therefore, that is one of the focuses of this thesis.

Chapter 3

Narrow-Band LNA and Mixer Theories

3.1 Narrow-Band LNA Fundamentals

The narrow-band low-noise amplifier is normally the first stage of the receiver front-end. Its function is to amplify the incoming RF signal while minimizing the amount of noise added to this signal. Therefore, the noise figure is one of the most important characteristics in an LNA design. Other desirable properties include high gain, linearity, low input and output return losses, and finally, low power consumption.

3.2 Performance of Narrow-Band LNA

3.2.1 Power Gain

Usually, the performance of a low-noise amplifier (LNA) can be measured by modelling the device as a two-port network and calculating the S -parameters. Figure 3.1 is an arbitrary two-port network connected to a source impedance Z_S and a load impedance Z_L [24]. As derived in Chapter 2, the voltage gain is equal to the power gain if the input and output impedances are matched. This means that if a good matching network is achieved, then the power gain is almost the same as the voltage gain. Therefore, the expression for the power gain is derived in terms of S parameters.

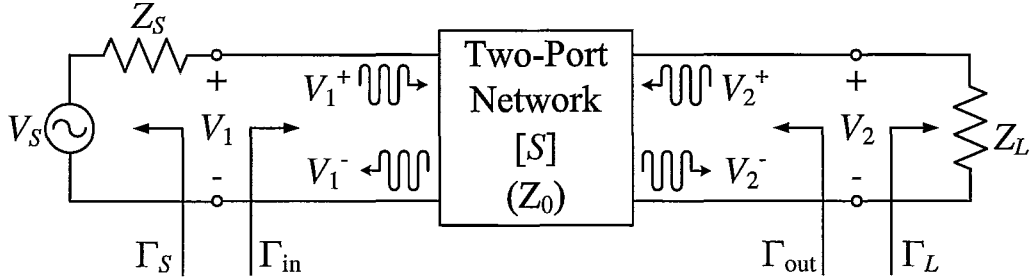


Figure 3.1: A two-port network with general source and load impedances [24].

There are generally three types of power gain [24]:

- *Power Gain*: $G = P_L/P_{in}$ is the ratio of power dissipated in the load Z_L to the power delivered to the input of the two-port network. This gain is independent of Z_S , although some active circuits are strongly dependent on Z_S .
- *Available Power Gain*: $G_A = P_{avn}/P_{avs}$ is the ratio of the power available from

the two-port network to the power available from the source. This assumes conjugate matching of both the source and the load, and depends on Z_S but not Z_L .

- *Transducer Power Gain*: $G_T = P_L/P_{avs}$ is the ratio of the power delivered to the load to the power available from the source. This depends on both Z_S and Z_L .

Assuming Z_S is the source impedance, Z_L is the load impedance, Z_{in} is the input impedance, Z_{out} is the output impedance, and Z_0 is the characteristic impedance (normally 50Ω). In general, we define Γ_S as the reflection coefficient seen looking toward the source, and can be shown to be [24]:

$$\Gamma_S = \frac{Z_S - Z_0}{Z_S + Z_0}, \quad (3.1)$$

while Γ_L is the reflection coefficient seen looking toward the load, which is:

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0}. \quad (3.2)$$

Applying the definition of S parameter in appendix B to Figure 3.1, we have [24]:

$$V_1^- = S_{11}V_1^+ + S_{12}V_2^+ = S_{11}V_1^+ + S_{12}\Gamma_L V_2^-, \quad (3.3)$$

$$V_2^- = S_{21}V_1^+ + S_{22}V_2^+ = S_{21}V_1^+ + S_{22}\Gamma_L V_2^-, \quad (3.4)$$

where V_1^+ is the incident wave seen from the input port, V_1^- is the reflected wave seen from the input port, V_2^+ is the incident wave seen from the output port, and

V_2^- is the reflected wave seen from the output port. Solving for V_1^-/V_1^+ from equations (3.3) and (3.4), the reflection coefficient seen looking toward the network model input is [24]:

$$\begin{aligned}\Gamma_{\text{in}} &= \frac{V_1^-}{V_1^+} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \\ &= \frac{Z_{\text{in}} - Z_0}{Z_{\text{in}} + Z_0},\end{aligned}\quad (3.5)$$

while the reflection coefficient seen looking toward the output is [24]:

$$\Gamma_{\text{out}} = \frac{V_2^-}{V_2^+} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S}.\quad (3.6)$$

By the voltage divider rule, V_1 can be expressed as [24]:

$$V_1 = V_S \frac{Z_{\text{in}}}{Z_S + Z_{\text{in}}} = V_1^+ + V_1^- = V_1^+ (1 + \Gamma_{\text{in}}),\quad (3.7)$$

where Z_{in} is the input impedance of the network. From equation (3.5), the input impedance is:

$$Z_{\text{in}} = Z_0 \frac{1 + \Gamma_{\text{in}}}{1 - \Gamma_{\text{in}}}.\quad (3.8)$$

Solving for V_1^+ in terms of V_S gives [24]:

$$V_1^+ = \frac{V_S}{2} \frac{(1 - \Gamma_S)}{(1 - \Gamma_S \Gamma_{\text{in}})}.\quad (3.9)$$

The average power delivered to the network can be obtained as [24]:

$$\begin{aligned} P_{\text{in}} &= \frac{1}{2Z_0} |V_1^+|^2 (1 - |\Gamma_{\text{in}}|^2) \\ &= \frac{|V_S|^2}{8Z_0} \frac{|1 - \Gamma_S|^2}{|1 - \Gamma_S \Gamma_{\text{in}}|^2} (1 - |\Gamma_{\text{in}}|^2), \end{aligned} \quad (3.10)$$

while the power delivered to the load is:

$$P_L = \frac{|V_2^-|^2}{2Z_0} (1 - |\Gamma_L|^2). \quad (3.11)$$

Then, solving for V_2^- from equation (3.4) and substituting into equation (3.11), gives [24]:

$$\begin{aligned} P_L &= \frac{|V_1^+|^2 |S_{21}|^2 (1 - |\Gamma_L|^2)}{2Z_0 |1 - S_{22}\Gamma_L|^2} \\ &= \frac{|V_S|^2 |S_{21}|^2 (1 - |\Gamma_L|^2) |1 - \Gamma_S|^2}{8Z_0 |1 - S_{22}\Gamma_L|^2 |1 - \Gamma_S \Gamma_{\text{in}}|^2}. \end{aligned} \quad (3.12)$$

The power gain can be obtained as [24]:

$$G = \frac{P_L}{P_{\text{in}}} = \frac{|S_{21}|^2 (1 - |\Gamma_L|^2)}{(1 - |\Gamma_{\text{in}}|^2) |1 - S_{22}\Gamma_L|^2}. \quad (3.13)$$

In our narrow-band LNA design, we use $Z_S = Z_L = Z_0 = 50\Omega$. From equations (3.1) and (3.2), we have $\Gamma_S = 0$ and $\Gamma_L = 0$. Substituting these values into equations (3.5) and (3.6), we have:

$$\Gamma_{\text{in}} = S_{11} = \frac{Z_{\text{in}} - Z_0}{Z_{\text{in}} + Z_0}, \quad (3.14)$$

$$\Gamma_{\text{out}} = S_{22}. \quad (3.15)$$

Since our LNA is well matched ($Z_{\text{in}} \approx Z_{\text{out}} \approx Z_0$), the power gain can be redefined approximately as:

$$G = \frac{P_L}{P_{\text{in}}} = |S_{21}|^2. \quad (3.16)$$

Expressing equation (3.16) in decibels (dB), we have:

$$G_{\text{dB}} = 10 \log(|S_{21}|^2) = 20 \log(|S_{21}|). \quad (3.17)$$

The available power gain is [24]:

$$G_A = \frac{|S_{21}|^2(1 - |\Gamma_S|^2)}{|1 - S_{11}\Gamma_S|^2(1 - |\Gamma_{\text{out}}|^2)}, \quad (3.18)$$

and the transducer power gain is [24]:

$$G_T = \frac{|S_{21}|^2(1 - |\Gamma_S|^2)(1 - |\Gamma_L|^2)}{|1 - \Gamma_S\Gamma_{\text{in}}|^2|1 - S_{22}\Gamma_L|^2}. \quad (3.19)$$

Again in the hypothetical design, the source impedance is equal to the load impedance and are both equal to the characteristic impedance, which is normally 50Ω . Then $\Gamma_S = \Gamma_L = 0$, and the transducer gain from equation (3.19) can be reduced to

$$G_T = |S_{21}|^2. \quad (3.20)$$

If expressed in decibels (dB), we have:

$$G_{T(\text{dB})} = 10 \log(|S_{21}|^2) = 20 \log(|S_{21}|), \quad (3.21)$$

which is the same as equation (3.17). Therefore, S_{21} in dB is commonly used to

measure the power gain of our LNA.

3.2.2 Noise

From Friis formula, equation (2.39), the overall NF is dominated by the first stage of a cascaded network. This means that the NF is dominated by the first transistor, M_1 , in the LNA. Furthermore, we assume that the dominant form of noise in M_1 is thermal noise. It follows then, that a convenient method for approximating the noise figure of a low-noise amplifier is to calculate the overall NF based only on the dominating noise.

Generally, the noise figure (NF) of the amplifier core is defined as [25]:

$$\text{NF} = \frac{N_{\text{device}} + N_{\text{in}}}{N_{\text{in}}} = 1 + \frac{N_{\text{device}}}{N_{\text{in}}}, \quad (3.22)$$

where N_{device} stands for the input-referred noise from the amplifier, which is mainly the thermal noise of the first transistor M_1 . The term N_{in} represents noise at the input side, which is mainly generated from the source resistance R_S . From Chapter 2, the thermal noise of a resistor is [22]:

$$V_n^2 = 4kTR, \quad (3.23)$$

where k is the Boltzmann constant and T is the temperature in Kelvin, Δf is used to emphasize that $4kTR$ is the noise power per unit bandwidth of $\Delta f = 1$ Hz, and V_n^2 is spectral density of the thermal noise of the resistor in the unit V^2/Hz .

The thermal noise current of a MOSFET, as shown in Figure 3.2 [22], can be modeled by a current source connected between the drain and source terminals.

This is known as drain current noise, since the most significant thermal noise is generated in the channel [22].

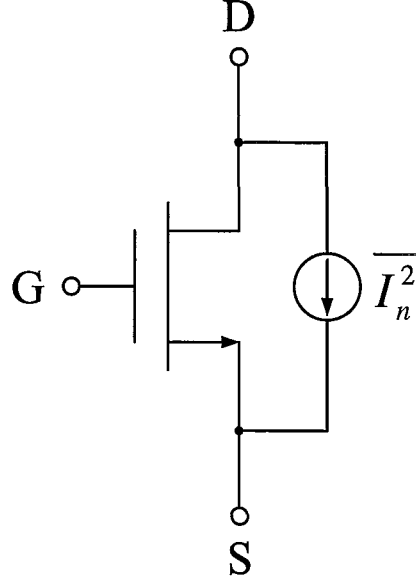


Figure 3.2: Thermal noise of a MOSFET [22].

The resulting drain current noise of a MOSFET is [30]:

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0}\Delta f, \quad (3.24)$$

where g_{d0} is the drain-source conductance at zero V_{DS} . Taking $\Delta f = 1$ Hz, the noise expression will be for the noise "power" per unit bandwidth. Furthermore, for long-channel devices, g_{d0} with V_{DS} is equal to g_m in saturation and hence, the spectral density of the thermal noise in the drain current can be obtained as [22]:

$$\overline{I_n^2} = 4kT\gamma g_m, \quad (3.25)$$

where $\gamma = 2/3$ for long-channel transistors. Note that this noise is given as power spectrum density of noise current in unit A^2/Hz .

3.2.3 Linearity

The linearity of a narrow-band low-noise amplifier (LNA) is usually measured by the input third-order intercept Point IIP_3 . From equation (2.46) in Chapter 2, if the amplitudes are the same for both the desired and undesired input signals in a "two-tone" test, the IIP_3 can be defined as:

$$IIP_3 = \sqrt{\frac{4}{3} \left| \frac{\alpha_1}{\alpha_3} \right|}, \quad (3.26)$$

where coefficients α_1 and α_3 are constants, and they are the first and third order coefficients in the polynomial approximation of the non-linear characteristic of the LNA, see equation (2.40) in Chapter 2.

3.2.4 Input and Output Return Loss

The source and load impedances are assumed $R_S = R_L = 50 = Z_O$. If the input and output matching networks are not perfect, then from equations (3.14) and (3.15), we have $\Gamma_{in} = S_{11}$ and $\Gamma_{out} = S_{22}$. Therefore, S_{11} is defined as the input return loss while S_{22} is defined as the output return loss. Normally both of those quantities should be below -10 dB in order to achieve good performance.

3.2.5 Power Dissipation

The power consumption of an LNA can be defined as [25]:

$$P = I_D V_{DD}, \quad (3.27)$$

where I_D is the DC current of the LNA circuit and V_{DD} is the supply voltage.

3.3 Narrow-Band LNA Topologies

3.3.1 Inductively Source Degenerated LNA

As mentioned previously, noise from resistors is a major factor at the amplifier input stage. Theoretically therefore, we should avoid using resistors in LNA design. However, it is necessary to build an input matching network in order to optimize the performance. Therefore, implementing both low noise and input matching is a key factor of an LNA design. One possible method is to employ the so-called inductive source degeneration technique, which is widely used in narrow-band LNA circuit designs.

Inductive source degeneration is implemented by placing an inductor at the source terminal, shown in Figure 3.3. Such a circuit is referred to as inductively degenerated common-source amplifier [30]. An important advantage of this method is that it can create a real input impedance without the use of real resistors.

In order to simplify the analysis and more clearly show the design theory, only a single MOSFET transistor with an inductor L_S at the source terminal will be analyzed here. Its high-frequency small-signal equivalent circuit can be readily

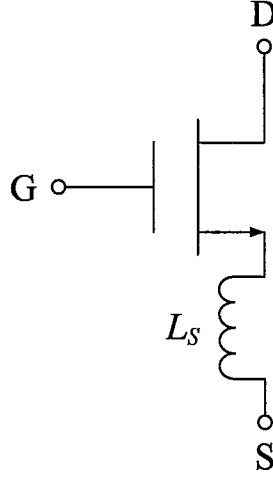


Figure 3.3: Inductively source degenerated amplifier.

obtained and is shown in Figure 3.4. In order to calculate the input impedance Z_{in} , a test voltage and current is applied at the gate terminal.

From the circuit in Figure 3.4, the gate-source voltage is:

$$V_{gs} = V_{test} - V_S. \quad (3.28)$$

By applying Kirchhoff's Current Law (KCL) at the node shown in Figure 3.4, we obtain:

$$\frac{V_{test} - V_S}{\frac{1}{sC_{gs}}} + g_m(V_{test} - V_S) = \frac{V_S}{sL_S}. \quad (3.29)$$

where $s = j\omega = j2\pi f$ The test current can be expressed as:

$$I_{test} = \frac{V_{test} - V_S}{\frac{1}{sC_{gs}}}. \quad (3.30)$$

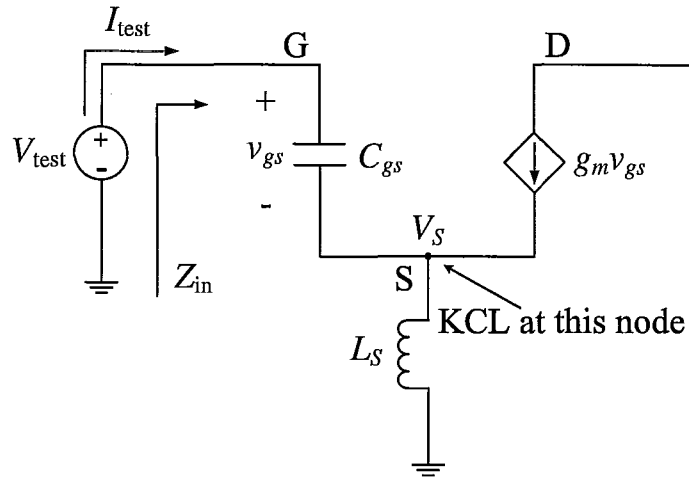


Figure 3.4: Small-signal equivalent circuit of inductively source degenerated amplifier.

Rewriting equation (3.30) to express V_S :

$$V_S = V_{\text{test}} - \frac{I_{\text{test}}}{sC_{gs}}. \quad (3.31)$$

Substituting equation (3.31) into (3.29), we have:

$$\begin{aligned}
& \frac{V_{\text{test}} - \left(V_{\text{test}} - \frac{I_{\text{test}}}{sC_{gs}}\right)}{\frac{1}{sC_{gs}}} + g_m \left(V_{\text{test}} - \left(V_{\text{test}} - \frac{I_{\text{test}}}{sC_{gs}}\right)\right) = \frac{V_{\text{test}} - \frac{I_{\text{test}}}{sC_{gs}}}{sL_S}, \\
\Rightarrow & \frac{\frac{I_{\text{test}}}{sC_{gs}}}{\frac{1}{sC_{gs}}} + g_m \left(\frac{I_{\text{test}}}{sC_{gs}}\right) = \frac{V_{\text{test}}}{sL_S} - \frac{I_{\text{test}}}{s^2C_{gs}L_S}, \\
\Rightarrow & I_{\text{test}} + \frac{g_m I_{\text{test}}}{sC_{gs}} = \frac{V_{\text{test}}}{sL_S} - \frac{I_{\text{test}}}{s^2C_{gs}L_S}, \\
\Rightarrow & I_{\text{test}} \left(\frac{1}{s^2C_{gs}L_S} + 1 + \frac{g_m}{sC_{gs}}\right) = \frac{V_{\text{test}}}{sL_S}, \\
\Rightarrow & \frac{V_{\text{test}}}{I_{\text{test}}} = sL_S \left(\frac{1}{s^2C_{gs}L_S} + 1 + \frac{g_m}{sC_{gs}}\right), \\
\Rightarrow & Z_{\text{in}} = \frac{V_{\text{test}}}{I_{\text{test}}} = sL_S \left(\frac{1}{s^2C_{gs}L_S} + 1 + \frac{g_m}{sC_{gs}}\right), \\
\Rightarrow & Z_{\text{in}} = sL_S + \frac{1}{sC_{gs}} + \frac{g_m L_S}{C_{gs}}. \tag{3.32}
\end{aligned}$$

Equation (3.32) shows that there is a real part, $\frac{g_m L_S}{C_{gs}}$, in the input impedance. Therefore, this inductive source degeneration method can provide a matching input impedance without real resistors. Because of this, the inductively source degenerated LNA is widely used in receiver front-end designs. The second condition for truly active matching is $\omega^2 L_S C_{gs} = 1$.

3.4 Mixer Fundamentals

A mixer, also known as a frequency converter, is used to translate the signals from one frequency band to another frequency band, with a certain gain and low distortion. Typically, the conversion is from a Radio Frequency (RF) ω_{rf} to a desired frequency, normally called the Intermediate Frequency (IF) ω_{if} . There are two types

of mixers: passive and active. Passive mixers only use the dynamic power of the RF signal instead from a DC voltage supply. This results in a conversion gain of less than one (conversion loss). Active mixers, on the other hand, achieve high conversion gain at the cost of poor linearity (high distortion). These mixers also dissipates quiescent power due to the requirement for a DC supply. This thesis focuses on active down-conversion mixers since they are used in receiver part.

The fundamental idea of frequency translation by a mixer is to multiply a local oscillator (LO) signal at ω_{lo} with a radio frequency (RF) signal at ω_{rf} and select the product with the required frequency. In mathematical terms, let the RF signal be $y_{rf}(t) = A_{rf} \cos(\omega_{rf}t)$, and the LO signal be $y_{lo}(t) = A_{lo} \cos(\omega_{lo}t)$. A mixer can thus be modeled by multiplying these two signals together as shown below:

$$y(t) = y_{rf}(t) \cdot y_{lo}(t) = A_{rf} \cos \omega_{rf}t \cdot A_{lo} \cos \omega_{lo}t, \quad (3.33)$$

which yields [25,31]:

$$\begin{aligned} y(t) &= A_{rf} \cos \omega_{rf}t \cdot A_{lo} \cos \omega_{lo}t, \\ &= \frac{A_{rf}A_{lo}}{2} [\cos(\omega_{rf} - \omega_{lo})t + \cos(\omega_{rf} + \omega_{lo})t]. \end{aligned} \quad (3.34)$$

From equation (3.34), it is obvious that two frequency translations of the signal ω_{rf} occur. By means of multiplication, the difference (down-conversion) and sum (up-conversion) between RF and LO frequencies create an output signal whose amplitude is proportional to RF and LO amplitudes. Therefore, if the LO amplitude is constant (as it usually is), any amplitude modulation in the RF signal is transferred to the IF signal [30]. In circuit design simulators (in our case, Cadence),

the RF port and the LO port are used to represent these two distinct inputs. The RF port simulates the input signal to be converted by the mixer while the LO port simulates the periodic waveform generated by the local oscillator. The multiplication function of a mixer is implemented as a switch controlled by the LO signal in order to mix with the RF signal. Figure 3.5 shows single switch implementation of a mixer [32].

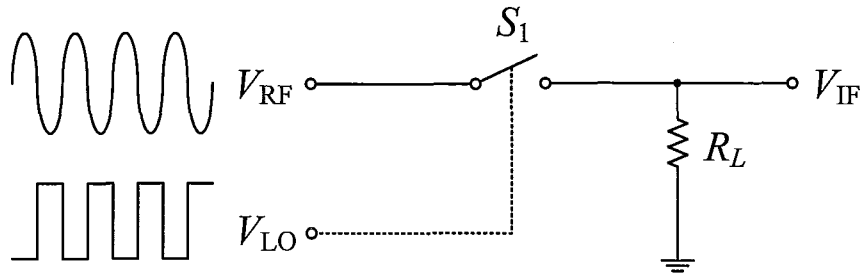


Figure 3.5: Simple switch used as mixer [32].

When switch S_1 is on, the IF output is equal to the RF input. When switch S_1 is off, the IF output is zero. Therefore, this operation can be viewed as a form of mixer because it is a multiplication of the RF signal by a periodic rectangular waveform (LO signal).

To implement this as an analog CMOS circuit, the LO signal is applied to the gate of a MOSFET while the RF signal is applied to the source/drain provided that the device is biased properly. Figure 3.6 illustrates this application using an NMOS device as a transmission switch.

The LO signal at the gate of the NMOS performs a switching function, which is ideally a periodic rectangular waveform with a period $T_{lo} = 2\pi/\omega_{lo}$, where ω_{lo} is the LO operating frequency, as shown in Figure 3.7. Here, $y_{lo}(t)$ denotes the LO

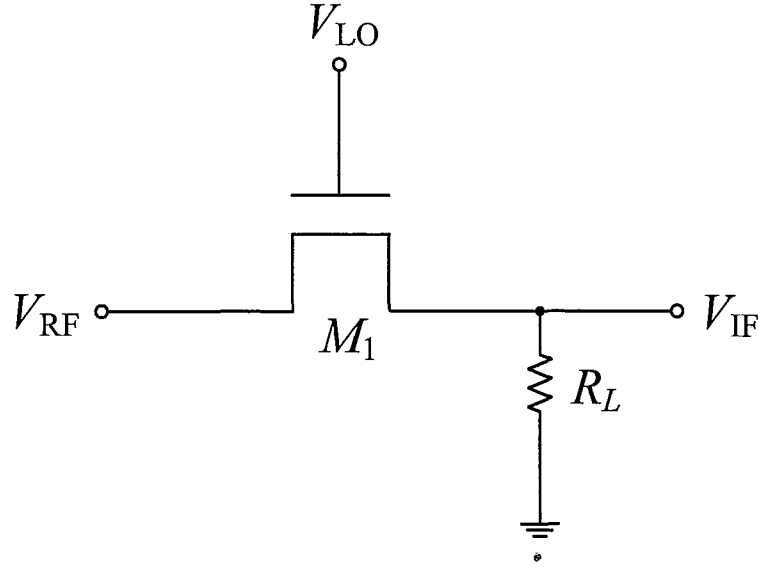


Figure 3.6: Implementation of a switch with an NMOS device [32].

signal, $y_{rf}(t)$ denotes the RF signal, and $y_{if}(t)$ denotes the IF signal. The behaviour of this NMOS implementation should be discussed according to two cases.

Case I: large amplitude (A_{lo}) of LO signal

In this case, we assume A_{lo} is large enough to switch the NMOS on and off. In this case, the transistor can be modeled as a periodic rectangular waveform that switches at frequency ω_{lo} with unity amplitude, shown in Figure 3.7. By applying Fourier series representation to this periodic rectangular signal, $y_{lo}(t)$ can be expanded as [25]:

$$y_{lo}(t) = \frac{1}{2} + \frac{2}{\pi} \cos \omega_{lo}(t) - \frac{2}{3\pi} \cos 3\omega_{lo}(t) + \dots \quad (3.35)$$

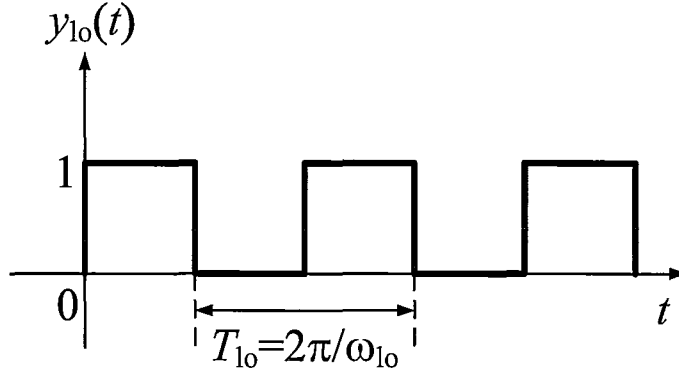


Figure 3.7: Periodic rectangular waveform of LO signal.

which can be further rearranged as:

$$y_{lo}(t) = \frac{1}{2} + \sum_{n=1}^{\infty} \frac{\sin\left(\frac{n\pi}{2}\right)}{\frac{n\pi}{2}} \cos(n\omega_{lo}t). \quad (3.36)$$

Substituting into equation (3.33), $y(t)$ can be shown to be

$$y(t) = A_{rf} \cos \omega_{rf} t \left[\frac{1}{2} + \sum_{n=1}^{\infty} \frac{\sin\left(\frac{n\pi}{2}\right)}{\frac{n\pi}{2}} \cos(n\omega_{lo}t) \right]. \quad (3.37)$$

If an appropriate bandpass filter is used to filter out those signals at high frequencies, then the desired IF signal $y_{if}(t)$ at $\omega_{if} = \omega_{rf} - \omega_{lo}$ can be obtained [31]:

$$y_{if}(t) = \left(\frac{A_{rf}}{\pi} \right) \cos(\omega_{rf} - \omega_{lo})t, \quad (3.38)$$

This is not a function of the amplitude A_{lo} of the large signal, which drives the gate of the MOSFET. This is a commonly used method for mixer designs as the second case has a critical drawback.

Case II: small amplitude (A_{lo}) of LO signal

In this case, y_{lo} is a small signal that can not be described purely in terms of an on/off switch (1 and 0 in Figure 3.7), while $y(t)$ is still the same as equation (3.34). It can be shown that the desired $y_{if}(t)$ is given by [31]:

$$y_{if}(t) = A_{lo} \left(\frac{A_{rf}}{2} \right) \cos(\omega_{rf} - \omega_{lo})t, \quad (3.39)$$

which is a function of A_{lo} . The disadvantage of this is that y_{if} depends on A_{lo} , which creates difficulties in controlling the conversion gain G_c , since A_{lo} is generated outside of the mixers.

3.5 Performance of Active Mixer

3.5.1 Conversion Gain

One important factor of a mixer is the conversion gain (or loss) G_c . It is defined as the IF output signal amplitude A_{if} (or power P_{if}) divided by the RF input signal amplitude A_{rf} (or power P_{rf}) at their respective centre frequencies [25]. However, this gain must be carefully defined in order to avoid confusion between voltage conversion gain and power conversion gain. Typically, power gain and voltage gain in a mixer are defined as power conversion gain and voltage conversion gain since the signal is converted from one frequency to another.

- Voltage conversion gain of a mixer is defined as the ratio of the rms (root mean square) voltage of the IF signal to the rms voltage of the RF signal [32].

If a sinusoidal input wave is applied, the rms voltage is $V_{rms} = \frac{V_{peak}}{\sqrt{2}}$.

- Power conversion gain of a mixer is defined as the IF power delivered to the load divided by the available RF power from the source [32].

The definitions of equations (2.16) and (2.17) in Chapter 2 can be applied to the conversion gain of a mixer. Therefore, the voltage conversion gain $G_c(\text{voltage})$ and the power conversion gain $G_c(\text{power})$ in decibels can be obtained as:

$$G_c(\text{voltage}) = 20 \log \left| \frac{v_O}{v_I} \right|, \quad (3.40)$$

$$G_c(\text{power}) = 10 \log \left| \frac{P_L}{P_I} \right| = 10 \log \left| \frac{v_O i_O}{v_I i_I} \right|. \quad (3.41)$$

If the input and output resistances are matched, from equation (2.21), the power conversion gain is equal to the voltage conversion gain in decibels.

$$G_c(\text{power}) = G_c(\text{voltage}). \quad (3.42)$$

If they are mismatched however, the relationship between the power conversion gain and the voltage conversion gain can be expressed from equation (2.22) as

$$G_c(\text{power}) = G_c(\text{voltage}) + 10 \log \left| \frac{R_{in}}{R_L} \right|. \quad (3.43)$$

For different types of mixers, the conversion gain is defined and calculated differently. For example, the conversion gain of unbalanced mixer, single balanced mixer, or double balanced mixer is different and the details will be discussed later in section for mixer topologies.

3.5.2 Noise

The definition of the noise figure (NF) of a mixer is different from that of a Low-Noise Amplifier (LNA) and needs to be carefully defined and understood since the distinction is subtle. In a typical mixer, there are two input frequencies, which are the desired RF signal and the image signal. Both of them will generate the intermediate frequency (IF) and are normally referred to as sidebands.

As has already been discussed, the IF frequency is the difference between the RF and LO frequencies. Therefore, signals with equal amount to the IF frequency which locates above or below LO frequency (ω_{lo}) will both produce the IF signal at the same frequency (ω_{if}). Hence, these two input frequencies are separated by $2\omega_{if}$ centered at ω_{lo} . This phenomenon is shown in Figure 3.8.

This leads to two different definitions of the noise figure for a mixer. If the desired signal only exists at the RF frequency, the term noise figure is defined as the single-sideband noise figure (SSB NF). On the other hand, if the desired signals exist at both the RF frequency and the image frequency, then the noise figure is defined as the double-sideband noise figure (DSB NF). However, DSB NF is the rarer case since the existence of an image frequency complicates noise figure computations. This is because the IF noise originates from both the desired and image frequencies where there is generally no desired signal at the image frequency [30].

Generally, the DSB noise figure is lower than the SSB noise figure due to a higher noise power at the input (N_{in}). In other words, if the IF noise power for both sidebands of the input are equal, this leads to an SNR_{in} of the case that SSB is higher than that for the DSB case since the noise power from the input N_{in} for SSB case is lower than that for the DSB. As a result, the SSB noise figure will be higher

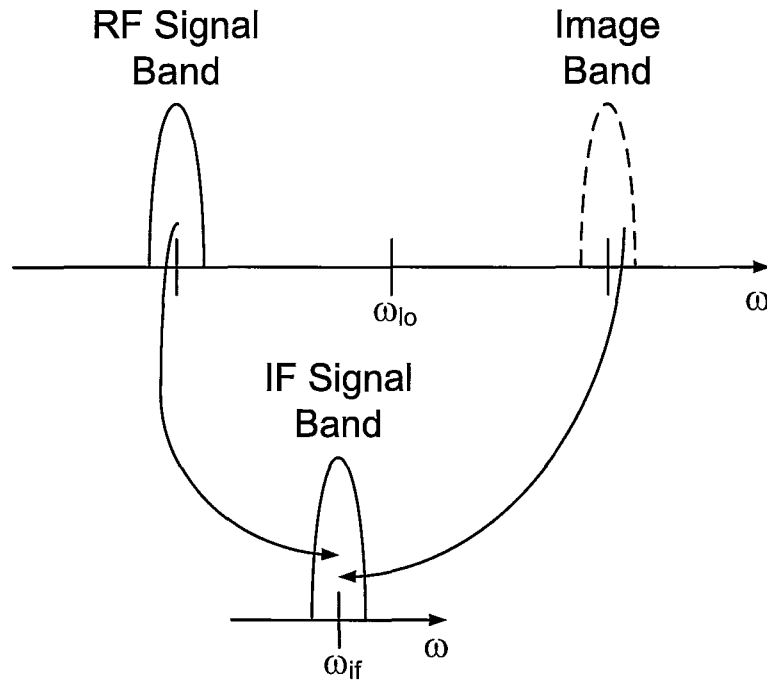


Figure 3.8: Folding of RF and image noise into the IF band [32].

than the DSB noise figure by 3dB if the noise powers of both sidebands are equal.

The noise figure for mixers tend to be considerably higher than for amplifiers because noise from frequencies other than at the desired RF can mix down to the IF [30]. Representative values for SSB noise figure range from 10dB to 15dB or more [30]. This is why in most receiver front-end designs, low-noise amplifiers are required. If the LNA has sufficient gain, then the RF signals can be amplified so that they are well above the noise levels of the mixer. Therefore, the overall NF will be dominated by the LNA and the noise effect by the mixer will diminish.

3.5.3 Linearity

The distortion and linearity of a mixer should be discussed according to two cases: the low-frequency case and the high-frequency case.

In the low-frequency case, the distortion parameters can be calculated according to [25]:

$$\text{HD}_3 = \frac{A_{rf}^2}{32} \frac{1}{(V_{GS1} - V_t)^2}, \quad (3.44)$$

$$\text{IM}_3 = \frac{3A_{\text{interference}}^2}{32 (V_{GS1} - V_t)^2}, \quad (3.45)$$

and,

$$A_{\text{IP3}} = \sqrt{\frac{32}{3}} (V_{GS1} - V_t), \quad (3.46)$$

where V_{GS1} is the gate to source terminal voltage of the MOSFET transistor M_1 , shown in Figure 3.13, and V_t is the threshold voltage of the MOSFET.

In the high-frequency case, the distortion parameters are [25]:

$$\text{IM}_3 = \frac{3A_{\text{interference}}^2}{32 (V_{GS1} - V_t)^2} \left[\left| 1 - \frac{2}{3} \frac{j(\omega_1)C_d}{2k(V_{GS} - V_t)} \right| \right], \quad (3.47)$$

where k is defined from MOSFET small-signal equation as following:

$$i_d = \frac{k}{2} (v_{rf} - v_s)^2, \quad (3.48)$$

where $j(\omega_1)$ is a constant coefficient, and C_d is the capacitance parallel to the current source I_{SS} due to high-frequency effect. Note that I_{SS} is shown in Figure 3.13.

Note that here we only show the final equations since the detailed derivation can be found in [25].

3.5.4 Feedthrough

In some types of mixers (typically un-balanced mixers), the RF and LO components appear at the mixer outputs. These undesired signals are called the RF feedthrough and LO feedthrough. In principle, the double balanced mixer can eliminate feedthrough, or at least in practice, can minimize feedthrough and thus improve the mixer performance.

3.5.5 Port-to-Port Isolation

Another desirable characteristic of a mixer is isolation among the RF, LO, and IF ports in order to minimize interaction. For example, if LO and IF frequencies are similar, a strong interference signal will appear at the IF output since normally the LO signal is quite large compared with that of RF signal. Therefore, the LO-IF isolation is important in order to avoid this out-of-band interaction. However, a filter stage usually follows the mixer stage and this problem may not be very important. The undesired signal can be filtered out if good isolation is achieved.

3.6 Mixer Topologies

3.6.1 Unbalanced Mixer

An unbalanced mixer, the simplest type of active mixers, is shown in Figure 3.9 [25]. In this circuit, the transistor M_1 is biased properly in order to convert the RF voltage signal $V_{rf}(t)$ to RF current signal $I_{rf}(t)$. Typically, the RF input is a small signal which has normally around -30dBm power, shown in Figure 3.10 [31], where

V_{G1} is the DC bias voltage of transistor M_1 . Therefore, M_1 operates as a transconductance amplifier, which amplifies the RF signal by a certain gain proportional to the transconductance g_{m1} . We use g_{m1} to denote the transconductance of M_1 . M_2 and M_3 are modeled as LO switches to mix the RF and LO signals. The basic principle behind this circuit is that:

1. the RF input voltage $V_{rf}(t)$ is converted to the RF current signal $I_{rf}(t)$ by M_1 ,
2. the RF current signal is mixed with the LO signal to create the desired IF current signal $I_{if}(t)$, by switching I_{rf} to flow either through M_2 or M_3 , and finally,
3. the IF current signal $I_{if}(t)$ flows into a resistor R_L and develops the IF output signal $V_{if}(t)$.

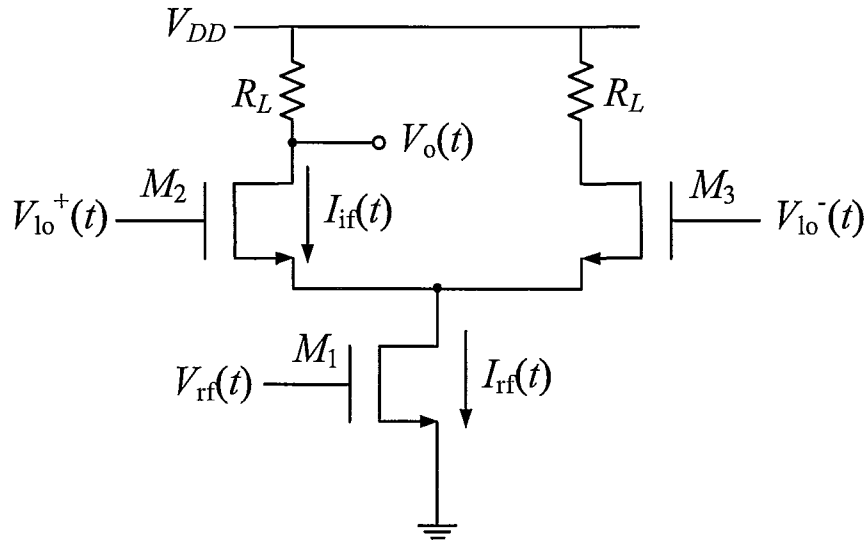


Figure 3.9: Unbalanced mixer [25].

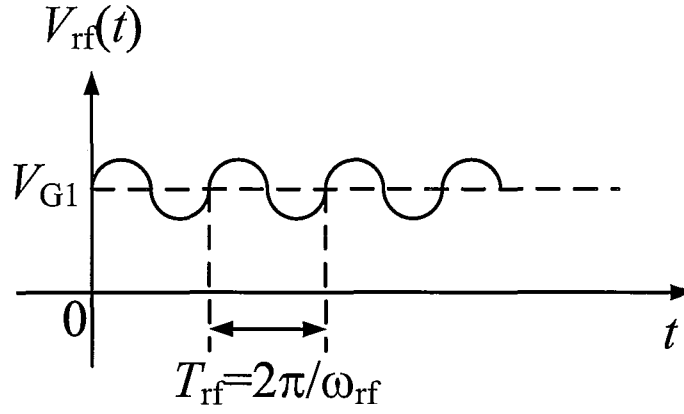


Figure 3.10: RF input signal [31].

Considering the DC current I_{DC} flowing through M_1 , the RF current signal, which is converted from the RF voltage signal is [31]:

$$I_{rf}(t) = I_{DC} + g_m A_{rf} \cos(\omega_{rf} t). \quad (3.49)$$

From equation (3.36), the LO signal $V_{lo}^+(t)$ can be obtained as:

$$V_{lo}^+(t) = \frac{1}{2} + \sum_{n=1}^{\infty} \frac{\sin\left(\frac{n\pi}{2}\right)}{\frac{n\pi}{2}} \cos(n\omega_{lo} t), \quad (3.50)$$

where $V_{io}^+(t)$ is the rectangular waveform, shown in Figure 3.12(a). Then, the mixed output signal of LO and RF from Figure 3.9 can be expressed as [31]:

$$\begin{aligned} V_o(t) &= V_o^+(t), \\ &= R_L(I_{DC} + g_m A_{rf} \cos \omega_{rf} t) \left[\frac{1}{2} + \sum_n \frac{\sin\left(\frac{n\pi}{2}\right)}{\frac{n\pi}{2}} \cos(n\omega_{lo} t) \right], \end{aligned} \quad (3.51)$$

$$\begin{aligned} &= R_L \left[\left(\frac{I_{DC}}{2} + \frac{g_m A_{rf} \cos \omega_{rf} t}{2} \right) \right. \\ &\quad \left. + (I_{DC} + g_m A_{rf} \cos \omega_{rf} t) \left[\sum_n \frac{\sin\left(\frac{n\pi}{2}\right)}{\frac{n\pi}{2}} \cos(n\omega_{lo} t) \right] \right]. \end{aligned} \quad (3.52)$$

Using equations (3.35) and (3.36), equation (3.52) can be rewritten as:

$$\begin{aligned} V_o(t) &= R_L \left(\frac{I_{DC}}{2} + \frac{g_m A_{rf} \cos \omega_{rf} t}{2} + \frac{2I_{DC}}{\pi} \cos \omega_{lo} t \right. \\ &\quad \left. + \left(\frac{2g_m A_{rf}}{\pi} \right) \cos \omega_{rf} t \cdot \cos \omega_{lo} t + \dots \right), \end{aligned} \quad (3.53)$$

where there are no even harmonics ($n = 2, 4, 6, \dots$). Analyzing equation (3.53), the output voltage V_o across R_L has the following components:

- the DC component: $R_L \left(\frac{I_{DC}}{2} \right)$,
- the RF feedthrough: $R_L \left(\frac{g_m A_{rf} \cos \omega_{rf} t}{2} \right)$,
- the LO feedthrough: $R_L \left(\frac{2I_{DC}}{\pi} \cos \omega_{lo} t \right)$, and
- the desired IF signal: $R_L \left(\frac{2g_m A_{rf}}{\pi} \right) \cos \omega_{rf} t \cdot \cos \omega_{lo} t$.

It can be seen that the RF and LO feedthrough appear significant at the output, which is undesired. Therefore, the drawback of unbalanced mixer is that it creates RF and LO feedthrough.

From above, the desired IF signal can be expressed as:

$$V_{if}(t) = R_L \left(\frac{2g_m A_{rf}}{\pi} \right) \cos \omega_{rf} t \cdot \cos \omega_{lo} t, \quad (3.54)$$

which can be further expanded according to equation (3.34) as:

$$V_{if}(t) = R_L \left(\frac{2g_m A_{rf}}{\pi} \right) \frac{1}{2} [\cos(\omega_{rf} - \omega_{lo})t + \cos(\omega_{rf} + \omega_{lo})t]. \quad (3.55)$$

The desired IF signal $y_{if}(t)$ at $\omega_{if} = \omega_{rf} - \omega_{lo}$ can be obtained if an appropriate bandpass filter is used to filter out high frequency terms. Hence, the expression IF $y_{if}(t)$ becomes:

$$y_{if}(t) = R_L \left(\frac{2g_m A_{rf}}{\pi} \right) \frac{1}{2} \cos(\omega_{rf} - \omega_{lo})t, \quad (3.56)$$

The amplitude of the IF signal is:

$$A_{if} = \frac{R_L}{2} \left(\frac{2g_m A_{rf}}{\pi} \right), \quad (3.57)$$

where the amplitude of the RF input signal is A_{rf} . Therefore, the conversion gain of an unbalanced mixer is given by [31]:

$$\begin{aligned} G_c &= \frac{A_{if}}{A_{rf}} = \frac{R_L}{2} \frac{\left(\frac{2g_m A_{rf}}{\pi} \right)}{A_{rf}}, \\ &= \frac{g_m R_L}{\pi}. \end{aligned} \quad (3.58)$$

3.6.2 Single Balanced Mixer

The single balanced mixer, shown in Figure 3.11, takes differential output signals instead of single side output signal. It is an improvement over the unbalanced mixer. The working principle of the single balanced mixer is introduced here in order to confirm this improvement.

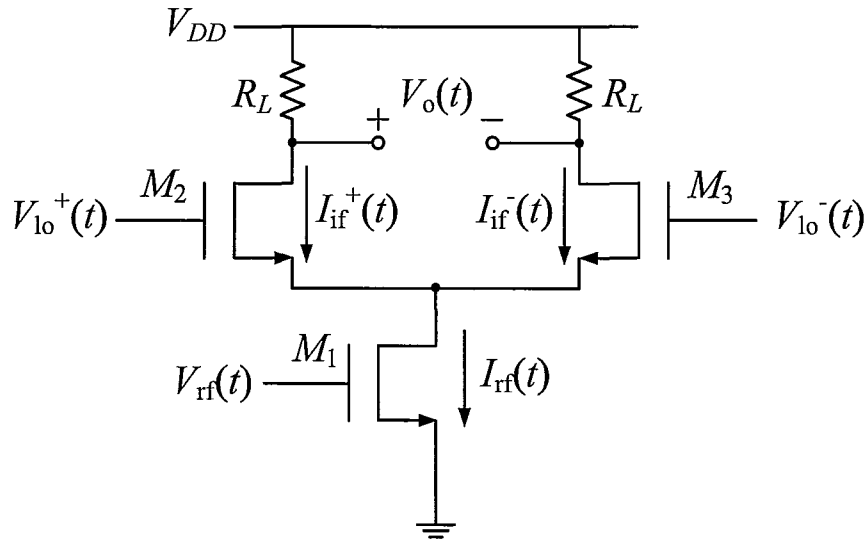


Figure 3.11: Single balanced mixer [25].

The differential LO signals, $V_{lo}^+(t)$ and $V_{lo}^-(t)$, are 180 degree out of phase as shown in Figure 3.12. Hence, it can be expressed mathematically as:

$$V_{lo}^-(t) = V_{lo}^+ \left(t - \frac{T_{lo}}{2} \right) = V_{lo}^+ \left(t - \frac{\pi}{\omega_{lo}} \right). \quad (3.59)$$

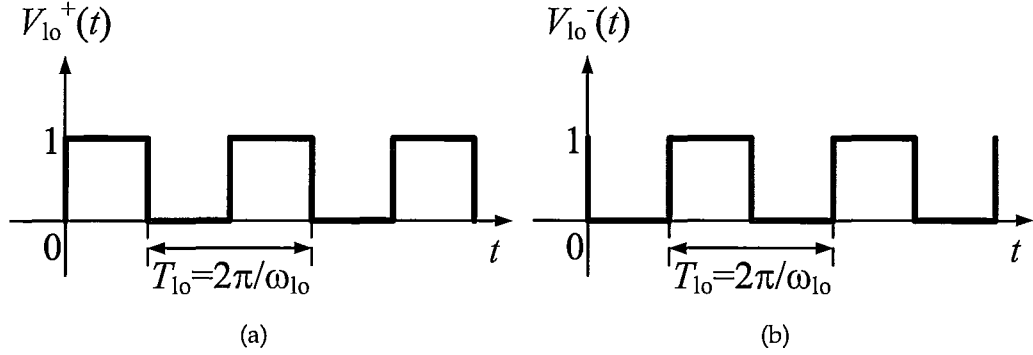


Figure 3.12: Differential LO signals: (a) V_{lo}^+ , and (b) V_{lo}^- [31].

Based on equation (3.50), $V_{lo}^-(t)$ can be obtained as [31]:

$$\begin{aligned}
 V_{lo}^-(t) &= V_{lo}^+(t - \frac{\pi}{\omega_{lo}}), \\
 &= \frac{1}{2} + \sum_{n=1}^{\infty} \frac{\sin(\frac{n\pi}{2})}{\frac{n\pi}{2}} \cos\left[n\omega_{lo}\left(t - \frac{\pi}{\omega_{lo}}\right)\right], \\
 &= \frac{1}{2} - \sum_{n=1}^{\infty} \frac{\sin(\frac{n\pi}{2})}{\frac{n\pi}{2}} \cos(n\omega_{lo}t),
 \end{aligned} \tag{3.60}$$

where there are no even ($n = 2, 4, 6, \dots$) RF harmonics. Recall from the expressions of $V_{lo}^+(t)$ in equations (3.51) and (3.52), $V_{lo}^-(t)$ can be further expanded as [31]:

$$V_o^-(t) = R_L(I_{DC} + g_m A_{rf} \cos \omega_{rf} t) \left[\frac{1}{2} - \sum_n \frac{\sin(\frac{n\pi}{2})}{\frac{n\pi}{2}} \cos(n\omega_{lo}t) \right], \tag{3.61}$$

$$\begin{aligned}
 &= R_L \left[\left(\frac{I_{DC}}{2} + \frac{g_m A_{rf} \cos \omega_{rf} t}{2} \right) \right. \\
 &\quad \left. - (I_{DC} + g_m A_{rf} \cos \omega_{rf} t) \left[\sum_n \frac{\sin(\frac{n\pi}{2})}{\frac{n\pi}{2}} \cos(n\omega_{lo}t) \right] \right],
 \end{aligned} \tag{3.62}$$

where $V_o^+(t)$ is the same as equation (3.52), recall here:

$$V_o^+(t) = R_L \left[\left(\frac{I_{DC}}{2} + \frac{g_m A_{rf} \cos \omega_{rf} t}{2} \right) + (I_{DC} + g_m A_{rf} \cos \omega_{rf} t) \left[\sum_n^{\infty} \frac{\sin\left(\frac{n\pi}{2}\right)}{\frac{n\pi}{2}} \cos(n\omega_{lo} t) \right] \right]. \quad (3.63)$$

Since $V_o(t)$ is the differential output of two branches, it can be defined as:

$$V_o(t) = V_o^+(t) - V_o^-(t). \quad (3.64)$$

Substituting equations (3.62) and (3.63) into equation (3.64), the output of a single balanced mixer can be obtained by [31]:

$$\begin{aligned} V_o(t) &= V_o^+(t) - V_o^-(t) \\ &= 2R_L(I_{DC} + g_m A_{rf} \cos \omega_{rf} t) \left[\sum_n^{\infty} \frac{\sin\left(\frac{n\pi}{2}\right)}{\frac{n\pi}{2}} \cos(n\omega_{lo} t) \right]. \end{aligned} \quad (3.65)$$

Equation (3.65) can be rewritten as:

$$\begin{aligned} V_o(t) &= 2R_L(I_{DC} + g_m A_{rf} \cos \omega_{rf} t) \left[\frac{2}{\pi} \cos \omega_{lo} t - \frac{2}{3\pi} \cos 3\omega_{lo} t + \dots \right] \\ &= 2R_L \left(\frac{2I_{DC}}{\pi} \cos \omega_{lo} t + \left(\frac{2g_m A_{rf}}{\pi} \right) \cos \omega_{rf} t \cdot \cos \omega_{lo} t + \dots \right). \end{aligned} \quad (3.66)$$

Analyzing equation (3.66), there are mainly two terms:

- the LO feedthrough: $2R_L \left(\frac{2I_{DC}}{\pi} \cos \omega_{lo} t \right)$, and
- the desired IF signal: $2R_L \left(\frac{2g_m A_{rf}}{\pi} \right) \cos \omega_{rf} t \cdot \cos \omega_{lo} t$.

It can be seen that only the LO feedthrough appears at the output as undesired

signal. The RF feedthrough is removed from the differential output signal. In addition, even RF harmonics also disappear in the output. However, the LO feedthrough still exists, which is the drawback of single balanced mixers. Nonetheless, it still improves the output to remove the RF feedthrough compared to unbalanced mixers.

The desired IF signal is:

$$\begin{aligned} V_{if}(t) &= 2R_L \left(\frac{2g_m A_{rf}}{\pi} \right) \cos \omega_{rf} t \cdot \cos \omega_{lo} t \\ &= 2R_L \left(\frac{2g_m A_{rf}}{\pi} \right) \frac{1}{2} [\cos(\omega_{rf} - \omega_{lo})t + \cos(\omega_{rf} + \omega_{lo})t]. \end{aligned} \quad (3.67)$$

If applying an appropriate bandpass filter to filter out high frequency terms, the desired IF signal $y_{if}(t)$ at $\omega_{if} = \omega_{rf} - \omega_{lo}$ becomes:

$$V_{if}(t) = 2R_L \left(\frac{2g_m A_{rf}}{\pi} \right) \frac{1}{2} \cos(\omega_{rf} - \omega_{lo})t. \quad (3.68)$$

The amplitude of the IF signal is:

$$A_{if} = R_L \left(\frac{2g_m A_{rf}}{\pi} \right). \quad (3.69)$$

Therefore, the conversion gain of a single balanced mixer is given by [31]:

$$\begin{aligned} G_c &= \frac{A_{if}}{A_{rf}} = R_L \frac{\left(\frac{2g_m A_{rf}}{\pi} \right)}{A_{rf}} \\ &= \frac{2g_m R_L}{\pi}, \end{aligned} \quad (3.70)$$

which doubles the gain of an unbalanced mixer shown in equation (3.58). This is

another improvement from single balanced mixer to unbalanced mixer.

3.6.3 Double Balanced Mixer

Double balanced mixer, a combination of two single balanced mixers, is typically called Gilbert mixer, shown in Figure 3.13 [25]. This is the most commonly used mixer in RF circuit designs and this thesis will focus on it.

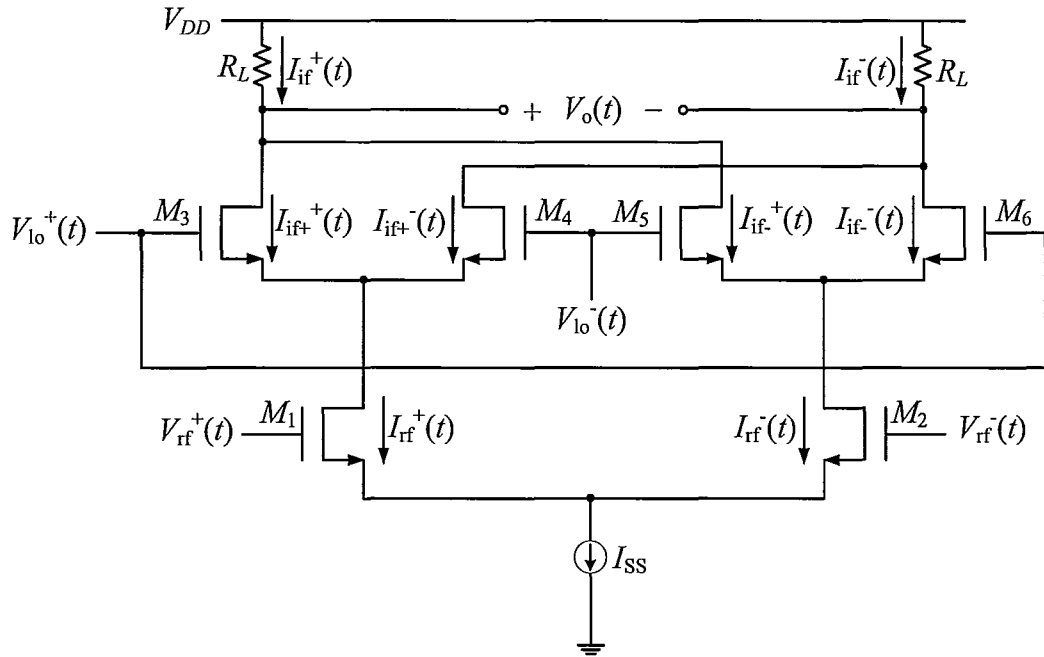


Figure 3.13: Double balanced mixer [25].

The method to calculate the IF output signal and conversion gain is quite similar to that of single balanced mixer. This time, there are two RF differential input signals, which are 180 degree out of phase, shown in Figure 3.14 [31]. Refereing to

equation (3.33), if we assume:

$$V_{rf}^+(t) = A_{rf} \cos(\omega_{rf}t), \quad (3.71)$$

then $V_{rf}^-(t)$ can be obtained as:

$$\begin{aligned} V_{rf}^-(t) &= V_{rf}^+\left(t - \frac{T_{rf}}{2}\right) = V_{rf}^+\left(t - \frac{\pi}{\omega_{rf}}\right) \\ &= A_{rf} \cos\left[\omega_{rf}\left(t - \frac{\pi}{\omega_{rf}}\right)\right] \\ &= -A_{rf} \cos(\omega_{rf}t). \end{aligned} \quad (3.72)$$

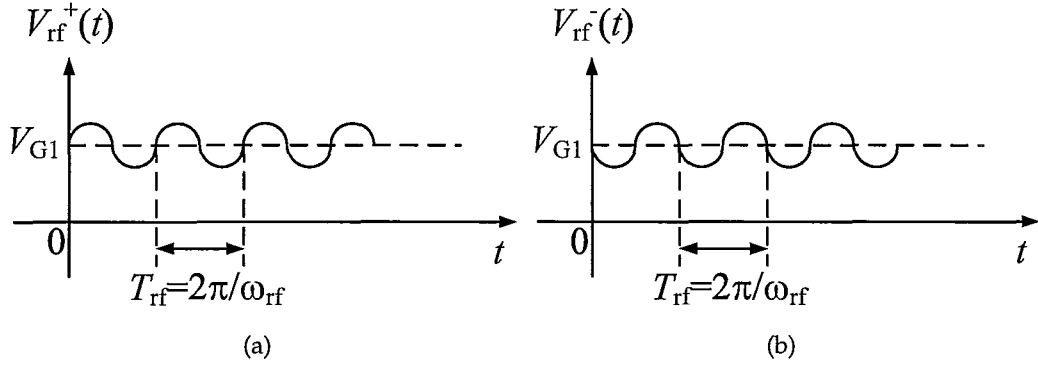


Figure 3.14: Differential RF input signals: (a) V_{rf}^+ , (b) V_{rf}^- [31].

Now instead of calculating the voltage, we will calculate the current at each branch, shown in Figure 3.13. Referring to equations (3.62) and (3.63), the currents

from each branch can be obtained as [31]:

$$I_{if+}^+(t) = \left(\frac{I_{DC}}{2} + \frac{g_m A_{rf} \cos \omega_{rf} t}{2} \right) + (I_{DC} + g_m A_{rf} \cos \omega_{rf} t) \left[\sum_n^{\infty} \frac{\sin\left(\frac{n\pi}{2}\right)}{\frac{n\pi}{2}} \cos(n\omega_{lo} t) \right], \quad (3.73)$$

$$I_{if+}^-(t) = \left(\frac{I_{DC}}{2} + \frac{g_m A_{rf} \cos \omega_{rf} t}{2} \right) - (I_{DC} + g_m A_{rf} \cos \omega_{rf} t) \left[\sum_n^{\infty} \frac{\sin\left(\frac{n\pi}{2}\right)}{\frac{n\pi}{2}} \cos(n\omega_{lo} t) \right], \quad (3.74)$$

$$I_{if-}^+(t) = \left(\frac{I_{DC}}{2} - \frac{g_m A_{rf} \cos \omega_{rf} t}{2} \right) - (I_{DC} - g_m A_{rf} \cos \omega_{rf} t) \left[\sum_n^{\infty} \frac{\sin\left(\frac{n\pi}{2}\right)}{\frac{n\pi}{2}} \cos(n\omega_{lo} t) \right], \quad (3.75)$$

$$I_{if-}^-(t) = \left(\frac{I_{DC}}{2} - \frac{g_m A_{rf} \cos \omega_{rf} t}{2} \right) + (I_{DC} - g_m A_{rf} \cos \omega_{rf} t) \left[\sum_n^{\infty} \frac{\sin\left(\frac{n\pi}{2}\right)}{\frac{n\pi}{2}} \cos(n\omega_{lo} t) \right]. \quad (3.76)$$

From Figure 3.13, the differential output currents from these four branches can be summarized as:

$$I_{if}^+(t) = I_{if+}^+(t) + I_{if-}^+(t), \quad (3.77)$$

$$I_{if}^-(t) = I_{if+}^-(t) + I_{if-}^-(t). \quad (3.78)$$

Substituting equations (3.73), (3.74), (3.75) and (3.76) into equations (3.77) and

(3.78), the differential output currents can be expressed as:

$$I_{if}^+(t) = I_{DC} + 2g_m A_{rf} \cos \omega_{rf} t \left[\sum_n \frac{\sin\left(\frac{n\pi}{2}\right)}{\frac{n\pi}{2}} \cos(n\omega_{lo} t) \right], \quad (3.79)$$

$$I_{if}^-(t) = I_{DC} - 2g_m A_{rf} \cos \omega_{rf} t \left[\sum_n \frac{\sin\left(\frac{n\pi}{2}\right)}{\frac{n\pi}{2}} \cos(n\omega_{lo} t) \right]. \quad (3.80)$$

Therefore, the differential output voltage V_o can be obtained as:

$$\begin{aligned} V_o(t) &= V_o^+(t) - V_o^-(t) \\ &= R_L \cdot [I_{if}^+(t) - I_{if}^-(t)] \\ &= 4R_L g_m A_{rf} \cos \omega_{rf} t \left[\sum_n \frac{\sin\left(\frac{n\pi}{2}\right)}{\frac{n\pi}{2}} \cos(n\omega_{lo} t) \right]. \end{aligned} \quad (3.81)$$

Equation (3.81) can be expanded as:

$$V_o(t) = 4R_L g_m A_{rf} \cos \omega_{rf} t \left[\frac{2}{\pi} \cos \omega_{lo}(t) - \frac{2}{3\pi} \cos 3\omega_{lo}(t) + \dots \right]. \quad (3.82)$$

Analyzing equation (3.82), there is only one term:

- the tesired IF signal: $4R_L \left(\frac{2g_m A_{rf}}{\pi} \right) \cos \omega_{rf} t \cdot \cos \omega_{lo} t$

It can be seen that the LO feedthrough, the RF feedthrough and even RF harmonics all disappear from the output signal. This improves the performance compared to a single balanced mixer and an unbalanced mixer.

The desired IF signal is:

$$\begin{aligned} V_{if}(t) &= 4R_L \left(\frac{2g_m A_{rf}}{\pi} \right) \cos \omega_{rf} t \cdot \cos \omega_{lo} t, \\ &= 4R_L \left(\frac{2g_m A_{rf}}{\pi} \right) \frac{1}{2} [\cos(\omega_{rf} - \omega_{lo})t + \cos(\omega_{rf} + \omega_{lo})t]. \end{aligned} \quad (3.83)$$

If applying an appropriate bandpass filter to filter out high frequency terms, the desired IF signal $y_{if}(t)$ at $\omega_{if} = \omega_{rf} - \omega_{lo}$ becomes:

$$V_{if}(t) = 4R_L \left(\frac{2g_m A_{rf}}{\pi} \right) \frac{1}{2} \cos(\omega_{rf} - \omega_{lo})t. \quad (3.84)$$

The amplitude of the IF signal is

$$A_{if} = 2R_L \left(\frac{2g_m A_{rf}}{\pi} \right). \quad (3.85)$$

Therefore, the conversion gain of a double balanced mixer is given by [31]:

$$\begin{aligned} G_c &= \frac{A_{if}}{A_{rf}} = 2R_L \frac{\left(\frac{2g_m A_{rf}}{\pi} \right)}{A_{rf}} \\ &= \frac{4g_m R_L}{\pi}, \end{aligned} \quad (3.86)$$

which doubles the gain of a single balanced mixer shown in equation (3.70). This is another advantage of using a double balanced mixer.

Chapter 4

Ultra-Wideband LNA Theories

4.1 Ultra-Wideband LNA Fundamentals

An Ultra-wideband (UWB) low-noise amplifier (LNA) is usually the first stage of an UWB receiver. As approved by the FCC, the UWB receiver has a 3.1-10.6 GHz frequency range and so our UWB LNA design will focus on this bandwidth. The UWB LNA is designed to amplify the weak incoming RF signal without adding significantly to the noise level. To meet this requirement, the noise figure of a UWB receiver should normally be less than 7 dB [33]. Recall that the noise figure is dominated by the noise from the first stage. This emphasizes that the UWB LNA should minimize the amount of noise added as much as possible. Otherwise, the following stages will simply amplify this noise along with the signal. Therefore, a low noise figure is a strict requirement for a UWB LNA, together with the requirement for as large as possible gain, discussed below.

In addition to the NF, the effectiveness of the UWB device is also dependent upon the requirement of the amplifier to provide a high and flat gain over the

entire bandwidth of interest. It therefore follows that a good matching network over this frequency range is also necessary.

4.2 UWB LNA Performance

4.2.1 Gain

As discussed in Chapter 3, the gain of a narrow-band LNA can be defined in terms of S_{21} if the input and output impedances are well matched. This definition is still valid in ultra-wideband low-noise amplifier design. However, unlike narrow-band LNA, ultra-wideband LNA needs to achieve a flat gain through the entire 7.5-GHz bandwidth (normally UWB is defined in 3.1-10.6 GHz frequency range). This implies that the input and output matching networks need to be well matched over the entire 7.5-GHz frequency range, while the narrow-band LNA only operates around a certain single frequency point, at which the matching is relatively easy to achieve.

Most of the ultra-wideband LNA designs target a flat gain over the entire bandwidth. However, this requirement is so stringent that with current semiconductor technology, other performances metrics such as power or noise figure have to be sacrificed [34]. Thus, the UWB LNA design is a trade off between all of the performance characteristics, so we need to optimize all of the parameters simultaneously. Therefore, the overall performance of the amplifier is the critical objective.

Usually, the published UWB LNA designs report the gain as $G \pm \Delta G$ or $G_{\min} - G_{\max}$ for the entire bandwidth of interest in order to describe both the gain and the gain flatness. The term ΔG is used to define the gain flatness. Therefore, our UWB

LNA design will focus on both the gain and the gain flatness throughout the entire 3.1-10.6 GHz bandwidth.

4.2.2 Noise

We can use the same noise model and method for calculating the noise figure (NF) for ultra-wideband amplifier as was used for the narrow band case. However, unlike the narrow band LNA, the UWB LNA needs to have a low noise figure over the entire bandwidth instead of at one single frequency point. This means that the NF should be low and flat from 3.1 GHz to 10.6 GHz frequency range. Therefore, we must focus not only on having low noise figure but also on the flatness of the NF. In addition, different topologies lead to slightly different calculations for the noise figure. However, a simple method for estimating the noise figure is to assume that the noise on the source side is mostly thermally generated by the source resistor R_S . This results in voltage noise power spectral density (PSD) V_n^2 , reproduced from equation (3.23):

$$\overline{V_n^2} = 4kTR_S. \quad (4.1)$$

The noise in the amplifier, however, is dominated by the thermal noise in the first MOSFET transistor. Therefore, the noise from the LNA can be primarily characterized by equation (3.25) for the drain current noise PSD, which is reproduced below:

$$\overline{I_n^2} = 4kT\gamma g_m. \quad (4.2)$$

The calculation of the noise figure itself follows equations (4.1) and (4.2). Note that we need to estimate the noise figure over the entire bandwidth to ensure that it is reasonable throughout the entire frequency range of interest.

4.2.3 Linearity

Referring to Chapter 3, recall that the linearity of the UWB LNA can be quantified using the input third-order intercept point, IIP_3 :

$$\text{IIP}_3 = \sqrt{\frac{4}{3} \left| \frac{\alpha_1}{\alpha_3} \right|}. \quad (4.3)$$

However, we usually report only the mid-band frequency IIP_3 as the linearity does not vary much over the bandwidth of interest. The mid-band value is therefore, selected to represent the overall linearity of the UWB LNA. For this thesis, the objective is to design the UWB LNA for the range of 3.1-10.6 GHz. Therefore, we will simulate the IIP_3 at 6 GHz, which is approximately the mid-band frequency of the UWB amplifier.

4.2.4 Input and Output Return Loss

From Chapter 3, the input and output return losses can be defined according to the S -parameters S_{11} and S_{22} , respectively. The difference in the case of UWB LNAs is that both S_{11} and S_{22} are required to be low over a wide bandwidth instead of just at a single frequency point. Normally, for a good UWB LNA design, both S_{11} and S_{22} should be below -10 dB over the entire frequency range.

4.3 UWB LNA Topologies

As discussed earlier, LNA designs involve tradeoffs so that we can not achieve high performance for all of the desired characteristics at the same time. As a result, there are several possible ultra-wideband LNA design topologies each with advantages and drawbacks. Therefore, a topology should be selected depending on the specific requirements of the LNA. On occasion, a combination of topologies can also be implemented in order to meet the requirements of an application. In this thesis, our UWB LNA is implemented using inductively source degenerated cascode configuration.

4.3.1 Inductively Source Degenerated UWB LNA

As discussed previously, the inductive source degeneration design is widely used in ultra-wideband low noise amplifier designs as it can achieve relatively good performance through the entire 3.1-10.6 GHz band. Importantly, it does so using a simple circuit structure and it is easy to understand on a theoretical basis.

Referring to Figure 3.3 in Chapter 3 and recalling from equation (3.32), the input impedance can be obtained as:

$$Z_{in} = sL_S + \frac{1}{sC_{gs}} + \frac{g_m L_S}{C_{gs}}, \quad (4.4)$$

where input impedance can be matched to 50Ω ($\frac{g_m L_S}{C_{gs}} = 50\Omega$) without using real resistors. However, unlike narrow-band LNA, a UWB LNA requires the input matching over the entire bandwidth.

One technique used in narrow-band LNAs to act as multi-band LNAs is designed to receive input RF signals at different frequency bands using an inductive source degeneration configuration [35] and input matching LC network. Extending this idea to ultra-wideband designs, we can embed the input network of the amplifier in a multi-section reactive network so that the overall input reactance is resonating over a wider bandwidth [36]. Proper implementation can be adding on LC filter in front of the input matching circuit of the MOS transistor stage with inductive source degeneration feedback, as shown in Figure 4.1.

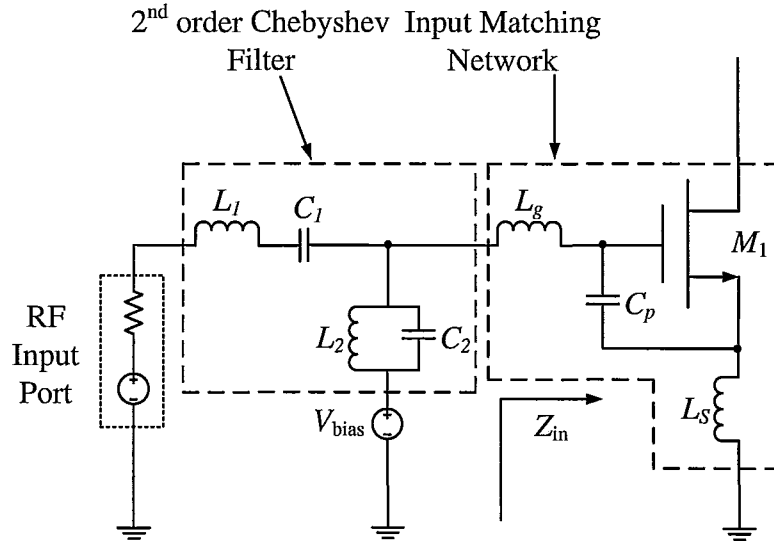


Figure 4.1: Inductive source degeneration technique for UWB LNA.

A three-section Chebyshev Filter is used to control the bandwidth since it can resonate the reactive part of the input impedance over the whole frequency band from 3.1 to 10.6 GHz. An inductor L_g is added at the gate terminal of the input MOSFET device M_1 and a capacitor C_p is added between the gate and the source

terminal of M_1 in order to improve the performance of the input matching network.

4.3.2 Cascode UWB LNA

The cascode LNA configuration, shown in Figure 4.2, can be used to improve the input-output reverse isolation due to high output impedance at the drain terminal of M_1 [37], and thus, increase the stability of the LNA. In addition, the cascode structure has the advantage of having a high gain and a wide bandwidth [38].

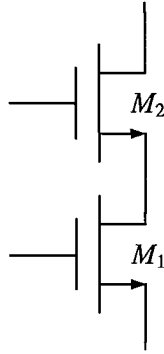


Figure 4.2: Cascode configuration of transistors that replace M_1 in the UWB LNA shown in Figure 4.1.

4.3.3 Feedback UWB LNA

Feedback circuits are widely used in UWB LNA design. The typical design is the resistive shunt feedback as shown in Figure 4.3. This circuit can achieve good wideband input and noise matching at the same time, [39, 40].

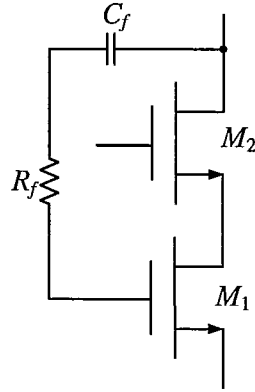


Figure 4.3: Feedback technique for UWB LNA.

4.3.4 Cascade UWB LNA

A high output gain can be achieved by cascading several amplifiers together, as shown in Figure 4.4. The overall gain of the resulting circuit can be expressed as:

$$G_{\text{LNA}} = G_1 \cdot G_2, \quad (4.5)$$

where G_1 is the gain of the first stage implemented with M_1 and G_2 is the gain of the second stage implemented by M_2 . However, this circuit consumes more power, a fact that must be weighed against the constraints of the desired application.

4.3.5 Differential UWB LNA

Normally, the LNA is followed by a mixer stage. Most mixers used in UWB systems are of the double balanced type, having a pair of differential inputs. While a pair of amplifiers designed to work with a differential structures can be used in the front-end as per Figure 4.5, this does increase the overall power consumption

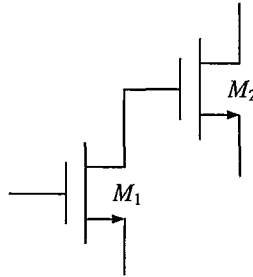


Figure 4.4: The amplifiers in a cascade structure.

of the system.

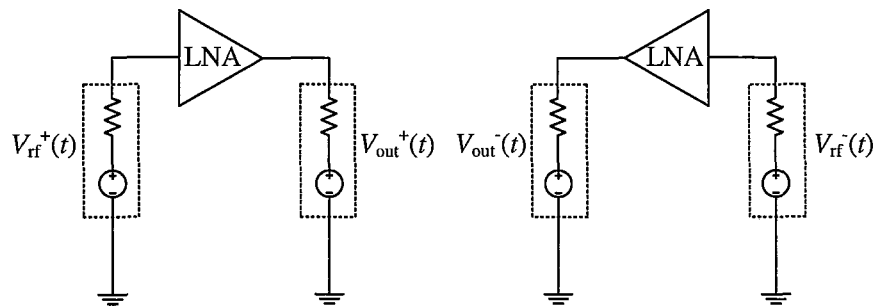


Figure 4.5: Differential UWB LNA configuration.

4.4 UWB LNA Literature Review

Because of a number of design tradeoffs, it is not possible for all of the performance characteristics such as gain, noise figure, linearity, or power dissipation to be simultaneously optimized. If one of the performance goals is optimized, compromises regarding the other characteristics are impossible to avoid. Some published designs may optimize particular aspects of the UWB LNA, while other designs may focus on achieving an overall level of performance for the LNA. Therefore, a

well thoughtout UWB LNA should be designed depending on the demand of the particular application being considered.

In [41–43], the UWB LNA designs focus on minimizing the noise figure. In [42], the LNA is designed using current-reuse configuration and feedback topology for noise cancellation. In [43], feedback topology is also implemented to cancel the total noise current by creating different signs of the noise current into one node. Indeed, applying these techniques can reduce the noise significantly. This is the main advantage of these designs, which is suitable for some ultra-wideband applications. However, some other parameters may be compromised simultaneously such as the gain not being very flat, or the linearity being too low.

Papers [44, 45] focus on the high gain UWB LNA design. Paper [44] shows a two stage cascode structure, which is a combination of cascode and cascade configurations. Clearly, refer to Chapter 4, the gain in this design is very high since a two stage cascade topology is implemented. However, this high gain is achieved at high power consumption.

Paper [46] presents UWB LNA with high linearity. Simultaneously, the gain is reduced since lower gain can definitely provide higher linearity. This design also consumes large DC power. Therefore, the advantage is its high linearity while the disadvantages are the low gain and large power dissipation.

In [47], the focus is on low power UWB LNA design. Obviously, the biasing currents were reduced since the DC currents can not be large if the power consumption needs to be minimized. As a result, the gain can not be high anyhow since lower drain current results in lower g_m according to equation (2.3). Therefore, low power UWB LNA design in [47] has the disadvantage of low gain.

In summary, the designs discussed above have their own advantages and disadvantages. It is obvious that the ultra-wideband LNA design is a decision between all the performance tradeoffs. In other words, the overall performance should be optimized as much as possible in order to design a competitive UWB LNA.

Chapter 5

Narrow-Band Receivers in 0.18- μm CMOS Technology

Considering the issues relating to the design of narrow-band receiver, a significant problem is that the receiver amplifier requires either a differential input, or an on-chip transformer in order to translate the single-ended RF output signal of the LNA into a differential signal pair as the input of the double balanced mixer.

5.1 Receiver Front-End Design

This chapter focuses on the 2.4 GHz receiver front-end design, shown in Figure 5.1. The main novel idea of the design is to use one PMOS and one NMOS instead of two NMOS devices for the RF amplification stage of the double balanced mixer so that the single RF input signal from the LNA can be translated into two differential inputs to the mixer.

The basic properties of this block are as follows:

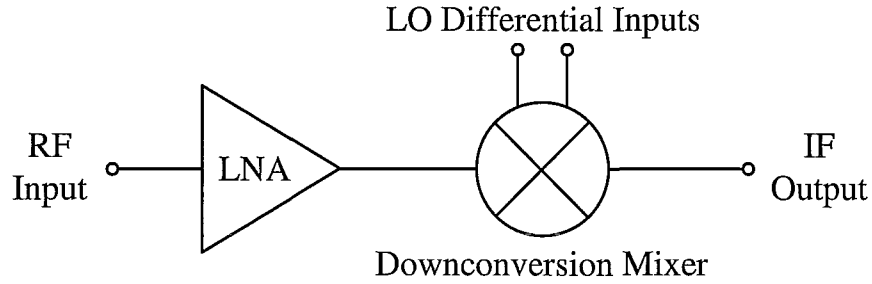


Figure 5.1: Block diagram of designed receiver front-end.

- the RF input frequency is $f_{rf} = 2.4$ GHz with an input power of $P_{rf} = -30$ dBm,
- the LO input frequency is $f_{lo} = 2.1$ GHz with an input power of $P_{lo} = 0$ dBm, and
- the desired IF output frequency is $f_{if} = 300$ MHz.

5.1.1 Design Process of Narrow-Band LNA

The narrow-band LNA was designed as an inductively source degenerated cascade structure, shown in Figure 5.2.

This circuit should be constructed in such a way as to realize the following design objectives:

- to achieve high gain (S_{21}) at 2.4 GHz,
- to achieve low noise figure (NF) at 2.4 GHz,
- to minimize the input return loss (S_{11}) and output return loss (S_{22}) at 2.4 GHz,
- to optimize the linearity (IIP₃), and

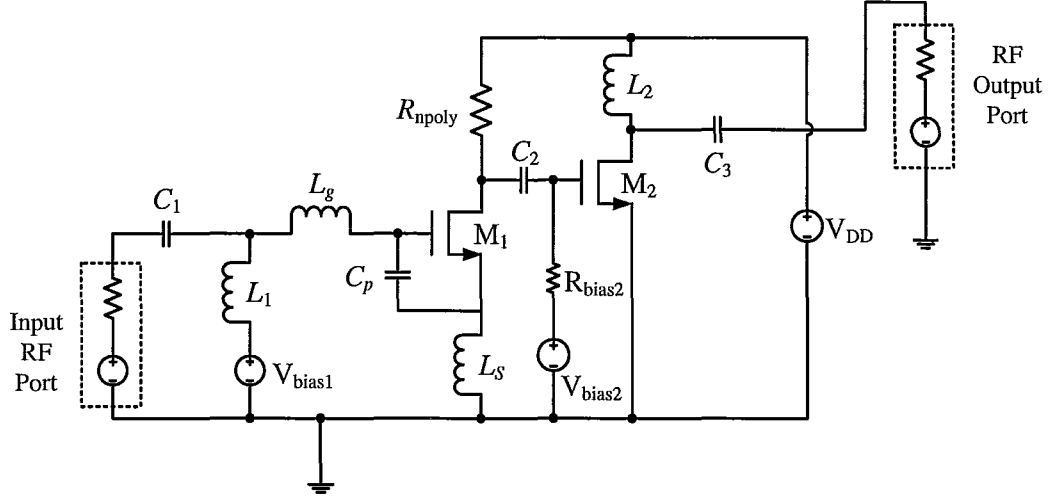


Figure 5.2: Schematic of the inductively source degenerated narrow-band LNA.

- to minimize the power consumption from the given a 1.5 V supply voltage.

In Figure 5.2, the RF signal is provided by the input RF port while the bias voltage is provided by the voltage source (V_{bias1}). The capacitor C_1 is used to block the DC signal and the inductor L_1 is used to block the AC signal. The elements L_g , L_s , C_p , and the NMOS transistor M_1 build the input matching network of the LNA, and its small-signal circuit model is shown in Figure 5.3. Referring to the derivation of equation (3.32) in Chapter 3, the input matching impedance of this amplifier can be expressed as [36]:

$$Z_{in} = \frac{1}{s(C_{gs} + C_p)} + s(L_s + L_g) + \frac{g_m L_s}{C_{gs} + C_p}. \quad (5.1)$$

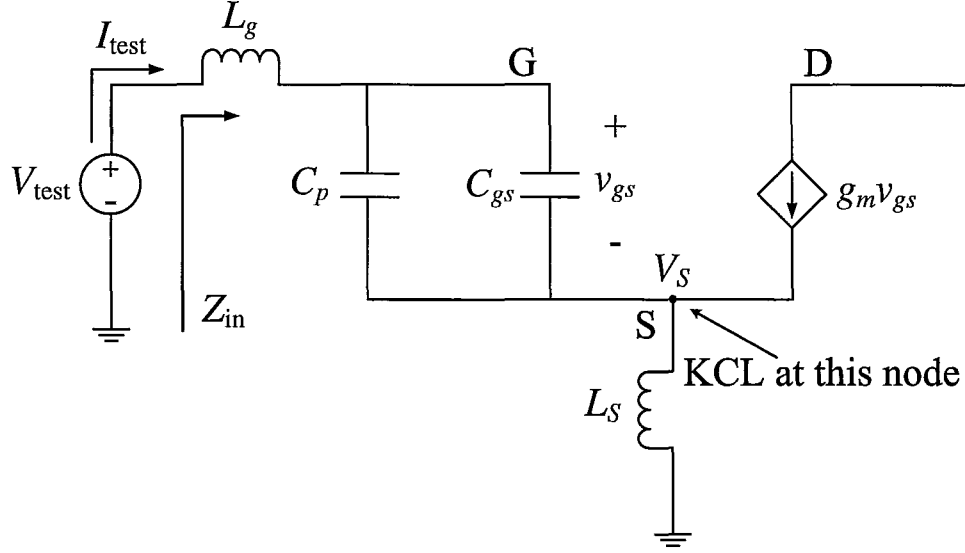


Figure 5.3: Small-signal equivalent input matching network of the inductively source degenerated narrow-band LNA.

Setting the real part of equation (5.1) to be equal to the assumed source resistance of 50Ω , we have:

$$\frac{g_m L_s}{C_{gs} + C_p} = Z_S = 50, \quad (5.2)$$

where the input matching is realized for $f = 2.4 \text{ GHz}$.

The RF signal enters the second NMOS transistor stage and will be amplified again due to the function of the cascade structure. The voltage source of V_{bias2} is used to provide the bias voltage of the NMOS transistor (M_2) while the capacitors C_1 and C_2 are designed to block DC signals. The inductor L_2 and resistor R_{npoly} are used for matching.

The output matching is not very important since usually the front-end amplifier is followed by the mixer stage. For measurement purposes, it is usual to use an

output buffer rather than a matching network.

From Chapter 3, the gain of the LNA can be measured for S_{21} and is:

$$G_{dB} = 20 \log(|S_{21}|). \quad (5.3)$$

Also from Chapter 3, the input return loss is defined as S_{11} while the output return loss is defined as S_{22} . Both S_{11} and S_{22} should be under -10 dB, if good LNA performance is to be achieved.

5.1.2 Design Process of Downconversion Double Balanced Mixer

In order to overcome the difficulties associated with the required differential input for the double balanced mixer, a novel design idea is introduced so that a single RF input signal can be translated into two differential signals in the mixer, shown in Figure 5.4. This modified double balanced mixer requires only a single RF output signal from the low-noise amplifier (LNA) without on-chip transformer.

In Figure 5.4, transistors M_3 and M_4 are used to transform the input RF voltage signal into the current signal. Transistors M_5 , M_6 , M_7 , and M_8 , are designed to perform the mixing stage and produce the converted intermediate frequency (IF) output, where the theory of this conversion has been discussed in Chapter 3. Then the mixer will produce a differential output.

The novel idea of this design is that an NMOS-PMOS pair is implemented as the RF input amplification stage, shown as M_3 and M_4 transistor pair in Figure 5.4, rather than using a conventional NMOS-NMOS differential configuration. Normally, in a standard double balanced mixer, the function of these two transistors

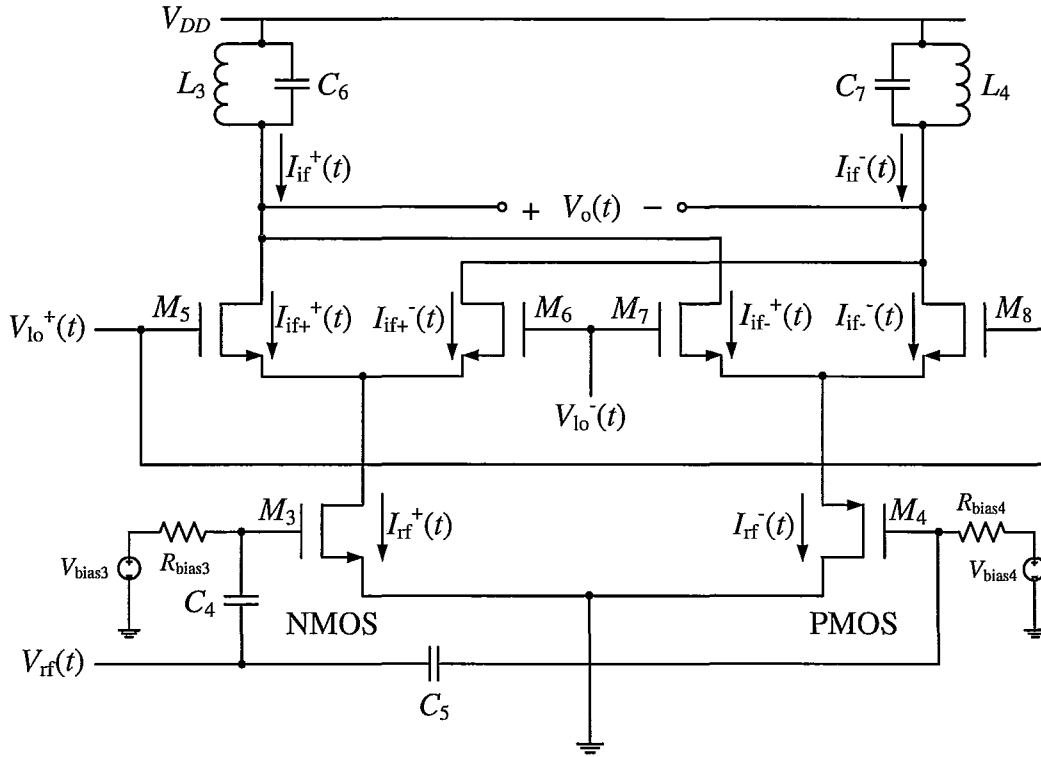


Figure 5.4: Schematic of the modified double balanced mixer.

is to translate the differential RF input voltage signals into the differential current signals, a process called V - I conversion. Typically, this stage also performs amplification as well. In the new design, the NMOS-PMOS pair not only performs V - I conversion and amplification, but can also translate the single-ended RF input into a differential signal pair.

The importance of this NMOS-PMOS pair is that it can create a differential current in two branches of the circuit. Recall from equation (2.2), that the current

of an NMOS in saturation region is:

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2. \quad (5.4)$$

Note that both M_3 (NMOS) and M_4 (PMOS) in Figure 5.4 work in saturation region. As shown Figure 5.4, when V_{rf} increases, V_{GS} of the NMOS (M_3) also increases. Equation (5.4) shows that when V_{GS} is also increasing, $(V_{GS} - V_t)^2$ is increasing, which means that the current I_D is also increasing. On the other hand, when V_{GS} is decreasing, the current I_D is decreasing. Therefore, when V_{rf} increases, the voltage V_{GS} of NMOS increases, resulting in an increasing I_D . The converse is also true. This means that when the sinusoidal RF input signal is on the increasing half-cycle (V_{rf} increasing), the current of this NMOS branch is increasing, and when the RF signal is on the decreasing half-cycle, the current is decreasing.

Recall from equation (2.13), that the current of a PMOS transistor in the saturation region is:

$$I_D = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} (V_{GS} - V_t)^2. \quad (5.5)$$

Equation (5.5) shows that when V_{GS} of the PMOS (M_4) is increasing, $(V_{GS} - V_t)^2$ is increasing, which in turn means that the current I_D is also increasing. On the other hand, when V_{GS} is decreasing, the current I_D is decreasing which is exactly the same pattern for the NMOS device. However, from Figure 5.4, when V_{rf} increases, V_{GS} of PMOS (M_4) decreases, leading I_D to decrease, because the voltage at the source terminal of PMOS is now larger than the voltage at the gate terminal. On the other hand, when V_{rf} decreases, V_{GS} increases and I_D increases as well. Therefore, when the sinusoidal RF input signal is on the increasing half-cycle, the current of

this PMOS branch is decreasing while the RF signal is on the decreasing cycle, the current of this PMOS branch increases. This V - I pattern is the exact opposite of the one in NMOS branch.

The overall V - I conversion can be summarized as follows:

- when the RF input signal is increasing, the current in the NMOS branch is increasing while the current in the PMOS branch is decreasing, and
- when the RF input signal is decreasing, the current in the NMOS branch is decreasing while the current in the PMOS branch is increasing.

Therefore, these two opposite currents create a differential signal pair, as shown in Figure 5.5. Thus the pair translates the single-ended RF input signal into a differential signal pair.

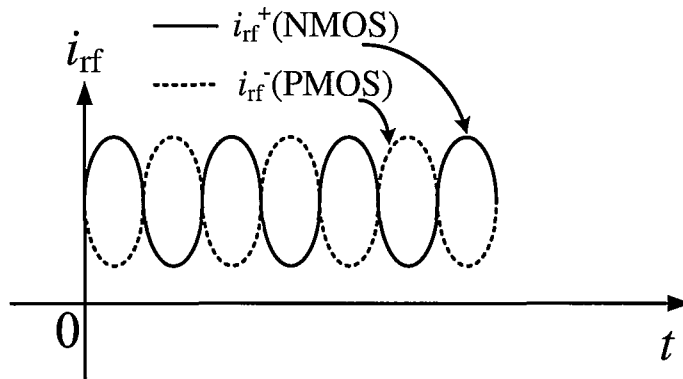


Figure 5.5: Ideal differential current signals of NMOS and PMOS branches.

Following the amplification stage, the modified double balanced mixer must be designed so as to meet the following performance objectives in addition to achieving its primary task:

- to achieve high conversion gain (G_c) at the IF output,
- to achieve a low noise figure (NF) at the IF output,
- to optimize the linearity (IIP₃),
- to minimize the RF and LO feedthroughs, and
- to minimize the power consumption given 1.5 V supply voltage.

Recall from equation (3.86) in Chapter 3, that the gain of double balanced mixer can be expressed as:

$$G_c = \frac{4g_m R_L}{\pi}. \quad (5.6)$$

Ideally, g_m and R_L alone affect the conversion gain. However, in reality, the gain will be affected by various other factors such as imperfect switching, RF cable loss, etc. Equation (5.6) shows that if transconductance g_m increases, then the gain also increases. This also means that the current i_D of the MOSFET also increases which results in increased power consumption by the device. Increasing the other parameter R_L will also increase the gain, but at the cost of increasing the level of noise added by the resistor.

5.1.3 Design Process of Receiver Front-End

The 2.4-GHz receiver in this design includes an low-noise amplifier (LNA) and a downconversion double balanced mixer, shown in Figure 5.6, where an output buffer is added for measurements.

The overall performance of the receiver should meet the following objectives:

- high gain at the IF output,

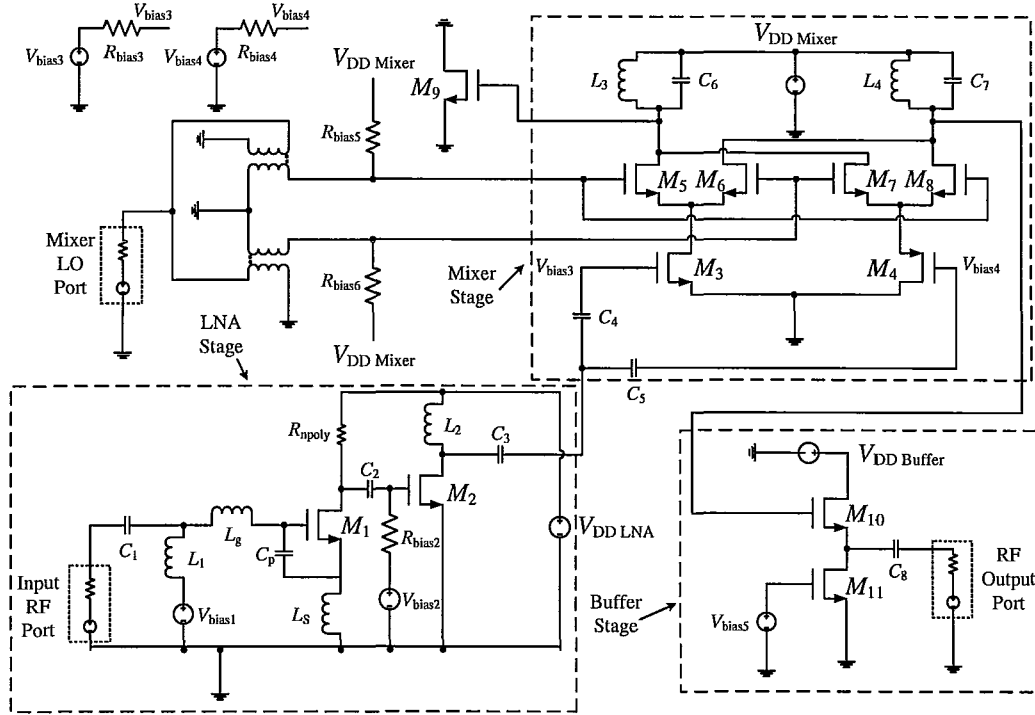


Figure 5.6: Circuit schematic of the receiver.

- low noise figure (NF) at the IF output,
- good linearity (IIP_3), and
- low power consumption given a 1.5 V supply voltage.

As we have already designed the 2.4 GHz narrow-band LNA and the down-conversion double balanced mixer, the overall performance can be obtained by considering the receiver as a two stage cascaded circuit with the first stage as the LNA and second stage as the mixer. With this structure, it is easy to obtain the overall performance figures.

The total gain of the receiver is:

$$G_{\text{receiver}} = G_{\text{amplifier}} \cdot G_{\text{mixer}}. \quad (5.7)$$

where G_{receiver} is the gain of the receiver, $G_{\text{amplifier}}$ is the gain of the LNA, and G_{mixer} is the conversion gain of the mixer. The overall noise figure of the receiver can be obtained from equation (2.39), which in this case can be expressed as:

$$\text{NF}_{\text{receiver}} = \text{NF}_{\text{amplifier}} + \frac{\text{NF}_{\text{mixer}} - 1}{G_{\text{receiver}}}. \quad (5.8)$$

where $\text{NF}_{\text{receiver}}$ is the noise figure of the receiver, $\text{NF}_{\text{amplifier}}$ is the noise figure of the LNA, and NF_{mixer} is the noise figure of the mixer. The overall IIP_3 of the receiver can be obtained from equation (2.48) which results in:

$$\frac{1}{\text{IIP}_{3,\text{receiver}}} \approx \frac{1}{\text{IIP}_{3,\text{amplifier}}} + \frac{G_{\text{amplifier}}}{\text{IIP}_{3,\text{mixer}}}. \quad (5.9)$$

where $\text{IIP}_{3,\text{receiver}}$ is the linearity of the receiver, $\text{IIP}_{3,\text{amplifier}}$ is the linearity of the LNA, and $\text{IIP}_{3,\text{mixer}}$ is the linearity of the mixer. The total power dissipation is:

$$\text{without output buffer} : P_{\text{receiver}} = P_{\text{amplifier}} + P_{\text{mixer}}, \quad (5.10)$$

$$\text{with output buffer} : P_{\text{receiver}} = P_{\text{amplifier}} + P_{\text{mixer}} + P_{\text{buffer}}. \quad (5.11)$$

where P_{receiver} is the power consumption of the receiver, $P_{\text{amplifier}}$ is the power consumption of the LNA, P_{mixer} is the power consumption of the mixer, and P_{buffer} is the power consumption of the buffer.

5.2 Circuit Implementation of Receiver Front-End

The design for the receiver front-end is fabricated in TSMC 0.18- μm CMOS Technology. The narrow-band low-noise amplifier is implemented using an inductively source degenerated cascade structure and the downconversion mixer is implemented according to double balanced configuration with complementary PMOS and NMOS transistors for the RF signal (path).

In the circuit diagram shown in Figure 5.6, the first stage including M_1 and M_2 is the 2.4 GHz inductively source degenerated cascade narrow-band LNA. The second stage including $M_3 - M_8$ is the downconversion double balanced mixer stage. The third stage including M_{10} and M_{11} is the output buffer stage for measurement purpose.

In 0.18- μm CMOS technology in the Cadence software, the width of the MOSFET transistor is fixed as 2.5 μm , and the finger length is 0.18 μm . As a result, the only method to control the transistor size is to change the parameter called number of fingers. This parameter together with bias voltages can be used to generate proper g_m of the MOSFET. And according to the simulator, the values of number of fingers for all the transistors are shown in Table 5.1.

The theory and function of the LNA and Mixer stage has been discussed before. In order to perform the function in each stage, all the MOSFET transistors should be biased properly. Therefore, the biasing voltages in this receiver design are 0.6 V. In addition, the voltage supplies for all the stages are 1.5 V.

For testing purpose, a dummy load is typically used in order to simulate as

standard electric load. M_9 is used as a dummy load. This is for reasons of symmetry, as a single-ended output is used for the purpose of experimental measurements.

The overall system design parameters are listed in Table 5.1, where the finger width is $2.5 \mu\text{m}$ and the finger length is $0.18 \mu\text{m}$ for all MOSFET transistors.

M_1	Number of Fingers = 15
M_2	Number of Fingers = 10
M_3	Number of Fingers = 50
M_4	Number of Fingers = 110
$M_5 - M_8$	Number of Fingers = 12
$M_9 - M_{11}$	Number of Fingers = 100
RF Input Power	-30 dBm @ 2.4 GHz
LO Input Power	0 dBm @ 2.1 GHz
DC Bias Voltages	0.6 V
DC Supply Voltage	1.5 V

Table 5.1: Narrow-band receiver design parameters.

The layout of the receiver circuit as designed in the Cadence software suite is shown in Figure 5.7, and a photomicrograph of the physically implemented version is shown in Figure 5.8.

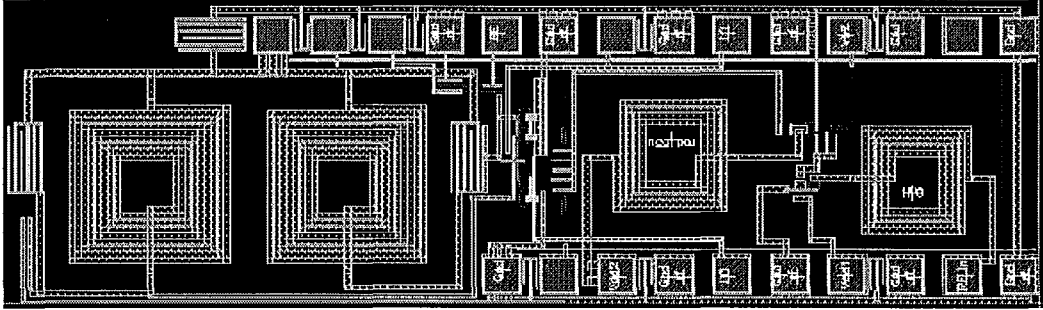


Figure 5.7: Physical layout of narrow-band receiver.

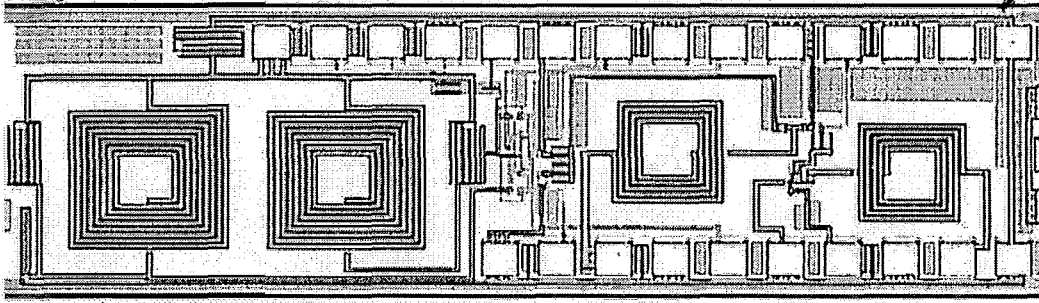


Figure 5.8: Photomicrograph of narrow-band receiver.

5.3 Simulation Results

The simulations were run in the Cadence software suite using the Spectre RF simulator package. A $0.18\ \mu\text{m}$ CMOS process was used with device models provided by CMC Microsystems. The simulator includes the narrow-band LNA as well as the double balanced mixer.

The output of the receiver is simulated using Transient (TRAN) analysis. Figure 5.9 shows the simulation results for an IF output signal appearing at 300 MHz with a power amplitude of -14.68 dBm. The LO feedthrough appears at 2.1 GHz with -47.0 dBm power amplitude, and the RF feedthrough appears at 2.4 GHz with a power of -47.61 dBm. Note that the LO and RF feedthroughs have significantly lower amplitudes compared to the desired IF output. As mentioned before, the RF input power is -30 dBm and therefore, the gain is $-14.68 - (-30) = 15.32\ \text{dBm}$. Refer to the schematic of the receiver in Figure 5.6, the results simulated here are single-ended in order to compare them to the measurement results.

The total gain of the receiver unit is simulated using both Periodic Steady-State

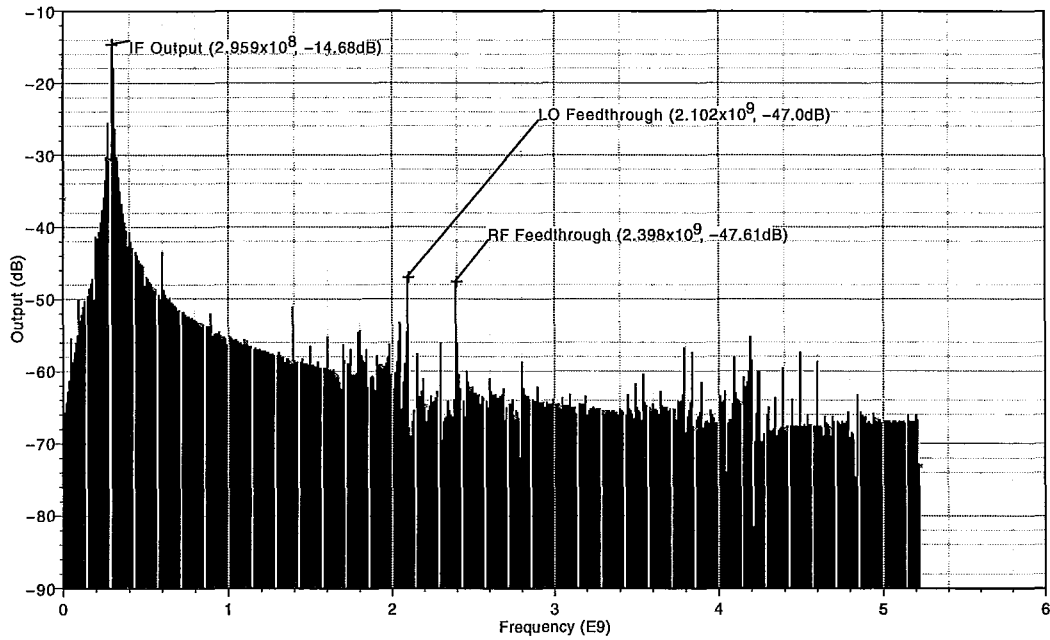


Figure 5.9: The output of narrow-band receiver.

(PSS) analysis and Periodic Transfer Function (PXF) analysis as provided in Cadence software. Figure 5.10 shows the gain of the receiver circuit at different frequencies. In our design, the RF input frequency is 2.4 GHz, and therefore, the proper value of the gain should be obtained at this frequency. As marked, the simulated gain is 18.2dB at 2.4 GHz (input frequency). Note that this result is obtained from the differential output of double balanced mixer. From theory in Chapter 3, equations (3.79), (3.80), and (3.81) can be used to show that if the output is single-ended, the output power amplitude is half of the differential output power amplitude, which implies the single-ended output power is 3 dB less than the differential output power. Therefore, the gain is also 3 dB less. If we compare

this differential gain to the single-ended one that we simulated previously, the differential gain is 18.2 dB and the single-ended gain is 15.32 dB. This verified that the differential gain is 3 dB higher than the single-ended value. We will choose 15.32 dB as our simulated gain in order to compare to the experimental result.

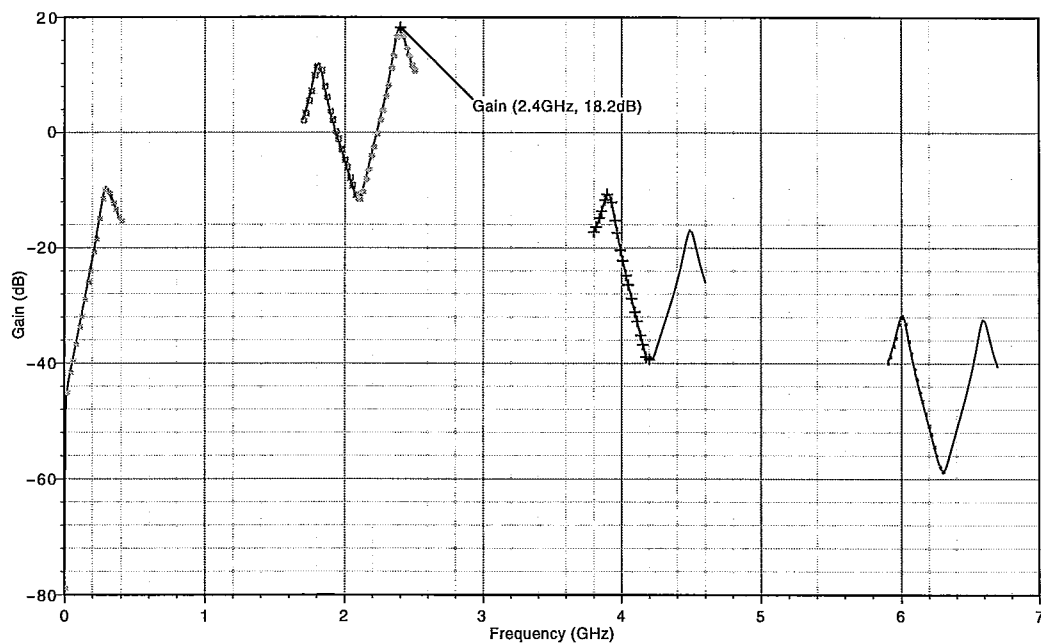


Figure 5.10: The gain of narrow-band receiver.

The overall noise figure (NF) of the receiver is calculated using both Periodic Steady-State (PSS) analysis and Periodic Noise (PNoise) analysis. Figure 5.11 shows the noise figure of the circuit. Because the IF output signal is centered at 300 MHz, this is also the frequency at which I measured the noise figure. As marked, the simulated NF is 9.99dB at the IF output frequency, 300MHz.

The IIP3 of the receiver is simulated using swept PSS followed by Periodic AC (PAC) analysis, as shown in Figure 5.12. As described in Chapter 2, a "two-tone"

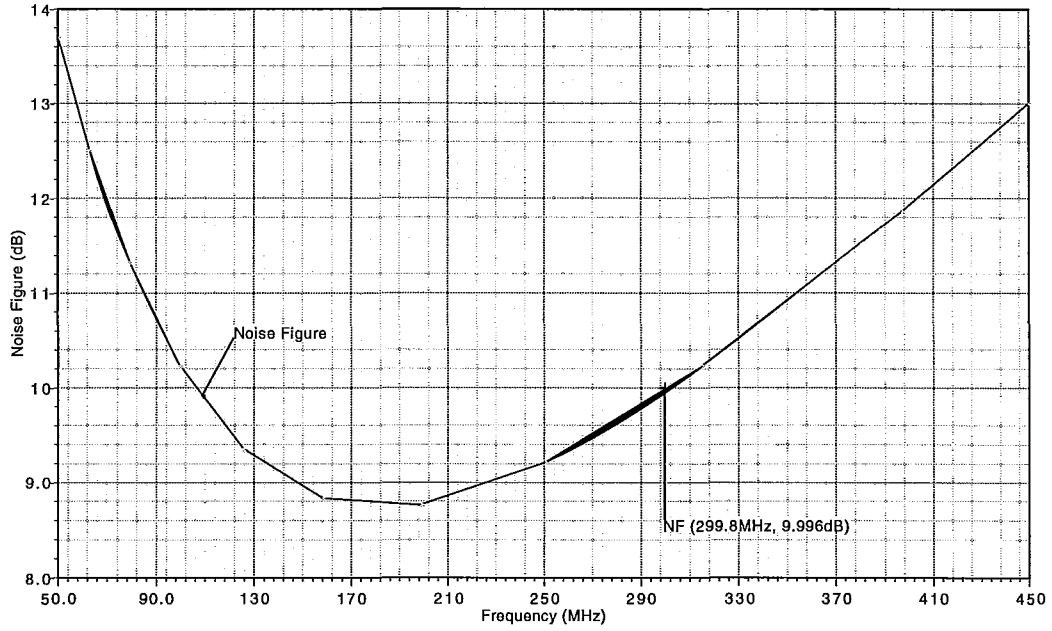


Figure 5.11: The noise figure of narrow-band receiver.

test should be applied to evaluate IIP_3 . In the simulation, a second RF input was applied at $f_{rf2} = 2.375$ GHz with the same input power as the desired signal component at $f_{rf1} = 2.4$ GHz. Note that we use f_{rf1} to denote f_{rf} for the sake of simplicity in this two tone test. The first order terms of interest will be at:

$$\begin{aligned} f_{if1} &= f_{rf1} - f_{lo} = 2.4 \text{ GHz} - 2.1 \text{ GHz} = 300 \text{ MHz, and} \\ f_{if2} &= f_{rf2} - f_{lo} = 2.375 \text{ GHz} - 2.1 \text{ GHz} = 275 \text{ MHz.} \end{aligned} \quad (5.12)$$

From equation (2.43), the third order terms of interest can also be obtained as:

$$\begin{aligned} 2f_{if1} - f_{if2} &= 2 \times 300 \text{ MHz} - 275 \text{ MHz} = 325 \text{ MHz, and} \\ 2f_{if2} - f_{if1} &= 2 \times 275 \text{ MHz} - 300 \text{ MHz} = 250 \text{ MHz.} \end{aligned} \quad (5.13)$$

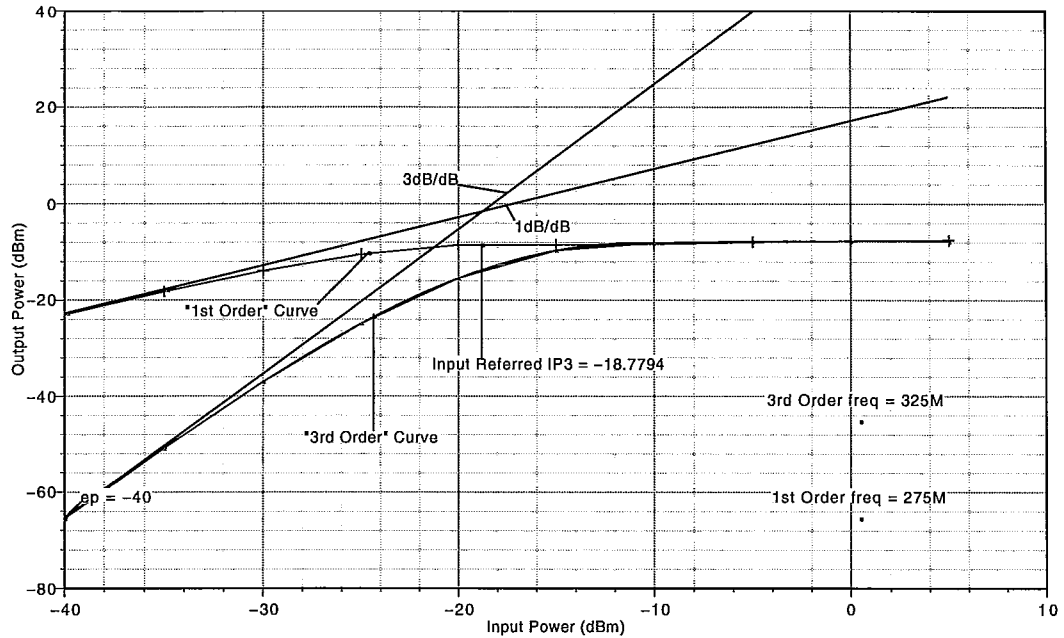


Figure 5.12: IIP_3 of narrow-band receiver.

Using the Cadence simulation, the first-order term was chosen to be the 275 MHz component, and the third-order term was chosen to be the 325 MHz component. The simulated IIP_3 was marked and the value was found to be -18.78 dBm.

The power consumption was simulated using DC analysis for a 1.5 V supply for the receiver circuit. The DC current for the narrow-band LNA is 1.322 mA which implies the power dissipation of the narrow-band LNA was found to be 1.983 mW, and the DC current of the mixer was 2.393 mA, which implies the power dissipation of this unit is 3.590 mW. In addition, the DC current of the output buffer is 4.308 mA, which means that the power dissipation of the output buffer is 6.462 mW. Therefore, the overall power consumption of the receiver front-end is 5.573 mW without the output buffer and 12.035 mW with the output buffer. The total

designed chip area is $2.7 \times 0.77 = 2.08 \text{ mm}^2$. The summary of the overall simulation results is listed in Table 5.2.

Technology	0.18 μm CMOS
Input frequency	2.4 GHz
Gain (differential)	18.2 dB
Gain (single-ended)	15.3 dB
NF	10 dB
IIP ₃	-18.8 dBm
Power dissipation (without buffer)	5.57 mW
Power dissipation (with buffer)	12.0 mW
Chip area	2.08 mm^2

Table 5.2: Simulation results of the narrow-band receiver performance.

5.4 Measured Performance

In addition to simulations, the performance of the fabricated receiver circuit, as shown in Figure 5.8, was also measured in the laboratory. The experimental setup, equipment, and measurement procedures are discussed in Appendix A. First of all, we will monitor the DC currents in all the stages including LNA, Mixer, Buffer stages by Semiconductor Parameter Analyzer and ensure that the DC currents are reasonable before measuring any values. Then we will start measure the receiver circuit, where the measured results and comparison to the simulated results are demonstrated here.

The measured output of the receiver circuit, shown in Figure 5.13, is the original result obtained from the Spectrum Analyzer. In order to analyze and show the output result clearly, we export the data from the Spectrum Analyzer to Microsoft

Office Excel and graph the output, shown in Figure 5.14.

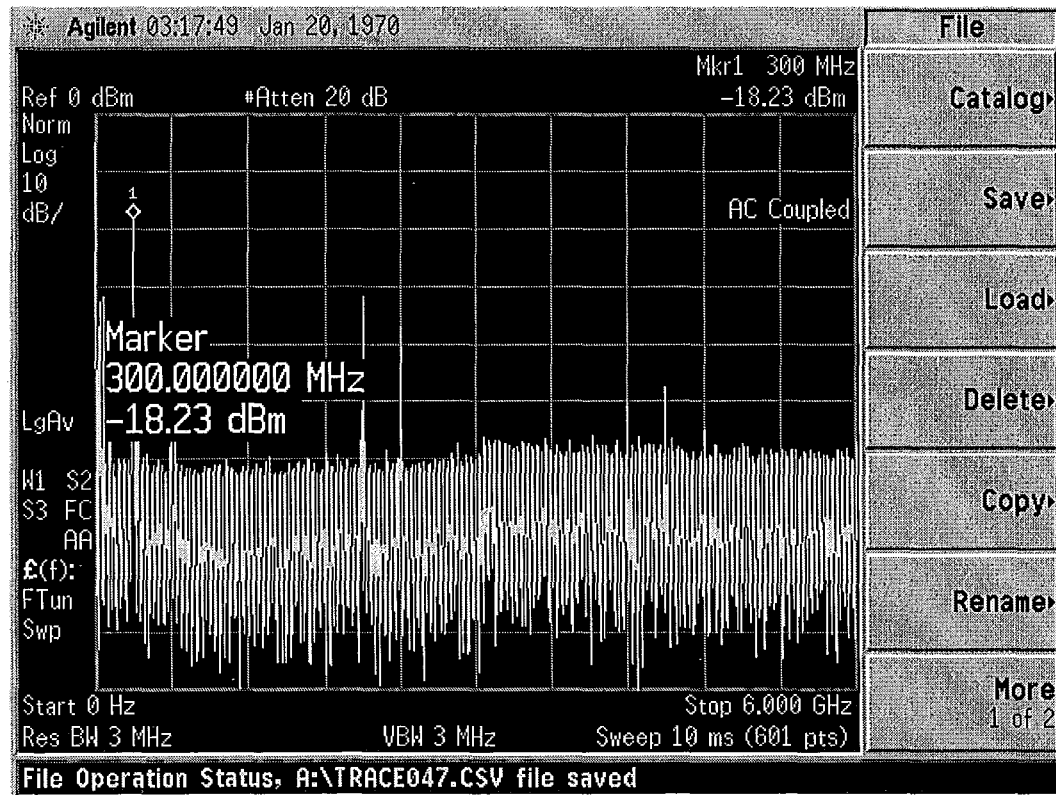


Figure 5.13: Measured output of narrow-band receiver from the spectrum analyzer.

All values of the receiver input parameters are obtained from Table 5.1, in which the input RF power is -30 dBm at 2.4 GHz and the input LO power is 0 dBm at 2.1 GHz. The output result in Figure 5.14 shows that the desired IF output power is -18.2 dBm. Note that as we discussed in Appendix A, the input losses can be easily compensated while the output losses can only be compensated manually, which implies we need to add the loss in our output. Using the method described in Appendix A, the RF cable loss at 300 MHz as measured at the output port was found to be about 1.5 dB. Hence, the actual output IF power should

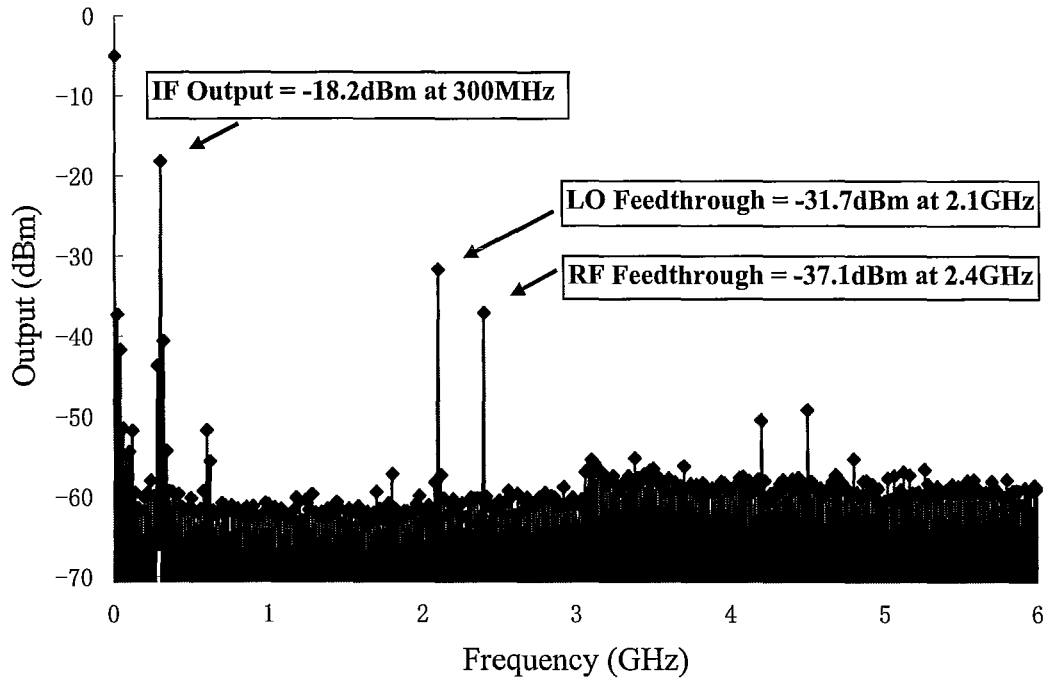


Figure 5.14: Measured output of narrow-band receiver from the output data at $P_{in} = -30$ dBm.

be $-18.2 + 1.5 = -16.7$ dB. Therefore, the measured gain of the receiver circuit is in fact $-16.7 - (-30) = 13.3$ dB. By comparison, the simulated gain value was 15.32 dB which indicates that the measured gain was about 2 dB lower. However, the losses from the RF cables, laboratory facilities, pins or pad contacts may not have been compensated accurately, a fact which will affect the measured output values. Therefore, a 2 dB difference is acceptable as a measured result. In addition, the overall gain (13.3 dB) of the receiver is measured from single-end. As we discussed before, it is 3 dB lower than the gain measured from differential pair, which implies that the gain should be $13.3 + 3 = 16.3$ dB if differential output is selected.

The measured noise figure of the fabricated receiver circuit is shown in Figure

5.15. As marked, the measured NF at 300 MHz (IF output frequency) is 11.5 dB, and the simulated value is 10 dB. This indicates that the experimental noise figure is 1.5 dB higher than the simulated one which is acceptable considering the loss of 1.5 dB in the cables and that the uncertainties in the behavior of real equipment and components may affect the measurements.

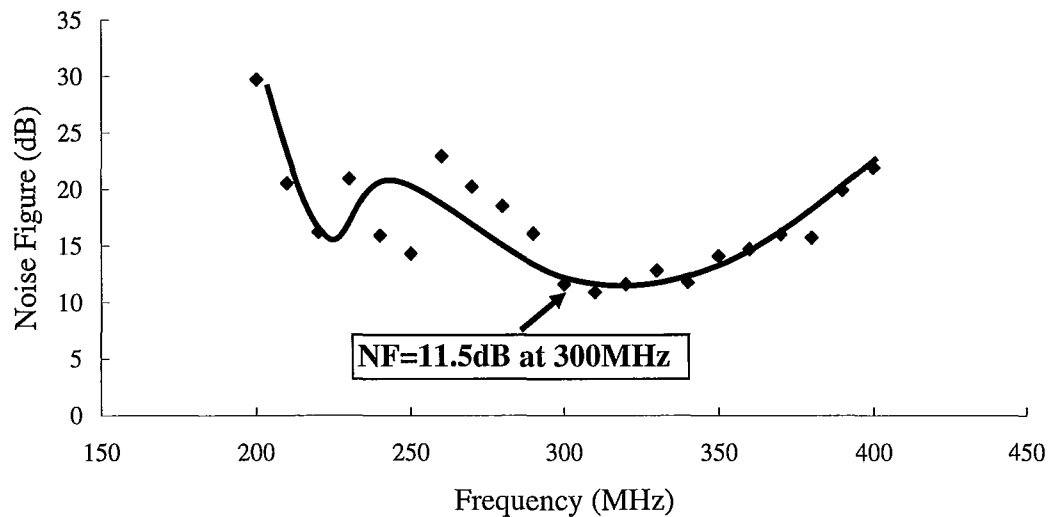


Figure 5.15: Measured noise figure of narrow-band receiver.

The measured IIP_3 is shown in Figure 5.16. This parameter value was measured as -19 dBm, while the simulation predicted a value of -18.8 dBm. This is a reasonable result given how close the measured value is to what was predicted by the theoretical analysis.

Figure 5.14 indicates that the LO feedthrough is -31.7 dBm at 2.1 GHz and the RF feedthrough is -37.1 dBm at 2.4 GHz. These are values well below the IF output signal power as desired. Furthermore, refer to the theory in Chapter 3, the feedthroughs can be significantly improved if differential outputs are taken.

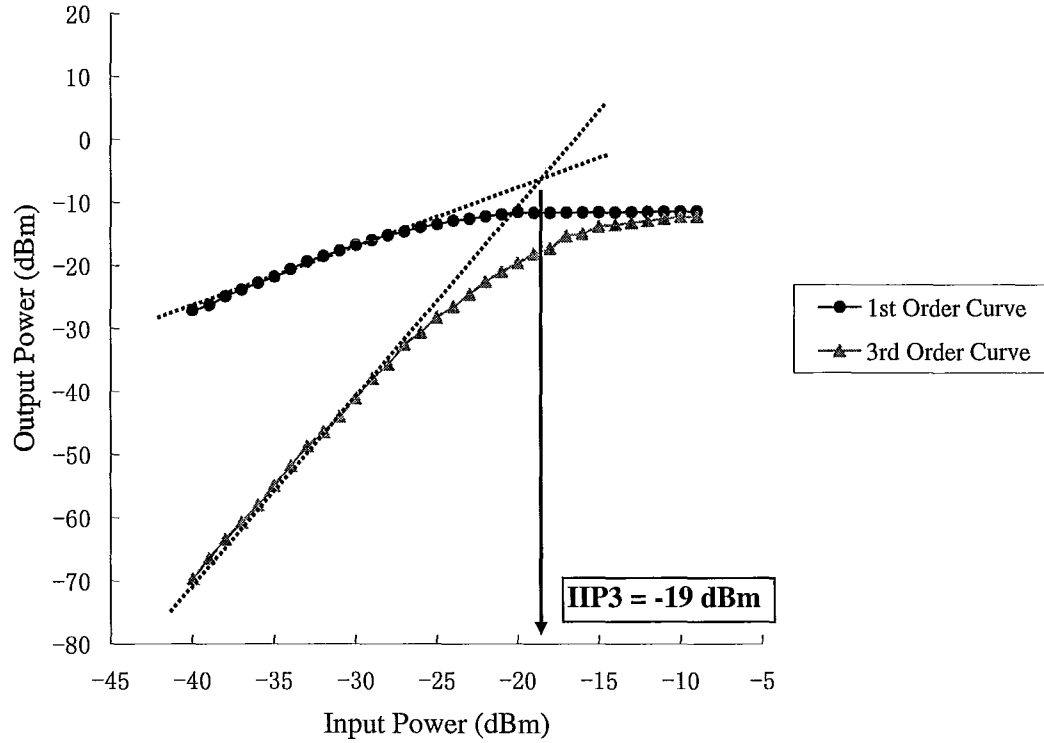


Figure 5.16: Measured IIP_3 of narrow-band receiver.

The supply voltage is 1.5 V. The measured DC currents are 1.22 mA for the amplifier stage, 3.27 mA for the mixer, and 4.07 mA for the output buffer. Therefore, the power consumption of each stage is 1.83 mW, 4.91 mW, and 6.11 mW. The overall power consumption of the receiver front-end is 6.74 mW without the output buffer and 12.85 mW with the output buffer. A summary of both the simulated and measured results is listed in Table 5.3.

	Simulated	Measured
Technology	0.18 μm CMOS	0.18 μm CMOS
Input frequency	2.4 GHz	2.4 GHz
Gain (differential)	18.2 dB	16.3 dB
Gain (single-ended)	15.3 dB	13.3 dB
NF	10 dB	11.5 dB
IIP ₃	-18.8 dBm	-19 dBm
Power dissipation (without buffer)	5.57 mW	6.74 mW
Power dissipation (with buffer)	12.0 mW	12.85 mW
Chip area	2.08 mm ²	2.08 mm ²

Table 5.3: Measured performance of the narrow-band receiver.

5.5 Comparison and Discussion

In order to compare the results with existing published works, a performance metric must be selected that accounts for all the performance parameters under discussion. Such quantity is called a figure of merit (FoM), and it is defined as:

$$\text{FoM} = 20 \log(f_{\text{RF}}) + G + \text{IIP}_3 - \text{NF} - 10 \log(P_{\text{diss}}), \quad (5.14)$$

where all values are measured in normalized units. The term f_{RF} is the input frequency of the RF signal in Hz normalized to 1 Hz, G is the gain of the receiver in dB normalized to 1 dB, IIP_3 is the linearity in dBm normalized to 1 dBm, NF is the noise figure in dB normalized to 1 dB, and P_{diss} is the power consumption of the receiver circuit in mW normalized to 1 mW. Note that FoM is only a value that estimates the overall performance of the circuit. As long as each individual term is calculated in the same metric, the differences among each FoM remain the same since. Therefore, the FoM is only a rough value for the purpose of comparison and

the unit is not strictly defined.

Table 5.4 shows both the simulated and measured results of our receiver design as well as comparisons with other recently published work. From Table 5.4, it is clear that the FoM of the proposed receiver is neither the best nor the worst. It is essentially average in terms of performance, and it is quite acceptable for practice. This is because the proposed design has its advantages. Note that the form of the NF we used here is SSB noise figure, which is usually 3dB higher than the DSB noise figure. In practice, the SSB noise figure should be reported in preference to the DSB NF, as it is a more meaningful metric.

	Tech. (μm)	Input Freq. (GHz)	Gain (dB)	NF (dB)	IIP ₃ (dBm)	P _{diss} (mW)	Chip Area (mm ²)	FoM
Simulated	0.18	2.4	18.2	10	-18.8	5.57	2.08	170
Measured	0.18	2.4	16.3	11.5	-19	6.74	2.08	165
[48]	0.09	2.4	30	18	-22	8.5	3.4	168
[49]	0.18	2.44	8	8.9	-13.5	2.754	N/A	169
[50]	0.25	2.4	14.5	4.8	-18	11.3	1.82	169
[51]	0.13	2.4	12.5	28	-21	3.4	3.3	146
[52]	0.18	2.4	23	9	-15	4.8	1.6	180
[53]	0.18	2.4	21.4	13.9	-18	6.5	N/A	169
[54]	0.18	2.4	20.4	19	N/A	0.5	0.765	N/A

Table 5.4: Comparison to other Narrow-Band Receiver Performances.

Because the standard RF input is single-ended, the receiver front-end usually requires either a pair of differential inputs to the LNA, or an on-chip transformer to create the inputs for the double balanced mixer. However, the on-chip transformer is relatively hard to realize, requires more circuit area, and has a power consumption. It also degrades the circuit performance. Therefore, the benefit of

our receiver design is that it requires only a single RF input signal to provide an output IF signal. No on-chip transformer is needed, which means that the single RF output signal can be translated into a differential signal pair without adding any elements in the circuit.

Overall, as a receiver, our design has the following advantages:

- requires a single-ended RF input without a need of using on-chip transformer,
- a simple circuit architecture that eases the process of fabrication,
- relatively low power consumption, and
- competitive overall performance compared to other designs

However, there are tradeoffs involved in this receiver design. Because we translate the single-ended RF signal to a set of differential signals, we use a PMOS-NMOS transistor pair, instead of NMOS differential pair. The mobility of PMOS transistor is smaller than the mobility of NMOS transistor. Therefore, the PMOS transistor normally is larger in size and switches more slowly than the NMOS transistor, a phenomenon that creates an imperfect phase relationship between the two differential signals at the output of the PMOS-NMOS pair. In addition, the current amplitude of the PMOS branch is not symmetrical with the NMOS branch due to the difference in mobility. This may degrade the performance of the mixer if the bias is not tuned precisely. Depending on what we have simulated and measured, our receiver works as a normal one and this issue could be solved in the future since we know the mobility of MOSFETS depends on process-technology from Chapter 2.

Chapter 6

UWB LNA in 0.13- μm CMOS Technology

Considering the issues discussed before in Chapter 4, this chapter will focus on low-power consumption design in biomedical application while optimizing other performance characteristics at competitive levels of the ultra-wide band (UWB) low-noise amplifier (LNA).

Based on [36], a simple structure of inductively source degenerated cascode UWB LNA is introduced. The inductive source degeneration cascode circuit was introduced earlier as a possible candidate architecture for a UWB LNA design. However, unlike the original version described in [36], the biasing voltage of the second MOSFET transistor is connected to supply voltage instead of to another biasing voltage. The output buffer is implemented in on-chip instead of using a DC current source, another MOSFET transistor is substituted in.

In a real circuit, the bias voltage input will affect the performance of the RF circuit. We should, therefore, attempt to minimize the number of bias voltages

inputs in order to obtain better performance. Therefore, our UWB LNA design only involves one off-chip biasing voltage, which is connected to the first MOSFET transistor.

6.1 Design Process and Theory of UWB LNA

The UWB LNA design in this thesis, shown in Figure 6.1, applies the inductive source degeneration technique in a cascode structure. This configuration is very simple, yet still yields good performance.

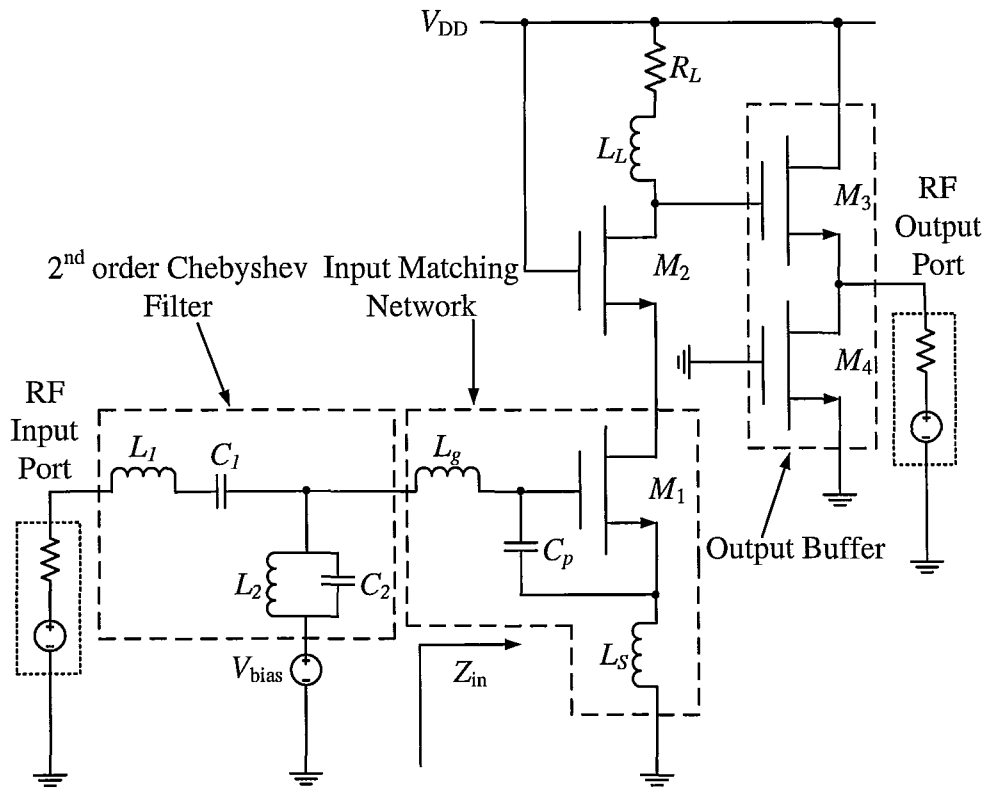


Figure 6.1: Circuit schematic of ultra-wideband low-noise amplifier.

The ultra-wideband low-noise amplifier design should optimize the overall performance according to the following criteria:

- wide bandwidth from 3.1 to 10.6 GHz (7.5 GHz frequency range),
- high and flat gain through 3.1-10.6 GHz bandwidth,
- low noise figure over the entire bandwidth,
- high linearity through the entire bandwidth,
- low input and output return loss through the whole bandwidth, and
- low DC power consumption.

In the circuit schematic shown in Figure 6.1, the input matching network is similar to that used for narrow-band amplifier designed in Chapter 5. The small-signal equivalent circuit of the matching network can be obtained from Figure 5.3 and refer to equation (5.1). The input impedance for the matching network of the amplifier is:

$$Z_{in} = \frac{1}{s(C_{gs} + C_p)} + s(L_s + L_g) + \frac{g_m L_s}{C_{gs} + C_p}. \quad (6.1)$$

This network is designed to ensure the real part of the input impedance $R_{in} = \frac{g_m L_s}{C_{gs} + C_p} = 50 \Omega$.

In order to extend this technique to the ultra-wideband LNA, we need to add the input matching network to two filter sections to form a three-section Chebyshev filter as shown in Figure 6.2. This filter is used to control the reactive part of the input impedance over the whole bandwidth because there is a relationship between the input reflection coefficient and the constant ripple of the Chebyshev filter.

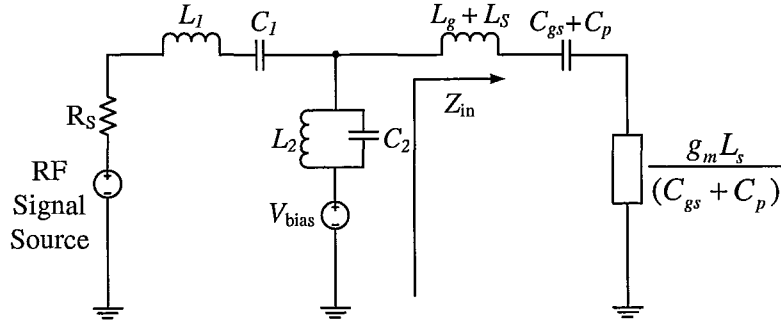


Figure 6.2: Circuit schematic of the three-section Chebyshev filter.

The design steps for the UWB matching network are:

1. Convert the requirement for the input matching into the requirement for filter design. A three-section band-pass Chebyshev filter is suitable due to the relationship between the input reflection coefficient Γ and the in-band ripple ρ_p and because the Chebyshev filter has constant ripple in the pass-band.
2. Follow standard procedure for filter synthesis [55] of a loss-less symmetrically loaded three-section band-pass Chebyshev filter to find the values of the ideal filter components such as L_1 , C_1 , L_2 , C_2 , $C_{gs} + C_p$, $L_s + L_g$, and $\frac{g_m L_s}{C_{gs} + C_p} = 50 \Omega$.
3. Select proper size and bias voltage of the MOSFET transistor to produce transconductance g_m in order to match the real part of the source impedance $\frac{g_m L_s}{C_{gs} + C_p} = R_S = 50 \Omega$.
4. Change the ideal models of the components to real models and tune the values in Cadence to achieve a performance close to the design with the ideal components.

Details for each design step are given below:

In the first step, the input reflection coefficient Γ is related to the in-band ripple ρ_p by [36]:

$$|\Gamma|^2 = 1 - \frac{1}{\rho_p}, \quad (6.2)$$

where we choose the input reflection coefficient $\Gamma < -10\text{dB}$ over the entire bandwidth. Consequently, the value of the ripple ρ_p can be obtained from equation (6.2). From the pass-band ripple, we can determine the filter ripple parameter ε by the following relationship [55]:

$$|\Gamma|^2 = 1 - \frac{1}{\rho_p} = 1 - \frac{1}{\sqrt{1 + \varepsilon^2}}. \quad (6.3)$$

In this way, we translate the input matching design into a design of filter with requirement for max ripple ε .

In the second step, the transfer function of the filter can be determined by the formula that relates the gain magnitude $|A|$ to the ripple parameter ε . The transfer function of the Chebyshev filter prototype is [55]:

$$A^2(\omega) = \frac{1}{1 + \varepsilon^2 T_n^2(\omega)}. \quad (6.4)$$

where $T_0(\omega) = 1$, $T_1(\omega) = \omega$ and $T_2(\omega) = 2\omega T_1(\omega) - T_0(\omega) = 2\omega^2 - 1$. Higher order polynomials can be calculated from the recursion relationship [56]:

$$T_n(\omega) = 2\omega T_{n-1}(\omega) - T_{n-2}(\omega). \quad (6.5)$$

$A(\omega)$ is the gain magnitude, $T_n(\omega)$ is the Chebyshev polynomial, and n is the order

of the Chebyshev filter.

This is the normalized low-pass prototype (L_{PP}) transfer function. Next we transform the L_{PP} to the band-pass filter. $A(\omega)$ is the transfer function of the normalized low-pass prototype L_{PP} . The general form of the transfer function of L_{PP} is [55]:

$$H_{L_{PP}}(s) = K \frac{b_0 + b_1s + b_2s^2 + \cdots + b_ms^m}{a_0 + b_1s + a_2s^2 + \cdots + a_ns^n}, \quad (6.6)$$

Through the substitution

$$s = \frac{1}{BW} \frac{p^2 + \omega_0^2}{p}, \quad (6.7)$$

$H_{L_{PP}}(s)$ is transformed into a band-pass transfer function $H_{BP}(p)$ with the form

$$H_{BP}(p) = K' p^{n-m} \frac{1 + B_1p + B_2p^2 + \cdots + B_2p^{2m-2} + B_1p^{2m-1} + p^{2m}}{1 + A_1p + A_2p^2 + \cdots + A_2p^{2m-2} + A_1p^{2m-1} + p^{2m}}. \quad (6.8)$$

In our design, we choose the pass-band frequencies as 3.1 and 10.6 GHz which means low angular frequency is $\omega_L = 2\pi(3.1 \times 10^9)$ rad/s and high angular frequency is $\omega_H = 2\pi(10.6 \times 10^9)$ rad/s. The parameter of ω_0 can be calculated as [55]:

$$\omega_0 = \sqrt{\omega_L \omega_H}, \quad (6.9)$$

and the bandwidth parameter is:

$$BW = (\omega_H - \omega_L) = 2\pi(10.6 \times 10^9 - 3.1 \times 10^9) \text{ rad/s}. \quad (6.10)$$

Now substituting ω_0 and BW back to equation (6.7), we obtain the expression of p . Then, the transfer function of the band-pass filter is determined by substituting p into equation (6.8). The transfer function is polynomial expressions which means

we can solve them to obtain the terms of each section. After that, the values of the inductors and capacitors can be selected according to the following expressions [55]:

$$Z_{\text{series}}(p) = pL_{\text{series}} + \frac{1}{pC_{\text{series}}}, \quad (6.11)$$

$$Y_{\text{parallel}}(p) = pC_{\text{parallel}} + \frac{1}{pL_{\text{parallel}}}, \quad (6.12)$$

where Z_{series} stands for the impedance of a series combination of an inductor and a capacitor while Y_{parallel} stands for the admittance of a parallel combination of an inductor and a capacitor. Now we can design the three-section (third-order) Chebyshev filter by following these standard filter design synthesis.

In the third step, we will choose the proper value of g_m . It is generated by choosing the proper size and bias voltage of MOSFET transistor in Cadence software. Therefore, the real part of the input impedance can be matched to 50Ω and the certain DC current can be determined.

The last step is to change all the ideal components into real components and tune the values in Cadence. The main purpose is to achieve low power consumption. Meanwhile, other performances are also optimized as much as possible. All the values of the components are listed in Table 6.1.

The output matching is not very important since usually the front-end LNA is followed by the mixer stage. However, here, output matching is needed since we can only simulate the UWB LNA by itself instead of as part of a whole receiver front-end system. Therefore, an output buffer is added to the circuit for the purposes of measurement within the simulation.

The output performance of the ultra-wideband LNA can be measured and

quantified in the same manner as for the narrow-band LNA of Chapter 5. However, the critical parameter in this UWB LNA design is to minimize the power consumption. The gain should be designed flat and high through the entire bandwidth. The noise figure (NF) should also be designed to be flat and low across the entire bandwidth, as should the input and output return losses. The linearity is measured by the IIP_3 value however, should be high while it is desirable that DC power consumption be as low as possible. The input return loss (S_{11}) and output return loss (S_{22}) should be low and flat over the entire bandwidth. Furthermore, the DC power should be carefully minimized as well.

6.2 Circuit Implementation of UWB LNA

The the proposed amplifier is designed to be implemented using IBM 0.13- μm CMOS technology and is simulated using the Cadence software suite package.

In Figure 6.1, the NMOS transistors M_1 and M_2 , which are built in cascode configuration and perform the amplification of the incoming RF signals, and the resistor R_L and inductor L_L , together with an output buffer built using the NMOS transistors M_3 and M_4 , form an output matching network, which is used for measurement purposes only.

The relevant values of all the circuit elements can be determined from the theories discussed in Chapter 4. In order to make the NMOS transistors M_1 and M_2 work properly, an appropriate biasing voltage should be selected to ensure that both transistors are working in the saturation region and that they provide a reasonable DC current I_D . Therefore, our biasing voltage is set to be 465 mV. In summary, the overall design parameters are listed in Table 6.1.

M_1	$W \times L = 160 \mu\text{m} \times 0.13 \mu\text{m}$
M_2	$W \times L = 50 \mu\text{m} \times 0.13 \mu\text{m}$
M_3	$W \times L = 48 \mu\text{m} \times 0.13 \mu\text{m}$
M_4	$W \times L = 48 \mu\text{m} \times 0.13 \mu\text{m}$
DC Bias Voltages (V_{bias})	0.465 V
DC Supply Voltage	1.2 V
L_1	600 pH
L_2	600 pH
C_1	500 fF
C_2	300 fF
L_g	1.108 nH
C_p	60.02 fF
L_s	401 pH
L_L	868 pH
R_L	122.2 Ω

Table 6.1: UWB LNA design parameters.

The resulting layout, as found using Cadence, is shown in Figure 6.3.

6.3 Simulation Results

The simulations were done using the Spectre RF package from the Cadence software suite in 0.13- μm CMOS process and the device models were provided by CMC Microsystems.

All of the performance characteristics except for the IIP_3 are simulated using S-Parameter (SP) analysis, the theory of which was discussed in Chapter 4.

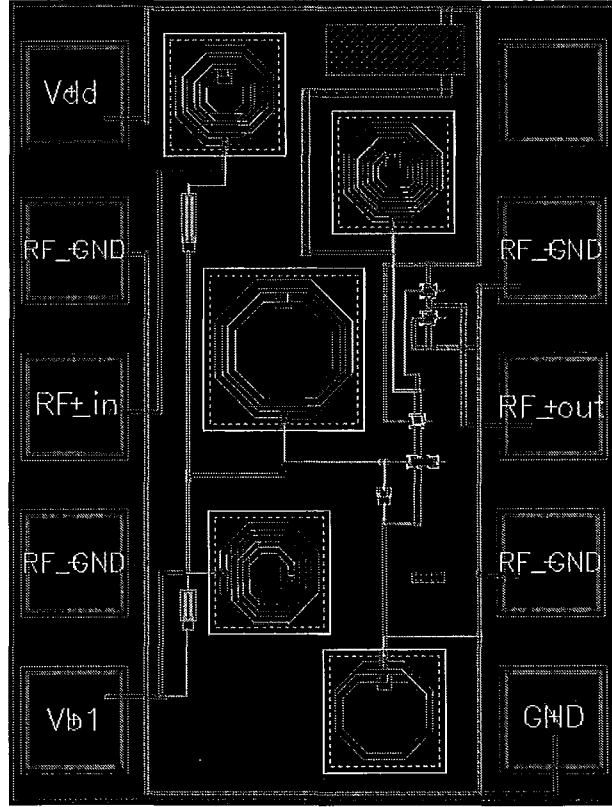


Figure 6.3: Physical layout of the ultra-wideband low-noise amplifier.

6.3.1 Gain

The gain vs. frequency was calculated for a matched input impedance $Z_{in} = Z_S = 50\Omega$, and an impedance matching output buffer. The resulting gain (S_{21}) values are shown in Figure 6.4, where the bandwidth of the designed UWB LNA is 3.1-10.6 GHz.

As marked, the maximum gain value is $G_{max} = 12.07$ dB and the minimum value is $G_{min} = 10.27$ dB. This indicates that the gain variation of our designed UWB LNA is $G_{variation} = G_{max} - G_{min} = 12.07 - 10.27 = 1.8$ dB. Meanwhile, the

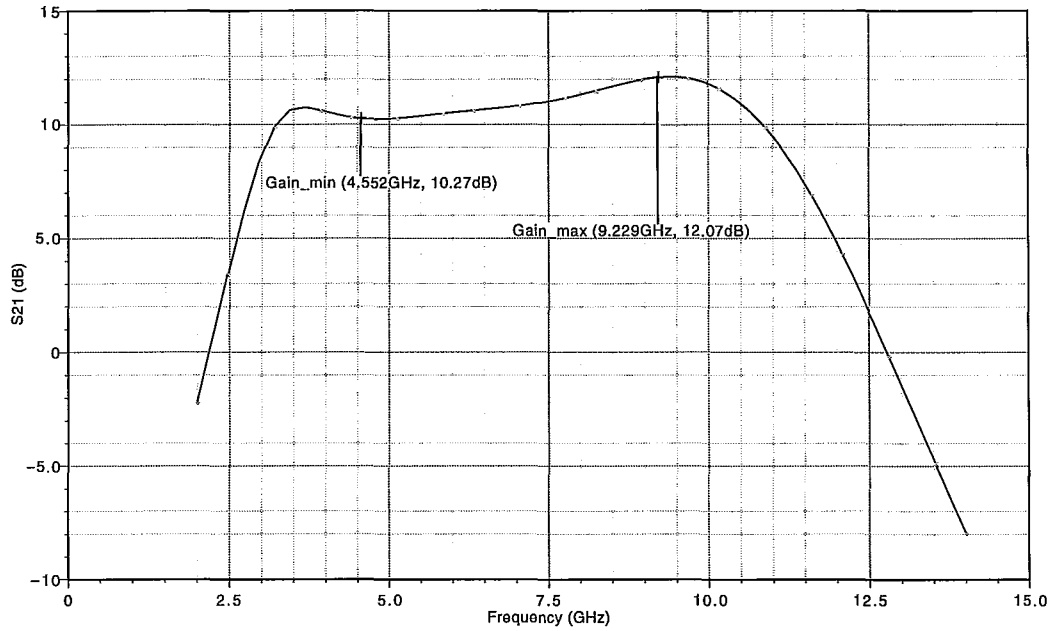


Figure 6.4: The gain (S_{21}) of UWB LNA.

average value of the gain in Figure 6.4 is $G_{\text{average}} = 11.17$ dB. From this, we can calculate that the gain flatness is $\Delta G = \pm 0.9$ dB ($11.17 - 10.27 = 0.9$ dB and $11.17 - 12.07 = -0.9$ dB).

6.3.2 Noise

Figure 6.5 shows the noise figure over the designed bandwidth. As indicated on the plot, the minimum value is $NF_{\text{min}} = 3.38$ dB and the maximum value is $NF_{\text{max}} = 5.92$ dB. Therefore, the noise figure variation is $NF_{\text{variation}} = NF_{\text{max}} - NF_{\text{min}} = 5.92 - 3.38 = 2.54$ dB. In addition, the average noise figure of this UWB LNA simulation is $NF_{\text{average}} = 4.65 \pm 1.27$ dB.

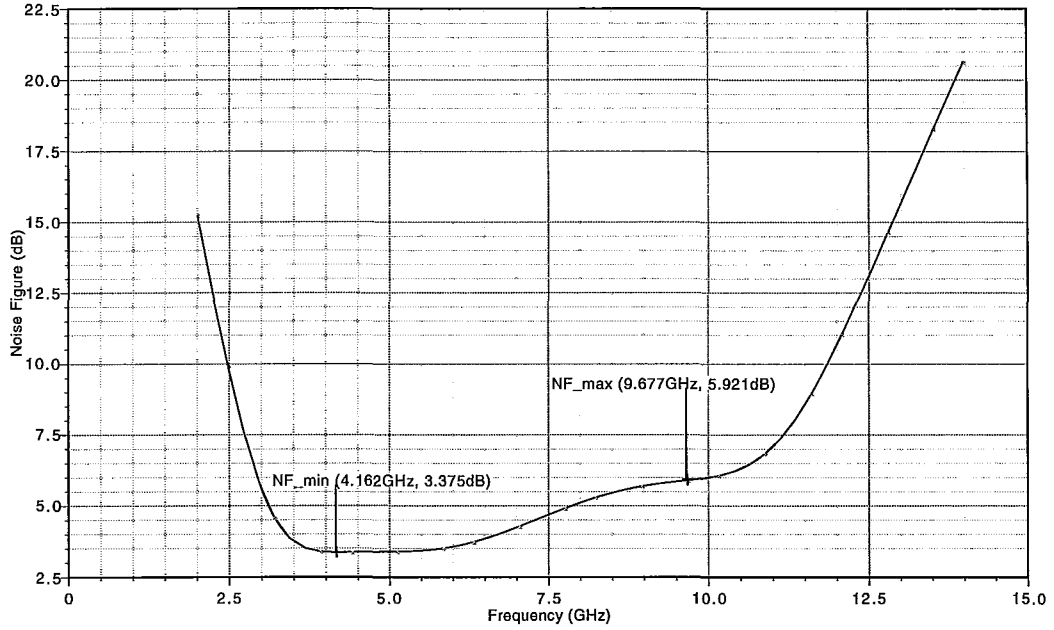


Figure 6.5: The noise figure (NF) of the UWB LNA.

6.3.3 Linearity

The simulated IIP_3 is simulated using Periodic Steady-State (PSS) analysis, at the mid-band frequency of 6 GHz. The two-tone test was applied and assuming the desired RF input signal to be $f_{rf1} = 6.0$ GHz with another RF signal present at $f_{rf2} = 6.1$ GHz. Therefore, the third order terms appeared at

$$\begin{aligned}
 2f_{rf2} - f_{rf1} &= 2 \times 6.1 - 6.0 = 6.2 \text{ GHz}, \\
 2f_{rf1} - f_{rf2} &= 2 \times 6.0 - 6.1 = 5.9 \text{ GHz}.
 \end{aligned} \tag{6.13}$$

In the simulator, we then picked the first order term at 6.0 GHz and third order term at 6.2 GHz. The simulated IIP_3 is shown in Figure 6.6 and has a value of -3.81

dBm.

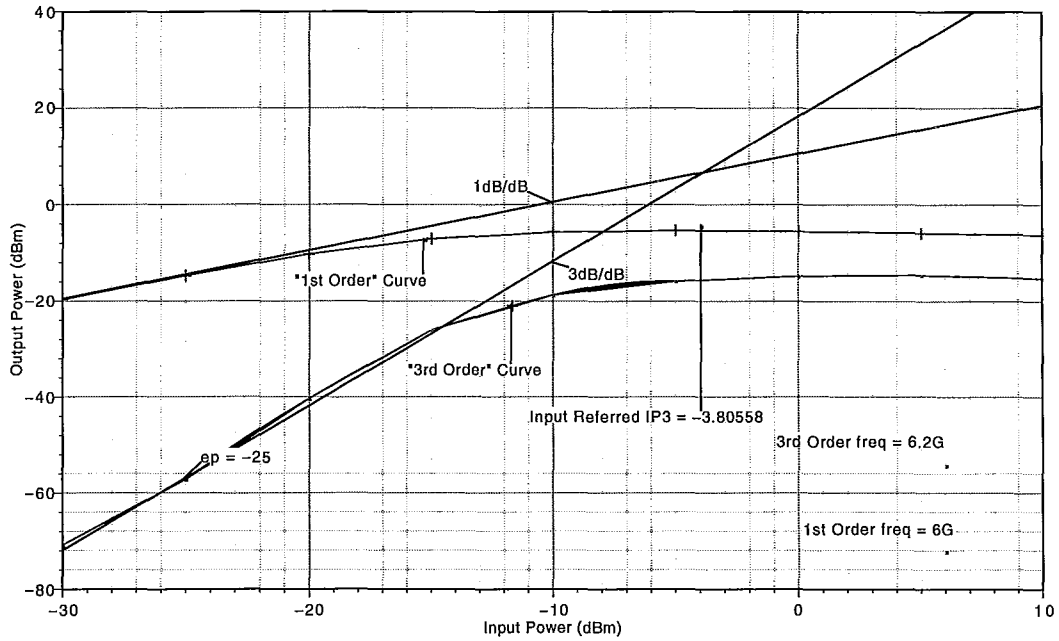


Figure 6.6: IIP_3 of UWB LNA.

6.3.4 Input and Output Return Loss

The input and output return losses are quantified by the two-port parameters S_{11} standing for the input return loss, and S_{22} standing for the output return loss. As marked in Figure 6.7, the value of S_{11} is below -10 dB within most of the bandwidth. However, when the input frequency is high, the input return loss increases, although the entire curve is still below -6.66 dB. Meanwhile, the value of S_{22} is always below -10 dB throughout the entire bandwidth of interest.

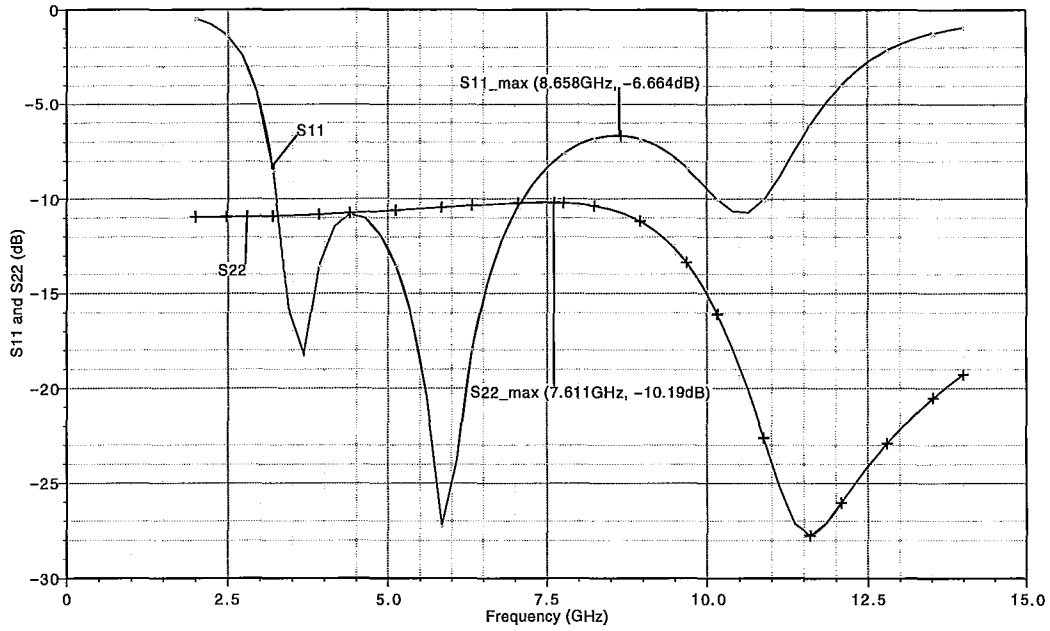


Figure 6.7: The input and output return loss (S_{11} and S_{22}) of UWB LNA.

6.3.5 Power Consumption

Given a 1.2 V supply voltage, the DC current of the UWB LNA core is 2.345 mA, and the DC current of the output buffer is 4.714 mA. This implies that the power consumption of the LNA core is 2.81 mW and the power consumption of the output buffer is 5.66 mW. Therefore, the total power consumption of the LNA can be summarized as being:

- 2.81 mW without the output buffer,
- 8.47 mW with the output buffer.

The total designed chip area is $0.6 \times 0.8 = 0.48 \text{ mm}^2$ including the on-chip output buffer and pads, shown in Figure 6.3.

A summary of the overall simulation results is listed in Table 6.2.

Technology	0.13 μm CMOS
Bandwidth	3.1-10.6 GHz
Gain (S_{21})	10.27-12.07 dB
NF	3.38-5.92 dB
IIP ₃	-3.81 dBm
Input return loss S_{11}	<-7 dB
Output return loss S_{22}	<-10 dB
Power dissipation (without buffer)	2.81 mW
Power dissipation (with buffer)	8.47 mW
Chip area	0.48 mm ²

Table 6.2: Simulation of UWB LNA Performance.

6.4 Comparison and Discussion

In order to compare the overall performance to other existing works, we need to define a performance metric for ultra-wideband low noise amplifier. Using equation (5.14) in Chapter 5, extended over the entire bandwidth, the figure of merit (FoM) of the UWB LNA can be defined as:

$$\text{FoM} = 20 \log(\text{BW}) + G + \text{IIP}_3 - \text{NF}_{\text{average}} - 10 \log(P_{\text{diss}}). \quad (6.14)$$

where we translate all the values into normalized unit and BW is the bandwidth in GHz normalized to 1 GHz, G is the gain of the LNA in dB normalized to 1 dB, IIP₃ is the linearity in dBm normalized to 1 dBm, NF is the noise figure in dB normalized to 1 dB, and P_{diss} is the power consumption of the UWB LNA circuit in mW normalized to 1 mW.

Table 6.3 shows that the FoM of our UWB LNA is much better than that of other designs published in the literature promising design. In other words, our ultra-wideband LNA is definitely dominant among those published works.

The advantages of our design are:

- Fairly simple structure for fabrication and an easy architecture for the purposes of analysis and understanding.
- Extremely low power consumption.
- A relatively high, flat gain and great flatness of the gain (little gain variation or small gain ripple).
- Large bandwidth according to FCC allocation rules.
- Relatively high IIP_3 at the mid-band frequency.
- Small chip area.

The disadvantages of our design are:

- Not a perfect noise figure (NF).
- Relatively high input return loss (S_{11}).

The primary benefits of this design is that it provides a simple circuit structure, flat and high gain, as well as a low power dissipation, and a very wide bandwidth. Normally LNA design involves tradeoffs. If some particular performance criteria need to be optimized, some others may need to be sacrificed, as there is no way to optimize every parameter simultaneously. Therefore, knowing what kind of

	CMOS Technology (μm)	S_{11} (dB)	Bandwidth (GHz)	Gain S_{21} (dB)	NF (dB)	IIP ₃ ^a (dBm)	DC Power (mW)	Chip Area (mm ²)	FoM ^b
This Work	0.13	<-7	3.1 – 10.6	10.3 – 12.1	3.4 – 5.9	-3.81	2.81	0.48	15.8
[36] STD	0.18	<-9.9	2.3 – 9.2	6.3 – 9.3	4 – 9.2	-6.7	9	1.1	1.73
[36] TW	0.18	<-9.4	2.4 – 9.5	7.4 – 10.4	4.2 – 9.2	-8.8	9	1.1	0.88
[57]	0.18	<-10	0.4 – 10	9 – 12.4	4.4 – 6.5	-6	12	0.42	8.10
[41]	0.18	<-11	1.2 – 11.9	6.7 – 9.7	4.5 – 5.1	-6.2	20	0.59	4.78
[58]	0.09	<-10	2 – 11	9 – 12	5 – 6	-4	17	0.7	7.78
[59]	0.18	<-9	2 – 4.6	9.8	2.3 – 5.2	-7	12.6	0.9	-3.65
[60]	0.18	<-16	0.03 – 7	7.4 – 8.6	4.2 – 6.2	1.8	9	1.16	11.9
[61]	0.18	<-8	0.6 – 22	6.5 – 8.1	4.3 – 6.1	N/A	52	1.35	N/A
[62]	0.18	<-8	3.1 – 10.6	13.5 – 16	3.1 – 6	-7	11.9	1.2	9.95
[39]	0.18	<-11	3.1 – 10.6	10.9 – 12	4.7 – 5.6	-12	10.6	0.67	1.55
[63]	0.18	<-12	3 – 6	13.5 – 15.9	4.7 – 6.7	-5	59.4	1.1	-4.20
[64]	0.18	<-10	2.7 – 9.1	10	3.8 – 6.9	1	7	1.57	13.3
[65]	0.18	<-11	3 – 5	11.4 – 14	5.0 – 5.3	-9.7	16.4	0.9	-8.28

Table 6.3: Comparison of UWB LNA Performance.

^aIIP₃ is estimated at mid-band frequency.^bFoM is calculated using average gain (S_{21}) and average noise figure (NF).

performance we are interested in and then optimizing it without sacrificing other parameters too much is the key to ultra-wideband LNA design.

From the simulation results, it is obvious that the advantages of the proposed design outweigh the disadvantages. In other words, we have achieved the desired UWB LNA performance with some acceptable tradeoffs.

Chapter 7

Conclusion

7.1 Summary

In this thesis, a new narrow-band receiver front-end containing a narrow-band low-noise amplifier followed by a downconversion double balanced mixer was investigated. This investigation included the design, simulation and physical instantiation of the system using TSMC 0.18- μm technology. Furthermore, the design of an ultra-wideband low-noise amplifier was also investigated through Cadence simulation of the device in IBM 0.13- μm CMOS technology.

The narrow-band receiver design was focused on solving the problem of connecting a LNA to a double-balanced mixer. In Chapter 5, a novel idea for solving this problem was proposed in the form of a re-designed mixer. The new double-balanced mixer needs only a single RF input from the LNA, and does not require an on-chip transformer. The receiver circuit is designed to operate at 2.4 GHz and produce the IF output at 300 MHz. The overall measured results are about average in terms of performance when compared to other published designs. Just as

importantly however, the new approach solving the LNA-to-mixer connection is both introduced and verified. The proposed improvements therefore likely aid in the design of future receivers.

The new ultra-wideband low-noise amplifier discussed in Chapter 6 is designed to optimize the overall performance with great emphasis on low-power consumption design. This inductively source degenerated UWB LNA is demonstrated in Chapter 6 through simulation in Cadence. This circuit operates through the entire UWB bandwidth from 3.1 to 10.6 GHz frequency range with good values for the different performance characteristics, such as gain, flatness, matching, linearity and noise. The power dissipation of this design is obviously much lower compared to other designs, and the overall performance of our UWB LNA in terms of FoM for UWB amplifiers is mostly superior when compared to other published works as was discussed in Chapter 6.

7.2 Future Work

7.2.1 Narrow-Band Receiver

The main issue to be resolved regarding the new receiver design relates to the double balanced mixer. Unlike standard mixer designs, we have placed a PMOS in one of the two circuit branches instead of using an NMOS device in each. As discussed in Chapter 2, the mobility of PMOS is much smaller than that of NMOS. This makes it hard to create a perfect differential signal pair due to the slower reaction of the PMOS. One possible solution to this problem is to improve the mobility

of PMOS in the CMOS process technology. This is not far-fetched, as new technology has already improved the mobility of both PMOS and NMOS [66]. Another possible solution is that we may sacrifice the mobility of NMOS in order to achieve better balance without degrading the performances out of competitive levels. As a result, the mobility of the PMOS is almost equal to the mobility of the NMOS. For example, we may use a lower technology NMOS such as $0.18\text{-}\mu\text{m}$ and a higher level PMOS such as $0.13\text{-}\mu\text{m}$ to create more balanced differential signal pair. These could solve the mixer design problem in the future. However, the costs associated with these solutions will also need to be considered.

7.2.2 Ultra-Wideband Low-Noise Amplifier

The problem with the new ultra-wideband low-noise amplifier design is that its noise figure is neither very flat nor extremely low. As described in Chapter 4, the noise figure of an amplifier can be significantly improved if a noise canceling technique [41, 42] is applied. In the future, noise canceling methods should be investigated while trying to maintain the other performance measures at almost the same level.

Another issue to be addressed is that the input return loss is relatively high. This is because the input matching network was not optimized for input return loss, as it was designed to optimize gain, noise figure and power dissipation instead. However, this problem could likely be solved by trading off increased power consumption for a better input return loss.

In summary, the UWB LNA has room for improvement. However, it is important to pay attention to the overall performance (the figure of merit) in order to

decide whether a particular modification is acceptable.

Appendix A

Experimental Setup

In order to measured the receiver circuit, the following equipments has been selected and used

- The RF and LO signals are generated by Signal Generators. Agilent E4422B Signal Generator, Agilent 83752A Synthesized Sweeper, and the Anritsu MG3694A Signal Generator have been used.
- The HP 4145B Semiconductor Parameter Analyzer has been used to provide the DC voltages and DC biases.
- The Agilent E4440A Spectrum Analyzer has been used to observe the output IF signal of the DUT.
- The HP 8970B Noise Figure Meter with Ailtech 7616 Noise Source have been used to measure the noise figure of the Device Under Test (DUT).
- The Anritsu K251 Bias Tees have been used to combine DC and RF signal to add DC offset to the signal so that the transistors in the circuits were biased

to work in saturation region.

- The Krytar Double Arrow 180° Hybrid Splitter has been used to produce a differential signal pair (180 degrees out of phase) for LO inputs of the mixers from the single-ended signal of signal generators.
- The 12GHz power divider combiner has been used to combine the two signals from signal generators, where the power combiner is from American Microwave Corporation.
- Two sets of Multi-Probes from GGB Industries INC are used to connect the cables to the pads of DUT. The measurements have been carried out on wafer, using Karl Suss PM8 probe station.

where the circuit condition is that the RF input signal is at 2.4 GHz with -30 dBm power amplitude, the LO input signal is at 2.1 GHz with 0 dBm power amplitude, and the IF output is at 300 MHz.

Note that the receiver IF output is single-ended, but not differential. As a result, we implement another MOSFET which functioned as a dummy load for 50 Ω matching for symmetric purpose on chip. Therefore, the actual differential output gain should be 3dB higher than the measured one and the actual RF and LO feedthroughs should be better if differential output is obtained according to the theory in Chapter 3. Another aspect is the RF cables, Splitter, and Bias Tees losses. One possible method to compensate the losses is that we connect a Signal Generator to the RF cables, Splitters, or Bias Tees and then feed them into a Spectrum Analyzer. Setting the frequency to 2.4 GHz, 2.1 GHz, or 300 MHz, we observed the certain losses for certain components at different frequencies. For example, we

only need to test the losses for all the RF input components at 2.4 GHz, test the losses for all the LO input components at 2.1 GHz, and test the losses for the IF output components at 300 MHz. Then we have the following conditions

- The RF input cable and Bias Tee has 3 dBm losses for gain measurement and if the power divider is added for IIP_3 measurement, the loss is 6 dBm since power divider has 2 dBm losses and another RF cable needs to be added for each RF inputs which has 1.6 dBm losses. Meanwhile, all the input losses are measured at 2.4 GHz.
- The LO input has RF cable losses, Splitter loss, and two Bias Tee losses which is approximately 4 dBm loss for each of the differential LO input at 2.1 GHz.
- The output RF cable has a 1.5 dBm at 300 MHz

As a result, the input losses are easy to compensate. For instance, if we measure the gain of the receiver circuit, we can setup the power to be -27 dBm in Signal Generator if we want the desired actual RF input power to be -30 dBm which compensates the 3 dBm loss due to the input components losses. The same theory can be applied to the LO input signal. However, at the output, we can simply add the power loss to whatever outputs we have observed from the Spectrum Analyzer.

A.1 Gain and output Measurement

In order to measure the gain and output of the receiver, we setup the experiment as shown in figure A.1. The 2.4 GHz RF input signal is from Signal Generator 1. Then it is fed into a Bias Tee to add necessary DC bias while the original RF input

signal passes through and flows to the DUT. In addition, Signal Generator 2 is used to generate the LO input signal at 2.1 GHz and it is connected to an 180° Splitter which creates a differential signal pair (180 degrees out of phase) of the LO signal. Then two Bias Tees are used to add DC bias for both signals. All the voltages sources including DC supply voltages and DC biasing voltages are provided by the Semiconductor Parameter Analyzer in which the DC currents of each stage of the receiver have been monitored. The spectrum of IF signal output is read by the Spectrum Analyzer. The spectrum includes the gain, the RF feedthrough, and the LO feedthrough.

A.2 IIP₃ Measurement

Figure A.2 shows an experimental setup to measure the linearity (IIP₃) of the receiver. All the components in the setup for gain and output measurements are reused for the two-tone measurement of IIP₃, and another Signal Generator 3 and one power divider are added to combine the RF signal. Signal Generator 3 is used to produce another RF input signal at frequency close to the original 2.4 GHz in order to create a two-tone test. The summation of these two RF signals is achieved by feeding them together into the power divider and hence, the output is the desired summed RF signal with adjacent frequencies. As discussed in chapter 5, the two-tone test in simulation in Cadence uses two RF signals at 2.4 and 2.375 GHz. Therefore, the 1st order harmonics are at 300 and 275 MHz and the 3rd order harmonics are at 325 and 250 MHz. Either one in 1st order terms and 3rd order terms will be used to plot the 1st and 3rd order curves and therefore, the IIP₃ can be obtained according to the theory in Chapter 2.

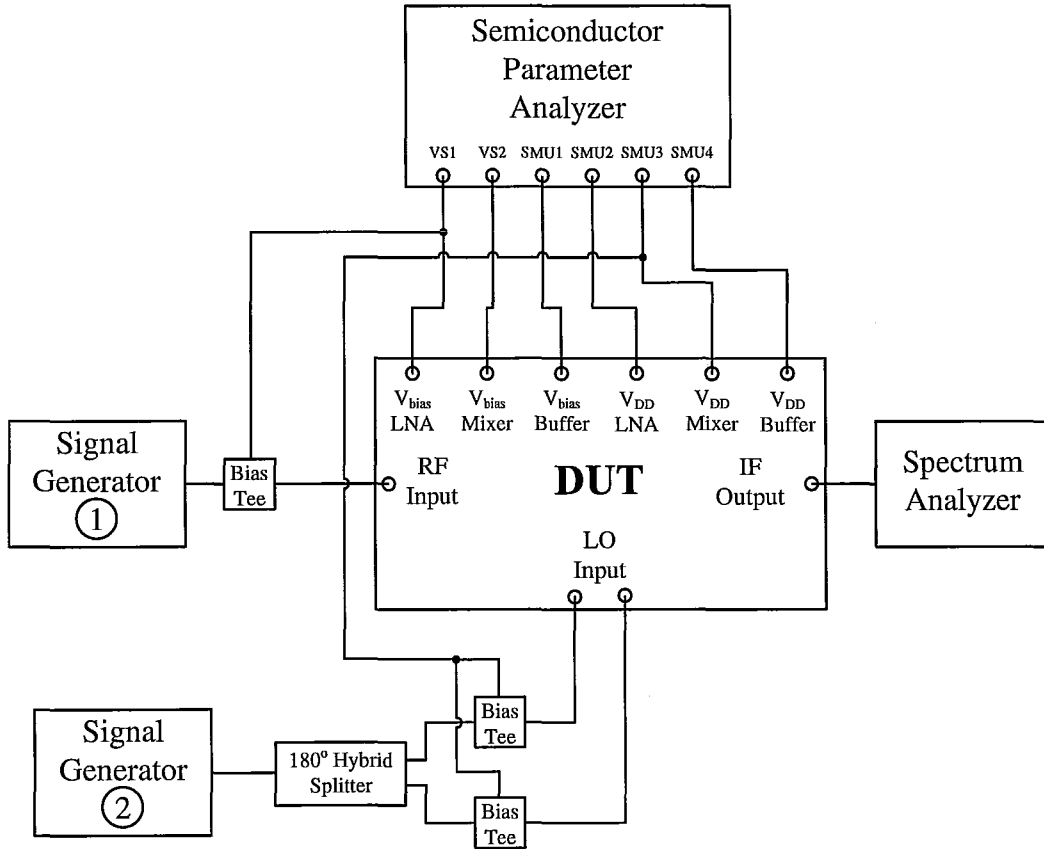


Figure A.1: Experimental Setup for output measurement.

A.3 Noise Figure Measurement

In order to measure the noise figure, a Noise Source and Noise Figure Meter are added and the experimental setup shown in figure A.3. The Noise Figure Meter is controlled by entering certain codes. Referring to the manual, we setup the noise figure measurement using special function 1.4 which is coded to control a generator to measure the NF of a receiver or mixer with an external LO system, as shown in figure A.3. Then we setup the conditions for our receiver circuit such as

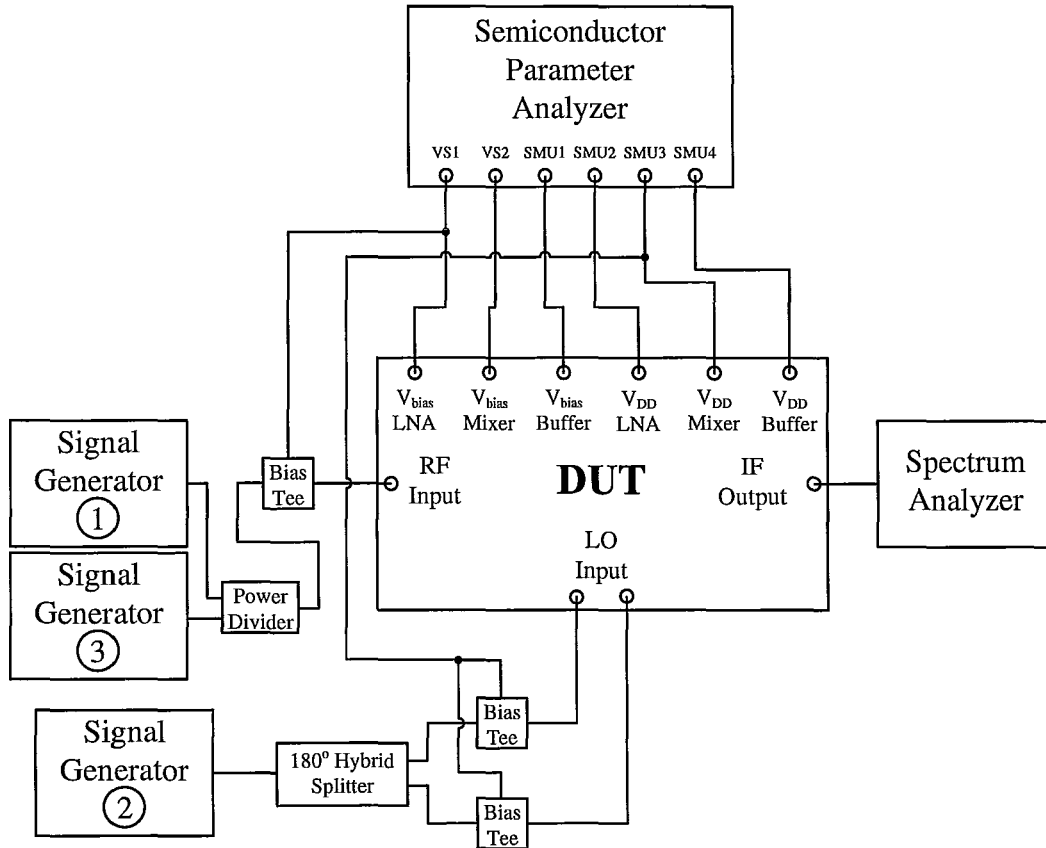


Figure A.2: Experimental Setup for IIP₃ measurement.

LO frequency, LO input power, and IF frequency, etc. A calibration was performed to compensate the losses in the components used in the setup, e.g. in cables and bias Tees.

After the calibration, we insert our DUT (receiver circuit) into the measurement system and the experimental setup is shown in figure A.4. Note that, the external LO system is controlled by the Noise Figure Meter via System Interface Bus (SIB)

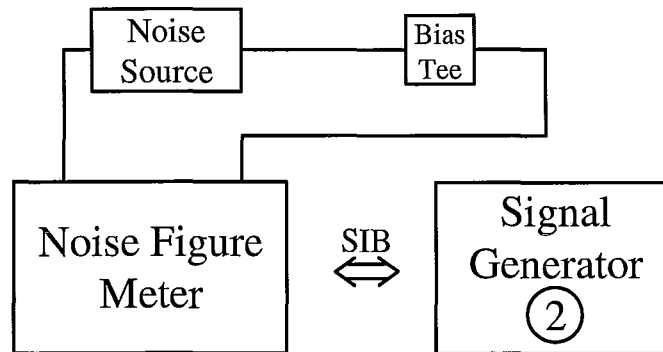


Figure A.3: Calibration Setup for noise figure measurement.

which is HP 10833A GPIB cable. The noise figure was measured by selecting "corrected noise figure and gain" function in which the losses have been compensated. Therefore, the values on the Noise Figure Meter display are the corrected values for NF and insertion gain of DUT.

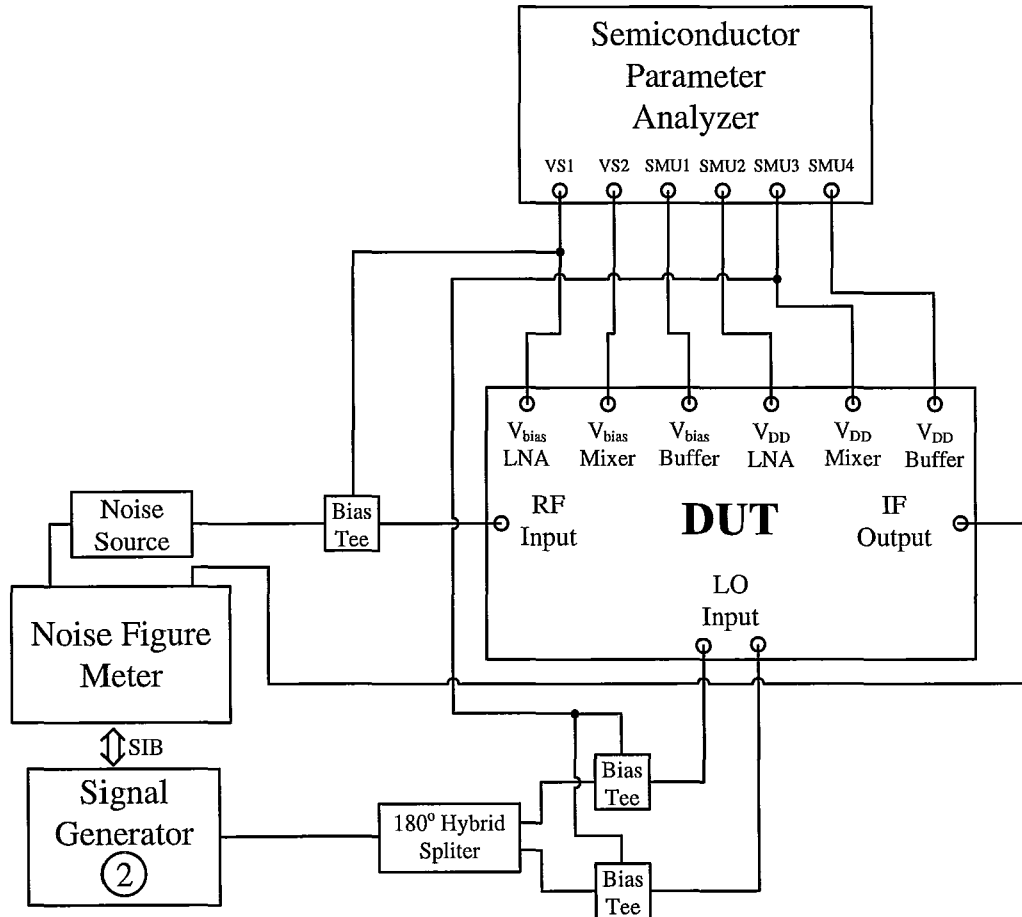


Figure A.4: Experimental Setup for noise figure measurement.

Appendix B

S -Parameters

Scattering parameters or S -parameters relates the voltage waves incident on the ports to those reflected from the ports, as shown in figure B.1. The S -parameters is widely used in microwave and electronic circuit designs for its convenience to analyze the network especially when the input and output ports are matched normally to $50\ \Omega$.

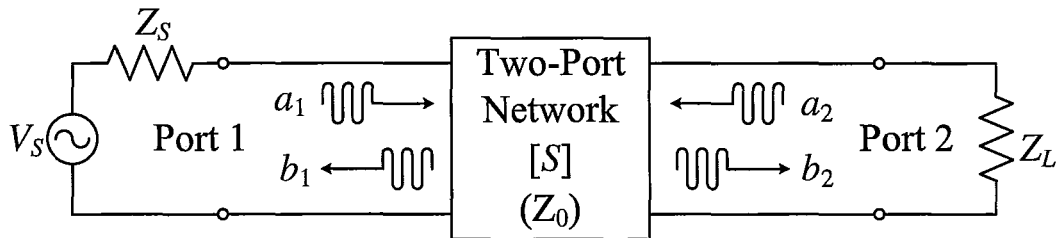


Figure B.1: Incident and reflected waves of a two-port network [24].

The two port network shown in figure B.1 can be analyzed using its signal flow graph, shown in figure B.2. The following equations of this two-port network can

be obtained as [24]:

$$b_1 = S_{11}a_1 + S_{12}a_2, \quad (\text{B.1})$$

$$b_2 = S_{21}a_1 + S_{22}a_2, \quad (\text{B.2})$$

where a_1 , a_2 , b_1 , and b_2 indicate the amplitudes of the incident and reflected waves.

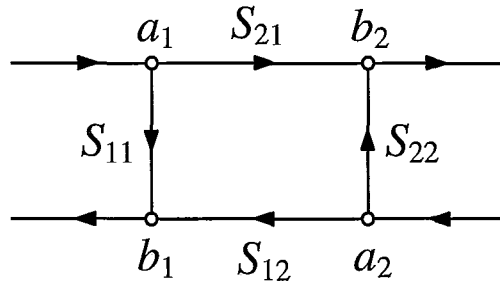


Figure B.2: Signal flow graph of a two-port network [24].

The overall definition of the S -parameters can be defined as [24] if the input and output ports are matched:

$$S_{11} = \left. \frac{b_1}{a_1} \right|_{a_2=0} = \text{Input reflection coefficient}, \quad (\text{B.3})$$

$$S_{22} = \left. \frac{b_2}{a_2} \right|_{a_1=0} = \text{Output reflection coefficient}, \quad (\text{B.4})$$

$$S_{21} = \left. \frac{b_2}{a_1} \right|_{a_2=0} = \text{Forward transmission gain}, \quad (\text{B.5})$$

$$S_{12} = \left. \frac{b_1}{a_2} \right|_{a_1=0} = \text{Reverse transmission gain}. \quad (\text{B.6})$$

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