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A COLOR-CODED RADAR DISPLAY

DESIGN AND HARDWARE IMPLEMENTATION OF A COLOR-CODED DISPLAY SYSTEM FOR RADAR SIGNALS

by

Soraya Mohammed El-sagir,

B.Eng. & B.Sc. (Mathematics)

A Thesis
Submitted to the Faculty of Graduate Studies
in Partial Fulfilment of the Requirements
for the Degree
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ABSTRACT

This thesis gives the design and hardware implementation of a display system for the synthetic presentation of real time radar signals. A color coding technique is applied in the system, where a color code of sixteen different colors is employed to encode the signal amplitude. The system consists of a color television monitor, a large scale random access memory and digital interfaces to buffer the real time input to the display.

A general study of the different types of display devices followed by a review of the common radar displays is presented. Then, a detailed investigation and a presentation of a color coding technique and its application is given.

The details of the system design and operation are given in addition to the experimental work for testing the system performance. The presentation of radar signals by the color coded display system is demonstrated.

ACKNOWLEDGEMENTS

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CHAPTER 1

INTRODUCTION

The interface between human observer and electronic equipment is of major importance, especially when a large quantity of irrelevant information is being presented. Such is the case in radar where the operator has to be responsive to target detection. In case of air traffic control radar, the targets of primary interest are aircraft . However, radar echoes are also received from a variety of other objects within the operating environment of the radar. These include objects on the ground such as buildings, trees, hills; those in sea such as waves, and floating objects; birds and weather conditions such as rain, snow, clouds, and air turbulence.

This means that aircraft are not the only objects to be displayed by the radar indicator. These extraneous echoes tend to mask the appearance of the display. For example, birds during migration can cover areas of the display, or, in a small group can give an indication similar to an aircraft. Air turbulence also has a similar effect on the indicator. Thus, it is extremely important to reduce the risk of aircraft disaster due to severe weather turbulence and the bird strike problem.

There have been many disastrous aircraft crashes due to problems caused by storms. Recently, on April 4, 1977 a Douglas DC-9, with its engines deadened due to hail stones in

a severe thunder storm, crashed in Georgia [1]. Reuter news agency reported 72 deaths and 28 injuries, many critical, when the plane attempted to land on a highway but instead hit a pole, trees, cars, and grocery store before it exploded and burned.

Birds have also caused a number of commercial and military aircraft crashes in various countries. The main problem occurs when birds get caught in aircraft engines since one or two large birds can destroy an engine. In the United States, birds caused the engine of a DC-10 to explode causing $25-million damage. In Canada, the average bill for such damage is now of the order of $150,000 a year and in some years runs as high as half a million dollars [2]. (The total for New York Kennedy Airport in 1975 was about $40-million).

It has been reported that the avoidance of birds is a major problem for pilots [3]. The Canadian Armed Forces lost a dozen CF-104 Star Fighters worth $1.5 million each in the last eight years. In West Germany, sixteen Luftwaffe planes have crashed since 1958 after striking birds [5]. In the latest accident on April 19, 1977 a Star-Fighter fell into the Baltic Sea after a sea-gull was sucked into the jet engine. The West German airforce intended action against birds and issued special warnings to its pilots.

The bird hazard has been sufficient to maintain a group in Ottawa called the National Research Council Associate Committee on Bird Hazards to Aircraft. The objectives of the group are to find means for excluding birds from airports and planes

in flight. Lately, National Research Council (NRC) has disbanded its bird committee because, in 14 years, it has created enough momentum for other Federal agencies to take over [4]. The committee contributed greatly to 'people safety' in the air. It also inspired inventors from far and wide to come forward with ideas for solving the costly and even potentially disastrous threat posed by mid-air collisions between birds and aircraft . A major problem is due to migrating birds in the area surrounding airports and methods for getting rid of them,have ranged from ultra-sonic sounds to blasts from shotgun. The bird hazard committee also pioneered the method of predicting migration patterns as an aid, to pilots, and its efforts over the years led to the creation of the Bird Strike Committee (Europe).

One of the main solutions to the problem of detecting and identifying aircraft, in the presence of interfering objects, is to improve the capabilities of the radar equipment especially in the area of display systems. This can be achieved by increasing the capacity for displaying large amounts of data with easier interpretation of the displayed information. A possible technique which can assist in this aspect is the use of color [6]. The phenomenon of seeing light and color has always been fascinating. Through the ages, people learned the properties of colors and the natural color mixing possibilities [7], and the color has been used in many different fields to provide useful discrimination properties.

In the area of information displays, presentation of

data using only a monochrome display conveys information in an incomplete form. Strong signals and weak signals yield essentially the same bright-up spot. The eye accepts and interprets the information despite its limitations but the display has a missing dimension, lacking all the variables provided by that which the eye recognizes as color. As a matter of fact, scientifically controlled tests showed that color-coding at any level yielded an improvement in time scores [8,9]. Color coding can further enhance the data presentation and make the interpretation easier. Also, an excellent selection of color devices exists (as shown in Chapter 2).

Scope of Thesis

The main objective of this thesis is the design and construction of a display system, in which a color coding technique is implemented. The display system employs a color television monitor and a large scale random access memory. The system function is to develop a synthetic presentation of real time radar signals, using sixteen different colors to encode the signal amplitude.

A survey of the different types of display devices is presented in Chapter 2. The advantages, disadvantages and the compatibility of these devices with this kind of application are also discussed.

Chapter 3 is devoted to a theoretical background review of the radar systems, and a description of the common radar displays. The last section of the chapter discusses the color-coding

technique, and its application in the raster scan color television display .

A presentation of the system function and general description is given in Chapter 4, followed by the details of the system design and operation.

The experimental procedure for color-code selection, system testing and color convergence adjusting are described in Chapter 5.

Chapter 6 gives the significant results of using the display system for the presentation of radar signals, together with a detailed discussion.

Finally, Chapter 7 contains the conclusions of this work and recommendations for further investigations .

CHAPTER 2

SURVEY OF DISPLAY DEVICES

2.1 LIGHT EMITTING DIODE DISPLAYS:

The light emitting diode (LED) is a solid state device which is capable of emitting electromagnetic radiation in the visible light region. Devices which emit in the red region of the spectrum are now commercially available and the ability to produce bi- or tri- colors (red; green and yellow) has been also shown [11, 12].

Although LED devices have a role as individual lamps for "on-off" logic indicators, their use in arrays offers a wider range of application. An addressable matrix or a series of addressable elements can be formed using LED devices with each diode representing a location (element). This addressable nature and the high resolution which can be achieved by these devices make it possible to construct quite complex alpha-numeric and graphic displays. The semi-conductor nature of the LED offers very high reliability and the life of the display device is more than 100,000 hours. Conversely, the LED type of display requires digital signal processing to obtain the correct form of matrix or element address.

A widely-expressed opinion is that LED devices are unlikely to offer an economical large panel display. However, advances in LED displays are not so much related to semi-conductor

technology, as to the problems of connecting to the device and to the heat dissipation, when operating in an "all on" mode. Whilst the heat problem is solvable, the connection problem seems to dictate a practical limit to the complexity of LED displays.

A typical LED matrix could consist of say, an array of 100 by 100 individual diodes controlled by 200 wires [11]. The representation of characters by selecting from an array of straight lines is illustrated by Fig. 2.1. The characters can also be constructed by selection of dots from a dot-matrix as shown in Fig. 2.2 and Fig. 2.3, which illustrates the alpha numeric LED displays.

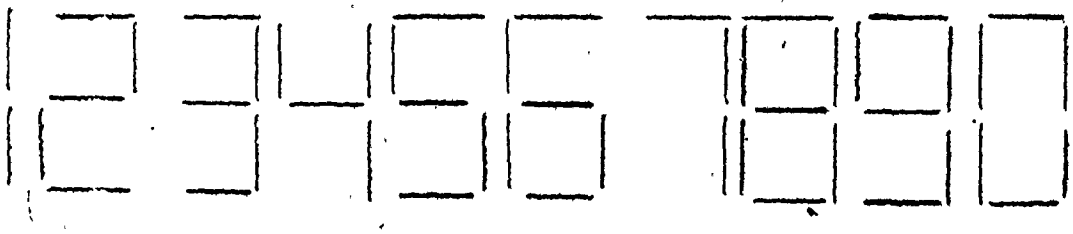
2.2 LIQUID CRYSTAL DISPLAYS

There has been much interest in the application of the light scattering properties of liquid crystals to the displays required in high ambient light conditions. This could be relevant to a number of radar display requirements.

A liquid crystal display is a monochromatic type which is viewed by scattering incident illumination when it is in the 'on' state (liquid crystals do not emit light), and there is no viewed light when it is in the 'off' state. Construction is achieved quite simply, by sandwiching a layer of organic liquid crystal, of approximately 15 μm thickness, between transparent conducting plates typically glass coated on the inner surface with thin oxide. The liquid is normally clear but when a voltage is applied between the plates, turbulence is induced in

(a)

(b)



(c)

Figure 2.1 Seven and nine segments light emitting diode displays.

(a) Seven segment display.
(b) Nine segment display.
(c) Typical figures.

Figure 2.2 Alpha-numeric displays.

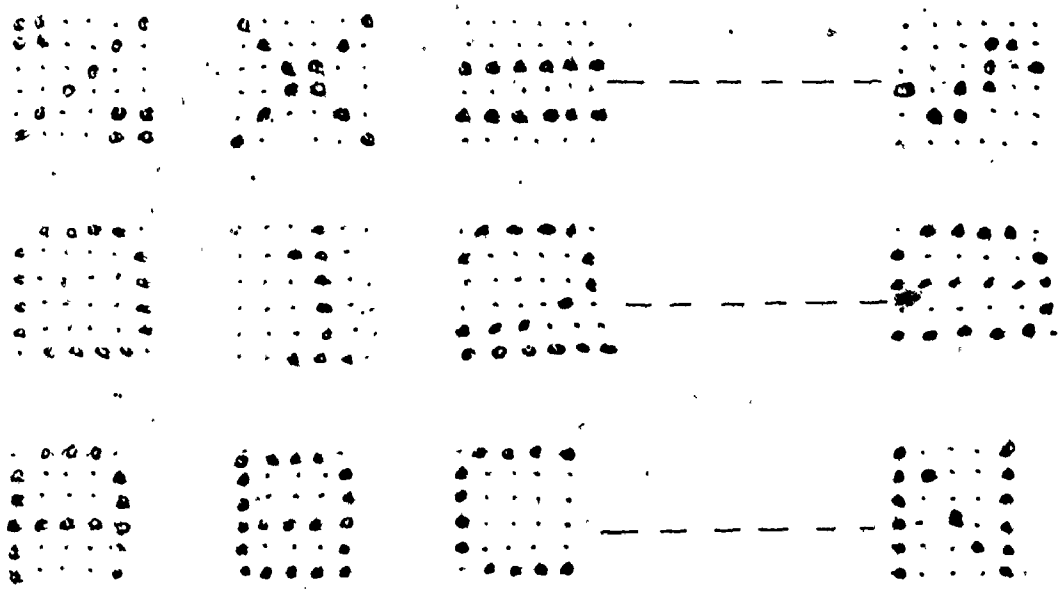


Figure 2.3 Examples of characters construction by selecting dots from a dot matrix of displays.

the liquid, which then appears milky white since it scatters any incident illumination. There are various other effects which may be used, but they all rely on ambient illumination.

The main advantages of a liquid crystal display are that it operates on very low power, it can be viewed under bright lighting, and it can be made as a flat panel for use as display. The device lifetime is greater than 10,000 hours and although ten times less than that of an LED display, is still adequate. The size of the display is only limited by the fabrication requirements of the glass sandwich construction.

The liquid crystal display device is of a digital nature and a display panel can be addressed using the matrix addressing technique. The complexity of this addressing technique limits the size of the display panel. However, new techniques and materials are emerging and within the characteristics represented above, it is likely that liquid crystals may be in use for special radar displays in the near future [13]. The use of liquid crystal displays to construct different characters is the same as LED displays (Fig. 2-1, Fig. 2-2 and Fig. 2-3)

2.3 PLASMA DISPLAYS:

The plasma display panel is a two dimensional array of bistable light-emitting gas-discharge elements, that exhibit inherent memory and are separated from the orthogonal exciting electrodes by thin transparent dielectric materials. This device is capable of receiving, storing, and displaying digital information in a random-access fashion and is one of the addressable

display devices [14].

At present, the plasma display is available only in one color which is red. An example of a commercially available plasma display is an alpha/graphic plasma display panel, which has been specially designed for computer-generated information. The plasma display screen (a matrix panel) is actually a thin glass "sandwich" consisting of two glass sheets, each with parallel conductive electrodes applied to their inner surface. The electrodes on the two sheets, intersecting at right angles, form a matrix of potential intersection. Small glass spacers separate the sheets of glass, and this narrow intervening space is filled with a neon gas mixture. When a voltage pulse is superimposed on any two intersecting electrodes, a gas discharge occurs, forming a spot light. The light dot remains until another voltage signal is applied in a manner to produce cancellation. An additional AC voltage is continuously applied to all electrodes in the matrix panel, providing the "flicker-free" display image with inherent memory.

The display matrix with a total depth of only 0.5 inch is completely transparent, and therefore can be used to display rear projection images. The active display area is 8.5 inches x 8.55 inches with maximum character capacity of 4284 characters. The total number of individually addressable points is 262,144 and the addressing rate is up to 833 characters per second. The display panel is available in the form of 5 x 7 matrix; 7 x 9 matrix; and 10 x 14 matrix. The light spectrum of the plasma display is neon orange. Fig. 2.4 illustrates an alpha/graphic

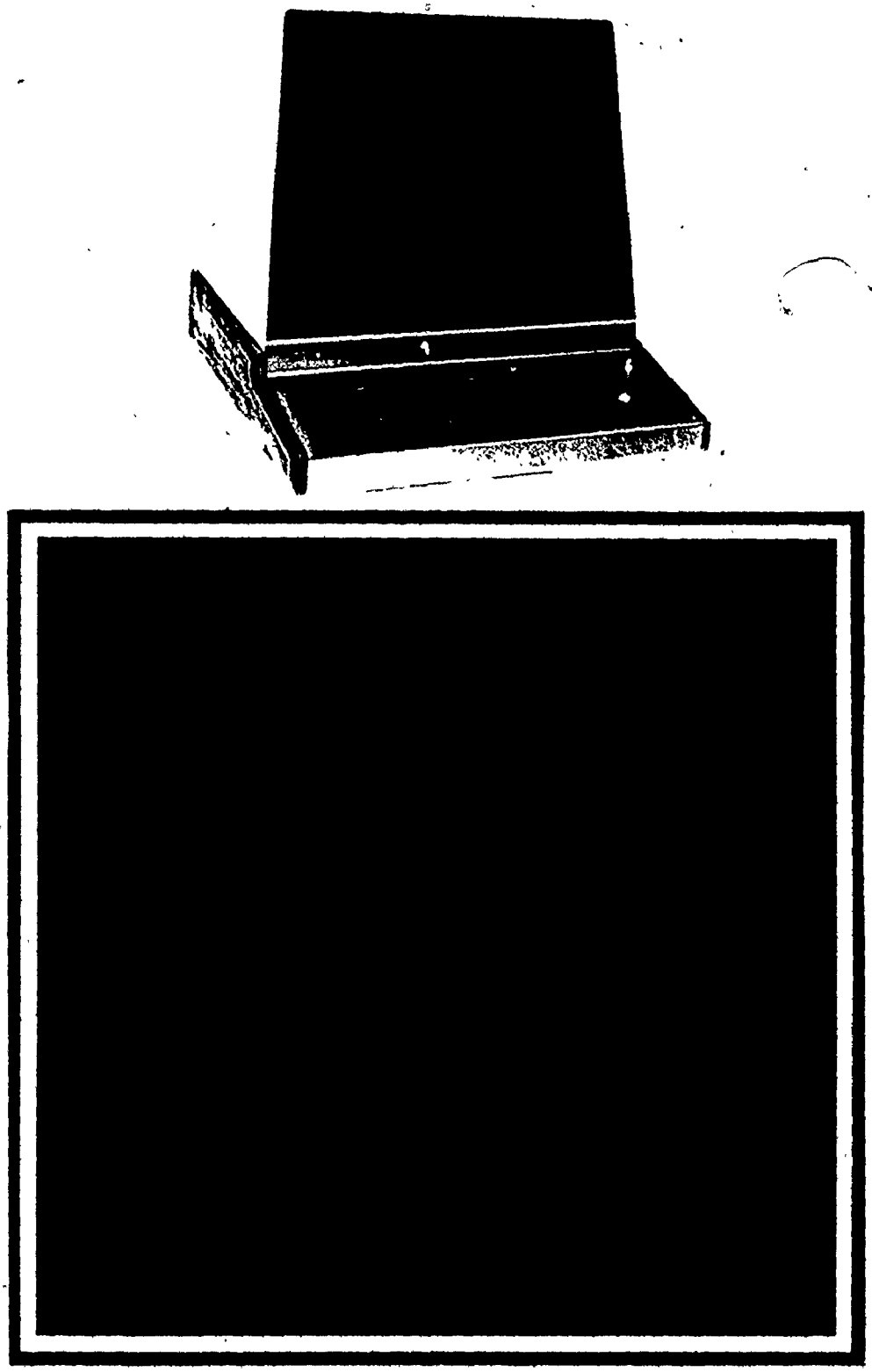


Figure 2.4 A plasma display terminal for computer general information and an example of the display capabilities.

plasma display terminal and examples of the display capabilities [15].

2.4 MONOCHROMATIC CATHODE RAY TUBE DISPLAYS

The cathode ray tube (CRT) is the most common display device used for radar indicators because of its flexibility, resolution, dynamic range, and simplicity of hardware relative to other display techniques. In particular, the CRT display lends itself ideally to the display of large amounts of information in general, and can be used for a wide number of different types of radar information [3, 10, 11, 13, 16-23]. The display has large capacity and is commercially available at relatively low cost.

The CRT consists of an electron-emitting element, or cathode, with an electronic beam-forming and control structure. The electron beam is focused and positioned on a phosphor by either electrostatic or magnetic fields. The energy of the electron excites the particles of a phosphor screen which reemits the energy as light. The color of light and storage (or decay rate of emission) depend on the properties of the phosphor. Brightness of the spot may vary smoothly over the range from zero light output to the maximum available from the tube, which means that the CRT is wholly an analog device [10].

An example of the monochromatic CRT display is the plan position indicator (PPI) which is the most commonly used display in radar. Other examples of the monochromatic CRT displays used

in radar are the A-scan, the B-scan and the raster scan displays. The first two displays will be discussed in detail in Section 3.3.

An example of the monochromatic CRT display is the raster scan black and white (BW) television display. The picture is produced by scanning the face of the CRT. The scanning procedure used employ horizontal linear scanning with the standard scanning pattern including a total of 525 horizontal scanning lines in a rectangular frame having an aspect ratio of 4 to 3. The frames are repeated at a rate usually 30 per second. Two fields are interlaced in each frame; the first containing all the odd-number scanning lines and the second containing all the even-number scanning lines.

The geometry of the standard odd-line interlaced scanning pattern is illustrated in Fig. 2.5. The scanning beam starts at the upper left corner of the frame and sweeps across the frame with uniform velocity to cover all the picture elements in one horizontal line. At the end of each trace, the beam is rapidly returned to the left side of the frame as shown by the dashed line. The horizontal lines slope downward in the direction of scanning. The slope of the horizontal line trace from left to right is greater than the slope of the retrace from right to left. Thus, the beam is continuously deflected downwards as the scanning proceeds. At the bottom of the field, the vertical retrace begins, and the beam returns to the top of the frame to begin the even-numbered field. The vertical "fly-back" time is very fast compared to the trace, but slow compared

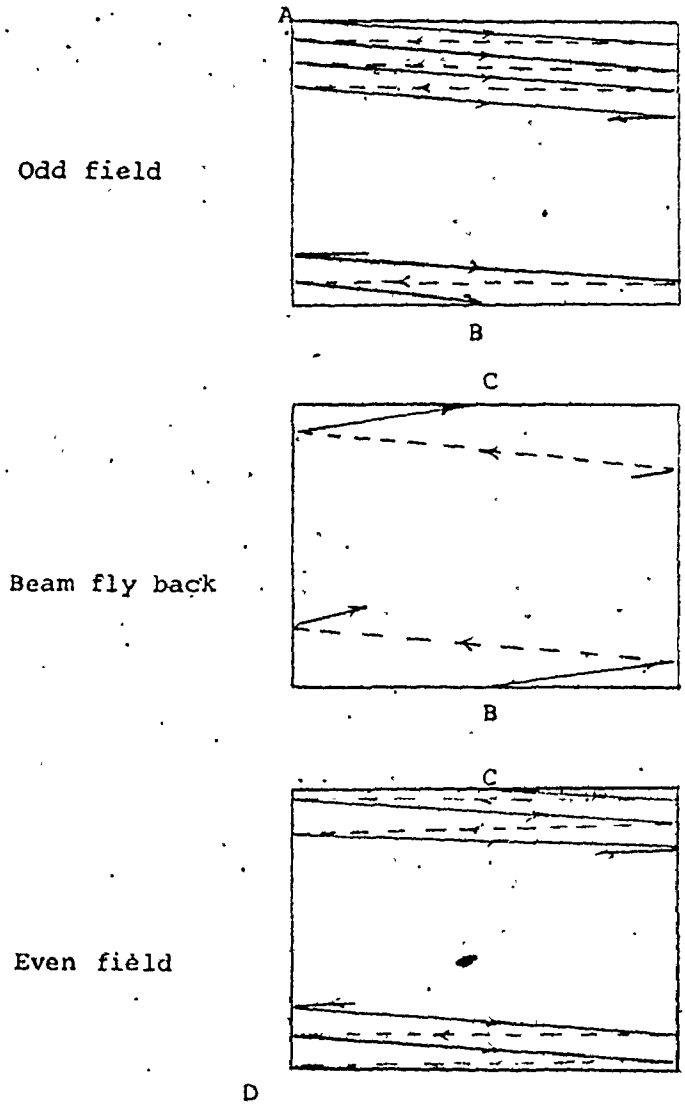


Figure 2.5 The odd and even interlaced scanning procedure for television display.

to the horizontal scanning speed, therefore, some horizontal lines are produced during the vertical fly back.

All odd-number fields begin at point A and all even-number fields begin at point C as shown in Fig. 2.5. With a separation of one-half line, and the slope of all lines being the same, the even-number lines in the even fields fall exactly between the odd-number lines in the odd field [24].

2.5 COLOR TELEVISION DISPLAYS:

Visible light consists of a small interval in the spectrum of electromagnetic radiation with all visible colors contained in a spectrum ranging in wavelength from 400 to 700 millimicrons. Although we name the colors of the rainbow red, orange, yellow, green, blue, indigo, and violet, these are merely the most obvious hues. Several hundred variations in color can be distinguished, even by a comparatively untrained observer.

A beam of white light passed through a prism, splits up into a color spectrum. Conversely, if a color spectrum is passed through a prism, the reverse process takes place and the spectral colors are recombined to form a beam of white light.

A beam of white light can also be formed by combining a minimum of three colored lights, which are called additive primaries. The most useful additive primaries are red, green and blue, and these are the primary hues that are utilized in color television. These three primaries allow the formation of the maximum range of hues when blended in various proportions. Additive primaries must not be confused with the subtractive

primaries used in printing processes and in paintings. Subtractive primaries are viewed by reflected light, and the most useful subtractive primaries are red, yellow, and blue colors.

Technically, white is not a color, but rather is light that is free of color. Black is defined as the absence of light [25].

The Color CRT used for the color television monitor, employs three independent guns, called the 'red', 'green' and 'blue' guns. Three input signals are applied to them and controlled by the horizontal and vertical deflection systems. All of the guns produce an electron beam, that is focused to the phosphor screen such that each beam produces one of the three colors at certain point, where the mixing of the three colors forms other colors.

Up to now, the color television monitor is the only display device which can provide a large number of colors, a large capacity and a relatively low cost. In addition, the color television monitor is recommended, in most of the cases, for the presentation of large amounts of information in color [3, 11, 12, 16].

CHAPTER 3

AIR TRAFFIC CONTROL RADAR AND RADAR DISPLAYS

3.1. FUNDAMENTALS OF PULSED RADAR

Radar is an electromagnetic technique for detecting and locating objects. It operates by transmitting a particular type of electromagnetic waveform and detecting the nature of the echo signal. The word radar is a contraction of the word radio detection and ranging.

A pulsed radar [19, 20, 26, 27] transmits a relatively short burst of electromagnetic energy, after which the receiver is turned on to listen for the echo. The echo not only indicates that a target is present, but the time that elapses between the transmission of the pulse and the reception of the echo is a measure of the distance between the radar and the target which is called the range (R). Comparison between the returned signal and the transmitted signal also yields information about the size and relative motion of the target with respect to the radar.

The basic principles of a pulsed radar system may be demonstrated by describing the operation of a typical system, shown by the block diagram Fig. 3.1. The synchronizing generator generates a series of narrow sync pulses, or timing pulses, at a rate called the pulse repetition rate (Fig. 3.2 a). The time interval, T_r, is called the pulse repetition interval (PRI), and

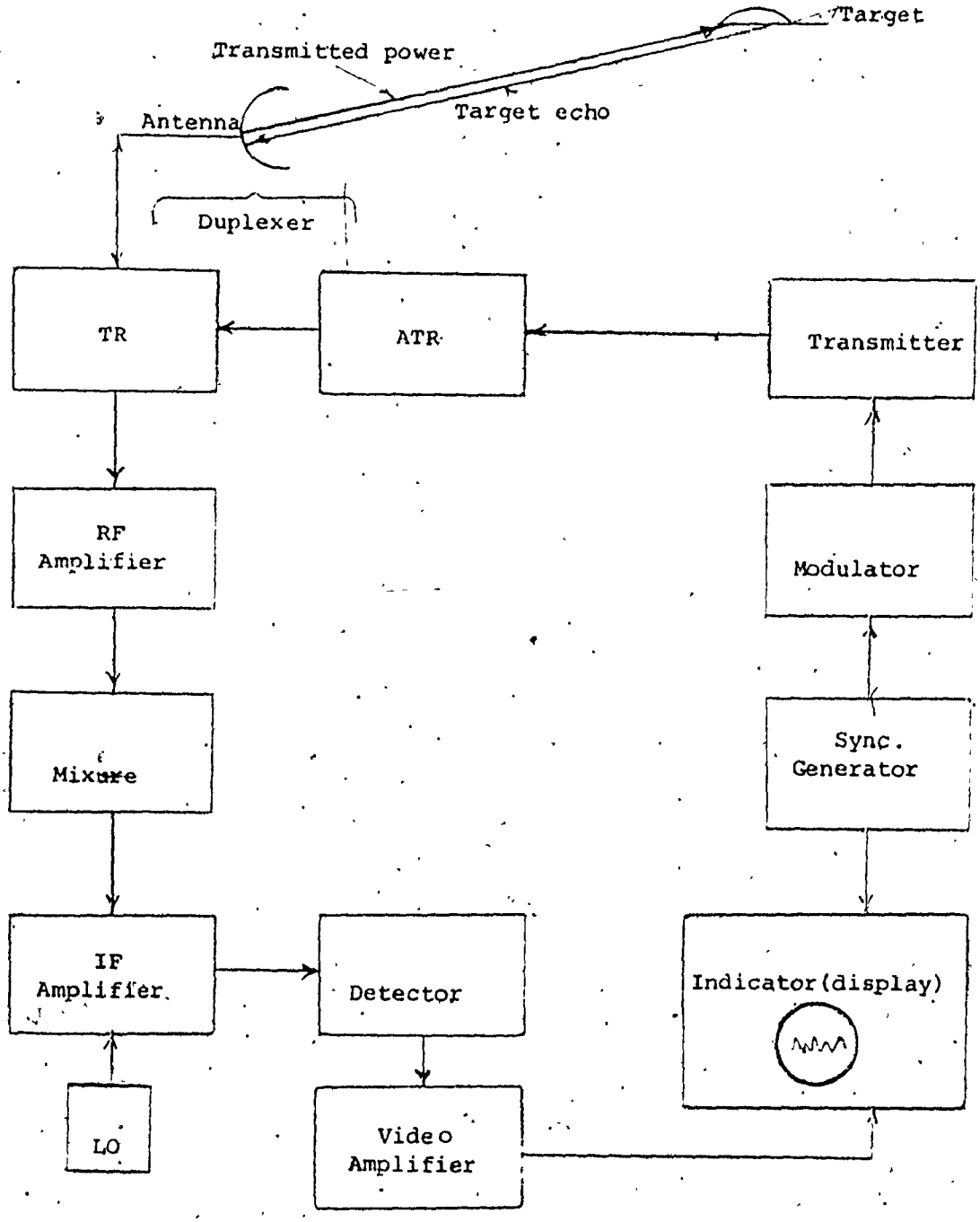


Figure 3.1 Block diagram of a pulsed radar.

the corresponding frequency is called the pulse repetition frequency (PRF). These sync pulses turn on the modulator which pulses the transmitter with a series of pulses with certain pulse width T as shown in Fig. 3.2.b. For example, a pulsed radar for aircraft surveillance may generate a repetitive train of short pulses, each of approximately one microsecond duration, at a PRF of several hundred per second. If an accurate range measurement is required, the transmitted signal should occupy a wide spectral bandwidth, as does, for example, a short pulse.

The transmitter generates a modulated RF pulse (Fig. 3.2.c) and sends the pulses through the transmit-receive switch to a narrow beam antenna where they are radiated. The narrow beam characteristic of the radar antenna not only permits more energy to be concentrated on the target but also permits a measurement of the target azimuth because of the localization of the energy in space. A common antenna is usually used for both transmitting and receiving.

Reflecting objects, or targets, intercept and re-radiate a portion of the radar signal and a small amount returns in the direction of radar. Some of the returned signal is collected by the antenna and detected by the receiver.

If the radar transmitted power is denoted by P_t, and the antenna has a transmitting gain equal to G_t, then the power density at a range R from radar is equal to $(P_t G_t / 4\pi R^2)$. Assuming that the target cross section is σ, then the power re-radiated in the direction of the radar is $(\sigma P_t G_t / 4\pi R^2)$. This means that the

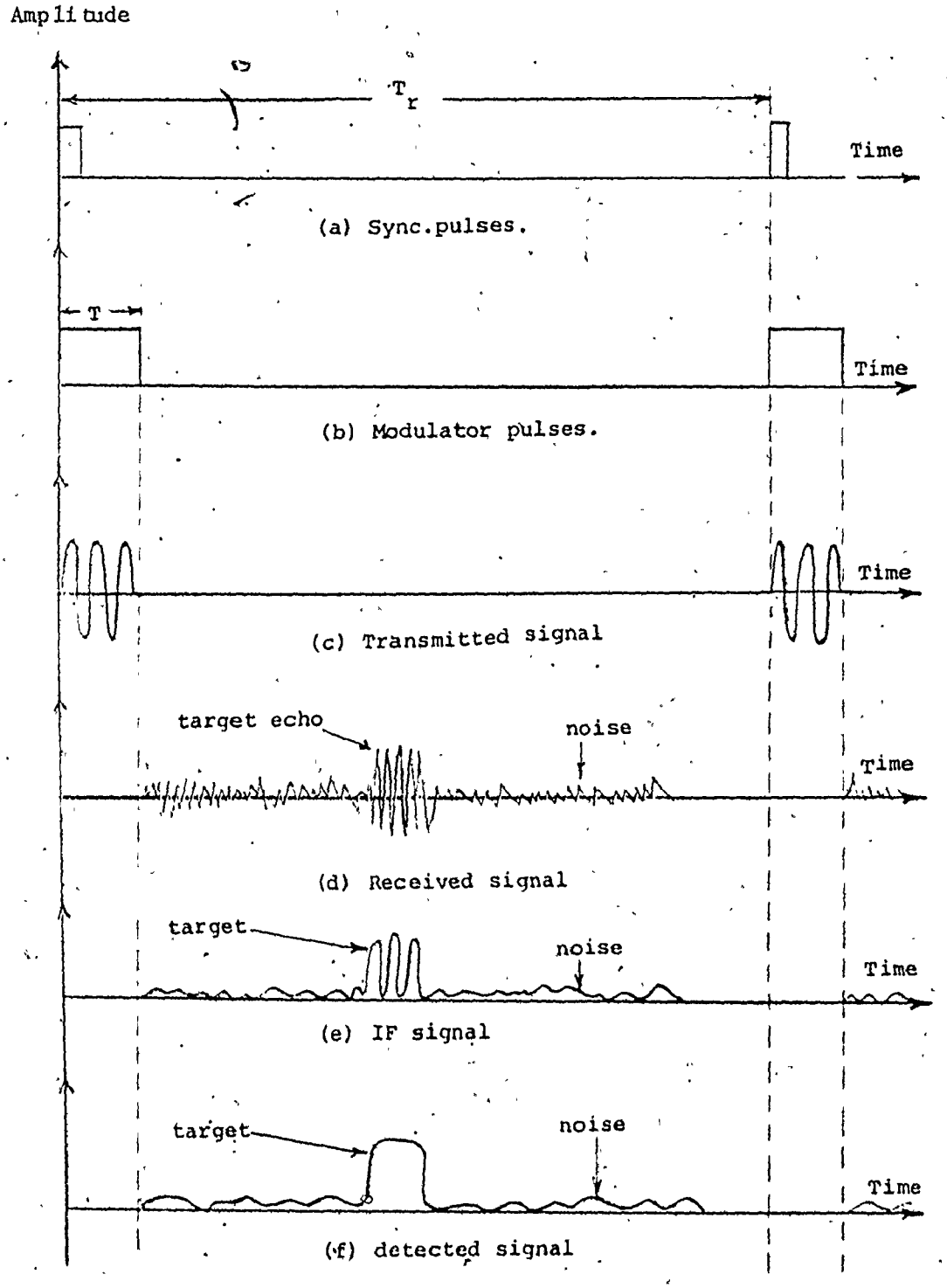


Figure 3.2 Typical pulsed radar timing diagram (same time scale).

reflected power density at the radar antenna is $(\sigma P_t G_t/(4\pi R^2)^2)$. Finally, if the antenna has an effective aperture area equal to A_r, then the received power (P_r) is given by the equation:

$$P_r = \frac{P_t G_t \sigma A_r}{(4\pi R^2)^2} \qquad (3.1)$$

This equation is one form of what is called "radar equation" which can take other different forms such as:

$$R^4_{max} = \frac{P_t G_t \sigma A_r}{(4\pi)^2 S_{min}} \qquad (3.2)$$

where R_{max} is the maximum radar range and S_{min} denotes the minimum detectable signal power of the radar receiver. R_{max} is defined as the distance beyond which a target can no longer be detected.

Another form of the radar equation can be obtained by relating G_t and A_r in the case of using a common antenna for both transmitting and receiving. If λ is the wave length of the transmitted signal, then $G_t = 4\pi A_r/\lambda^2$, since the effective aperture area is the same for transmitting and receiving. By introducing this into equation (3.2), another form of the radar equation can be obtained:

$$R_{max} = \frac{P_t A_r^2 \sigma}{4\pi \lambda^2 S_{min}} \qquad (3.3)$$

The above equations are actually simplified forms for describing the range performance which do not include the various losses which can occur in a radar. The mirimum detectable signal can be expressed in terms of the signal-to-noise ratio (S/N) required for reliable detection and the receiver noises. If P_n is the power level of the noise in the receiving system, then the signal-to-noise power ratio can be defined as:

$$\frac{S}{N} = \frac{P_r}{P_n}$$

which implies

$$P_r = \left(\frac{S}{N}\right) P_n$$

and the minimum value of P_r that can be detected is the value of S_{min} which means that S_{min} can be expressed as:

$$S_{min} = \left(\frac{S}{N}\right)_{min} P_n$$

A fast acting switch called the transmit-receive (TR) switch (Fig. 3.1) disconnects the receiver during transmission. After the passage of the transmitted signal, the TR switch reconnects the receiver to the antenna. Another switch called anti-transmit-receive (ATR) switch acts on reception to channel the received signal power in to the receiver. In the absence of the ATR, a portion of the received power would be dissipated in the transmitter rather than enter the receiver. The TR and the ATR are together called the duplexer. If separate antennas are employed for transmitting and receiving, a duplexer may not be

necessary if the isolation between the two separate antennas is sufficiently large.

The RF amplifier is the first stage of the radar receiver. The mixer and local oscillator (LO) convert the RF signal to an intermediate frequency (IF) since it is easier to build high gain narrow band amplifiers at the lower frequencies. A typical IF amplifier might have a centre frequency of 30 or 60 MHZ and a bandwidth of one or two MHZ.

The received and IF signals are illustrated by Fig. 3.2 (d, e, f). The RF pulse modulation is extracted by the detector and amplified by the video amplifier to a level where it can operate the indicator. Sync pulses are also applied to the indicator. Target positional information is obtained from the direction of the antenna and is used to properly display the co-ordinates of the target location. Two of the most common forms of indicators [19, 20] using the CRT are the A-scope and the plan position indicator (PPI), as described in Section 3.3.

3.2 AIR TRAFFIC CONTROL RADAR:

The air traffic control radar is a pulsed air search radar which is assigned to cover a given volume of space and is expected to detect and locate aircraft within this volume and those entering it [26].

The airport and airways surveillance radar (AASR) is one kind of an air traffic control radar. A typical example of AASR system is the Raytheon Company Airport and Air Ways Surveillance Radar AASR-1 [28, 29]. AASR-1 system is an air search radar

system with a maximum range of 150 miles and a frequency range of 1220-1350 MHZ. The pulse repetition rate is 400 pulses per second with a pulse length of a 2 micro seconds. The search for returning echoes is accomplished by continuous rotation of the antenna at one of several speeds such as 6, 9 and 12 rpm. The antenna beamwidth at half-power points is 1.35 degrees horizontal and 6.50 degrees vertical.

A second example of air traffic control radar is the airport surveillance radar (ASR). Usually, ASR has less range than AASR since ASR is assigned for the detection and location of aircraft around the airport only, but the operating environment of AASR includes airways in addition to the airport. A typical ASR is the ASR-803 which is also a Raytheon Compary radar [29]. The frequency range is 1250-1350 MHZ and the pulse repetition frequency is 800 HZ with a pulse length of 1.1 microsecond. The antenna rotation speed is 12 rpm and the antenna beam width is 1.25 degrees horizontal. The radar maximum range for aircrafts is 80 miles.

3.3 COMMON DISPLAYS FOR RADAR:

The purpose of a radar display is to present the information contained in the radar echo signal in a form suitable for interpretation by the operator. The display may be connected directly to the video output of the radar receiver. However, if the information available from the radar signal is obtained at a rate which is greater than the operator can assimilate, automatic data processors such as digital computers may be needed to

interpret the radar data, and display only the condensed information. This is what is called the synthetic display of radar signal [10, 30] . Signals which are displayed when they become available are called real time signals.

The most common form of radar display is usually some form of CRT. There are two basic methods of displaying information on a CRT. The first method is the deflection modulated CRT such as the A-scope. In this type of display, targets are indicated by the deflection of the electron beam. The second display method is the intensity-modulated CRT. An example of the second type is the PPI scope which is normally dark in the absence of a target, and the target is indicated by intensifying the beam and presenting a luminous spot on the face of the CRT. In general, deflection modulated scopes are better adapted to making range or angle measurements. On the other hand, intensity-modulated displays have the great advantages of presenting data in a convenient and more easily interpreted form.

The various forms of displays which are used in radar systems [10, 13, 19, 20] are illustrated in Fig. 3.3. The common displays are the PPI, the A-scope and the B-scope. The PPI, which is the most commonly used display in radar, maps the target in angle and range on a polar display. The target echo amplitude is used to modulate the electron beam intensity as the electron beam is made to sweep outward from the centre with range. The beam rotates in angle in response to the antenna position and targets are indicated as bright spots (called blips). The A-scan display is similar in operation to the normally-used

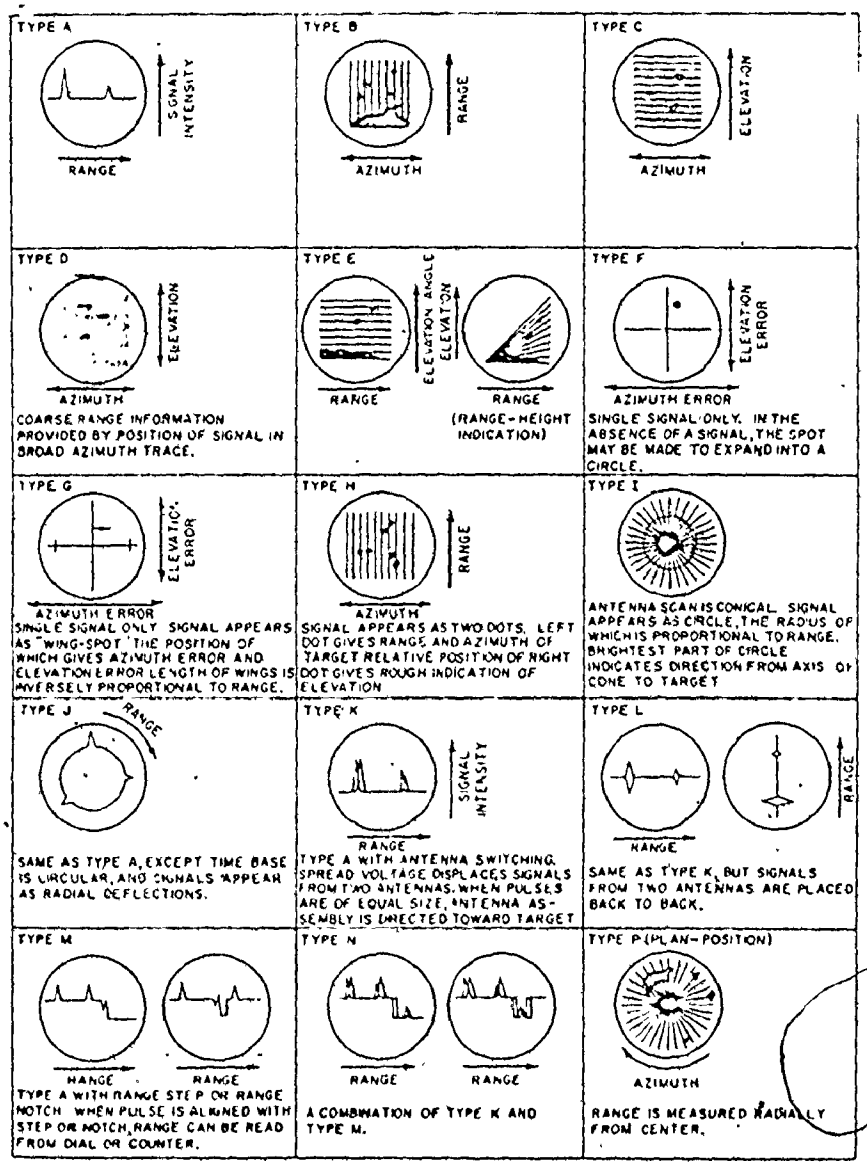


Figure 3.3 Common CRT radar displays.

oscilloscope. It displays the target amplitude (y-axis) vs-range (x-axis), as shown in Fig. 3.3, and no angle information is shown. Signals are applied to the vertical deflection circuit, so that radar targets appear as vertical spikes along a horizontal line, which represents the range. The B-scan display is an intensity-modulated display and it is sometimes used with sector scanning radar. The vertical deflection is proportional to the range and the horizontal deflection is proportional to the azimuth. Targets are presented as bright spots (Fig. 3.3)

3.4 COLOR-CODED TELEVISION DISPLAY FOR RADAR:

3.4.1 Color-Coding Technique:

A color-coding technique can be designed to encode the signal amplitude to a set of different distinguishable colors. Each color can represent an interval on the amplitude scale depending on the code size and the type of application. A possible technique is to divide the signal level between the zero and the maximum possible amplitude into equal intervals, and to assign a color for each interval. This is the same as digitizing the signal amplitude with each color corresponding to a digital number, and the number of bits being determined by code size. For the binary number system, 2^n colors (code size) corresponds to n-bit binary numbers starting at zero and rangingupto$(2^n - 1)$ as the signal level increases from zero to the maximum value. The set of colors employed in the color-coding technique is called the "color code".

3.4.2 Color-Coded Display

A display system which applies the previously described color coding technique, using a color television monitor, is presented in this thesis. The color-coded display system employs sixteen different colors as the color code. The design and construction of the system is described in Chapter 4, and the presentation of radar signals by the display system is demonstrated in Chapter 6. Fig. 3.4 illustrates the color coding technique applied to radar signal and one selection for the color code.

The wide range of colors provided by the color television monitor makes it easy to select the best sixteen distinguishable colors available. A unique color represents every sample of the input signal (Fig. 3.4). This provides the ability to recognize the level interval in which the signal belongs at certain time or range. This range, in turn, corresponds to positions on the raster scan of the color television monitor.

3.4.3 Advantages of Color-Coded Display:

The color-code can be selected and arranged to suit the nature of the displayed information, or to reflect certain features to make the data interpretation easier. This concept is illustrated by the example shown in Fig. 3.5 where the low signal levels are represented by dark colors such as black, purple and blue, while the high levels are represented by the bright colors such as white, orange, red and yellow. This aids in the discrimination between noise and targets since noise will

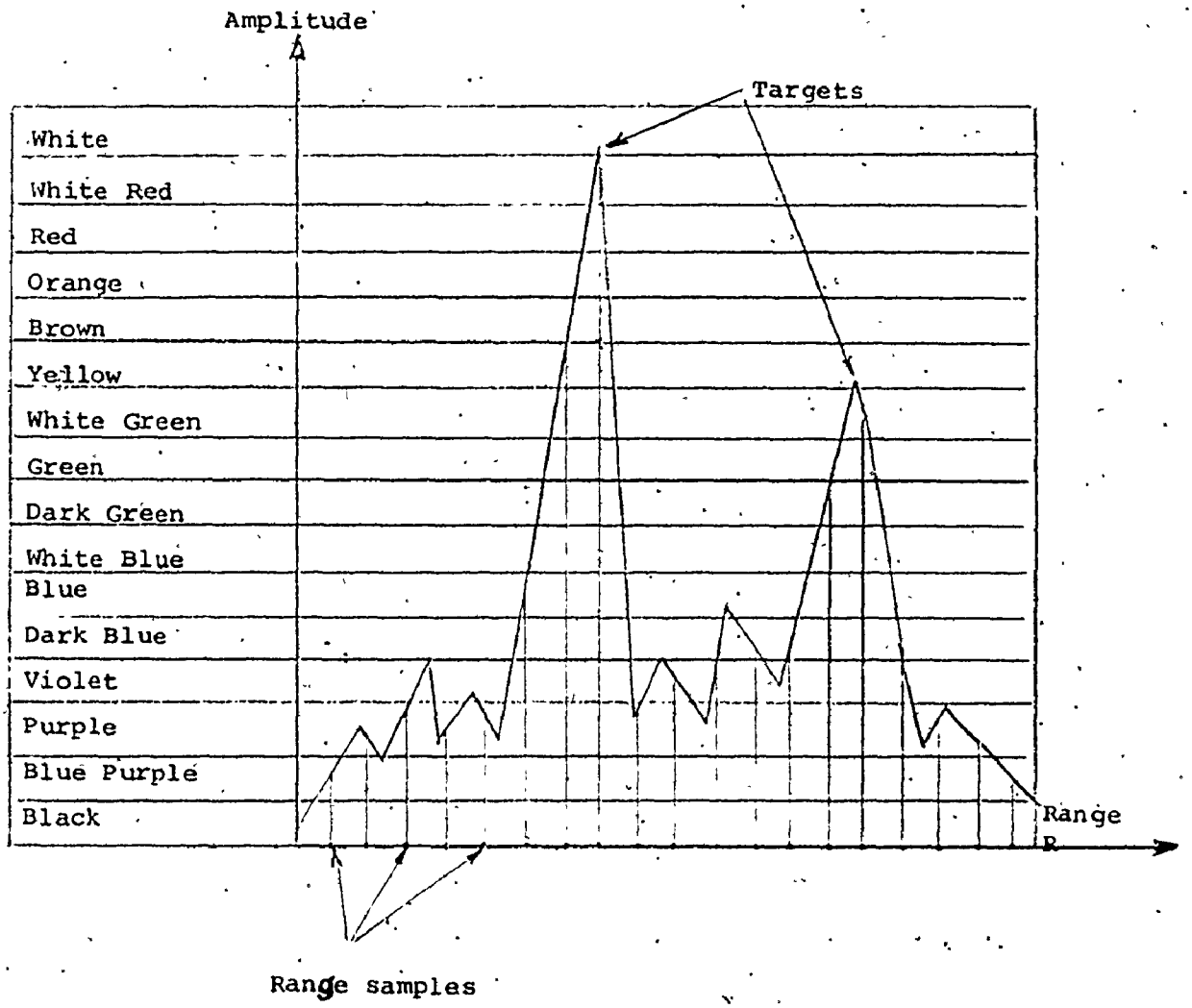


Figure 3.4 Color-coding technique for radar signal and an example of the color code

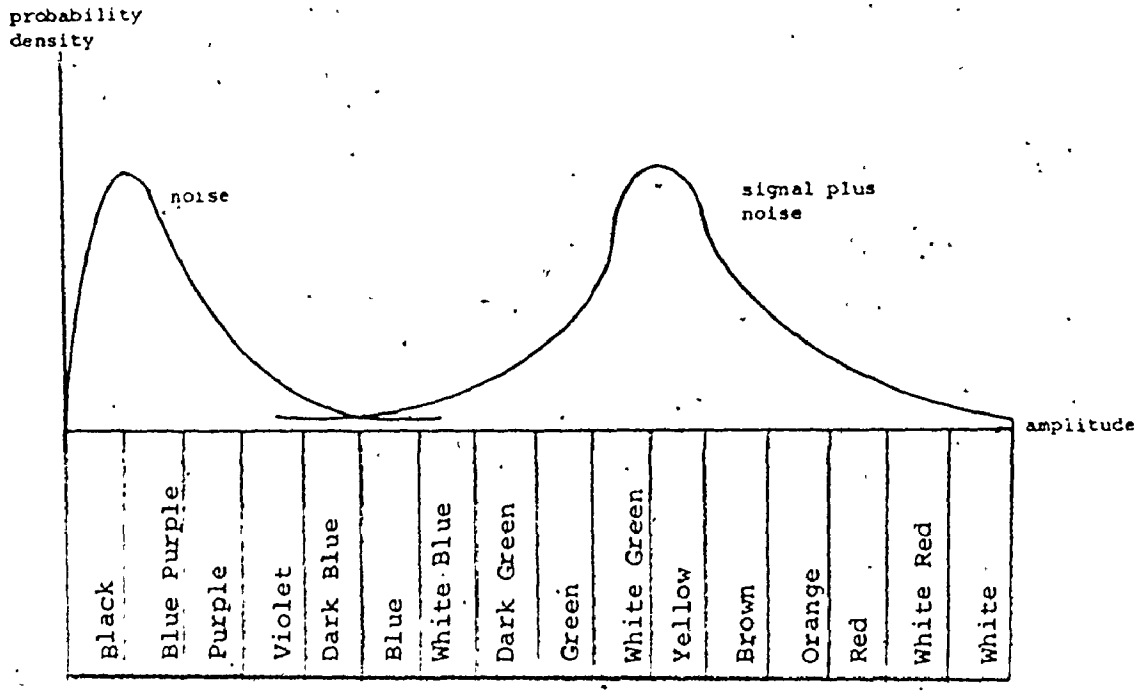


Figure 3.5 Probability density functions for typical radar signal with color coding showing sixteen colors.

be represented by a known set (range) of colors, and signal due to target will fall in a different range of colors.

This technique, with the previously mentioned advantages, can improve the performance of radar systems especially air traffic control radar. It makes the detection and identification of aircraft, in the existence of noise, easier since targets and noise are represented by colors which belong to different color ranges. In addition, the use of color in the presentation of radar information assists in making data interpretation and operator response faster which is essential in air traffic control radar.

CHAPTER 4

THE DESIGN AND CONSTRUCTION OF THE COLOR-CODED DISPLAY SYSTEM

4.1 SYSTEM FUNCTION AND BASIC CONCEPTS:

The function of the display system (Fig. 4.1) is the synthetic display of signals from sources such as radar, sonar and meteorological satellites, in real time, employing a color-coding technique. The signal is encoded in amplitude using sixteen different colors to present information on the raster scan of the color television monitor. Features are added to the system to display the colors employed in color coding in order to compare the displayed data with the color code.

The interfacing function between the input signal, in real time, and the display is performed by five major subsystems (Fig. 4.1). These subsystems are input-memory interface; addressing and timing circuit; random access memory (RAM) system; memory-display interface and sync generator. The memory stores data and allows the interface between the real time processes and the synthetic display of data. The other mentioned subsystems perform three duties: 1) it controls the flow of data from the input to the memory and from the memory to the output; 2) it provides the interfacing signals required between the memory and the external circuitry; and 3) it color encodes

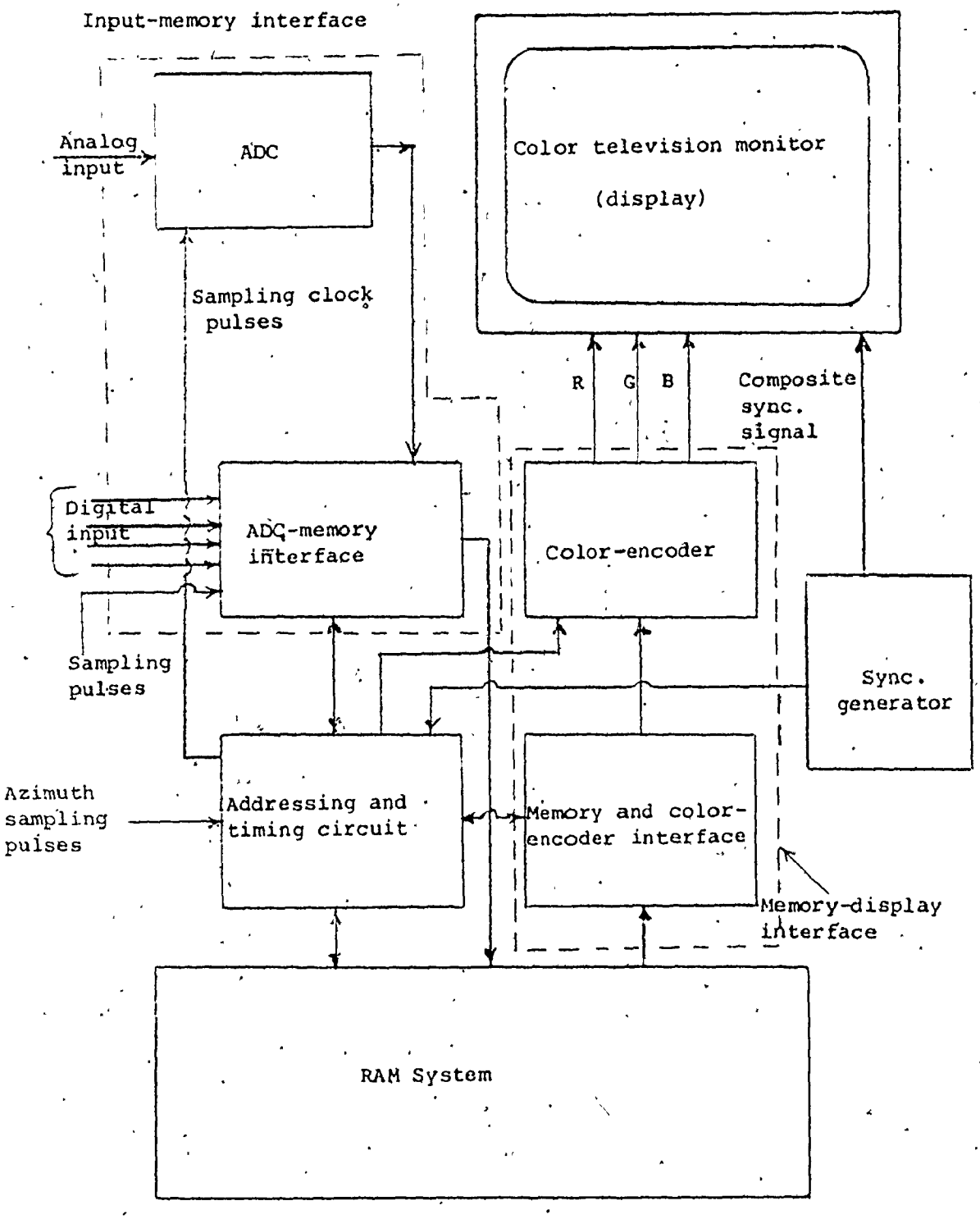


Figure 4.1 Block diagram for the color-coded display system for radar signal.

the input signal amplitude according to certain selectable coding arrangement.

Digital circuitry and digital random access memory are emplcyed in the system design. The digital system, in this type of application, is capable of providing a picture of definable quality and within the constraints imposed by storage capacity, theoretically, any required resolution can be achieved. The digital memory is perfectly uniform and the stored signal can be read out at high signal to noise ratio. With all these advantages, the digital system provides a high quality stored display [22].

The flexibility of digital storage allows the same memory to be alternately used for different resolution, codes and different system modes. Also, a fast digital memory makes the transformation of the input data format to the TV raster scan format a straight forward process.

Digital signal processing can be achieved if a processor can communicate with the stored data. This can be attained in the display system by introducing a microcomputer which receives instructions by the operator. A selectable signal processing technique can be applied by executing one of several stored routines. The microcomputer can also contribute by controlling the system and adding more flexibility to the system function. This is because the digital system is easy to expand and simple to integrate with existing computer installations [31].

4.2 SYSTEM DESCRIPTION AND OPERATION

4.2.1 General Description

A detailed block diagram of the color-coded display system is shown in Fig. 4.1. The system incorporates a color television monitor as a display and a large scale RAM system. The input-memory interface is divided into two blocks, the analog to digital converter (ADC), and the ADC-memory interface. The color-encoder and the memory-color encoder interface perform the function of the memory-display interface. The addressing and timing circuit is interconnected with the other blocks to address the stored data and control the system operation. The sync generator supplies sync pulses to the color television monitor, the memory-color encoder interface, and the addressing and timing circuit.

The input real time signal can be either in analog or digital format. In the first case, it is sampled and digitized by the ADC at a selectable sampling rate. This sampling rate is controlled by sampling clock pulses fed to the ADC. In the second case, digital data and its associated sampling clock pulses are applied directly to the ADC-memory interface.

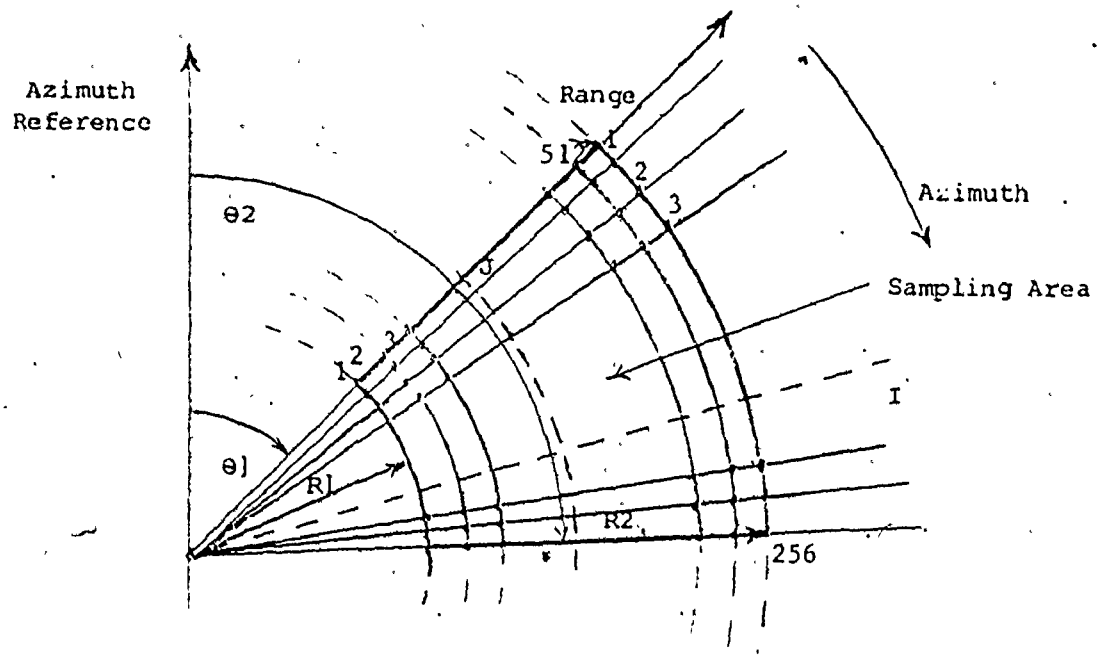
The ADC-memory interface facilitates the storing of data fed to the memory with the help of the addressing and timing circuit. The latter performs the addressing function for both writing data in, and reading data from the RAM system. In addition, the addressing and timing circuit controls the switching between different modes of operation and provides the required interfacing signals to the memory.

The direct memory access (DMA) technique is used to store the data in the RAM system. The same technique is used to read the data from the RAM system through the memory-color encoder interface. The data are then fed to the color-encoder which encodes the data into a set of colors, called the color code, which represents information on the raster scan of the color television monitor. The output format is described in details in the next section.

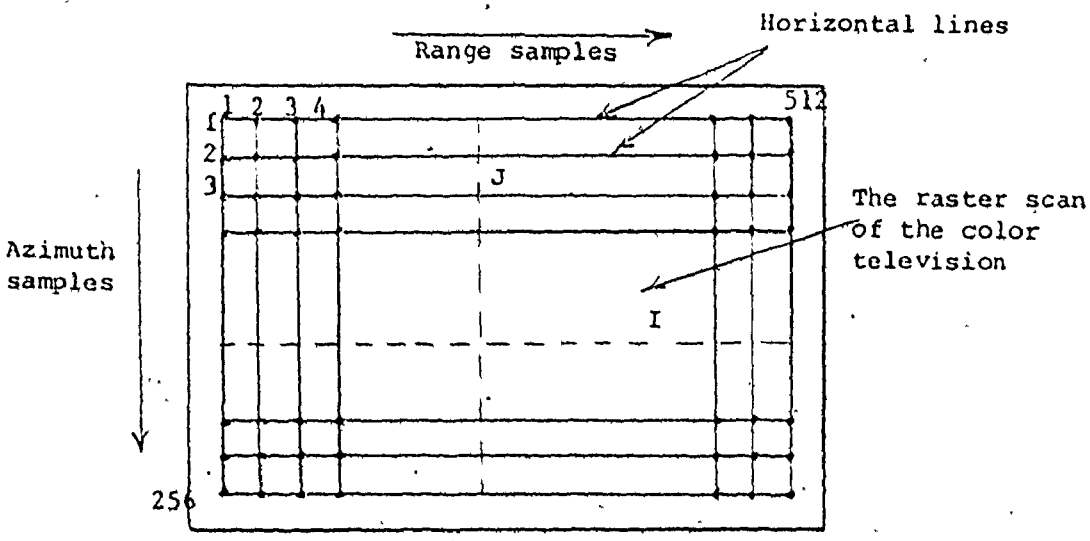
A sync generator provides the required scanning sync signals for the color television monitor, and clock pulses controlling reading the data from the memory (system sync). It also contributes in generating general reset pulses for the display system.

4.2.2 System Capacity and Sampling Area

The system capacity is defined as the total number of input samples represented on the raster scan of the color television monitor. In the case of displaying radar data, the capacity is equal to the number of azimuth segments multiplied by the number of range samples as shown in Fig. 4.2. The area covered by these samples is called the sampling area, which is bounded by the range values R_1 and R_2; and azimuth values θ_1 and θ_2. This sampling area can be expanded and presented on the raster scan of the color television monitor with the azimuth segments represented by horizontal data lines (horizontal data lines means the horizontal lines representing different information on the raster scan of the color television monitor).



Sampling area boundries



Representation of radar signal samples on the raster scan of the color television monitor.

Figure 4.2 Sampling area and output format.

The range samples (4-bit words) in each azimuth segment are represented by data points on the corresponding data line (Fig. 4.2). Thus, the system capacity determines the maximum memory capacity requirements and the display resolution. (The display resolution is defined as the number of data horizontal lines multiplied by the number of data points of every data line.)

The maximum capacity of the display system described here is 512 x 512, but construction was based on capacity of 256 x 512 as determined by the available memory capacity. The 256 azimuth segments are represented by 256 horizontal data lines. Data represented by horizontal lines are repeated for the odd and even interlaced fields. Thus the two fields are identical.

Another input signal, which is called azimuth sampling pulses is applied to the system to control the sampling process. This signal is generated from radar system timing pulses illustrated by Fig. 4.3. These pulses are the azimuth reference pulses (ARP) and the radar sync pulses (transmission pulses). The radar sync pulses are fed to an external circuit [29] which can be used to reduce the frequency by any selectable integer as described later. This output, from the circuit, is referred to as the modified radar sync pulses. The external circuit is also used to generate the azimuth sampling pulses which sample the azimuth sector between the values θ_1 and θ_2 into equiangular segments (The number of azimuth segments in

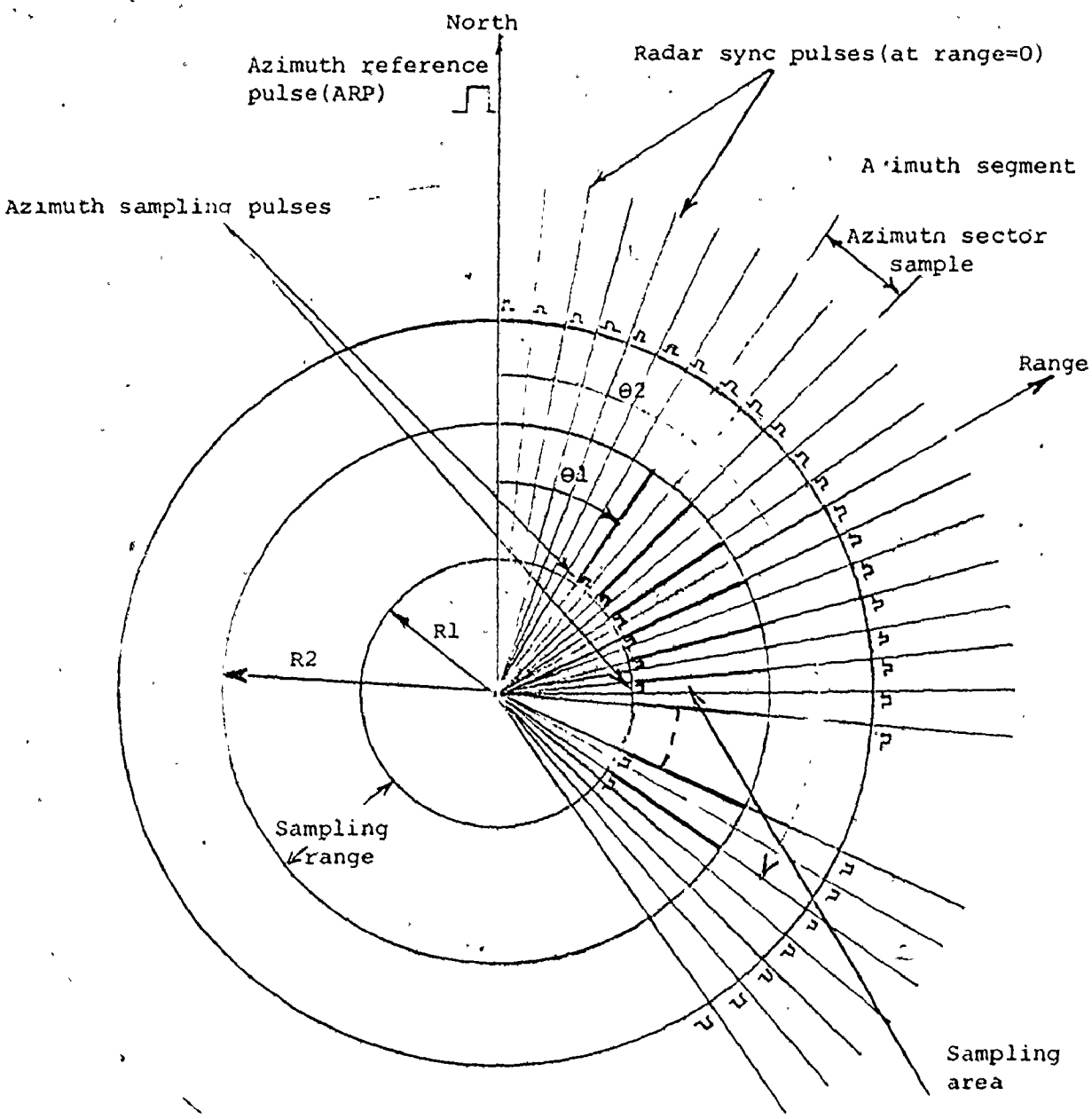


Figure 4.3 Radar sync pulses, azimuth sampling pulses and sampling area.

our case is 256). The azimuth sampling pulses are generated such that they are synchronous with the modified radar sync pulses but delayed by the time corresponding to range R_1.

The selectable integer mentioned above depends on the required increment of angle between two consecutive azimuth segments, and on the speed of the rotation of the radar antenna. Also, the antenna beamwidth affects the selection of the value of the increment of angle between the azimuth segments. As an illustrative example, let the radar PRF be 1000 pulses/second and the antenna beamwidth be 2.4 degrees. If the speed of rotation is 60 degree/second, then the antenna will rotate an angle of $\frac{60}{1000} = 0.06$ degrees, between any two sync pulses (two transmissions). Thus, the beamwidth is 40 times the increment 0.06 degrees. In other words, 40 transmissions will occur while the radar antenna beam crosses certain point. If the increment between azimuth segments is chosen to be half that of the antenna beamwidth (i.e. the beam hits each point twice) then the modified radar sync pulse frequency must be $\frac{1}{20}$ that of the radar sync pulses. This corresponds to dividing the radar PRF by the integer number 20.

For every azimuth segment, the range between the value R_1 and R_2 is sampled 512 times at the rising edges of the sampling clock pulses. The relation between sampling clock pulses and azimuth sampling pulses is illustrated in Fig. 4.4. The rate of the sampling clock pulses is adjustable according to the band width of the input signal in order to satisfy the

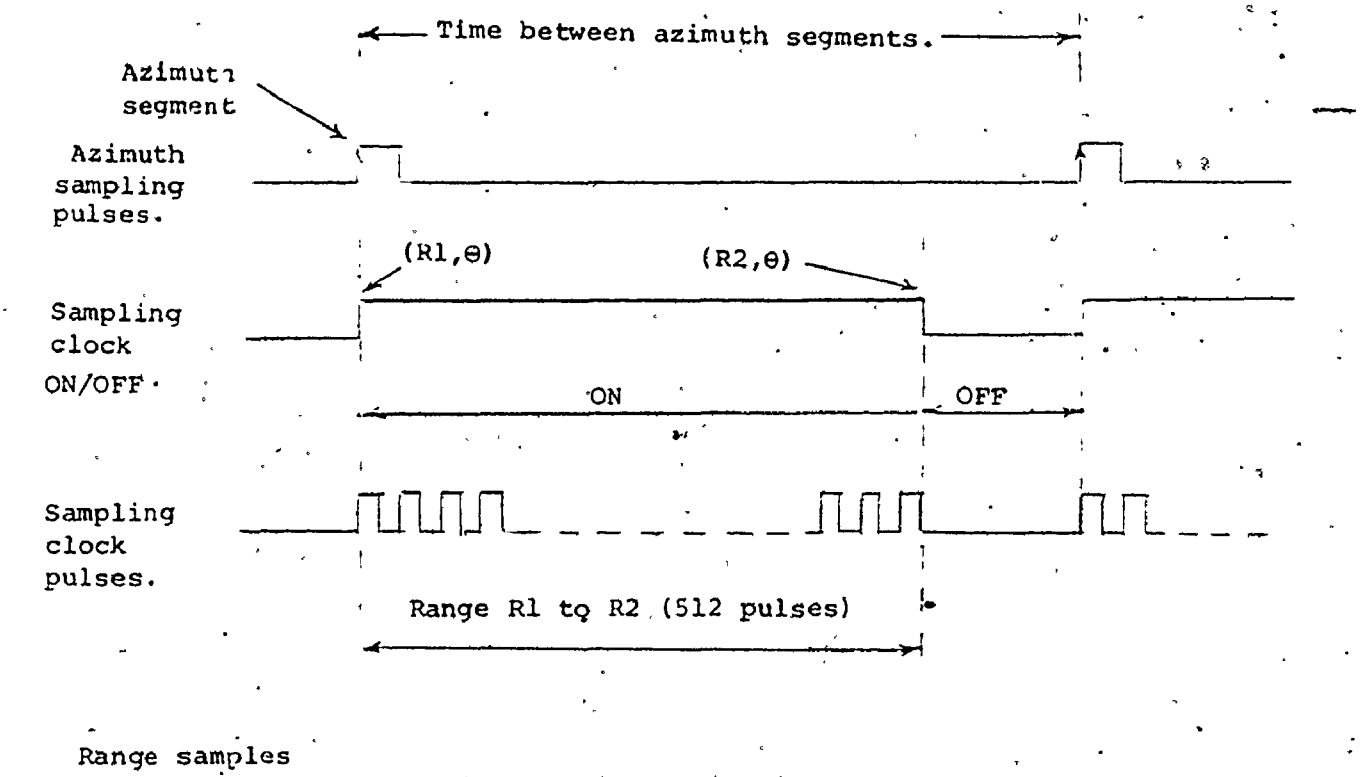


Figure 4.4 Sampling in range.

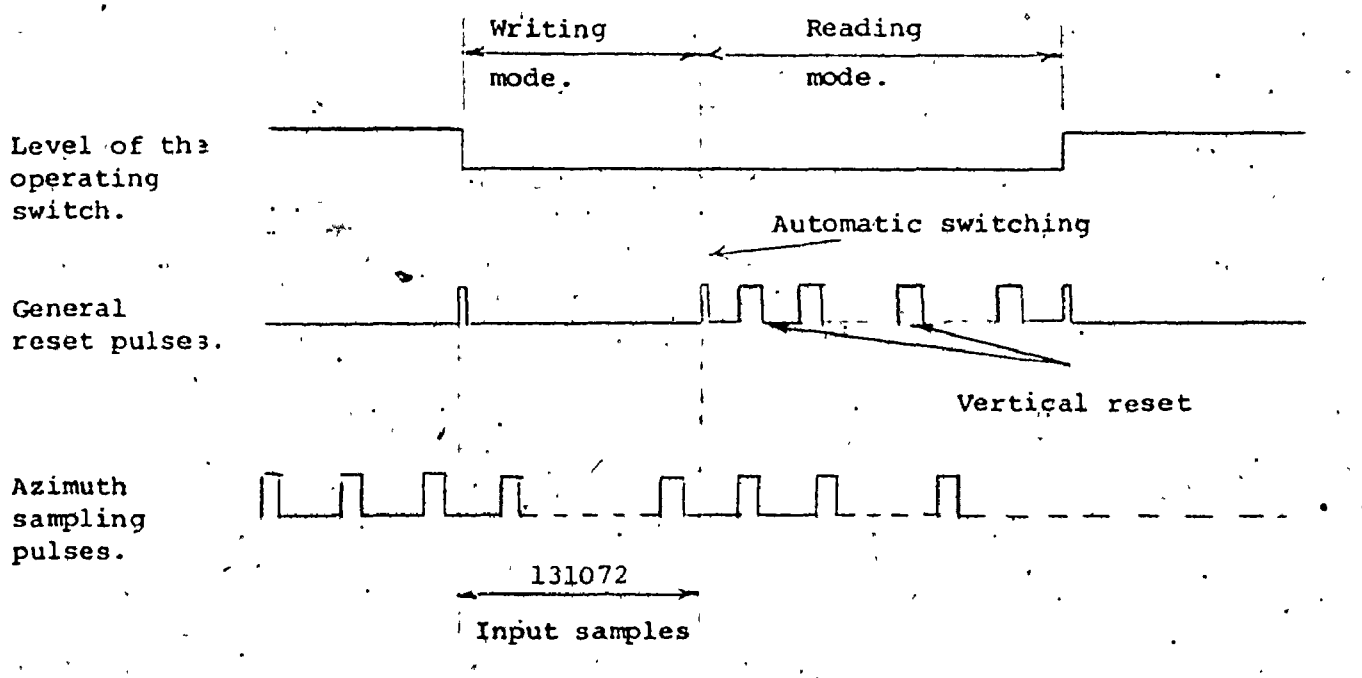


Figure 4.5 Switching between modes of operation and its relation with azimuth sampling and general reset of the display system.

sampling theorem [32].

The sampling area boundaries are determined and specified to the display system by the ARP, the azimuth sampling pulses, and the sampling clock pulses. This is since the delay time between the azimuth sampling pulses and the radar sync pulses determines the value of R_1. Also, the azimuth value at which the azimuth sampling pulses starts is the value of θ_1. The angle θ_2 is equal to the azimuth value corresponding to the last pulse of the azimuth sampling pulses. The range R_2 is determined by R_1 and the time required to store 512 range samples in the system (this time corresponds to certain range value), which depends on the rate of the sampling clock pulses. This means that the sampling area can be changed by adjusting the delay and rate of the azimuth change pulses and the rate of the sampling clock pulses, for the same system capacity. In addition, the sampling area can be moved in radial and angular directions by changing R_1 and θ_1. This is possible by adjusting the external circuit which generates the azimuth sampling pulses. The total area covered by the samples can be changed by changing range and azimuth sampling rates.

4.2.3 Timing and Modes of Operation

System timing and display sync pulses are controlled by a crystal oscillator of frequency 25 MHZ, called the master clock. It provides a highly stable frequency which is necessary for this type of system. By using a master clock, the television raster scanning pulses are synchronized with data which

are read out of the memory to the color-television monitor input. This synchronization process is important for a stable and flicker free picture.

There are two modes of the system operation, the first is the writing mode of operation in which fresh data are stored in the memory. The operator starts this mode using a manual operating switch which has two different positions. The first position is for starting the system operation, which automatically starts the writing mode of operation. The second is for stopping the system operation. The writing mode of operation ends automatically after the proper number of input samples are stored in the memory which is 256 x 512 = 131072 samples, in our case. The second mode is the reading mode of operation in which data are displayed on the raster scan of the color television monitor by reading data out of the memory. This mode starts automatically at the end of the writing mode of operation and continues until the operator switches the system to the writing mode of operation.

Fig. 4.5 illustrates the timing of the writing and reading modes of operation, and the relation between the azimuth sampling pulses and the automatic switching from the writing mode to the reading mode of operation. A general reset signal is generated with the switching between the two modes of operation, and during the time of flyback of the television raster scanning beam (called the vertical reset) in the reading mode of operation. The vertical reset is necessary for

system synchronization and picture stability.

4.2.4 Hardware Implementation of the Display System:

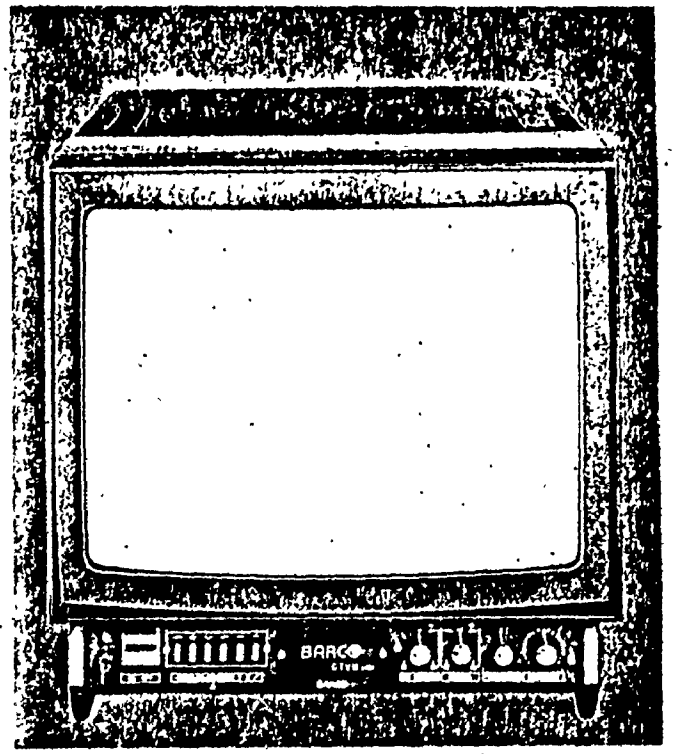
The system is constructed using wire wrapping technique on circuit boards 4.5 inch x 6.5 inch with 42 input/output terminals, in addition to grounding and power supply terminals. Every block of the block diagram Fig. 4.1, except the display and RAM system, is constructed on a circuit board. The boards are plugged in to one chassis which provides connectors for the interconnections between the boards inputs/outputs, and +5 volt power supply with external on/off switch. Two external power supplies (+11 and -6 volt) are used for the ADC circuit.

The chassis connectors are connected with the memory interfacing pins through twisted pair wires. Coaxial cables carry the red, green and blue gun input signals to the color television monitor, in addition to the composite sync input. Two external switches are used in the system construction, one for starting the data refreshing and the other to switch between displaying the data or the color code. The hardware details can be found in Appendix 3.

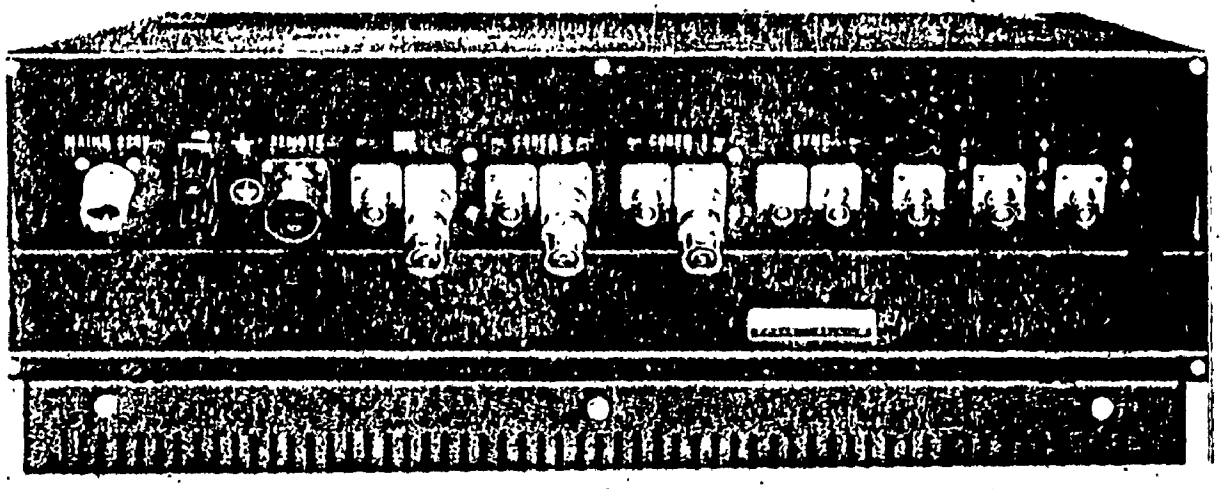
4.3 THE DISPLAY SET:

4.3.1 Type and Specifications:

The color television monitor has been chosen for this application since it provides a wide range of colors. This is necessary for implementing a color coding technique. The display system employs a studio color television monitor with the screen diagonal of 51 cm. Fig. 4.6 is a photograph of the



Front view



Back view

Figure 4.6 Photographs of the front and back views of the color television monitor

front and back views of the color television monitor. Access to color electron guns and external sync signal input are available in the back through BNC jacks (Fig. 4.6). Detailed characteristics of the color television monitor, according to the operation and maintenance manual, can be found in Appendix I.

4.3.2 Sync Signals for Color Television Monitor:

The standard scanning pattern for a television system [24] includes a total of 525 horizontal lines. The frames are repeated at a rate of 30 per second with two fields interlaced in each frame. The first field consists of all the odd number scanning lines and the second consists of all even number scanning lines. This means that the field repetition rate is 60 per second which is the same as the vertical scanning rate.

The sync pulses (Fig. 4.7) are timing pulses which control the horizontal and vertical scanning generators. The vertical sync pulses have a frequency of 60 HZ to provide 60 fields per second and 30 frames per second. The sync pulses are designed in this system to employ only 512 horizontal lines of the 525 available lines which makes each field consists of 256 horizontal lines. This means that 256 horizontal sync pulses must be applied to the horizontal scanning generator between each two vertical sync pulses. There is a 5.5 μS duration horizontal pulse every 63.5 μS. Six pulses immediately precede, and six pulses immediately follow the

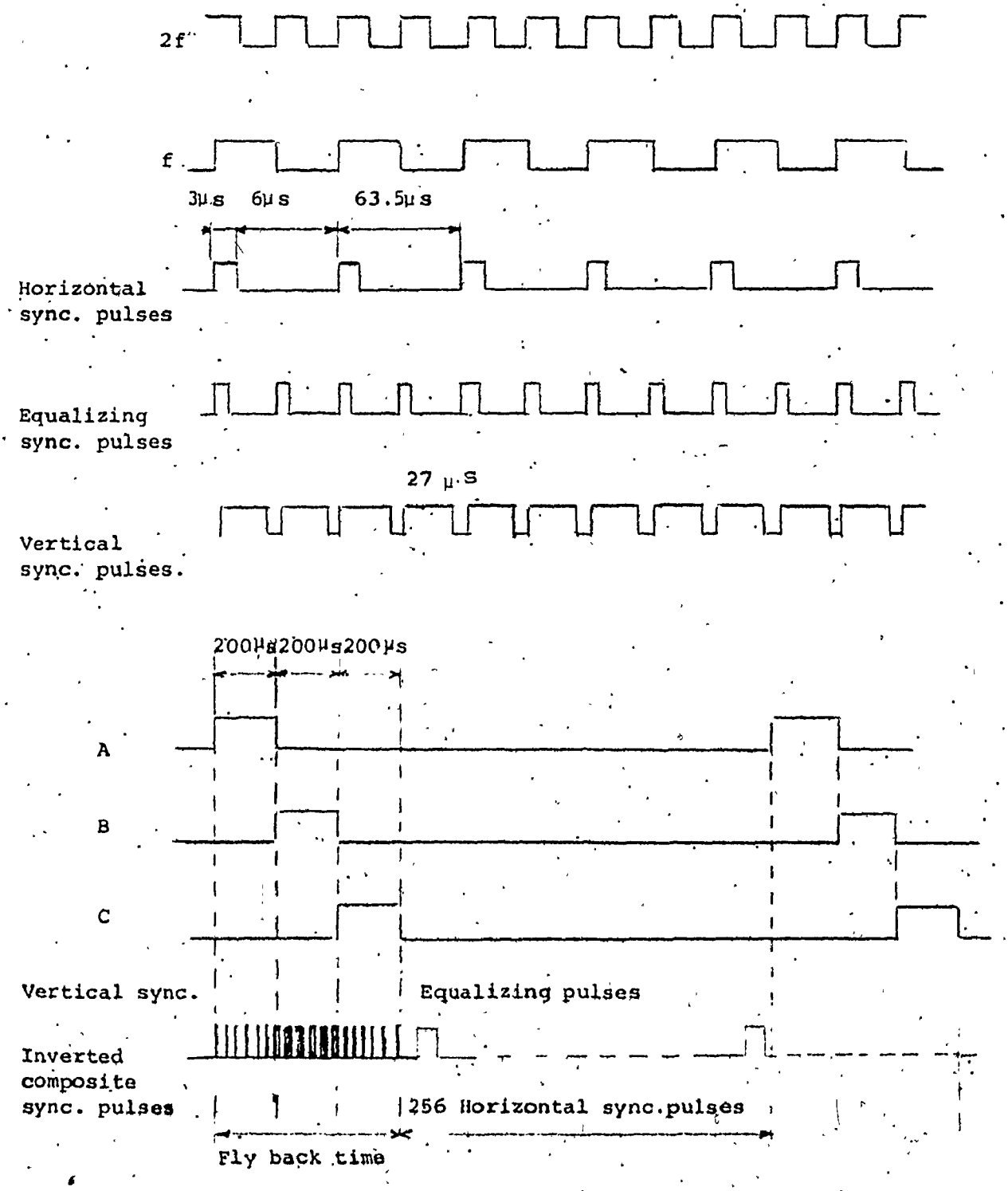


Figure. 4.7 Synchronization signals for the color television.

vertical sync pulses to compensate for half line intervals. They are called the equalizing pulses and their standard frequency is double the horizontal sync pulse frequency with a standard pulse width half the horizontal sync pulse width. The vertical sync pulses have a total width of approximately 200 μS and the complete pulses are divided in to 6 individual pulses that provide horizontal sync during the vertical retrace time. The individual pulse has a pulse width of approximately 27 μS.

Finally, the horizontal, equalizing and vertical sync pulses are combined to form the composite sync pulse train (Fig. 4.7). This composite sync pulse train is then fed to the color television monitor sync input, where the horizontal and vertical sync pulses are separated internally and applied to the corresponding deflection generator.

4.3.3 Sync Signal Generator:

The sync signal generator contains the master clock used to generate all of the sync pulses for the color television monitor as illustrated by Fig. 4.7. These include the horizontal, the equalizing and the vertical sync pulses. These pulses are combined to form the standard composite sync pulse signal which activates the scanning of the color television monitor.

One of the circuit outputs is the vertical reset pulse signal shown in Fig. 4.7, which is used as a general reset for the display system during the time of the beam flyback . Also, the clock pulses, which control reading the data

from the memory (system sync pulses), are generated from the master clock pulses by dividing 25 MHZ by three to meet the required data rate.

The sync signal generator circuit diagram is illustrated by Fig. 4.8.a. The signal starts at the master clock output and goes through series of frequency dividers. The frequency divide by 109 circuit is shown in Fig. 4.8.b. The different sync signals are generated by the circuit, then the pulse width of each signal is adjusted by means of a monostable multivibrator. Also, monostable multivibrators are used to generate the pulses B and C from A (Fig. 4.8.a).

4.4 RANDOM ACCESS MEMORY SYSTEM

Considering the existing commercial storage systems such as discs, shift registers and random access memory systems, it was found that the solid state RAM system is compatible with the writing speed of the display. The access cycle time of the RAM system which is used in the display system is approximately 400 ns, while the access cycle time of discs or shift registers are of the order of several milliseconds [16]. The RAM system also has the advantage of inherent addressing flexibility [34] and its non-sequential data access capability reduces the required control circuitry [33]. From the economy point of view, it would seem that since the computer industry is concerned almost exclusively with RAM system for scratch pad memories, further development will concentrate on these devices.

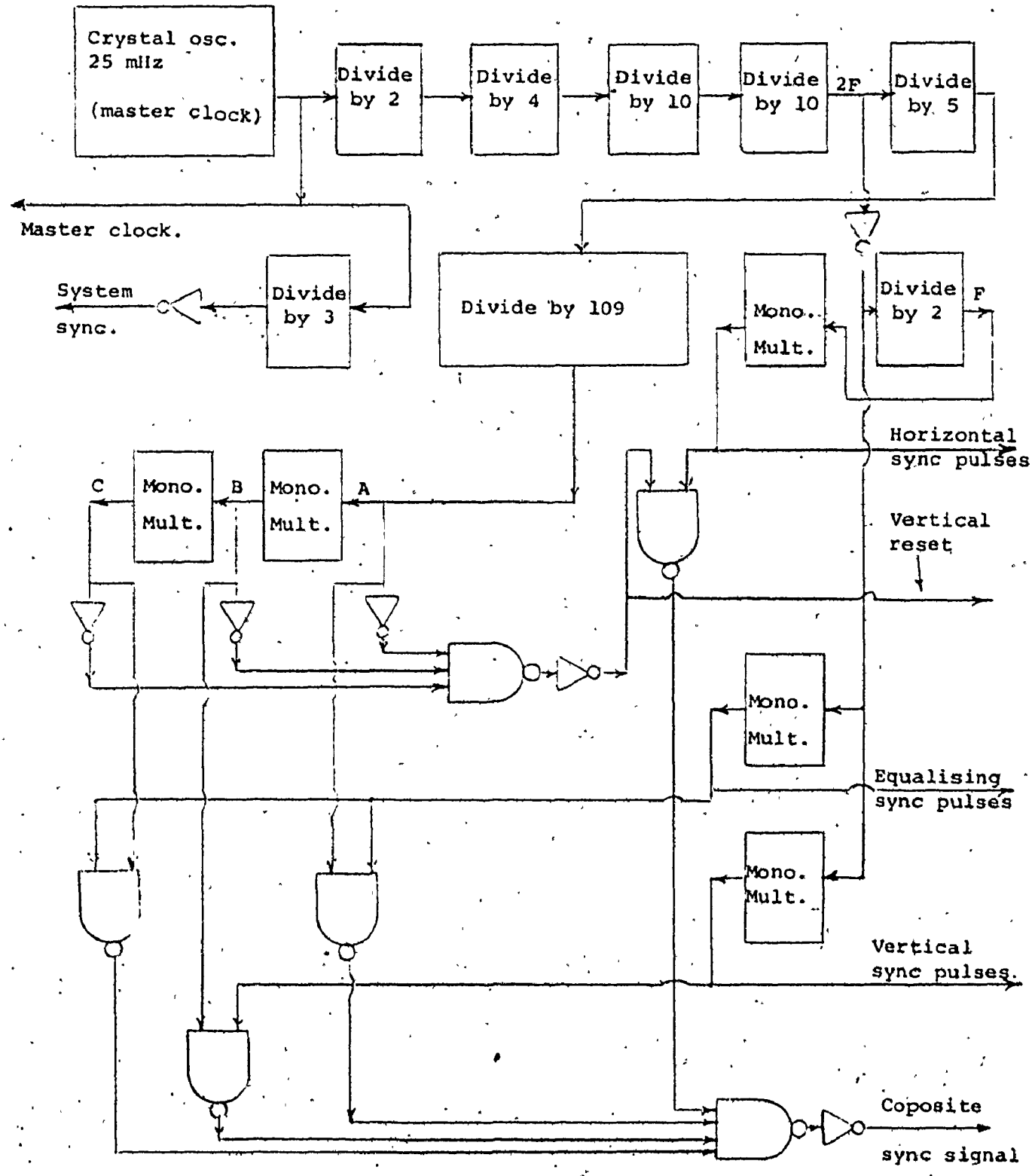


Figure 4.8.a Sync signal generator circuit diagram.

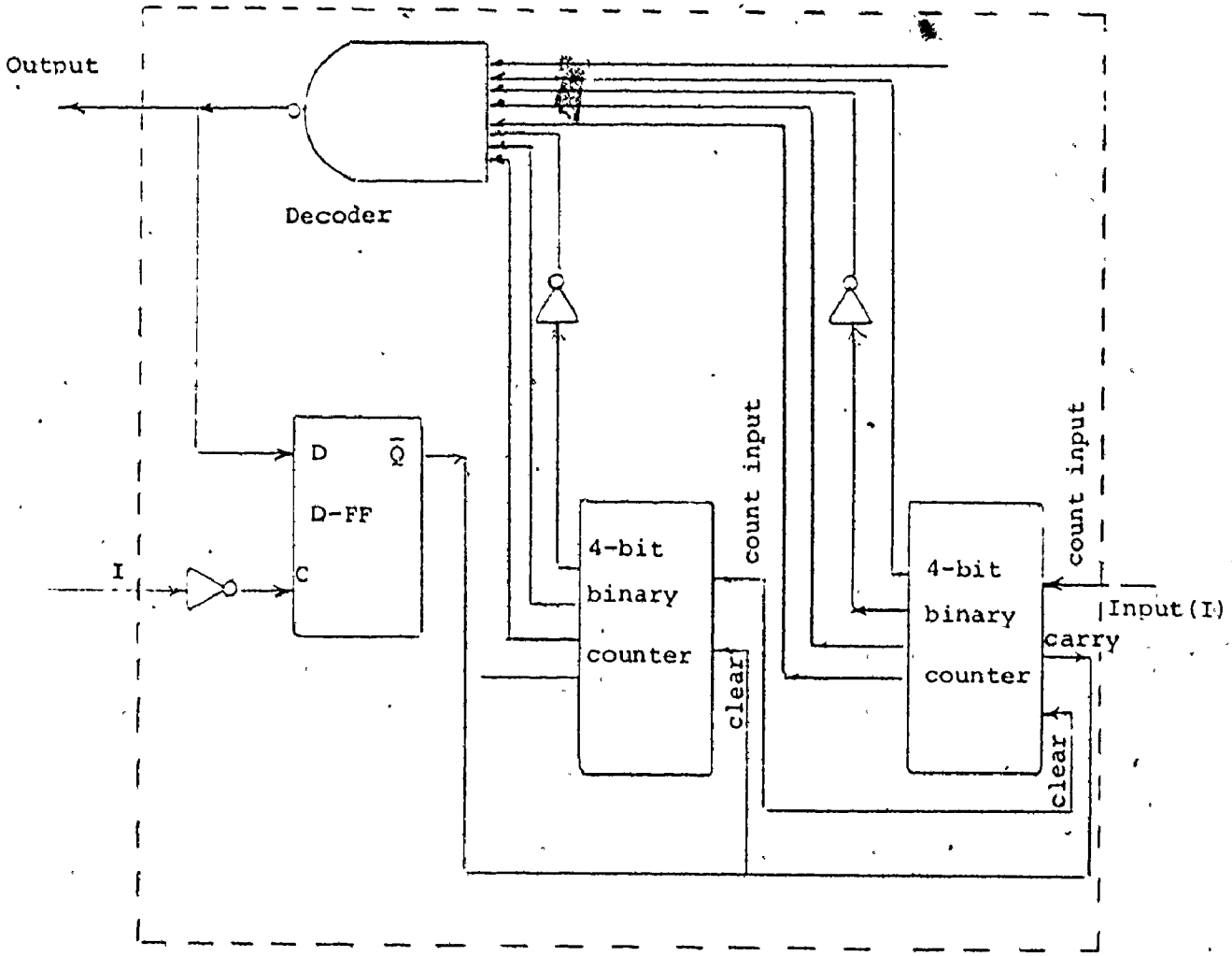


Figure4.8.b Divide by 109 circuit diagram.

Two new memory technologies may alter the selection of RAM as the optimum memory in the near future. These are the bubble memories and charge coupled devices. Both of these technologies promise high bit packages, high densities and low cost, but they are serial access memories. Therefore, more complex associated addressing circuitryis required for their operation in this type of application, offsetting some of their advantages [22]. As well, bubble memories are slower than semiconductor memories in general; they bridge the gap between the access time in electronic and electromagnetic storage systems [35]. The difference between the access time in electronic and electromagnetic storage system is called the "access gap".

4.4.1 RAM System Specifications and Operation:

The memory system used is a self contained random access semiconductor memory, shown in Fig. 4.9, employing the 3400 N type of RAM unit. The memory system consists of up to four Memory Card Assemblies with a maximum capacity of 32,768 of 18 bit words. Only two cards are available to our display system and each card can be accessed independently.

The modes of operation for a card are Read, Write, and Read/Modify/Write (Split-Cycle). Table 4.1 is a list of general specifications of the memory. The interface circuitry is shown in Fig. 4.10.

Fig. 4.11 is the timing diagram of the interface signals with times shown measured at the 50% point of signal transmission. A list of interface signal functions and line

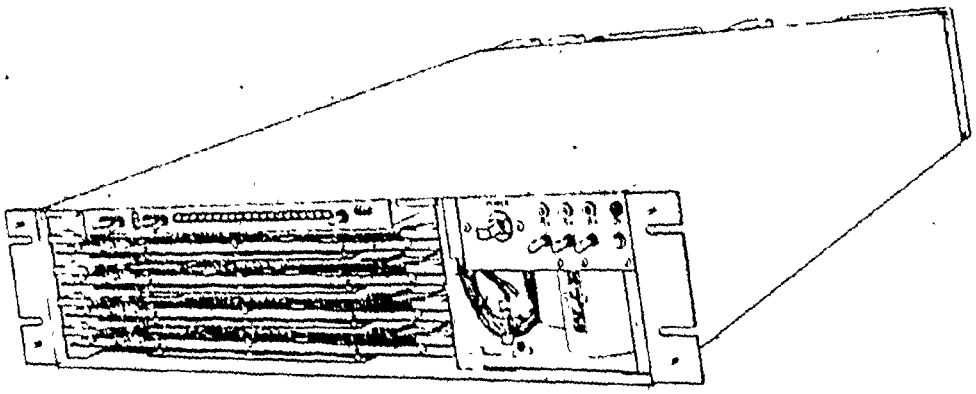


Figure 4.9 MICRORAM semiconductor system
(front panel removed)

Table 4.1 Memory system 3400N Specifications

	ITEM	SPECIFICATIONS
*	Type of Memory	Random access NMOS Semiconductor
*	Card Configurations	32, 768 words by 18 bits
*	Modes of Operation	Read
		Write
		Read/Modify/Write (Split Cycle)
*	Timing:	
	Read Cycle	450 ns
	Write Cycle	450 ns
	Read/Modify/Write	900 ns
	Access	275 ns max
*	Interface Circuitry	Open Collector Output-74S 38TTL
*	Logic Levels:	Input-75S XX Series
	Logic zero	+ 2.5 to 5.0 volts
	Logic One	0.0 to 0.5 volts.

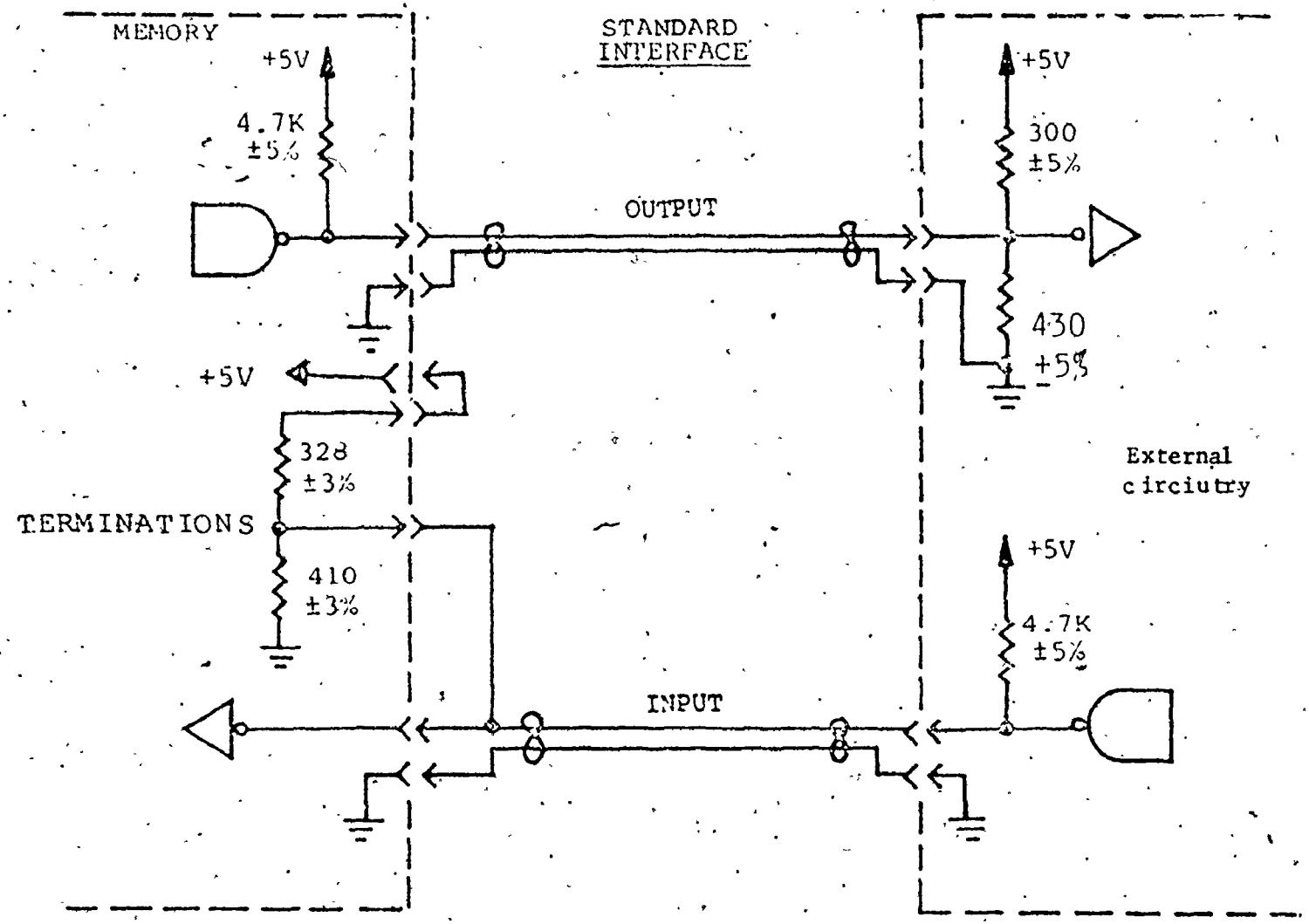


Figure 4.10 Interface circuitry between the memory and the external system.

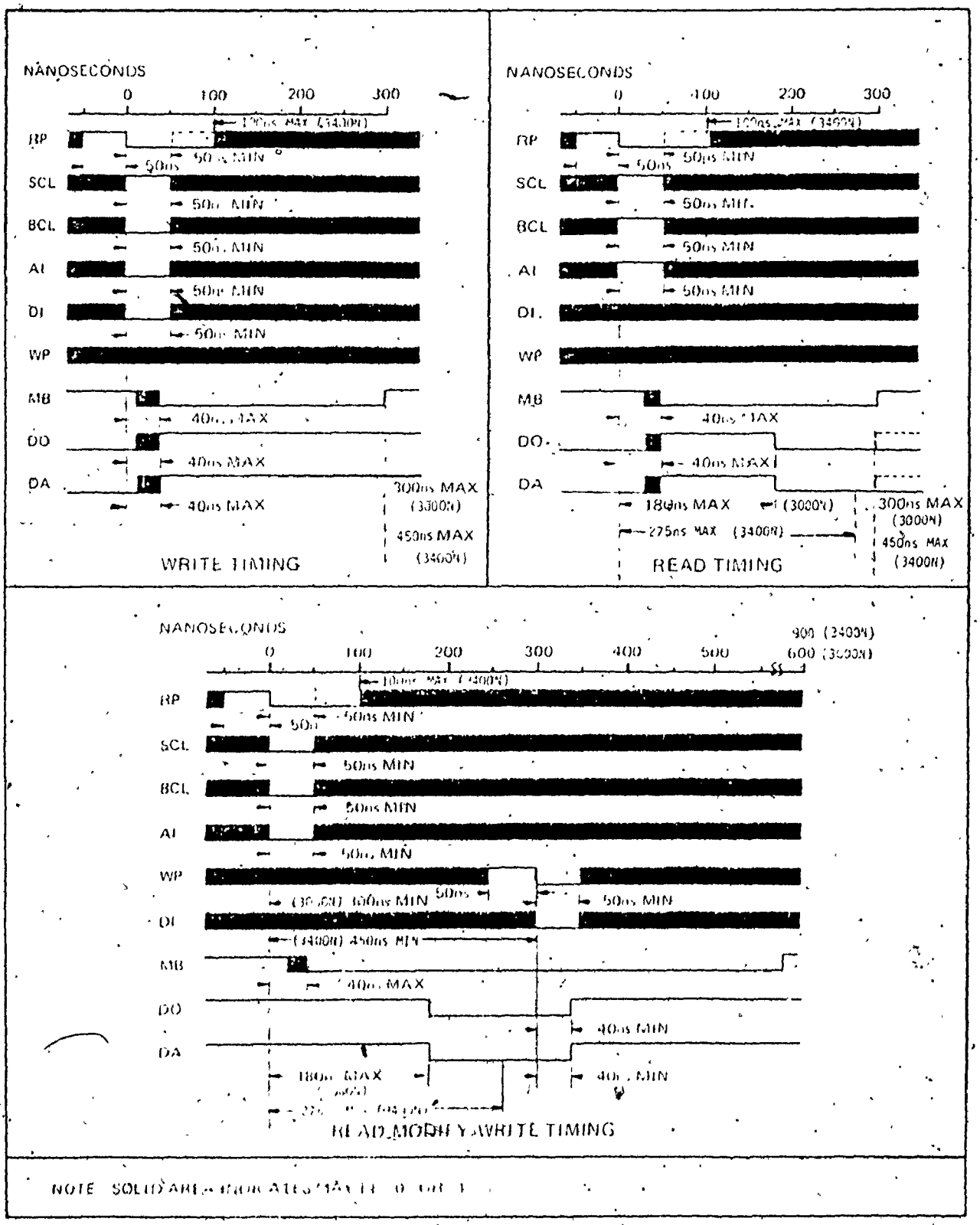


Figure 4.11 RAM system 3400N interface signals timing diagram.

loading characteristics is given in Table 4.2. The interface signals are described in more detail with the design of the other circuits which are interconnected with the memory. Appendix 2 contains the details of the RAM specifications, and the connection of the interface connector pins with the external circuitry.

4.4.2 Memory Organization:

The memory is organized as a matrix of 16 bit words (two bits left for other purposes) with each word encoded so as to include four adjacent spots of a given TV raster scan lines. Every spot represents a 4-bit data word which is the digital value of an input sample. By handling four parallel channels of data words the data rate is increased four times over that of the maximum rate of the memory. The location of the word to be accessed is specified by the address applied to the memory address lines by the external circuitry.

The required capacity of the memory is determined by the display resolution in terms of the number of samples displayed by the TV raster scan. The display system is designed for the capacity of 256 x 512 = 131072 samples which requires a storage of 37,768 of 16-bit words. One memory card is used by the system and the other card is left for future extension such as to increase the system capacity or to store processed data.

Table 4.2 Descriptions of the RAM system interface signal

Signal Name	ABBR	Type/*per Card	Description
Initiate	PP	-pulse/ 1 TTL load	Starts memory cycle when memory is available.
Write Pluse	WP	-pulse/ 1 TTL load	In conjunction with Splic-Cycle signal starts the Write phase of a split cycle.
Split Cycle	SC	Level/ 1 TTL load	When low, enables a Split-Cycle operation; when high, enables Read or Write operation.
Byte Control	(BCL 1, BCL2)	Level/ 1 TTL load per line	Determines mode of operation of applicable byte. When BCL is low, RP executes Write cycle. When BCL is high, RP executes a Read cycle.
Address In	AI00-AI13**	Level/ 1 TTL load per line	Binary coded signals that select memory address.*** These signals must be stable at the start of a memory cycle.
Address In	AI14	Level/ 1 TTL load	Address bit used with Address Option (ADOP) to change address configureation: ADOP.. AI14 = 16K x 10 or 32K x 10 ADOP = 8K x 20 or 16K x 20

NOTE:

* When termination resistors are connected (by external jumpers), each source must be capable of sinking 17 ma in addition to

(contd)

Table 4.2 continued

Signal Name	ABEP	Type/*per Card	Description
Extended Address In	XA11, XA12 XA13	Level/ 1 TTL load per line	Binary coded signals that select the Memory Card.
Data In	(DI00-DI19)	Level/ 1 TTL load per line	Information signals (input).
Data Out	(Do00 Do19)	Level	Information signals (output).
Data available	DA	-level	Indicates to CPU that data is available on data output lines.
Memory Busy	MB	-level	Indicates to CPU that memory is busy and cannot accept an RP.
General Reset	GR	-pulse/ 1 TTL load	Signal that resets all registers and initializes timing circuits. CAUTION: Do not execute a general reset while a memory cycle is in progress. Loss of data could result.

listed load.

** AI13 must be held low if second array card (Extender Memory Card) is not inserted.

*** Unused address lines are open (high).

4.5 INPUT-MEMORY INTERFACE:

4.5.1 Analog-to-Digital Converter (ADC):

The ADC is a 4-bit binary device with comparatively fast speed. The speed requirement is related to the rate of sampling clock pulses, such that the maximum digitizing speed determines the upper limit of the rate of the sampling clock pulses. For example, if the ADC digitizing time is 100 ns, then, the maximum sampling frequency is 10 MHZ.

No commercially available ADC has this fast speed with low price. For this reason an ADC was constructed with a digitizing time less than 100 ns. Fig. 4.12 illustrates the ADC inputs and outputs where the binary word $X_4X_3X_2X_1$ represents the digital value of the analog input at the rising edge of the sampling clock pulse. This value remains on the output lines IN0 to IN3 until the rising edge of the next sampling clock pulses.

The circuit diagram of the ADC is shown in Fig. 4.13 and the implementation of the ADC logic circuit is shown in Fig. 4.14 . Each of the fifteen comparators has one input biased to a voltage level at which the digital equivalent of input signal should change. Voltages A_1 through A_{15} along resistor chain R_1 to R_{15} are the values at which each comparator switches. The 3-bit version of this circuit can be found in [36] .

The ADC digitizes the input according to the levels A_1 through A_{15} to the binary numbers representing the decimal

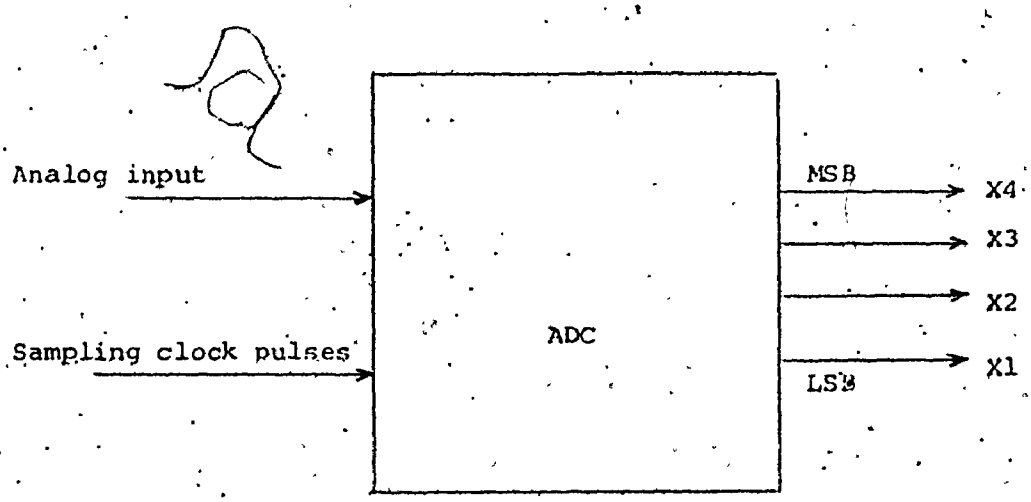


Figure 4.12 ADC block diagram.

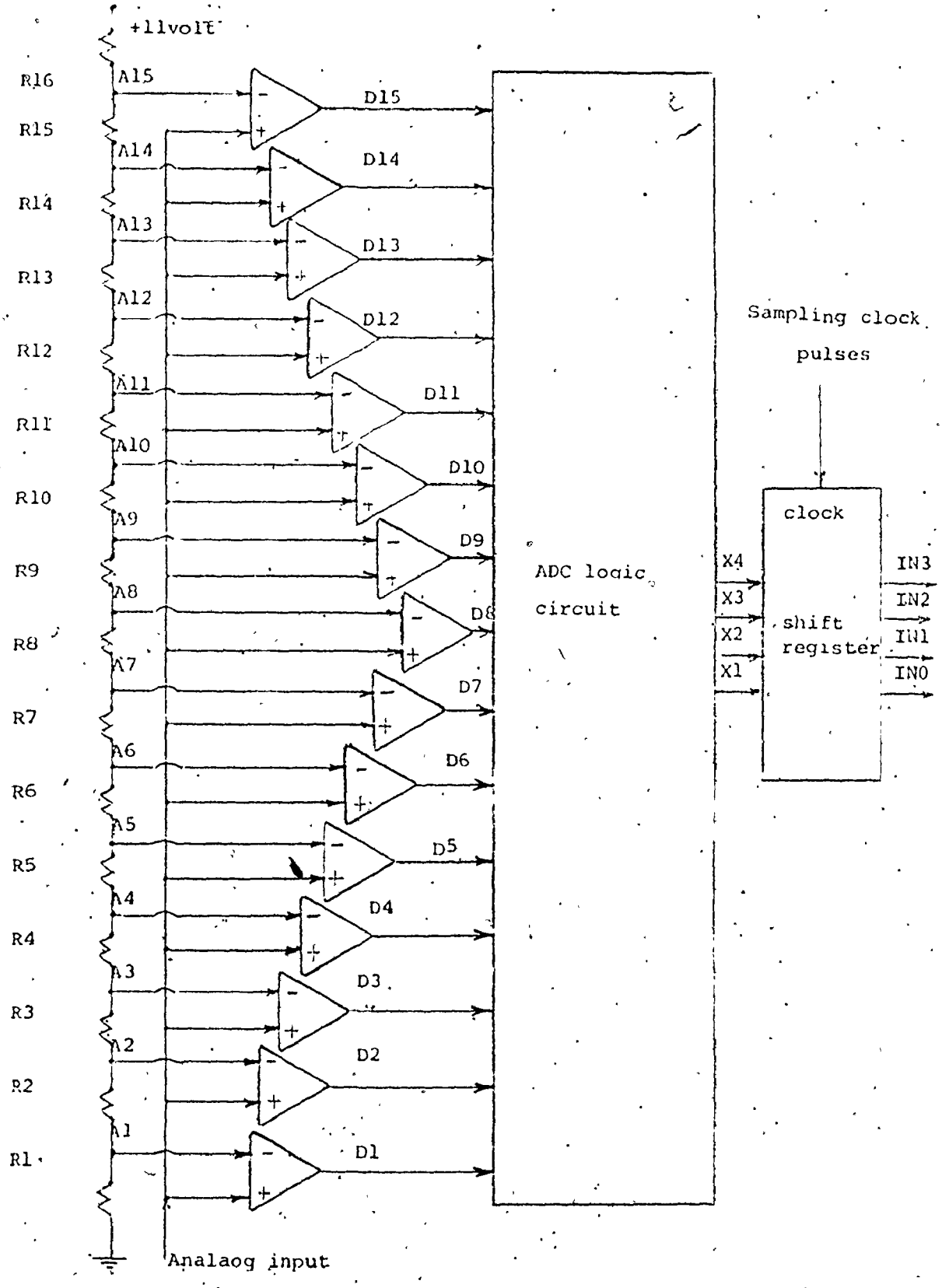


Figure 4.13 ADC circuit diagram.

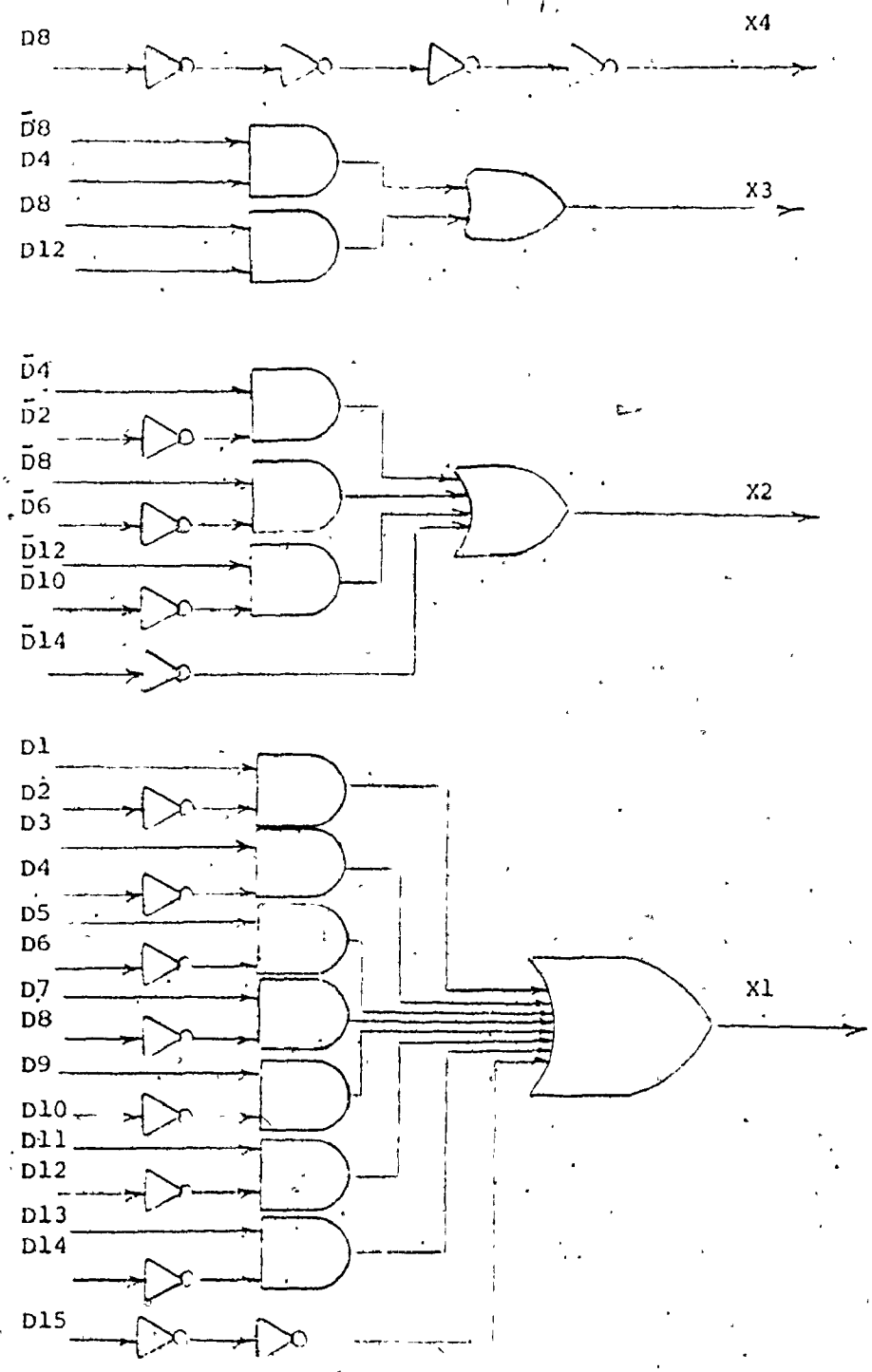


Figure 4.14 ADC logic circuit diagram.

numbers from 0 to 15 as shown in Table 4.3. The truth table of the logic circuit is given in Table 4.4 and the minimized solutions of this logic design problem are the following equations:

$$X_1 = D_1\bar{D}_2 + D_3\bar{D}_4 + D_5\bar{D}_6 + D_7\bar{D}_8 + D_9\bar{D}_{10} + D_{11}\bar{D}_{12} + D_{13}\bar{D}_{14} + D_{15} \quad (4.1)$$

$$X_2 = D_2\bar{D}_4 + D_6\bar{D}_8 + D_{10}\bar{D}_{12} + D_{14} \quad (4.2)$$

$$X_3 = D_4\bar{D}_8 + D_{12} \quad (4.3)$$

$$X_4 = D_8 \quad (4.4)$$

4.5.2 Interface Between the ADC and the Memory:

The basic requirement of this interface circuit is the conversion of 4-bit data words from the ADC, or through the system digital data input, to the form of a 16-bit RAM system words. The circuit receives and combines consecutive 4-bit input samples to produce 16-bit word which are then addressed by the addressing and timing circuit, and stored in the RAM system using the direct memory access technique (DMA).

At the same time the circuit generates some of the interfacing signals required for operating the memory in the writing mode of operation. These include the address counting pulses for writing in the memory (WC) and the memory cycle initiating pulses (as described in Table 4.2) in the writing mode of operation (RPW) (Fig. 4.15). The address counting pulses are fed to the addressing and timing circuit to increment the address

Table 4.3 ADC Digitizing levels and their binary representations.

Digitizing level		Binary Representation			
		X4	X3	X2	X1
Max.level	A15	1	1	1	1
	A14	1	1	1	0
	A13	1	1	0	1
	A12	1	1	0	0
	A11	1	0	1	1
	A10	1	0	1	0
	A9	1	0	0	1
	A8	1	0	0	0
	A7	0	1	1	1
	A6	0	1	1	0
	A5	0	1	0	1
	A4	0	1	0	0
	A3	0	0	1	1
	A2	0	0	1	0
	A1	0	0	0	1
Zero level	A0	0	0	0	0

Table 4.4 Truth table of the ADC logic circuit

D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	X_4	X_3	X_2	X_1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	1
0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	0	0
0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	1
0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	1	0
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	1	1
0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	1
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	1	0
0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

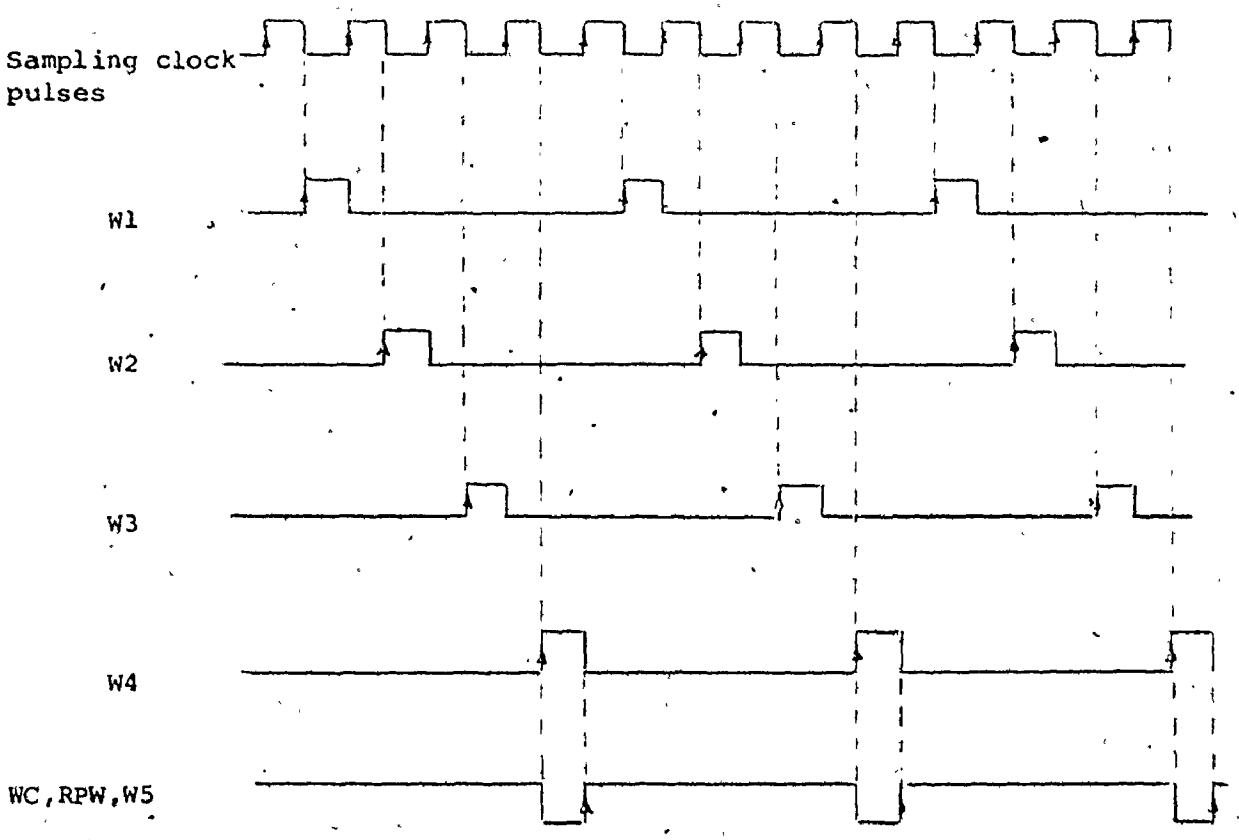


Figure 4.15 Timing diagram for writing mode of operation.

counter.

The circuit diagram for the interface is shown in Fig. 4.16 and Appendix 3 contains the hardware details. The signals W_1, W_2, W_3, W_4, W_5, WC, RPW and sampling clock pulses are shown in Fig. 4.15. One of the circuit inputs is the sampling clock pulses from the sampling clock located in the addressing and timing circuit. Sampling clock pulses are applied to the clock input of a serial input/parallel output shift register (SR9) to generate the pulses W_1 through W_4 and then W_5, WC and R_p as shown in the circuit diagram. Input data are applied to the input lines of the parallel input/parallel output shift registers SR1, SR2, SR3, and SR4 through a 4-line data bus. Data are transferred to the parallel input/parallel output shift registers SR5, SR6, SR7 and SR8 at the rising edges of the pulses W_1, W_2, W_3 and W_4 respectively. Data transfer occurs such that four 4-bit consecutive words are applied to the four shift registers inputs before the rising edge of the next pulse of W_5. Data are then transferred to the 16-output lines of the four shift register DI-0 through DI-15. The output lines are connected directly to the data input connector pins of the RAM. Data become available at the memory input at the proper time according to the timing diagram Fig. 4.11. Also the signals WC and RPW are generated accordingly, to the same timing diagram.

4.6 ADDRESSING AND TIMING CIRCUIT

The first requirement of the addressing and timing circuit is to address data coming in to the memory in the writing mode

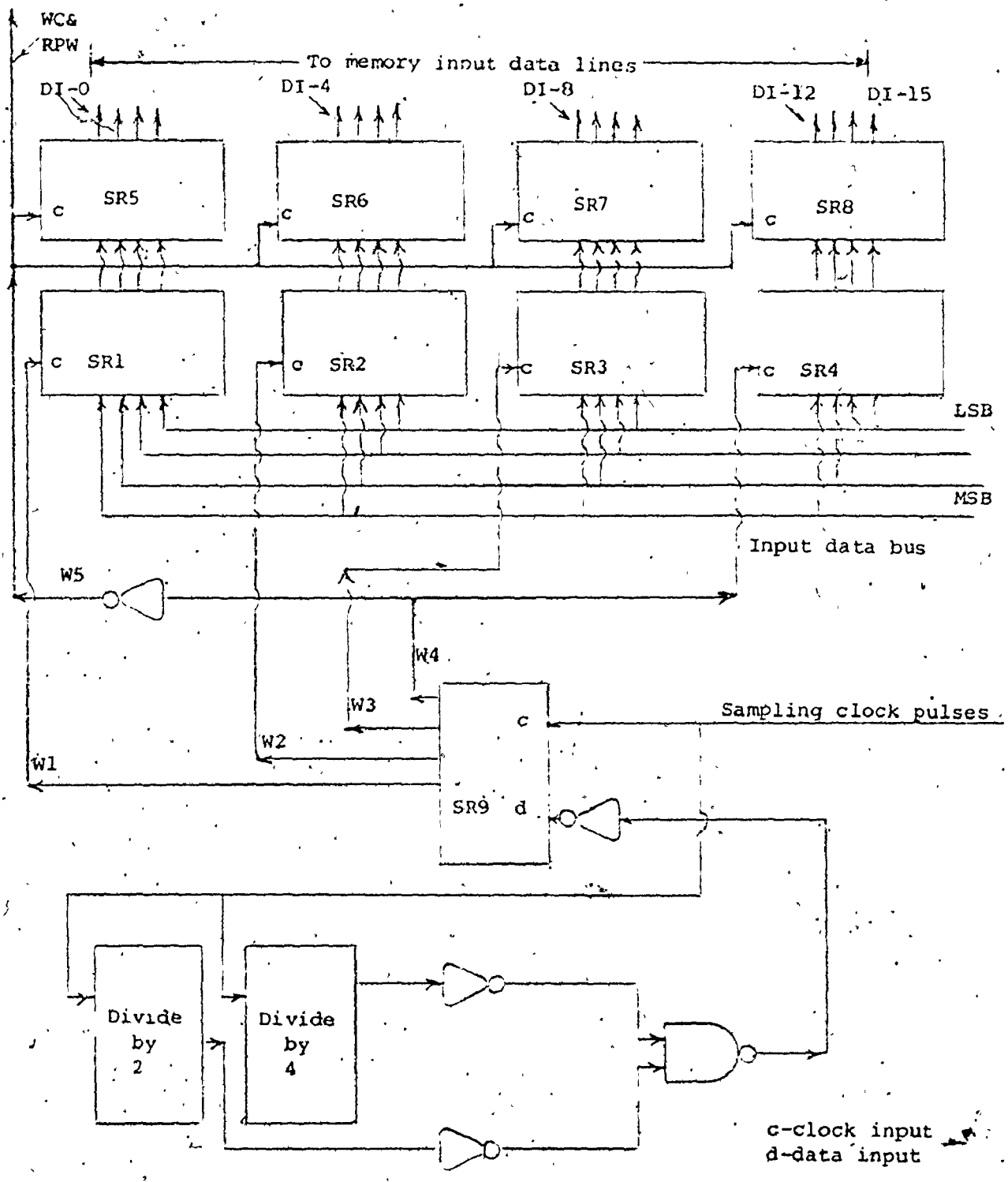


Figure 4.16 Circuit diagram for the ADC-memory interface.

of operation, and data from the memory in the reading mode of operation. The address information is applied to the address lines of the memory according to the RAM system interface signals (Fig. 4.11).

The second function of this circuit is to provide the memory cycle initiating pulses (RP) during the two modes of operation, and the signal BCL for switching the memory between different modes of operation (Fig. 4.11 and Table 4.2). It also provides the memory general reset as defined in Table 4.2 (GRM in Fig. 4.17).

The sampling clock is located in this circuit where the azimuth sampling pulses control its ON/OFF input as shown in Fig. 4.4 and explained in section 4.2.2. As well, the circuit controls switching the display system between writing and reading modes of operation as explained in section 4.2.3 and illustrated by Fig. 4.5. The general reset pulses (GRP, GRN) shown in Fig. 4.5 are generated by the addressing and timing circuit and supplied to the entire system.

The circuit diagram for the addressing and timing circuit is shown in Fig. 4.17 and the hardware details are given in Appendix 3. A 16-bit address counter is employed to provide addresses for every 16-bit word stored into/or read-from the memory. The count input of the counter receives clock pulses coming from the ADC-memory interface circuit (WC as shown in Fig. 4.15) in the writing mode of operation, and coming from the memory-encoder interface circuit (RC as shown in Fig. 4.18) in the reading mode of operation. The switching between the

two signals is controlled by the signal BCL. Finally, the counter is cleared by the general reset pulses (Fig. 4.5).

The memory cycle initiating pulses RP are actually the pulses RPW (Fig. 4.15) in the writing mode of operation and RPR (Fig. 4.18) in the reading mode of operation. The switching between the two signals is performed by the aid of the signal BCL. The pulse width of RP is adjusted by a monostable multivibrator. The level BCL is generated by the circuit according to the mode of operation (Fig. 4.11).

A two state switch with high (H) and low (L) position is used to operate the system by starting the writing mode of operation when in the low position. The automatic switching from writing to reading mode of operation occurs when the 256 counter counts 256 of azimuth sampling pulses, and the 512 counter counts 512 of the sampling clock pulses. Thus, a total of 256 x 512 samples are stored and BCL goes high. The BCL level is also used to gate the azimuth sampling pulses such that when the system switches to the reading mode of operation, the gate is off.

The sampling clock is a free running oscillator having a frequency which can be adjusted by varying two resistances and two capacitances (see appendix 3). The sampling clock pulses are fed to one of the circuit outputs providing availability for the other circuits. The circuit generates the general reset pulses (GRP) and the inverted value of this pulse (GRN) for the devices which need a negative pulse to be cleared. MGR (Fig. 4.17) exists only when the system switches between modes of operation, if RP is not applied to the memory.

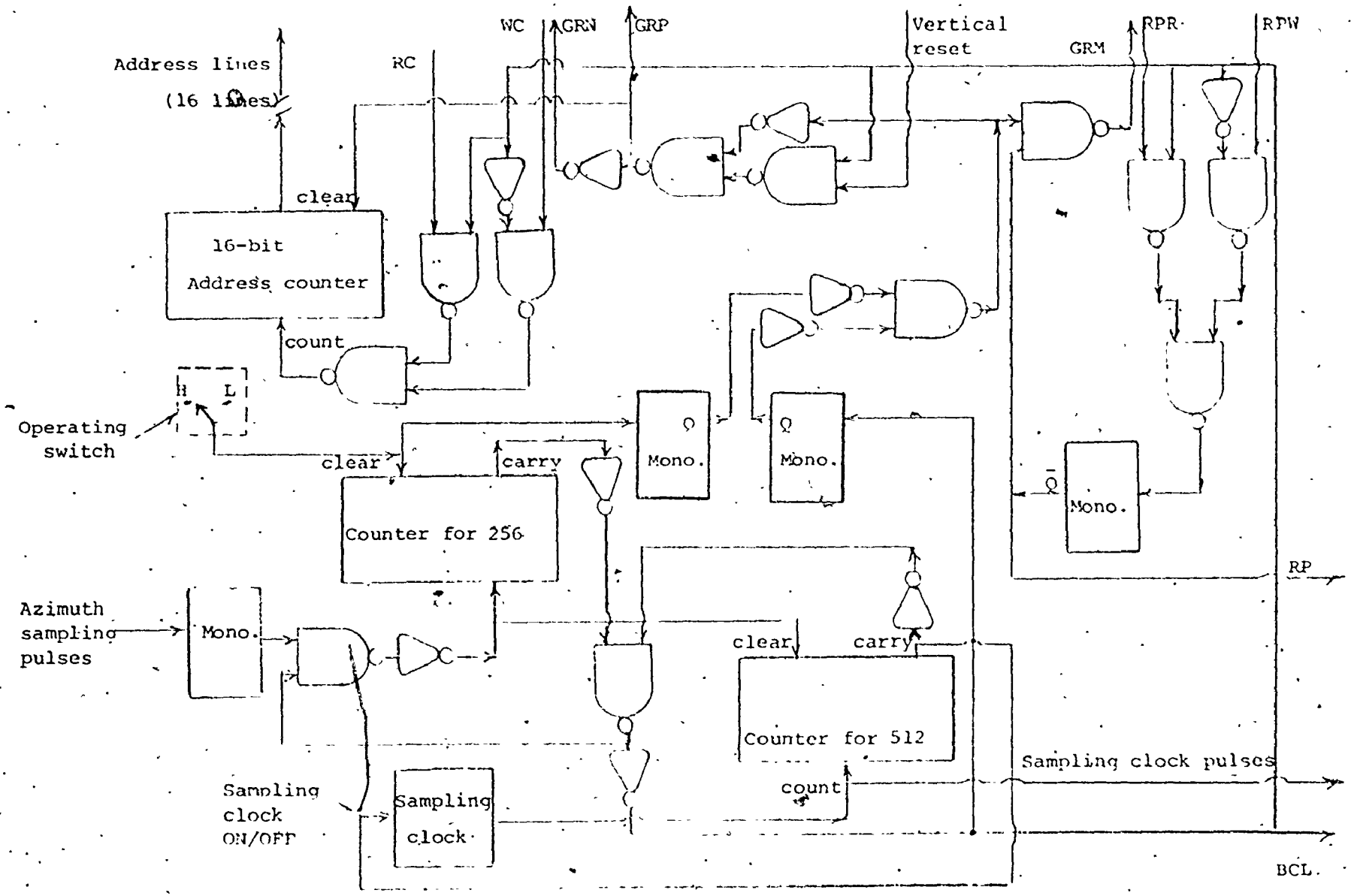


Figure 4.17 Logic circuit diagram for addressing and timing circuit.

4.7 MEMORY-DISPLAY INTERFACE:

4.7.1 Interface Between the Memory and the Color-Encoder:

/The basic function of this circuit is to read data out of the memory using DMA technique. The circuit receives every 16-bit word output from the RAM system when the data are available at the memory output lines (Fig. 4.11). The circuit then splits the 16-bit word to four consecutive 4-bit words and feeds these data to the color-encoder such that two conditions are satisfied. The first, is the compatibility of the data rate with the writing speed of the color television monitor, and the second is the synchronization of the data to the raster scan of the color television monitor.

For a resolution of 512 effective spots per horizontal line, the minimum data rate is 4-bit word every 112.3 ns. This speed is directly compatible with memory speed of 400 ns per 16-bit word since every effective spot corresponds to a 4-bit word every 100 ns. The circuit automatically displays exactly 512 4-bit samples per horizontal line for each of the 256 lines. This means that same data are displayed for the odd field and the even field of the frame producing a matrix of 256 x 512 as explained in section 4.2.2

In addition, the circuit generates the interfacing and timing signals for the memory in the reading mode of operation such as the address counter increment pulses (RC) and the memory cycle initiating pulses (RPR), as illustrated

by the timing diagram Fig. 4.18.

The circuit for the interface between the memory and color-encoder is shown in Fig. 4.19. Hardware details can be found in Appendix 3. The basic concepts applied for this circuit design are the same as in the ADC-memory interface circuit with the direction of data flow reversed. The 16-bit data output DO-0 through DO-15 of the memory is applied to the input lines of four 4-bit parallel-in/parallel-out shift registers. The output lines of this set of shift registers are connected to the input of another set of four 4-bit parallel-in/parallel-out-tri-state shift registers. The data are transfered from the input of the first set to the input of the second set at the rising edges of the pulses R_5. The data are then transferred from the second set of inputs to the output data bus with the aid of the pulses R1, R2, R3 and R4 with one 4-bit word at a time. Thus, the same sequence is achieved at the output as was encoded at the input.

The tri-state output shift registers are interfaced directly with the data bus. They have gated output control lines for enabling or disabling the outputs such that when the output control is high, the output is disabled to the high impedance state. The output of each of the four shift registers is enabled consecutively at the same instant as the clock pulse C by applying the inverted clock pulses at the output control inputs (E), i.e., the output is enabled only during the clock pulses, otherwise it is disabled. Hence, the output data bus transfers the 4-bit data to the color encoder input.

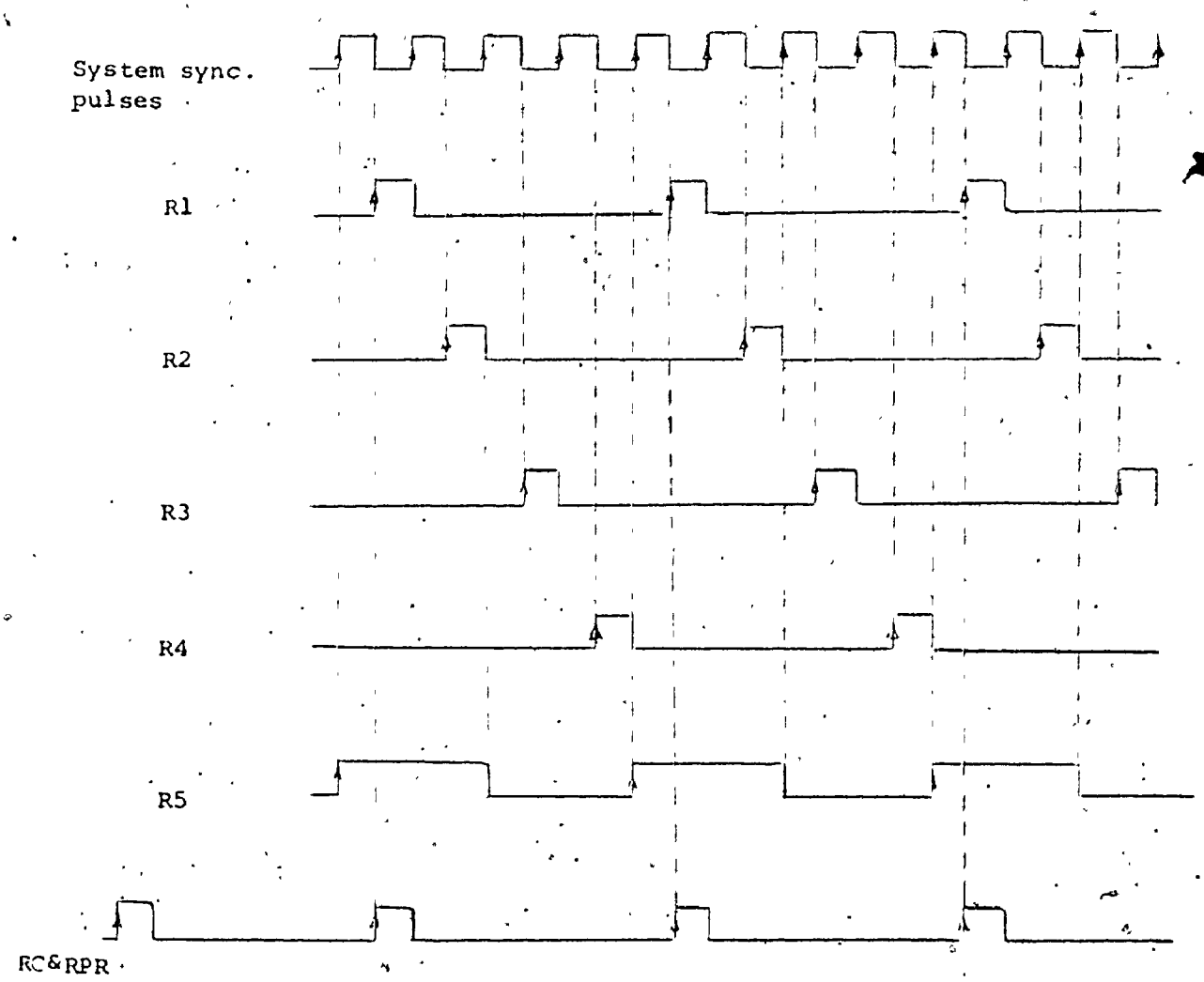


Figure 4.18 Timing diagram for reading mode of operation.

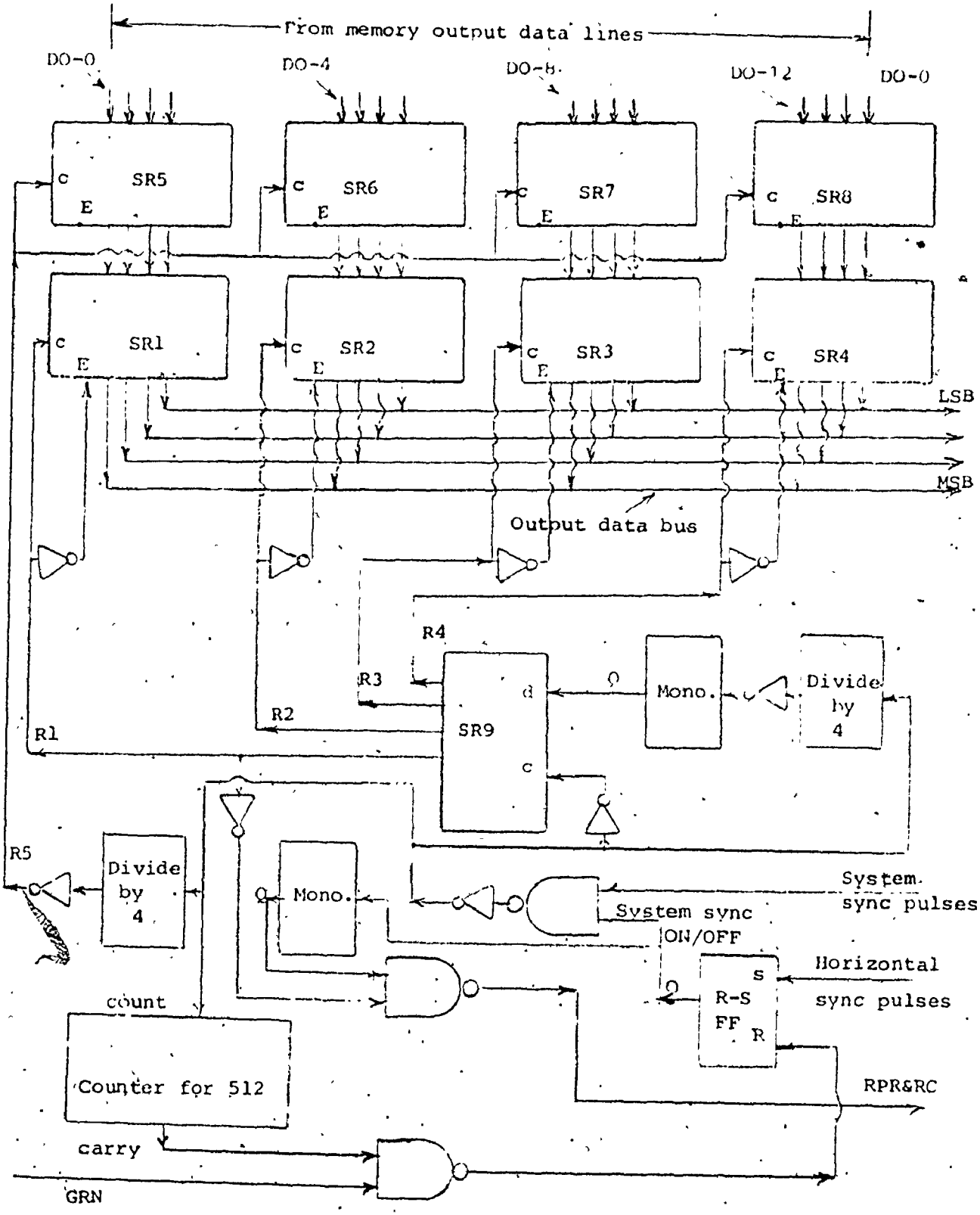


Figure 4.19 Memory-color encoder interface circuit diagram.

The signals R_1 through R_4 are generated by a serial input/parallel output 4-bit shift register at a rate compatible with the system sync pulse rate as illustrated by the timing diagram of Fig. 4.18. The system sync pulse rate is 8.9 MHZ which corresponds to a sample every 112 ns. The other signals such as R_5, RC and RPR are generated as shown by the logic circuit. Only the first pulse of the RPR pulses is generated by the trailing edge of each general reset pulse (GRP) in order to initiate the first memory cycle at the beginning of the reading mode of operation.

A 512 pulse counter for system sync pulses is used to terminate the clock pulse train to the serial-in/parallel-out shift register (input C) to stop transferring the data to the circuit output. The counting starts with the leading edges of the horizontal pulses and stops after 512 pulses. Also, the system sync pulses and the clock pulses C are gated by the general reset pulses (GRN) such that they terminate during the reset time. Thus, the compatibility of data rate with the writing speed of the color television monitor is satisfied by selecting the proper data rate. Also, the data synchronization condition is satisfied by feeding data with the horizontal pulse and by stopping the whole process during the general reset pulses. This synchronizes the process with the switching between the modes of operation and with the raster scanning.

4.7.2 Color-Encoder

During the reading mode of system operation, the color encoder converts each of 16 4-bit words from the RAM system into a unique combination of three voltages which are used to derive signals for the red, green and blue guns of the television monitor. The colors used for the color coding range from black as the lowest level up through blues, yellows and reds with white as the highest levels.

Another function of the color encoder circuit provides a feature to display the color code on the raster scan of the color television monitor. This is presented in the form of horizontal bands which are in the same order as that of the signal amplitude color-coding scheme. This feature can be enabled any time during the reading mode of operation by the aid of a toggle switch (the color testing switch), thus allowing the viewer to see either the data or the color code. The color code can also be displayed during the writing mode of operation.

The logic circuit diagram of the color-encoder circuit is shown in Fig. 4.20. The hardware details are given in Appendix 3. In this circuit, digital signals are converted to analog signals before the color television red, green and blue gun inputs. Any specific digital-to-analog conversion code can be applied for the design of the digital-to-analog converter (DAC). This code, as illustrated by Fig. 4.21 means that each of the three similar DAC circuits (Fig. 4.20) transforms every one of the three possible 2-bit inputs to only one of

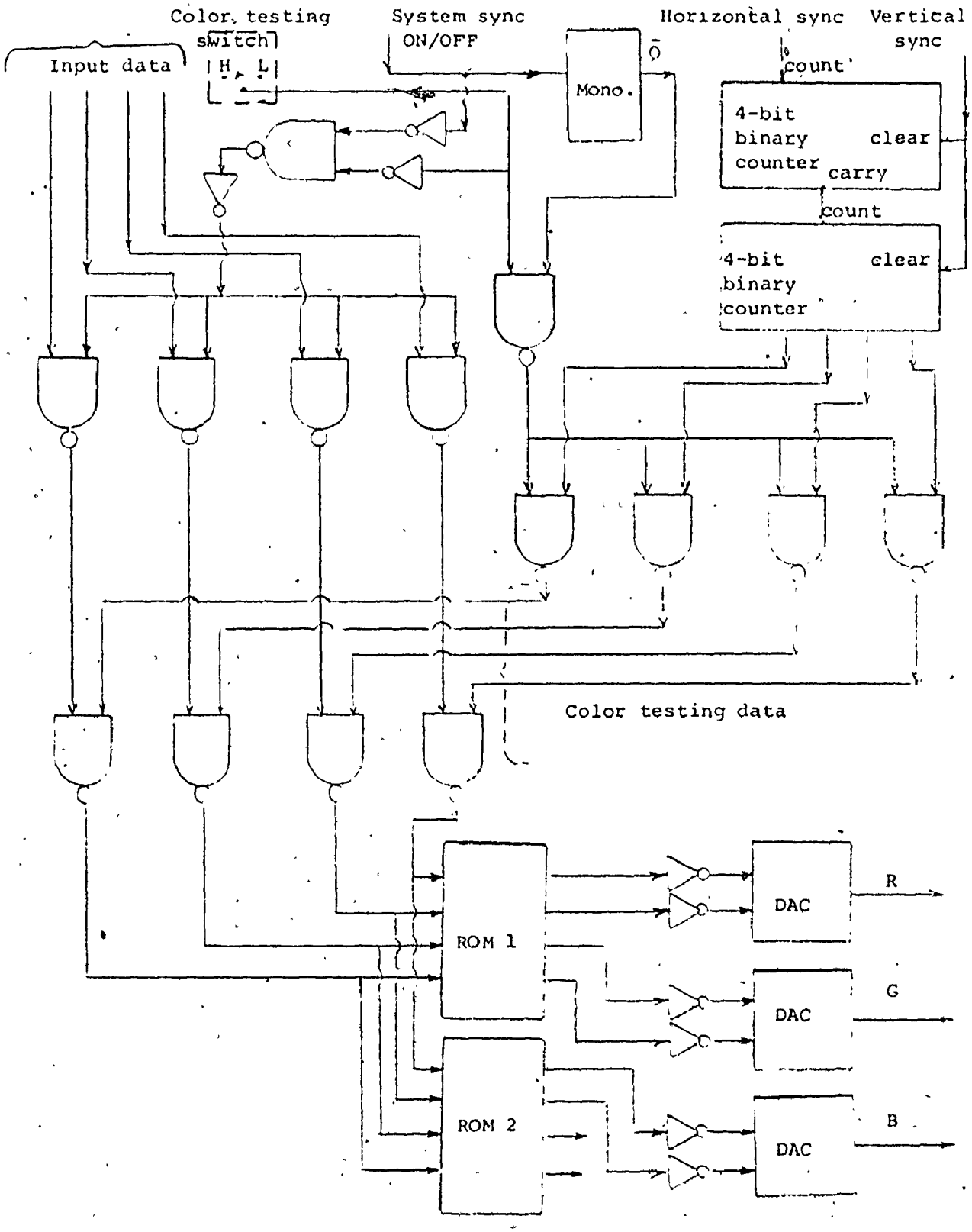
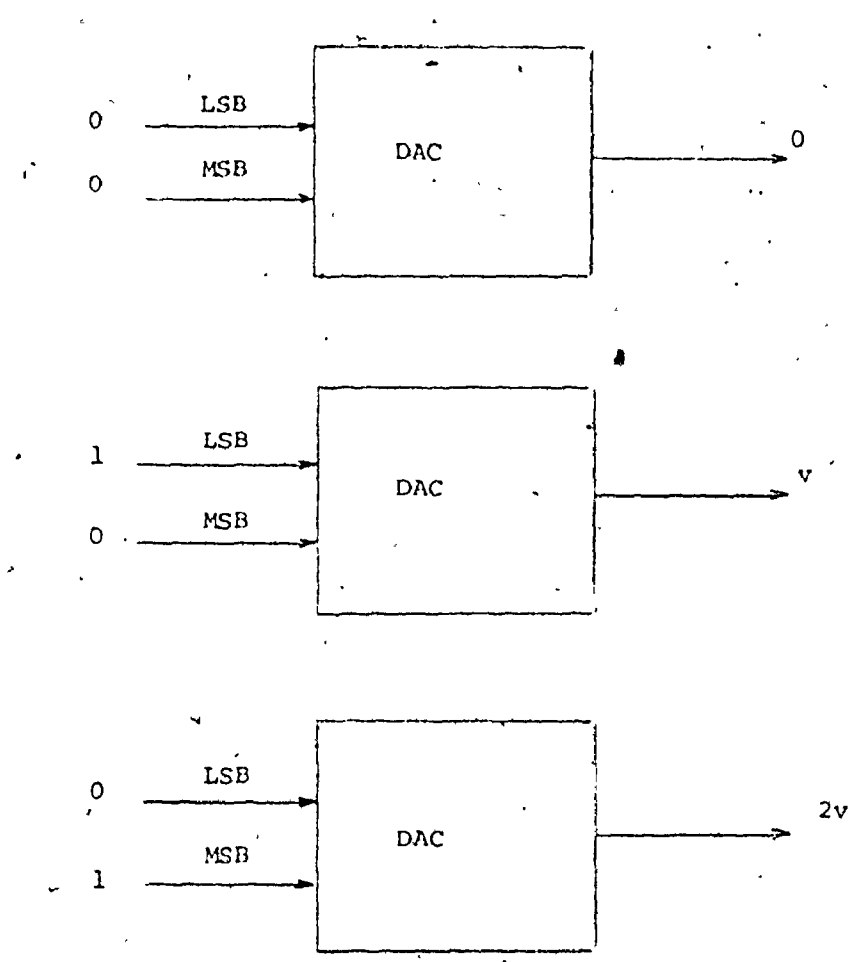


Figure 4.20 Color-encoder circuit diagram.



2v=1.4volt=the maximum permissible video at the electron gun input

Figure 4.21 Digital to analog conversion code.

three outputs.

The same color-coding technique described in section 3.4 is applied in the design of the color-encoder circuit. The implementation of the color-coding technique, as shown in Fig. 4.22 utilizes a read only memory (ROM), to perform the logical function as a practical alternative to simple logic [37] . The ROM unit converts every word applied at the address input to unique set of zeros and ones at the output data lines depending on the program stored in the ROM. This program is directly related to the digital to analog conversion code such that the word stored in every location corresponds to certain specified color. Table 4.5 shows the program stored in the ROM, in binary format. Two 4-bit ROM units are used to provide 6 output lines (with two unused bits) which are applied to three DAC units to drive the red, green and blue guns of the color television monitor.

A manual switch called the color testing switch, controls the path of the input data to the address lines of the ROM units. It operates a logical switch to pass input data when the system sync pulses are "ON" (Fig. 4.19) and the switch is in the low (L) position, and it passes the color testing data when the switch is at high (H) position.

The color testing data are generated by using the horizontal sync pulses to generate 16 different binary words. A frequency divider and a counter are used for this purpose such that the counter changes its output after 16 horizontal pulses. The output binary numbers from 0000 to 1111 are gated

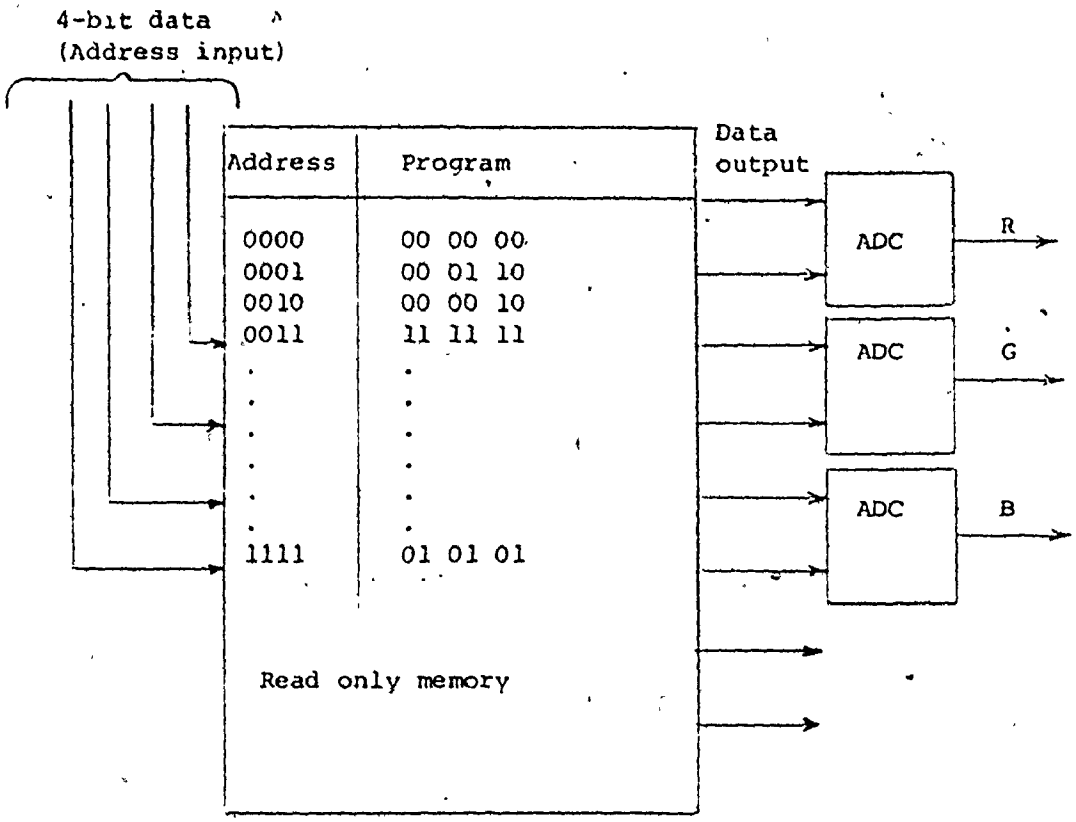


Figure 4.22 The implementation of the color coding technique.

Table 4.5 ROM Program for the selected color code

Address	Program (Binary)		Input Ratio			Color
	ROM 1	ROM 2	B	G	R	
0 0000	00 01	01 01	1	1	1	White
1 0001	00 01	11 01	1	0	1	Purple
2 0010	00 10	10 01	½	½	1	Yellowish purple
3 0011	00 11	11 01	0	0	1	Red
4 0100	00 11	10 01	0	½	1	Orange
5 0101	00 11	01 01	0	1	1	Yellow
6 0110	00 11	01 11	0	1	0	Green
7 0111	00 11	10 11	0	½	0	Dark Green
8 1000	00 11	10 10	0	½	½	Brown
9 1001	00 01	10 10	1	½	½	Blue Violet
10 1010	00 10	01 11	½	1	0	White Green
11 1011	00 01	01 11	1	1	0	White Blue
12 1100	00 01	10 11	1	½	0	Blue
13 1101	00 01	11 11	1	0	0	Dark Blue
14 1110	00 01	11 10	1	0	½	Violet
15 1111	00 11	11 11	0	0	0	Black

with the system sync "ON/OFF" (Fig. 4.19) after adjusting the pulse width, in order to synchronize the data with the raster scanning. Hence, either the input data or the color testing data are applied to the address lines of the ROM units, according to the position of the color testing switch.

CHAPTER 5

COLOR CODE SELECTION AND SYSTEM TESTING

5.1 COLOR CODE SELECTION:

The experimental work described in this section is divided into two separate parts. The object of the first part is the testing of the output color response to the input voltage changes. This determines the approximate amount of the required change in one of the input voltages to cause a noticeable change in the output color. Three different video amplitudes are applied to the red, green and blue gun inputs of the color television monitor, using a three variable resistances and a video signal generator as illustrated by Fig. 5.1. The three inputs are then varied in all the possible ways and the output color changes are carefully observed. It was found that the best results are obtained when the input signal amplitude is changed by an amount approximately equal to half the maximum input video.

The second part of the experimental work is designed to generate all the possible colors which can be produced by applying all the possible combinations of the three inputs of V, ½V and zero volts, where V is the maximum input video level. The number of possible colors is 27 colors and any 16 of these can be selected as the color code.

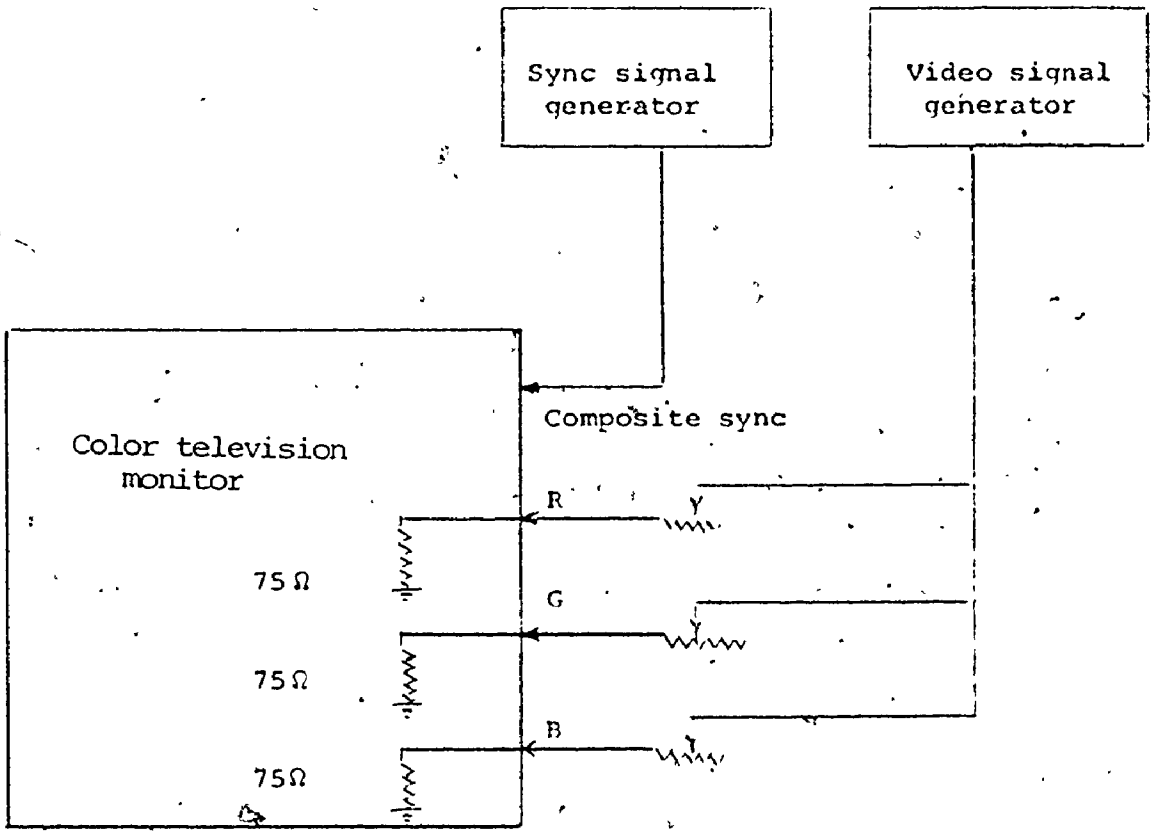


Figure 5.1 Testing the response of the output color on the color TV screen to the change in the input voltage.

A color testing signal generator has been designed and constructed to generate the video signal required to produce those colors on the raster scan of the color television monitor. Different colors are arranged in the form of a horizontal bands. The width of each band is 16 horizontal lines (eight lines each of interlaced fields) as shown in Fig. 5.2.

In the circuit of the color testing signal generator (Fig. 5.3), one 8-bit reprogrammable ROM is used to perform the same function as the two 4-bit ROMs used in the color-encoder circuit. The same digital to analog conversion code (Fig. 4.21) is applied in the design of the ROM program and the three digital to analog converters. The reprogrammable ROM allows modifications in the program to change the colors or re-arrange their order. The program stored in the ROM, which generates the 27 different colors, is listed in Table 5.1.

Figure 5.4 is a photograph of the 27 color bands, of which sixteen can be selected to form the color code in any arbitrary arrangement. Figure 5.5 is a photograph of one of the possible selections and the corresponding program is listed in Table 5.2 with the list of colors.

As shown in the circuit diagram Fig. 5.3, the ROM output data are gated by 100 ns square pulses. This signal tests the response of the color television monitor to a particular frequency, since this rate is the maximum speed at which the memory feeds 4-bit words to the color-encoder. The gating process is also necessary because the TV monitor does not give a good response to frequencies below the frequency of the horizontal

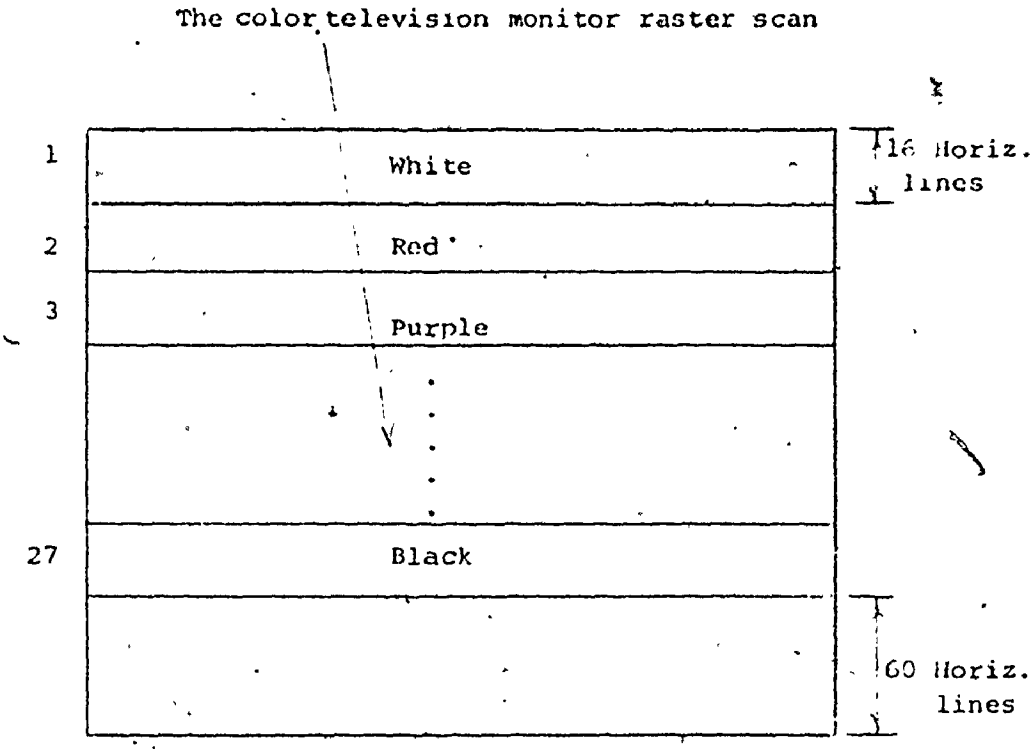


Figure 5.2 The display of 27 color bands.

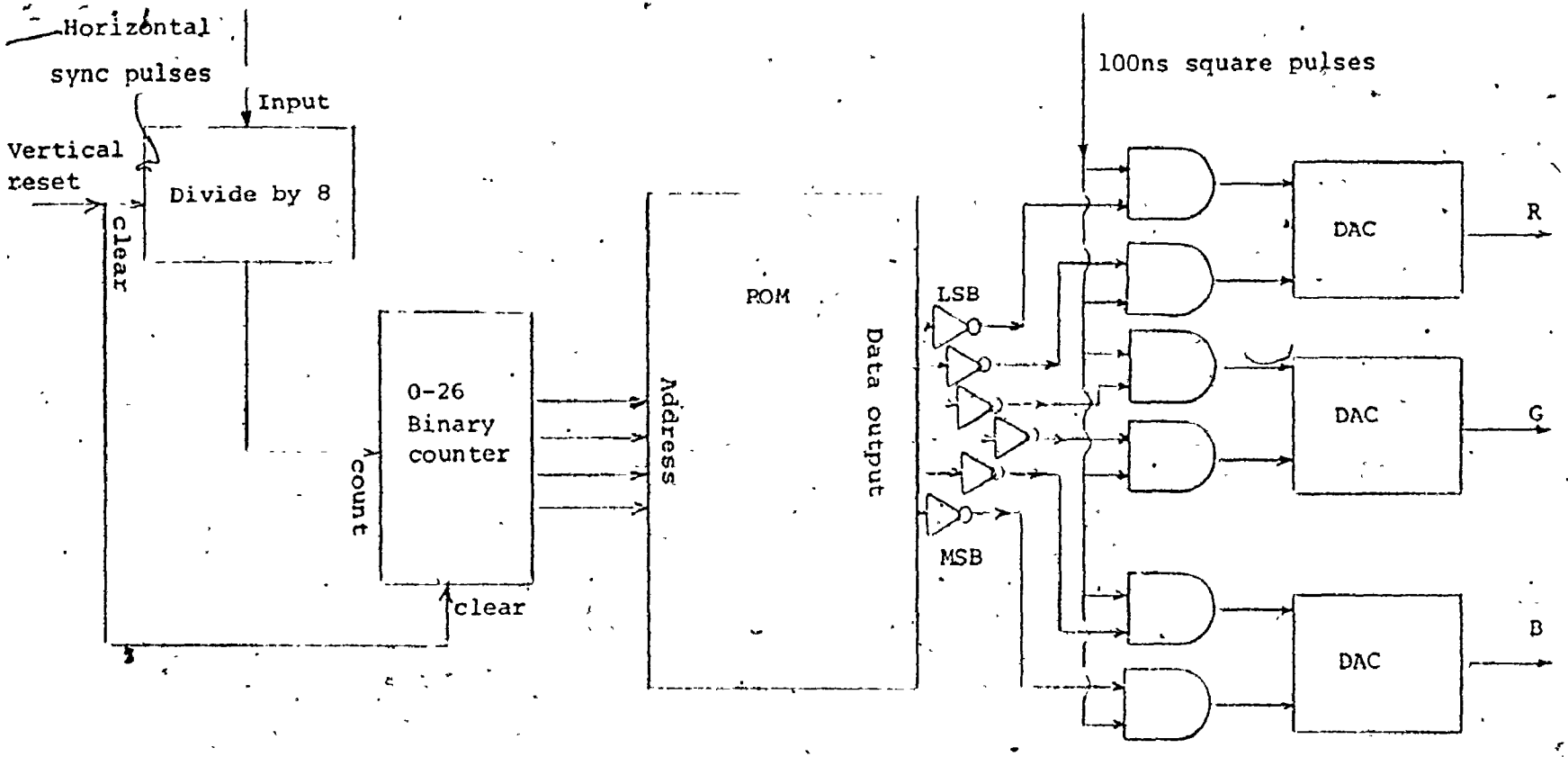


Figure 5.3 The logic circuit of the color testing signal generator.

Table 5.1 ROM Program to generate 27 different colors.

ROM address		Program (binary)	Input ratio		
			B	G	R
0	00000	00111111	0	0	0
1	00001	00111110	0	0	½
2	00010	00111101	0	0	1
3	00011	00011101	1	0	1
4	00100	00101101	½	0	1
5	00101	00010110	1	1	½
6	00110	00100110	½	1	½
7	00111	00101110	½	0	½
8	01000	00101010	½	½	½
9	01001	00011110	1	0	½
10	01010	00011010	1	½	½
11	01011	00111001	0	½	1
12	01100	00111010	0	½	½
13	01101	00110101	0	1	1
14	01110	00110110	0	1	½
15	01111	00110111	0	1	0
16	10000	00111011	0	½	0
17	10001	00011001	1	½	1
18	10010	00101001	½	½	1
19	10011	00010101	1	1	1
20	10100	00100101	½	1	1
21	10101	00100111	½	1	0
22	10110	00101011	½	½	0
23	10111	00010111	1	1	0
24	11000	00011011	1	½	0
25	11001	00011111	1	0	0
26	11010	00101111	½	0	0

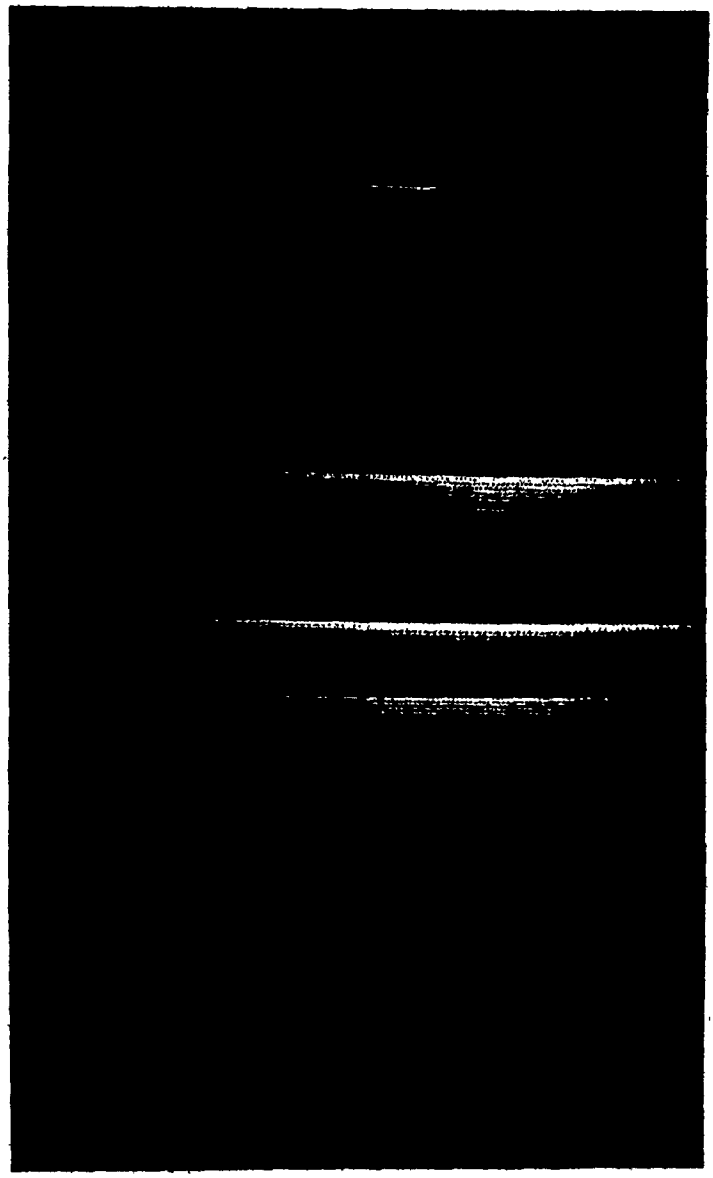


Figure 5.4 Photograph of the 27 color bands produced by the color television monitor.

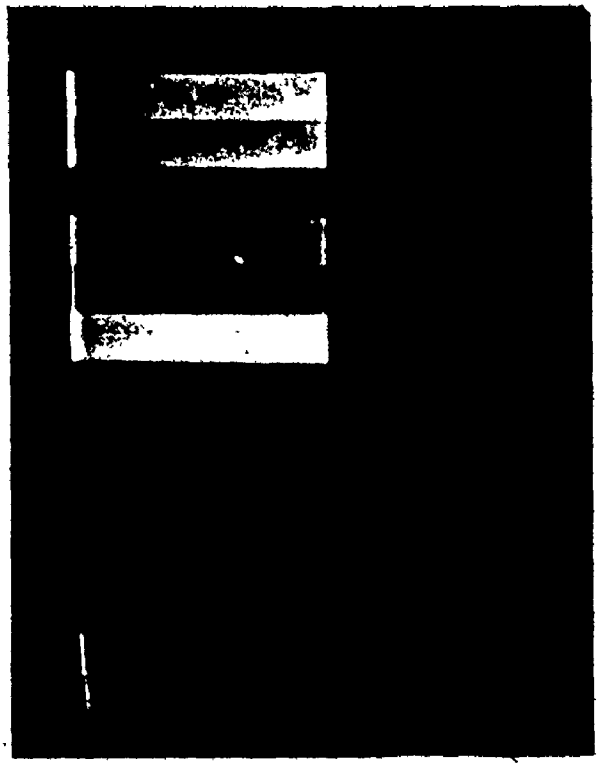


Figure 5.5 Photograph of the selected color code.

Table 5.2 ROM Program for the selected color code

Address		Program (Binary)				Input Ratio			Color
						B	G	R	
0	0000	00	01	01	01	1	1	1	White
1	0001	00	01	11	01	1	0	1	Purple
2	0010	00	10	10	01	½	½	1	Yellowish purple
3	0011	00	11	11	01	0	0	1	Red
4	0100	00	11	10	01	0	½	1	Orange
5	0101	00	11	01	01	0	1	1	Yellow
6	0110	00	11	01	11	0	1	0	Green
7	0111	00	11	10	11	0	½	0	Dark Green
8	1000	00	11	10	10	0	½	½	Brown
9	1001	00	01	10	10	1	½	½	Blue Violet
10	1010	00	10	01	11	½	1	0	White Green
11	1011	00	01	01	11	1	1	0	White Blue
12	1100	00	01	10	11	1	½	0	Blue
13	1101	00	01	11	11	1	0	0	Dark Blue
14	1110	00	01	11	10	1	0	½	Violet
15	1111	00	11	11	11	0	0	0	Black

sync pulses.

5.2 SYSTEM ADJUSTING AND TESTING

5.2.1 Test Card and Test Pattern

A technique has been designed for testing the display system performance. A test signal is applied to the system, stored in the memory, and then displayed on the raster scan of the color television monitor. The display pattern is compared with the expected pattern in order to ensure that the system is operating properly. A test card which replaces the ADC card in the display system, is designed to provide the required signal.

The test pattern shown in Fig. 5.6 is selected for this purpose. The corresponding test signal and its relation with the system timing signals are illustrated by Fig. 5.7. The logic circuit of the test card, for this test pattern, is shown in Fig. 5.8 with two inputs and an output expanded into 4 lines. The output is connected to the 4-bit digital input to the display system. As shown in Fig. 5.7, the field input data and the line input data are available as the 4th and 12th bits of the address counter output. Fig. 5.9 is a photograph of the test pattern displayed during the test showing good agreement with the expected result.

5.2.2 Color Convergence Adjustment:

The color convergence is adjusted for the color television monitor by applying the test pattern signal to the color television monitor and following the adjusting steps as explained

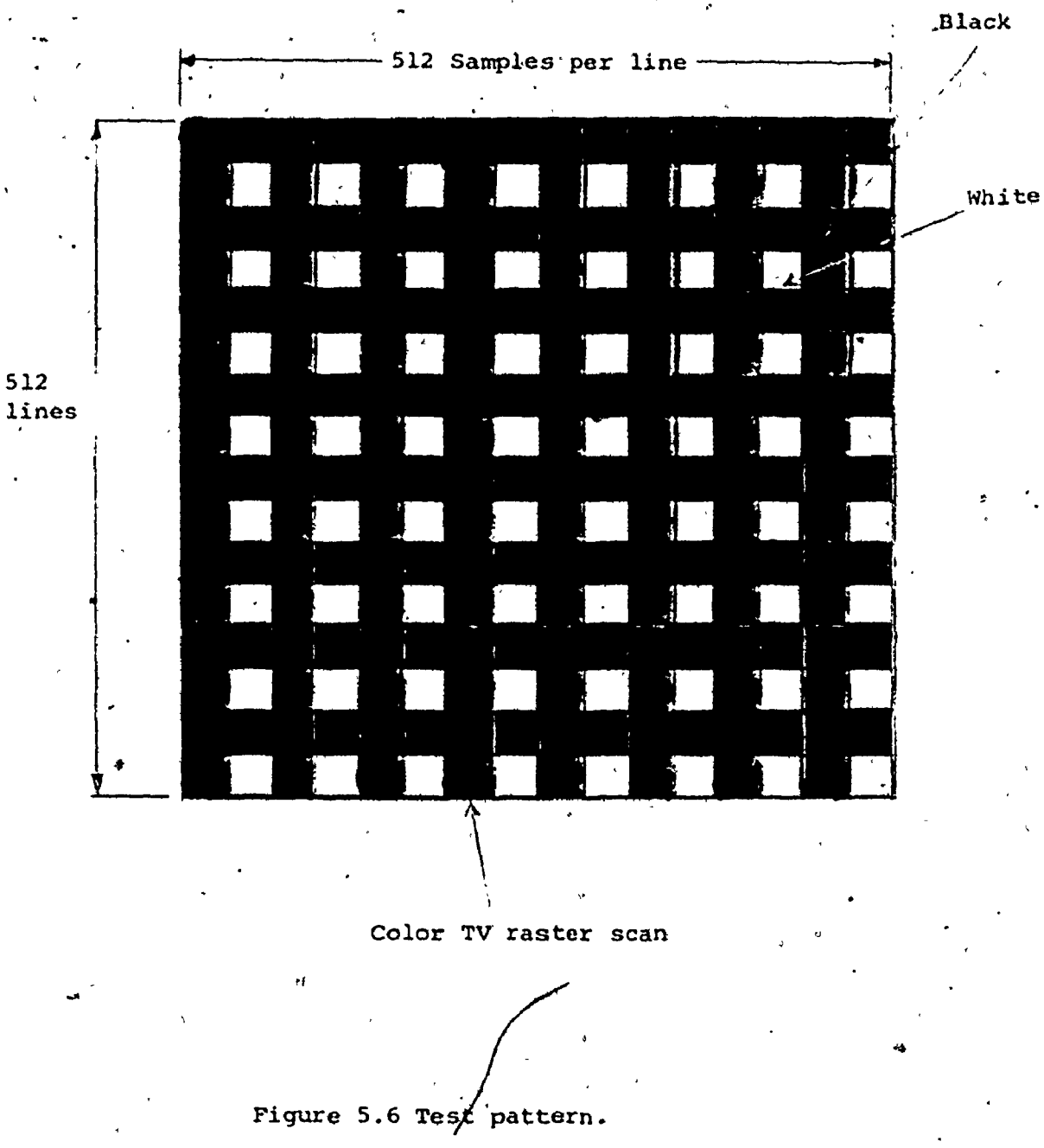


Figure 5.6 Test pattern.

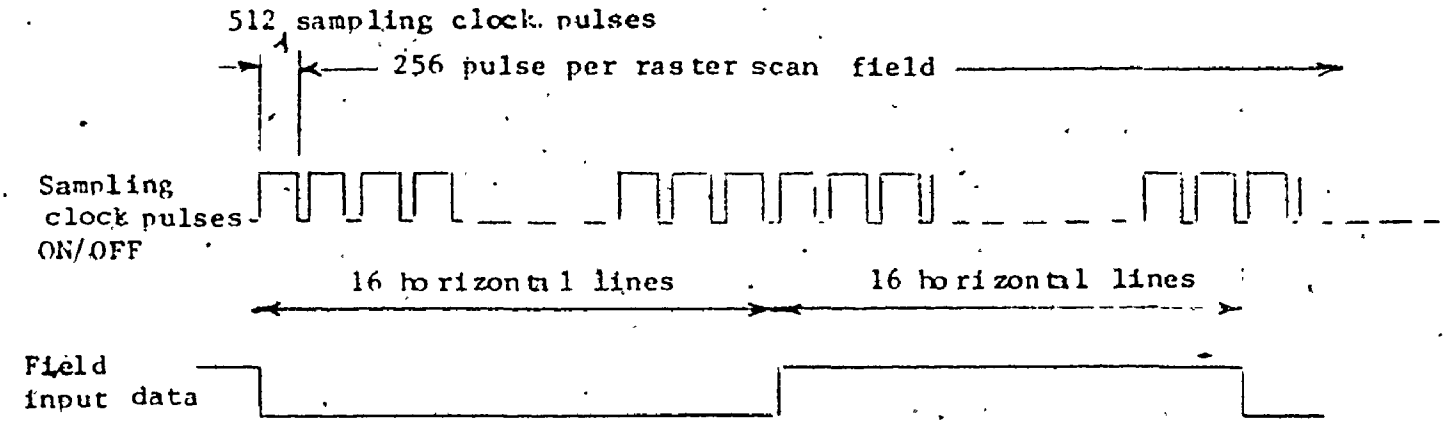


Figure (a)

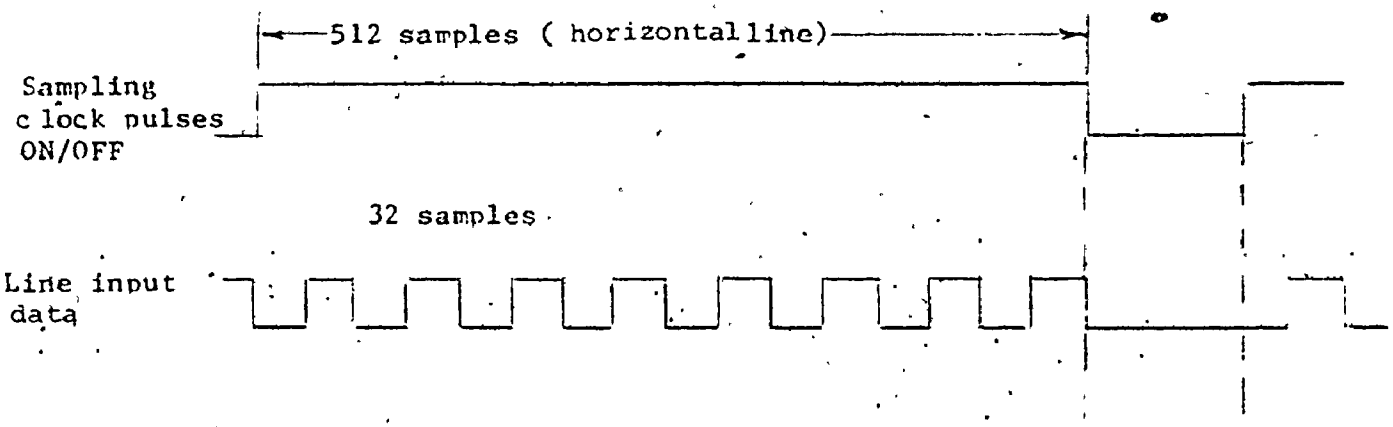


Figure (b)

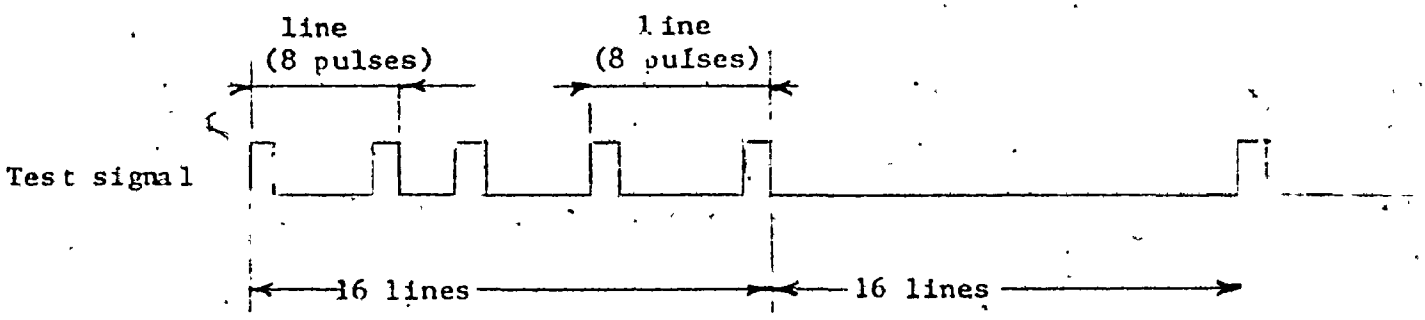


Figure (c)

Figure 5.7 Test signal and its relation with the timing pulses.

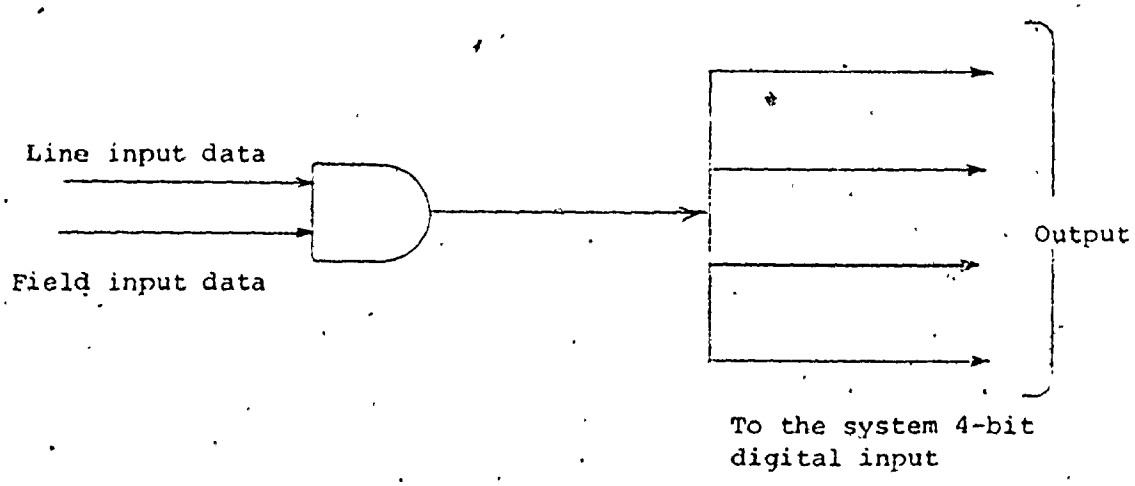


Figure 5.8 Test card circuit diagram.

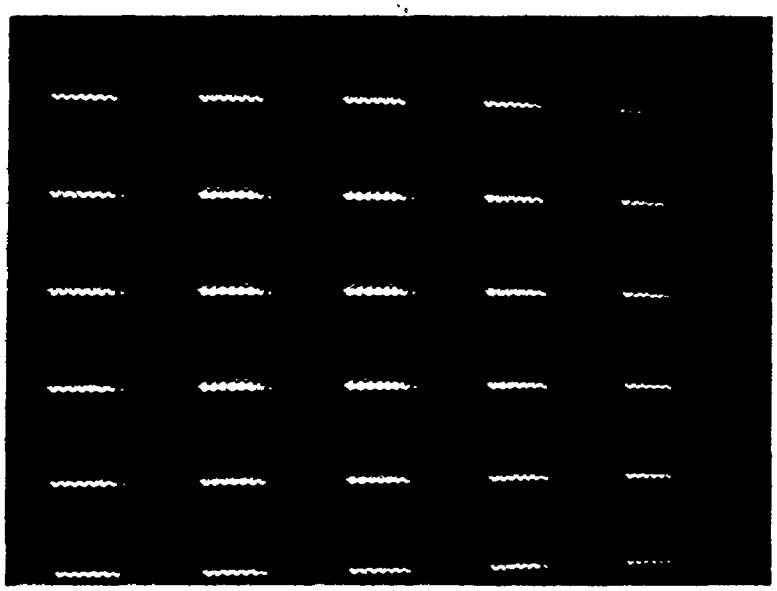


Figure 5.9 A photograph of the test pattern as displayed.

in the operating manual. The test pattern shown by Fig. 4.6 was selected to be suitable for the color convergence adjusting. Thus, the same test card described in Section 4.2.1 is used for this process.

CHAPTER 6

THE PRESENTATION OF RADAR SIGNALS BY THE COLOR-CODED DISPLAY SYSTEM

The display system has been used to present real time radar signals, in order to test the system performance and to demonstrate the color coding technique. The radar signals are recorded on a magnetic tape, using a wide band video recorder, with two video and two auxiliary channels. Two types of video are available: 1. normal video (positive unipolar) which is simply the detected RF echo signal, and 2. MTI video which is the received signal after having undergone MTI filtering. Also, the timing signals (sync pulses, ARP and ACP) are available to generate the azimuth sampling pulses as illustrated in Section 4.2.2.

A series of photographs have been taken for the radar data presentation by the color-coded display system. The MTI video, recorded on two different magnetic tapes (obtained by Communications Research Laboratory staff), have been used for this purpose. The sampling area boundaries have been changed in order to present different areas.

In the following two examples, the vertical axis represents the azimuth; that is, the height of the raster scan (11 ½ inch) corresponds to the sampling area total sector angle. This sector angle is determined by the azimuth sampling pulse rate (ASPR) which is variable. This ASPR is equal to the PRR

divided by a known selectable integer (I). By selecting a smaller integer, a magnification effect is produced as illustrated by the following results.

The horizontal axis represents the range; that is, the width of the raster scan (15 3/8 inch) corresponds to the sampling area range $R_2 - R_1$ (Section 4.2.2). This range is determined by the sampling clock pulse frequency which is constant (1 MHZ). This frequency corresponds to a sampling area range of 41.29 n.m.

Example 1

The tape used for this example was recorded during a spring rain storm at Bogotville Airport, Quebec. The PRR is 1040 Hz and the pulse width is 0.6 μS. The antenna rotation speed is 12 rpm.

Fig. 6.1.a is a photograph of the storm as displayed by the color television monitor. In this case, I = 16 and then ASPR = $\frac{1040}{16}$ = 65 sector sample/second. The antenna rotation is 72° per second, which means that the width of a sector sample is $\frac{72}{65}$ = 1.1°. For 256 sector samples, the sampling area total sector angle is 281.6°.

The same storm is shown in Fig. 6.1.b. after the storm has moved to the east direction.

The presentation of the storm when the total sector angle is 140.8° (ASPR = 130 sector samples/s), is shown in Fig. 6.2.

The effect of changing the ADC maximum digitizing

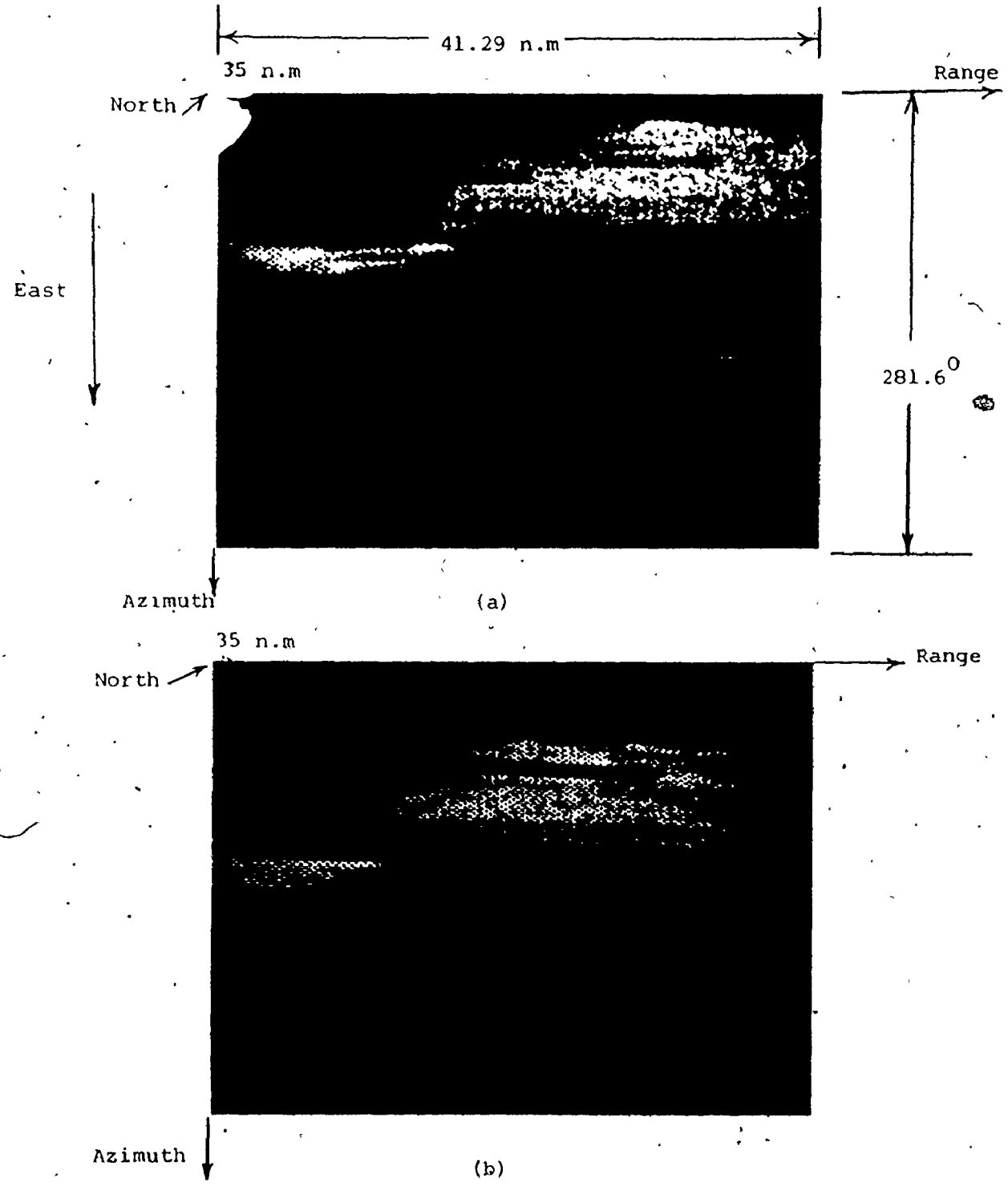


Figure 6.1 The presentation of the rain storm by the display when the total sector angle is 281.6 degrees.

(a) The rain storm at the north-east showing the areas of strong and weak signal.
(b) The storm after it has moved to the east.

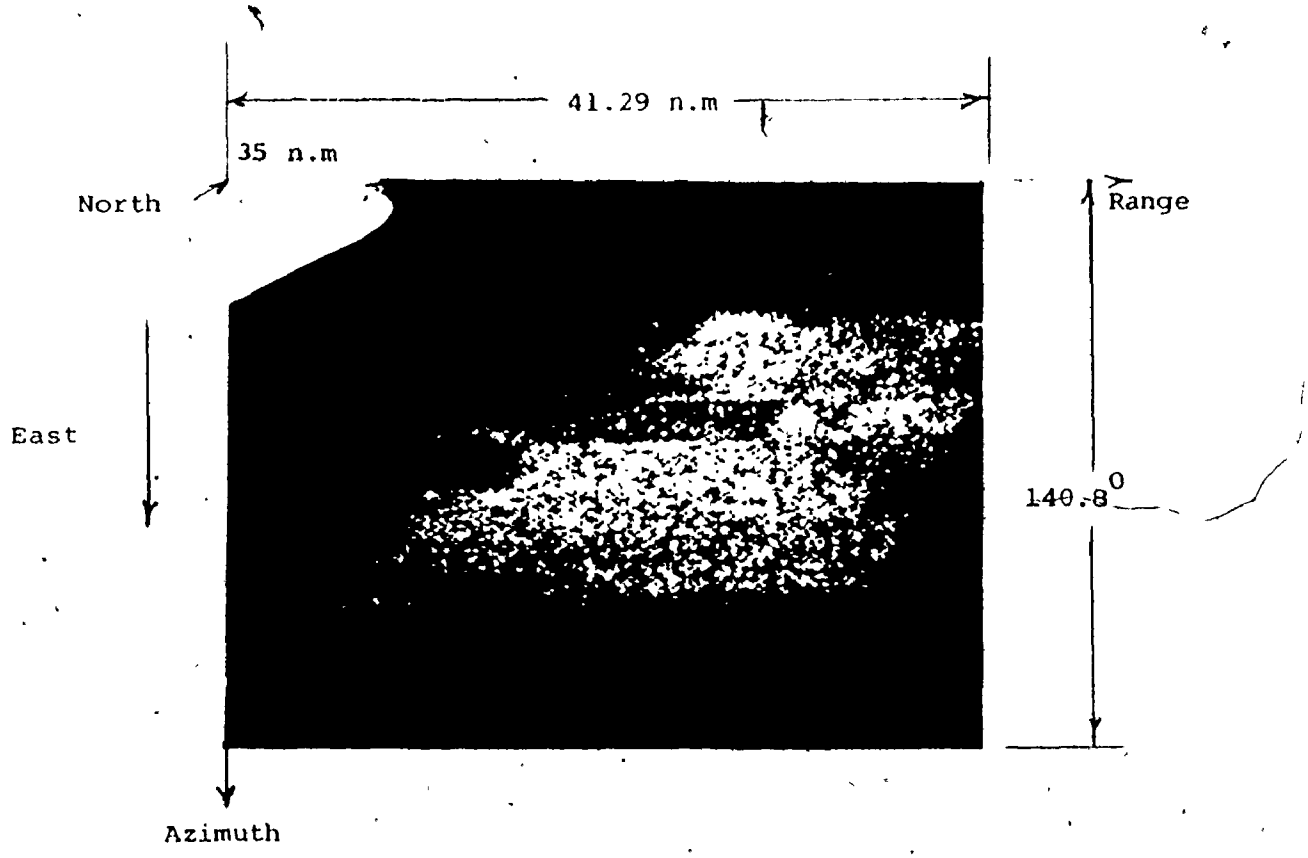


Figure 6.2 The presentation of the rain storm by the display when the total sector angle is 140.8 degrees with the area covered by the storm cloud is expanded showing more details.

level, with respect to the maximum video level, on the displayed colors is illustrated by Fig. 6.3 (a and b). Fig. 6.3.a and Fig. 6.3.b are the same as Fig. 6.2 with a digitizing level below and above the maximum video respectively.

Fig. 6.4 shows the storm as it appears when the total sector angle is 70.4° (ASPR = 260 sector samples/S). The picture concentrates on the northern-most part of the storm cloud.

By decreasing the sector angle to the value 35.2° (ASPR = 320 sector samples/S), different parts of the storm cloud are expanded to show more details. Fig. 6.5.a shows the expansion of the northern-most part of the storm, while Fig. 6.5.b shows the expansion of the centre part of the storm cloud.

Example 2

The tape used for this example was recorded during a severe winter freezing rain storm at Toronto International Airport. The PRR is 400 HZ, and the pulse width is 2 μS. The antenna speed of rotation is 6 rpm.

Two video segments of the freezing rain storm are shown in Fig. 6.5 (a and b) as presented by the display system. The sampling area sector angle in this case is 184.3° (ASPR ≈ 50 sector samples/s).

DISCUSSION

The previous results show clearly some advantages of using the color coding technique. The display indicates the

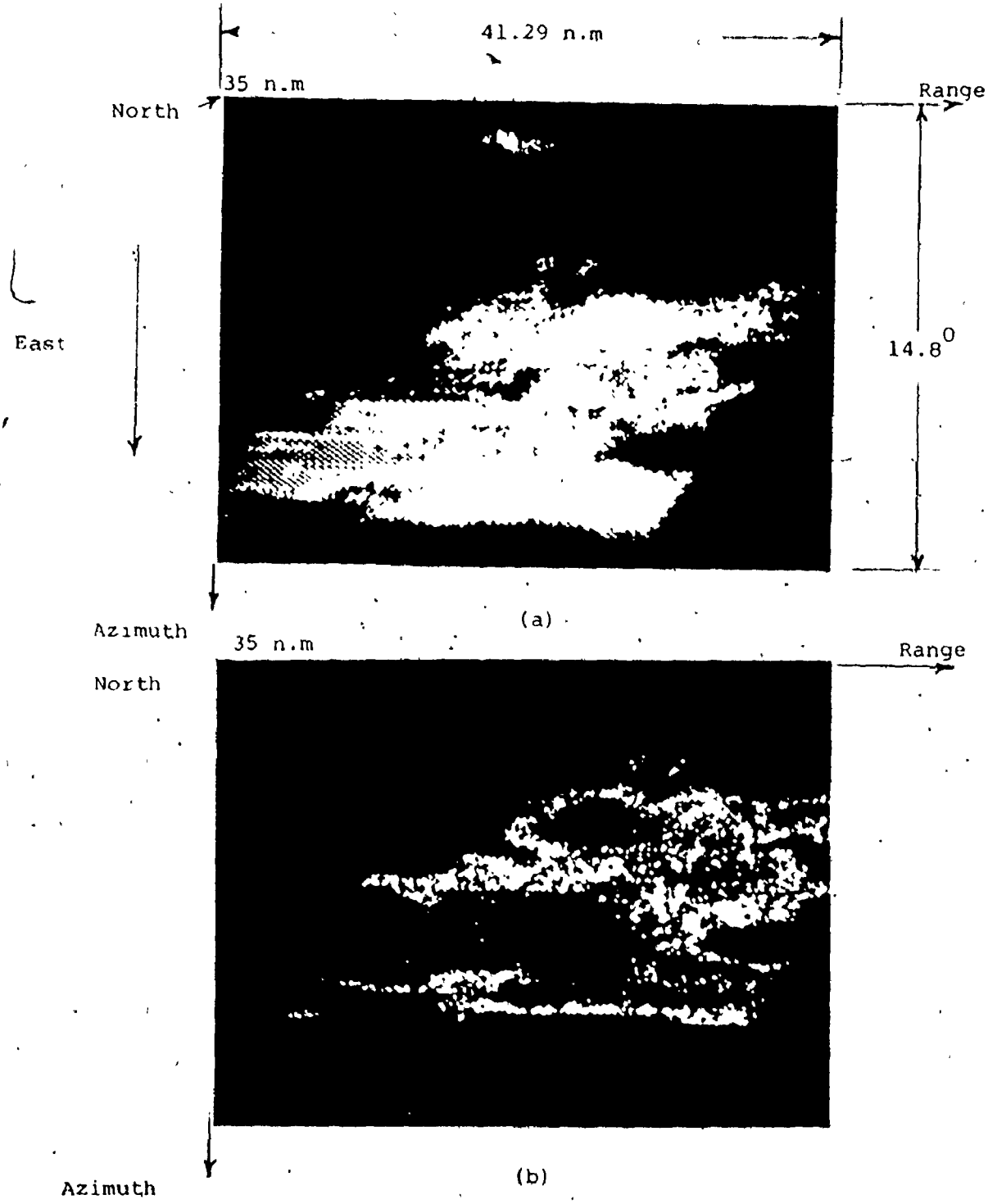


Figure 6.3 The effect of changing the maximum digitizing levels with respect to the maximum video level on the color presentation of data.

(a) The rain storm as presented when the maximum digitizing level is much below the max. video.
(b) The storm when the maximum digitizing level is much above the max. video.

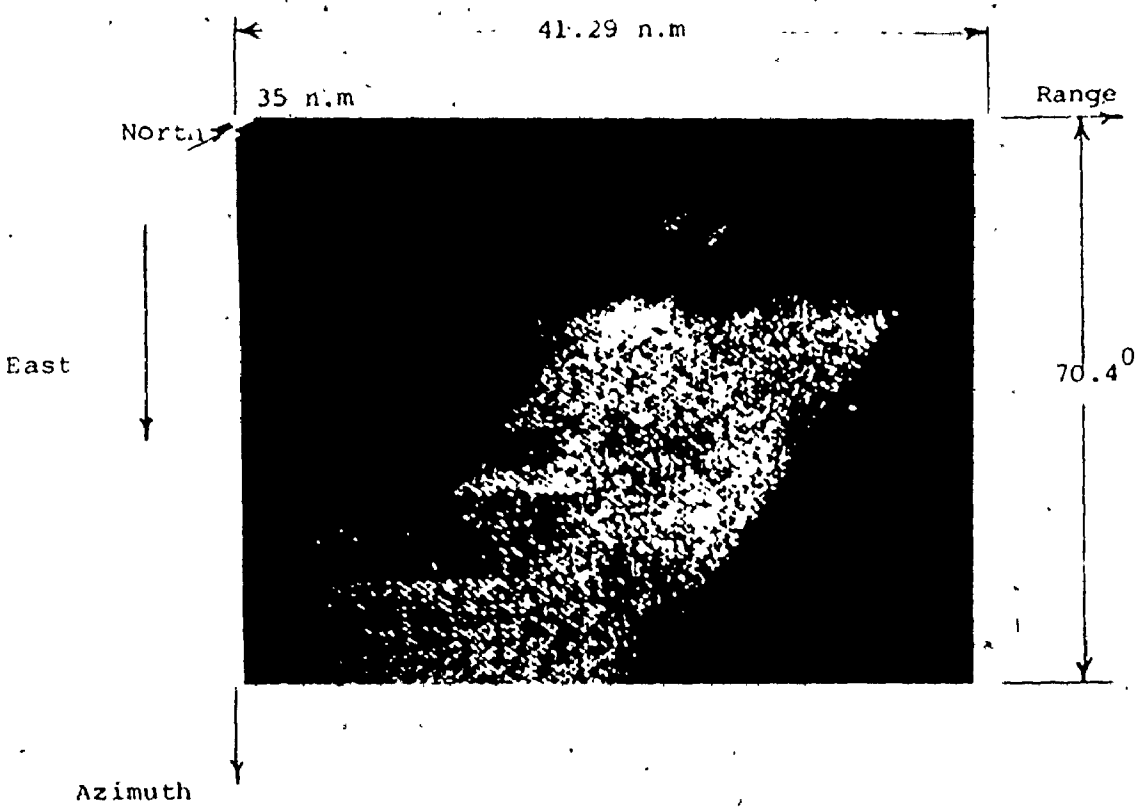


Figure 6.4 The presentation of the rain storm by the display when the total sector angle is 70.4 degrees and the north-most part of the storm cloud is expanded.

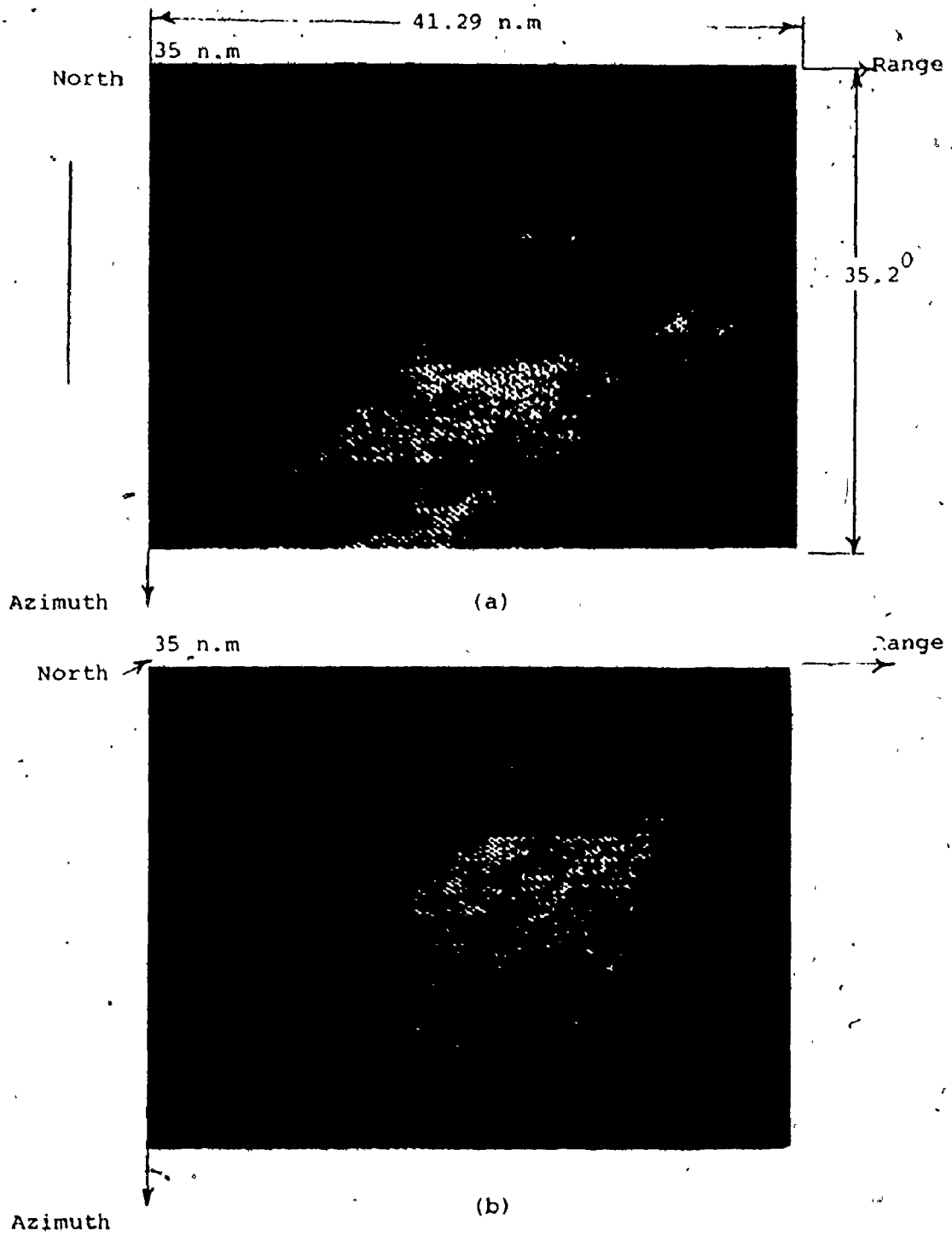


Figure 6.5. The presentation of the rain storm when the total sector angle is 35.2 degrees showing two parts of storm cloud magnified by decreasing the sector angle.

(a) The northern-most part of the rain storm expanded.
(b) The center part of the rain storm expanded.

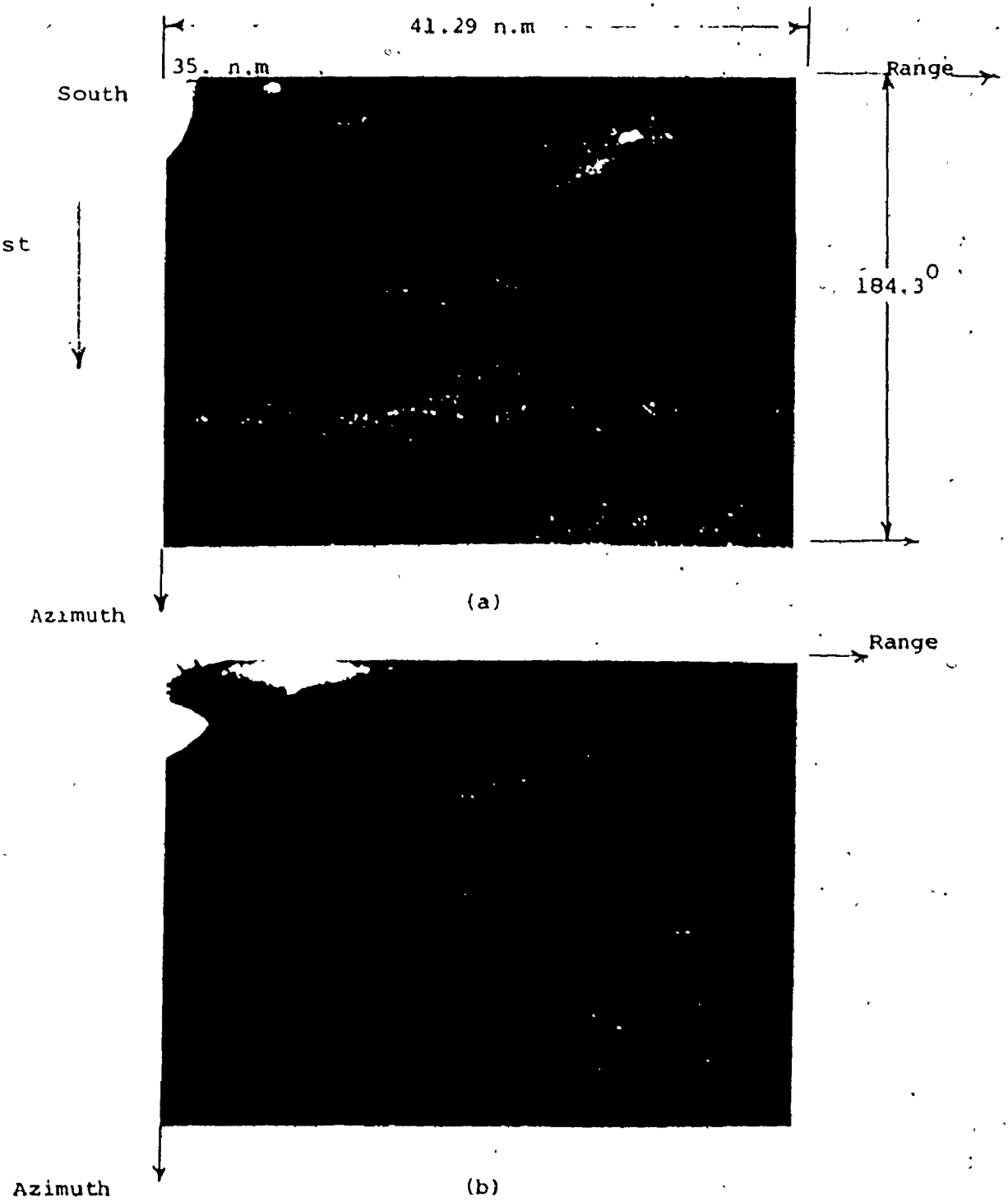


Figure 6.6(a&b) Two video segments of the freezing rain storm as presented by the display when the total sector angle is 184.3 degrees.

strength of the signal in the different points of the reflecting object, together with its area. Sixteen different signal levels are clearly distinguishable. Thus, a third dimension is added to the display picture representing the signal amplitude. This increases the displayed information and eases data interpretation.

As shown in the photographs, the high level areas are represented by the white and red colors. The medium levels are represented, for example, by the yellow, orange and green colors. Finally, the low level areas are represented by the blue colors. On the other hand, noise is represented by dark spots which eases recognition.

By comparing the photographs of Examples 1 and 2, it is evident that the display reflects the nature of the input signal. In the first example, the high density signal is represented by a concentrated cloud. In the second example, the display shows a low density of high level points.

A useful feature of the presented display system is the ability to concentrate and expand small areas of space on the raster scan. This allows examination and study of more details.

The effect of the digitizing level on the color representation, is demonstrated by Fig. 6.3 (a and b). When the digitizing level is below the maximum video, most of the different signal levels are encoded into the white color. Conversely, the signal levels are encoded into the blue colors

when the digitizing level is above the maximum video level. The signal is encoded into the sixteen different colors, when the maximum video level is equal to the maximum digitizing level. This is the case in the other photographs presented in Examples 1 and 2.

CHAPTER 7

CONCLUSIONS AND RECOMMENDATIONS

7.1 CONCLUSIONS

The use of color in data presentation adds a missing variable to the monochromatic display, which is easily recognized by the human eye. Moreover, the color coding adds to the display a third dimension representing the signal amplitude. Thus, more information is displayed in an easy to interpret form indicating the different levels of the input signal.

The system has been successfully designed and it gives excellent results for both the performance test and radar data presentation. The color television monitor is simple to use and provides an excellent color selection.

The large scale random access digital memory and the digital circuitry make the system easy to expand and to integrate with computer installations.

7.2 RECOMMENDATIONS

The introduction of a microcomputer to the system can considerably improve its function, flexibility and performance. Thus, the following advantages can be realized.

1. Signal processing by communicating with the raw data stored in the first card of the RAM system, and storage of processed data

in the second card. Thus, either the raw data or the processed data can be displayed. Many signal processing techniques can be implemented by storing a set of subroutines and a main program in the microcomputer. Any of the subroutines can be executed by entering a control number to the microcomputer through a key board.

2. Adjustable sampling rate which can be achieved by entering a second control number to the microcomputer. Thus, the microcomputer can send a message to the sampling clock to generate sampling clock pulses with a selectable frequency.
3. Changeable color code by storing a number of color codes in the microcomputer and selecting the desired color code by means of a third control number. Then, the microcomputer transfers the new code to the color encoder.
4. Automatically controlled sampling area, data refreshing and switching between modes of operation.
5. Possibility of data format transformation while the data are stored in the memory.

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APPENDIX I

COLOR TELEVISION MONITOR
CTM2/51 TECHNICAL SPECIFICATIONS

Raster	525 lines per picture, 60 fields per interlaced field.
Power	average 125 watts.
Consumption	117 to 135 W (dependent on the CRT beam current drawn, and for nominal mains voltage). Maximum 165 Watts (for maximum CRT beam current and a + 10% mains voltage).
Supply Voltage	the supply voltage is switchable between 110, 130, 150, 220, 240, 260 Volts. No alteration of performance for a ± 10% variation of mains voltage. Supply frequency variable between 45 and 62 Hz.
Signal Inputs (RGB)	RGB non-composite Red, Green and Blue Video 0.7 Vpp ± 6 dB positive 75 Ohms internally terminated. Sync. 2-8 Vpp negative looped through high Z.
Cross Talk	> 50 dB up to 5 MHz, any input to any other.

Max Standing DC on the Inputs	± 5 Volts (all inputs drive a differential input amplifier)
Frequency Response	15 kHz to 6.0 MHz ≤± 0.5 dB at 8 MHz ≤- 1 dB at 10 MHz ≤- 5 dB (gradual roll-off)
Sync	external sync for RGB. Switchable external/internal sync for display of composite input.
Underscan	reduction in height and width w.r.t. normal scan (switchable).
Display Performance	Picture height 11½ inch Picture width 15 3/8 inch
Range of temperature	$+5^0$C to + 35^0C ambient air temperature to meet nominal specifications. -10^0C to $+45^0$C for normal operation.
Relative Humidity	95% for the whole temperature range.
Altitude	normal performance to 10,000 ft (3000 m).
Warm Up Period	1 minute to display 30 minutes to meet specifications.
Automatic Degaussing	on switching on the monitor.

Fuses	all fuses are externally exchangeable	
	all fuses have indicator lamps.	
Dimensions (Fig. A.1.1)	Width	17.77 inch
	Height	18.32 inch
	Depth	23.64 inch
	Weight	40.00 kg

Second Order Controls

All second order controls are located in the front drawer.

Shift	horizontal direction
	vertical direction
Line Time Base	line frequency
	line sync phase
	phase comparator symmetry
Field Time Base	field frequency
	height
	linearity
Scanning Size	switch for underscan/normal scan
Sync.	switch internal/external sync.
Color convergence adjustment	by controls located in the front drawer (1 thorugh 18)
Color Temperature Adjustment	by Controls in the front drawer (p 20, p19, p18)

Gun . Cut-off for red, green, blue..

/ Switches

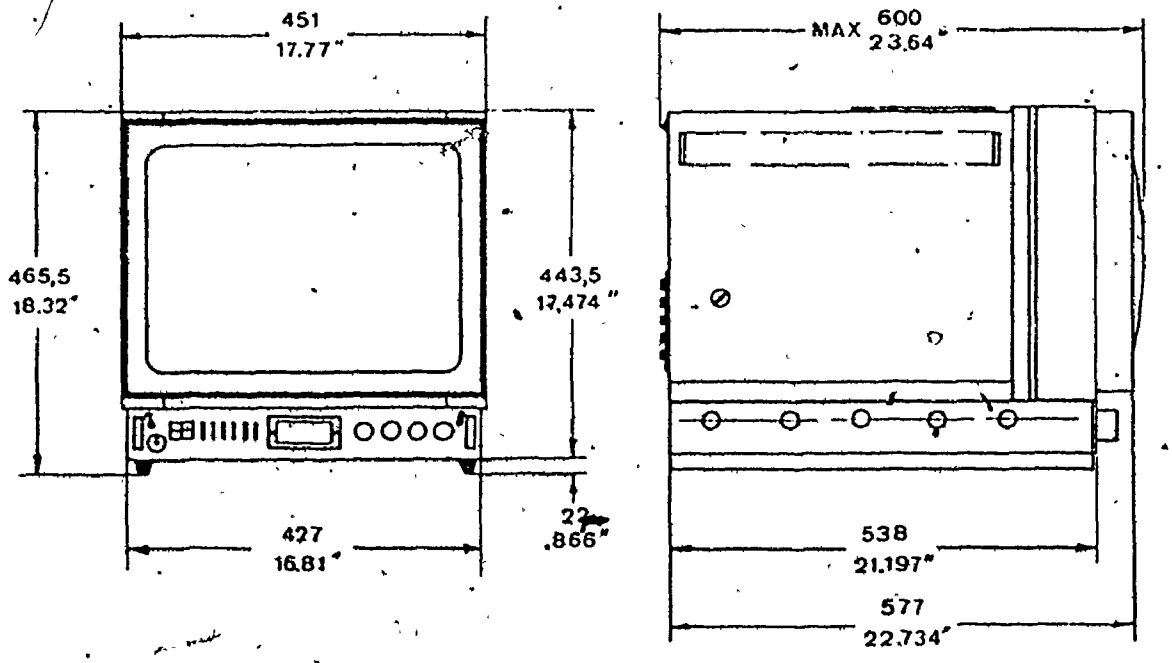


Fig. A.1.1 Dimensions of the CTM2/51

APPENDIX 2

RAM SYSTEM SPECIFICATION AND OPERATION

Table A.2.1 - RAM System General Specifications

ITEM	SPECIFICATIONS
Type of Memory	Random access NMOS semiconductor
Configurations (Each Card):	
3400N	32,768 words by 18 bits
	65,536 words by two 9-bit bytes
Modes of Operation	Read
	Write
	Read/Modify/Write (Split Cycle)
Timing:	3400N
Read Cycle	450ns min
Write Cycle	450ns min
Read/Modify/Write	900ns min*
Access	275ns max
Interface Circuitry	Open collector Output-74S38 TTL
	Input-74SXX series
Logic Levels:	
Logic Zero	+2.5 to +5.0 volts
Logic One	0.0 to +0.5 volt

* Modify Plus Time = Time required for processor to respond to input data from Memory.

Power Requirements:	
ACV to Power Supply	115, 208, 220, 230 (±10%)
Frequency	48 to 63 Hz
Line	1200 Va max
Power Supply Capability:	Volts (±2%) Current (amps max)
DCV	+5 @ 18.5 amps
	+15 @ 14.0 amps
	-15 @ 2.0 amps
ACV to Fans	115 ±10% @ 0.4 amps.

Table A.2.2 RAM System Environmental Specifications

ITEM	SPECIFICATIONS
Operating Conditions	
Ambient Temperature	0°C to +50°C
Thermal Shock	±10°C per hour
Relative Humidity	95% max w/o condensation
Altitude	-1000 ft. to +10,000 ft.
Shipping and Storage	
Ambient Temperature	-40°C to +85°C
Thermal Shock	±40°C per 2 minutes
Relative Humidity	95% max w/o condensation
Altitude	+40,000 ft. max
Mechanical Shock (in shipping container)	Drop Test per MIL-STD-810 Method 516, Procedure V.

Memory Wiring:

Color Code:

The following color code is repeated for every pin group (Table A.2.3) of the connected pins (excluding the unconnected pins).

Red, Orange, Yellow, Green, Blue, Violet, Brown, Gray, White.

Table A.2.3 PAM System interface connector pin assignments.

CONNECTOR				CONNECTOR			
PIN	J12	J13	J14	PIN	J12	J13	J14
A	DI-0	A10	DI-18	BB	--	SC	--
B	RET	RET	RET	BC		RET	
C	DI-1	A11	DI-19	BD	DO-38/18 ③		DO-36
D	RET	RET	RET	BE	RET	--	RET
E	DI-2	A12	DI-20	BF	DO-39/19 ③	--	DO-37
F	RET	RET	RET	BH	RET		
H	DI-3	A13	DI-21	BJ	DO-0	MP ②	DO-18
J	RET	RET	RET	BK	RET	RET	RET
K	DI-4	A14	DI-22	BL	DO-1	DA	DO-19
L	RET	RET	RET	BM	RET	RET	RET
M	DI-5	A15	DI-23	BN	DO-2	MB	DO-20
N	RET	RET	RET	BP	RET	RET	RET
P	--	--	--	BR	--	--	--
R	DI-6	A16	DI-24	BS	DO-3		DO-21
S	RET	RET	RET	BT	RET	RET	RET
T	DI-7	A17	DI-25	BU	DO-4	--	DO-22
U	RET	RET	RET	BV	RET	--	RET
V	DI-8	A18	DI-26	BW	DO-5	BCL-1	DO-23
W	RET	RET	RET	BX	RET	RET	RET
X	DI-9	A19	DI-27	BY	DO-6	BCL-2	DO-24
Y	RET	RET	RET	BZ	RET	RET	RET
Z	DI-10	A110	DI-28	CA	DO-7	BCL-3	DO-25
AA	RET	RET	RET	CB	RET	RET	RET
AB	DI-11	A111	DI-29	CC	DO-8	BCL-4	DO-26
AC	RET	RET	RET	CD	RET	RET	RET
AD	--	--	--	CE	--	--	--
AE	DI-12	A112	DI-30	CF	DO-9	--	DO-27
AF	RET	RET	RET	CH	RET	--	RET
AH	DI-13	A113	DI-31	CJ	DO-10	--	DO-28
AJ	RET	RET	RET	CK	RET	--	RET
AK	DI-14	A114	DI-32	CL	DO-11	EX IN USE ①	DO-29
AL	RET	RET	RET	CM	RET	RET	RET
AM	DI-15	A115	DI-33	CN	DO-12	--	DO-30
AN	RET	RET	RET	CP	RET	--	RET
AP	DI-16	A116	DI-34	CR	DO-13	--	DO-31
AR	RET	RET	RET	CS	RET	--	RET
AS	DI-17	MEMCLR (GR)	DI-35	CT	DO-14	--	DO-32
AT	RET	RET	RET	CU	RET	--	RET
AU	--	--	--	CV	--	--	
AV	DI-38/18 ③	RP	DI-36	CW	DO-15	--	DO-33
AW	RET	RET	RET	CX	RET	--	RET
AX	DI-39/19 ③	WP	DI-37	CY	DO-16	--	DO-34
AY	RET	RET	RET	CZ	RET	--	RET
AZ	--	--	--	DA	DO-17	--	DO-35
BA	--	--	--	DB	RET	--	RET

① In Systems Using Self-Test

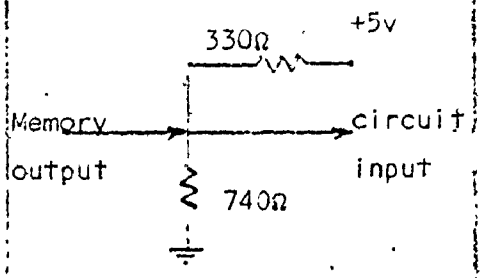
② In Systems Without Power Supply

③ These connections are for bits 38 and 39 in a 40 bit system, and for bits 18 and 19 in 20 bit system.

Table A.2.4 Memory Inputs/Outputs and Interfacing

INPUTS		
Memory Input	Input Signal	Interfacing
DI-0 DI-1 DI-2 DI-3 . . . DI-15	Data output of ADC-memory interface	Direct Connection
DI-16 DI-17	Open	
AI-0 AI-1 AI-2 AI-3 . . . AI-14	Address counter output	Direct Connection
AI-15	High	
AI-16	High	
GR	GRM (High)	Direct Connection
RP	RP	Direct Connection
WP	Low	

Table A.2.4 (continued)

Memory Input	Input Signal	Interfacing
BCL-1 BCL-2 BCL-3 BCL-4	BCL	Direct Connection
SC	High	
	OUTPUTS	
Memory Output	Output Signal	Interfacing
DO-0 DO-1 DO-2 . . . DO-15	Memory-Color Encoder Interface Input Data	
DO-16 DO-17	Open	
:A	Open	
MB	Open	

APPENDIX 3

HARDWARE DETAILS FOR THE DISPLAY SYSTEM

A.3.1 Sync Signal Generator

Table A.3.1 Functions of the integrated circuits used for the construction of the sync signal generator (Fig. A.3.1)

Package Number	Function
1	Crystal oscillator for the master clock
2	Divide by 2
3	Divide by 4
4 & 5	Divide by 10 each
6	Divide by 2 and by 5
7 & 8	Binary counters for the divide by 109 circuit (Fig. 4.8.b)
9	6 inverters
10	8 input NAND gate for the decoder (Fig.4.8).
11	D-FF for the divide by 109 circuit
12	Two mono. mult. for generating pulses B and C from A (Fig. 4.8.a)
13	Mono. mult. for adjusting horizontal sync pulse width
14	Mono. mult. for adjusting equalizing sync pulse width.
15	Mono. mult. for adjusting vertical sync pulse width.

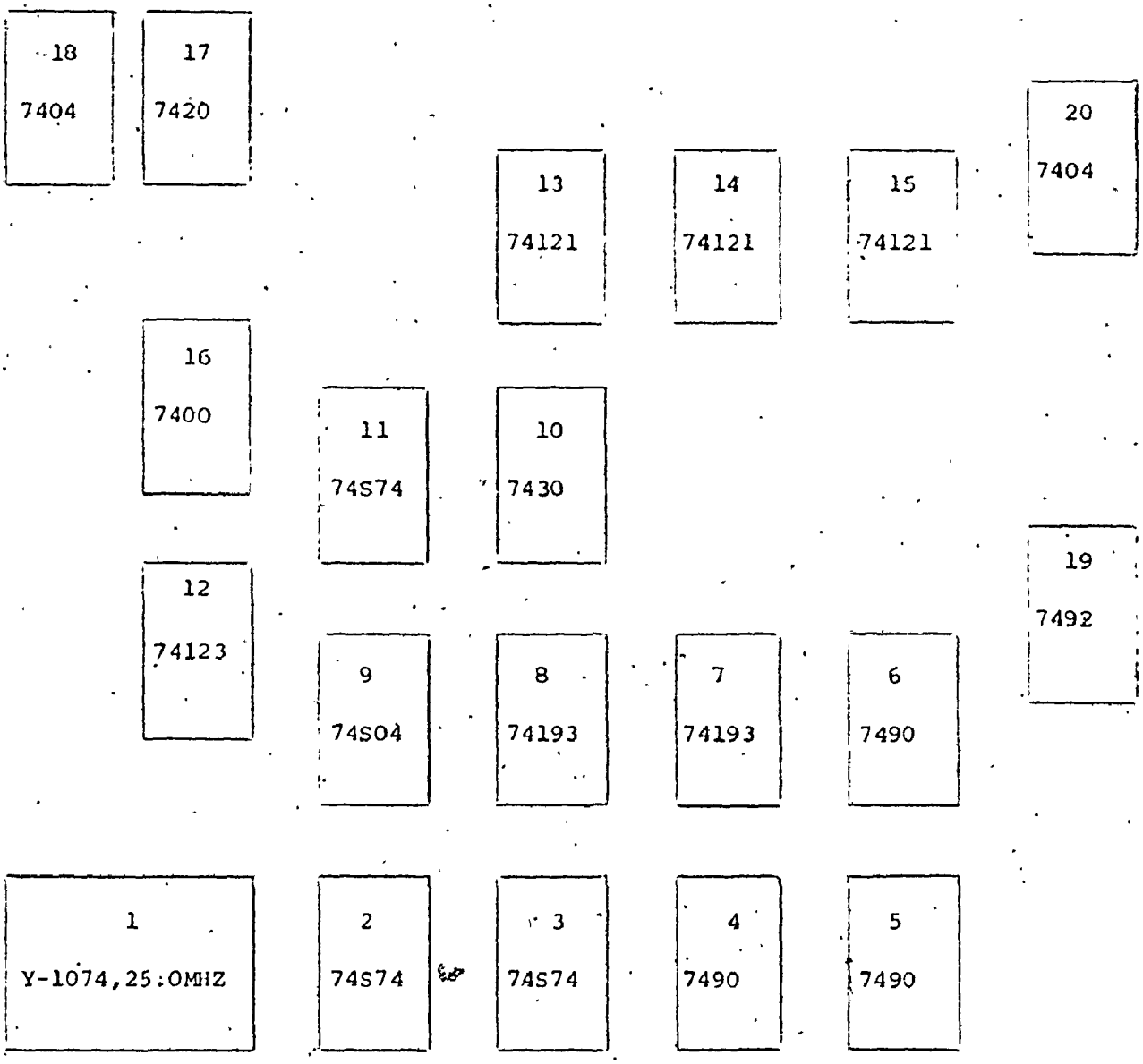


Figure A3.1 Circuit lay out and integrated circuits for the sync signal generator.

Table A.3.1 (contd)

16 & 17	NAND gates
18	6 inverters
19	Divide by 3 to generate system sync.

A.3.2 ADC-Memory Interface

A.3.2 ADC-Memory Interface:

Table A.3.2 Functions of the Integrated Circuits Used for the Construction of the ADC-Memory Interface (Fig. A.3.2)

Package Number	Function
1 → 9	Shift registers number 1 → 9 (Fig 4.16)
10	NAND gates
11	6 Inverters
12	Divide by 2 and divide by 4

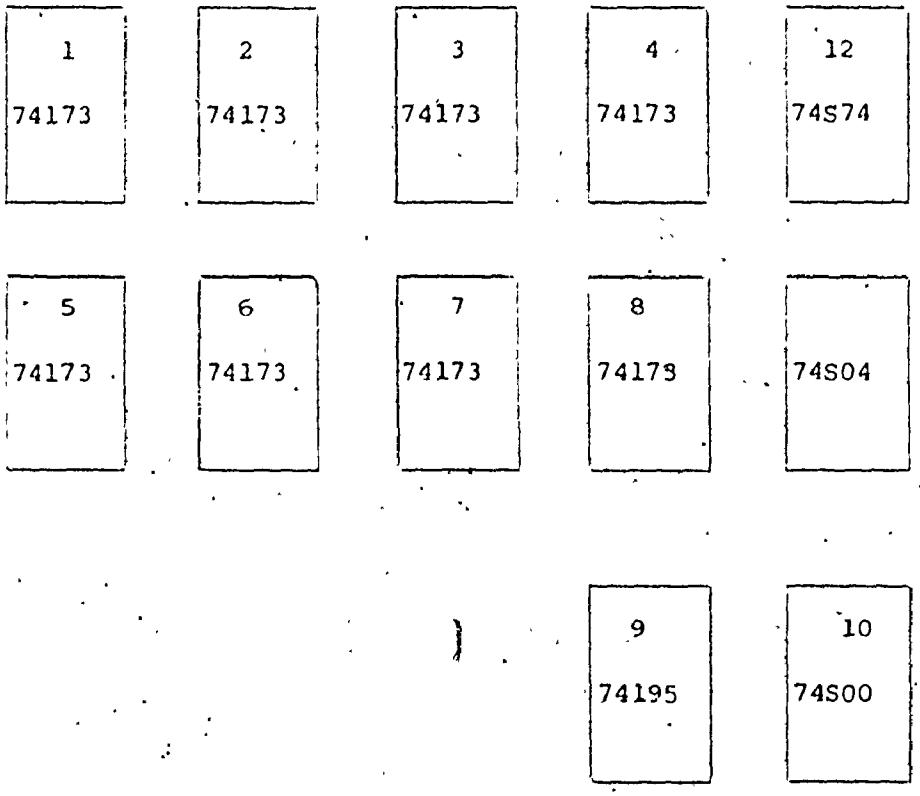


Figure A3.2 Circuit lay out and integrated circuits for the ADC-memory interface.

A.3.3 Addressing and Timing Circuit:

Table A.3.3 Function of the integrated circuits used for the construction of the addressing and timing circuit (Fig.A.3.3)

Package Number	Function
1 → 4	Address counter with 1 as the least significant 4 bits, and 4 as the most significant 4 bit
5	NAND gates
6	6 Inverters
7	NAND gates
8, 9	Counter for 256
10, 11	Mono.mult. for generating a general reset pulse at the switching between modes of operation.
12	NAND gates
13	6 Inverters
14	Mono.mult. for adjusting RP signal pulse width.
15	NAND gates
16	6 Inverters
17	Mono.mult. for adjusting azimuth sampling pulse width
18, 19, 20	Counter for 512
20	Sampling clock (Fig A. 3.4)

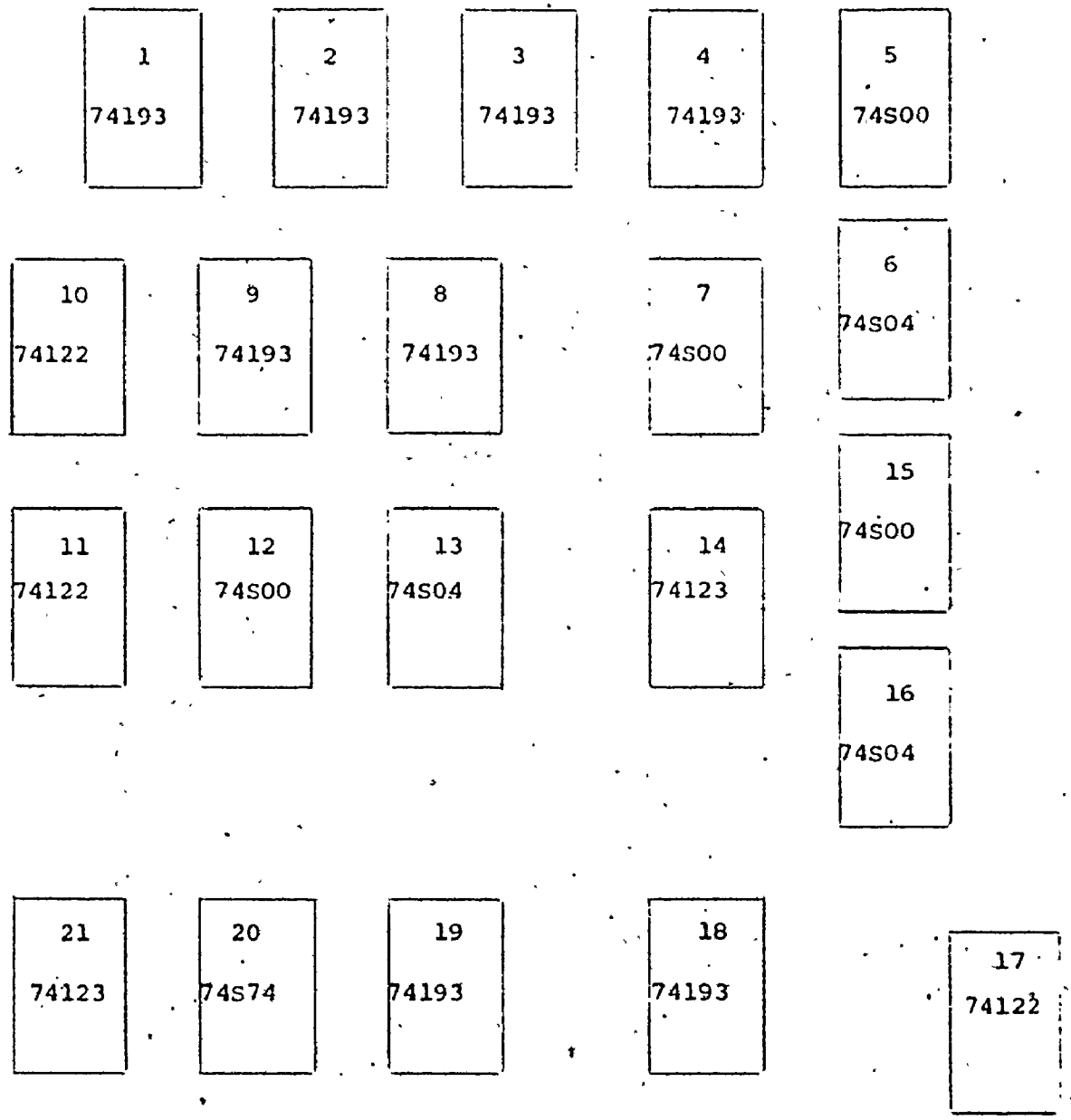


Figure A3.3 Circuit lay out and integrated circuits for the addressing and timing circuit.

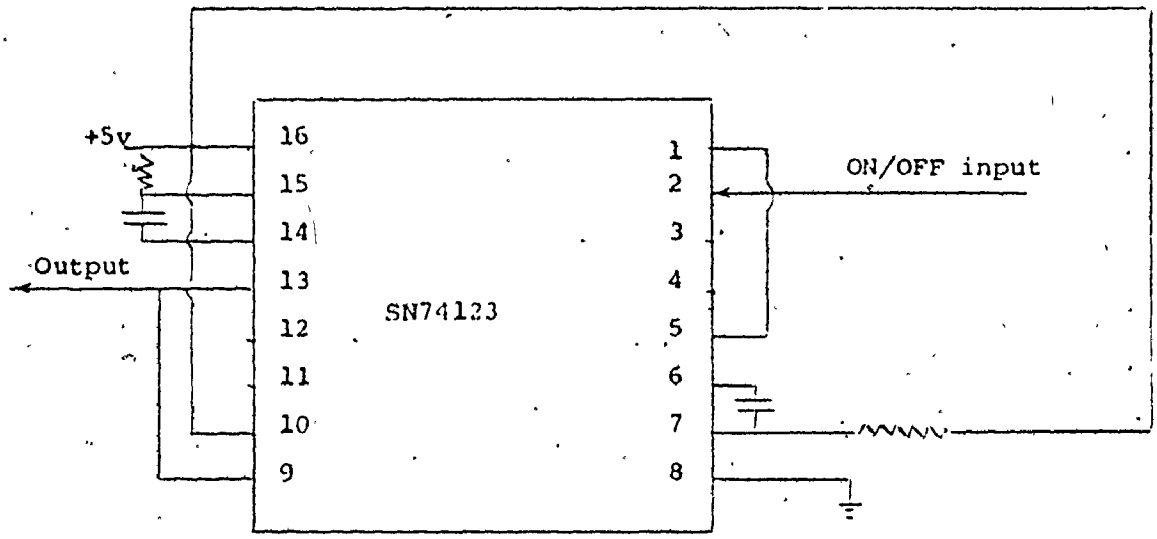


Figure A3.4 Sampling clock cicuit.

A.3.4 Memory-Color Encoder Interface

Table A.3.4 Functions of the integrated circuits used for the construction of the memory-color encoder interface (Fig. A.3.5)

Package Number	Function
1 + 8	Shift registers 1 + 8 (Fig. 4.19)
9	NAND gates
10	Mono. mult. for generating a pulse for memory cycle initiation with the switching from writing to reading modes of operation
11	Inverters
12	Shift register 9
13	Inverters
14, 15	Divide by 4, the latter for generating R_5 (Fig. 4.19)
16, 17, 18	Counter for 512
19	Mono. mult. for adjusting the pulse width of SR9 data input
20	OR gate to generated R pulse for the R-S FF when the carry of 512 counter is on or during the general reset pulse.
21	R-S FF

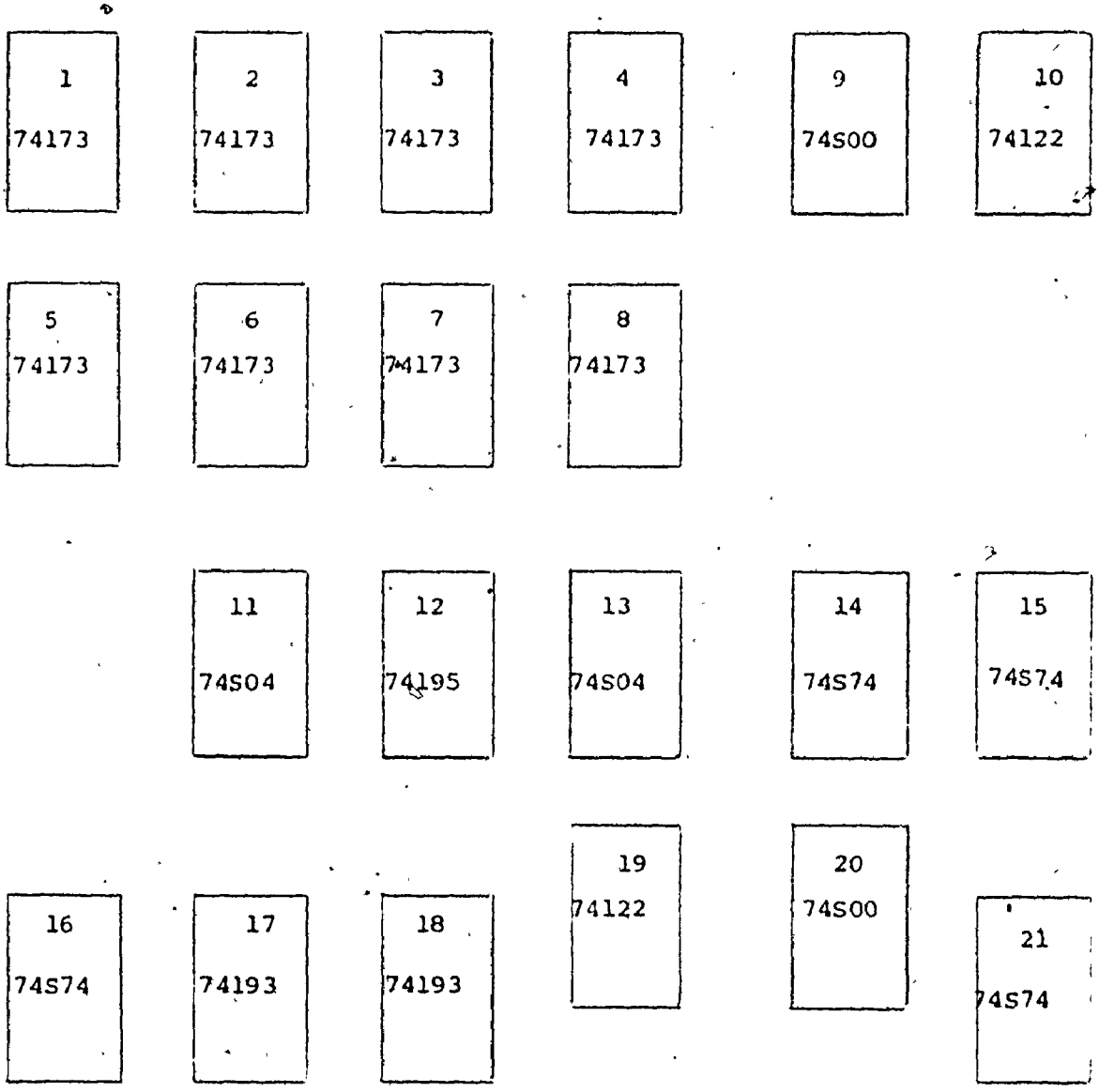


Figure A3.5 Circuit lay out and integrated circuits for the memory-color encoder interface.

A.3.5 Color-Encoder

Table A.3.5 Functions of the integrated circuits used for the construction of the color encoder (Fig. A.3.6)

Package Number	Function
1	Divide by 16
2	4-bit binary counter
3	6-Transistors for DAC
4	Mono. mult.
5	NAND gates for testing data
6	Inverters for data output from ROMs
7	Two NAND gates for gating data with system sync
8	OR gates to gate the input and testing data
9	ROM 1
10	ROM 2
11	Inverters
12	NAND gates for input data
13	Inverters
14	Inverters

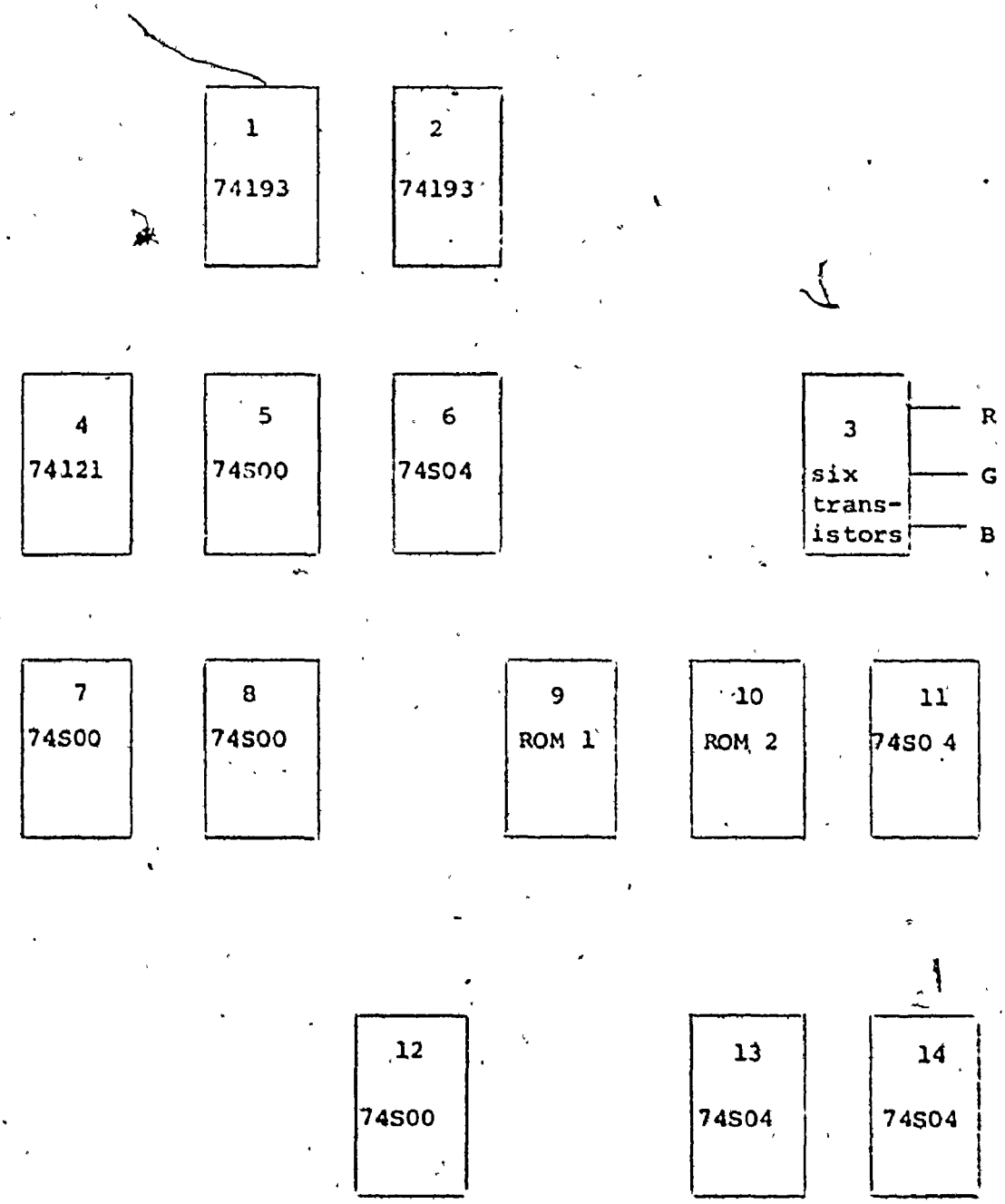


Figure A3.6 Circuit lay out and integrated circuits for the color-encoder.