

**Fabrication and Characterization of Si/Si_{1-x}Ge_x -Based
Double Heterojunction OptoElectronic Switches (DOES)
and
Heterojunction Field Effect Transistors (HFET)**

by

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The Si/Si_{1-x}Ge_x -Based DOES and HFET

Abstract

The fabrication and characterization of the double heterojunction optoelectronic switch (DOES) and the heterojunction field effect transistor (HFET) in the Si/Si_{1-x}Ge_x materials system is described. The significant achievements of this work are summarized below.

The theory of operation of the DOES and HFET are reviewed. A computer-based, one-dimensional, analytical model is used to calculate the current-voltage characteristics and operational parameters of the DOES. From this, the design of the inversion-channel Si/Si_{1-x}Ge_x heterostructure is shown to contain a manifold parameter space. For example, the switching voltage of the DOES is shown to be extremely sensitive to the magnitude of doping in the charge sheet. In the HFET, the threshold voltage is calculated to have a non-linear dependence on the magnitude of the doping in the charge sheet.

The measured switching voltages and currents compare well with the calculations of the model. Separately, the effects of illumination and temperature on the dc electrical characteristics of the device are investigated. Illumination is seen to reduce the switching voltage and holding current. With decreasing temperature, the switching voltage and holding current are observed to increase. The effects of illumination and temperature are explained as phenomena related to carrier injection (or the lack thereof).

An account of the fabrication of these devices is given in detail. A self-aligned technology for the Si/Si_{1-x}Ge_x -based HFET was developed using the aluminum gate as a mask for reactive ion etching and ion implantation procedures.

Oscillatory electrical behavior of the DOES is examined. Self-induced oscillations are shown to be correlated to the regime of negative differential resistance. The dc current-voltage characteristics of the DOES are demonstrated to be affected by this oscillatory behavior. In addition, an enhancement in the optical emission over a narrow range of drive currents in the DOES is shown to be a result of device oscillations.

Changes in the electrical characteristics of the DOES in response to third terminal current injection are measured for both active layer contact and inversion layer contact. Contact to the inversion layer is shown to be more effective than a third terminal contact to the active layer. These experimental observations are supported by the computer-based model. Concurrent usage of optical and electrical injection to affect the I-V characteristic of the device is demonstrated. Electrical extraction via the third terminal is shown to negate the effect of optical injection.

The highest reported transconductance in a Si/SiGe-based metal-semiconductor FET is found in the HFETs reported in this thesis. Peak transconductance of 8mS/mm is measured for a depletion mode device. Subthreshold slope is measured as 720mV/decade and a high frequency 3-dB point for voltage gain is seen to be 1.8GHz.

The suitability of this technology for integration is examined by demonstrating a Reset-Set Flip-Flop which is comprised of two HFETs and a three-terminal DOES. The range of operational voltages for the circuit are shown to be determined primarily by the operational characteristics of the DOES. Gate leakage from the HFET is seen to hinder circuit performance.

Dedication

To Diane, for making it easy.

Publications and Presentations

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CHAPTER 1

INTRODUCTION

It is arguable that no other technology has had as much of an impact on society as the transistor and related devices. Bardeen and Brattain [1] could hardly have foreseen the uses and abuses of the technology spawned by their device - 'a semiconductor triode'. Within thirty years, we have become a society which is dependent upon telecommunications and information processing to satisfy the most basic human needs. Since the first transistor, technological and conceptual developments in devices and systems have taken place at a frenetic pace. Starting from the bipolar junction transistor (BJT) of 1948, transistors based on the effect of an electric fields such as the metal-oxide-semiconductor field-effect transistor (MOSFET) [2], the insulated gate field-effect transistor (IGFET) [3], the metal-semiconductor field-effect transistor (MESFET) [4], the junction field-effect transistor (JFET) [5], and the semiconductor-insulator-semiconductor field-effect transistor (SISFET) [6] have all been realized.

The introduction of heterostructures in 1962 [7] has extended existing device concepts as in the case of the heterojunction bipolar transistor (HBT) [8] and has invigorated research into entirely new types of transistors such as the resonant-tunneling hot electron transistor (RHET) [9]. In most cases, the impetus for development has been to realize devices that are: i) fast and have high current drive capabilities in order to satisfy capacitive loads; or ii) have very low power consumption requirements while at the same time have very stable and well-defined operating states. The latter requirements arise when the device is used as

a switch rather than as a driving element. The logical state of the switch represents a variable or bit of information. However, a single transistor is not intrinsically a bistable device. Bistability is achieved by combining two transistors. One way to optimize speed and lower power consumption is to make the device smaller. Device processing engineers have made strong efforts in this area. Transistors with gates as narrow as 500 Å have been obtained in which intrinsic device capacitance has been reduced to fF [10]. Materials research is critical for many of the most recent developments in device performance. For example, strained layer growth of semiconductor heterostructures has allowed the incorporation of very high mobility materials [11] which have improved the speed of devices. Also, the use of very thin layers, where doping and composition are well controlled, have manifested quantum size effects within devices. Quantum effects, such as those due to carrier confinement, have improved device performance by enhancing carrier transport [12] and have introduced entirely new device phenomena into the design arena [9].

1.1 Technology Directions and System Considerations

For information processing circuits such as memory chips, all of the aforementioned operational attributes are desired. Silicon-based very large scale integration (VLSI) of the MOSFET [13] now dominates information processing circuits. Each MOSFET must be able to drive the capacitive load associated with subsequent devices in the circuit, switch operating states quickly, and use as little power as possible. The capacitive load in VLSI comes not only from the following devices in the circuit, but also from the interconnecting metal wire. In fact, it

is this interconnect capacitance which at present is the dominant capacitive element in VLSI and, therefore, the factor which limits circuit speed [14]. This so-called 'interconnect bottleneck' is unavoidable if electrons are used to transport a signal to the next device. A solution to this bottleneck is to use light to carry information either interchip or intrachip using waveguides or free-space optical links. Optical interconnects offer an number of basic advantages over electrical interconnects [15]:

- a) They can be more densely placed than electrical wires and can even intersect pathways.
- b) Propagation delays will be at least one-third shorter, with no dependence on number of interconnect branches. This is simply because photons travel approximately three times faster than electrical signal on strip lines. In addition, with metal interconnects, each branch off the interconnect adds capacitive load and increases the propagation delay.
- c) Electrical transmission lines need to be terminated with a load which matches the impedance of the interconnect to avoid reflections which add to the power requirement of the signal. Using optical interconnects, power requirements are determined only by the sensitivity of the photodetector and interconnect losses.

These advantages have been recognized by the telecommunications industry as seen by the drive to implement optical-fiber based networks. If light is chosen to carry signals, perhaps some of the electrical-to-optical and optical-to-electrical conversions which are required can be avoided.

Recently, there has been some interest in developing devices and monolithically integrated circuits which are sensitive to an optical signal and re-emit that signal after some signal processing [16, 17]. These opto-electronic integrated circuits (OEICs) can be used as pre- or post-processors of signals and information from Si-based VLSI circuits in a hybrid scheme or, potentially, even replace it. Introducing photons into information processing and storage methodologies has, and will continue to, drive development into entirely new device concepts and functions.

An example of this development is the inversion-channel family of devices, as manifested in the GaAs/AlGaAs alloy system. These include: the double heterojunction opto-electronic switch (DOES) [18]; the heterojunction field-effect transistor (HFET) [19]; the bipolar inversion-channel field-effect transistor (BICFET) [20]; and the two- and three-terminal inversion-channel laser [21, 22]. Some of the opto-electronic and electronic devices introduced above are designed to provide amplification while others are used as switches. Devices that have distinct bistable operating states such as the DOES have also been the subject of investigation. Using this technology, a number of OEIC demonstrations have been reported [23-25], although no performance comparisons to Si-based processors has been made to date.

Devices based on direct bandgap and high mobility materials have been available to system designer for some time but Si-based circuits have continued to be used for mass produced electronic processors. In effect, although state-of-the-art discrete Si-based devices do not compare well with those based in III-V alloys, the demands of the system as a whole require the properties of Si. These considerations include cost, reliability, and reproducibility. The exception to this is GaAs-based monolithic microwave integrated circuits [26]. Here, in this purely

electronic application, GaAs-based circuits are desired for their high-frequency capabilities. However, even this niche for GaAs-based circuits is being threatened by the recent introduction of $\text{Si}_{1-x}\text{Ge}_x$ alloy heterostructures [27]. A $\text{Si}_{1-x}\text{Ge}_x$ -based HBT has already been demonstrated at IBM with $f_T \approx 75$ GHz [28]. In addition, these $\text{Si}_{1-x}\text{Ge}_x$ alloys have also been shown to be luminescent with efficiencies far greater than one would expect for the alloy of two indirect-gap materials [29]. The potential for efficient luminescence and the hetero-offset which accompanies the smaller bandgap $\text{Si}_{1-x}\text{Ge}_x$ layer grown on Si may make this materials system a candidate for OEICs. A number of opto-electronic device concepts using the Si/ $\text{Si}_{1-x}\text{Ge}_x$ have been proposed or realized to date [30-32].

In Si-based VLSI of complementary MOS (CMOS) technology, the p-channel transistor is the 'weak' device from a performance perspective. Si-based, p-channel MOSFETs are typically two or three times the size of their n-channel counter-parts [33]. The size difference comes about simply because of lower p-channel mobility and a desire to balance the current from both types of devices. Researchers hope that from improvements in p-channel devices using $\text{Si}_{1-x}\text{Ge}_x$ -based heterostructures, the greatest gains in VLSI packing density and speed will be realized.

A parallel development has been BICMOS - the incorporation of bipolar transistor (BJT) into CMOS circuits. The goal here is to use the current drive ability of BJTs and the low power consumption and high density of CMOS to yield a faster circuit with minimum power penalty and avoiding a costly reduction in gate length of the MOSFETs. A logical extension of this is to bring together the best attributes of $\text{Si}_{1-x}\text{Ge}_x$ -based HBTs and CMOS technology. However, much work is still needed in the area of device fabrication in order to realize a $\text{Si}_{1-x}\text{Ge}_x$ -based VLSI circuit.

1.2 Material Properties of Si/SiGe

Si-based VLSI is a mature technology and has dominated information processing for 30 years with good reason. Silicon has exceptionally good material properties for making circuits. It is an abundant element with little or no volatility or toxicity and a relatively high melting point (1415°C). A high melting point allows a high thermal budget for device fabrication. Silicon readily forms a stable oxide which has excellent dielectric properties and has fair mechanical strength. The SiO₂ is used in VLSI CMOS technology as an diffusion and implant mask and also as a platform for metal interconnects.

As a semiconductor material, silicon is capable of changing resistivity over 10 orders of magnitude by doping with group III or V elements but its energy bandgap of 1.12eV is indirect which precludes it from being used as a material for optical sources. Germanium (group IV) also has good mechanical properties and an indirect bandgap of 0.66eV.

Compound semiconductor materials such as GaAs, InP, and related quaternaries and ternaries have been predominately used in opto-electronic devices and circuits. This, in spite, of the fact that in these materials, devices are much harder to fabricate than those based on silicon. In addition, devices based on the III-V materials have operational characteristics which are difficult to control. However, the III-V materials, in general, have better intrinsic electron and hole conduction characteristics. Electron mobility (at 300°C) in GaAs (8500cm²/V-s) is twice that of Ge (3900cm²/V-s) which, in turn, has mobility approximately three times larger than Si (1500cm²/V-s) [34]. Thus, discreet device applications which require the highest frequency operation are generally fabricated using the III-V material system [35]. Another advantage of the

compound III-V materials is the ability to grow alloys of the compounds commensurately on the underlying substrate. Thereby, the best properties of each III-V compound and alloy can be used in a device design. A clear example of this is to compare the performance of the homojunction and the double heterojunction laser [36].

This design flexibility is now available with Si- and Ge-based devices. The alignment of Si and $\text{Si}_{1-x}\text{Ge}_x$ conduction and valence bands is type I if the $\text{Si}_{1-x}\text{Ge}_x$ layer is grown commensurately on Si(001) substrate. That is, the narrower $\text{Si}_{1-x}\text{Ge}_x$ energy gap falls within the wider gap of the Si. Thus, a thin strained layer of $\text{Si}_{1-x}\text{Ge}_x$ between unstrained layers of Si forms an energy well for both holes and electrons. However, the well for electrons is quite shallow compared to that for holes in $\text{Si}_{1-x}\text{Ge}_x$ layers grown on Si [37]. Commensurate growth of $\text{Si}_{1-x}\text{Ge}_x$ strained layers on Si(001) results in a biaxial in-plane compression of the $\text{Si}_{1-x}\text{Ge}_x$ layer and an extension normal to the interface. The effect of the strain on the indirect bandgaps can be estimated using a deformation potential theory [38] and is found to decrease the energy gap of the $\text{Si}_{1-x}\text{Ge}_x$ (Fig. 1). That decrease is seen predominately in an increase the valence band hetero-offset. For example, for $\text{Si}_{1-x}\text{Ge}_x$ with Ge fraction 0.25 grown on Si(001), $\Delta E_v \approx 0.185\text{eV}$ and $\Delta E_c \approx 0.02\text{eV}$ [37].

A number of devices have been reported in the literature which take advantage of the hetero-offset between $\text{Si}_{1-x}\text{Ge}_x$ and Si. These include n- and p-channel MODFETs [39,40], PMOS [41], and the p-channel BICFET [42]. From these and other studies [43-46] an enhancement in p- and n-channel mobility in the strained $\text{Si}_{1-x}\text{Ge}_x$ layers compared to unstrained, bulk material has been both predicted and observed.

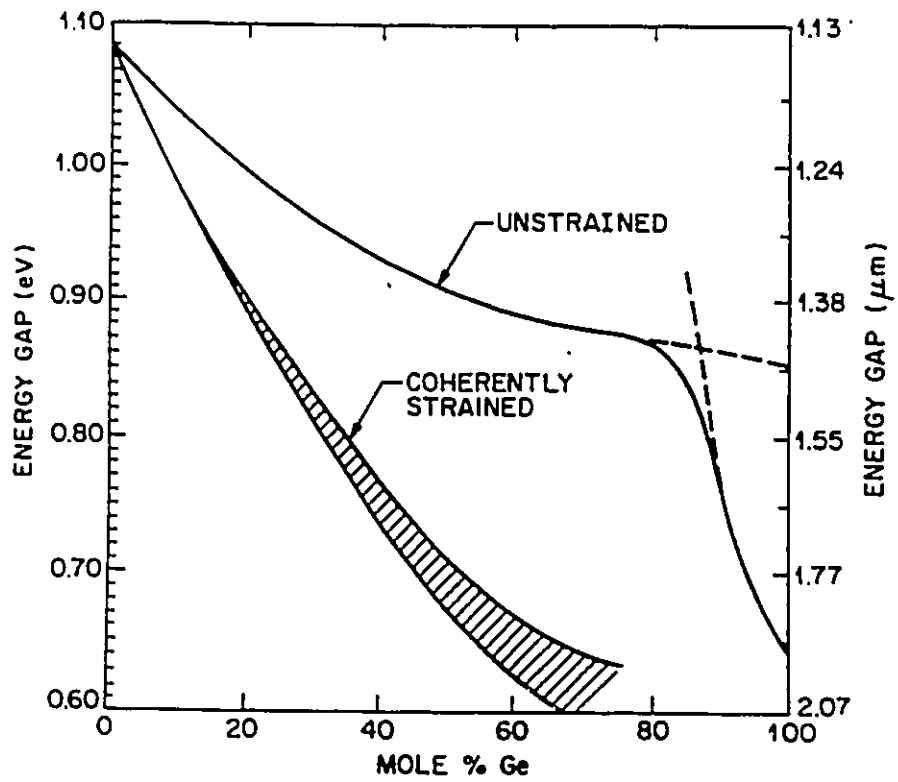


Figure 1.1: The lowest energy indirect bandgap of coherently strained $\text{Si}_{1-x}\text{Ge}_x$ alloys on Si(001) substrates.

Although, strain in these heterostructures appears to benefit device performance, some less appealing properties and issues must be dealt with. The thickness of the strained $\text{Si}_{1-x}\text{Ge}_x$ layers must be restricted to avoid strain relaxation in the form of misfit dislocations. If pervasive throughout a device, these dislocations can act as fast recombination/generation centers [47], increase dark currents in $\text{Si}_{1-x}\text{Ge}_x$ -based photo-detectors [48], or simply reduce the strain-induced contribution to bandgap lowering.

Heterostructures incorporating strained $\text{Si}_{1-x}\text{Ge}_x$ are restricted to layers smaller than the critical thickness (h_c). Experimentally, the maximum thickness which can be grown on a Si(001) is considerably larger than values predicted by the early theory of strain relief. People and Bean [49] have proposed extensions to this theory [50-53] and have obtained a good fit to the experimental data. Heterostructure designs which require $\text{Si}_{1-x}\text{Ge}_x$ layers close to h_c will at the same time place restrictions on device processing. In particular, the amount of heating the wafer experiences (the so-called 'thermal budget') must be kept low in order to keep the $\text{Si}_{1-x}\text{Ge}_x$ layer in the metastable strained state [54]. This may or may not exclude a $\text{Si}_{1-x}\text{Ge}_x$ -based heterostructure from the same processing steps used to make MOSFETs. In the formation of a MOSFET, several high temperature (>700°C) processes, including the formation of the gate and field oxide and the annealing of ion implantation damage for the source and drain contacts, are required [55].

The $\text{Si}_{1-x}\text{Ge}_x$ -based MESFET is easier to fabricate than the MOSFET since no gate oxide deposition or growth is required. Pearsall and Bean [40] were able to restrict processing temperatures to 700° C in the fabrication of p-channel $\text{Si}_{1-x}\text{Ge}_x$ MODFETs. A BF_2 implant of the source and drain was used. The degree of dopant activation desired and the annealing of crystal damage after an

implant will determine the ultimate processing temperatures required in the fabrication of a $\text{Si}_{1-x}\text{Ge}_x$ MODFET.

1.3 Objectives of the Thesis

It is the objective of this work to experimentally and theoretically investigate two- and three-terminal DOES devices and the p-channel HFETs based in the $\text{Si}/\text{Si}_{1-x}\text{Ge}_x$ alloy system. This is the first time the inversion-channel technology has been applied to the $\text{Si}/\text{Si}_{1-x}\text{Ge}_x$ material system.

Following this introductory chapter, the theory of operation of the DOES and HFET in the $\text{Si}/\text{Si}_{1-x}\text{Ge}_x$ system is presented (Chapters 2 & 3 respectively). The fabrication procedure developed for these devices is presented in Chapter 4. In Chapters 5, 6, and 7 the experimental characteristics of the DOES and HFET, are found and compared to simulations based on the theory. A logic circuit application of these devices and their monolithic integration is demonstrated in Chapter 8. Finally, in Chapter 9, a summary of the major findings and a discussion on future research directions for this work concludes the thesis.

CHAPTER 2

OPERATIONAL THEORY OF THE DOES

This chapter reviews the theory of operation of the DOES and relates it to the salient electrical characteristics of the device. Much of the theory behind the Si/SiGe DOES presented here is an extension of the work of Simmons, Taylor, and Swoger [56-58]. Indeed, simulations of both the two- and three-terminal DOES which appear in this chapter use a computer algorithm written by Swoger with alterations applicable to the Si/SiGe-based heterostructure.

2.1 Current-Voltage Characteristics of the DOES

In previous manifestations of the DOES based in the GaAs/AlGaAs material system [18], if current is driven from the emitter to the collector and the voltage required to do this is recorded, then an 'S'-shaped current-voltage characteristic will be observed (Fig. 2.1). This characteristic exhibits electrical bistability; a high-impedance OFF-state and a low-impedance ON-state that are separated by a differential negative resistance region. Without any injection current from the third-terminal, a switching voltage, V_{SO} , and its associated current, I_{SO} , define the limit of the high-impedance state. The onset of the low-impedance state is characterized by a holding voltage, V_{HO} , and an associated current, I_{HO} . By injecting carriers via the third terminal, the switching voltage, V_S , is reduced below V_{SO} , I_S and I_H move to slightly lower values, and V_H remains

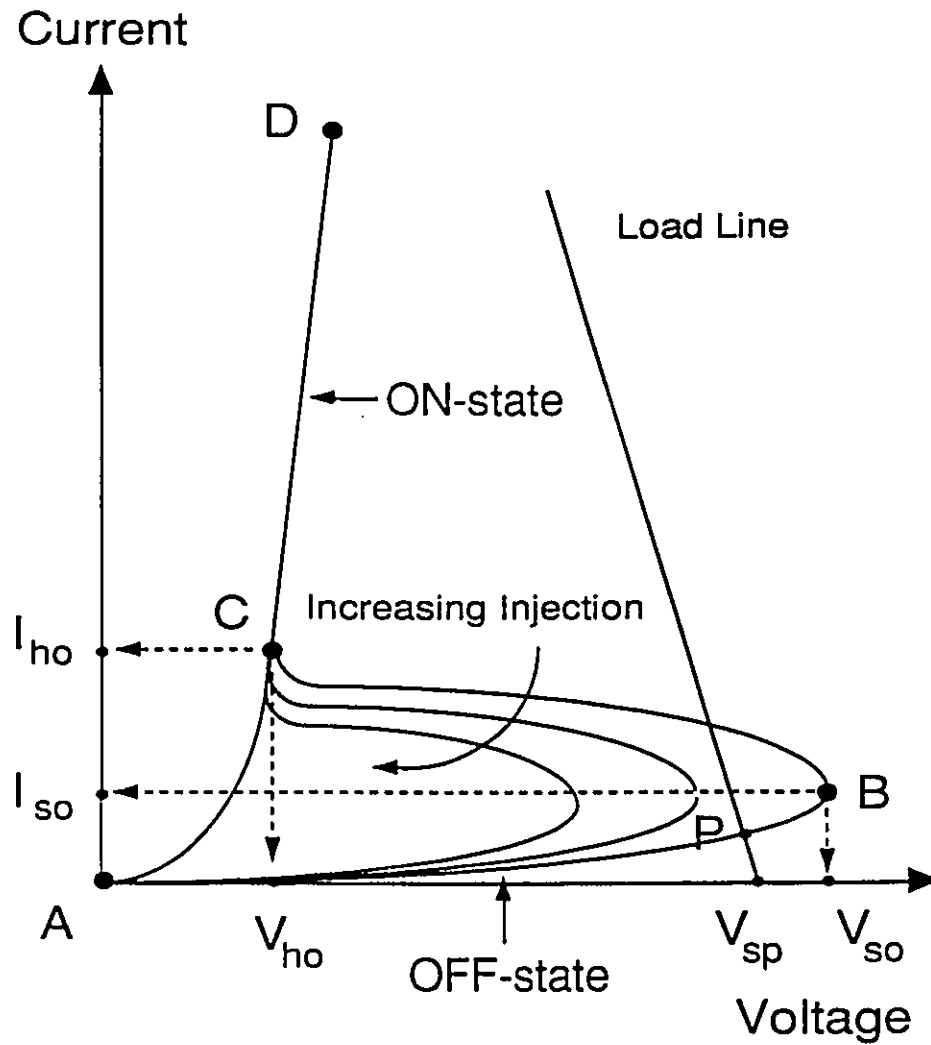


Figure 2.1: The hypothetical current-voltage (I-V) characteristic of the DOES with increasing third-terminal injection as a parametric variable. The switching voltage, V_{so} , switching current, I_{so} , holding voltage, V_{ho} , and holding current, I_{ho} , mark the boundaries of the impedance states of the device with no third-terminal injection. From point A to B, the device is in the OFF-state, from point B to C, in the regime of negative differential resistance, and from point C onwards to higher current, the device is in the ON-state.

essentially unchanged. Thus, with I_{inj} as a parametric variable, a family of I-V curves nesting within the original ($I_{inj} = 0$) I-V characteristic is generated as shown in Fig. 2.1. A simple switching circuit may be constructed using a load resistor in series with the device. For the $I_{inj}=0$ curve, assume that the operating point is P on the high impedance portion of the device characteristic. Here, essentially all the supply voltage, V_{sp} , is dropped across the device and only a small current flows in the external circuit. When a third-terminal injection current is applied it is seen that the load line can only intersect the low impedance portion of the new I-V curve. Thus, there is now only V_h across the device and $V_{sp}-V_h$ across the resistor, and therefore substantial current is now flowing in the circuit. One would expect that the device can be switched from the ON-state back to the OFF-state by extracting current, which results in quenching the feed-back current flowing in the device.

2.2 The Physical Structure of the Si/SiGe-Based DOES

The basic physical structure of the DOES comprises, in sequence, a heavily-doped p-type wide-bandgap semiconductor (WBGS), a n-type narrow bandgap active layer, a highly doped p-type charge sheet, and a n-type wide bandgap barrier layer. The first p-type layer is usually the substrate. The heterostructure designed to implement the Si/SiGe DOES and HFET is seen in Fig. 2.2. It must be emphasized that this was the target heterostructure from which the actual grown layer may deviate substantially.

The Si/SiGe DOES heterostructure resembles the npnp structure of the Si-based optical thyristor [59]. However, there are two distinct and critical features of this design. The first is a 50Å thick layer of Si doped p-type at $5 \times 10^{18} \text{ cm}^{-3}$

with boron. This layer forms the charge sheet and creates a triangular energy barrier. This charge sheet is depleted of free charge and, as we shall see later, minimizes the problems of charge storage. The magnitude of the doping in the charge sheet has been shown [56] to have a strong effect on the electrical characteristics of a DOES. Astride the charge sheet, are the barrier and active layers. These layers are doped n-type at $2 \times 10^{17} \text{ As cm}^{-3}$ and $1 \times 10^{17} \text{ As cm}^{-3}$ respectively. The barrier layers (sometimes called the emitter) includes a highly doped cap layer to facilitate an ohmic contact.

The second feature is a layer of $\text{Si}_{.75}\text{Ge}_{.25}$, with no intentional doping incorporated, placed between the charge sheet and the active layer. This layer is grown lattice matched to the underlying (100) Si active layer and as such is under compressive strain. The $\text{Si}_{.75}\text{Ge}_{.25}$ layer forms a valence band hetero-offset at nearly the same point as the charge sheet. It is at this hetero-offset that free holes induced by the charge sheet collect. In actuality, the charge sheet and the $\text{Si}_{.75}\text{Ge}_{.25}$ layer are separated by a 50 \AA thick spacer layer of undoped Si which is required to spatially separate the holes in the inversion layer from the acceptors in the charge sheet and thereby reduce ionized impurity scattering [12].

The entire heterostructure was grown on a Si(100) substrate doped p-type at $2 \times 10^{18} \text{ cm}^{-3}$ with boron. The substrate was used in this design as a contact and is called the collector.

The magnitude of the valence band discontinuity at the Si-SiGe interface is determined by the Ge content in the alloy. A large offset in the valence band is conducive to hole accumulation at the Si/SiGe interface and enhances the feedback gain in the DOES and reduces gate leakage in the HFET. We shall see that the gain of the hetero-structure has an exponential dependence on the valence-band discontinuity or, equivalently,

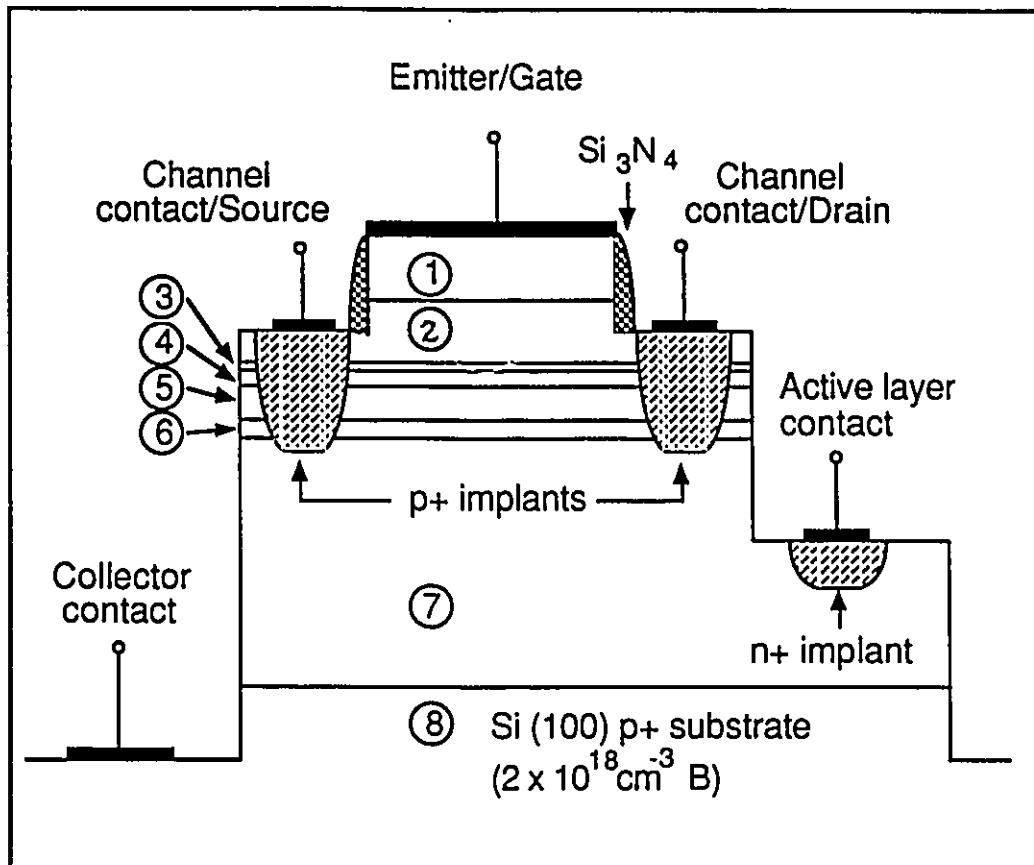


Figure 2.2: The layer structure and cross-sectional view of the self-aligned three-terminal DOES/HFET with terminals contacting the inversion charge on both sides of the mesa with a p^+ implant. Another terminal is seen to make contact to the active layer with an n^+ contact. The layer sequence : 1) 100nm of n-type Si ($2 \times 10^{18} \text{ cm}^{-3} \text{ As}$); 2) 200nm of n-type Si ($2 \times 10^{17} \text{ cm}^{-3} \text{ As}$); 3) the 5nm charge sheet of p-type Si ($5 \times 10^{18} \text{ cm}^{-3} \text{ B}$); 4) 20nm of undoped Si; 5) 60nm of undoped Si_{0.75}Ge_{0.25}; 6) 20nm of undoped Si; 7) the 1000nm active layer of n-type Si ($1 \times 10^{17} \text{ cm}^{-3} \text{ As}$); and finally, 8) the substrate.

on the Ge content of the SiGe well. Also, creating or reducing hole accumulation at the Si-SiGe interface by third-terminal injection/extraction is the primary method of controlling the switching voltage of the device. In the DOES, the

third-terminal refers to the terminal which makes contact to the charge which is trapped at the hetero-interface or a terminal to the active region. This is illustrated in Fig. 2.2.

The switching voltage can also be controlled by optical injection. Light absorbed in the depletion regions astride the charge sheet will enhance the hole accumulation at the hetero-interface. Electrons and holes created by absorption are spatially separated by the electric field associated with the depletion regions. Holes are swept to the n-n hetero-interface whereas electrons are swept to the neutral part of the barrier and active layers. The operational parameters of the DOES will depend on the incident optical power and the wavelength-dependent absorption depth of the light. This has been reported for DOES manifested in the GaAs/AlGaAs system [18].

2.3 Energy Band Diagrams

The energy band diagram for the structure shown in Fig. 2.2 under equilibrium conditions is shown in Fig. 2.3. A principle feature of this diagram is the depleted n-layers on either side of the Si/Si-Ge well, which are induced by the depleted p^+ region. Thus, with the charge sheet acceptors fully occupied by electrons, the sheet assumes a negative polarity and the depleted barrier and active layers assume a positive polarity. It will be shown that the occupancy of the charge sheet acceptors depends on the position of the Fermi level at the n-n hetero-junction.

The relatively small thickness of the charge sheet compared with that of the barrier layer allows us to illustrate the sheet as part of the surface layer of the barrier. The junctions formed by the barrier layer, the charge sheet, and the active

layer are collectively called the n-n heterojunction. The junction formed by the wide bandgap active layer and the substrate is called the p-n junction.

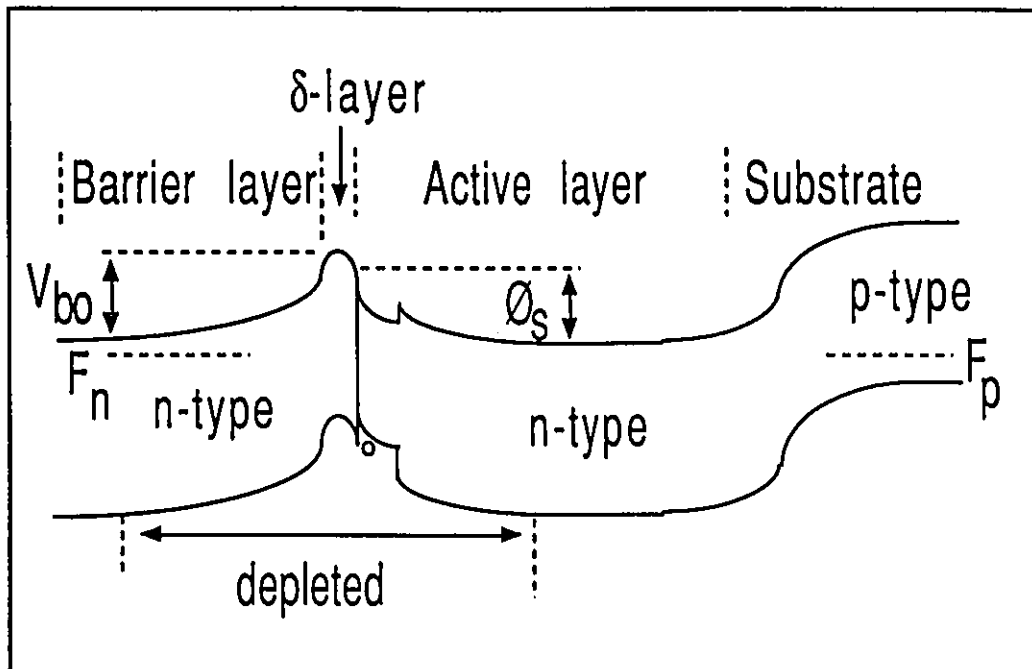


Figure 2.3: The schematic energy band diagram of the heterostructure under equilibrium conditions. F_n and F_p are the Fermi levels in the neutral part of the barrier layer and substrate respectively. ϕ_s is the total surface potential in the active layer.

Under forward-bias conditions (emitter is biased negatively with respect to the substrate), the Fermi-level in the emitter is raised and the barrier-sheet junction becomes forward-biased while the sheet-active layer junction becomes reverse-biased. The active-collector junction also becomes forward-biased to some extent. A brief explanation of the I-V characteristics of the device can be made with reference to the energy diagrams in Fig. 2.3 & 2.4. In the OFF-state, Fig. 2.4(a), the n-n heterojunction and the active region-substrate junction are

both slightly forward-biased, but the left side of the active layer is reversed-biased and, as such, its surface potential ϕ_s absorbs most of the applied voltage. Electrons flowing over the barrier layer into the active layer also pass over the p-n junction, thereby forward-biasing it. Consequently, this causes the injection of holes into the active region, which then pass through the barrier layer. This process incrementally forward-biases the barrier layer, thus augmenting the flow of electrons through the barrier layer. This positive feed-back action continues with increasing current and voltage until the small-signal gain of the heterojunction and the p-n junction reaches unity. This causes the depletion region and, hence, ϕ_s to collapse (Fig. 2.4(b)) with further increase in the current, a process which generates a regime of negative differential resistance (Fig. 2.1). The device exists in this condition until the surface potential reduces to a few millivolts, when the device then enters the low-impedance mode.

It is constructive in this discussion to briefly identify some of the figures of merit for a device such as the DOES. As a switch, one would presumably like to have the two operational states as extreme as possible; the OFF-state having extremely large impedance (high V_s and low I_s); and the ON-state having very low impedance (diode-like). The time to switch between states is also an important figure of merit for the applications envisioned for the DOES. Sensitivity to third-terminal injection and optical injection is a critical aspect of this device. The change in V_s versus optical intensity or third-terminal injection is perhaps the most simple way to describe the sensitivity.

The mathematical discussion to follow will attempt to focus on the aforementioned figures of merit. In Fig. 2.5, the energy band diagram of the Si/SiGe heterostructure described above illustrates the physical parameters, current components, and the various potentials to be referenced in the equations.

A parameter followed by the subscript naught (o) indicates the equilibrium value. For example, the barrier potential at equilibrium is denoted by V_{b0} , as opposed to simply V_b , the non-equilibrium value.

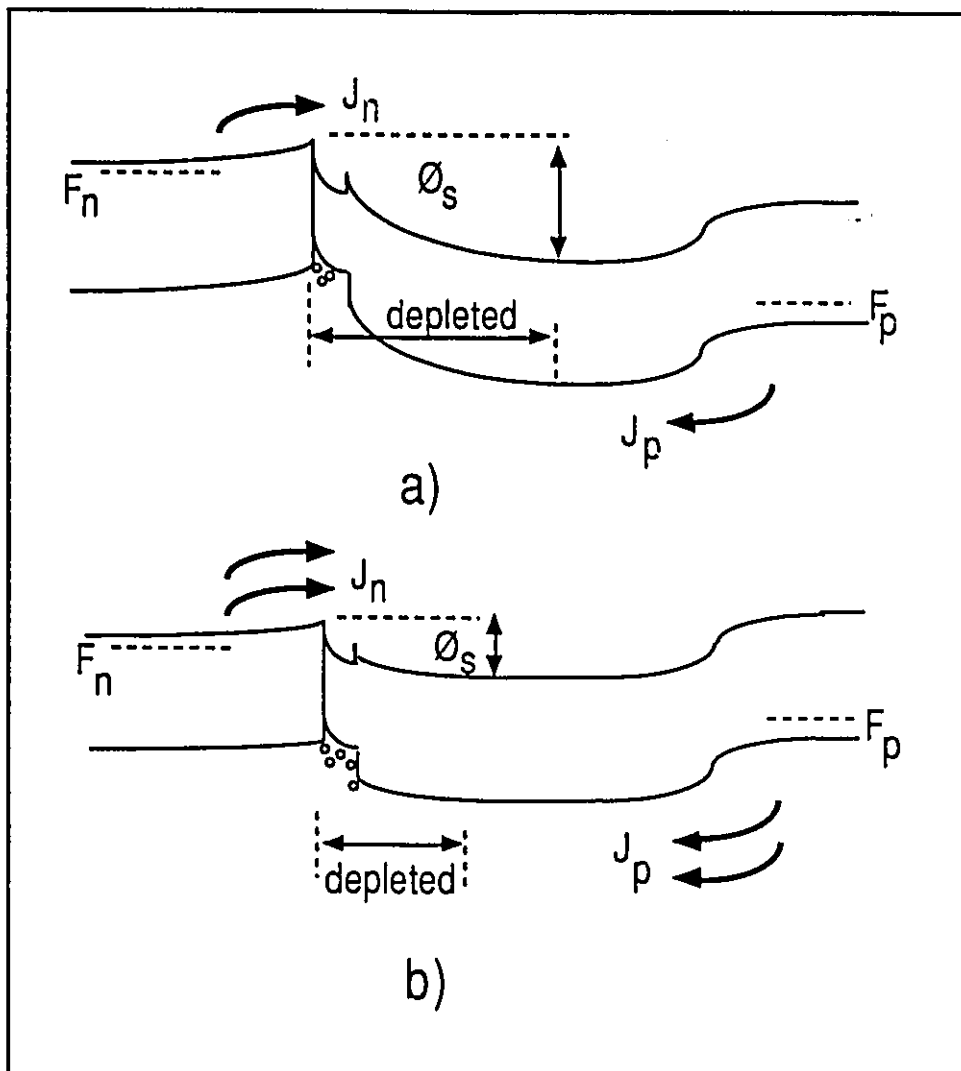


Figure 2.4: The schematic energy band diagram of the heterostructure under forward-bias conditions in the (a) OFF-state and in the (b) ON-state. J_n and J_p are the electron current over the barrier and the hole current from the substrate respectively.

2.4 Charge equations

Charge neutrality in the heterostructure dictates that,

$$Q_o + Q_b + Q_{Si} + Q_{SiGe} + q p_o = 0 \quad (2.1)$$

where the Si barrier depletion charge is Q_b , the charge in the p^+ doped Si charge sheet is Q_o , the hole charge in the channel is $q p_o$, and the charge of the depleted n-type dopants in the Si active region is Q_{Si} and Q_{SiGe} for the SiGe well. All of the above are in units of charge density per unit area.

In practice, in this heterostructure, the SiGe well was not doped to any degree intentionally. Any doping in this well arises from the residual effects within the MBE growth facility and therefore is doped orders of magnitude below the Si active layer.

In equation 2.1, Q_o , the contribution from the charge sheet, is given by:

$$Q_o = \frac{-q N_o}{1 + \exp\left[\frac{(E_a + \Delta E_{Fpj} - \Delta E_v)}{V_t}\right]}, \quad (2.2)$$

where E_a is the activation energy of the acceptors and N_o is the acceptor areal density of the charge sheet given by the product of the doping in the delta layer multiplied by the thickness. Clearly, from equation 2.2, if $(\Delta E_{Fpj} - \Delta E_v)$ approaches E_a then Q_o will begin to fall. This must be compensated by a decrease in Q_b , Q_{Si} , Q_{SiGe} , and $q p_o$. This will be shown to have severe repercussions vis a vis the operation of the Si/SiGe-based HFET.

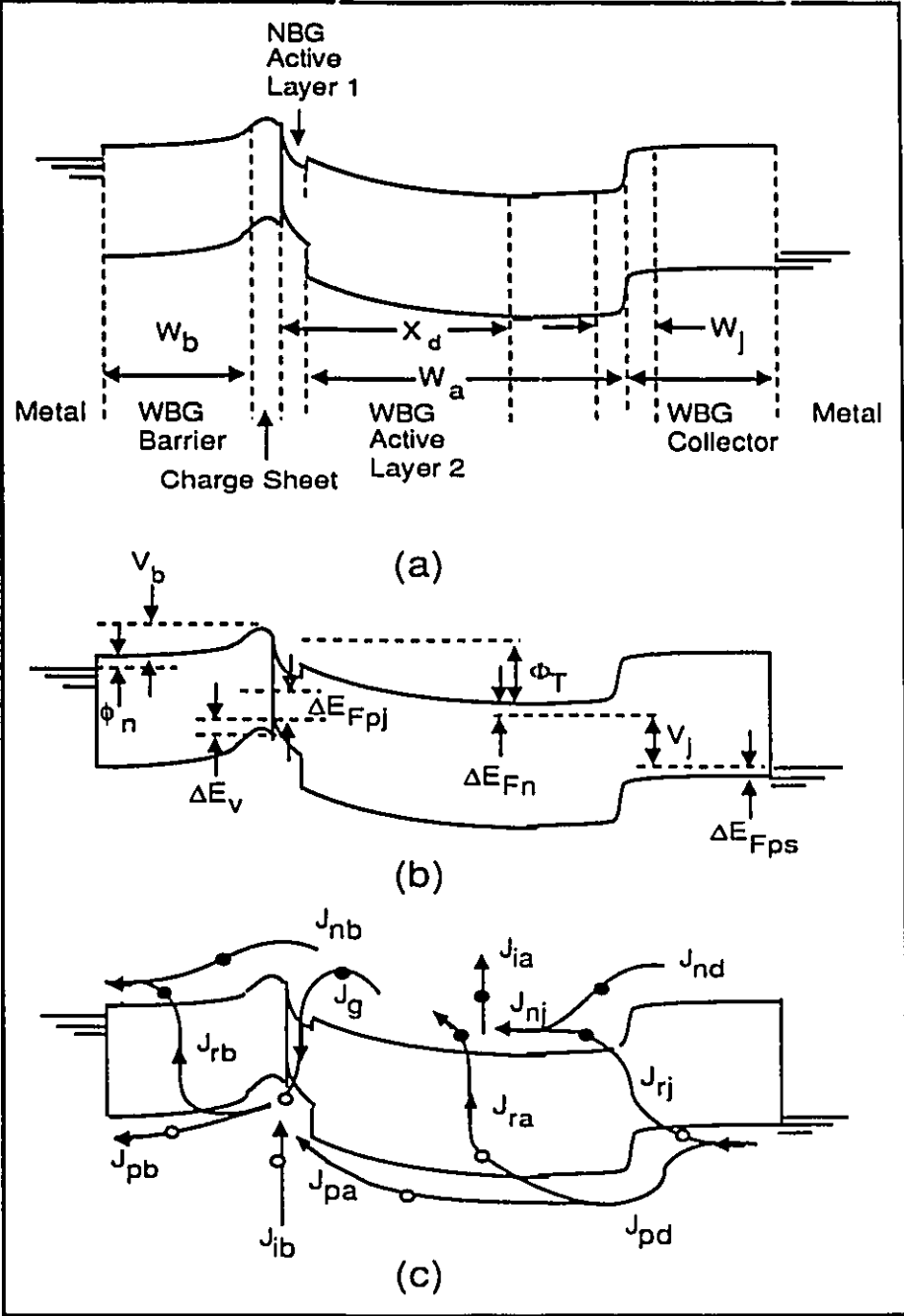


Figure 2.5: The schematic energy band diagram of the heterostructure with (a) layers and thickness identified, (b) various potentials shown, and (c) current components labeled.

The depletion approximation is used to determine the depleted charge from the barrier and active layer. For the barrier:

$$Q_b = \sqrt{2 q \epsilon_b N_{b0} V_b} , \quad (2.3)$$

where V_b is the barrier potential, and N_b is the donor concentration in the barrier. Similarly, in the active region,

$$Q_{SiGe} = q N_{SiGe} W_{SiGe} , \quad (2.4)$$

$$Q_{Si} = \sqrt{2 q \epsilon_{Si} N_{Si} \phi_{Si}} , \quad (2.5)$$

where N_{SiGe} and N_{Si} is the doping concentration in the SiGe and Si active region respectively, and ϕ_{SiGe} and ϕ_{Si} are the surface potential of the SiGe and Si depletion regions, respectively.

The next step is to solve for p_0 in the channel. Here the analysis is complicated by a number of factors. Firstly, under bias conditions, the SiGe-well is a triangular-like quantum well which contains quantized energy levels. The electric field in the active layers determines the width of the well. In such energy levels, the density of states is altered to become a step-like density where the first energy level lies above the valence band edge [60]. Secondly, the free charge in the channel is dependent upon ΔE_{Fpj} in a manner which requires a self-consistent solution. Finally, the conduction channel lies in the strained SiGe well where splitting of the valence bands is predicted [36]. This will almost certainly affect mobility and hole mass in the channel. In the following analysis the effect of strain and interband mixing is neglected.

The channel is approximated by a triangular quantum well, as is commonly done for High Electron Mobility Transistors (HEMTs). Using this model, which is graphically illustrated in Fig. 2.6, the first two energy levels in the well are given [61] by:

$$E_1 = \beta_1 \left[\frac{q\phi_0 + \sqrt{2q \epsilon_{\text{SiGe}} N_{\text{SiGe}} \phi_{\text{SiGe}}}}{\epsilon_{\text{SiGe}}} \right]^2, \quad (2.6)$$

and

$$E_2 = \left(\frac{7}{3}\right)^{2/3} E_1, \quad (2.7)$$

where

$$\beta_1 = \left(\frac{\hbar^2}{8q m_p}\right)^{1/3} \left(\frac{q}{8}\right)^{2/3}$$

If we can neglect the hole filling of the second energy level then we need only to integrate the density of states multiplied by the Fermi-filling function over E_1 to E_2 ; that is, the Fermi level in the channel always remains above E_2 . Then

$$p_0 = \int_{E_2}^{E_1} g(E) f(E) dE$$

where

$$g(E) = \frac{4\pi q m_p}{h^2}$$

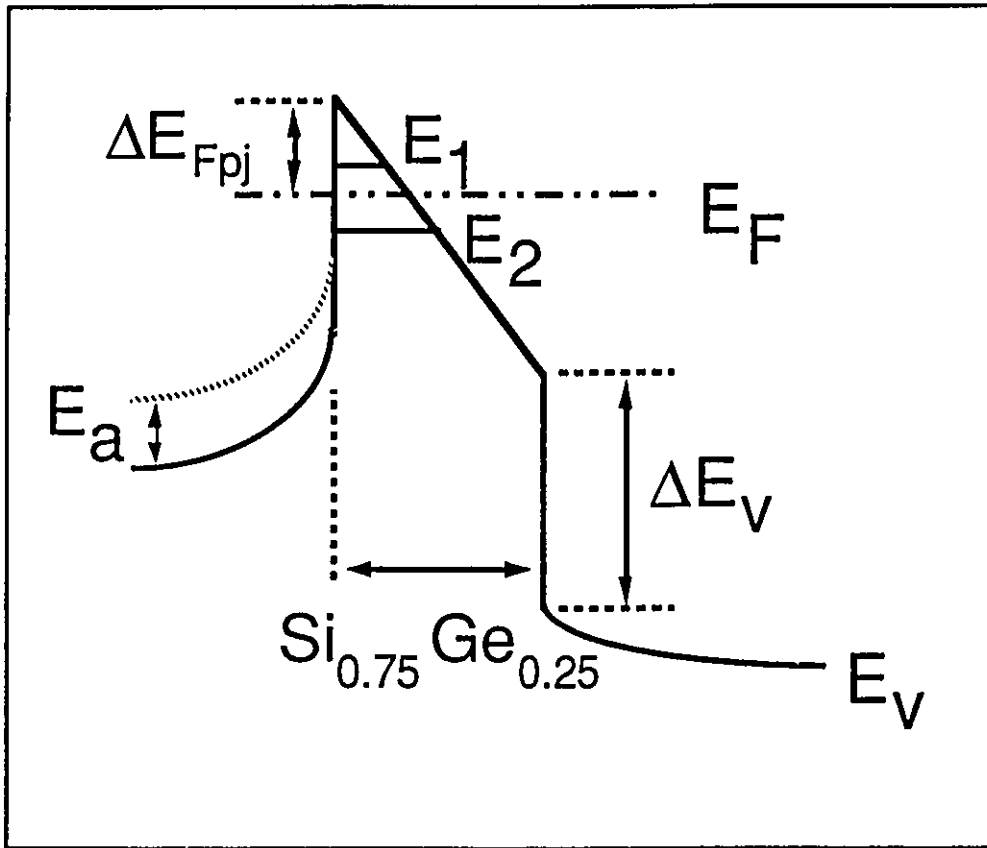


Figure 2.6: A schematic representation of the formation of hole energy levels in the valence band at the n-n heterojunction. Also illustrated is the Fermi-level in the channel, E_F , and the activation energy, E_a , of the dopant in the charge sheet. ΔE_{Fpj} is the difference between E_F and the valence band edge, E_v , at the hetero-interface. The quantized energy levels arising due to carrier confinement are labeled E_1 and E_2 .

is the density of states, and

$$f(E) = \frac{1}{1 + \exp\left(\frac{E - \Delta E_{Fpj}}{V_t}\right)}$$

is the Fermi-filling function. The Fermi level position is found by combining the above equations to give:

$$\Delta E_{Fpj} = - V_t \ln \left[\frac{\exp\left(\frac{-E_1}{V_t}\right) - \exp\left(\frac{-E_2}{V_t}\right) e^A}{e^A - 1} \right] \quad (2.8)$$

where

$$A = \frac{p_0 h^2}{4 p q m_p V_t}$$

The value of p_0 used here is found by re-arranging eqn. (2.1):

$$p_0 = \frac{Q_0 - Q_b - Q_{SiGe} - Q_{Si}}{q} \quad (2.9)$$

Swoger [57] has developed a computer-based algorithm which solves equations (2.8) and (2.9) in a self-consistent manner. Thus, in theory, given an arbitrary heterostructure design, the above equations are used to determine p_0 and ΔE_{Fpj} .

2.5 Current Equations

By examining the current components in Fig. 2.5(c) and assuming steady state conditions, two of continuity relations can be discerned. First, the electron flow over the barrier, J_{nb} , plus the generation current in the active layer, J_g , must balance the electron flow into the substrate, J_{nd} , plus the recombination currents

in the neutral part of the active layer, J_{ra} , and the recombination current at the p-n junction, J_{rj} :

$$J_{nb} + J_g = J_{rj} + J_{nd} + J_{ra} \quad (2.10)$$

A summation of currents at the hetero-interface indicates that, hole flow into the barrier, J_{pb} , plus the rate at which holes recombine in barrier, J_{rb} , must balance holes which flow to the hetero-interface from the active layer, J_{pa} , plus the generation current in the active layer, J_g , plus any hole injection via the third terminal, J_{ib} :

$$J_{pb} + J_{rb} = J_{pa} + J_g + J_{ib}. \quad (2.11)$$

Analytical expressions for the various current components can be found in appendix A . These expressions differ somewhat from the expressions used by Swoger [56] in that the SiGe-well requires segmentation of the active region.

The total applied bias voltage, V , between the emitter and collector can be found by summing the various potentials in Fig. 2.5(b):

$$V = V_j + \phi_T - \phi_{T_0} + V_{b_0} - V_b, \quad (2.12)$$

where

$$\phi_{T_0} = \phi_{SiGe_0} + \phi_{Si_0} + \Delta E_c$$

$$\phi_T = \phi_{SiGe} + \phi_{Si} + \Delta E_c$$

2.6 Simulations and Predictions

Given equations 2.1 to 2.12, it is possible to predict the salient operating characteristics of both the two- and three-terminal DOES. For example, the areal charge sheet doping density can be varied to investigate the effect on switching voltage. These simulations will be compared to the experimental data in later chapters of this thesis. Other parameters of interest are the injected current both at the barrier, J_{ib} , and into the active layer, J_{ia} . In both cases, injecting current will allow the DOES to satisfy the criterion for switch back at a lower voltage. It is possible to determine the sensitivity of the DOES to third-terminal injection. However, such a determination, obtained using a computer-based model, can be inaccurate when the physical design and fabrication process of the device has not been considered. Rather than attempt absolute measures, it is more realistic and, perhaps, more informative to compare device sensitivity to electrical injection into the inversion layer and into the active layer.

2.6.1 Effect of Charge Sheet Doping Density

Figure 2.7 illustrates the calculated logarithmic of current density versus voltage ($\log(J)$ -V) characteristics of the DOES with structure identical to that of Fig. 2.2 with the exception that the charge sheet doping density, N_0 , is used as a parameter. Varying the charge sheet doping density (either by varying the width of the charge sheet or by varying the doping density itself) was calculated to have the greatest effect on the operational characteristics of the DOES.

With increasing charge sheet doping density, the I-V characteristic is seen to change from a 'diode'-like curve at $N_0=2.2 \times 10^{12} \text{ cm}^{-2}$ to a 'S'-like curve at $N_0=4.4 \times 10^{12} \text{ cm}^{-2}$ with switching voltage, $V_{so} \approx 6.2 \text{ V}$.

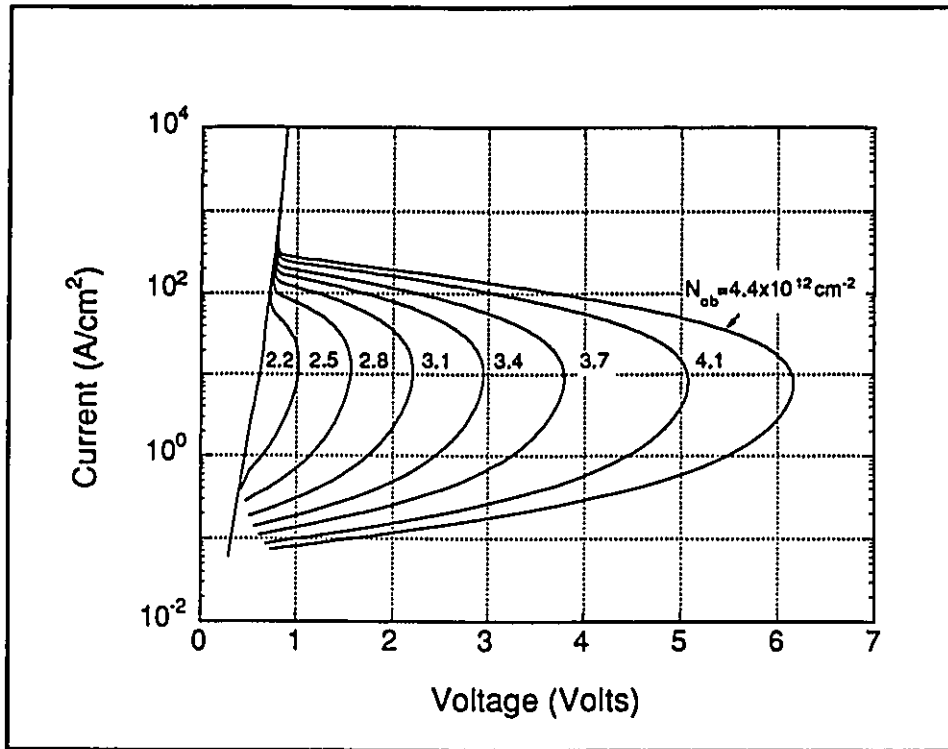


Figure 2.7: The calculated logarithm of current density versus applied voltage ($\log(J)$ - V) characteristics of the Si/SiGe-based DOES with charge sheet doping density, N_{ob} , as a parameter.

Also, the current before switching decreases markedly with higher doping in the sheet whereas the holding current is seen to increase.

Figure 2.8 represents a compilation of switching voltages with varying N_0 for set doping in the barrier and active layers. A family of curves can be generated if the doping in the barrier or active layers is varied. It was also found in these simulations that the switching current is relatively insensitive to N_0 . This implies that the criterion of switch back in the DOES - unity gain in the feedback loop, is primarily determined by the current and not by the voltage. In retrospect, this is a fairly obvious point exemplified the fact that the DOES is a current drive

device. For a device of dimension $50\mu\text{m} \times 50\mu\text{m}$ square, we can predict that the switching current is should be approximately 0.25mA .

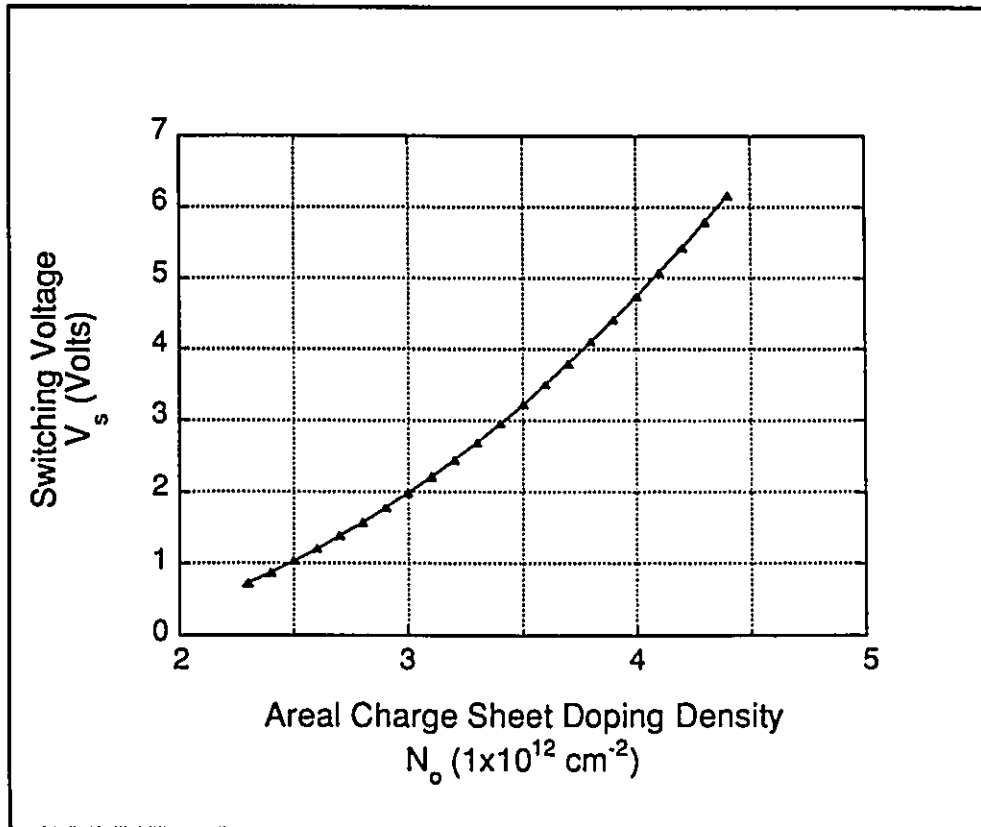


Figure 2.8: Predicted switching voltages, V_{s0} , as a function of areal charge sheet doping density, N_{ob} .

2.6.2 Effect of Barrier Layer Doping

The doping on either side of the charge sheet is also important in determining the I-V characteristics of the DOES. Figure 2.9 plots the equilibrium barrier surface potential, V_{b0} , versus the magnitude of the doping in the barrier layer, N_{b0} .

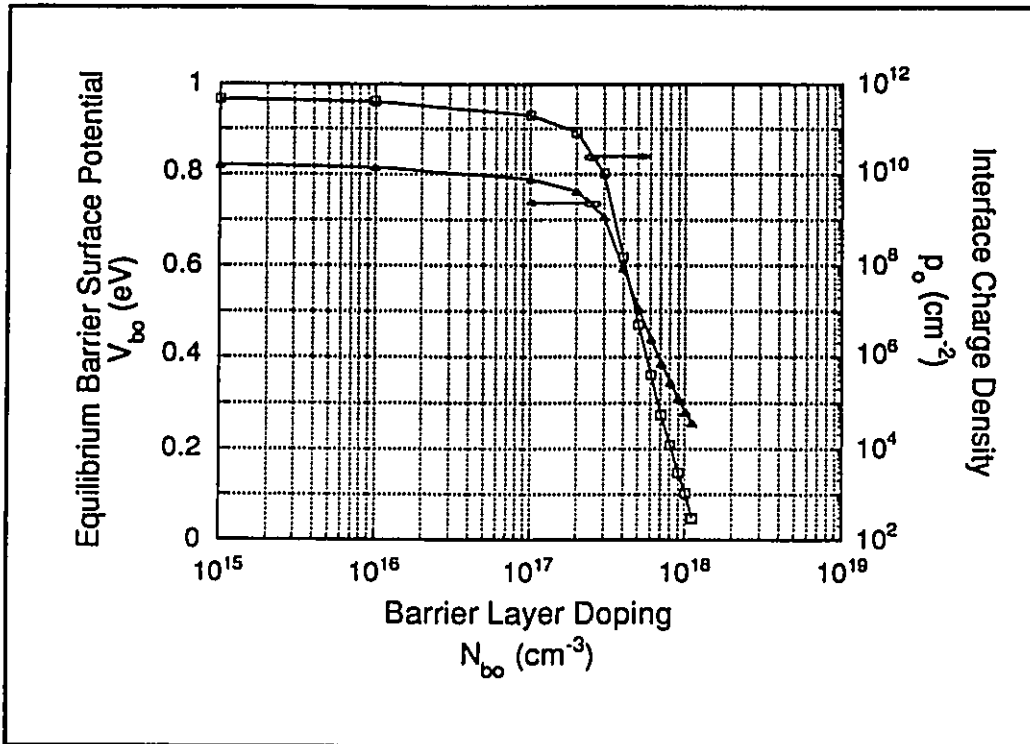


Figure 2.9: The calculated equilibrium barrier surface potential, V_{bo} (open squares), and the interface charge density, p_o (dark triangles), versus the doping density in the barrier layer, N_{bo} .

With increasing N_{bo} , V_{bo} is initially insensitive from $N_{bo}=1 \times 10^{15} \text{ cm}^{-3}$ to $1 \times 10^{17} \text{ cm}^{-3}$. However, over the range of N_{bo} from $1 \times 10^{17} \text{ cm}^{-3}$ to $1 \times 10^{18} \text{ cm}^{-3}$, V_{bo} falls quickly. The barrier surface potential measures the height of the triangular barrier for electron flow into the active region. Large V_{bo} values impedes electron flow into the active layer and necessitates high switching voltages.

Also plotted in Fig. 2.9 along with V_{bo} is the equilibrium interface charge density, p_o , which mirrors the dependence of V_{bo} but changes values over nine orders of magnitude.

Figures 2.7-2.9 show graphically how sensitive the I-V characteristics and the parameters of energy band diagram are to the design of the heterostructure. Implicitly, this allows a device designer freedom to optimize a heterostructure for particular operational characteristics and, in general, manipulate the design parameter space. However, this sensitivity also necessitates very rigid control over growth and doping.

2.6.3 Effect of Injection Current

The calculated effect of J_{ib} is illustrated in Fig. 2.10. The simulated I-V characteristics of the DOES with structure identical to that of Fig. 2.2 (except $N_{ob}=3.7 \times 10^{12} \text{ cm}^{-2}$) shows that with increasing J_{ib} the curves partially nest toward lower V_s and higher I_s . Also, the current before switching is seen to increase as the energy barrier to electron flow is progressively reduced by the hole accumulation at the n-n heterojunction.

A summary of this effect is seen in Fig. 2.11 where V_s and I_s are plotted against J_{ib} . This summary will prove useful in Chapter 6 to compare experimental results obtained with the three-terminal DOES. With increasing J_{ib} a monotonic reduction of V_s is observed. When extended to high channel injection values V_s is calculated to saturate at the holding voltage of the device. The switching current also increases with increasing J_{ib} .

In Fig. 2.12, the switching voltage versus injection current is plotted for third-terminal injection directly into the inversion layer, J_{ib} , and into the active layer, J_{ia} . Injection into the inversion layer is seen to lower device switching voltage more effectively than into the active layer. This is explained by examining the path that current injected into the active layer is required to take in order

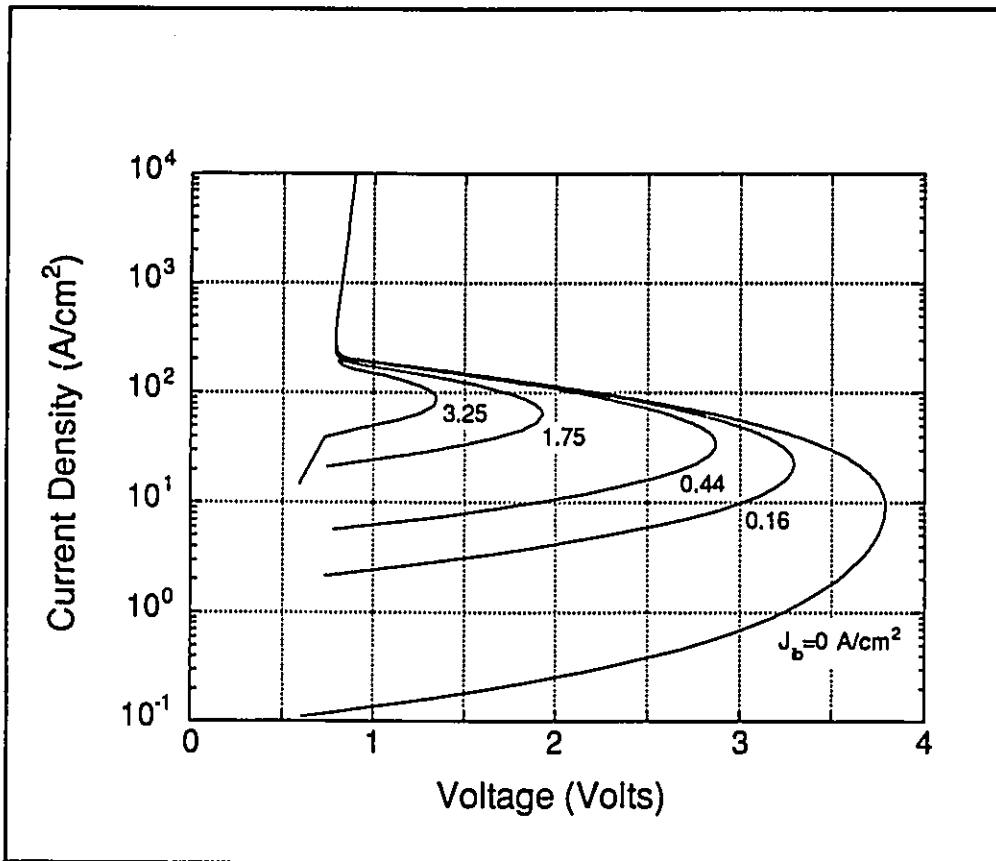


Figure 2.10: The calculated logarithmic of current density versus voltage ($\log(J)$ - V) characteristic with current injected at the n-n heterojunction, J_{ib} , as a parameter.

to effect the inversion channel hole population (Fig. 2.5(c)). Electrons injected in the active layer are first required to diffuse across the p-n junction formed by the active layer and the substrate. This, in turn, causes hole injection from the substrate into the active layer. Only a fraction of these will add to the hole population at the hetero-interface and thereby affect the barrier voltage.

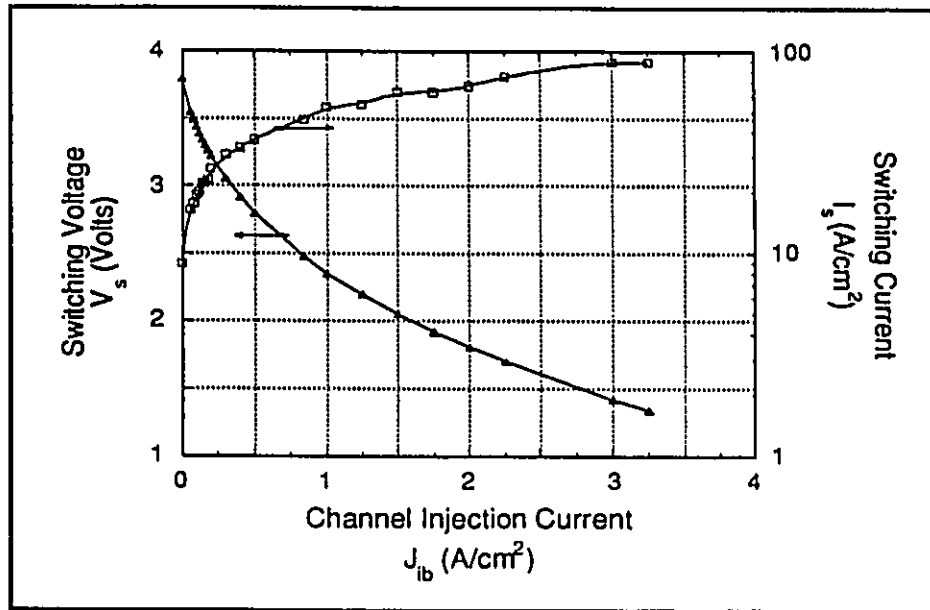


Figure 2.11: Calculated switching voltages and currents as a function of current injected directly into the channel via the third-terminal.

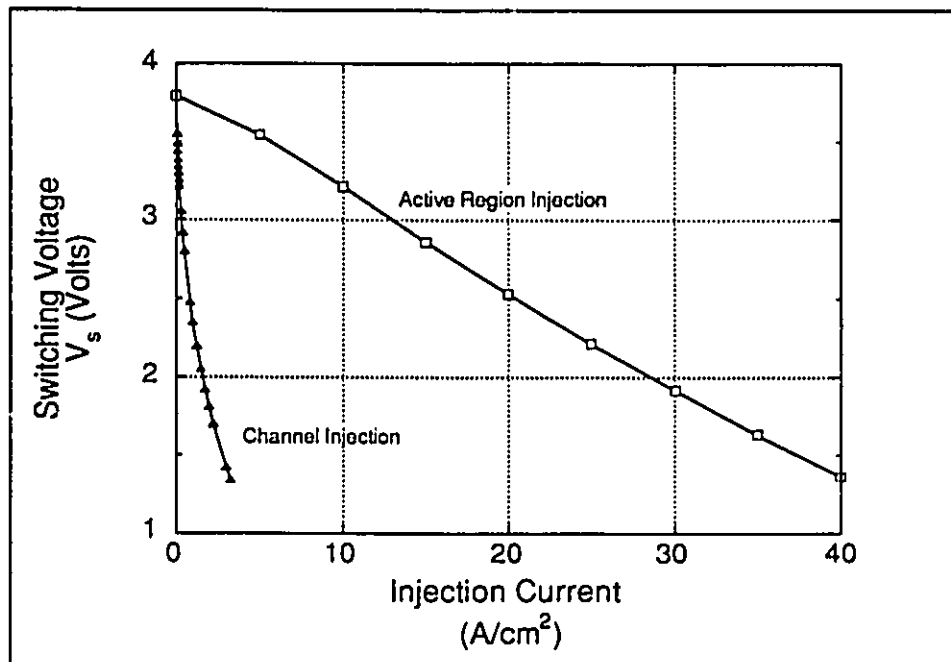


Figure 2.12: The predicted switching voltages as a function of current injected into the active layer and directly into the inversion channel.

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CHAPTER 3

OPERATIONAL THEORY OF THE HFET

This chapter reviews the theory of operation of the HFET and relates that theory to the salient electrical characteristics of the device. The DOES and the HFET are distinct devices but much of the theory of the DOES concerning the inversion charge will be reiterated for the HFET.

3.1 Si/SiGe HFET: An Operational Discussion

In the preceding section, it was stated that within the strained SiGe-well at the n-n hetero-interface, an accumulation of holes is found to be sensitive to the bias on the emitter terminal. The basis of the SiGe HFET is to use this hole accumulation as a conductive channel between source and drain contacts. To visualize this, a three-dimensional energy band diagram is required (Fig. 3.1).

In the SiGe HFET, all voltage biases are referenced with respect to the source terminal which is at ground potential. The gate of the SiGe-HFET serves much the same purpose as the gate of a MOSFET. That is, to modulate the channel charge by changing the width of the depletion regions, and thereby affect the source to drain conduction properties. An idealized family of FET current-voltage (I-V) characteristics are seen in Fig. 3.2 where gate bias is used as a parametric variable. In Fig. 3.2, three regions of operation can be identified; i) the linear region where current increases monotonically with increasing source-

drain bias, ii) the saturation region where the output impedance approaches infinite values, and iii) the subthreshold region where regardless of source-drain bias very little current is extracted. However, because the Si/SiGe DOES heterostructure is inherently bipolar and capable of

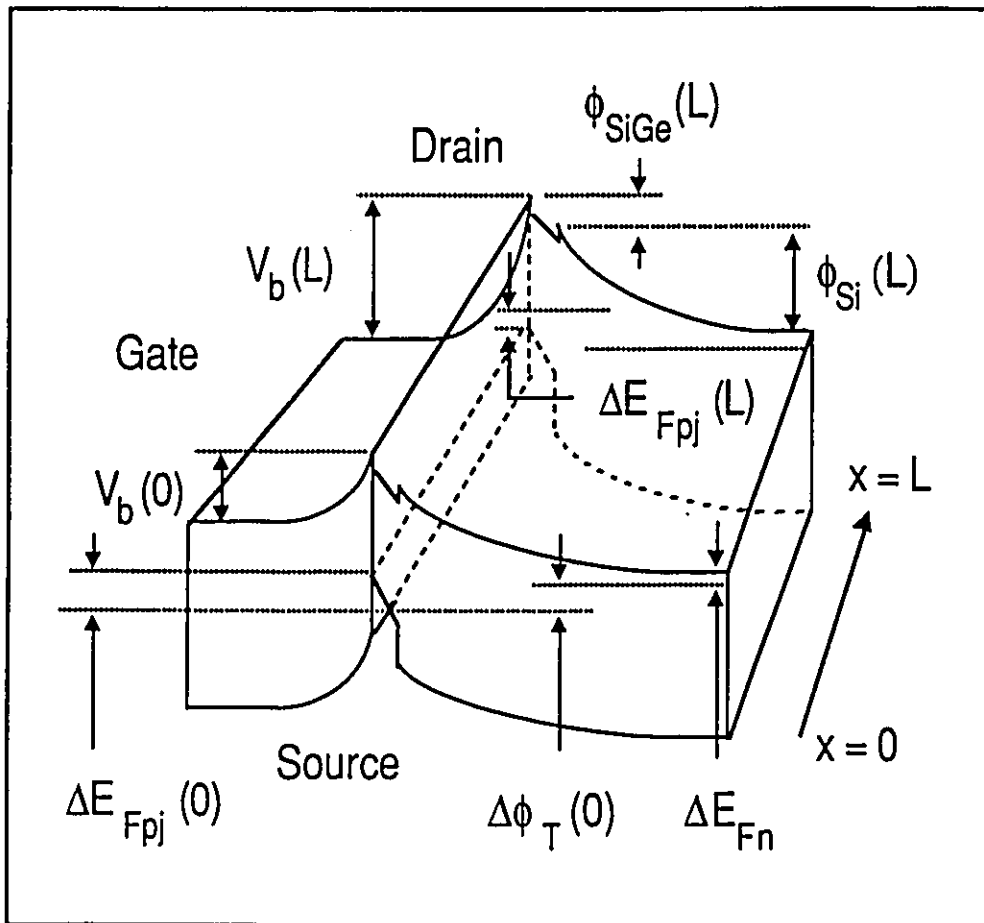


Figure 3.1: Schematic three-dimensional energy band diagram of the HFET with non-zero source and drain potential.

feedback, the dependence of the hole accumulation on the gate bias requires a more complex treatment than the MOSFET. In the ideal theory of the MOSFET,

the oxide forms a perfect insulator and gate leakage is not considered. This treatment is given by Leiby [62] and is qualitatively described in this section. In the HFET, gate leakage is a consequence of forward-biasing the n-n heterojunction and can have dramatic effect on the channel properties. In the discussion to follow, the idealized theory of HFET operation is first presented along with some of the important figures of merit for this class of device. Following this, issues related to gate leakage and feedback are examined.

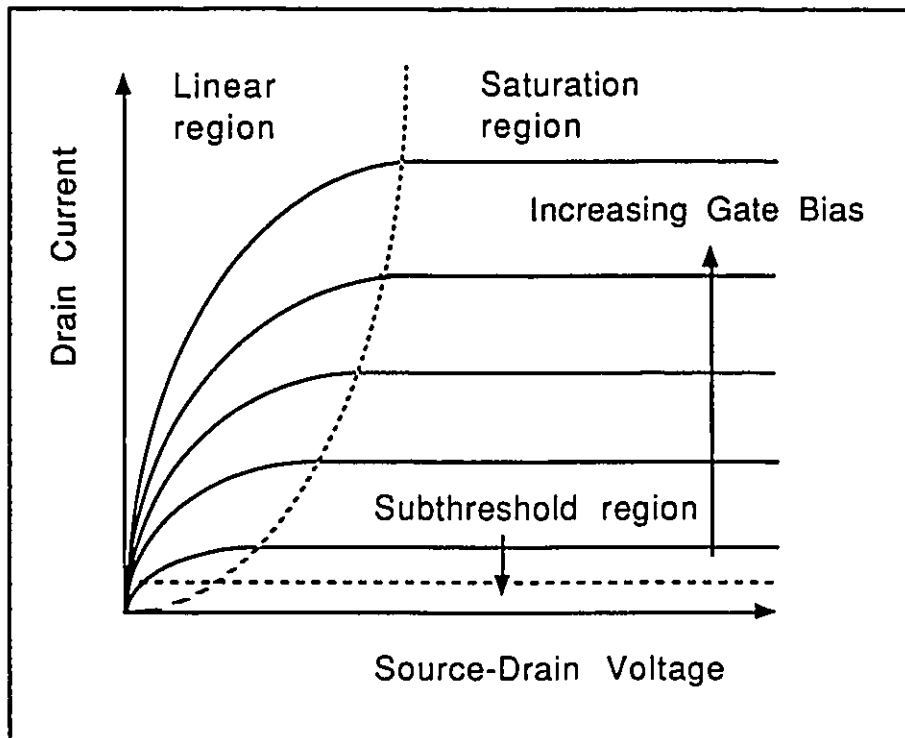


Figure 3.2: Idealized source-drain current-voltage characteristics for a FET with gate bias as a parametric variable. The dashed line delineates between the various region of operation.

3.2 Conduction Equations

Assuming that the barrier layer acts as a perfect insulator allows an analysis of the HFET which much resembles the description of a MOSFET. However, even with such a simplification, the channel charge requires a self-consistent analysis. In the HFET, the hole density in the channel increases when the gate to charge sheet diode is forward-biased. Biasing the gate negatively with respect to the source ($V_{gs} < 0$) causes a reduction of the barrier layer depletion region which from the charge neutrality requirements (eqn. 2.1), causes an increase in the hole population in the channel.

Assuming no gate leakage, the diode formed by the active region and the charge sheet becomes reverse-biased in response to a negative V_{gs} and the depletion layer in the active region expands. Hypothetically, this reduces the over-all increase in the hole population since some of the decrease in the barrier layer charge goes to increase the active layer charge. Conversely, a positive V_{gs} reduces the hole population in the channel since the barrier depletion region expands in response to the reverse-bias. Graphically, these bias conditions are illustrated in Fig. 3.3(a,b,c). When the Fermi level at the drain is raised with respect to the source (negative V_{ds}) the hole population along the channel will gradually decrease. At the drain end of the conduction channel the gate to drain potential is $V_{gs} - V_{ds}$.

The current-voltage characteristics of the HFET can be described using a gradual channel approximation outlined by Shur [63]. Briefly, the current from source to drain at any position x along the channel can be shown to be

$$I_{ds} = q\mu_p p_0(x) \frac{dV_c(x)}{dx} W, \quad (3.1)$$

where;

$$V_c(0) = 0 \ \& \ V_c(L) = V_{ds}$$

where μ_p is the low-field hole mobility in the channel, $p_0(x)$ is the position dependent hole density in the channel, W is the gate width of the HFET, and $dV_c(x)/dx$ is the electric field at position x . Equation 3.1 is only valid for those V_{ds} values at which an inverted hole population still exists (ie. $p_0(L) \geq 0$). In eqn. 3.1, I_{ds} would seem to change along the length of the channel as $dV_c(x)/dx$ increases from source to drain. In actuality, $p_0(x)$ decreases at a rate which balances the increasing electric field term to yield a constant I_{ds} value across the channel. However, as V_{ds} is progressively increased, I_{ds} will increase accordingly. When an inverted hole population no longer exists for a particular V_{ds} , then the channel is described as 'pinched-off'. For V_{ds} values beyond those where the channel is pinched-off, no increase in I_{ds} is expected on the first order. The channel current is said to be saturated at I_{dsat} and the output impedance of the device is infinitely large. In practice, other factors such as channel length modulation, velocity saturation, and avalanche breakdown near the drain will combine to yield the non-ideal non-saturating current-voltage characteristics [63].

An important figure of merit in the HFET is transconductance, g_m , given by:

$$g_m = \left. \frac{\partial I_{ds}}{\partial V_{gs}} \right|_{\text{constant } V_{ds}} \quad (3.2)$$

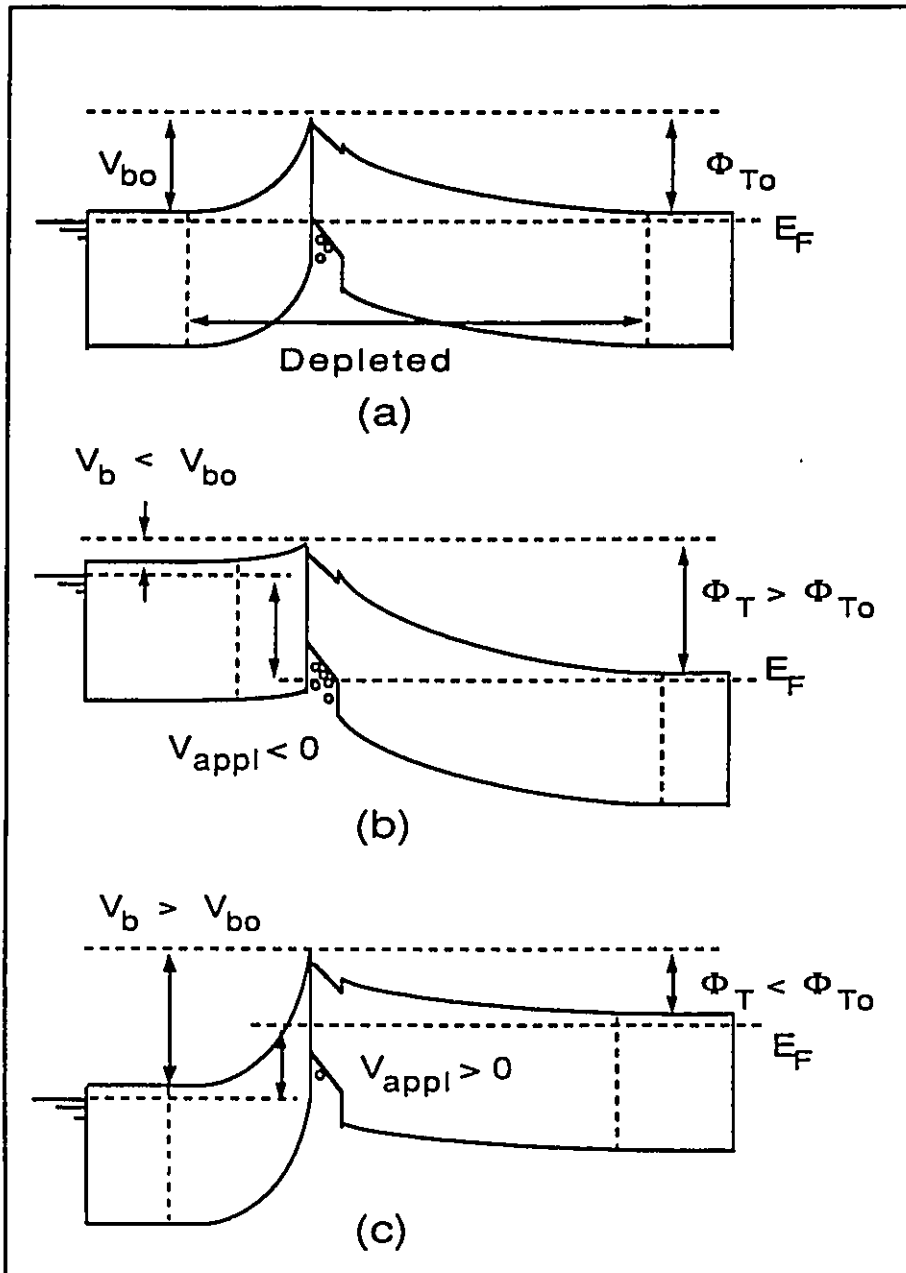


Figure 3.3: The energy band diagram of the HFET (at $V_{ds}=0V$) (a) under equilibrium conditions, (b) with a negative potential on the gate with respect to the source (forward-bias), and (c) with a positive potential on the gate (reverse-bias).

Using eqn. 3.1, g_m is given by:

$$g_m = \mu_p \left(\frac{W}{L} \right) c_i V_{dsat} \quad (3.3)$$

where c_i is the capacitance per unit area of the gate electrode. Using long channel devices where channel width, W , and the length, L , are approximately equal, the device transconductance and saturation voltage, V_{dsat} , may be used to calculate channel mobility. Alternatively, the differential drain conductance, g_{ds} , is given by

$$g_{ds} = \left. \frac{dI_{ds}}{dV_{ds}} \right|_{V_{gs}} = \mu_p \left(\frac{W}{L} \right) c_i (V_G - V_{Th}) \quad (3.4)$$

for $V_G - V_{Th} < V_{dsat}$

Using eqn. 3.4 and measuring the slope of the linear region of the FET I-V characteristic for a specific V_{gs} , the channel mobility can also be calculated. However, this calculation also requires knowledge of the threshold voltage, V_{Th} , and the capacitance per unit area of gate.

Another important figure of merit for transistors intended for use in logic applications is the subthreshold slope of the I_{ds} versus V_{gs} characteristic at constant V_{ds} . Subthreshold slope is typically expressed as the change in gate potential in millivolts required to change I_{ds} by one decade. This figure of merit gives an indication of how easily the transistor can be turned to a low conducting state. In the HFET, the subthreshold slope can be optimized by properly designing the heterostructure. The height of the triangular energy barrier, the

doping in the barrier and active layers, and gate leakage will all affect the subthreshold slope. Ultimately, it is the hole population at the hetero-interface and its sensitivity to gate bias which determines many of the figures of merit relevant to this transistor. For this reason, it is critical that all phenomena in these devices which can affect the interface hole population be understood.

3.3 Charge in the Conduction Channel

In this section, the population of free holes in the channel is examined. A one-dimensional analysis is performed with consideration to charge sheet dopant ionization and gate leakage. From the calculation of free hole density in the channel, the threshold voltage of the HFET is predicted for a variety of heterostructure parameters. In addition, the transconductance characteristic is calculated.

3.3.1 Effect of δ Layer Doping and Dopant Ionization

First considered is the ionized charge in the sheet and the interplay between ionization of the dopant and Fermi level at the hetero-interface. The three dimensional energy band diagram of the Si/SiGe HFET heterostructure (Fig. 3.1) describes the physical parameters, and the various potentials to be referenced in the equations 3.1-3.12 when dealing with the HFET. However, these quantities vary from the source to the drain when a potential is placed on the drain with respect to the source (non-zero V_{ds}).

The degree of doping in the charge sheet has a profound effect upon the hole population in the channel. This follows from the charge neutrality condition

(eqn. 2.1) and the dependence of Q_0 on the position of the Fermi level in the channel (eqn. 2.2). The depletion approximation is again used to determine the depletion charge in the barrier and active layers but now equations 2.3-2.5 become:

$$Q_b = \sqrt{2 q \epsilon_b N_b V_b(x)}, \quad 0 \leq x \leq L \quad (3.5)$$

$$Q_{SiGe} = q N_{SiGe} W_{SiGe}(x), \quad 0 \leq x \leq L \quad (3.6)$$

$$Q_{Si} = \sqrt{2 q \epsilon_{Si} N_{Si} \phi_{Si}(x)}, \quad 0 \leq x \leq L \quad (3.7)$$

where V_b , W_{SiGe} , and ϕ_{Si} have are a function of the position and L is the gate length. The total surface potential in the active layers at position x is given by:

$$\phi_T(x) = \phi_{SiGe}(x) + \phi_{Si}(x) - \Delta E_c, \quad (3.8)$$

From eqn. 2.2, if $(\Delta E_{Fp_j}(x) - \Delta E_v)$ approaches E_a the ionized dopant centers in the charge sheet will start to refill with holes and Q_0 will begin to fall. This must be compensated by a decrease in Q_b , Q_{Si} , Q_{SiGe} , and slows down the rate of growth of p_0 . This will affect the operation of the Si/SiGe-based HFET and must be considered when attempting to design the heterostructure for a specific threshold voltage. Also, it is primarily the magnitude of Q_0 which will determine whether or not the device is depletion or enhancement mode. Again, using the simple theory of the MOSFET, the threshold voltage is related to the interface Fermi level by [58]:

$$V_{Th} = V_{FB} + 2\phi_F + \frac{1}{C_h} \left[2q\epsilon_{SiGe} N_{SiGe} (2\phi_F) \right]^{1/2}, \quad (3.9)$$

and

$$\phi_F = E_{gSiGe} - \Delta E_{Fpj} - \Delta E_{Fn} , \quad (3.10)$$

where V_{FB} is the flatband voltage, ΔE_{Fn} is the difference in energy between the Fermi level in the neutral part of the Si active layer and the conduction band edge, E_{gSiGe} is the bandgap energy of the $Si_{1-x}Ge_x$ alloy, and C_b is the capacitance of the barrier depletion region. In eqn. 3.10, ϕ_F is normally defined in the theory of the MOSFET as the potential difference between the intrinsic Fermi level, E_i , and the Fermi level in the neutral part of the active region:

$$\phi_F = \frac{kT}{q} \ln\left(\frac{N_{Si}}{n_i}\right), \quad (3.11)$$

In the MOSFET, threshold is defined as that gate voltage at which the Fermi level at the interface is twice ϕ_F removed from E_i . That is, the inverted carrier density at the interface is a factor of e^2 larger than the carrier density in the neutral part of the Si active region. Using equation 3.9 to predict threshold values will yield inaccurate results. In the HFET, both C_b and V_{FB} will depend upon the gate bias. That is, equation 3.9 is non-linear. A more accurate prediction of V_{Th} requires a self-consistent solution which allows both the barrier depletion region and the barrier capacitance to change.

Figure 3.4 illustrates the dependence of V_{Th} on N_{ob} with doping in the silicon part of the active region, $N_{a,Si}$, as a parameter. From Fig. 3.4, it can be seen that the design of the heterostructure will determine if the HFET is enhancement or depletion mode. Also, with increasing charge sheet doping density, the

V_{Th} values predicted are seen to decrease rapidly and with a non-linear dependence. The theory used by Lebbby [62] predicts V_{Th} will have a linear dependence on N_{ob} .

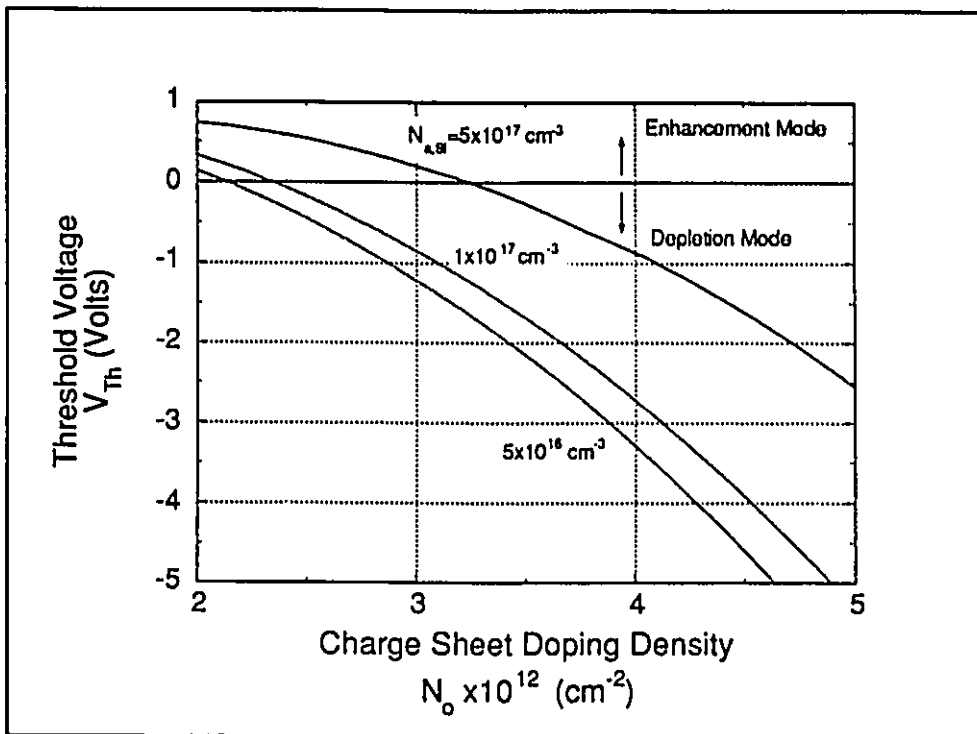


Figure 3.4: The calculated dependence of the HFET threshold voltage, V_{Th} , on the areal charge sheet doping density, N_{ob} , is plotted with active layer doping density, $N_{a,Si}$, as a parametric variable. Where the curves cross the $V_{Th}=0V$ line, the device is predicted to be depletion mode.

Leakage current from the gate of the HFET biased at V_{Th} will also be strongly dependent on the design of the heterostructure. A larger energy barrier at the n-n heterojunction inhibits gate leakage via thermionic emission and this dependence is exponential (see eqn. A1 in appendix A).

With increasing doping in the charge sheet, the equilibrium barrier surface potential, V_{b0} , is predicted to increase. This is seen in Fig. 3.5. V_{b0} is seen to be very sensitive to N_{ob} over the range from $1 \times 10^{12} \text{ cm}^{-2}$ to $3 \times 10^{12} \text{ cm}^{-2}$. For a depletion mode device biased at V_{Th} , the barrier layer-charge sheet junction is reversed-biased and the only gate leakage expected is the reverse saturation current.

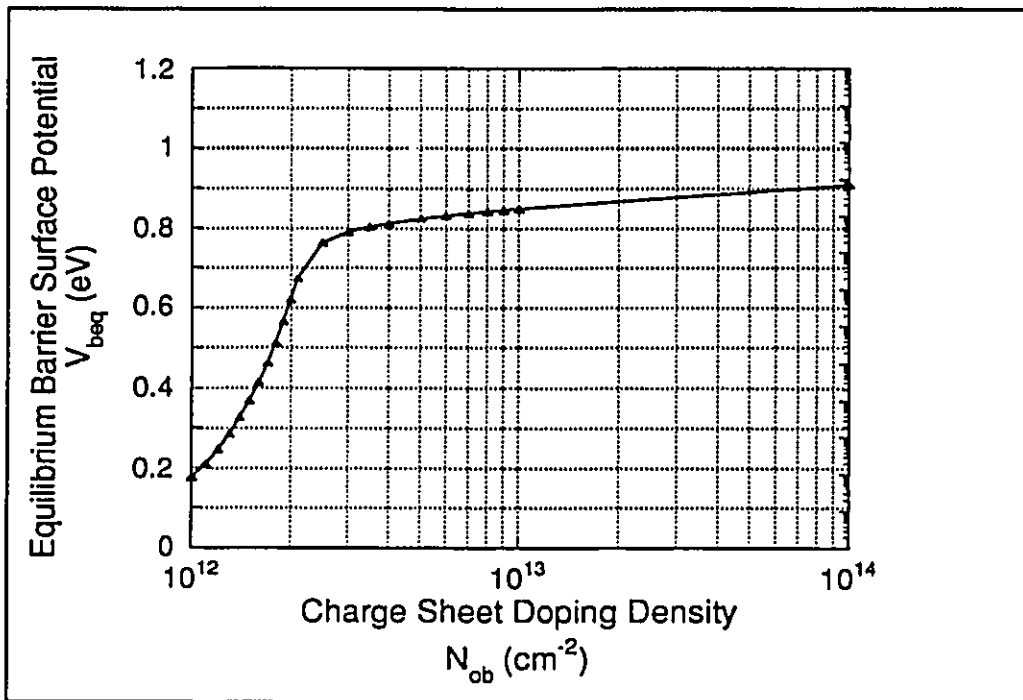


Figure 3.5: The calculated equilibrium barrier surface potential, V_{beq} , versus the areal charge sheet doping density, N_{bo} , in the HFET.

In the HFET, ΔE_{Fpj} is directly related to the interface charge (eqn. 2.8 and 2.9). Thus, if the doping in the charge sheet is changed, this has an effect on the charge in the channel, and therefore the degree of dopant ionization in the charge sheet is also changed. In Fig. 3.6, the dependence of interface charge, p_o , on the

charge sheet doping is illustrated with and without consideration of the charge sheet dopant de-ionization. As the charge sheet doping is increased, the charge at the interface is also observed to increase. However, the rate of increase of the interface charge is reduced for higher charge sheet doping.

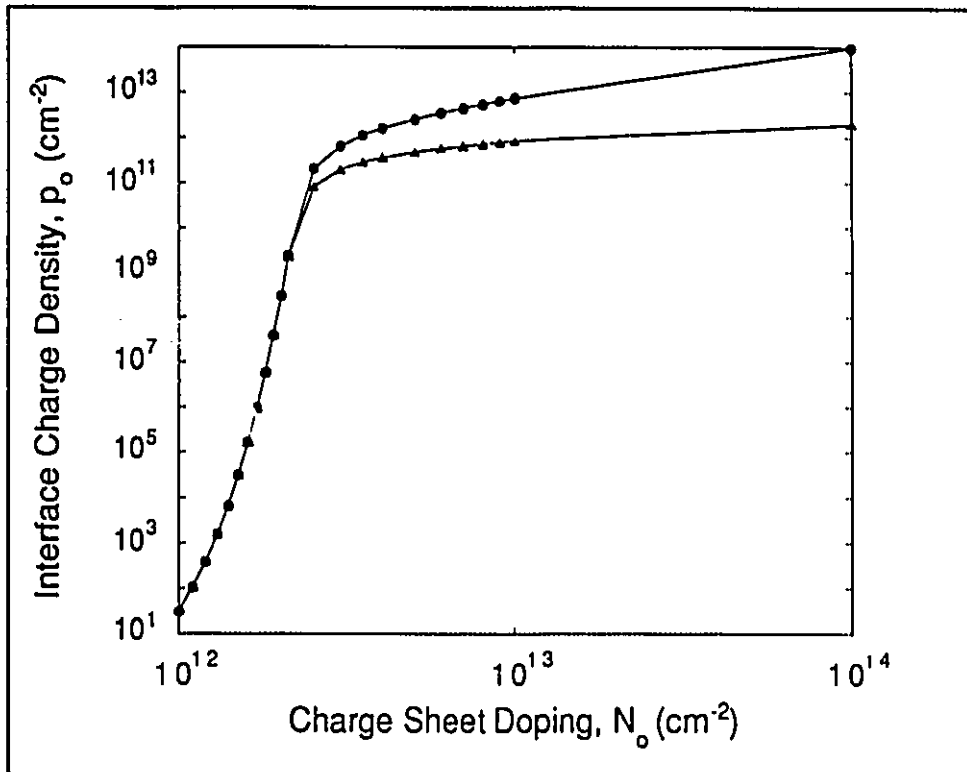


Figure 3.6: The dependence of the hetero-interface charge density, p_0 , on the doping in the charge sheet is plotted with and without consideration to the degree of charge sheet dopant ionization.

With respect to the operation of the device, if under some bias conditions the charge at the hetero-interface becomes so large that the dopant in the charge

sheet becomes partially de-ionized then again a self-consistent solution is required. Ultimately, this lowers device transconductance since:

$$g_m \approx K \frac{\Delta p_0}{\Delta V_g}, \quad (3.12)$$

where K is a constant of proportionality.

By finding a value for p_0 which satisfies equations 2.1-2.8, the dependence of device transconductance on gate bias can be estimated. In Fig. 3.7, the dependence of the transconductance, g_m , on the gate bias is illustrated with and without consideration of the charge sheet dopant de-ionization. In both cases, the rate of growth of $\Delta p_0/\Delta V_{gs}$ increases as gate voltage squared as the barrier is progressively forward-biased. However, the effect of dopant ionization is to lower the sensitivity of the channel to the gate bias.

Another characteristic which is affected by the design of the heterostructure is frequency response. Excluding parasitic circuit elements, the high frequency response of the HFET is determined by the capacitance of the barrier layer-charge sheet junction (or the gate to drain capacitance, C_{gd}). The design of the heterostructure can minimize this capacitance. A low barrier layer doping will be conducive to low intrinsic device capacitance. Here, some design trade-offs are required. In order to make the DOES device, a low resistivity contact is desirable and, therefore, a barrier with high doping is preferred. Conversely, to optimize frequency in the HFET, a barrier with low doping is needed.

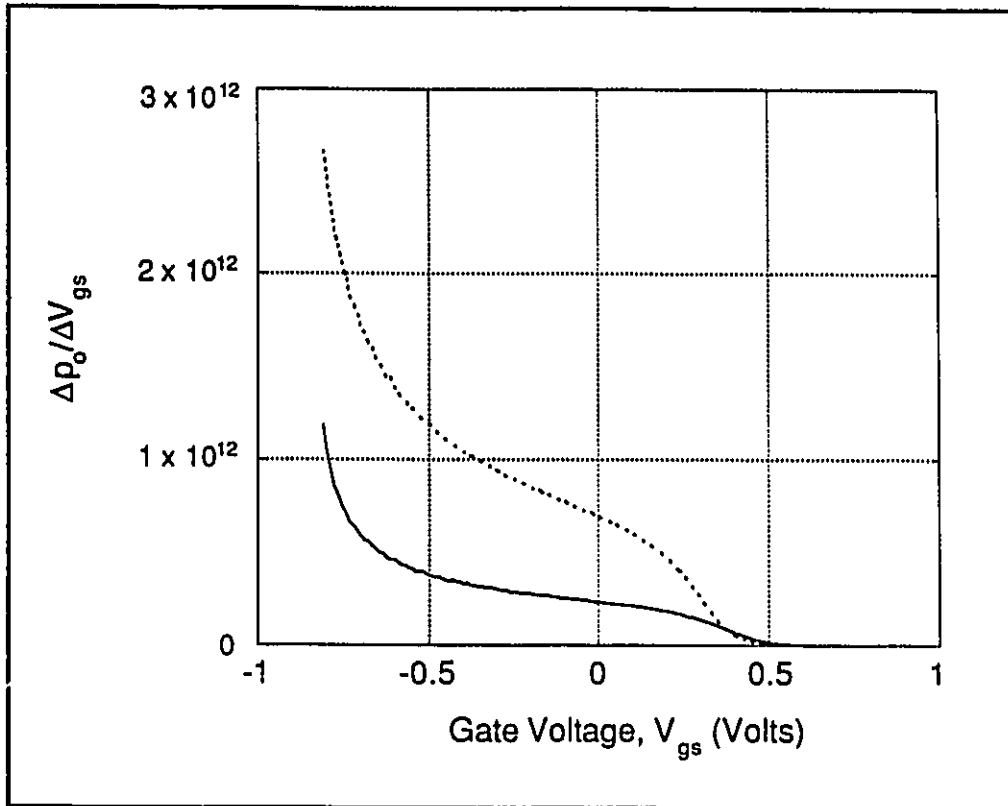


Figure 3.7: The dependence of the effective transconductance, g_m , on the gate bias is plotted with and without consideration to the degree of charge sheet dopant ionization.

3.3.2 Effect of Parallel-Path Gate Leakage

An ohmic contact to the gate is made in the inversion-channel technology. A gate current, I_g , can flow and play an important role in the device operation. A second factor which can be identified as affecting device transconductance is parallel gate current arising from the structure of the device. Referring to Fig. 3.8, as the gate voltage is increased (negative with respect to the source and drain) one observes a forward-biased diode characteristic (I_{IS} and I_{ID} for small V_{DS}). That is,

from the gate (the barrier layer) to the implanted source and drain contacts, an n^+ p^+ diode is seen as a parallel current path.

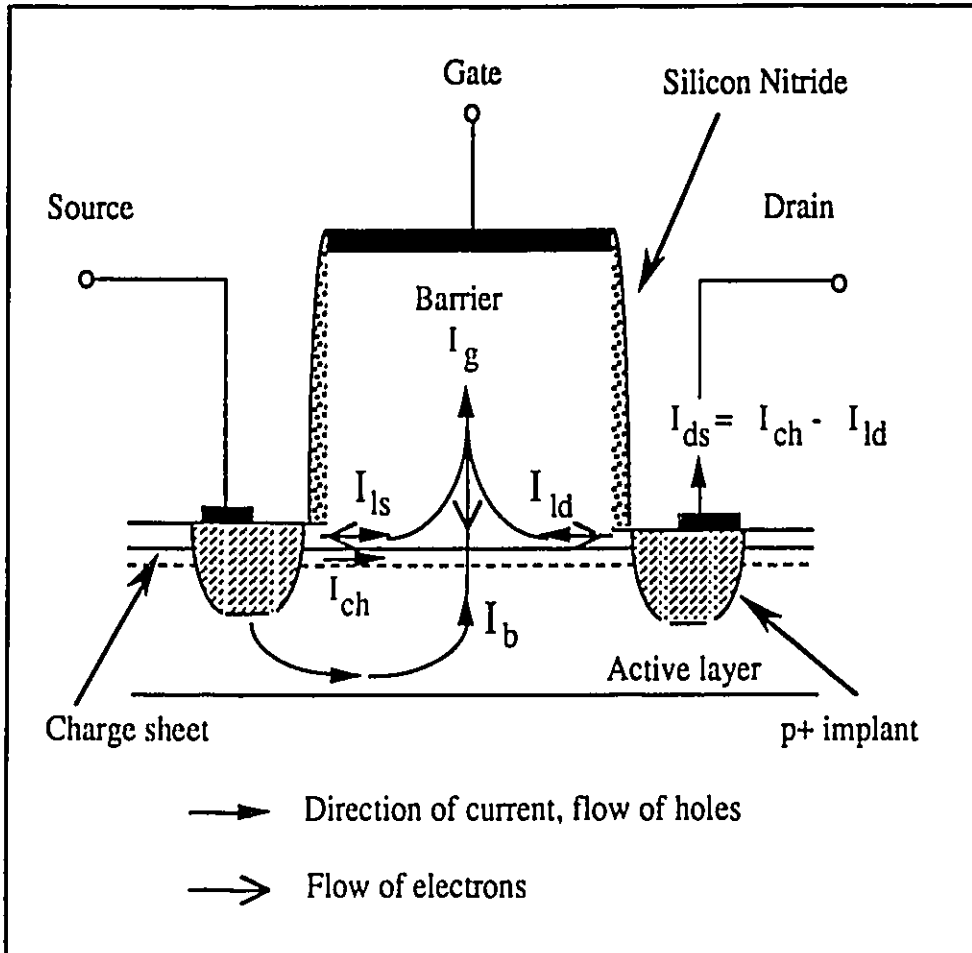


Figure 3.8: A cross-sectional view of the HFET with gate leakage pathways illustrated. I_b represents the total current over the barrier, I_{ls} and I_{ld} are the currents leaking from the barrier layer to the source and drain contacts, respectively, and I_{ch} is the channel current flowing from source to drain.

This component adds to the gate leakage, and, until the potential on the drain is raised above that of the gate, also subtracts from the drain current. That is, when

experimentally evaluating the source-drain current, I_{ds} , the actual current measured is:

$$I_d = I_{ch} - I_{ld} , \quad (3.13)$$

where I_{ch} is the channel current. Also, current flowing from the gate causes an ohmic voltage drop which must be considered in the denominator of eqn. 3.12. As a parallel conduction path, the potential drop across the barrier to the active layer (at the source end) can never exceed the drop across the n-p⁺ diode.

With increasing V_{ds} , gate current leaking to the drain will decrease exponentially and saturates at a constant value. The constant value represents the current coming over the barrier into the active region (I_b) and current leaking out the forward-biased n-p⁺ diode formed by the gate and implanted source contact (I_{ls}). The latter component can be reduced by etching as close as possible to the charge sheet when forming the gate mesa. In this manner, only a thin electrical connection is made between the gate and the source contact on the side of the barrier closest to the surface.

3.3.3 Effect of Gate Leakage on the Active Layer

The third phenomenon which can affect device transconductance is gate leakage over the barrier (I_b in Fig. 3.8). In the SiGe/Si HFET, as V_{gs} becomes progressively larger, (increasingly negative values) the height of the triangular barrier is reduced. In this case, electron flow over the barrier (I_b from gate to active region) increases exponentially. The electrons which accumulate in the active region forward-bias the active-source junction and (at small V_{ds}) the active-

drain junctions, and leak to ground through the implanted contacts. This causes a voltage drop (V_j) between the contact and the active region. Thus, the MOSFET assumption that the Fermi level in the channel is matched to that in the active region is no longer valid. Now for a given I_b , ϕ_T becomes $(\phi_T - \Delta\phi_T)$ where:

$$\Delta\phi_T = V_j = V_t \ln \left(\frac{I_b}{I_{a0}} \right), \quad (3.14)$$

and I_{a0} is the saturation current of the source-active layer diode. With gate leakage, ϕ_{SiGe} and ϕ_{Si} do not increase monotonically as in the case of a MOSFET, but rather, decrease with increasing gate leakage. This augments the channel population since the depletion charge associated with ϕ_{SiGe} and ϕ_{Si} now become smaller with increased negative gate bias as eqn. 2.1 must still be satisfied.

Calculating the gate leakage over the barrier is difficult. Following the path of I_b , we see that the current traverses an npnp structure, with one of the p-layers being the charge sheet. This type of structure is commonly referred to as the double heterostructure opto-electronic switch (DOES) and must be analyzed with due consideration to carrier feedback. Rather than attempting to couple the equations governing both current and potential, we simplify the analysis by assuming the change in surface potential of the barrier, ΔV_b , is related linearly to the change in surface potential of the active region, $\Delta\phi_T$. That is:

$$\Delta\phi_T = k \Delta V_b, \quad (3.15)$$

where k is a constant between 0 and 1. Thus, shrinkage of the barrier depletion region induces some shrinkage of the active layer depletion region.

In Fig. 3.9, a simulation of $\Delta p_o / \Delta V_{gs}$ versus the gate bias is illustrated with and without consideration to the forward-biasing of the active-source and -drain junctions and using $k=0.25$ in eqn. 3.15. For negative gate bias, the simulated effect of the gate current is to increase $\Delta p_o / \Delta V_{gs}$ (and thus g_m) above values determined without considering gate current.

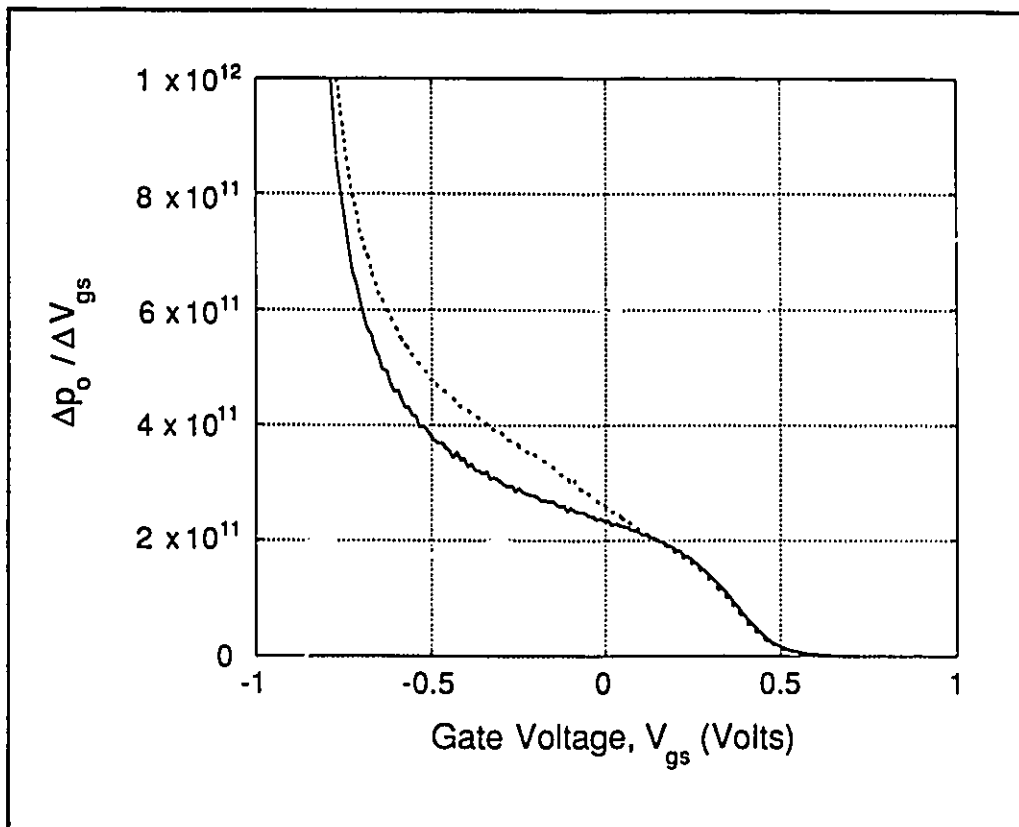


Figure 3.9: The dependence of transconductance, g_m , on the gate bias is plotted with and without consideration to the effect of gate leakage. The dotted curve includes the simulated effect of the gate leakage into the active layer whereas the solid line represents the results of the simulation when this phenomenon is ignored.

At this point it must be stressed that the calculations presented thus far are relevant only for small source-drain bias ($V_{ds} \ll V_{gs} - V_{Th}$). For larger V_{ds} values, the majority of the electron gate leakage escapes via the source contact. Figure 3.1 illustrates the three-dimensional energy band diagram which applies for non-zero V_{ds} . Now, at the drain end of the FET, very little current flows over the barrier and a large difference between the Fermi level in the channel and active layers at the drain end is to be expected since this junction is reverse-biased. A concentration of barrier current is found at the source end and, therefore, also a difference between the Fermi levels in the channel and the active layer representative of forward-bias conditions. Clearly, a two-dimensional analysis, is required.

CHAPTER 4

HETEROSTRUCTURE GROWTH & DEVICE FABRICATION

This chapter describes the growth and analysis of the heterostructure used to implement two- and three-terminal DOES and HFETs and also the fabrication of these devices. Three batches of devices were fabricated from wafer #951 which was grown by molecular beam epitaxy (MBE) at the National Research Council's Institute for Microstructural Sciences (IMS). Batch D1 constituted the fabrication of two-terminal DOES devices utilizing a primitive wet chemical processing procedure. Batch D2 constituted the fabrication of three-terminal DOES with the third terminal contacting the active layer. Again, with batch D2, a primitive fabrication procedure was used. In the final batch, D3, both two- and three-terminal DOES with the third terminal contacting the inversion layer, and HFETs were fabricated. Batch D3 comprised the most sophisticated fabrication sequence and required the highest degree of mask transfer resolution. In addition, batch D3 differed from D2 and D1 in that the process utilized a 'self-aligned' technique which allowed for much smaller devices and much finer control over the separation of the third terminal from the device mesa. This may be an important factor in attempting to determine the sensitivity of the DOES to the third-terminal input. The sensitivity of a device with a third-terminal far removed from the mesa will suffer from current spreading effects.

4.1 Growth and Analysis

This section is concerned with the growth and subsequent physical analysis of the Si/Si_{1-x}Ge_x heterostructure used to realize inversion-channel devices. Details of the growth are given. Analysis techniques employed include transmission electron micrography, secondary ion spectroscopy, and rocking-curve x-ray diffraction spectroscopy.

4.1.1 Heterostructure Growth

The target heterostructure, illustrated in Fig. 2.1, was grown by MBE on a 100 mm diameter p⁺-Si(100) substrate ($2 \times 10^{18} \text{ cm}^{-3}$ boron). MBE is the preferred growth technique for this heterostructure where doping, layer thickness, and alloy composition need to be rigidly controlled. Alternative techniques such as chemical vapour deposition (CVD) have less ability to target a specific heterostructure design but are capable of higher growth rates and higher doping densities in grown layers [64]. Before growth was initiated, the substrate was treated to an ultra-violet ozone environment and, then placed within the growth chamber. Any native oxide on the surface was desorbed at $\approx 900^\circ\text{C}$. The background pressure within the growth chamber was $\approx 1 \times 10^{-9}$ mbar and is composed mainly of H₂ and CO.

Initial growth occurred at a substrate temperature of 500°C and a constant Si rate of $0.5 \text{ nm}\cdot\text{s}^{-1}$ to form the 1000nm-thick active Si layer, which was doped n-type using a low-energy (200eV) As ion source [65]. The temperature was then ramped during the growth down to 400°C over 120s and held there for all subsequent layers. Low growth temperatures favor metastable, strained hetero-

structures by suppressing the formation of misfit dislocations at Si/SiGe interfaces [66]. A 5nm-thick p⁺-delta layer with $2 \times 10^{18} \text{ cm}^{-3}$ B was incorporated using a high-temperature elemental B sublimator [67].

The Si_{0.75}Ge_{0.25} well was targeted to be 600Å thick. The critical thickness of this alloy is approximately 800Å as predicted by the theory of People et. al. [48] and supported by the experimental data of Bean et. al. [68]. In theory, the Si_{0.75}Ge_{0.25} well is coherently strained and therefore has a lower band gap than the bulk alloy. People predicts the indirect band gap of the alloy to be 0.88eV [38] and the valence band offset with Si ($E_g=1.12\text{eV}$) to be $\approx 0.185\text{eV}$ [69].

4.1.2 Transmission Electron Micrography of Wafer #951

Figure 4.1 is a transmission electron micrograph (TEM) of the heterostructure. Using a calibration of the magnification factor (magnification, $\approx 153\,000$), the actual thickness of the Si_{0.75}Ge_{0.25} well is found to be 590Å (target 600Å) and the thickness of the barrier layer is seen to be 4300Å (target 3000Å). This is critical information from the perspective of device processing. The height of various mesa formations will depend on the actual thickness of the layers grown. The image also indicates that after growth the Si_{0.75}Ge_{0.25} well is free of strain-relieving dislocations. However, within the layer representing the alloy on the TEM are seen slight contrast fluctuations indicative of fluctuations in the Ge content. Surrounding the alloy layer in the TEM is also a gradual contrast lightening which is indicative of the strain relief as one move away from the Si_{0.75}Ge_{0.25} well. In order to preserve the strained nature of the Si_{0.75}Ge_{0.25} well, device processing temperatures were restricted to 550° C.



Figure 4.1: The transmission electron micrograph (TEM) of MBE growth #951.

4.1.3 Secondary Ion Spectroscopy of Wafer #951

In Fig. 4.2, the secondary ion mass spectrograph (SIMS) of the heterostructure is seen. This analysis tool provides a measure of the concentration of specified atomic species as a function of depth in the heterostructure. It is a destructive technique in which an ion beam (cesium) mills a crater into the surface of the slice and the released secondary ions are analyzed by mass spectroscopy. The positional dependency is found by determining the final depth of the crater and using the total milling time. One assumes a constant milling rate and the crater has areal dimension of $400\mu\text{m} \times 400\mu\text{m}$ square which the ion beam rasters.

The data presented in Fig. 4.2 was obtained at the National Research Council Canada. In the SIMS analysis performed on Wafer #951, three species were counted: boron, germanium, and silicon. Boron, with atomic weight 11, identifies layers with p-type doping which includes the charge sheet and the substrate. In Fig. 4.3, the processed data from the SIMS analysis plots boron concentration versus depth into the sample. The charge sheet is seen at approximately 4000\AA and has peak concentration of $\approx 1.5 \times 10^{18} \text{ cm}^{-3}$. The full width at half maximum of the boron peak is seen to encompass 400\AA . This is not a reflection of boron diffusion but rather the depth resolution of SIMS. Also, it must be noted that SIMS analysis counts all the boron yield off the slice and makes no discrimination of whether the boron was activated as a dopant or not. That is, interstitial boron incorporated in the Si lattice is counted equally as well as substitutional boron. The target doping for the charge sheet was 50\AA at $5 \times 10^{18} \text{ cm}^{-3}$ which corresponds to an overall doping density of $2.5 \times 10^{12} \text{ cm}^{-2}$.

The lack of resolution of the SIMS analysis requires that the area under the peak be evaluated to determine how much doping is in the sheet. Assuming a

triangular peak with base 1000\AA and height $1.5 \times 10^{18} \text{ cm}^{-3}$ gives a total doping of approximately $3.2 \times 10^{12} \text{ cm}^{-2}$. The boron count returns to the noise level in the barrier and the active layers. The boron count again becomes significant in the

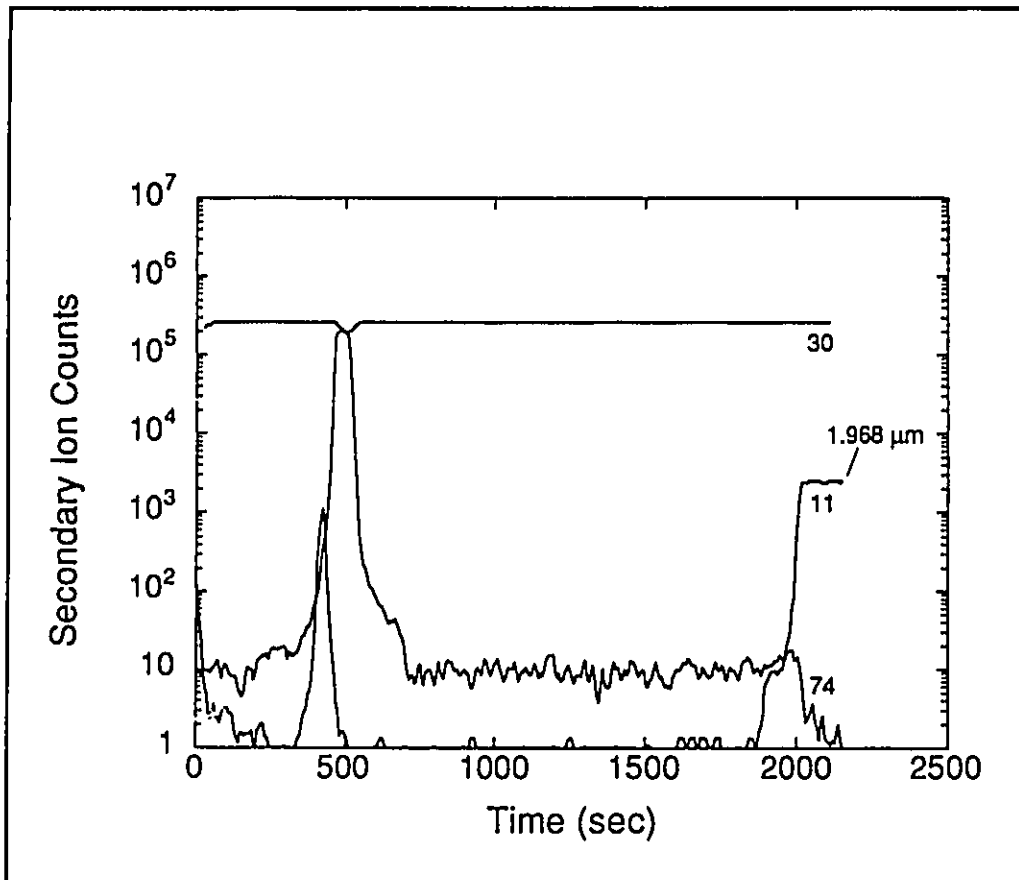


Figure 4.2: The Si (30), B (11), and Ge (74) profile of wafer # 951 obtained by SIMS.

substrate. Using a surface profilometer the final depth of the crater was measured as $1.968\mu\text{m}$ (milling time ≈ 2150 sec).

The Ge count is low except in the SiGe well placed next to the boron charge sheet. After approximately 500 sec. of milling, the Ge (atomic weight 74)

count climbs to virtually the same level as that of the Si (atomic weight 30, Fig. 4.2). Interestingly, the Ge count in the barrier and Si active layers is higher than the count in the substrate. This would indicate that even when attempting to grow pure Si layers by MBE, memory effects from prior SiGe layer growths create a residual Ge content in the Si layers. However, no deleterious effect is expected from the small Ge content in the Si layers.

The SIMS analysis of the Ge content in the heterostructure provides confirmation of the position of the well with respect to the charge sheet and corroborates the TEM evidence of the thickness of the SiGe well. The actual Ge content of the $\text{Si}_{0.75}\text{Ge}_{0.25}$ alloy was determined by rocking-curve x-ray spectroscopy.

4.2 Batch D1

Batch D1 was the first device fabrication of two-terminal Si/SiGe-based DOES. The most simplistic processing sequence was designed to maximize yield and expedite functional devices from wafer #951. The process sequence is illustrated in Fig. 4.4 and outlined below.

4.2.1 Wafer Cutting and Cleaning

Wafer pieces (#951-1, #951-2), $\approx 1.5 \text{ cm}^2$, were cut from the wafer using the diamond scribe technique. In this technique, the wafer is placed on a clean yielding surface (for example, six sheets of filter paper) such that the back of the slice faces upwards. A clean glass microscope slide is used to guide the diamond

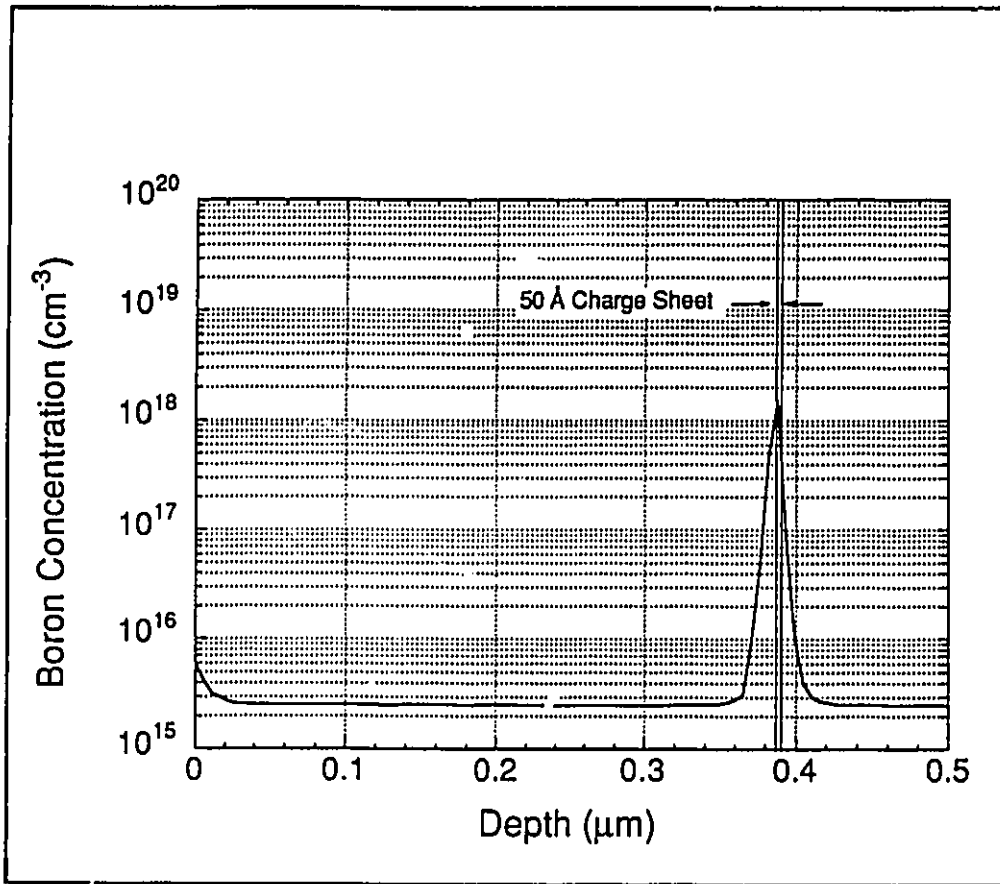


Figure 4.3: The calibrated boron concentration profile of wafer #951.

scribe as a scratch is made along the length of the wafer. Dust arising from the scratch is quickly blown away and to avoid causing abrasions on the polished side of the wafer. The wafer is then placed again on a new clean and yielding surface such that the scratch faces upwards. Six or seven sheets of clean filter paper are then laid on top the wafer. A moderate amount of rolling pressure is then applied to the back of the wafer using a glass or steel rod of ≈ 1 inch diameter. The pressure is applied such that the axis of the rod is parallel to the scratch. When

cutting small pieces, simply applying downward pressure with a rounded implement may be sufficient.

Some preparation should be made to comprehend the most probable direction of wafer cleave and the resultant angle the cleave makes with the surface of the slice. Upon cleaving (or breaking), again the dust is blown away with dry nitrogen and the sheet of filter paper in contact with the piece are discarded. This will minimize surface abrasions on the polished side. This procedure is repeated with each new division of a slice. In addition, a map of the wafer and the historical location of the cut pieces should be recorded. This is a prudent measure in light of the spatial variations in layer thickness, composition, and doping which arise in MBE grown heterostructures.

Following division of the wafer, slices were degreased and cleaned. The procedure for degreasing is as follows. Slices are first immersed in 80 ml trichloroethylene at 50°C for 3 minutes. In addition, during that time the slice experiences agitation in an ultra-sonic bath. The bath transmits to the slice and beaker ultra-sonic vibrations which can damage the slice if insufficient liquid is used in the beaker. For slices which have been thinned to less than 300µm the ultra-sonic bath should be avoided. During this time, another beaker is prepared with 80 ml of acetone at 50°C. Following the elapse of 3 minutes in the trichloroethylene, the slice is transferred to the acetone quickly to avoid drying of the slice. If left to dry, the slice will be stained with remnants of trichloroethylene. A beaker with 80 ml of methanol at 50°C is also prepared and following the elapse of 3 minutes in the acetone, the slice is transferred to the methanol in the same quick manner. The slice remains in the methanol for 3 minutes and is then quickly transferred to large beaker of deionized water (DI) to rinse for 5 minutes. In this degreasing procedure, the trichloroethylene is the most potent degreasing

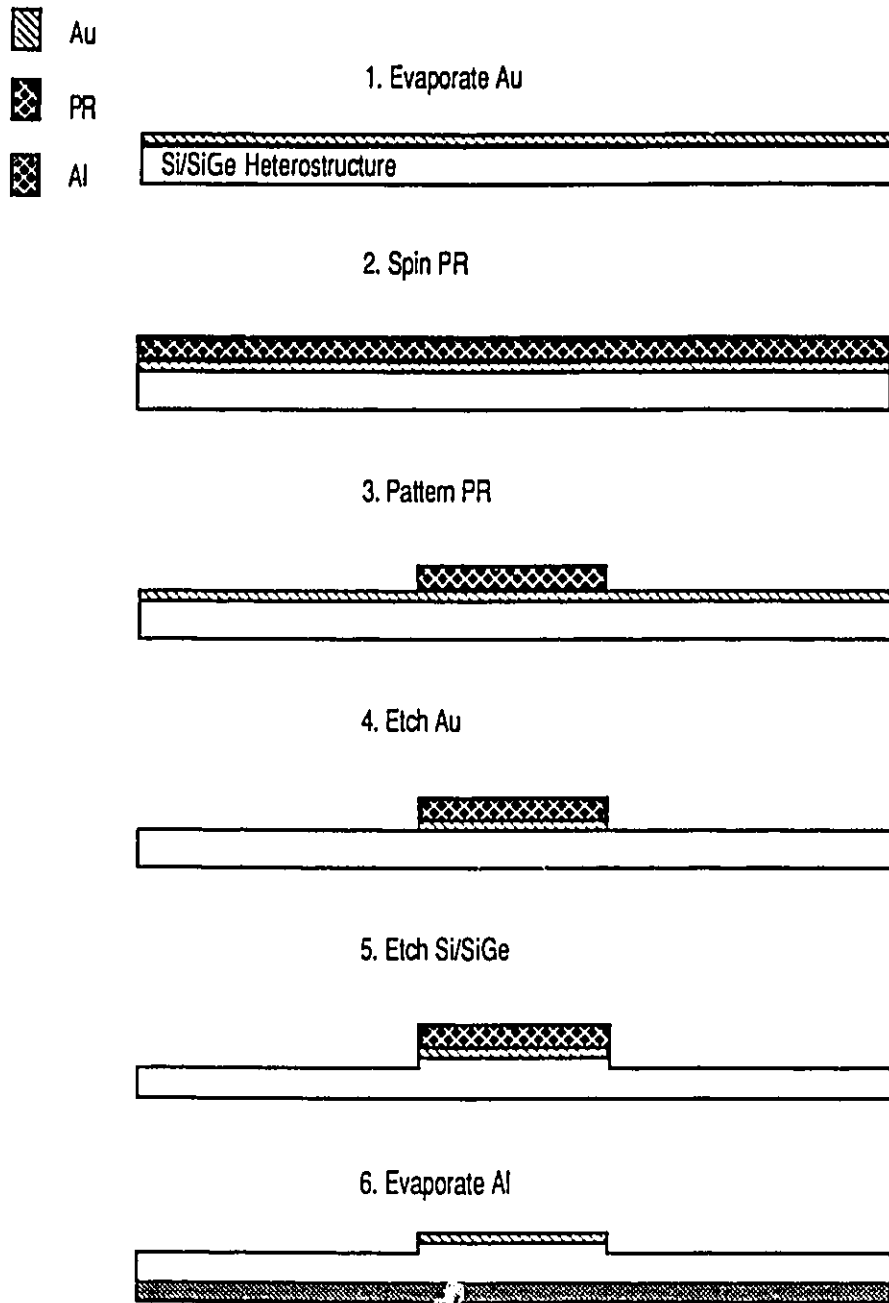


Figure 4.4: The fabrication sequence for batch D1.

agent while the acetone is used to rinse the trichloroethylene. Methanol is used to rinse the acetone from the slice and the DI is used to finally rinse the methanol.

Following degreasing, and immediately prior to the deposition of the first metal contacts, the native surface oxide is removed using a hydrofluoric acid (HF) dip. In this process the slice is immersed in 10:1 DI:HF solution for 10 seconds and then rinsed in copious quantities of DI. The slice is blown dry using nitrogen and then quickly loaded into the metal deposition system. This minimizes contamination of the slice and re-oxidation of the surface.

4.2.2 Metallization & Photolithography

The metal deposition system utilizes an electron beam to heat and evaporate metal placed in a carbon hearth. The first metallization used in the fabrication of the Si/SiGe-based DOES was 1000\AA of Au as measured using a crystal thickness monitor (step 1 of Fig. 4.4). Following metallization, a photoresist pattern was established on the slice to delineate areas where a Au etch would remove the metal. Positive photoresist ($1\mu\text{m}$ PR) was applied using the spin-on technique (4000 rpm for 30 seconds) and subsequently prepared for exposure by 'soft' baking at 90°C for 30 minutes (step 2 of Fig. 4.4). The slice was then exposed to ultraviolet light (wavelength 365nm) for 7.5 seconds through a photolithographic mask with opaque circular areas of various diameters ($100\mu\text{m}$ - $600\mu\text{m}$). Areas where the light was incident upon the PR were rendered sensitive to a developing solution which dissolves PR. The developing solution, supplied by the manufacturer of the PR, was diluted with DI in the ratio of 5:1 DI:Developer. The pattern on the slice was developed for 40 seconds and then rinsed in flowing DI for several minutes (step 3 of Fig. 4.4). The slice was then

given a post bake at 150°C for 1 min. to make the PR most resilient to chemical attack. With the PR pattern established, the Au was etched in a solution of KI:H₂O until visually, all the metal was removed from unprotected areas. This left the slice with circular areas of PR with underlying Au (step 4 of Fig. 4.4).

4.2.3 Mesa Etch

Using the same pattern of PR established for the Au etch, the slice was etched in a solution of HNO₃:HF:CH₃COOH in the ratio of 5:1:4 for 12 seconds (#951-2) and 28 seconds (#951-1). This resulted in mesa structures with height of 1.91 μm and 4.8 μm respectively (step 5 of Fig. 4.4). Referring to the heterostructure in Fig. 4.3, both of these values are sufficient to isolate the charge sheet and active layers. The aforementioned etch is part of a family of solutions often used in etching silicon. For example the 'CP4' etch [70] is commonly used for polishing silicon (etch rate = 80 μm/min.) and is made up from HNO₃:HF:CH₃COOH in the ratio of 5:3:3. Unfortunately, solutions from this family are quite vigorous and attack both Si and PR quickly. Only the most gross features can be etched using this etching family. No etch for Si has been developed which proceeds at a moderate rate (<1 μm/min) and can be used with a PR or SiO₂ mask.

The final step made towards the fabrication of these devices consisted of evaporating aluminum onto the back side of the slice. This metal contacted the p-substrate. Aluminum in silicon is a p-type dopant and forms an ohmic contact to p-type silicon when properly annealed [70]. For n-type silicon, a tunneling junction or 'high-low' junction is the only simple way to form a low resistivity contact using Al. In light of this, the final MBE grown layer of n-type silicon will be highly doped if a low resistivity contact is desired. This was the case for

wafer # 951 where the final 200Å of n-type silicon in the barrier layer was doped $1 \times 10^{19} \text{ cm}^{-3}$ with As. Putting a highly doped cap layer on heterostructure design is a common technique of facilitation a low resistivity contact. The exception to this is heterostructures designed for MODFETs or Schottky barrier devices.

Finished devices were given a heat treatment using the technique of rapid thermal annealing (RTA). In this technique, high intensity lamps are current driven in a feedback loop using a thermocouple. The slices were subjected to 450°C for 15 sec. The primary objectives of this step are to improve the metal to semiconductor contact in terms of lowering resistivity and metal adherence.

4.3 Batch D2

Batch D2 was the second device fabrication attempt. Both two- and three-terminal Si/SiGe-based DOES were fabricated. For the three-terminal device, the third terminal made contact to the active layer. Thus, when operating this device, the third terminal acts like an injector or extractor of electrons. Again, the most simplistic processing sequence was designed with gross alignment requirements on the order of 100µm. The process sequence is illustrated in Fig. 4.5 and outlined in the sections below.

4.3.1 PR Patterning and Mesa Etch

Wafer pieces (#951-3, #951-4), $\approx 1.5 \text{ cm}^2$, were cut from the wafer. After an initial cleaning quite similar to batch D1, the slices were patterned for the mesa etch (steps 1, 2 of Fig. 4.5). Again, PR was used as the photosensitive material. The pattern consisted of round PR dots ranging in dimension from 100 to 600µm

diameter. Following the developing of the PR pattern (as described in section 4.2.2), the slice was subjected to a descuming procedure. The objective of this procedure is to remove any organic residue from the slice in areas the PR has been developed away. The descum procedure uses a microwave source to excite an oxygen plasma at low pressure (≈ 10 Torr). The excited oxygen species is effective in removing carbon based molecules from the surface. For example, PR is removed at the rate of $\approx 50\text{\AA}/\text{min}$ in the system which was employed. The descuming system can remove up to $500\text{\AA}/\text{min}$ of PR and is sometimes utilized as a PR stripping technique when wet chemical methods have failed.

A post-bake of the patterned PR was also performed on the slice. The post-bake (10 minutes at 155°C on a temperature stabilized hot plate) is intended to make the pattern more resilient to chemical attack by the strong acids used in the mesa etch.

As with batch D1, the mesa etch was performed using a wet chemical bath which attacks the Si/SiGe layers at a fast rate. The $\text{HNO}_3:\text{HF}:\text{CH}_3\text{COOH}$ system was used in the ratio of 10:1:2. The time duration of the etch was 4 sec and violent agitation was applied concurrent to the etch. The mesa height, as measured using the surface profilometer DEKTAK, was found to be between 0.6 and $0.8\mu\text{m}$ (step 3 in Fig. 4.5). Referring to Fig. 2.2, this meant that the floor of the mesa was coplanar with the n-type active layer of the heterostructure.

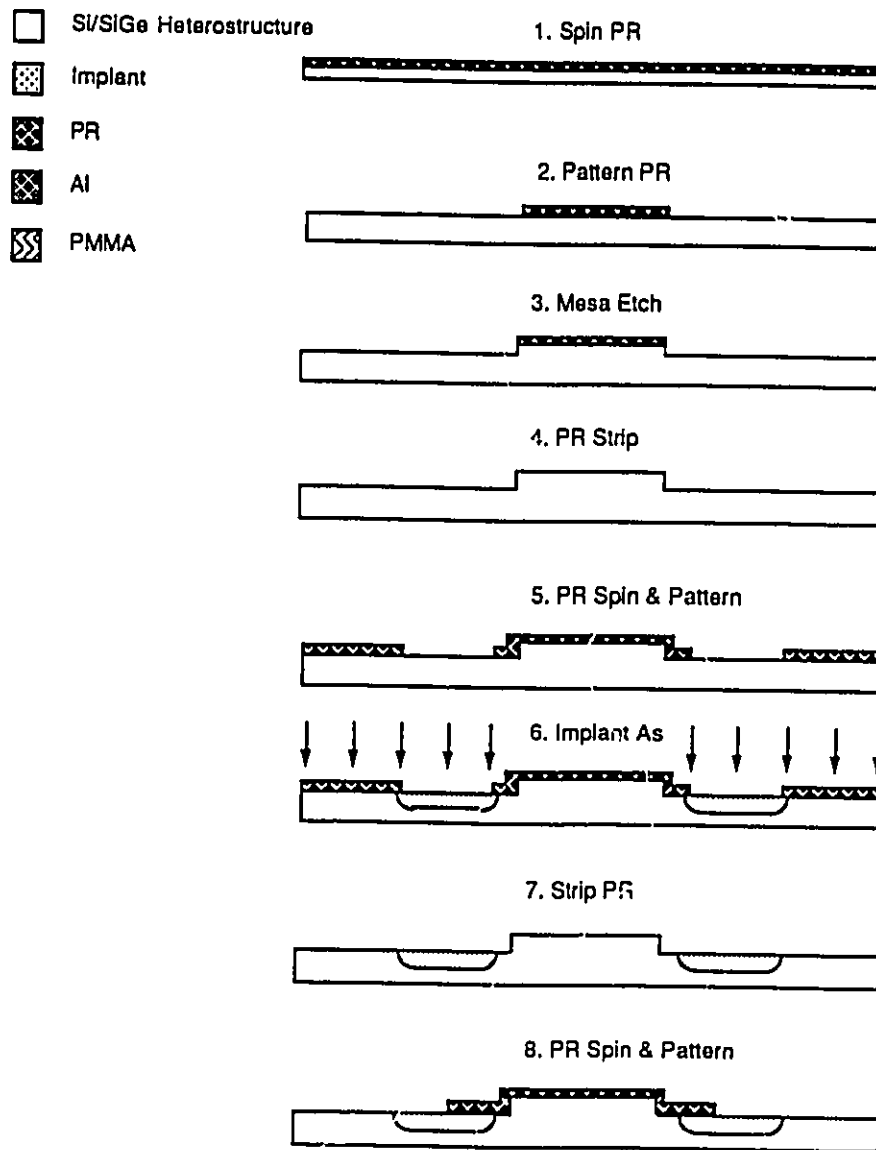


Figure 4.5: The fabrication sequence for batch D2 (steps 1-8).

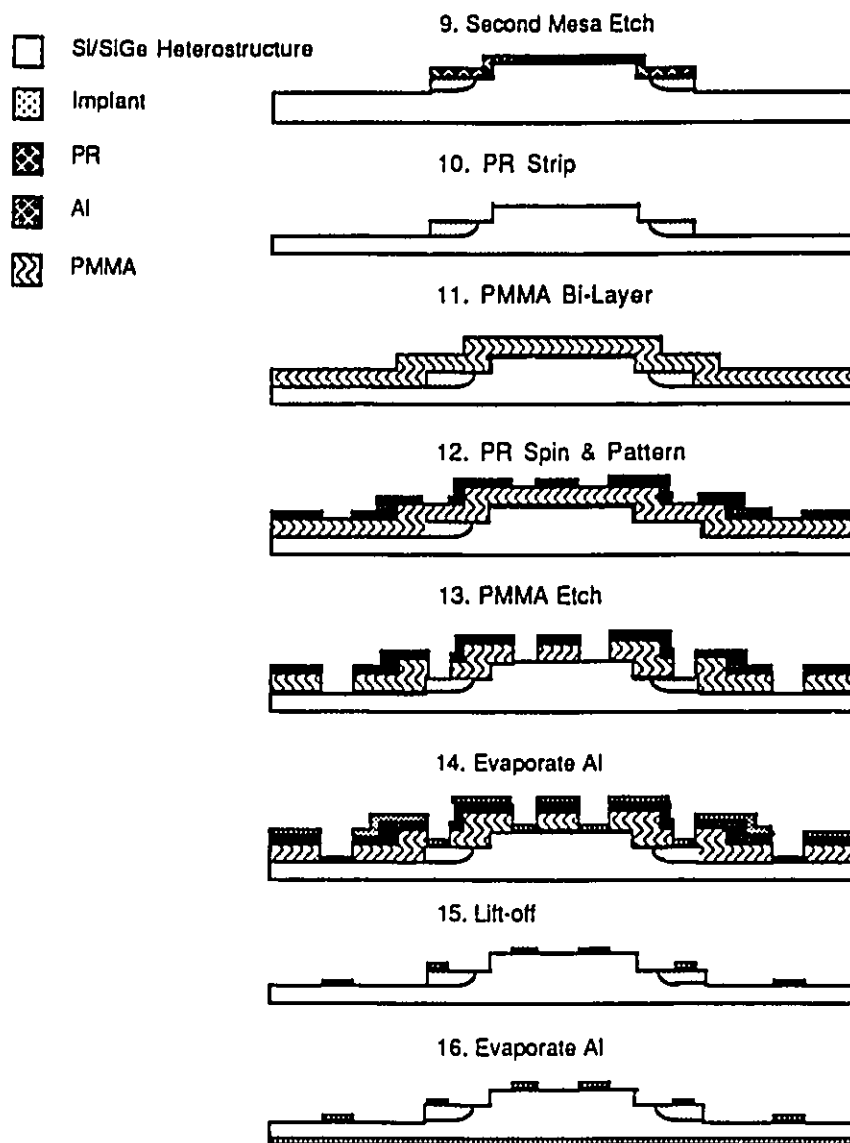


Figure 4.5 cont'd: The fabrication sequence for batch D2 (steps 8-16).

4.3.2 Implantation and Annealing

The PR from both slices was then stripped and re-applied so that fresh PR covered the top of the mesa and overlapped slightly all around the mesa (step 4, 5 in Fig. 4.5). The PR was intended to form an implantation barrier. Surrounding the mesa, implants to facilitate contact to the lightly doped n-type active layer were made (40keV As⁺ at a dose of $1 \times 10^{15} \text{ cm}^{-2}$ followed by 10keV As⁺ at a dose of $5 \times 10^{14} \text{ cm}^{-2}$). The implants were performed in such a manner that the slice surfaces were aligned 7° off normal beam incidence and were done at McMaster University. Implanted slices were then stripped of the PR mask (step 6, 7 in Fig. 4.5) by immersing the slices in an 80°C bath of NMP (di-methyl perodine). The NMP dissolves hardened PR and has little or no reaction with metal or the Si/SiGe. Following stripping, the slices were subjected to an RTA of 550°C for 2 minutes in order to anneal the crystalline damage induced by the ion implantation and to activate the dopant within the Si matrix. Normally, an As implant is subjected to much hotter temperatures ($\approx 800\text{-}950^\circ\text{C}$) in order to anneal damage and activate the dopant. However, in this case, the preservation of the strained nature of the Si/SiGe heterostructure took precedence over obtaining the lowest possible resistivity contact.

4.3.3 Second Mesa Etch & Lift-off

With the first mesa and implant established, it remained to isolate the devices and apply contact metal to the emitter, the active layer, and the substrate. To this end, PR was applied and patterned so that a larger area was protected for the second mesa etch (step 8 in Fig. 4.5). A solution of 5:3:3 HNO₃:HF:CH₃COOH was used for 3 sec. with agitation. The PR was then

stripped and the second mesa height measured to be $>1.2\mu\text{m}$. Effectively, the etch brings the lowest surface of the wafer topology into the substrate and thereby isolates the active layer of each individual device (step 9 in Fig. 4.5).

The final steps in the fabrication sequence included patterning of the metallization and contact annealing. To pattern the two metal contacts on the surface of the slice, a bi-layer lift-off process was used (step 10-15 of Fig. 4.5). The bi-layer procedure is required for metal lift-off patterning when the metal is quite thick ($\approx >8000\text{\AA}$) or when the topology of the surface of the slice is severe. The bi-layer lift-off is required in this fabrication process because of the severe topology. For instance, the first mesa rises almost $2\mu\text{m}$ above the floor of the slice.

In general, the lift-off technique is used when etching the metal is undesirable or a fine lithography is required. In lift-off, the PR pattern is first established and the material to be lifted off is placed on top of the PR. In areas where there is no PR, the metal is also deposited. The slice is later immersed in a chemical which first bloats and then dissolves PR (typically acetone or NMP). The metal deposited on the PR is lifted from the surface of the slice and the metal which was deposited on clear areas remains. This procedure is facilitated by the fact that the metal forms a discontinuous film on the slice and no tearing of the metal is required. The metal is deposited in a highly directional manner and the edge of the PR pattern is shaped into a form which incorporates an overhanging lip. The lip and the vertical nature of the pattern edge creates a space where no metal can be deposited.

The recipe for lift-off is much the same as for normal PR however, prior to developing the exposed pattern, a thin more resilient layer of PR is induced on the surface of the pattern by immersing the slice in chlorobenzene for 6 minutes. The

chlorobenzene is rinsed with trichloro, trifluoroethane (freon) for 15 sec., and the slice is blown dry with N₂. The freon is further driven off the surface of the PR by baking the slice on a hot plate for 60 sec. at 90°C. The initial soft bake (45 sec. at 70°C) prior to exposure is more moderate than the normal PR procedure. Development takes place in the same solution described above but now requires 2-3 minutes of immersion and gentle agitation. A visual inspection of the pattern is made and if required more development can take place. Of course, using the inspection microscope one must ensure that the UV component of the microscope's illumination spectrum is filtered out. Otherwise, inspecting the slice will, in fact, expose the slice.

The bi-layer lift-off is quite similar to the conventional lift-off procedure. In the bi-layer lift-off, prior to the PR, a layer of polymer (9% PMMA, 950K molecular weight) is applied and simply acts as a spacer between the surface of the slice and the PR. The polymer is dissolved in the open areas (no PR) after the lift-off PR pattern is established and, of course, before the metal is deposited. This allows much thicker metal lift-off and more severe topologies. In this fabrication sequence, 3000Å of Al was evaporated using an electron beam system for the bi-layer lift-off. The pattern consisted of a central metal dot surrounded by a metal ring. The dot is placed in the center of the first mesa and the ring contacts the ledge of the second mesa (step 14 of Fig. 4.5). Immediately prior to the evaporation, the slice was subjected to an acid dip as described in section 4.2.1. After the lift-off, the contact pattern was annealed at 450°C for 5 minutes. On the back of the slice, 3000Å of Al was also deposited and annealed to complete the fabrication.

4.4 Batch D3

Batch D3 was the final device fabrication run. In addition to the HFET, both two- and three-terminal Si/SiGe-based DOES were fabricated. In these three-terminal DOES devices, the third terminal contacts the inversion channel. The third terminal or, equivalently, the source and drain, can serve as an injector or extractor of holes. The mask set used for this final fabrication sequence was written using an electron beam system at Northern Telecom Electronics Ltd. and incorporated features and alignment tolerances of less than $1\mu\text{m}$. Nine mask levels were used. The fabrication sequence utilized a self-aligned technology and extensive use of the most modern etching and deposition systems in modern day VLSI. The facilities of the National Research Council's Institute for Microstructural Sciences (IMS) and the Solid-State Optoelectronic Consortium (SSOC) were used. The process sequence is illustrated in Fig. 4.6 and outlined in the sections below. A 1.5cm^2 slice (#951-6) was cut from the wafer for this process. In addition, in order to qualify the procedures that were developed, eight 1cm^2 slices of Si were processed in parallel.

4.4.1 Cleaning Procedures

The slices were first cleaned which included degreasing and an RCA4 cleaning. The procedure for degreasing or solvent cleaning is much the same as was described in section 4.2.1, however, in place of acetone and methanol, the rinse solution for trichloroethylene is iso-propanol. In addition, only dedicated

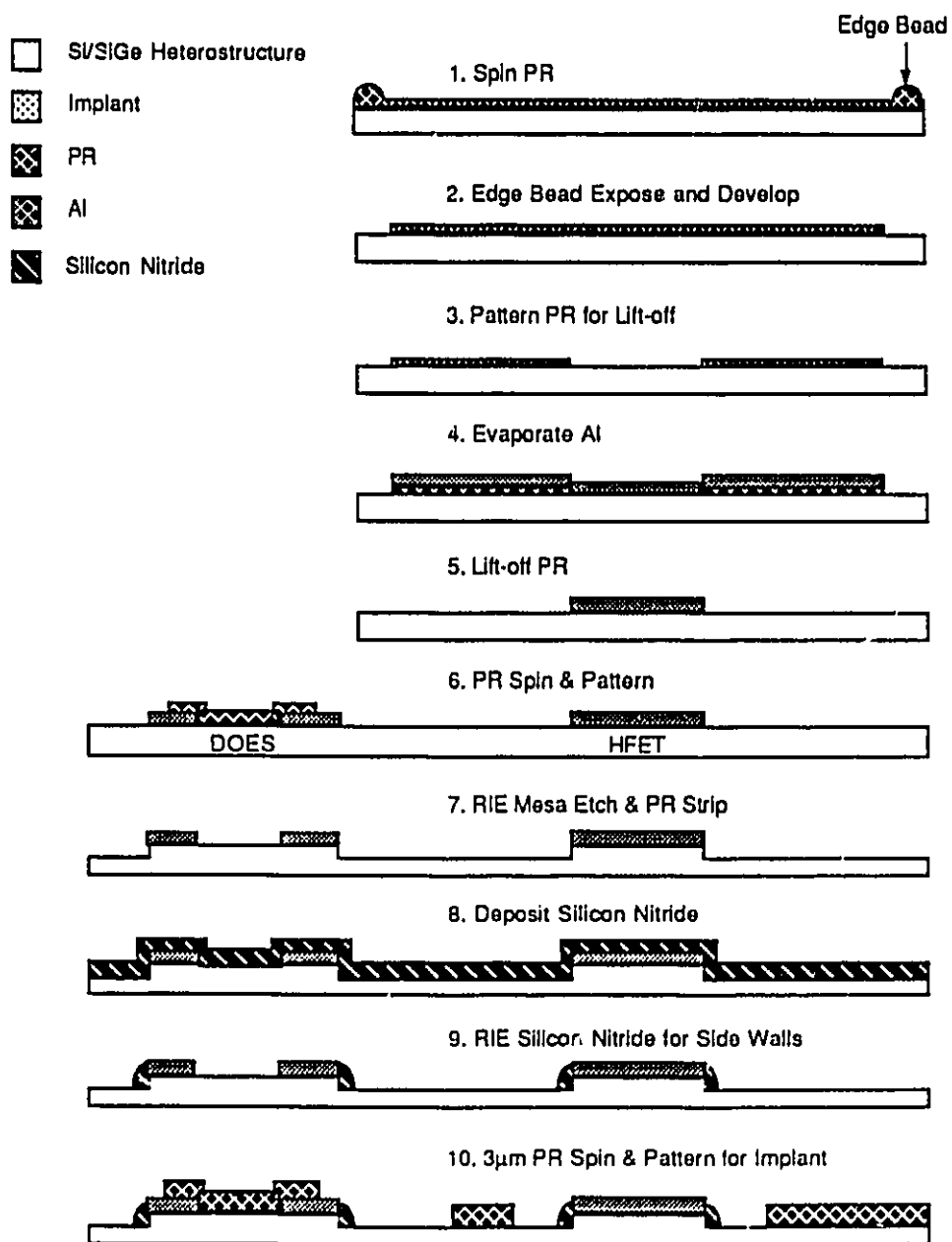


Figure 4.6: The fabrication sequence for batch D3 (steps 1-10).

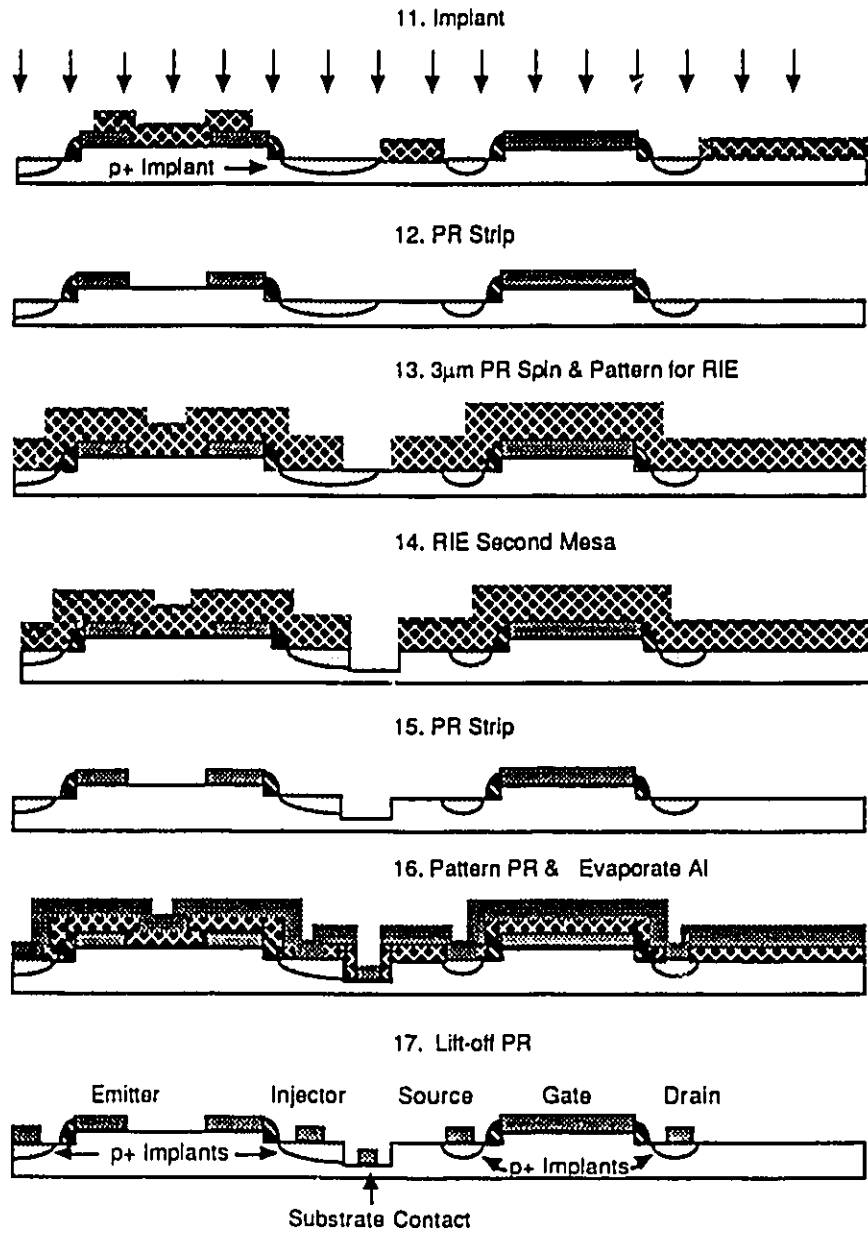


Figure 4.6 cont'd: The fabrication sequence for batch D3 (steps 11-17).

beakers are used. A two compartment cascade DI bath is used to rinse the isopropanol. Slices are blown dry with N_2 . The RCA4 cleaning is designed to remove surface contaminants from the surface of the slices. In this procedure, the slices are first placed in a solution of $NH_4OH:H_2O_2:DI$ (1:1:5) at $80^\circ C$ for 15 minutes. This solution is effective in removing organic contaminants. Preparing this solution, the DI is the final component added. Small slices tend to float in this solution as bubbles form on the slice. Slices were held in a Teflon basket which is compartmentalized to avoid slice-slice contact.

Next a solution of $HF:DI$ (1:10) is prepared and used at room temperature. Simply adding the acid causes a rise in the temperature of the solution to $\approx 30^\circ C$. The slices are immersed in this solution for 30 sec. to remove the native surface oxide. The third solution is $HCl:H_2O_2:DI$ (1:1:6) at $80^\circ C$. When preparing this solution, the H_2O_2 is added last. The slices are immersed in this solution for 15 minutes to remove metallic contaminants. Finally, a fresh solution of $HF:DI$ (1:10) is used for 30 sec. to remove oxide. After each solution, the slices are rinsed in DI and after the final rinse are blown dry.

4.4.2 Photolithography

The chlorobenzene lift-off process described in section 4.3.3 was used for all metal patterning in this batch. A slight variation was developed for the first gate metallization of this batch to enhance mask transfer resolution. The finest feature on the gate metal pattern is a $1\mu m$ metal gate line. The photolithographic process relies on contact image transfer. Good transfer requires that the mask is in intimate contact with the PR on the slice. Spinning PR creates an edge bead on the slice which inhibits good contact. The edge bead is a natural consequence of

surface tension as the PR spins off the edge. The bead can rise up to $8\mu\text{m}$ above the plain of the slice which is a problem when working with smaller slices. Larger slices or full wafers also form an edge bead but the effect is not as critical since over larger areas the mask can flex. In order to obtain the $1\mu\text{m}$ metal line, it was found necessary that the edge bead be removed using the following procedure. After applying the PR in the standard manner (step 1 of Fig. 4.6), a double exposure was added to the chlorobenzene lift-off procedure. The slice was first exposed through a mask that is translucent only at the edges of the slice. The exposure was extended to 2 minutes after the soft-bake of 70°C for 60 sec. This long exposure allow a very short developing time of 10 sec. in the standard developing solution (step 2 of Fig. 4.6). After 5 sec. of developing, the grip on the slice was changed. The slice was then rinsed in DI and blown dry. Now, the standard chlorobenzene lift-off could be followed minus, of course, the initial soft bake (step 3 of Fig. 4.6). Before metal to be lifted off is deposited, the slice is descummed and given an acid dip. Aluminum (3000 \AA) is used as the gate metal and is deposited using electron-beam evaporation (step 4, 5 of Fig. 4.6).

For reactive ion etching, the photolithography procedure is quite different. Here, fine lithography and stabilization of the PR is required. In this procedure, the film is applied by spinning the slice after a drop of PR has been placed in the center. The slice is spun at 5000 rpm for 30 sec. resulting in an $\approx 1\mu\text{m}$ film. A 60 sec. soft bake at 90°C prepares the film for exposure. The slice is exposed for 2.7 sec. and developed in 5:1 DI:Developer for 45 sec. After rinsing in DI and drying the slice, it is exposed to deep UV light (wavelength 260nm) for 15 minutes. Following this, the slice is baked for 10 minutes at 100°C on a hot plate and the deep UV exposure is repeated. Finally, the slice is baked at 120°C for 10 minutes to complete PR stabilization.



The stabilization cross-links the polymer bonds in the PR and makes it more resistive to attack in the plasma environment of the RIE. The PR is stripped in a bath of hot (80° C) PR stripper (Shipley A-30) for 20 minutes and then a bath of hot (80° C) iso-propanol to rinse the A-30. The slice is then rinsed in DI and subjected to the descuming procedure.

4.4.3 Reactive Ion Etching

In this fabrication procedure, extensive use of dry etching techniques was employed. These include reactive ion etching and plasma ashing. The IMS is equipped with an Ion and Plasma Etching (RIE 1000) system which employs a parallel plate chamber with 30 cm diameter electrodes. The system is equipped with mass flow controllers which are interfaced to a central computer in addition to various diagnostic sensors. For Si, SiGe alloys, and for Si₃N₄, the reactive species used were CH₃F and O₂. The flow rate of CH₃F was 50 sccm and that of O₂ was 2.5 sccm at a chamber base pressure of 2×10^{-6} torr. The O₂ was found to be a necessary in order to inhibit polymer deposition on the slice and subsequent micro-masking. With these flow rates and 75 watts of RF power, the etch rate for Si was 1800 Å/hr and for Si₃N₄ was 400Å/min. Unfortunately, the gate metal, Al, is also sputtered away at the rate of 600Å/hr and PR is removed at the rate of ≈ 5000 Å/hr. Thus, a 1µm mask of PR will be effective for only 2hrs of RIE and during that time ≈ 3600 Å of Si will be etched. For deeper etching, a 3µm resist layer (Shipley 1400-16) would be applied. The slice was subjected to 1 hr and 45 minutes of RIE to etch down 3200Å towards the charge sheet (step 7 of Fig. 4.6), which brings the etch surface of the slice to within 1100Å of the charge sheet, as seen in the TEM (Fig. 4.1). Note that if the processing specifications were based

solely on the target heterostructure of Fig. 2.1, a much shallower etch would have been required. Without the benefit of the TEM results, the implant to follow could have been too shallow to make a low resistivity contact to the charge sheet.

In this fabrication procedure, a self-aligned technology is used. That is, the gate metal established in the first step serves to mask the slice for the formation of the gate mesa by RIE and is an implant mask for the source and drain contacts. A PR pattern is placed on the slice but it is used only to protect the two- and three-terminal DOES devices. The loss of the Al due to sputtering during RIE brings the metal layer from approximately 3000Å to 2000Å. This is illustrated in the micrograph of Fig. 4.7 and is detrimental to the performance of the device as it raises resistive losses along the length of the gate and reduces the masking ability of the metal.

After the formation of the gate mesa, the PR is stripped from the slice and a 1000Å film of Si₃N₄ was deposited. During deposition, the temperature of the slice was kept below 300°C. The film deposits conformally over the topology of the slice. Immediately after deposition, the slice is given an acid dip and subjected to 5 minutes of RIE to etch back the Si₃N₄ to the Si surface (step 8, 9 of Fig. 4.6). Because the Si₃N₄ film is conformal and the RIE highly directional (normal to the surface of the slice), the 1000 Å Si₃N₄ film remains on the walls of the mesa. The side-walls serve to mask the mesa during implantation. This may or may not be necessary. The initial etch of the gate mesa using RIE forms quite vertical mesa walls as shown in the micrograph of Fig. 4.8. However, because the implantation is carried out at 7° off normal incidence, it was deemed prudent to incorporate the side-walls into the procedure. After formation of the sidewalls a slope was discernible on the mesa (Fig. 4.9).

4.4.5 Implantation & Annealing

With the gate metal and Si_3N_4 side-walls defined, the next step in the fabrication process was to implant the slice to form a contact to the inversion charge. This contact forms the source or drain in the HFET and also forms the third-terminal for hole injection or extraction in the DOES. It is desirable that a low resistivity contact be made and thus a high dose and activation fraction are required. If, for example, the source contact has high resistivity then this is reflected in the extrinsic transconductance of the HFET [63]. One reason for using a self-aligned technology is to minimize the distance between the source and drain contacts and the gate mesa. Minimizing this distance reduces the area of channel which is not subject to the gate bias. Effectively, that portion of the channel which is not subject to the gate potential will have constant zero gate bias channel conduction properties.

This raises an interesting point in that depletion mode devices will intrinsically have better extrinsic transconductance properties than enhancement mode FETs because that portion of the channel not under the influence of the gate potential will have lower resistivity.

Following the formation of the Si_3N_4 side-walls, a pattern in $3\mu\text{m}$ PR was defined as an implant mask (step 10 of Fig. 4.6) over those areas where the gate metal was not present and no implantation was desired (Fig. 4.10). Establishing this PR pattern presented some difficulties.

The developing solution is based on the OH^- radical which also attacks Al. Thus, in areas where the PR is to be removed, exposing both the Si surface and Al, care must be taken to minimize developing time. To this end, the exposure time was increased to 1 minute and the developing time reduced to 5 sec.

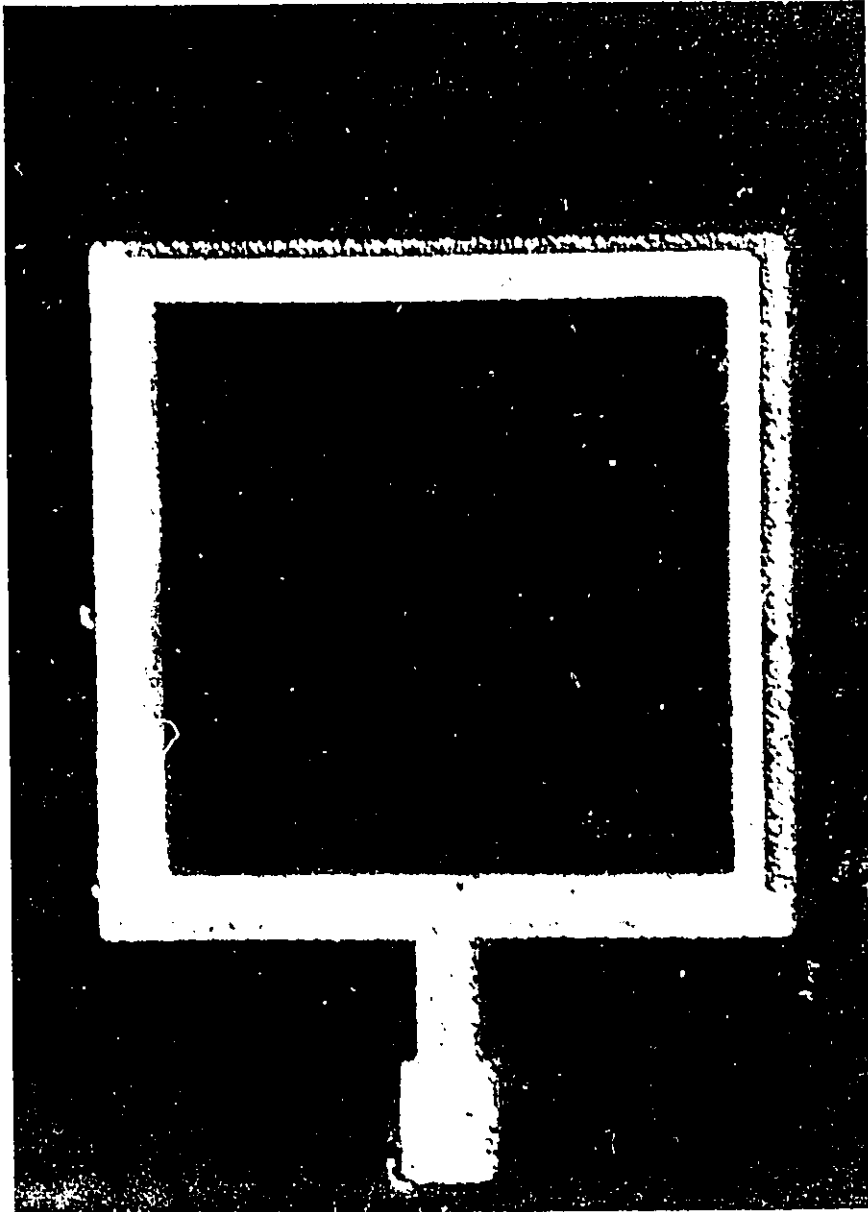


Figure 4.7: The optical micrograph of the metallization illustrating the effect of Al sputtering during RIE. The magnification factor is 1000.

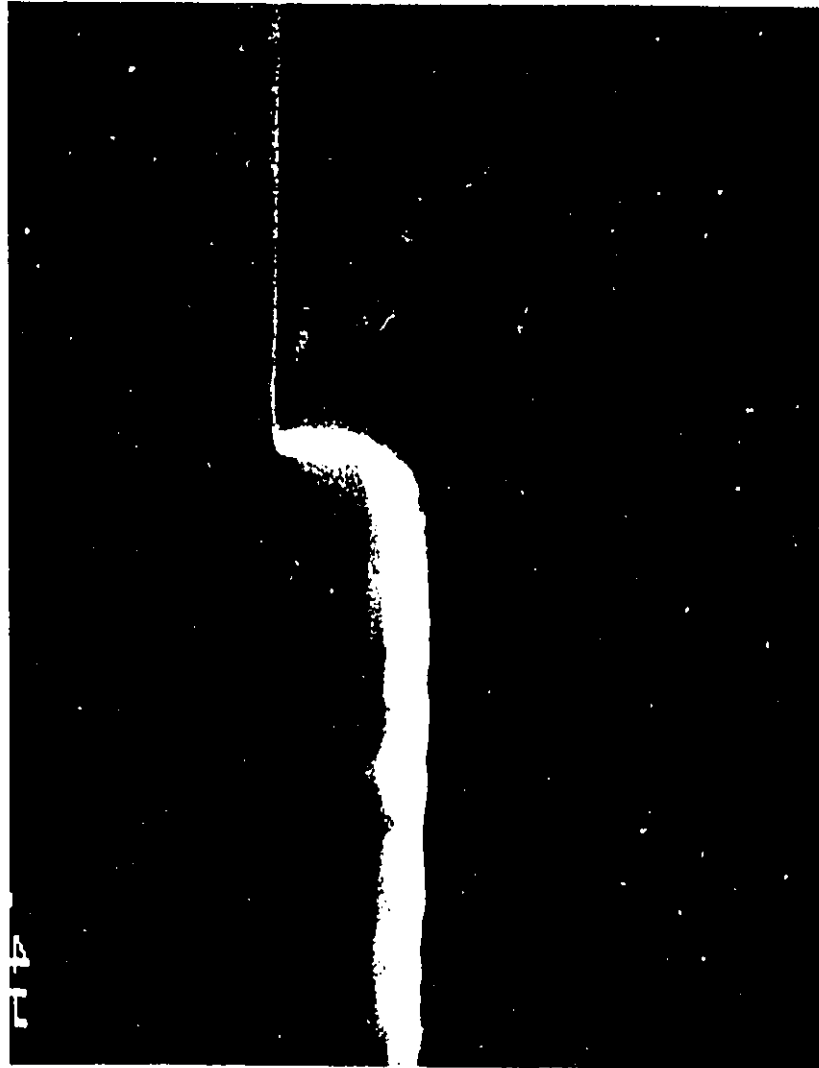


Figure 4.8: The scanning electron micrograph (SEM) of the mesa illustrating the vertical nature of the side walls. The magnification factor is 25000.

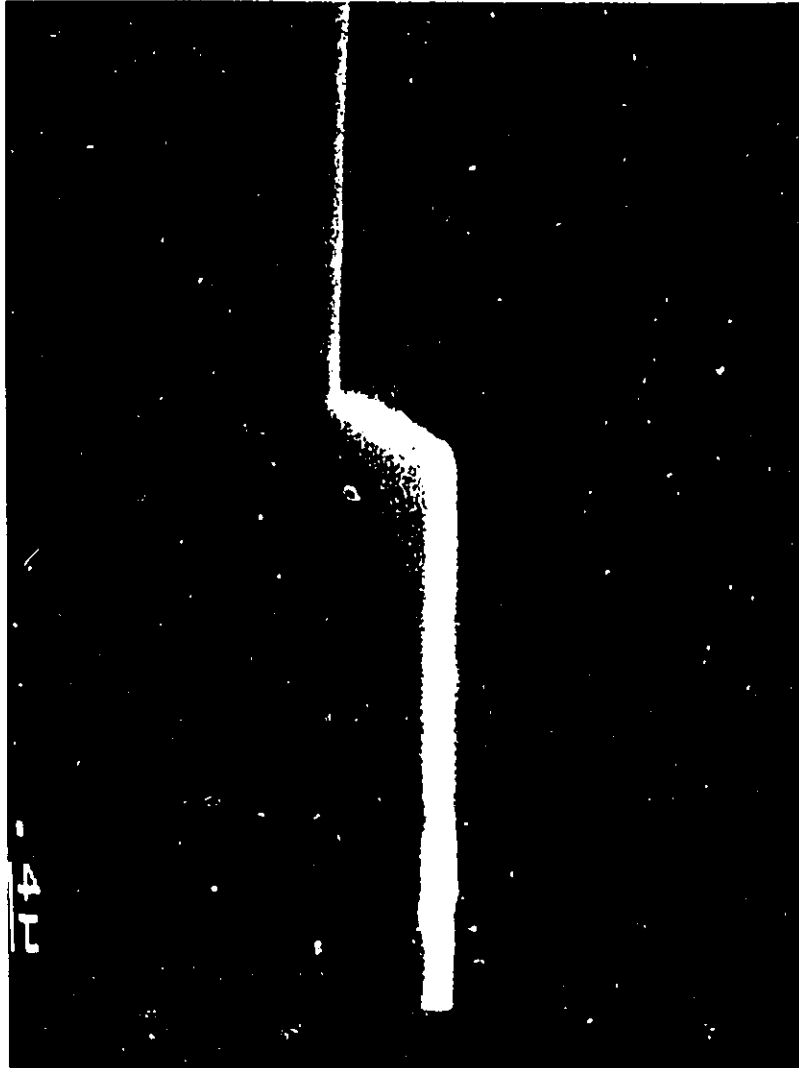


Figure 4.9: The scanning electron micrograph (SEM) of the mesa after formation of the Si₃N₄ side-walls. The magnification factor is 25000.

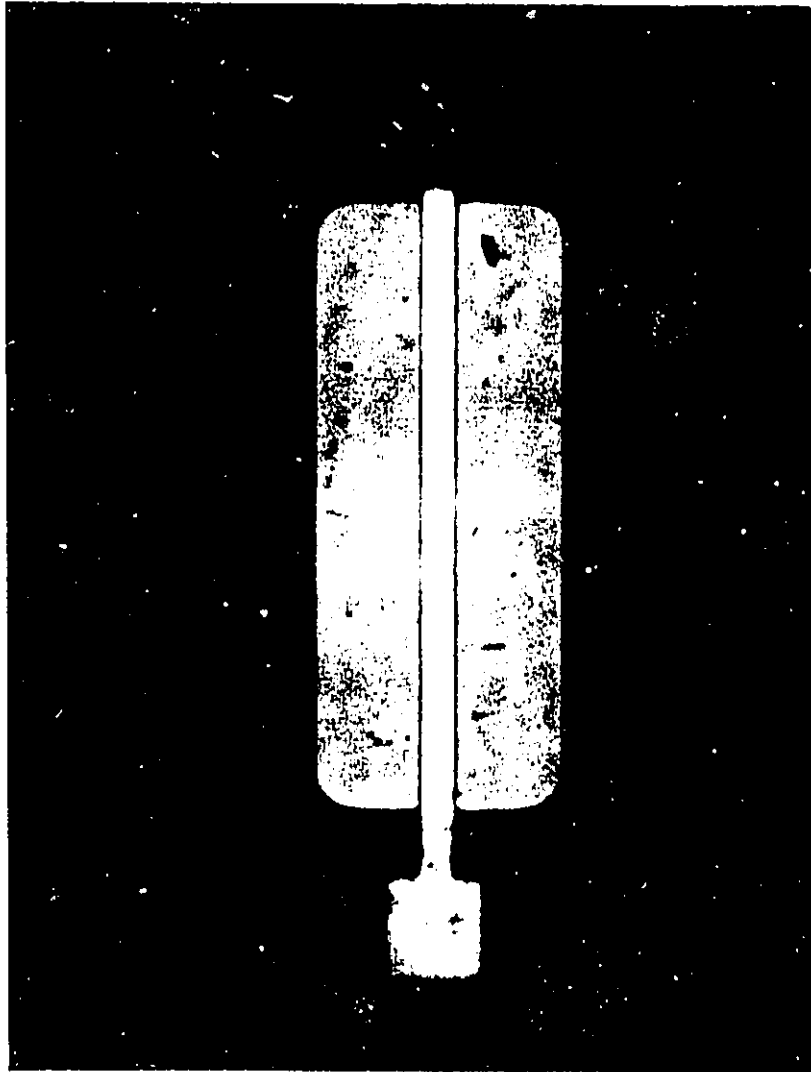


Figure 4.10: The optical micrograph of the gate metal for the HFET with source and drain implant area defined with $3\mu\text{m}$ PR. The magnification factor is 1000.

This variation is detrimental to mask transfer resolution however only gross feature were required at this stage in the fabrication.

A boron implant was carried out at McMaster University that had dose $2 \times 10^{13} \text{ cm}^{-2}$ at an energy of 20keV (step 11 in Fig. 4.6). The implant ion was derived from an elemental source. The predicted dopant distribution profile is seen in Fig. 4.11 and is obtained using;

$$N(x) = \frac{\text{Dose}}{\sqrt{2\pi} \Delta R_p} \exp \left[-\frac{1}{2} \left(\frac{x - R_p}{\Delta R_p} \right)^2 \right], \quad [4.1]$$

where ΔR_p is the projected longitudinal straggle and R_p is the projected range. For 20 keV boron in silicon, $R_p = 730 \text{ \AA}$ and $\Delta R_p = 341 \text{ \AA}$, into aluminum, $R_p = 714 \text{ \AA}$ and $\Delta R_p = 350 \text{ \AA}$.

Thus, with the charge sheet approximately 1100 \AA below the surface of the Si, the implanted ion concentration at the inversion-channel will be approximately $2 \times 10^{18} \text{ B/cm}^3$ and at the surface will be $1.5 \times 10^{18} \text{ B/cm}^3$.

Following the implant, the PR was stripped and the slice descumed and cleaned. Annealing of the implant damage and activation of the dopant was performed using RTA. However, the anneal was performed later in the fabrication process. After the second mesa had been formed (steps 13-15 in Fig. 4.6) and the source and drain metal contacts were patterned using (steps 16, 17 in Fig. 4.6). Here, Al was used and a film 3700 \AA thick was deposited for the source and drain metal as well as the third terminal of the DOES. The metal was annealed for 5 minutes at 500°C . At this temperature approximately 25% dopant activation is expected and diffusion is minimal [71].

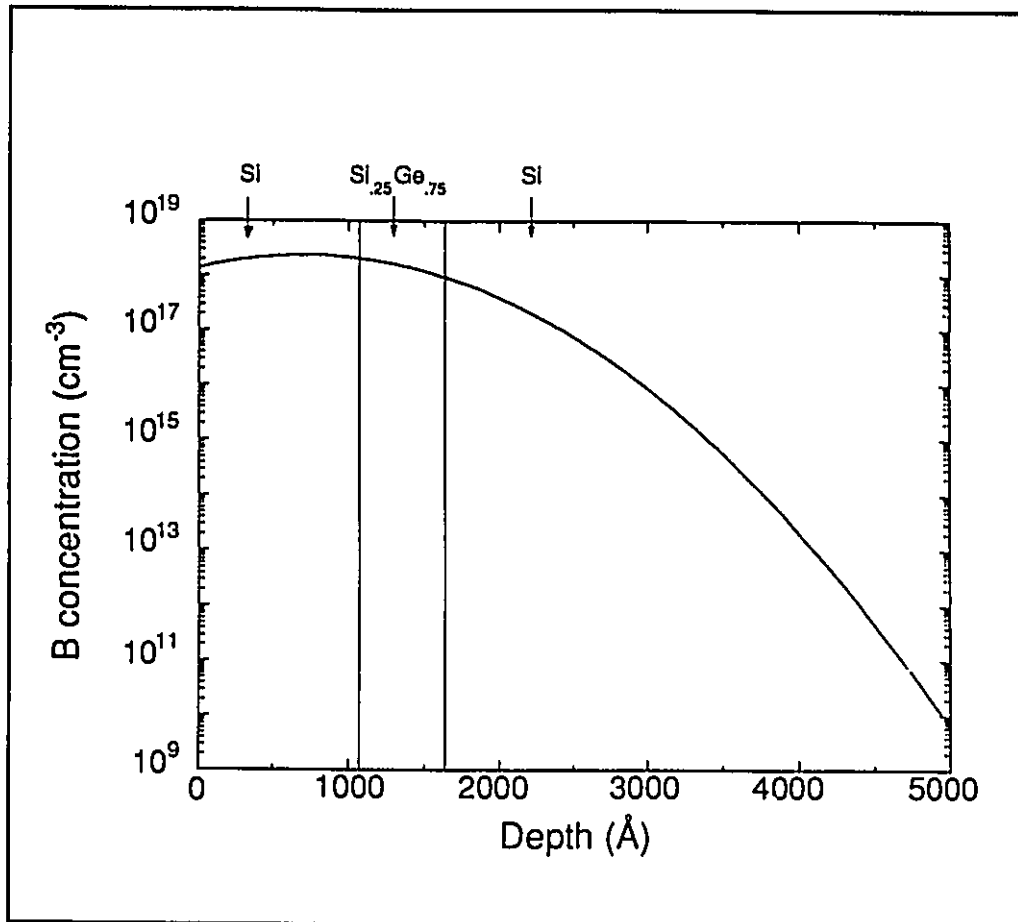


Figure 4.11: The predicted implant profile for boron at 20keV and dose $2 \times 10^{13}/\text{cm}^2$.

4.4.6 Si₃N₄ Vias

The final steps in the fabrication process involve applying a thick film of Si₃N₄ (7200Å) to protect and passivate the surface and also create a platform onto which the final bonding pad metal can be formed. A thicker film will reduce the parasitic capacitance of the parallel plates formed by the bonding pads and the underlying Si. However, a trade-off between device yield and performance must be considered. A thicker film of Si₃N₄ will result in deep vias to the source and

drain metal. The difficulty in obtaining a continuous contact between the source and drain metal and the bonding pad metal increases quickly with deep vias. Vias to the gate, source, drain, and substrate through the nitride film are formed by patterning PR using mask 8 and using RIE to etch to the metal level. After etching, the PR is stripped and the slice prepared for the lift-off technique. In the same manner as described in section 4.4.2, PR is applied and patterned. Aluminum is deposited (4000\AA) and partially fills the vias with metal to form a continuous contact. The finished HFET and three-terminal DOES are shown in figures 4.12 and 4.13, respectively.

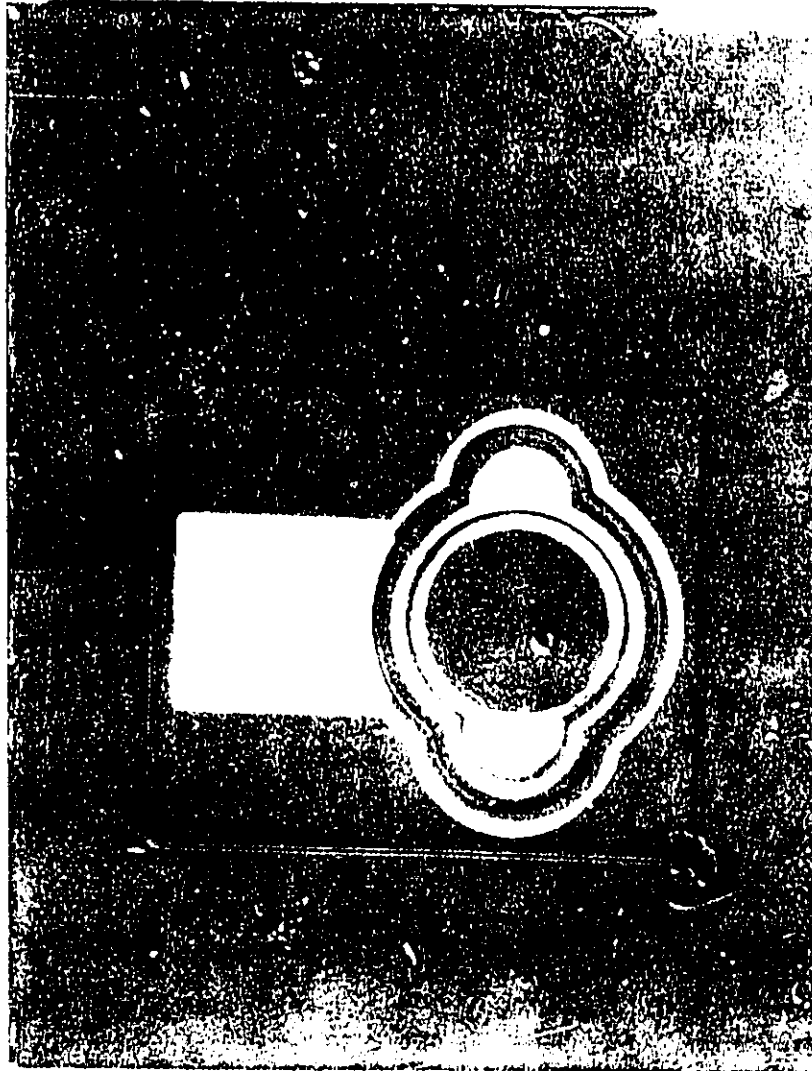


Figure 4.12: The optical micrograph of a double-mesa three-terminal DOES. The magnification factor is 206.

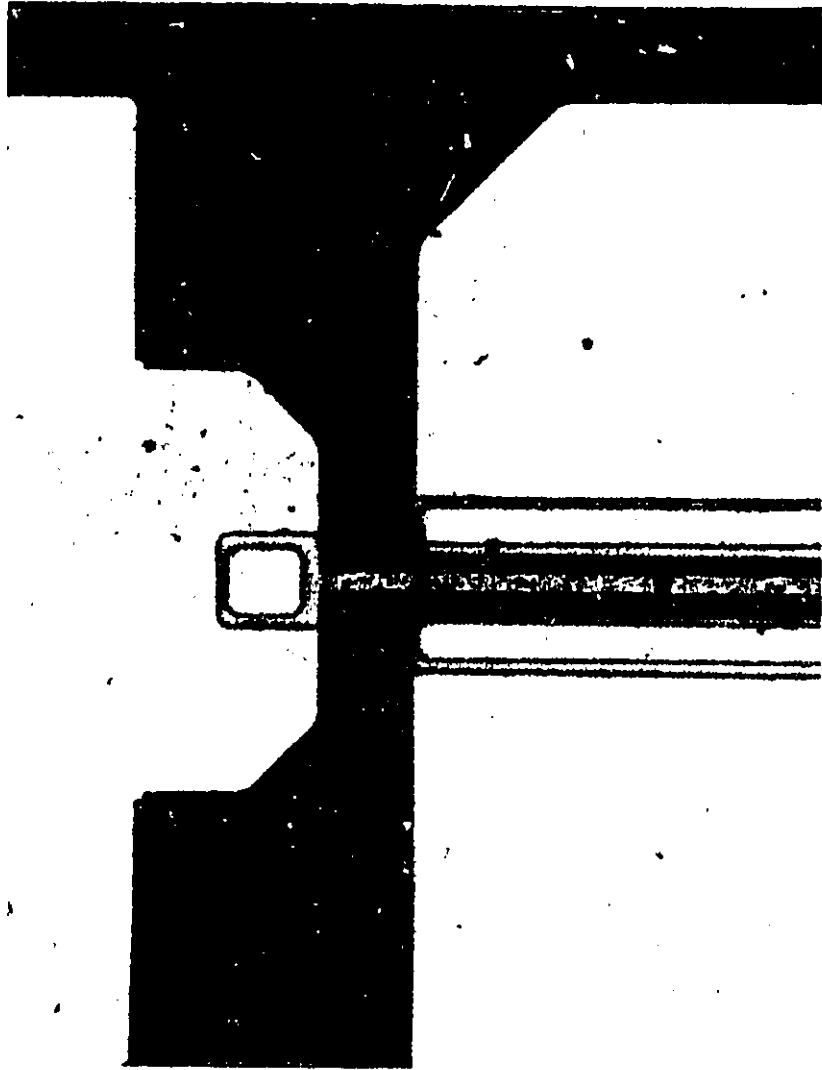


Figure 4.13: The optical micrograph of a self-aligned HFET. The magnification factor is 1044.

CHAPTER 5

TWO-TERMINAL DOES: EXPERIMENTAL RESULTS & DISCUSSION

This chapter of the thesis presents the experimental characterization of the two-terminal Si/Si_{0.75}Ge_{0.25}-based DOES. Some experimental detail on the measurement procedure and set-up is also given. Although most of the results presented in this thesis are time independent, this chapter includes a section on oscillatory behavior and instabilities within the DOES which are pertinent not only to the Si/SiGe materials system but to the DOES in general. Wherever possible, the experimental observation presented here are related to the theory of operation outlined in chapter 2.0.

As was stated in chapter 4, three batches of devices were fabricated and characterized. No attempt is made to explain any differences in the device characteristics based on processing variations. In some cases, such a comparison may appear warranted but invariantly other issues and factors are involved. However, for completeness, the batch number is stated with each experimental result. Also lacking in these results is any statistical data on the measured operational characteristics of the devices. The yield from batch D1 was five devices (100%), from batch D2, three devices ($\approx 70\%$), and from D3 over 30 devices ($\approx 80\%$). In view of the fact that the results represented here are the first experimental realization of the Si/SiGe-based DOES, no statements concerning reproducibility from device to device was warranted at this stage of technology development.

5.1 Experimental Procedure

The experimental set-up used for the bulk of the measurements reported in the thesis is seen in Fig. 5.1. To perform low temperature measurements, diced chips were wire bonded in a flat 20 pin metal package. Within the package, devices were fixed with a polymer glue to a ceramic flat in order to isolate electrically the device from the package. For low temperature measurements the package was then mounted directly onto the cold finger of a closed-cycle helium refrigerator. Embedded in the cold finger was a resistive heater which allowed thermal stabilization to a set-point temperature. Electrical measurements were performed using a Hewlett-Packard 4145B Semiconductor Parameter Analyzer which is composed of four independent current/voltage sourcing and measuring units (SMU). The data acquired using the HP4145B was then transferred via an interface bus (IEEE 488) to a computer. Devices could be illuminated while on the cold head via a quartz window. Any optical emission from the DOES was collimated, passed through an optical chopper, and refocused on to a InGaAs p-i-n photodetector.

For ac measurements, individual wire-bonded devices were mounted directly onto the center conductor of an 18 GHz SMA connector. The closed loop made by the testing circuit was made as small as possible. For example, the bonding wire leads were trimmed to less than 1mm to minimize inductance.

5.2 Current-Voltage Characteristics

In this section, the dc electrical characteristics of the two-terminal Si/Si_{0.75}Ge_{0.25}-based DOES (Batches D1 & D2) are presented. In addition, the effect of illumination and temperature on those characteristics is reported and discussed.

5.2.1 Dark I-V Characteristics

The typical current-voltage (I-V) switching characteristic of the two-terminal Si/Si_{0.75}Ge_{0.25}-based DOES (Batch D1) is seen in Fig. 5.2. This measurement was performed on a round device with diameter 100 μ m. The interesting feature of the device is that it exhibits electrical bistability: the electrical characteristics exhibit a high-impedance OFF-state and a low-impedance ON-state, separated by a region of negative differential resistance (NDR). A switching voltage V_S and its associated current I_S define the limits of the high-impedance state, which are seen to be 2.6V and 500 μ A, respectively, and the off-state impedance is typically 40 Ω . The onset of the low-impedance state is characterized by a holding voltage V_H and an associated current I_H , which are typically 1.3V and 1.0mA respectively. A negative bias applied to the substrate produces typical reverse-bias characteristics of a p-n heterojunction.

5.2.2 Effect of Illumination

The I-V characteristics of the device are shown as a function of increasing incident illumination intensity in Fig. 5.3. A Helium-Neon laser at 632.8 nm provided a collimated beam which was focused onto the device. Neutral density

filters of varying optical density were used to step down the illumination intensity. The reverse current generated for each illumination intensity at -1V applied to the substrate was recorded and used as an intensity

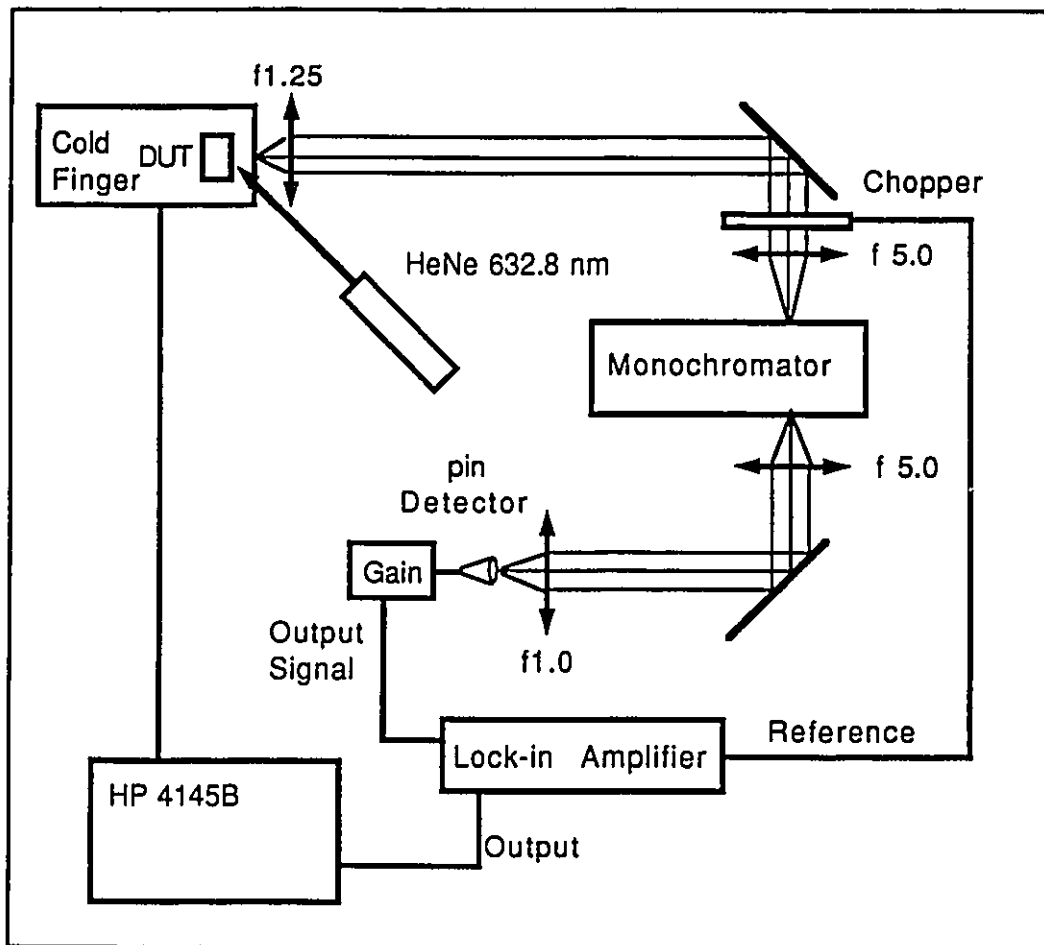


Figure 5.1: A schematic representation of the experimental set-up used to electrically characterize the devices under low temperature and/or illumination conditions. DUT refers to the device under test.

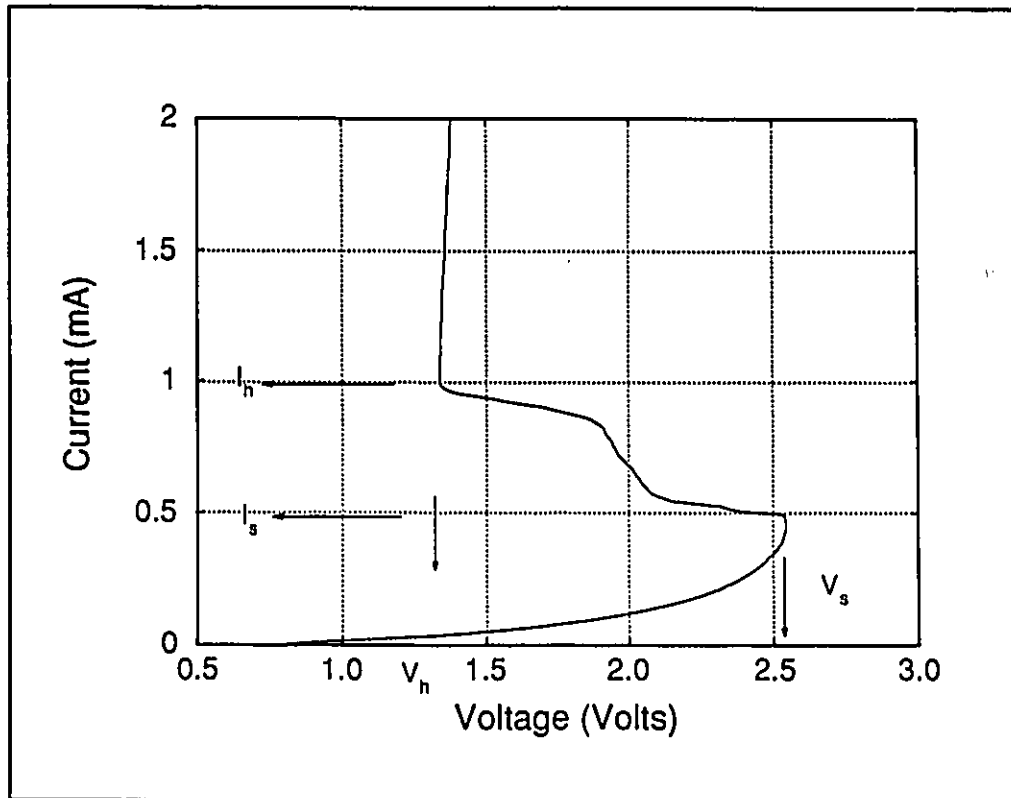


Figure 5.2: The dark current-voltage (I-V) characteristic of the two-terminal Si/Si_{0.75}Ge_{0.25}-based DOES (Batch D1). Labeled are the switching voltage, V_s , the switching current, I_s , the holding current, I_h , and the holding voltage, V_h .

parameter in Fig. 5.3. It is estimated that the 'full power' illumination intensity in Fig. 5.3 was approximately 500 μ W. From Fig. 5.3 it is observed that with increasing illumination V_s and I_s slightly decrease, while I_h decreases and V_h remains almost unchanged. With no light on the device, the switching voltage, V_s , and switching current, I_s , are 2.6V and 500 μ A respectively, and the holding voltage, V_h , and holding current, I_h , are 1.3V and 1.0mA respectively. With full power illuminating the device, the reverse-biased photo-current measured was

255 μ A compared with 128 μ A at 50% optical power, and only 4nA with no illumination.

When excess carriers are generated in the depletion region of the active region, such as by optical absorption, the internal gain increases. This results in the device entering the NDR mode at a lower switching voltage, V_s , than without the presence of light. The red HeNe is not an optimal source for optical injection into the DOES. At wavelength 632.8nm, the absorption depth is approximately 2 μ m. Therefore, only a small fraction of the light is absorbed in the depletion regions of the DOES.

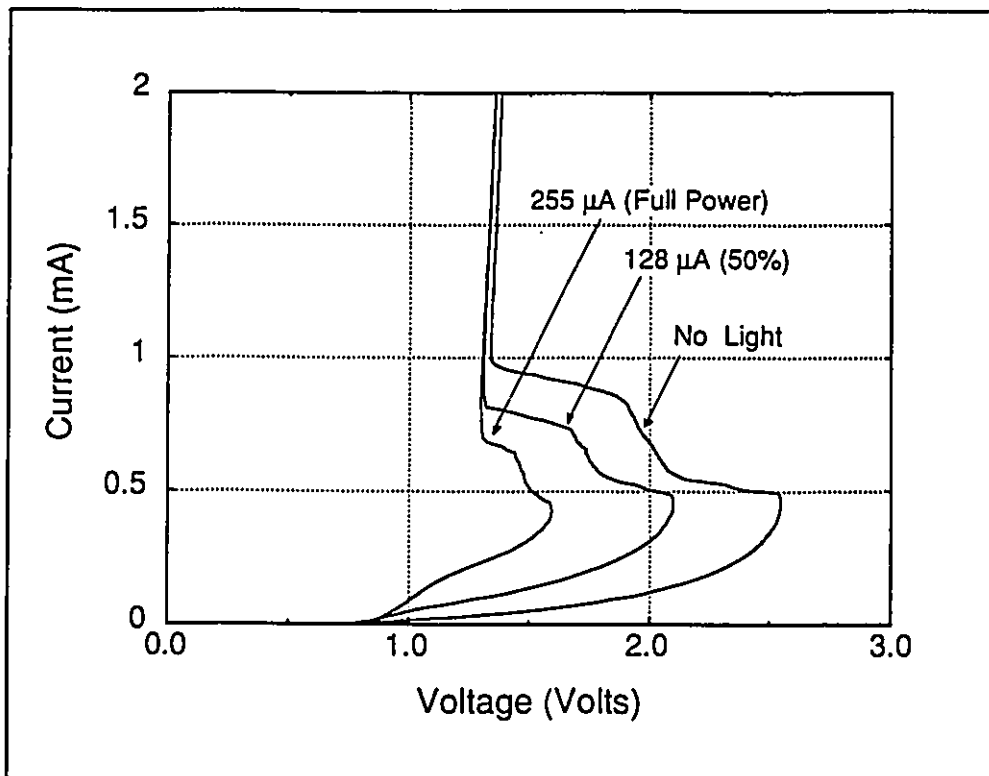


Figure 5.3: The I-V characteristics of the two-terminal Si/Si_{0.75}Ge_{0.25}-based DOES (Batch D1) with optical input as a parametric variable.

5.2.3 Effect of Temperature

From section 2.5, or more directly, from eqn. A1, increasing the temperature of the device increases the rate of generation of carriers in the depletion region and also increases the flow of carriers over the barrier. The net effect of this process is to increase the small signal gain, and reduce V_S . This is seen in Fig. 5.4 and 5.5 which illustrates the I-V characteristics of the device with temperature as a parameter. The labeled temperatures are those of the cold finger, but some self-heating of the device is suspected, which would put the actual device temperature at a few degrees above the recorded value. In Fig. 5.4, with decreasing temperature, V_S is seen to increase from $\approx 2.6\text{V}$ to 3.5V over the temperature range from 300K to 200K . The switching current appears to decrease over the same range of temperature. No statement concerning the behavior of the holding current can be made due to instabilities in the device, which are discussed in section 5.3. At 200K the I-V characteristics in the regime of NDR has expanded to encompass a wide range of currents.

In contrast to the optical sensitivity, changes in the I-V characteristics with decreasing temperature can be explained as due to the suppression of carrier generation in the active region and the suppression of carrier flow over the barrier. This is most evident in Fig. 5.5 in which illustrates the logarithm of the current versus voltage ($\log(I)$ -V) characteristic of a $100\mu\text{m}$ diameter $\text{Si}/\text{Si}_{0.75}\text{Ge}_{0.25}$ -based DOES from batch D2. With decreasing temperature, the current before switching decreases as the switching voltage increases. Based on the numerical simulations (section 2.6), this current is predominately generation current in the depleted part of the active region.

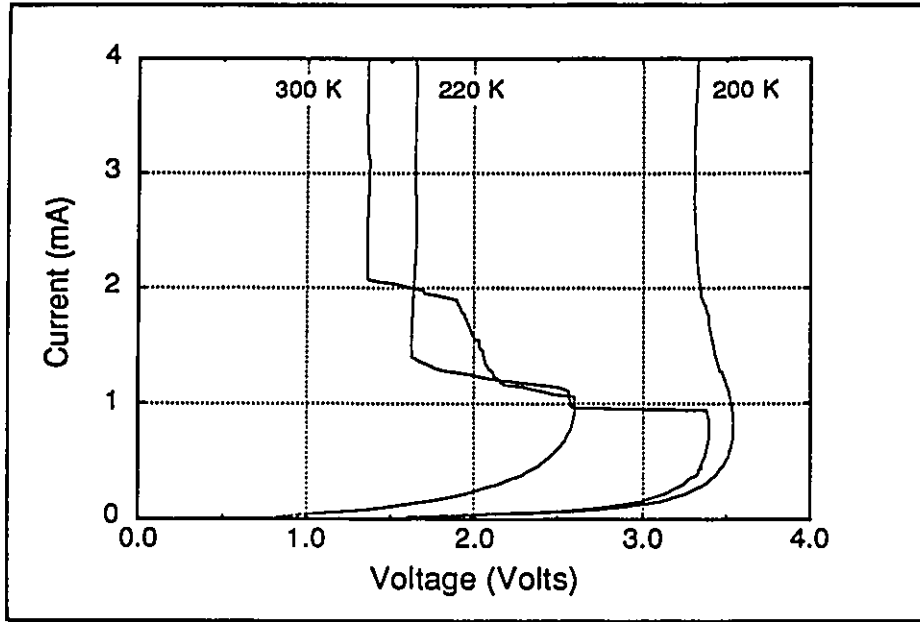


Figure 5.4: The I-V characteristic of the two-terminal Si/Si_{0.75}Ge_{0.25}-based DOES (Batch D1) with temperature as a parametric variable.

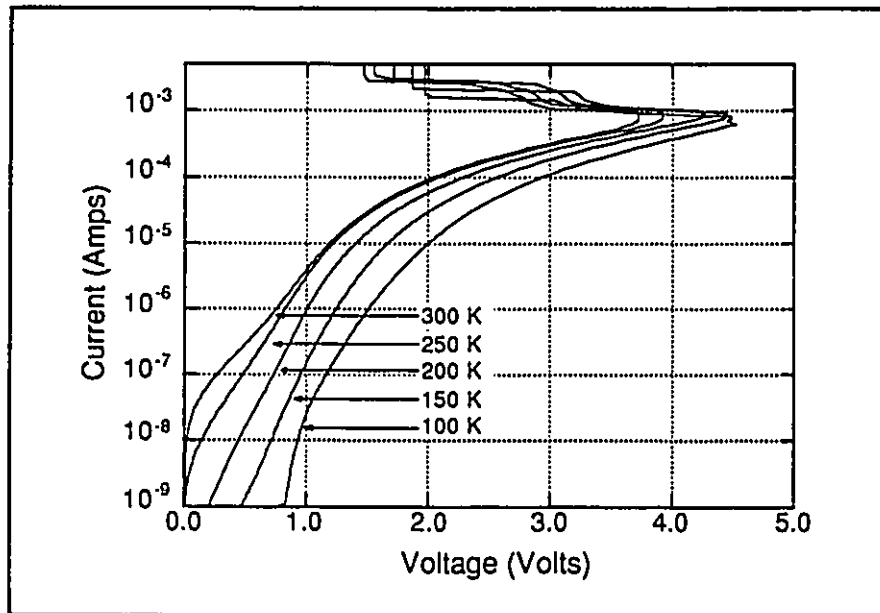


Figure 5.5: The logarithm of current versus voltage (log(I)-V) characteristic of the two-terminal Si/Si_{0.75}Ge_{0.25}-based DOES (Batch D2) with temperature as a parametric variable.

5.3 Oscillations in the DOES

It is well known that electronic devices exhibiting negative differential resistance are difficult to characterize. Temporal instabilities which manifest as hysteresis in the dc I-V characteristics and/or instrumentation oscillations are typical features of the NDR regime [72]. These instabilities have been observed in the DOES.

Electrical oscillations in devices demonstrating N-type or S-type negative differential resistance are the subject of some controversy in the literature pertaining to resonant tunneling diodes [73]. Liu [74] has reported a simple treatment of the behavior of N-type NDR devices in RLC circuits, and has been able to simulate oscillatory behavior and plateau-like dc I-V characteristics in the NDR region. Plateau-like dc I-V characteristics have also been observed in the GaAs/AlGaAs-based DOES [18], and some attempt has been made to explain these characteristics based on avalanching [75]. Avalanching has also been suggested as a mechanism for enhanced optical emission in AlGaAs/GaAs-based triangular barrier opto-electronic switches biased in the regime of NDR [76].

This section describes the electrical oscillations in the DOES when operated in the NDR regime. These oscillations have temporal characteristics which are determined by the resistance, inductance, and capacitance of the measurement circuit and of the device itself. In this section, it is proposed that the fine structure that is observed in the NDR region of the dc I-V and enhanced L-I characteristics is a direct result of these oscillations.

5.3.1 Oscillatory Behavior

Figure 5.6 illustrates the lumped element test circuit which can be used to explain oscillatory behavior in the DOES. Voltage oscillations across the capacitor were observed using a 125MHz digital oscilloscope.

As the constant current to the device is incremented beyond the switching current, I_S , the device enters the NDR region and begins to oscillate, with the peak-to-peak voltage oscillation extending slightly beyond the ON-state ($\approx 2.1V$) and the OFF-state ($\approx 5.5V$) as shown in Fig. 5.7. The maximum frequency of these oscillations is determined using a circuit configuration where no external capacitance is added.

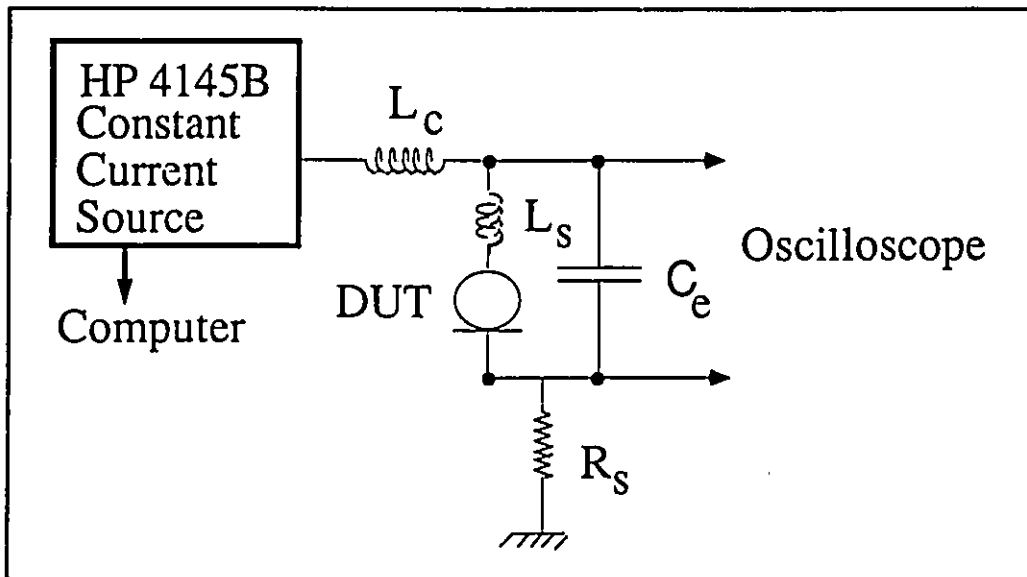


Figure 5.6: A schematic of the lumped circuit which is used to explain oscillations in the regime of negative differential resistance in the DOES. A RF choke inductor, L_c , is used to further stabilize the constant current source. In parallel with the device under test (DUT) and any parasitic inductance, L_s , is placed a external capacitor, C_e . A series resistance, R_s , is also placed in the circuit but has no bearing on the oscillations observed.

Transitions to the ON-state have been observed with a time constant of less than 100ns, indicating an intrinsic parasitic capacitance on the order of 10nF, if we assume an ON-state impedance of $\approx 10\Omega$. The net parasitic capacitance depends on the internal bias condition of the p-n junctions, as these capacitances dominate both the bonding pad and mount capacitance.

When C_e is chosen to be much larger than the intrinsic device capacitance, the waveform of the voltage oscillations is saw-tooth in shape (Fig. 5.8). The ON-to-OFF voltage transition is linear in time, as one would expect charging a capacitor with approximately constant charging current. However, with no external capacitor, the transition has structure indicative of an internal device capacitance which *changes* as the device charges up (Fig. 5.7).

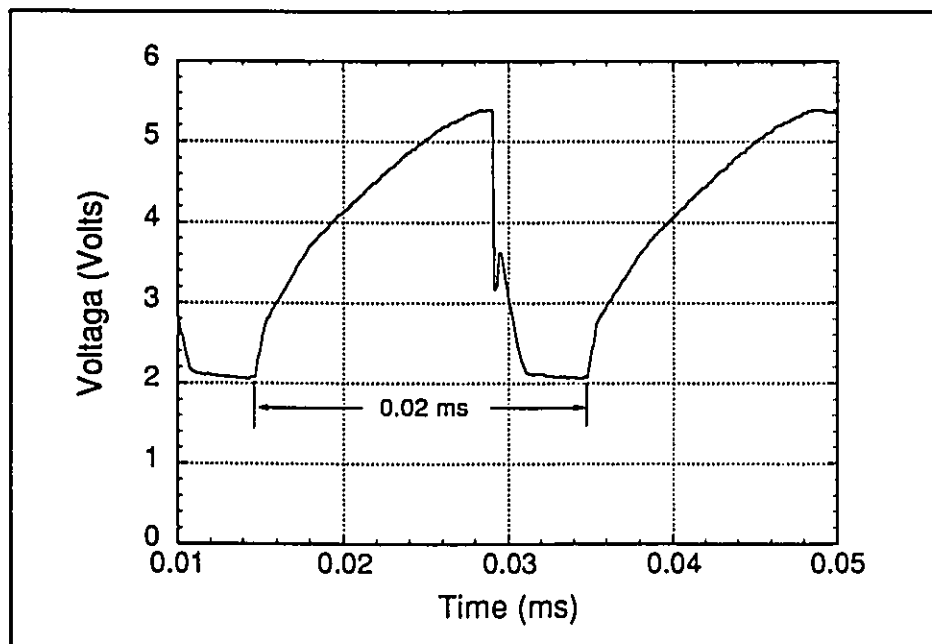


Figure 5.7: The oscilloscope trace of the voltage across the two-terminal DOES (Batch D3), a series inductance, L_s , and with no external capacitor added to the circuit. A constant current of 1.4mA was supplied to the DOES.

If the voltage oscillation is not a saw-tooth waveform, the measured dc voltage becomes a function of the drive current. For the measurement circuit (Fig. 5.6) with an external capacitor, C_e , of 22nF placed in parallel with the device, the voltage transition to the ON-state is made with a time constant of approximately 5 μ s while the transition to the OFF-state is more gradual ($\tau_{RC} \approx 100\mu$ s) as seen in Fig. 5.8. The frequency and duty cycle of these oscillations scale linearly with drive current. Driving a larger constant current into the test circuit induces oscillations with greater frequency as seen by comparing the trace with $I_d=1.4$ mA and 2.0mA in Fig. 5.8.

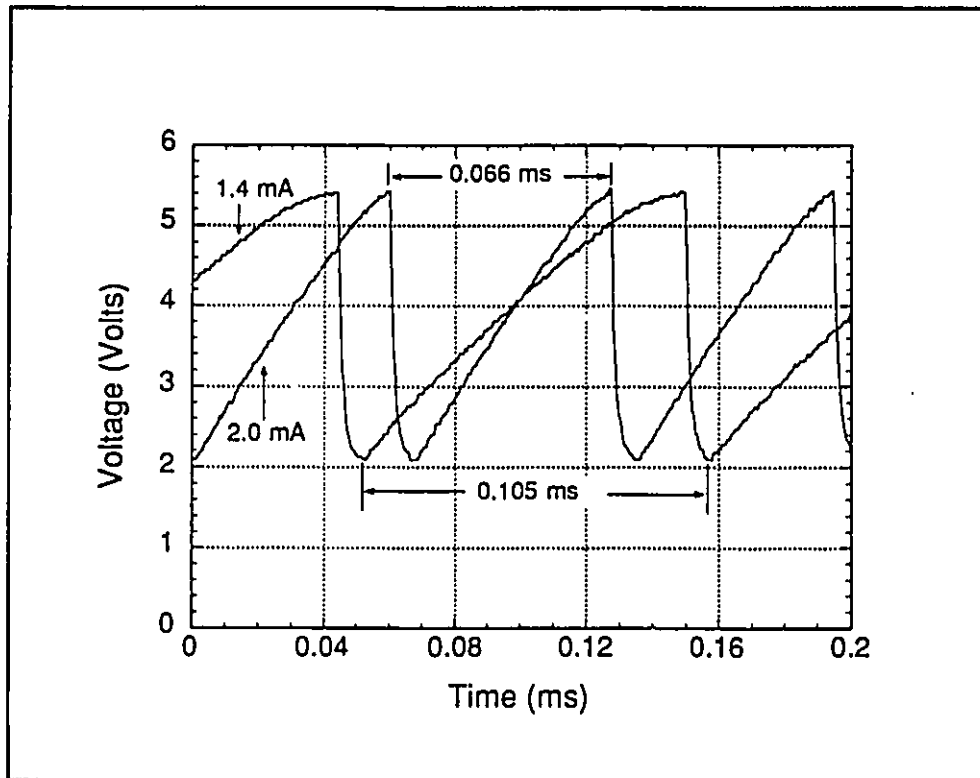


Figure 5.8: The oscilloscope trace of the voltage across the external capacitor (22nF) placed in parallel with the two-terminal Si/Si_{0.75}Ge_{0.25}-based DOES (Batch D3) with drive current 1.4 and 2.0 mA.

5.3.2 Effect of the Oscillations on dc I-V and L-I Characteristics

Over the same range of I-V operating points that the oscillations occur, plateau-like structure in the NDR portion of the dc I-V characteristic is observed. The dc voltage value measured in the NDR region must be a time-average over the oscillation cycle. In Fig. 5.9, the measured dc I-V of a device is shown with and without an external capacitor. A step-like shape in the NDR region is apparent in both cases but the sharpness of the step increases with increasing external capacitance. In addition, we have observed that at larger circuit capacitance values, I_h increases and hysteresis is introduced into the dc I-V characteristics.

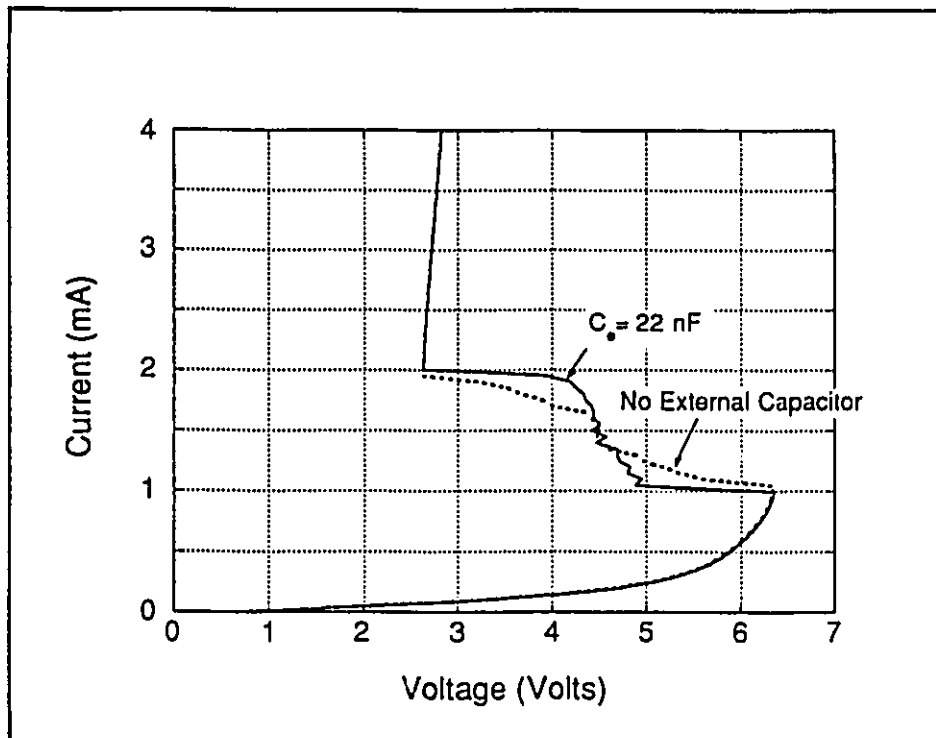


Figure 5.9: The measured I-V characteristic of the DOES with and without a 22nF external capacitor in the test circuit.

Inherently associated with the voltage oscillations in the DOES will be a variation in current through the device. It is these current pulsations which result in an apparent enhancement of the dc optical output versus current (L-I) characteristic when the device is operating in the NDR regime. Over precisely the same current range that oscillatory behavior is observed in the DOES, the dc L-I characteristic will have increased efficiency of optical emission (Fig. 5.10). Consistent with the earlier observations that with decreasing temperature the switching current decreases, so does the current at which the optical enhancement commences. That is, the correlation between electrical oscillations and optical enhancement is invariant with temperature.

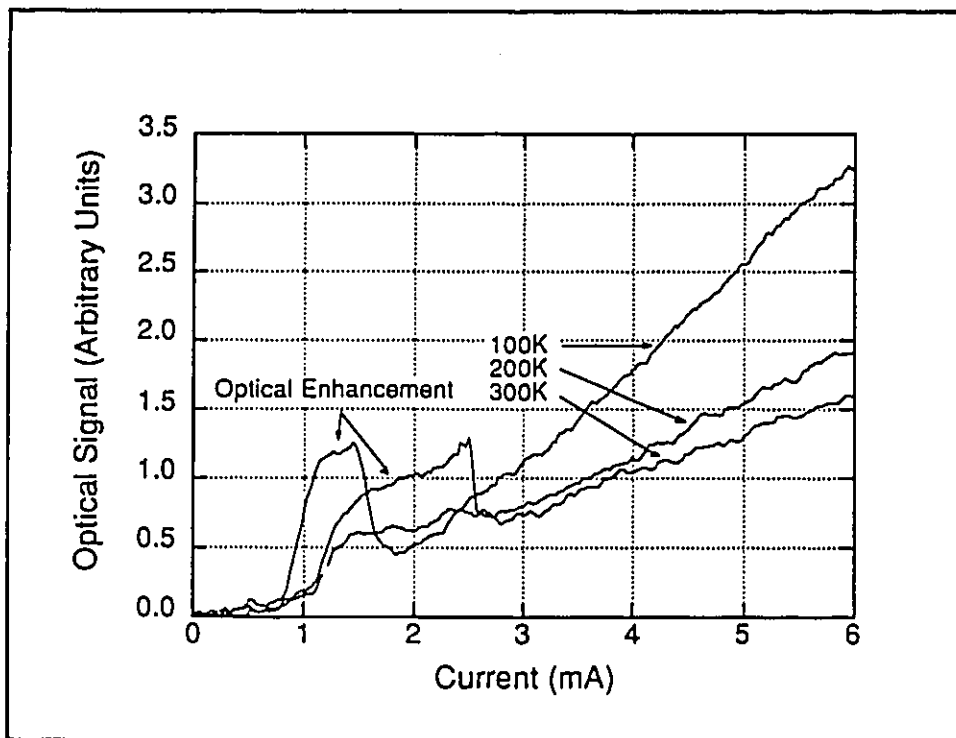


Figure 5.10: The measured light output versus current (L-I) characteristic of the two-terminal DOES with temperature as a parametric variable. In some current ranges, an enhancement in the dc luminosity is observed.

Another effect of the oscillations in the regime of NDR is hysteresis in the I-V characteristics. Depending on the direction of the current sweep performed for the measurement, an I-V characteristic with differing limits for the regime of NDR is observed (Fig. 5.11). In most experimental measurements, the hysteresis is observed in the final plateau of the I-V characteristic before the holding point (V_h , I_h). Again, for this measurement, oscillations are seen whenever the operating point of the device is within the region of extrinsic NDR.

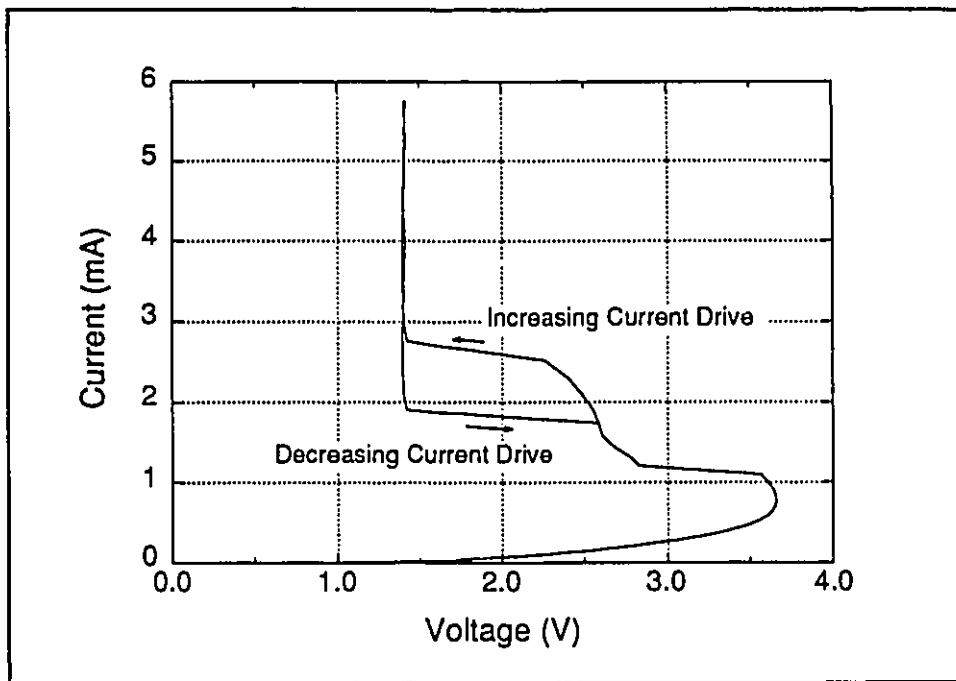


Figure 5.11: The measured dc I-V characteristic for a current sweep from zero to approximately 6 mA and a sweep in the opposite direction.

5.3.3 Effect of Parasitic Circuit Elements

Although a simple relationship between the shape of the dc I-V characteristic in the NDR region and the circuit parameters is not apparent, Liu [74] has

demonstrated similar plateau-like structure in a simple simulation of N-type NDR device behavior and was able to simulate an expansion or contraction of the NDR region by changing the external capacitance attached in parallel with a resonant tunneling diode. The observations presented in this thesis are consistent with Liu's results.

The oscillations described in section 5.3.2 can be modeled by driving a current, I_d , to the circuit illustrated in Fig. 5.6 and assuming an intrinsic S-type I-V characteristic for the device. The differential equation governing the voltage observed across C_e is given by

$$\frac{d^2V_O}{dt^2} + \frac{R_n}{L_s} \frac{dV_O}{dt} + \frac{1}{L_s C_e} V_O = \frac{R_n I_d + R_n I_{n-1} + V_{n-1}}{L_s C_e} \quad (5.1)$$

where R_n is the device resistance at the operating point; I_n and V_n are the current and voltage, respectively, at that operating point; and L_s and C_e are the inductance and capacitance, respectively, prescribed in the circuit. The right-hand side of eqn. (5.1) is a constant for a particular drive current and operating point on the intrinsic I-V characteristic supplied to the simulation. Solving equation 5.1 numerically in a computer-based model, plateau-like dc I-V characteristics in the region of NDR are simulated and shown in Fig. 5.12. Each point on dashed line in Fig. 5.12 is the average voltage and current (over 10 cycles) obtained for the particular constant drive current and the intrinsic I-V curve supplied to the model. The average current must be precisely the constant current supplied. However, the average voltage will depend on the locus of operating points taken during one oscillation cycle. For a constant current in the vicinity of the NDR, the modeled device enters stable, self-sustained voltage and current oscillations (for example,

$I_d=1.65\text{mA}$ in Fig. 5.12). The solution method requires that an initial operating point must be supplied to the computer-based model and this initial point will to a large extent determine if oscillations will arise in the DOES. For initial operation points below the switching point (V_s, I_s), the transition to a constant drive current greater than I_s will necessitate that the circuit experience negative resistance for a short time. It is this experience which causes the modeled circuit to oscillate. Thus, even if a constant drive current is specified which is beyond the intrinsic regime of negative differential resistance (NDR) oscillations are possible as they initiate the moment the circuit experiences NDR. However, if the initial operating point is above the regime of NDR and a constant current is specified which is not within the intrinsic regime of NDR then no oscillations are predicted since the circuit never experiences NDR. This 'memory' effect observed in the model may be the basis of hysteresis in the measured dc I-V characteristics. The onset of oscillations at a specific drive current may be determined by the last operating point of the DOES.

For drive currents below the switching current or much beyond, the oscillation may commence but decays to a stable operating point (for example, $I_d=4.0\text{mA}$ in Fig. 5.13).

Oscillations that arise in the DOES can be explained by following the current and voltage changes across the RLC elements of the circuit. The resistance, R , must be taken as the instantaneous resistance of the device. When the constant drive current becomes larger than the DOES switching current, I_s , the voltage across the device falls from the switching voltage, V_s , to the holding voltage, V_h . At this point, the capacitive element in the circuit must discharge to V_h through the device (segment AC on Fig. 5.12). Simultaneously, the current

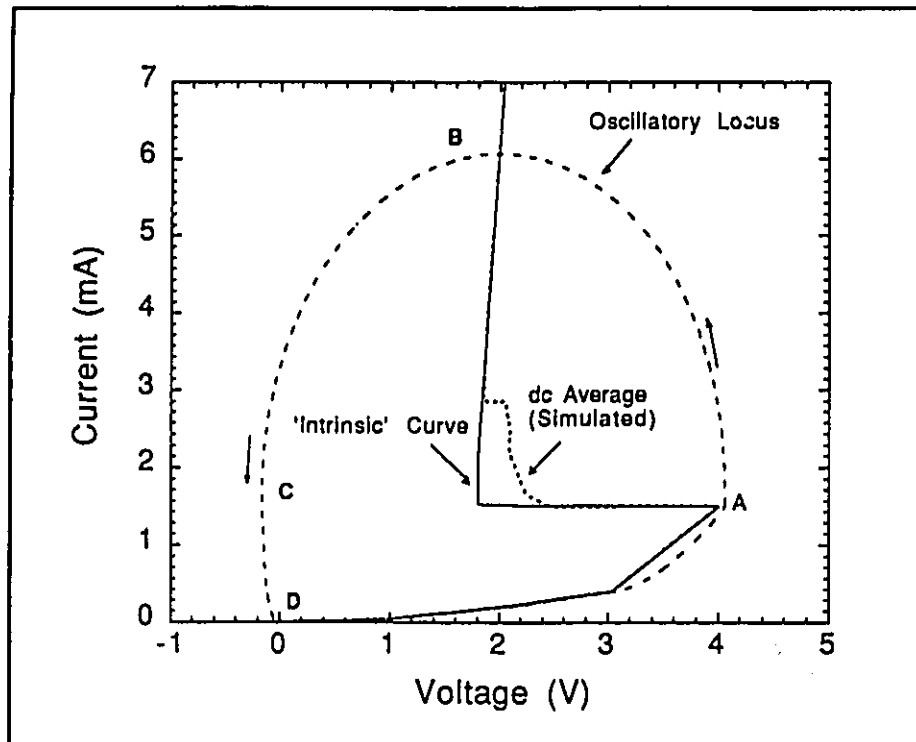


Figure 5.12: The calculated dc average of voltage and current oscillations simulated in a numerical model. Also seen is the simplified intrinsic I-V characteristic used as an input to the model. Superimposed on the I-V characteristics is the calculated locus of operating points during one oscillatory cycle as the device is driven at an operating point in the vicinity of the regime of negative differential resistance (1.65 mA). Chosen values for C_c and L_s were 22nF and 5mH respectively.

supplied by the capacitor does not rise instantaneously, but rather is impeded by the inductive element in series with the DOES. Similarly, as the current from the capacitor falls, the inductor attempts to maintain a fixed current and, as a result, the voltage across the capacitor undershoots the DOES holding voltage (segment BC on Fig. 5.12). This causes the current to be diverted from the DOES through the capacitor, which momentarily reduces the amount of current being supplied to

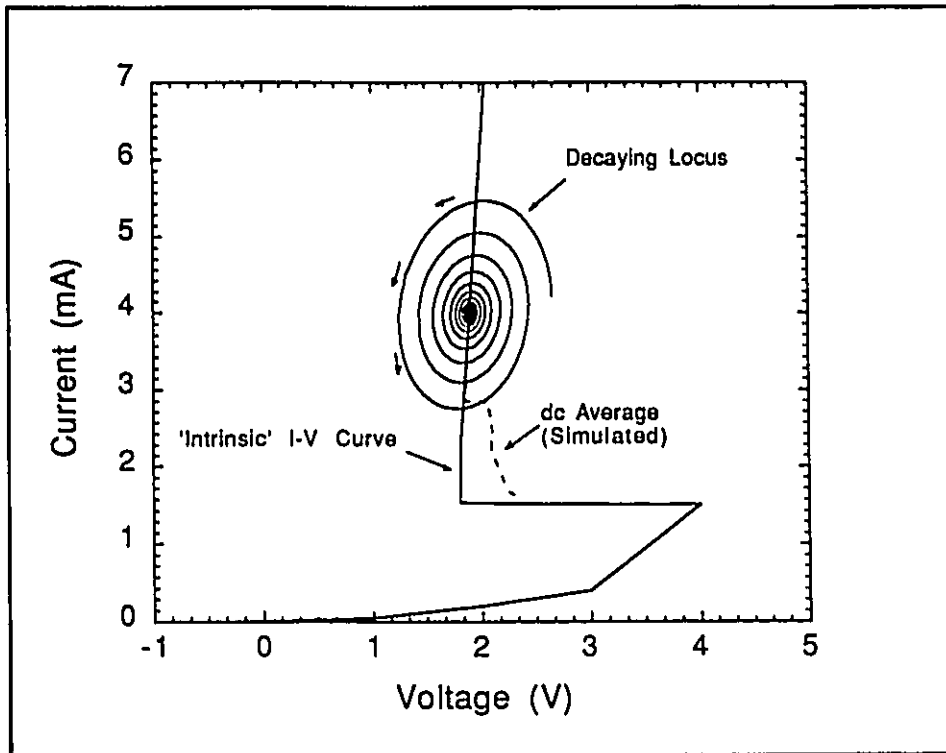


Figure 5.13: The calculated dc average of voltage and current oscillations simulated in a numerical model. Also seen is the simplified intrinsic I-V characteristic used as an input to the model. Superimposed on the I-V characteristics is the calculated locus of operating points during the decaying oscillation as the device is driven at an operating point far removed from the regime of negative differential resistance (4mA). Chosen values for C_c and L_s were 22nF and 5mH respectively.

the DOES device from the constant current source. When the current to the DOES falls below I_h , the device returns to the high-impedance OFF-state (segment CD on Fig. 5.12). Subsequently, the voltage across the device rises to V_s and again switches to the ON-state (segment DA on Fig. 5.12). Of course, charging the DOES device to V_s means that the external and internal capacitors must also be charged to V_s .

Ultimately, the charging and discharging of the external capacitor temporally dominates the oscillation cycle. Thus, the measured dc voltage and current in the NDR region are simply the time-averaged voltage of the charging and discharging cycle and the constant current being supplied.

The transition from the OFF- to ON-state causes the parasitic capacitive elements to discharge through the device. This occurs with a time constant determined by the external and intrinsic capacitance elements and the ON-state impedance of the device. For example, given that the external capacitor employed to obtain the voltage oscillations seen in Fig. 5.12 is 22nF, and that this capacitance dominates other capacitive elements in the circuit, then the ON and OFF-state impedance can be estimated to be approximately 200 Ω and 50 k Ω , respectively. From the dc I-V characteristics measured previously, these values are plausible. However, a direct comparison is inappropriate, since the device impedance varies with internal bias conditions.

With increasing capacitance in the circuit, the step-like nature of the dc I-V in the NDR becomes sharper. This is because the waveform becomes more saw-tooth in shape and the dc voltage measured from a saw-tooth waveform becomes less frequency dependent. However, it must be noted that a perfect saw-tooth waveform is not possible since as the device voltage rises, the RC time constant varies with the changing device impedance. Thus, following segment DA in Fig. 5.12, the DOES device demands a greater percentage of the constant drive current. This has been observed in our measurements and can be seen in Fig. 5.7 as a deviation from linearity during the charging cycle. Oscillations will cease with a sufficient dc drive current since the diversion of current from the DOES due to the overshoot will be insufficient to reduce the device current below

I_h. A more comprehensive analysis of the stability criteria and description of the modeling of these oscillation is an area where this work can be extended.

Depending on the integration time, a dc instrument's voltage measurement may or may not be erroneously affected by the decaying oscillation. The integration time of the instrument will determine to what degree the measurement is affected. For this reason, different dc I-V characteristics may result with different instrument integration times.

CHAPTER 6

THREE-TERMINAL DOES: EXPERIMENTAL RESULTS & DISCUSSION

In the AlGaAs/GaAs materials system, the three-terminal DOES has been incorporated into a variety of applications [23-25]. However, in order to realize these complex applications of the DOES device, it is essential to incorporate a third terminal to control switching between the binary states (set/reset functions). The three-terminal device can also be used in conjunction with an optical input to further enhance device functionality. In this chapter, the experimental results for the three-terminal Si/Si_{0.75}Ge_{0.25}-based DOES are presented. Various aspects of the operation were investigated including the effect of current injection and extraction on the I-V characteristics, the effect of concurrent illumination and electrical injection or extraction, and a comparison of simulations and experimental data.

Two batches of devices were fabricated to study the effect of the third-terminal. Batch D2 utilized a simplistic wet chemistry and mask alignment technology where the third-terminal makes contact to the active region. Batch D3 utilized a more complex, self-aligned fabrication procedure using RIE and contact is made to the inversion charge directly. Some comparisons are made in this chapter which attempt to elucidate the benefits of the self-aligned terminal which makes contact to the inversion charge.

6.1 Current-Voltage Characteristics

This section presents the measured I-V characteristics of the three-terminal Si/Si_{0.75}Ge_{0.25}-based DOES (batches D2 and D3) under a variety of conditions. In general, when presenting the operational characteristics of the device a linear plot of current versus voltage is given. In some instances, the logarithm of current versus voltage (log(I)-V) is presented to illustrate the behavior of the OFF-state current.

6.1.1 Current Injection into the Active layer

The room temperature I-V characteristic with injection current, I_{inj} , as a parameter is shown in Fig. 6.1 for a 100 μ m diameter device. As with the two-terminal device, the three-terminal version exhibits electrical bi-stability; the electrical characteristics exhibit a high-impedance OFF-state and a low-impedance ON-state, separated by a differential negative resistance region. With no injection current into the active layer, a switching voltage, V_{SO} , and its associated current, I_{SO} , define the limit of the high-impedance state, which are seen to be ≈ 3.7 V and 0.7 mA, respectively, and the OFF-state impedance is typically 10 to 15 k Ω .

The onset of the low-impedance state is characterized by a holding voltage, V_h , and an associated current, I_h , which are typically 1.3 V and 2.6 mA respectively. By injecting carriers via the third terminal, the switching voltage, V_s , is reduced below V_{SO} , I_s and I_h move to slightly lower values, and V_h remains essentially unchanged. Thus, with I_{inj} as a parametric variable, a family of I-V curves nesting within the original ($I_{inj} = 0$ mA) I-V curve is generated as shown in

Fig. 6.1. The ratio of the injection current required to partially collapse the switch-back region (say to one-half V_{SO}) over the switching current is perhaps the most simple way to quantify device sensitivity to injection. For the device in Fig. 6.1, the ratio can be calculated as approximately 2.2.

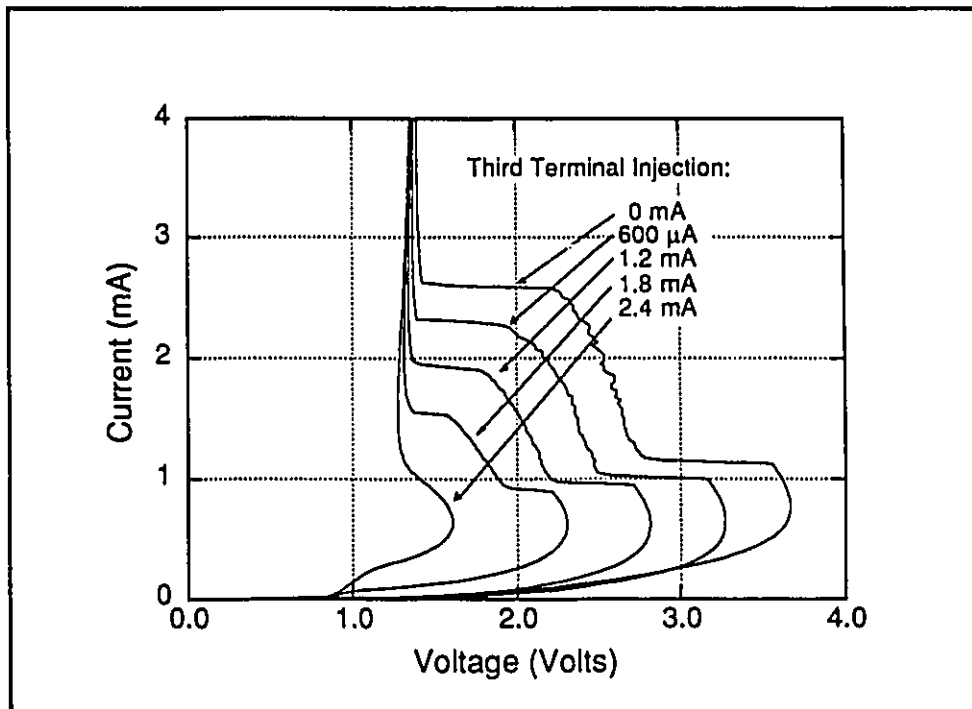


Figure 6.1: The measured current-voltage (I-V) characteristic for the three-terminal Si/Si_{0.75}Ge_{0.25}-based DOES (batch D2) with injection into the active layer contact as a parametric variable.

Figure 6.2 plots the same family on a log(I)-V axis. The device current before switching tends to increase with increasing injection into the active layer. This is reflective of lower barrier surface potential in response to the higher small-signal gain in the system.

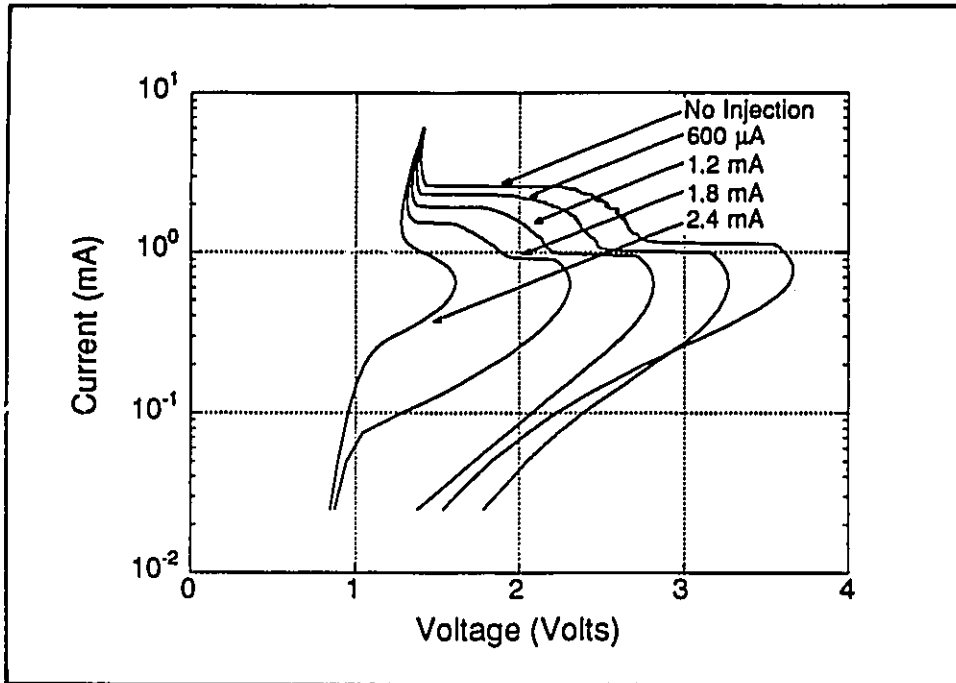


Figure 6.2: The measured logarithm of current versus voltage ($\log(I)$ -V) characteristic for the three-terminal Si/Si_{0.75}Ge_{0.25}-based DOES (same data as in Fig. 6.1).

6.1.2 Current Injection into the Inversion Channel

The effect of injection directly into the inversion-channel can be seen in Fig. 6.3. Again, a family of nesting curves with progressively smaller V_s is seen for the device with areal dimension $\approx 100 \times 100 \mu\text{m}^2$. However, with this third-terminal contacting scheme, the sensitivity ratio of approximately 0.1 is seen to be much better than that measured in Fig. 6.1. Thus injecting current into the inversion channel is the more efficient way of modulating the device I-V characteristics. This data is also consistent with the numerical model calculations presented in Fig. 2.12.

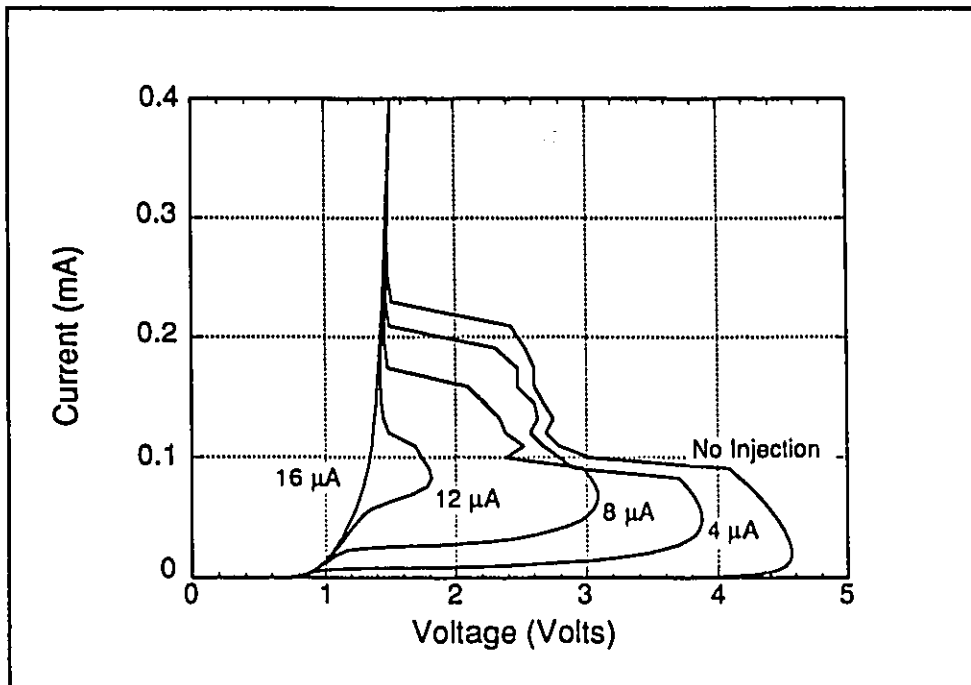


Figure 6.3: The room-temperature current-voltage characteristics for the three-terminal Si/Si_{0.75}Ge_{0.25}-based DOES (batch D3) with current injection into the inversion channel as a parametric variable.

Figure 6.4 illustrates the logarithmic version of the I-V characteristics where it is seen that with increasing injection the current before the switching point increases. This is predominately generation current in the depleted part of the active layer and the current from carriers which surmount the barrier. Thus, for the same bias on the emitter terminal, the depletion region in the active layer is larger and the barrier surface potential smaller with third-terminal injection.

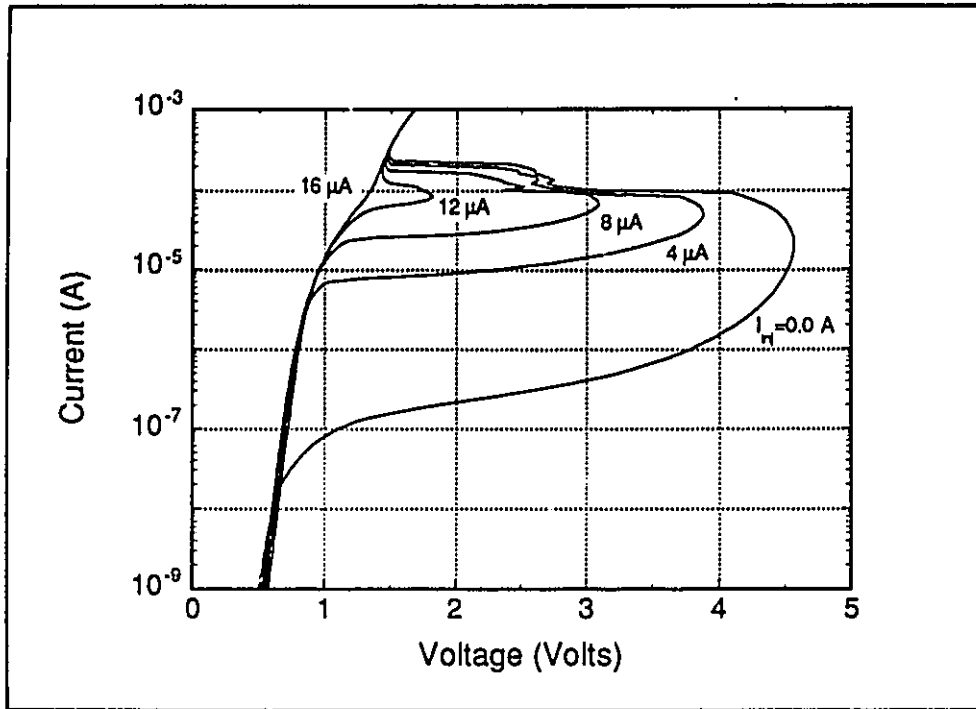


Figure 6.4: The room-temperature logarithm of current versus voltage ($\log(I)$ - V) characteristics for the I-V characteristics of Fig. 6.3.

6.1.3 Effect of Extraction

The effect of third-terminal extraction can be seen in Fig. 6.5 for a $100\mu\text{m}$ diameter device (batch D2). Extracting current from the active region (electrons) serves to increase the switching voltage but lower the switching currents. This effect on the I-V characteristics is not as pronounced as injection. The net effect of extraction is to lower the Fermi-level in the active region. This reduces the feedback current coming from the pn junction formed by the active layer and the substrate. Thus, for a given emitter bias, less hole current reaches the hetero-interface and the overall small-signal gain is reduced. The switching current is reduced because lowering the Fermi-level in the active region expands the

depletion region formed by the junction of the charge sheet and the active layer. Thus, with increasing extraction of electrons from the active layer more generation current in the active layer is seen. This is also the main reason why extraction is less effective than injection at moving V_s .

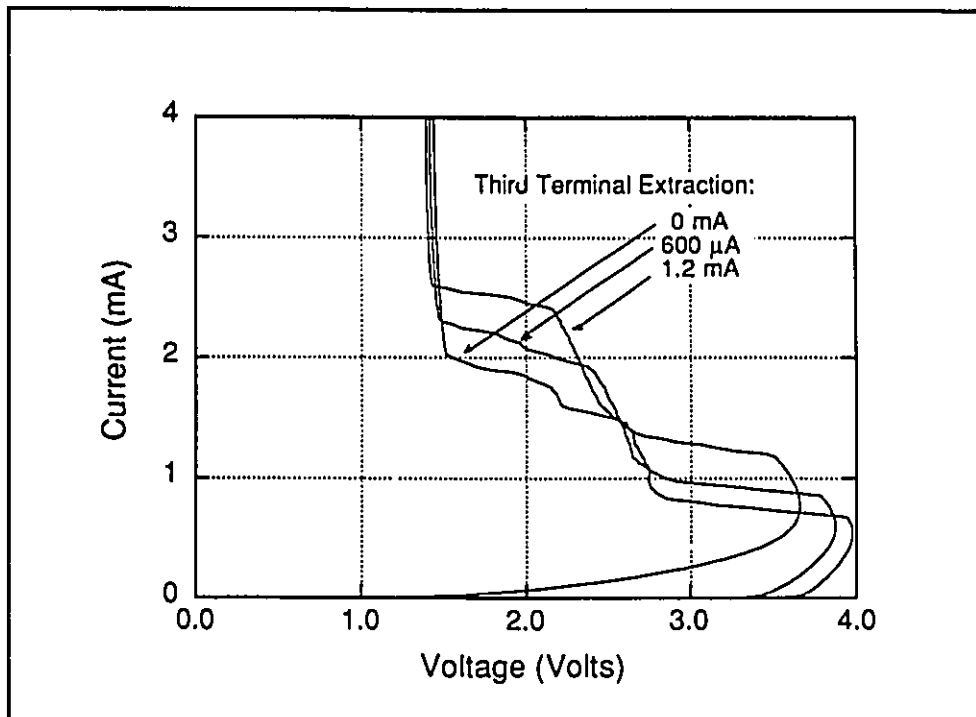


Figure 6.5: The measured current-voltage (I-V) characteristic for the three-terminal Si/Si_{0.75}Ge_{0.25}-based DOES (batch D2) with current injection into the contact to the active region as a parametric variable.

Contrary to injection experiments, extraction from the active layer is more effective than extraction from the channel directly. Extraction from the inversion-layer directly causes the Fermi-level at the hetero-offset to rise with respect to the Fermi-level in the barrier layer and the active layer. This again increases the generation current in the active layer by reverse-biasing the n-n heterojunction.

6.1.4 Optical and Current Injection

Using optical illumination, concurrent with third-terminal injection or extraction, will permit the thresholding of the input signal (optical or electrical) used to trigger the DOES into the ON-state. The effect of concurrent use of optical and third-terminal injection is to transpose all the switching voltages towards lower values (Fig. 6.6). It is interesting to note that for $500\mu\text{A}$ of optical injection and no third-terminal injection, the switching voltage of curve B in Fig. 6.6 is 3.4 V, whereas with no illumination and $600\mu\text{A}$ of third terminal injection, the switching voltage is 3.3 V (Fig. 6.1). This comparison allows an estimate of the magnitude of injection induced by illuminating the device. Alternatively, the amount of optical injection can be estimated by measuring the photocurrent generated within the device when reverse-biased. However, this method may be inaccurate. Although the light from the red HeNe is absorbed approximately evenly throughout the heterostructure, it is in the depletion regions that the photo-generated carriers become spatially separated and affect the potential distribution. These depletion regions will be much different in the case of a forward bias on the device: narrower in the barrier and wider in the active layer. For $500\mu\text{A}$ of optical injection, it was necessary to illuminate the device with 1mW from the HeNe laser (wavelength 632.8 nm). These two methods compare well and seem to suggest a quantum efficiency of approximately 50%.

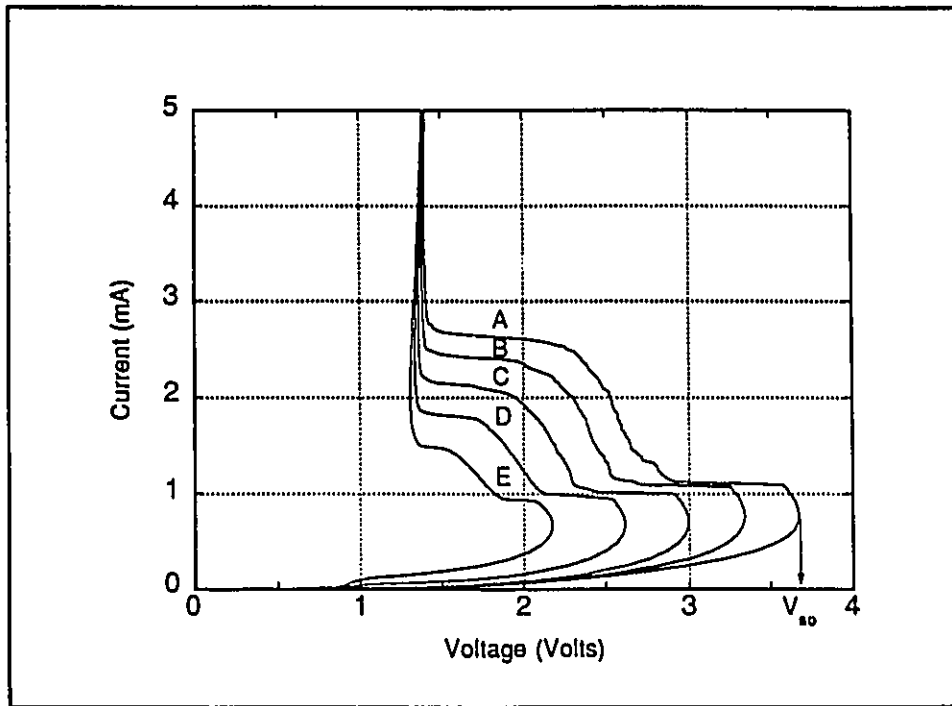


Figure 6.6: The measured room-temperature I-V characteristic of the three-terminal Si/Si_{0.75}Ge_{0.25}-based DOES (batch D2) with concurrent optical injection and electrical injection. Curve A is with no illumination or third terminal injection, B with 500 μ A of optical injection and no third terminal injection, C with the same optical injection and 500 μ A of electrical injection, D with the same optical injection and 1mA of electrical injection, and E with the same optical injection and 1.5mA of electrical injection.

The use of extraction current is also of interest. With 500 μ A of optical injection and, concurrently, 500 μ A of third-terminal extraction, the switching voltage is found to be almost the same value as if no injection or extraction of charge were administered (Fig. 6.7). That is, extraction can be used to negate the effect of optical injection. This is potentially very useful for thresholding the device to trigger the ON-state. Depending on the state of the injection line and the operational load, an optical pulse may or may not trigger the device into the

ON-state. Unfortunately, there is no way to return to the OFF-state except by extracting enough current from the active layer to bring the current flow into the collector below the holding current. This issue will be discussed again in chapter 8 where an integrated circuit is examined which is comprised of the Si/SiGe-based DOES and HFET.

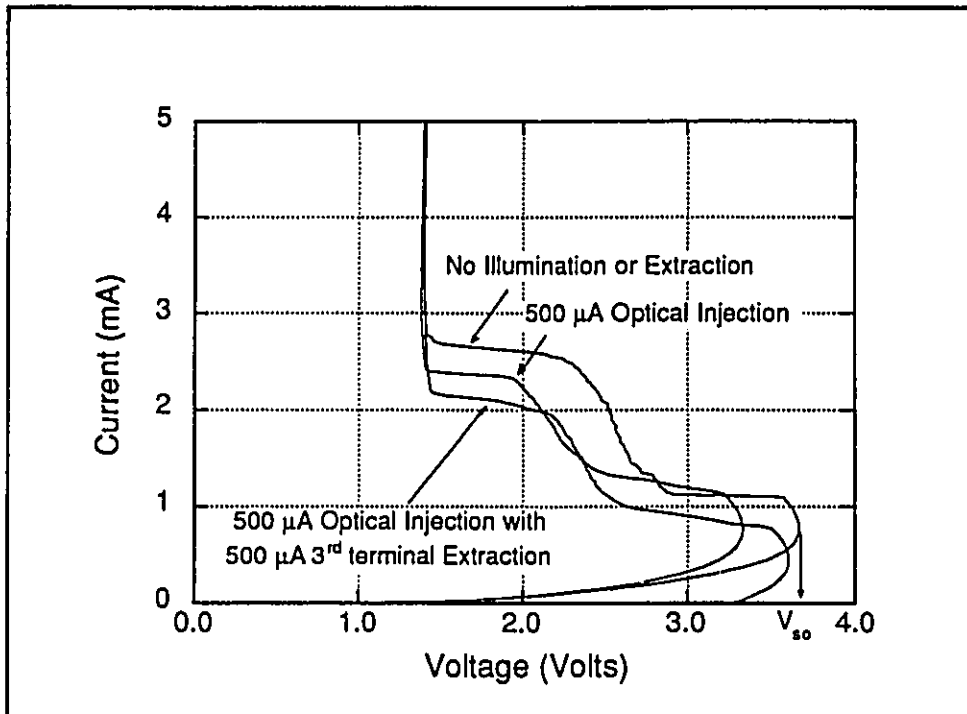


Figure 6.7: The measured room-temperature I-V characteristic of the three-terminal Si/Si_{0.75}Ge_{0.25}-based DOES (batch D2) with concurrent optical injection and electrical extraction.

6.2 Comparison with Simulations

In the preceding sections comparison of the experimental results and the theory of operation outlined in Chapter 2 have been restricted to qualitative statements. The computer-based simulation mentioned in Chapter 2 requires a number of input parameters which must be estimated for the Si/SiGe materials system. In effect, quantitative comparisons between the calculated results of the model and the experimental data are inappropriate in light of these adjustable material parameter. For example, by varying the generation lifetime in the depleted part of the active region by two orders of magnitude (say from 2ps to 200ps) will lower the predicted switching current by approximately one order of magnitude. A more effective and realistic evaluation of the accuracy of the model is to compare the ratios of injection efficiency (previously described). Fig. 6.8 plots the calculated and experimental logarithm of current density versus voltage ($\log(J)$ -V) characteristic. The calculated data is for the identical structure illustrated in Fig. 2.2 with the exception that the doping density in the charge sheet is $3.7 \times 10^{12} \text{ cm}^{-2}$ instead of the target value of $2.5 \times 10^{12} \text{ cm}^{-2}$. The calculated family of curves (dashed lines) appears to overestimate the current densities in the device by one order of magnitude. However, in both sets of data, the injection current required to collapse V_{SO} to one-half V_{SO} is almost precisely the same fraction of the switching current.

The operational characteristics predicted from the model also has a much lower holding voltage than the experimental data. This can be attributed to parasitic resistance in the experimental measurements. As in the experimental data, the model also predicts an increase in the generation current in the depleted active layer with increasing injection.

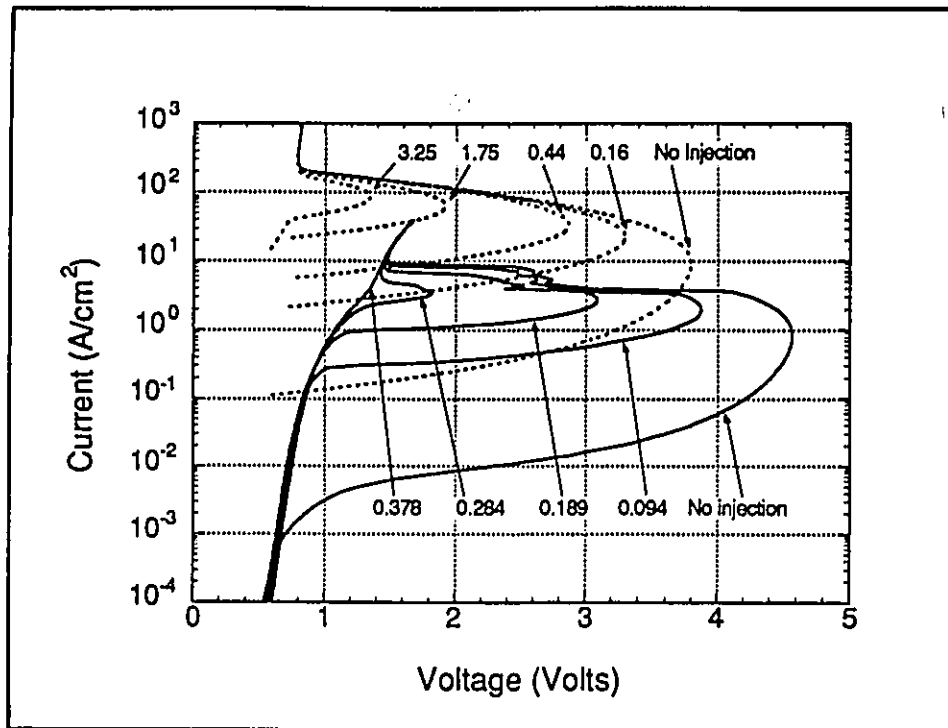


Figure 6.8: Comparing measured (solid line) and calculated (dashed line) room-temperature I-V characteristics for the three-terminal Si/Si_{0.75}Ge_{0.25}-based DOES (batch D3) with the third terminal making contact to the inversion channel. Used as a parametric variable in both family of curves is the injected current density.

CHAPTER 7

HFET: EXPERIMENTAL RESULTS & DISCUSSION

In this chapter, the experimental characteristics of the first Si/SiGe-based Heterojunction Field Effect Transistors (HFET) are presented. Preceding these characteristics is a brief description of the experimental set-up for both dc and ac measurements. Following this section, dc measurements including the current-voltage characteristics of the source and drain, gate leakage, and the transconductance are presented. An investigation of the high frequency characteristics of the transistor is reported in section 7.3.

On each die of the slice (batch D3), a variety of transistors with gates ranging in size from $1\mu\text{m} \times 25\mu\text{m}$ to $4\mu\text{m} \times 150\mu\text{m}$ were fabricated. Some analysis and comparison based on the gate dimensions is also presented in this chapter.

7.1 Experimental Procedure

Figure 7.1 illustrates a cross-sectional schematic of the HFET with the electrical leads labeled. For the most part, the HP4145B was used as the system controller for the dc electrical measurements. Electrical contact to the transistor was made by either by probing the device with tungsten needle probes mounted on fine XYZ positioners or by wire bonding the device in a 20-pin metal package

and using the HP personality board. In either case, an RF shield was used and each source/measuring unit (SMU) of the HP4145B is on triaxial cable.

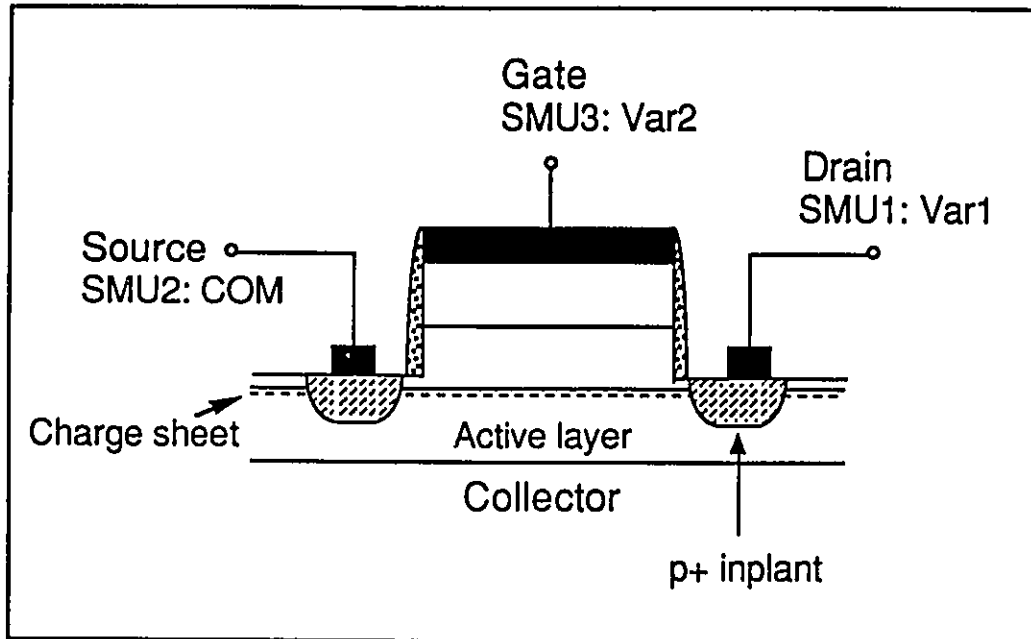


Figure 7.1: A cross-sectional schematic of the HFET with electrical leads labeled to the source, drain, and gate.

High frequency characteristics were performed using the facilities of the Communications Research Laboratory (CRL) at McMaster University. Figure 7.2 is a schematic of the experimental set-up for these measurements. The HP8341B Synthesized Sweeper was used to generate the ac signal sent to the gate. The frequency of this signal could be adjusted over the range from 10MHz to 20GHz. The power, or equivalently, the peak-to-peak voltage launched into the 50 Ω line, could also be adjusted. For these measurements, power was maintained, for all frequencies, at 5dbm which corresponds to a peak-to-peak voltage swing at the gate of 0.5624V. For each frequency to be used, the signal at the gate of the tran-

sistor was measured and the power setting of the HP8341B adjusted to 5dbm. This would remove any frequency dependence in the output port and transmission line. The HP4145B Semiconductor Parameter Analyzer supplied a constant negative voltage (-7V) to the drain of the transistor (through a bias T) and a ground to the source contact.

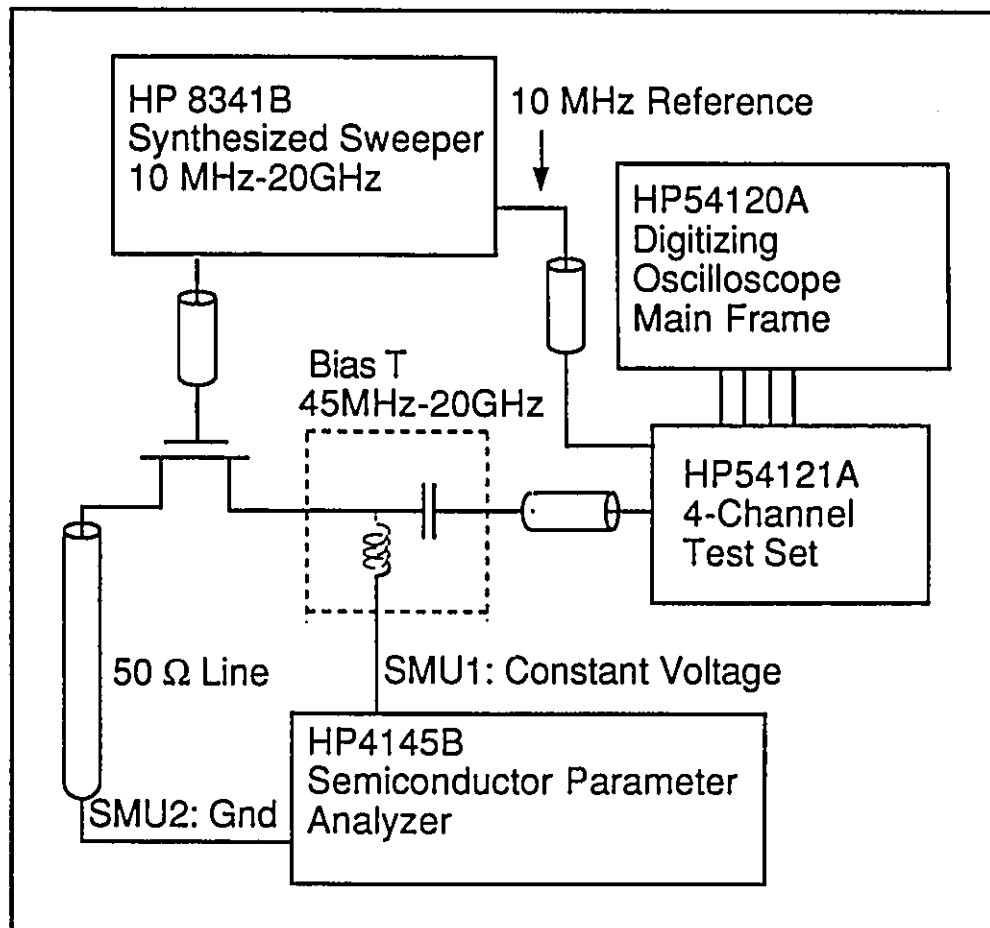


Figure 7.2: A schematic of the experimental set-up used to measure the high frequency characteristics of the HFET.

The response of the transistor was capacitively coupled to the 50Ω input of the HP54121A 4-Channel Test Set. The sampled points were then sent to a HP54120A Digitizing Oscilloscope. Electrical contact to the device was made with a set of Cascade Microtech high frequency probes with foot print matching the contact metallization pattern of the device.

7.2 dc Current-Voltage Characteristics

This section contains the dc electrical characteristics of the Si/Si_{0.75}Ge_{0.25}-based HFET. These results include the source-drain current-voltage characteristics, the subthreshold characteristics, the transconductance characteristics, and some of the effects of gate dimension.

7.2.1 Source-Drain Current Characteristics

With zero gate bias, the saturated source-drain current (I_{dsat}) was measured to be $\approx -3\text{mA}$ at -4V source-drain bias (V_{ds}) indicating a depletion mode device with distinct ohmic ($\approx 66\Omega/\text{mm}$) and saturation regions (Fig. 7.3). The source-drain characteristics have Early voltage of $\approx 80\text{V}$. With increasing positive gate-source bias, V_{gs} , I_{dsat} was observed to decrease to approximately $-10\mu\text{A}$ at $V_{ds}=-4\text{V}$ and $V_{gs}=+4\text{V}$. With increasing negative gate bias, I_{dsat} was observed to increase to values greater than -6mA at $V_{ds}=-4\text{V}$ and $V_{gs}=-2\text{V}$. Over the range of $V_{gs}=-2\text{V}$ to $+6\text{V}$, leakage from the gate was below $10\mu\text{A}$ with little or no dependence upon V_{ds} . Beyond these limits, gate leakage was observed to increase exponentially. Exponential growth was also observed in I_{dsat} at voltages greater than $V_{ds}=-12\text{V}$.

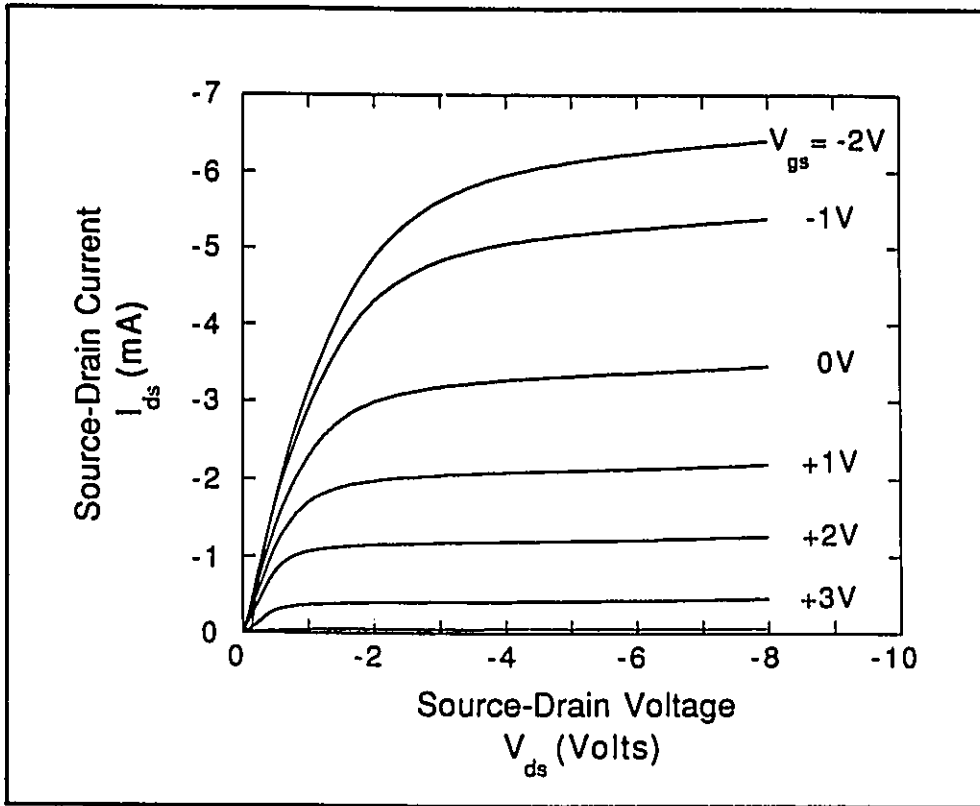


Figure 7.3: The source-drain I-V characteristic of the Si/Si_{0.75}Ge_{0.25}-based HFET with gate length 1 μ m and width 150 μ m. Gate voltage, V_{gs} , is seen as a parameter where source-drain current, I_{ds} , is plotted versus source-drain voltage, V_{ds} .

Figure 7.4 shows the gate and drain current as a function of V_{ds} at $V_{gs} = -2V$. With increasing V_{ds} , gate current decreases exponentially and saturates at a constant value ($\approx 4.8mA$). The constant value represents the current coming over the barrier into the active region (I_b) and current leaking out the forward-biased $n-p^+$ diode formed by the gate and implanted source contact (I_{ls}). Interestingly, at $V_{ds}=0V$, the leakage current is approximately double the saturated value at larger V_{ds} . This symmetry is evidence that gate leakage is primarily composed of lateral

leakage to the source and drain as opposed to current over the barrier. As described in section 3.3.2, the latter component can be reduced by etching as close as possible to the charge sheet when forming the gate mesa. In this manner, only a thin electrical connection is made between the gate and the source contact on the side of the barrier closest to the surface.

The primary effect of the gate leakage on the extrinsic drain characteristic is to record a lower current value. Thus, some care must be taken in order to extract operational characteristics such as mobility from this data. In attempting to characterize these devices it is prudent to simultaneously record source current as well as the drain current.

Mobility values, extracted from long channel device measurements, were found to be between 50 and 150cm²/V·s which is consistent with values observed in other p-channel Si/Si_{1-x}Ge_x-based metal-semiconductor FETs (40, 42).

The subthreshold slope was measured to be 720mV/decade and the characteristic is seen in Fig. 7.5. This is a much larger value of subthreshold slope than that seen in SiGe or Si-based MOSFETs where typical values are on the order of 100mV/decade for device of comparable gate dimension. However, in the inversion-channel Si/SiGe HFET, the sensitivity of I_{ds} to V_{gs} is dependent upon the design of the heterostructure and subject to optimization.

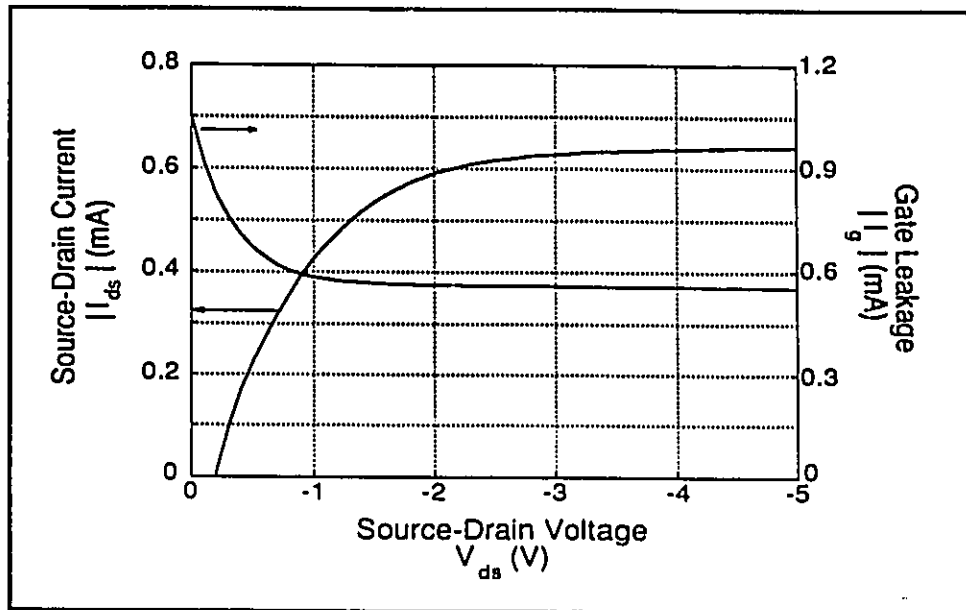


Figure 7.4: At a gate to source voltage of -2V, the experimentally observed dependence of source-drain current, and gate leakage current on source-drain voltage is plotted. The transistor had gate length $3\mu\text{m}$ and width $100\mu\text{m}$.

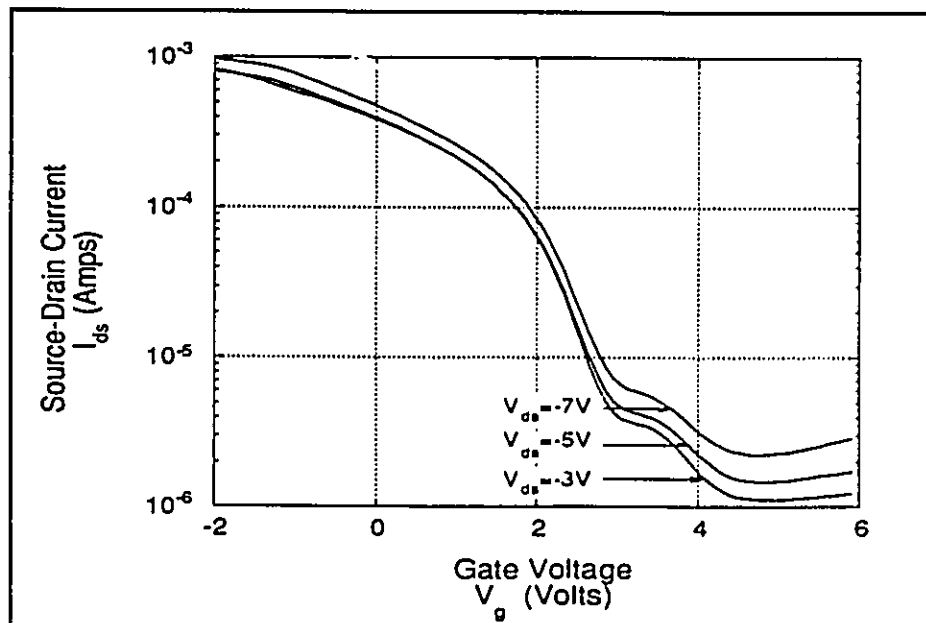


Figure 7.5: The subthreshold characteristics of the HFET with gate length $1\mu\text{m}$ and width $150\mu\text{m}$ and with source-drain voltage as a parameter.

7.2.2 Transconductance Characteristics

In Fig. 7.6, the dependence of g_m on V_{gs} is seen. For increasing V_{gs} , a rapid rise in g_m over the range $V_{gs}=0V$ to $-1V$ was observed for all V_{ds} values above V_{dsat} . These measurements allude to a complex interaction between V_{gs} and the channel properties. A mechanism for these observations which relates the channel hole population to the gate leakage has been proposed in section 3.3.2.

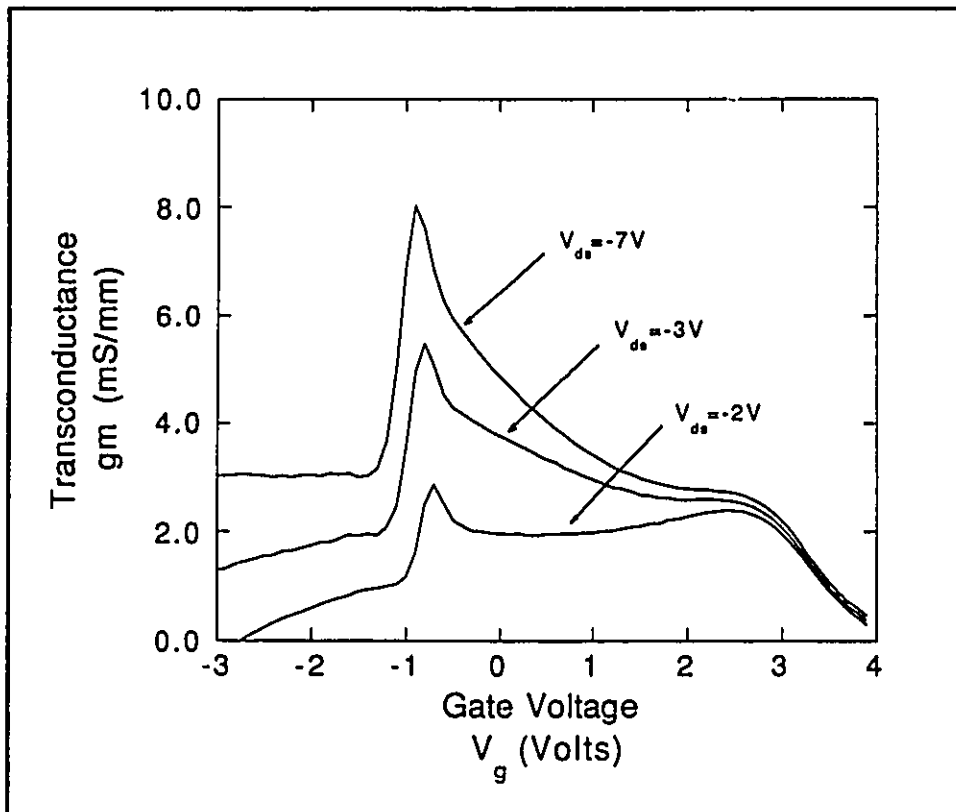


Figure 7.6: The transconductance characteristic of the Si/Si_{0.75}Ge_{0.25}-based HFET with gate length 1 μ m and width 150 μ m. Source to drain voltage, V_{ds} , is used as a parameter where transconductance, g_m , is plotted against gate voltage, V_{gs} .

Below $V_{gs} = -1V$, the gain of the transistor is seen to drop sharply. Figure 7.7 superimposes the gate leakage on the transconductance characteristic for $V_{ds} = -7V$. At the same point gain is seen to fall in the device the gate leakage exponentially increases. Thus, a plausible explanation for this region of the transconductance characteristic is ohmic losses at the gate which account for any further increase in the gate voltage.

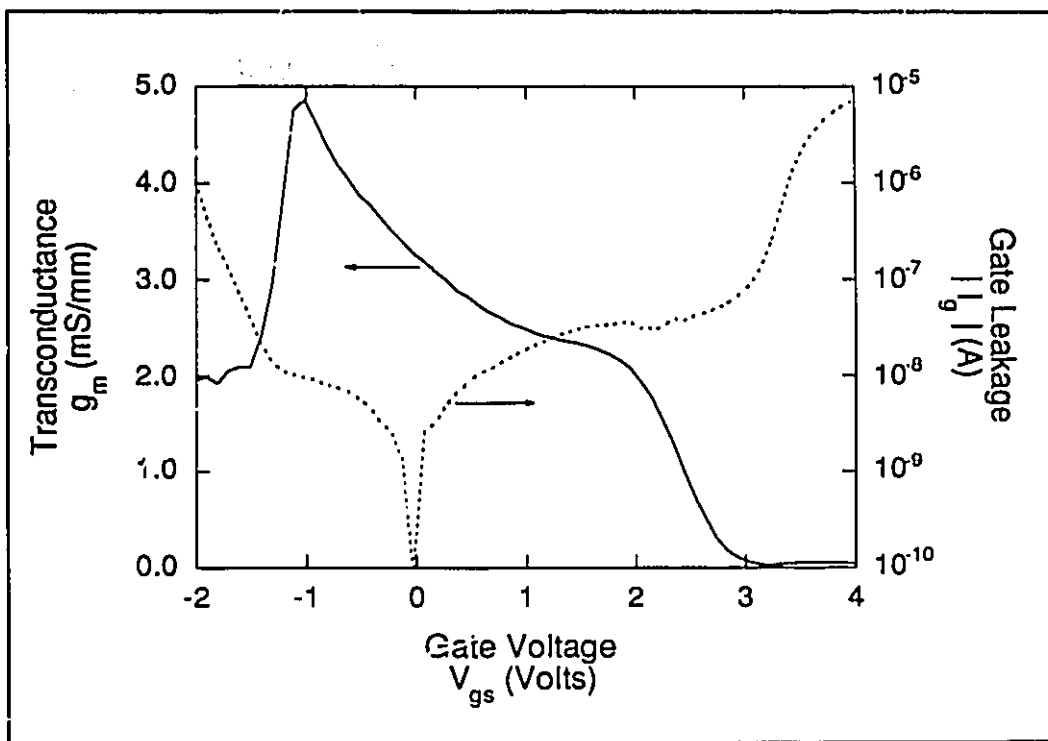


Figure 7.7: Superimposed on the same plot are the experimentally observed transconductance characteristic (g_m versus V_{gs}) and the absolute value of gate leakage, I_g , for a device with gate length $1\mu m$, width $150\mu m$, and source-drain voltage, $V_{ds} = -7V$.

7.2.3 Effect of Device Size

Gate length is an important physical dimension in determining the I-V characteristics of the HFET. Consistent with the theory outlined in chapter 3, with decreasing gate length the saturated source-drain current is observed to increase (Fig. 7.8). Each curve in Fig. 7.8 is the average of several devices with identical gate dimension.

With increasing gate width a similar trend is observed (Fig. 7.9) however, whereas one might expect I_{dsat} to double with double the gate length, this is not observed. For example, doubling the width of the gate from $50\mu\text{m}$ to $100\mu\text{m}$ increases I_{dsat} from $\approx 2.4\text{mA}$ to $\approx 3.5\text{mA}$.

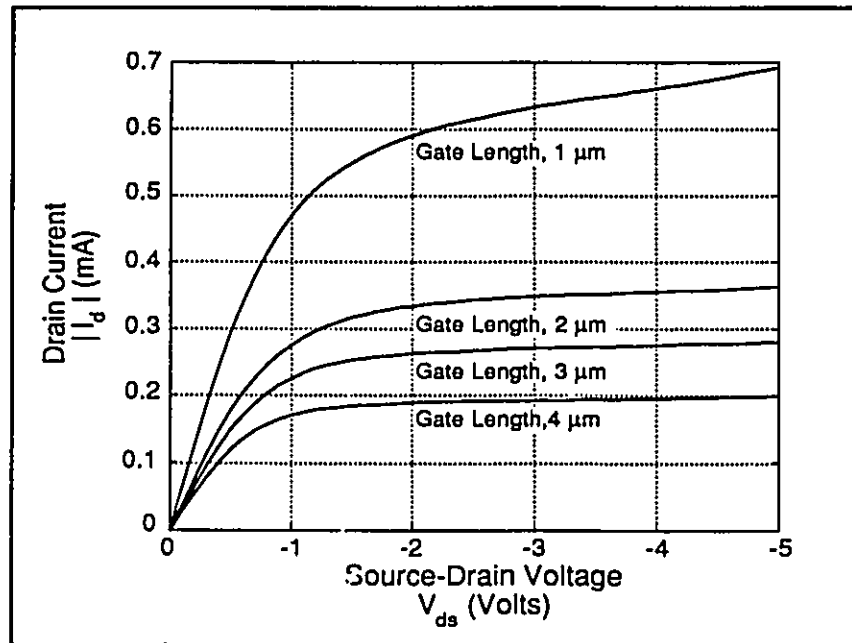


Figure 7.8: The source-drain I-V characteristic of the Si/Si_{0.75}Ge_{0.25}-based HFET with $V_{gs}=1\text{V}$ and gate width $100\mu\text{m}$. The gate length is used as a parameter.

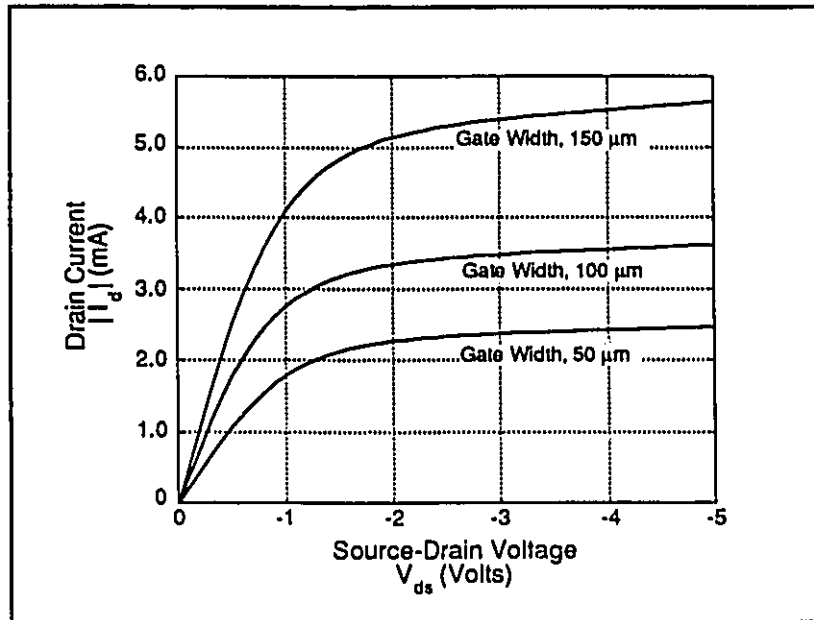


Figure 7.9: The source-drain I-V characteristic of the Si/Si_{0.75}Ge_{0.25}-based HFET with $V_{gs}=1\text{V}$ and gate length $2\mu\text{m}$. The gate width is used as a parameter.

7.3 High Frequency Characteristics

The high frequency characteristics of the Si/Si_{0.75}Ge_{0.25}-based HFET with gate length $1\mu\text{m}$ and width $150\mu\text{m}$ are seen in Fig. 7.10. This measurement is described in section 7.1. With $V_{ds}=-5\text{V}$ and $V_{gs}=0\text{V}$, the voltage gain was observed to have a 3-dB frequency of $\approx 1.8\text{GHz}$. This value reflects the gate to drain capacitance, C_{gd} , measured as $3\text{-}4\text{pF}$ with a gate-drain bias, V_{gd} , of $+5\text{V}$. This capacitance will have an inverse square root dependence on V_{gd} since it arises from the depletion of the barrier layer. Thus, the 3-dB frequency will, to some extent, be dependent upon the bias conditions on the device.

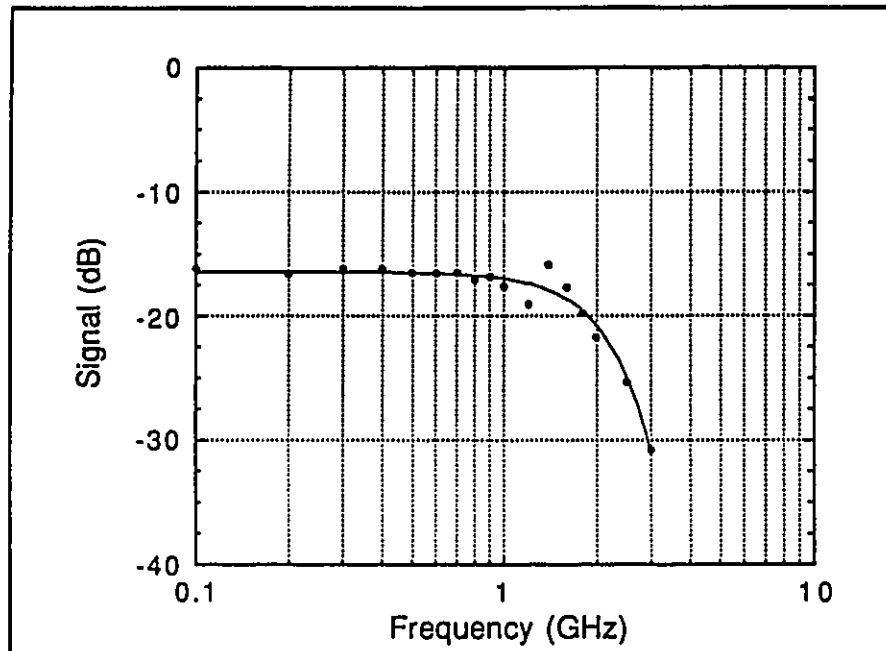


Figure 7.10: The high frequency response of the HFET. The device had gate length $1\mu\text{m}$ and width $150\mu\text{m}$ and a dc $V_{gs}=0\text{V}$ on the gate.

A direct measurement of the gate-to-drain capacitance is seen in Fig. 7.11. As expected, a linear dependence for device capacitance on gate dimension is observed. The intercept of the y-axis on this plot indicates some constant parasitic capacitance element. The stray capacitance of the leads and the test fixture was eliminated from this measurement. Thus, the capacitance associated with the y-intercept is intrinsic to the device. A possible source for this is the bonding pads. These devices were constructed on a highly doped substrate. The metal contact pads are separated from the substrate by 5000\AA of silicon nitride and has areal dimension of $\approx 22,500\mu\text{m}^2$. Taking the dielectric constant of silicon nitride as 7.5 gives a capacitance of $\approx 3\text{pF}$. This corresponds well with the y-axis intercept.

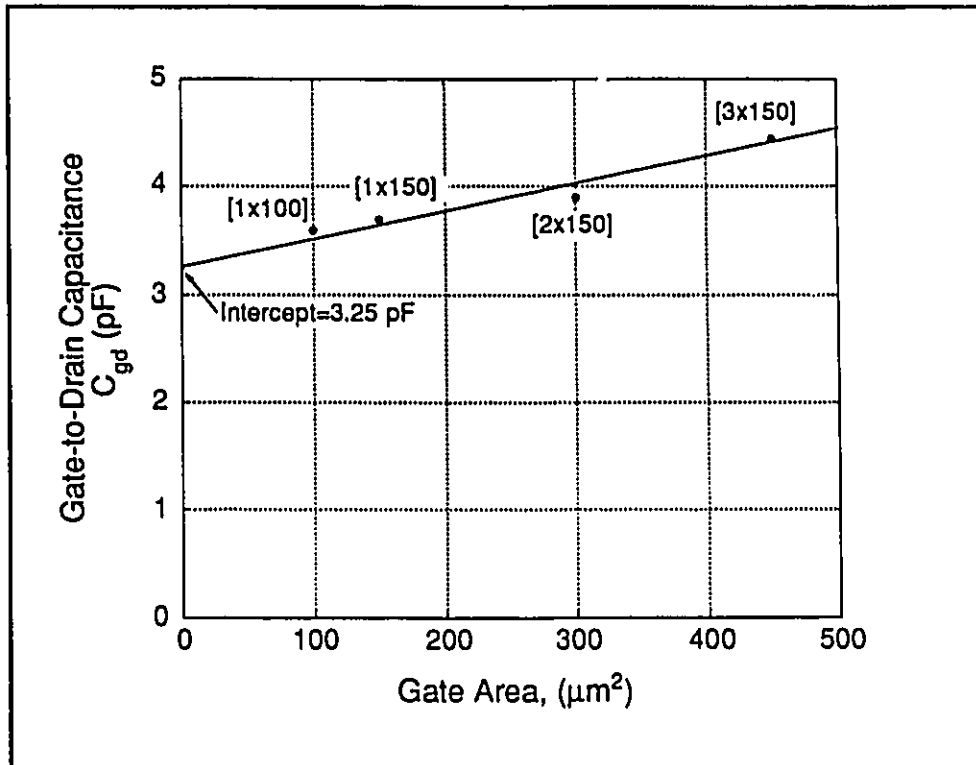


Figure 7.11: The measured dependence of gate-to-drain capacitance on gate size of the Si/Si_{0.75}Ge_{0.25}-based HFET. There was no dc bias on the gate or drain. For each point on the graph the actual gate dimension (width x length) is given in brackets. The straight line fit intercepts the y-axis at 3.25pF which represents the stray capacitance of the measurement test circuit and bonding pads.

7.4 Simulations & Comparisons

In Fig. 7.6, peak transconductance, g_m , of $\approx 8\text{mS/mm}$ at $V_{ds}=-7\text{V}$ and $V_{gs} \approx -1\text{V}$ was measured. This is the largest p-channel transconductance value measured to date in a Si/SiGe-based metal-semiconductor FET but still considerably lower than values measured in SiGe-based MOSFET. Researchers have demonstrated p-channel SiGe/Si metal-oxide-semiconductor (MOS) FETs and

have measured transconductance values as high as 64mS/mm [44]. This value compares well with modern-day Si PMOS ($g_m \approx 80\text{mS/mm}$), although in both cases high temperature processing ($> 800^\circ\text{C}$) is required.

The general shape of the transconductance characteristic is remarkably similar to the calculations presented in Chapter 3. However, on the experimental curve, the range of voltages over which the transconductance rises and reaches a pinnacle is much broader than the range predicted by theory. In addition, the calculated values continue to rise with increasingly negative gate voltages as ohmic drops in the gate are not considered in the model.

In Chapter 4 it was determined from the analysis of the SIMS that the areal doping density in the charge sheet was $\approx 3.2 \times 10^{12}\text{ cm}^{-2}$. Referring to Fig 3.4 and using the curve with active layer doping $1 \times 10^{17}\text{ cm}^{-3}$, a depletion mode device with threshold voltage $\approx -1\text{V}$ is predicted for a charge sheet doping of $3.2 \times 10^{12}\text{ cm}^{-2}$. This calculation compares very well with the measured results seen in Fig. 7.3.

CHAPTER 8

DEMONSTRATION OF A Si/SiGe OPTOELECTRONIC RS FLIP-FLOP

In this chapter, the integration of Si/SiGe heterojunction field effect transistors (HFET), and a three-terminal, double-heterostructure, optoelectronic switch (DOES), in a functional circuit is demonstrated. The emphasis was to use devices based on a common growth sequence and compatible fabrication methodology which will allow integration of various optoelectronic devices on a single monolithic chip. The optoelectronic reset-set flip-flop presented in this work uses the Si/SiGe-based HFET and the three-terminal DOES fabricated from MBE growth #951. In actuality, three HFETs were used where one of the HFETs was electrically configured as a three-terminal DOES. That is, the gate of the HFET was made the emitter of a DOES whilst the source was made to act as a third-terminal injector. Contact to the substrate was made to complete the transformation from HFET to DOES. The switching I-V characteristic of the HFET with terminal configuration rendering it a DOES is seen in Fig. 8.1. The switching voltage and holding voltage are both slightly larger than normally observed of the DOES devices fabricated from this wafer. (c.f. Fig. 6.1)

The circuit utilizes the ability of the three-terminal Si/SiGe DOES to respond to optical and electrical inputs simultaneously to realize an optoelectronic logic circuit. This circuit is described in section 8.1. Issues related to the integration of devices based on the inversion-channel technology are discussed in section 8.2.

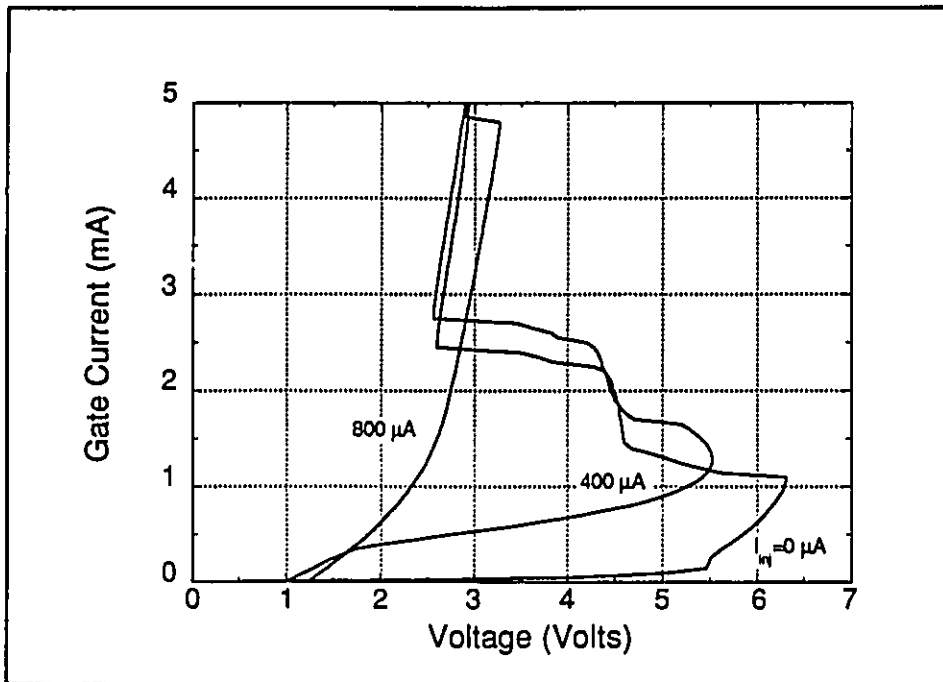


Figure 8.1: The switching I-V characteristic of an HFET electrically configured to operate as a DOES with current injected into the source as a parameter. The device had gate length $1\mu\text{m}$ and width $150\mu\text{m}$.

8.1 CIRCUIT DESIGN AND OPERATION

The flip-flop, also known as the bi-stable multivibrator, is commonly used as a memory device in logic systems, since it can store information about previous events [77]. A reset-set flip-flop has two inputs. An event, represented by a pulse at the set input, triggers the RS flip-flop output to a high-logic state. Following this, a pulse at the reset input returns the output to a low-logic state. This type of flip-flop is not commonly used in electrical logic systems because its output value becomes indeterminate if a high-logic state is present at the set and reset inputs

simultaneously. The optoelectronic RS flip-flop presented here does not have this problem, since the output goes to a low-logic state whenever its electrical reset input is in a high logic state, independent of the status of the optical set input.

The basic configuration of the complete Si/SiGe optoelectronic reset-set flip-flop is shown in Fig. 8.2, and Fig. 8.3. The circuit design can be divided into three modules, the optoelectronic switch, the carrier injector, and the current bypass.

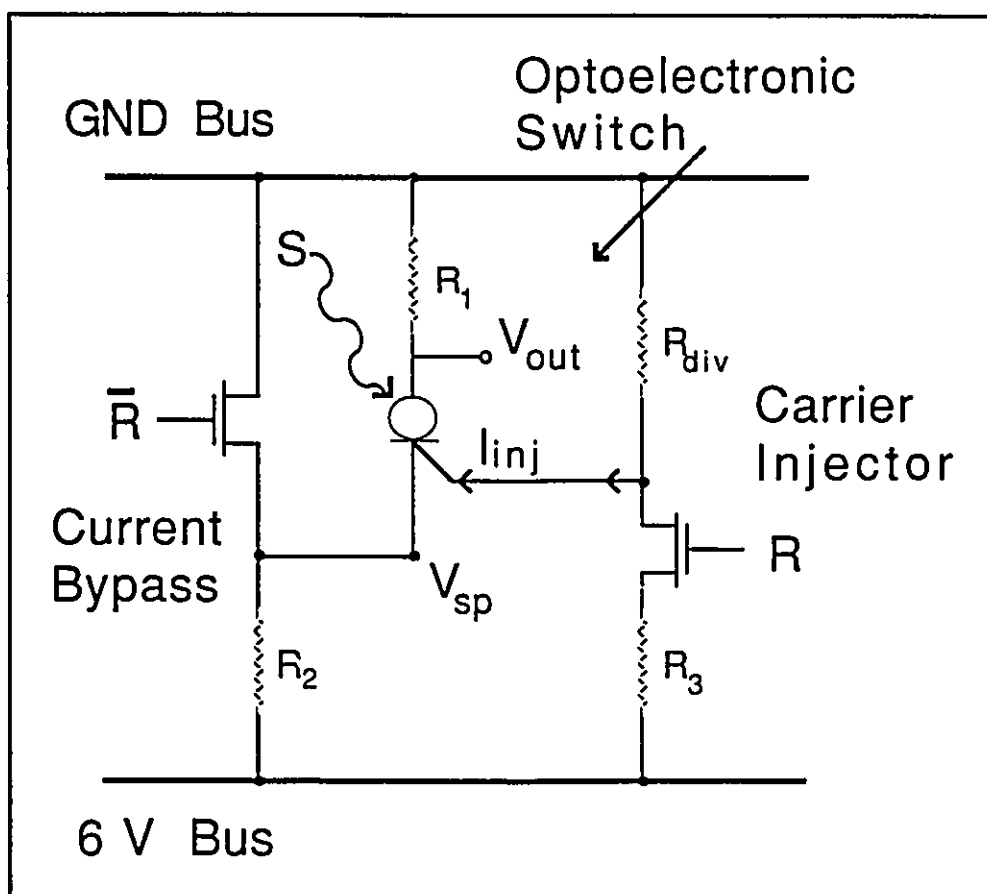


Figure 8.2. A schematic of the RS flip-flop design.

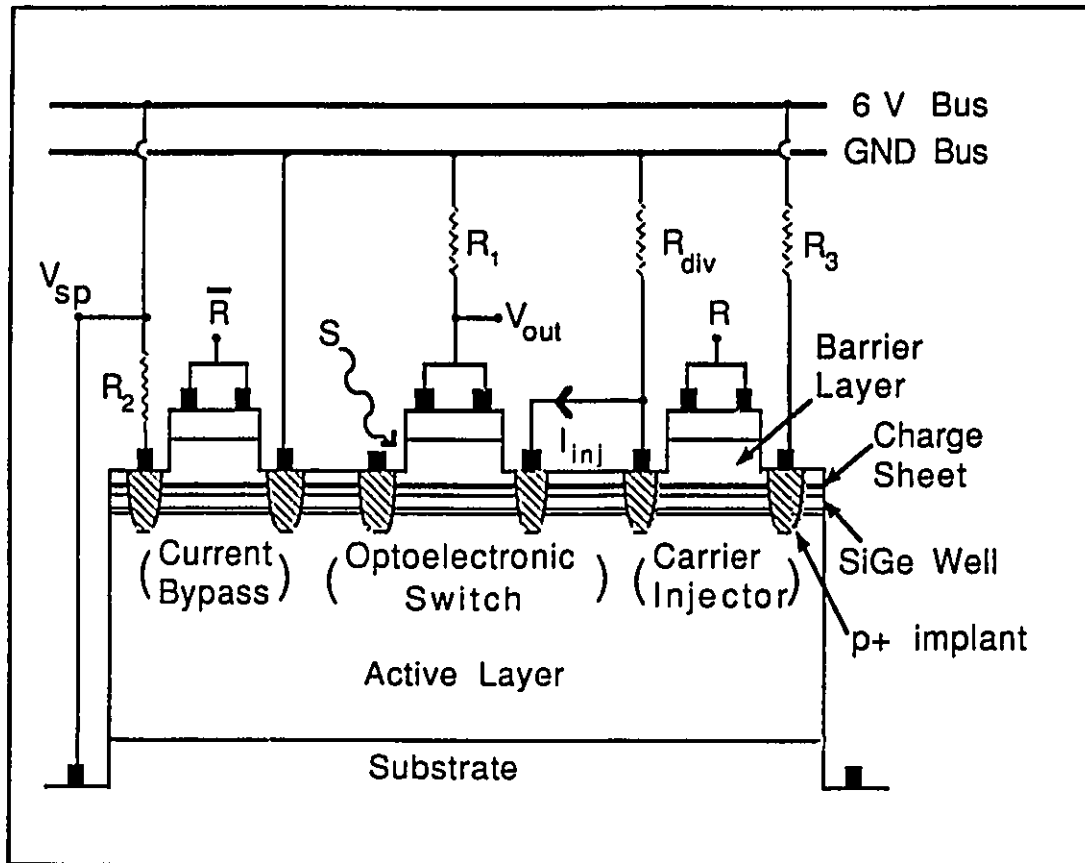


Figure 8.3: The RS flip-flop design, showing the integrated heterostructure. The three HFETs were from the same die and were mounted and wire bonded in a 20-pin flat metal package.

8.1.1 Optoelectronic Switch Module

The optoelectronic switch module consists of load resistor R_1 in series with a three-terminal DOES. Details of the operation of this particular configuration are described in chapter 6. In the optoelectronic switch module, a load resistor R_1 is placed in series with the DOES so that the operating point of the module will be on the high impedance portion of the device characteristics. Using electrical injection, via the third terminal of the DOES, this operating point can be shifted closer to the

limit of the OFF-state. If optical injection is then added concurrently, the I-V curve of the DOES can be shifted to rest within the previous characteristic so that the operating point of the switch module can no longer stay in the OFF-state. Using simultaneous electrical and optical injection an optical threshold can be set for triggering the device into the ON-state.

The position of the operating point for the optoelectronic switch is determined by the voltage V_{sp} , shown in Fig. 8.2, and Fig. 8.3. Changes in the voltage drop across resistor R_2 , resulting from the changes in the current flowing through the optoelectronic switch module, are reflected in the supply voltage V_{sp} . These changes that occur in V_{sp} throughout the operating cycle of the optoelectronic RS flip-flop are illustrated by the three load lines seen in Fig. 8.4. The operating points resulting from the intersection of each load line with the appropriate DOES I-V curves represent the three states the circuit can be in, the injected state, the ON-state, and the OFF-state.

A design consideration encountered with the optoelectronic switch module is how the shape of the DOES characteristics limit the range of bus voltages that can be used for the flip-flop circuit. From the nested characteristics in Fig. 8.4 it is seen that a bus voltage lower than 4V would not allow the optoelectronic switch to operate in its ON-state, and a voltage higher than 7V would not allow operation in its OFF-state. The design of the DOES heterostructure will determine the extremes of voltages that can be used on the bus and therefore the rails of the output. The DOES used to implement the optoelectronic switching module had unusually high holding voltage when compared to the results of chapter 6. This may be related to contact resistance to the gate of the HFET structure in use as a DOES.

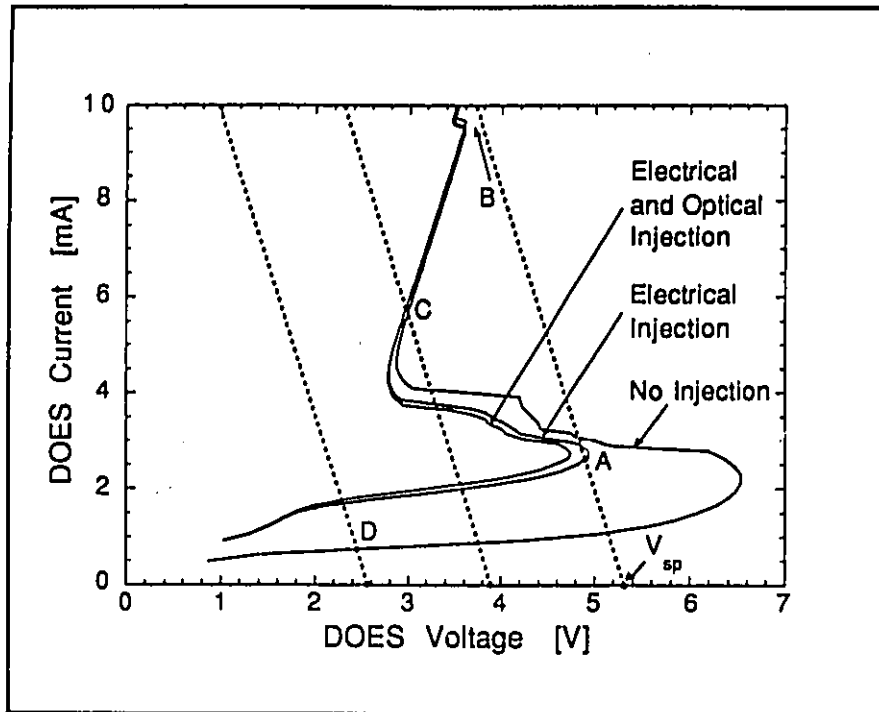


Figure 8.4. The characteristic I-V of the opto-electronic switch module under three conditions: 1) no injection, 2) electrical injection, and 3) both optical and electrical injection. Superimposed on the characteristic is the load line appropriate for each condition.

8.1.2 Carrier Injector Module

In the RS flip-flop circuit, an HFET in the carrier injector module supplies current injection I_{inj} to the third terminal of the DOES. The Si/SiGe HFETs used in this circuit operate as depletion mode devices. It has been observed section 7.2.1 that with zero gate bias these HFETs have a saturated source-drain current, I_{dsat} , of approximately -2mA with I_{dsat} increasing to values greater than -6mA with increasing negative gate bias. Thus, when the reset input, R, at the gate terminal of the carrier injector module is in a low voltage state (0V), the bias voltage V_{gs} for the

carrier injector HFET is approximately -6V , resulting in a very large I_{dsat} . This current is reduced to an acceptable level with the addition of resistor R_3 which draws down V_{gs} . The resistor R_{div} acts as a current divider which is used to select the level of current injection, I_{inj} , passing to the third terminal of the DOES. This level of current injection is selected so that the resulting I-V characteristic of the DOES narrowly intersects the load line of R_1 at point A in the high impedance portion of the DOES characteristic as shown in Fig. 8.4. If, while in this injected state, the DOES is sufficiently illuminated with the optical input S, as shown in Fig. 8.2, and Fig. 8.3, its I-V curve will change so that the load line for R_1 can only intersect the low impedance portion of the DOES IV at point B. However, the increased current flow through R_2 results in a decrease in V_{sp} , which shifts the operating point of the optoelectronic switch to point C.

8.1.3 Current Bypass Module

The current bypass module is necessary to turn off the optoelectronic switch. This is accomplished by dropping the supply voltage V_{sp} of the optoelectronic switch module so that the load line for resistor R_1 can only intersect the DOES IV in the high impedance portion of the DOES characteristic. The current bypass module consists of an HFET in parallel with the optoelectronic module and resistor R_2 in series. While the reset input, R, of the injector module is in a low voltage state (0V) the inverted reset input, \bar{R} , at the gate terminal of the current bypass module is in a high voltage state (6V). Referenced to V_{sp} , the HFET in the current bypass module will have V_{gs} greater than 0V resulting in a relatively small I_{dsat} which will not contribute to the circuit operation. When the \bar{R} input is changed to a low voltage state (0V), V_{gs} for the HFET in the current bypass module will

become negative resulting in a large jump in I_{dsat} . Passing through resistor R_2 , this increased current flow drops V_{sp} and shifts the operating point of the optoelectronic switch to the high impedance portion of the DOES IV at point D.

8.2 RESULTS AND DISCUSSION

The output signal of the circuit for simultaneous periodic optical and electrical inputs is illustrated by the top voltage trace shown in Fig. 8.4. This output signal was taken across the load resistor R_1 at V_{out} in the optoelectronic switch module, using an HP54601A digital oscilloscope. The trace was generated by applying a 500 Hz, 6V dc pulse at input R, the same signal one half cycle out of phase at input \bar{R} , and a 245 Hz optical pulse to the surface of the DOES, shown as optical input S in Fig. 8.2, and Fig. 8.3. The electrical pulses were generated by a WaveTek pulse generator, in conjunction with an HP-8112A pulse generator in trigger mode. The optical pulses were generated by chopping the unfocused beam of light with wavelength 632.8nm (HeNe laser) and are illustrated here by the lower voltage trace in Fig. 8.5. Optical filters were used to control the intensity of the pulses. By reducing the pulse intensity it was found that the lowest optical power the circuit would operate at was $187\mu\text{W}$, at a pulse frequency of 245 Hz.

The three voltage levels seen on the output voltage trace coincide with the three operating points A, C, and D that occur in the operating cycle of the circuit seen in Fig. 8.4. The point D results in the reset output voltage value of 0.12V seen in Fig. 8.5 which occurs when R is in the high voltage state (6V), and \bar{R} is in the low voltage state (0V). While in this state the circuit is unaffected by optical input S. When R is in the low voltage state (0V), and \bar{R} is in the high voltage state

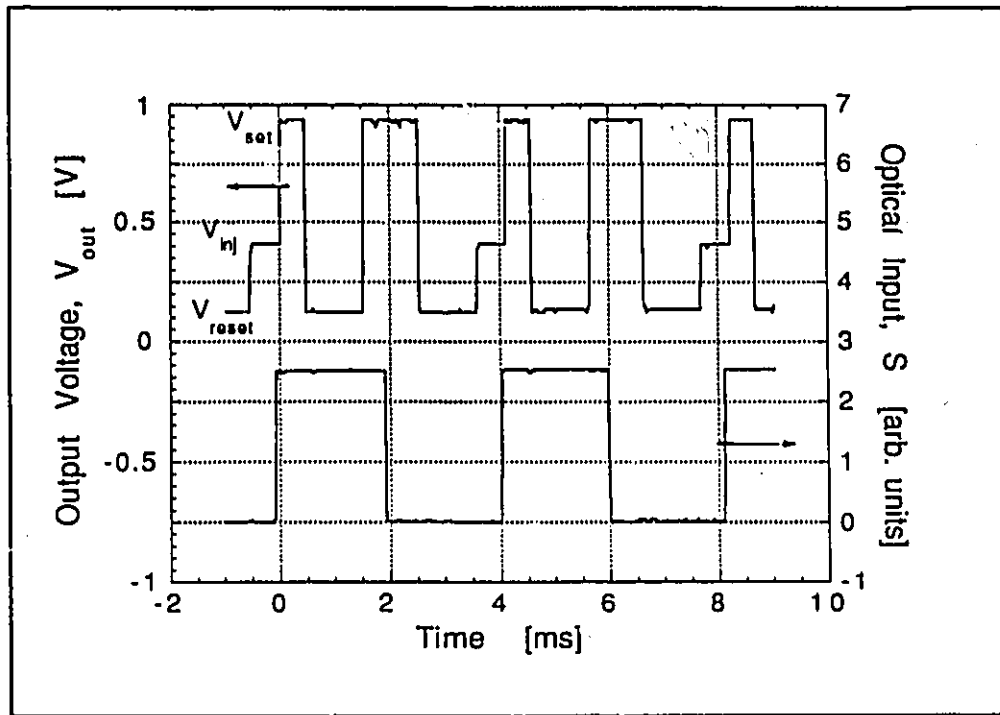


Figure 8.5. The oscilloscope trace of the voltage states, V_{out} , of the RS flip-flop in response to the optical input, S . Various voltage levels of the RS flip-flop's output are illustrated on the trace including V_{Reset} , the output with no injection and the bypass module turned on, V_{inj} , the output with electrical injection but no optical input, and V_{Set} , the output with both electrical injection and optical injection.

(6V), the circuit output becomes dependent on optical input. If the DOES is not illuminated, the optoelectronic switch will remain in the electrically injected state associated with the point A resulting in the injection output voltage value of 0.42 V. When the DOES is illuminated the operating point of the optoelectronic switch module will move to point C resulting in the set voltage value of 0.93 V.

The optical turn on time of the optoelectronic switch module is depicted in Fig. 8.6. The upper voltage trace is the output voltage of the circuit, and the lower voltage trace is the voltage at the \bar{R} input. The first transition observed in the output

voltage of the circuit is due to a phase offset between the triggered pulse generators producing the electrical inputs R , and \bar{R} . In this case, the carrier injector module has been activated before the current bypass module was deactivated. For this particular trace, the DOES was continuously illuminated so the optical turn on time of the switch is the time delay between the rising edge of the lower trace representing \bar{R} and the large transition seen in the output voltage trace. The turn on time was approximately $4.6\mu\text{s}$ which is limited by parasitic RC elements associated with the circuit and the test set-up.

The use of depletion mode Si/SiGe HFETs in this circuit presented some design difficulties. Since the HFETs were still 'on' with a zero volt bias at the gate, some carrier injection was occurring even when the carrier injector module was to have been deactivated. This injected current added to the emitter current of the DOES in the optoelectronic switch module. As a result, the reset output voltage of the circuit was higher than the expected output voltage of the optoelectronic switch in its OFF-state. In addition, the bus voltage was chosen to be 6V to optimize the use of the DOES characteristics. This meant that when the inputs were 0V the HFETs had a gate bias of approximately -6V not including the effects of resistors R_2 and R_3 . This large negative bias resulted in large gate leakage currents at these inputs. Both these problems could be avoided by using enhancement mode HFETs. This would result in a much lower reset output voltage, and eliminate the need for resistor R_3 to reduce the gate bias in the circuit design.

The devices used in this demonstration did not have optimal I-V characteristics. In spite of this, an optoelectronic function was demonstrated and many of the design issues have been revealed. With proper design optimization, the circuit could be made to operate with standard TTL (0-5V) specifications and with high frequency limited only by the turn-on time of the DOES.

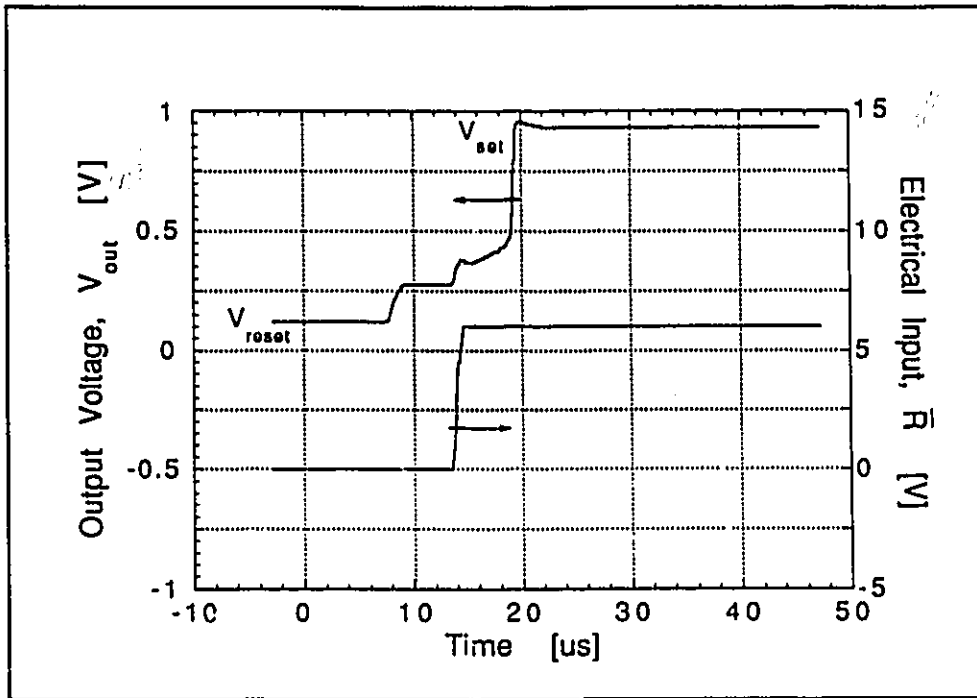


Figure 8.6. The oscilloscope trace of the transition of the RS flip-flop from the low to the high state (V_{Reset} to V_{Set}) in response to a change in the electrical injection current. In this trace, the optical input was continuously high.

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CHAPTER 9

CONCLUSIONS

In this thesis, a number of achievements have been made towards fabricating, characterizing, and modeling Si/Si_{1-x}Ge_x -based inversion-channel devices. Bistability in the dc electrical characteristics of the Si/Si_{1-x}Ge_x -based DOES has been realized with switching voltages from 3-7V, switching currents on the order of 1mA, and holding currents and voltages which depend on oscillatory behavior in regime of negative differential resistance.

Transistor action has been seen in the HFET with peak transconductance (8mS/mm) which exceeds the largest value reported to date in p-channel metal-semiconductor transistors using Si/Si_{1-x}Ge_x alloys. However, this value is still smaller than state-of-the-art Si or Si/SiGe-based p-channel MOSFETs.

The advantage of Si/Si_{1-x}Ge_x -based inversion-channel technology may lie with increased circuit functionality derived by integrating on a common heterostructure devices with distinct abilities. Integration of functionalities was demonstrated by implementing the Reset-Set Flip-Flop in chapter 8.

Hopefully, from this work a more clear understanding of Si/Si_{1-x}Ge_x -based inversion-channel devices has emerged and with it a better ability to evaluate the potential of this technology . However, a number of important issues remain on speculative ground. Further research is required to understand fully how Si/Si_{1-x}Ge_x heterostructures can be incorporated, to best advantage, into the modern-day CMOS process. The reproducibility and reliability of Si/Si_{1-x}Ge_x

-based devices has not yet been addressed. Finally, modeling indicates that devices fabricated using the inversion-channel heterostructure will be quite sensitive to small variations in the magnitude of the doping and layer thickness. This sensitivity might be a detriment to manufacturability of circuits based on this technology.

APPENDIX A: CURRENT COMPONENTS

A.1 Barrier Thermionic Currents

The electron current which surmounts the barrier and flows into the active region is expressed as:

$$J_{nb} = J_{nbo} \left[\exp\left(\frac{\Delta V_b}{V_t}\right) - \exp\left(\frac{\Phi_{To} - \Phi_T}{V_t}\right) \right] \quad (\Lambda 1)$$

where

$$\Delta V_b = V_{bo} - V_b$$

$$\Phi_{To} = \Phi_{SiGeo} + \Phi_{Sio} + \Delta E_c$$

$$\Phi_T = \Phi_{SiGe} + \Phi_{Si} + \Delta E_c$$

$$J_{nbo} = \frac{4 p q m_n V_t^2}{h^3} \exp\left[-\frac{(\Phi_T + V_{bo})}{V_t}\right]$$

The hole current which escapes the SiGe well and forward biases the barrier to charge sheet junction is given similarly by:

$$J_{pb} = J_{pbo} \left[\exp\left(\frac{\Delta V_b + \Delta E_{Fpj} - \Delta E_{Fpjo}}{V_t}\right) - 1 \right] \quad (\Lambda 2)$$

$$J_{pbo} = \frac{4 p q m_p V_t^2}{h^3} \exp\left[-\frac{(V_{bo} + \Delta E_v - \Delta E_{Fpjo})}{V_t}\right]$$

A.2 Recombination Currents

At the n-n heterojunction and the p-n junction some current will be lost to recombination. At the barrier:

$$J_{rb} = J_{rbo} \left[\exp \left(\frac{\Delta V_b + \Delta E_{Fpj} - \Delta E_{Fpjo}}{2V_t} \right) \right] \quad (A3)$$

$$J_{rbo} = \frac{q W_b n_{ib}}{\tau_{rb}}$$

where τ_{rb} is the recombination lifetime at the barrier. From the point of view of device simulation, this is a critical constant. Values which are too long will inhibit 'S'-shaped I-V characteristics. Values which are too short will result in very large switching currents and switching voltages.

The current which recombines in the active region is simply the difference between what enters the active region from the collector and that which enters the depletion layer at the n-n hetero-interface.

$$J_{ra} = J_{pd} - J_{pa} \quad (A4)$$

Recombination at the p-n junction is represented by:

$$J_{rj} = J_{rjo} \left[\exp \left(\frac{V_j}{2V_t} \right) - 1 \right] \quad (A5)$$

$$J_{rjo} = \frac{q (n_{is} N_{Si} + n_{iSi} N_s) W_j}{2 \tau_{rj} (N_s + N_{Si})}$$

where n_{iS} and n_{iSi} are, respectively, the intrinsic carrier densities in the substrate and Si-part of the active region, N_s and N_{Si} are the dopant concentrations in the substrate and Si-part of the active region, respectively, τ_{rj} is the recombination lifetime in the p-n junction, and W_j is the p-n junction width, given by:

$$W_j = \left(\frac{\epsilon_{Si} N_s}{\epsilon_s N_{Si}} + 1 \right) \sqrt{\frac{2 V_a \epsilon_{Si} \epsilon_s N_{Si}}{q N_s (\epsilon_{Si} N_{Si} + \epsilon_s N_s)}} \quad (A6)$$

and
$$V_a = E_{gSiGe} + \Delta E_v - \Delta E_{Fn} - V_j - \Delta E_{Fps}$$

A.3 Generation Current

Current generated in the depleted part of the active region is given by:

$$J_g = \frac{q n_{iSiGe} X_d}{\tau_g} \left[1 - \exp \left(\frac{\Delta E_{Fpj} + E_{gSi} - \phi_T - \Delta E_{Fn}}{2 V_t} \right) \right] \\ + \frac{q t_0 P_{in}}{h\nu} [1 - \exp(-\alpha_{SiGe} W_{SiGe})] \\ + \frac{q t_0 P_{in}}{h\nu} [1 - \exp(-\alpha_{Si} (X_d - W_{SiGe}))] \quad (A7)$$

where t_0 is the transmission coefficient of the emitter to the incident light, P_{in} is the optical power incident on the emitter, $h\nu$ is the energy of the incident light, α_{SiGe} and α_{Si} are the absorption coefficients of the incident light in the SiGe- and Si-part of the active region, respectively.

A.4 Diffusion Currents

The diffusion of excess holes from the p-n junction is given by:

$$J_p(x) = q D_p \frac{d\Delta p}{dx} \quad (\text{A8})$$

$$\Delta p(x) = A_1 \exp\left(\frac{-x}{L_p}\right) + A_2 \exp\left(\frac{x}{L_p}\right) \quad (\text{A9})$$

where $\Delta p(x)$ is the excess hole concentration at a distance x from the edge of the depletion region into the zero field section of the active region.

$$J_{pa} = J_p(0) = q D_p \left[\frac{A_2 - A_1}{L_p} \right] \quad (\text{A10})$$

where D_p and L_p are the hole diffusion coefficient and length, respectively, in the active region, and

$$A_1 = \frac{\left\{ N_{vSi} \exp\left(\frac{\Delta E_{Fpj} - \phi_T}{V_t}\right) - p_{no} \right\} \exp\left(\frac{W_{al}}{L_p}\right) - p_{no} \left[\exp\left(\frac{V_j}{V_t}\right) - 1 \right]}{2 \sinh\left(\frac{W_{al}}{L_p}\right)} \quad (\text{A11})$$

$$A_2 = N_{vSi} \exp\left(\frac{\Delta E_{Fpj} - \phi_T}{V_t}\right) - p_{no} - A_1 \quad (\text{A12})$$

$$p_{no} = \frac{n_i Si^2}{N_{aSi}}$$

where $W_{a1} = W_{Si} + W_{SiGe} - X_d$ = the width of neutral section of the active region, N_{vSi} is the effective density of states of the valence band in the active region, and N_{aSi} is the ionized donor concentration in the active region.

$$J_{pd} = J_p(W_{a1}) = q D_p \left[\frac{A_2}{L_p} \exp\left(\frac{W_{a1}}{L_p}\right) - \frac{A_1}{L_p} \exp\left(-\frac{W_{a1}}{L_p}\right) \right] \quad (A14)$$

$$J_{nd} = J_{ndo} \left[\exp\left(\frac{V_j}{V_t}\right) - 1 \right] \quad (A15)$$

$$J_{ndo} = \frac{q D_n n_{is}^2}{L_n N_s}$$

where D_n and L_n are the electron diffusion coefficient and length, respectively, in the substrate.

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