THE CHARACTERIZATION OF THIN HEAVILY DOPED LAYERS IN SILICON

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ABSTRACT

The electrical characteristics of a thin heavily doped layer in silicon were determined.

A p^+ 200 Ω/□ 3 μm junction depth boron diffusion in a 2 Ω cm n-type phosphorous doped substrate was considered a typical thin heavily doped layer. This layer is of considerable practical importance being a standard base and resistor diffusion in planar processing.

To completely characterize the heavily doped layer, it was necessary to study the layers on either side; substrate and thermal oxide; and their interfaces with the heavily doped layer. The resultant structure was examined by means of MOS C-V, oxide leakage and breakdown, Hall effect, p-n junction characterization, and differential sheet resistivity using anodic sectioning and a four-point probe. These tests yielded the impurity profile, the transport and recombination properties of the substrate, the dielectric constant, thickness, breakdown field and leakage current of the oxide and the properties of the substrate diffused layer interface. However, the properties of the heavily doped layer and its interface with the oxide were still unknown. To find them, an experimental procedure utilizing a new test structure was introduced.

The test structure consisted of an MOS capacitor formed over a heavily doped layer. The layer in turn formed one side of a p-n junction diode. The resultant structure was an MOS capacitor-emitter transistor (MOSCET). In operation, the p-n junction was reverse biased and became a minority carrier collector, while the MOS capacitor was biased into

inversion for a controlled length of time during which minority carriers were generated and formed the inversion layer. A voltage pulse applied to the MOS capacitor caused it to release minority carriers from the inversion layer. The carriers were transported across the layer under the combined influence of diffusion, and internal fields to the p-n junction where the charge that had not recombined during transit was collected.

The theoretical behaviour of the MOSCET was determined. First a MOS capacitance program was used to determine the inversion charge as a function of the bias voltage. Then a model of the device was developed to explain the transient response when no inversion charge was present. A finite difference formulation was used to account for the minority carrier transport across, and recombination in, the diffused layer. A time dependent release mechanism was introduced as a boundary condition which included values calculated in the non-inversion response. The result was a self consistent model of the MOSCET which also agreed with the other experimental data available.

The MOSCET can be used to study two other phenomena as well as the characterization of thin heavily doped layers. This structure supplies the only direct confirmation of the relationship between inversion charge and bias voltage on the MOS capacitor. A study of the avalanche properties of p-n junctions can be made, at very low multiplication values, with the MOSCET since the number of injected carriers is so well known.

Measurements on the MOSCET yield the following properties of

thin heavily doped layers.

(1) The minority carrier generation lifetime near the interface.

(2) The generation centre energy level.

(3) The average minority carrier recombination lifetime in the layer.

(4) The transport properties across the layer.

(5) The inversion potential.

(6) The fixed oxide charge density.

(7) The insulator stability.

These properties combined with those determined by the other techniques provide the most complete electrical characterization of the thin heavily doped layer to date.

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CHAPTER 1

INTRODUCTION

Since the discovery of the transistor by Bardeen and Brattain[1] in 1948 the electrical properties of semiconductor layers have been of concern to the device designers and process engineers. Initially the work concentrated on producing better material of higher purity, with fewer crystal defects and more controlled means of introducing impurities; first by alloying, then diffusion and now epitaxy and ion implantation. At first the efforts were concentrated on characterizing the lightly doped regions which dominated the device operation. With closer specifications and much better control of the properties of the lightly doped regions the heavily doped regions have become much more significant. At present the properties of thin heavily doped layers are of great importance throughout the semiconductor industry; in large scale integration the shallow heavily doped emitter is critical; in power devices the lifetimes in the heavily doped layers limit the operation and in FET's the heavily doped source and drain are of major significance.

To completely characterize a thin heavily doped layer is not a simple matter. It is necessary to know not only the properties of the layer itself but also the properties of its interfaces with the neighbouring layers and to determine these, it is necessary to evaluate the properties of these layers as well. With a semiconductor, three different types of neighbouring layers are possible; another semiconductor, an

insulator or a metal. In this work only the first two will be considered.

To completely characterize a thin heavily doped layer it is necessary to know

(1) Impurity Distribution

(2) Recombination-Generation Lifetimes and Activation Energies

  (a) at the dielectric-semiconductor interface

  (b) in the heavily doped layer

  (c) in the substrate

(3) Transport Properties

  (a) in the dielectric

  (b) in the heavily doped layer

  (c) in the substrate

(4) Dielectric-Semiconductor Interface Properties

  (a) surface potential

  (b) fixed oxide charge

  (c) fast surface states

  (d) insulator stability

(5) Heavily Doped Layer-Substrate Interface Properties

  (a) diode characteristics

Three basic techniques are available for determining the impurity profile; C-V, spreading resistance and sectioning. C-V is virtually useless in heavily doped material since only a very short distance can be profiled before the semiconductor breaks down. This techniques can be combined with sectioning to give a complete profile but is not often used.

The spreading resistance probe is very good for deep profiles since it is speedy and does not require a large area. However, the minimum step is coarse so it is not often used for shallow layers. Sectioning techniques are time consuming and require a large area but for shallow layers this is the best technique. Differential sheet resistivity is the best method to determine the electrically active profile. In fact, if the Hall effect is used to measure the resistivity, the transport properties parallel to the surface can be determined at the same time.

The generation lifetime at the dielectric-semiconductor interface and in the semiconductor below the surface are normally determined by pulsed MOS capacitance measurements. However, for heavily doped layers the capacitance change is so small that this method can not be used. Photoconductive decay is a common method of determining recombination lifetime in semiconductors but can not be used in this case because the lifetimes are too short and the p-n junction isolation, which is essential, can not be maintained in thin layers under photo excitation. Diode recovery measurements yield the lifetime in the substrate and its activation energy can be determined from the temperature dependence of the reverse current of the diode.

The transport properties in the dielectric can be determined from the MOS capacitor leakage current as a function of bias voltage. The Hall effect coupled with sectioning will yield the transport properties of the heavily doped layer parallel to the surface. However, the transport properties across the layer can not be determined. Simple Hall effect will give the transport properties of the substrate.

The dielectric-semiconductor interface properties are usually determined using an MOS capacitor. As previously mentioned, for a heavily doped layer, the capacitance changes are so small that the properties can not be accurately determined.

The interface between the heavily doped layer and the substrate forms a diode and if the diode is characterized, then the interface properties are known.

These techniques will not yield the properties of the heavily doped layer or its interface with the dielectric. Consequently, a new technique utilizing a new device structure must be introduced.

The test structure consists of an MOS capacitor formed over the thin heavily doped layer to be evaluated. This layer is of the opposite conductivity type to the substrate and a p-n junction is formed. The resultant structure is an MOS capacitor-emitter transistor (MOSCET). In operation, the p-n junction is reverse biased and becomes a minority carrier collector, while the MOS capacitor is biased into inversion for a controlled length of time during which minority carriers are generated and form the inversion layer. A voltage pulse applied to the MOS capacitor causes it to release minority carriers from the inversion layer. These carriers move under the combined influence of internal fields and diffusion to the p-n junction where they are collected. However, as the charge crosses the base, recombination occurs and only a fraction of the carriers initially released arrive at the collector to be detected.

By studying the charge collected as a function of the different variables both generation and recombination lifetimes, the generation

activation energy, the transport properties across the layer and all the semiconductor-insulator interface properties, except fast surface states density can be determined.

It was decided to select one thin heavily doped layer and study it in detail using all of the techniques possible. The layer selected was a p^+ 200 Ω/□, 3 μm junction depth boron diffusion in an n-type substrate with a thermal oxide on the surface. This layer is of considerable practical importance being a standard base and resistor diffusion in planar processing.

CHAPTER 2

DEVICE FABRICATION

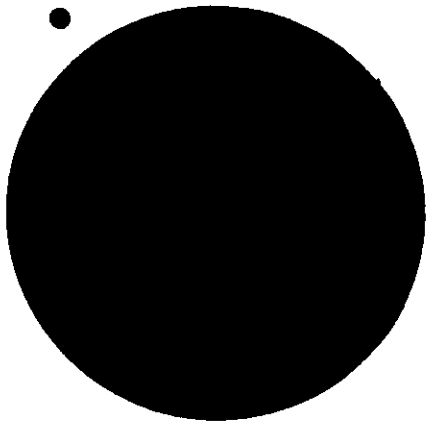
2.1 Processing

The p^+ diffused layer to be studied was fabricated at the Solid State Device Department of Westinghouse Canada.

The substrate was n-type phosphorous doped 2 Ω-cm <111> silicon. The wafer was cleaned using hydrogen peroxide as proposed by Kern.[2] The actual cleaning procedure was a rinse in 30% H_2O_2 in H_2SO_4 followed by a dip in 10% HF and then a dip in hot HNO_3.

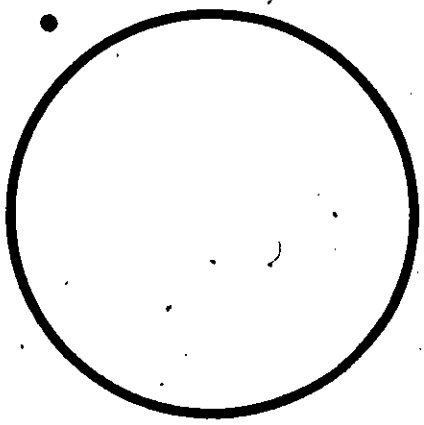
An oxide was grown on both sides of the wafer at 1100°C in oxygen saturated with water at 95°C for 1 hour. The resulting 0.75 μm layer acted as a mask during the diffusion processes.

The mask of Fig. 2.1 was used to define the window in the oxide through which the boron was diffused. This was accomplished by covering the wafer with photoresist, placing the mask in position and then shining ultraviolet light to expose the photoresist not covered by the mask. The exposed photoresist shielded the oxide from the subsequent HF etch but the oxide which had been under the mask was etched away and a window was opened for the subsequent diffusion. The previously outlined cleaning procedure was employed to remove the exposed photoresist prior to the diffusion. The boron diffusion was a two step process. First was the deposition at 900°C from a gas of 1 part 1% diborane in argon, 1 part O_2 and 200 parts N_2 for 40 minutes. This was followed by a drive at 1200°C in pure O_2 for 40 minutes which redistributed the boron and formed a dry



F1/B

Figure 2.1 The mask used to define the boron diffusion (x 40)



F1/ C

Figure 2.2 The mask used to locate the base contact (x 40)

thermal oxide over the diffusion.

The masking oxide was then stripped from the back of the wafer in preparation for the phosphorous diffusion. The phosphorous was deposited at 1050°C from a gas consisting of 30 parts 1% phosphine in argon, 920 parts N_2 and 50 parts O_2 for 20 minutes and then driven, at the same temperature, for 90 minutes in pure O_2. The purpose of the phosphorous treatment was to form an n^+ layer on the back of the wafer and to form a phosphosilicate glass over the oxide. The n^+ layer acted as a getter for transition elements (particularly gold)[3] and improved the back contact while the phosphosilicate glass acted as a getter for any sodium ions present in the oxide.[4]

The mask of Fig. 2.2 was used with the photoresist technique to open a contact pattern to the p^+ layer. The top of the wafer was covered by a layer of aluminum 1 μm thick which had been evaporated from a tungsten filament source. The mask of Fig. 2.3 was used with photoresist to define the metalization pattern. In this case it was the unexposed photoresist which shielded the aluminum.

The final processing step was an anneal at 450°C in 75% dry N_2 and 25% N_2 saturated with water at room temperature for 30 to 40 minutes to reduce the surface state density.[5]

The processing was now complete and Fig. 2.4 shows a photograph of the top of the device on which the metalization pattern can be clearly seen. Figure 2.5 is a cross-section of the device.

Three additional wafers, which received blanket diffusions, were processed with the devices. These were used in destructive measurements

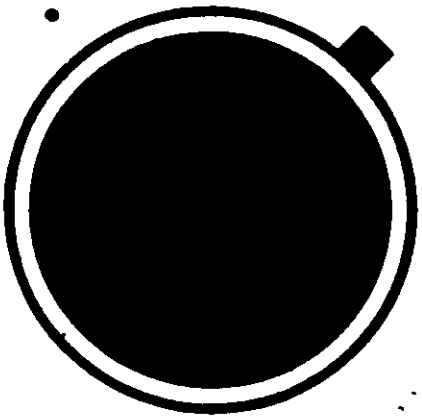


Figure 2.3 The mask used to define the metalization pattern (x 40)

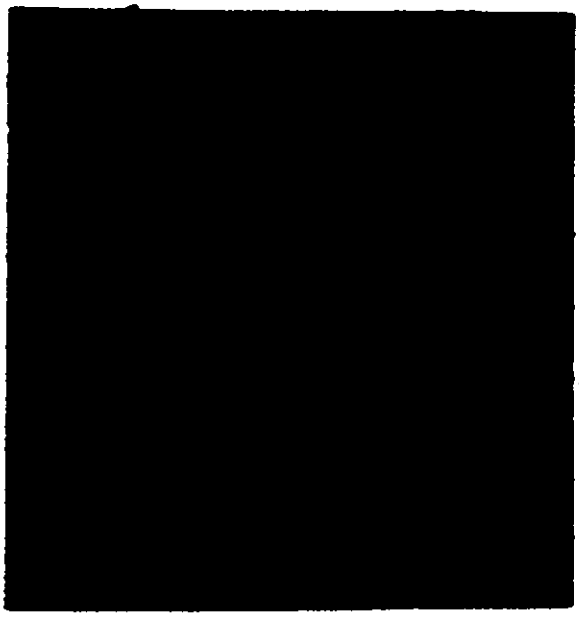
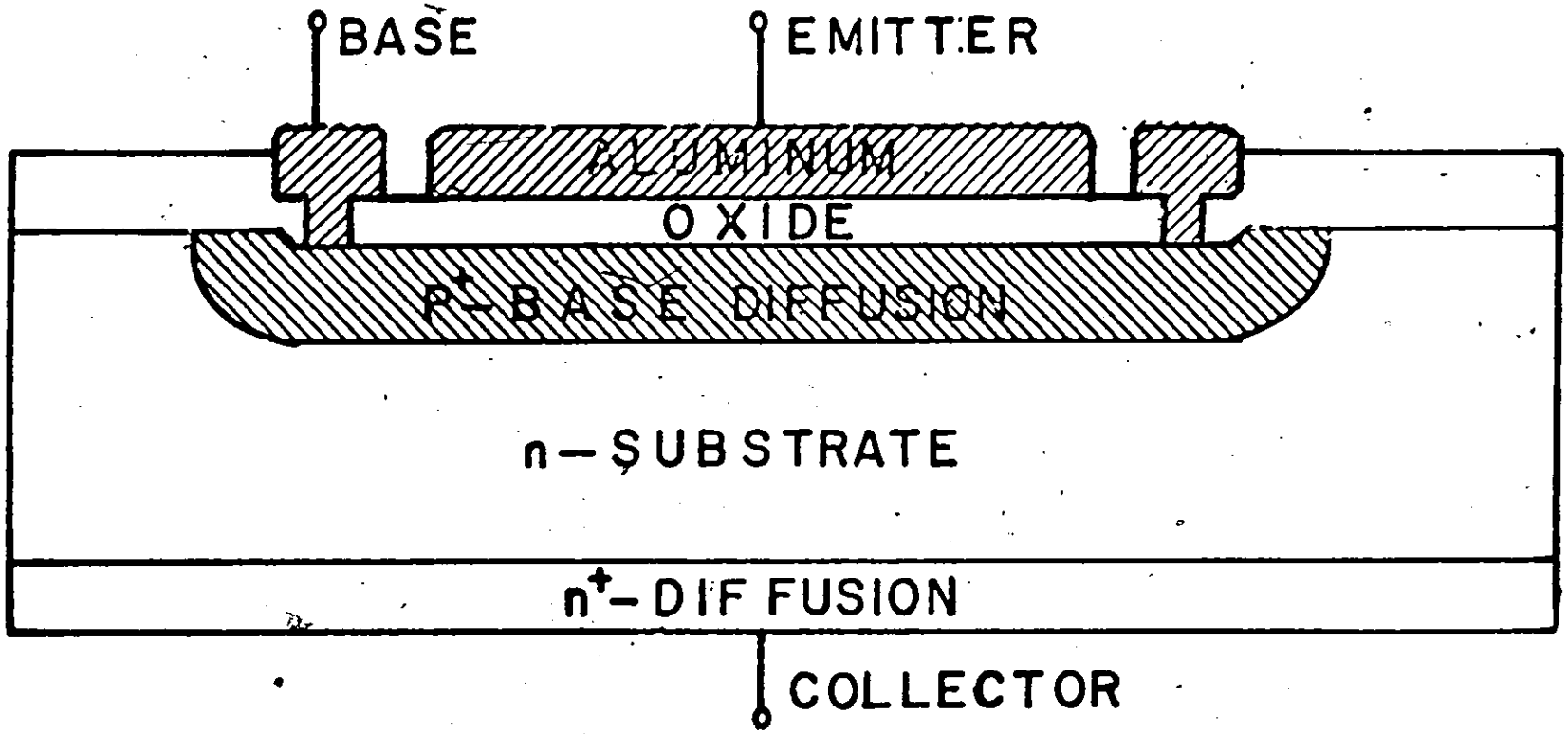


Figure 2.4 Photograph of the completed device (x 40)



MOS CAPACITOR-EMITTER TRANSISTOR (MOSCET) STRUCTURE

Figure 2.5 A cross-section of the test structure

of impurity distribution and oxide thickness.

2.2 Preliminary Tests

The completed wafers were placed on a probe table and a random sample tested using a curve tracer for three criteria

(1) Oxide breakdown of greater than ±50 V

(2) No measurable current on the curve tracer when a reverse bias of 15 volts was applied to to the p-n junction diode

(3) High reverse breakdown voltage for the diode

Since all devices tested satisfied the first two conditions and most had satisfactory reverse breakdown, it was decided to simply mount the devices without selective testing.

The wafers were scribed and the chips mounted on 4 pin TO-5 headers by means of the gold-silicon eutectic at approximately 400°C. The device contacts were bonded to the appropriate header pins by a thermal compression nail head bonder. The headers were then capped and hermetically sealed in an atmosphere of dry nitrogen.

The devices were once more tested on the curve tracer using the same criteria as before. The results are presented in Table 2.1.

The devices were all graded for diode and MOS capacitor quality. The MOS devices with open circuits were attributed to bonding failures while the short circuits indicated complete oxide breakdown. Certain devices started as good capacitors but broke down at less than 50 volts bias. One group appeared which had not been expected. These were devices where

TABLE 2.1 INITIAL TEST RESULTS

P-N / MOS	Reverse >70 V	Breakdown 20-70 V	Voltage <20 V	High Reverse Current	Open Circuit	# and % in each MOS Group
Short Circuit	22 (35.5) (41.5) (18.6)	12 (66.7) (22.6) (10.2)	14 (50) (26.6) (11.9)	3 (50) (5.6) (2.5)	2 (50) (3.8) (1.7)	53 (45)
Schottky Barrier	19 (30.7) (67.8) (16.1)	2 (11.1) (7.2) (1.7)	6 (21.4) (21.4) (5.1)	1 (16.7) (3.8) (0.8)		28 (23.8)
Good	16 (25.8) (55.2) (13.6)	4 (22.2) (13.8) (3.4)	7 (25) (24.2) (5.9)	2 (33.3) (6.9) (1.7)		29 (24.6)
Failed during test	3 (4.8) (75) (2.5)		1 (3.6) (25) (0.8)			4 (3.4)
Open Circuit	2 (3.2) (50) (1.7)				2 (50) (50) (1.7)	4 (3.4)
# and % in each P-N Group	62 (52.5)	18 (15.2)	28 (23.8)	6 (5.1)	4 (3.4)	118

Example: Number in group 22 (35.5) % of P-N group

% of MOS group (41.5) (18.6) % of Total

the oxide was partially broken down and the result was a Schottky diode. The good devices were capacitors for which the oxide had not broken down at ±50 volts bias. The diodes with open circuits and high leakage currents were segregated and the rest evaluated according to their reverse breakdown voltage.

Two conclusions were drawn from these tests:

(1) The nail head bonder has an extremely detrimental effect on the MOS capacitor. The thin oxide layers were seriously damaged on approximately 70% of the devices by this operation.

(2) There appears to be no correlation between the quality of the p-n junction and the MOS capacitor.

The subsequent work was concentrated on the devices with good MOS capacitors and diode breakdown voltage greater than 70 volts.

CHAPTER 3

Conventional Characterization

3.1 Introduction

The thin heavily doped layer to be characterized is part of a more complex system and cannot be studied in isolation. In the test structure the heavily doped layer is sandwiched between the oxide and the substrate. To completely characterize the shallow heavily doped layer it is necessary to know the properties of the oxide, the substrate and their interfaces with the layer.

In this chapter, conventional experimental procedures were utilized to determine the electrical characteristics of the structure.

3.2 The MOS Capacitor

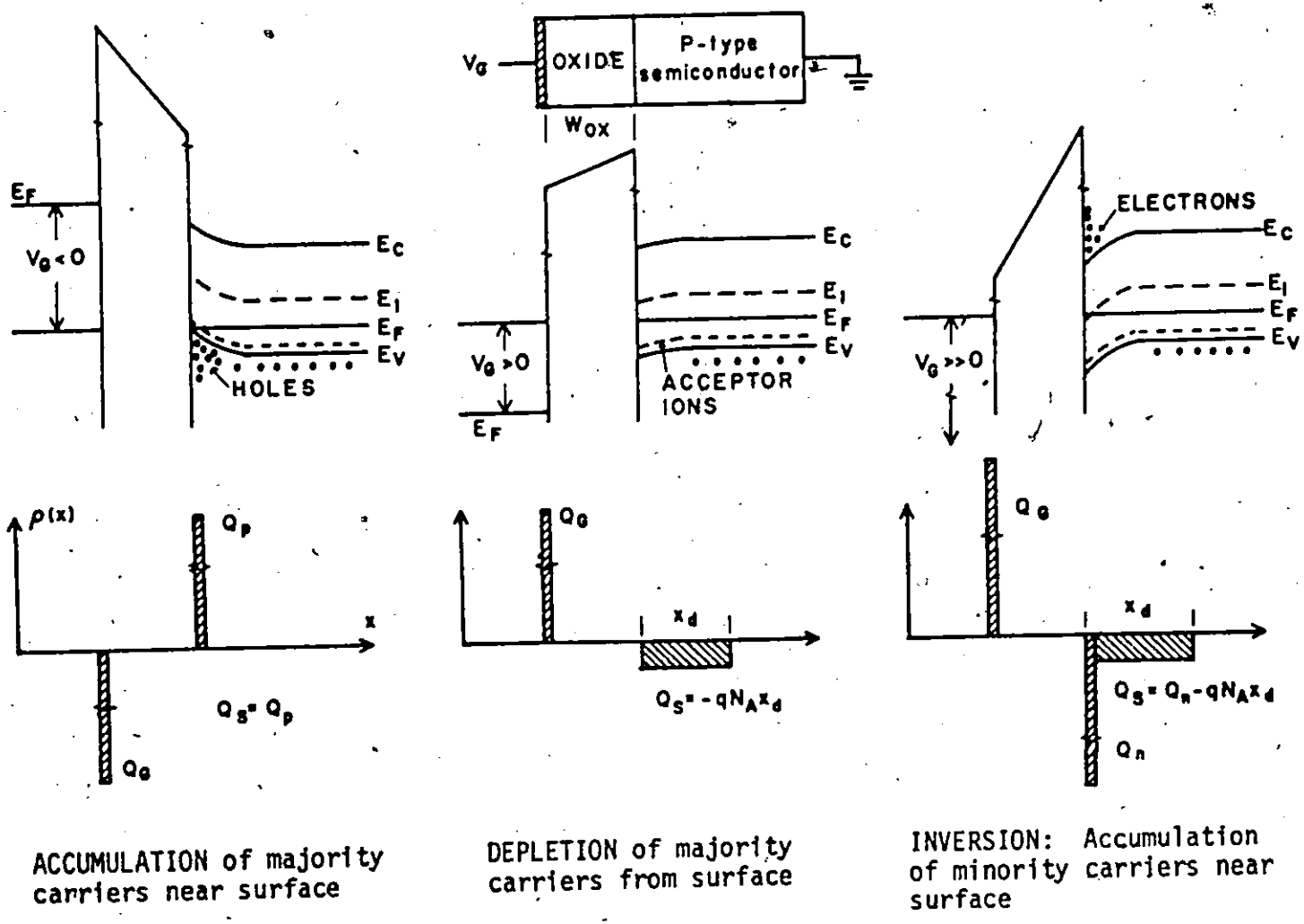
The metal-oxide-semiconductor (MOS) capacitor is the most useful device in the study of semiconductor surfaces. Not only does it yield the properties of the oxide-semiconductor interface but also many of the properties of the semiconductor layer beneath the capacitor.

Comprehensive reviews of the subject are found in books[6,7] review articles[8,9,10] and a bibliography.[11]

3.2.1 Theory of Operation

The MOS capacitor is fundamentally simple. When a potential is applied across the MOS capacitor the energy bands bend and the charge in

the semiconductor redistributes. Figure 3.1 shows the results for the important bias conditions while Fig. 3.2 shows the small signal capacitance as a function of the bias voltage (a C-V curve). When a negative bias voltage is applied to the metal (Fig. 3.1(a)), the semiconductor bands bend up, the holes are attracted and accumulate at the surface. Then the capacitance is just that of the oxide, C_{ox}. For a small positive bias (Fig. 3.1(b)), the bands bend down, the holes are repelled and a depletion layer is formed with a density of fixed impurity charge equal to the doping density (N_A). This layer is equivalent to the dielectric of another capacitor in series with C_{ox} reducing the total capacitance (see Fig. 3.2). To this point, the only mobile charge considered is majority carriers which respond with the dielectric relaxation time ($\simeq 10^{-13}$ s), consequently no frequency effects are observed. As the bias is increased, the bands bend further, more electrons are attracted to the surface and an inversion layer forms (Fig. 3.1(c)). Beyond a certain value of bias, all further increases in voltage only increase the charge in the inversion layer and the depletion layer width remains constant. The formation of the inversion layer is dependent on the generation of minority carriers, a relatively slow process and the C-V curve of Fig. 3.2 becomes multivalued. When the inversion charge is in equilibrium with the bias and the test frequency, the capacitance returns to C_{ox} since effectively all of the charge is at the surface in the inversion layer. When the inversion charge is in equilibrium with the bias but cannot respond with the small signal test frequency, the capacitance becomes a constant equal to the series combination of the maximum depletion layer capacitance and C_{ox}. When the bias is applied so rapidly



ACCUMULATION of majority carriers near surface

DEPLETION of majority carriers from surface

INVERSION: Accumulation of minority carriers near surface

Figure 3.1 Energy bands and charge distribution in a MOS structure under various bias conditions, in the absence of surface states and work function difference (After Grove et al Ref. 12)

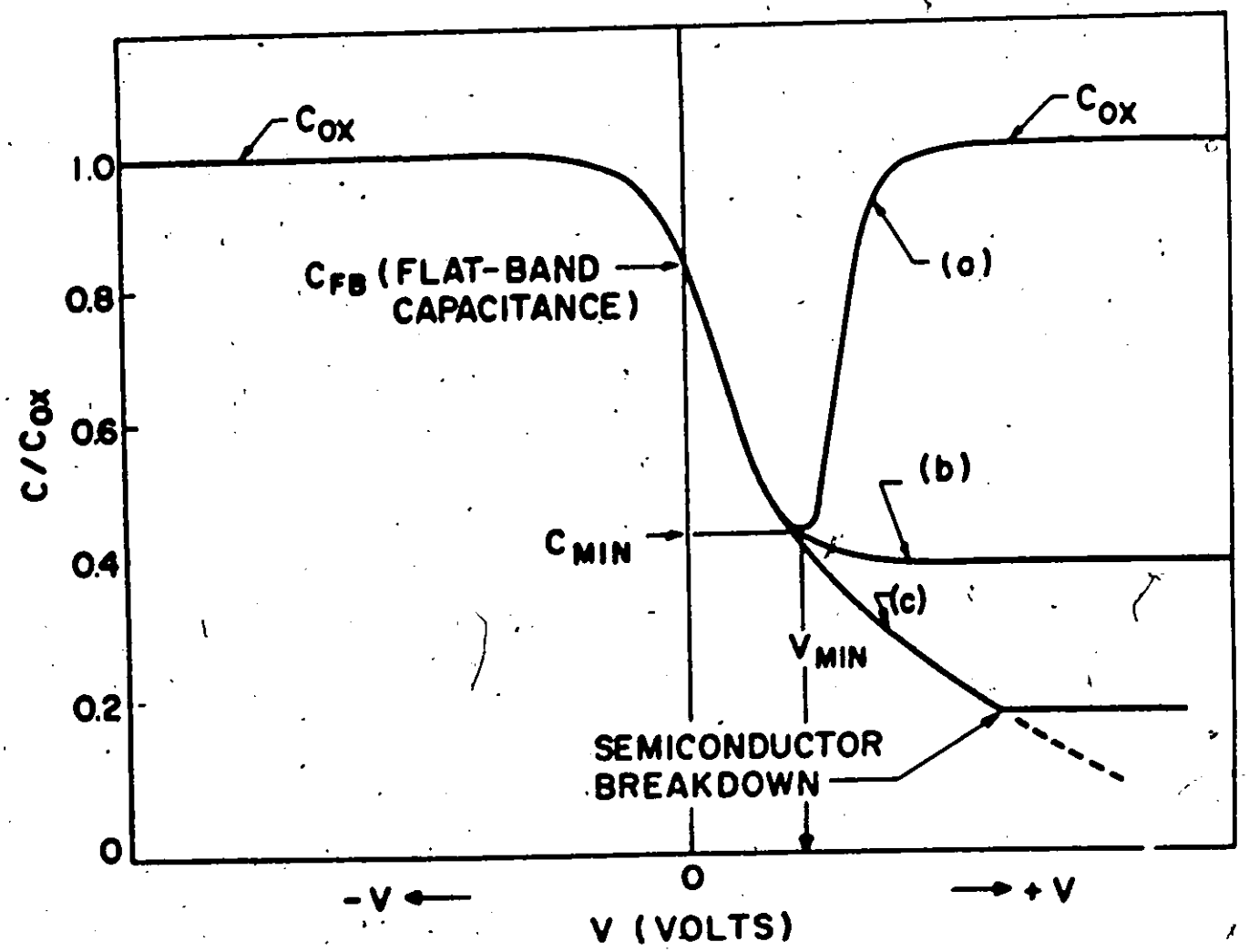


Figure 3.2 MOS capacitance-voltage curves: (a) low-frequency, (b) high-frequency, (c) deep depletion (After Grove et al Ref.12)

that the inversion charge cannot be generated fast enough to maintain equilibrium, the MOS capacitor continues into deep depletion.

While this description accounts for the qualitative behaviour of the MOS capacitor as a function of bias voltage, to determine the exact relationship it is necessary to solve Poisson's Equation

$$\frac{\partial^2 \psi}{\partial x^2} = -\frac{\rho(x)}{\epsilon_o K_s} \qquad 3.2.1$$

where ψ is the electrostatic potential, ϵ_o is the permittivity of free space (8.86×10^{-14} f/cm), K_s is the relative dielectric constant of silicon (11.7)[6] and $\rho(x)$ the charge density is

$$\rho(x) = q(p - n + N_A^- + N_D^+ + N_t^+ - N_t^-) \qquad 3.2.2$$

where q is the charge on the electron (1.6×10^{-19} coulombs), n and p are the free electron and hole densities and N_A^-, N_D^+, N_t^+ and N_t^- are the ionized acceptor, donor and trap densities. A general closed form solution to the equation is not possible but simplified analytic solutions exist for specific regions, depletion[6], and accumulation and inversion.[13] Kingston and Neustadter[14] present a more general solution requiring certain functions which are evaluated using computer generated standard curves. Young[15] extends the solution by determining further curves. The experimental C-V curves are related graphically to the device parameters by a number of authors.[10,16,17]

The computer program of Temple and Shewchun[18] can generate theoretical MOS data. This program employs numerical integration to evaluate Poisson's Equation for full Fermi statistics assuming parabolic bands and the measured impurity profile. The C-V curves can be calculated as a function of

frequency. As well, the non-ideal effects of work function difference, fixed oxide-charge, distributed fast surface states and potential fluctuations can all be considered.

Figure 3.3 shows an ideal theoretical high frequency C-V curve calculated using this program.

3.2.2 Experimental Equipment

A number of different capacitance measuring systems were employed to determine the MOS capacitance.

The Wayne-Kerr B641 was a null system which gave a very accurate value of capacitance (C) and conductance (G) for a test signal of 10^4 radians/s at 4 V p-p. The test frequency and signal level were fixed and the system would not take a bias. Table 3.1 shows the values determined using this bridge.

The Boonton 77 A-R had an analog C output but no value of G. It operated at 1 MHz with a low signal level of 25 mv p-p and would readily take a bias. Table 3.1 shows values measured at biases of +40, 0 and -40 V on this bridge using an offset capacitance of 205 pf.

The Boonton 75 A-SB was a null system which gave a good value of C and a crude value of G. It operated at 1 MHz with a low signal level of 25 mv p-p and would readily take a bias. It was only used as a check on the other methods.

The fourth system which will be referred to as the C-K-C system consisted of a GR 1615A Capacitance Bridge, a GR 1311A Audio Oscillator and a GR 1232A Tuned Amplifier and Null Detector. This system gave very

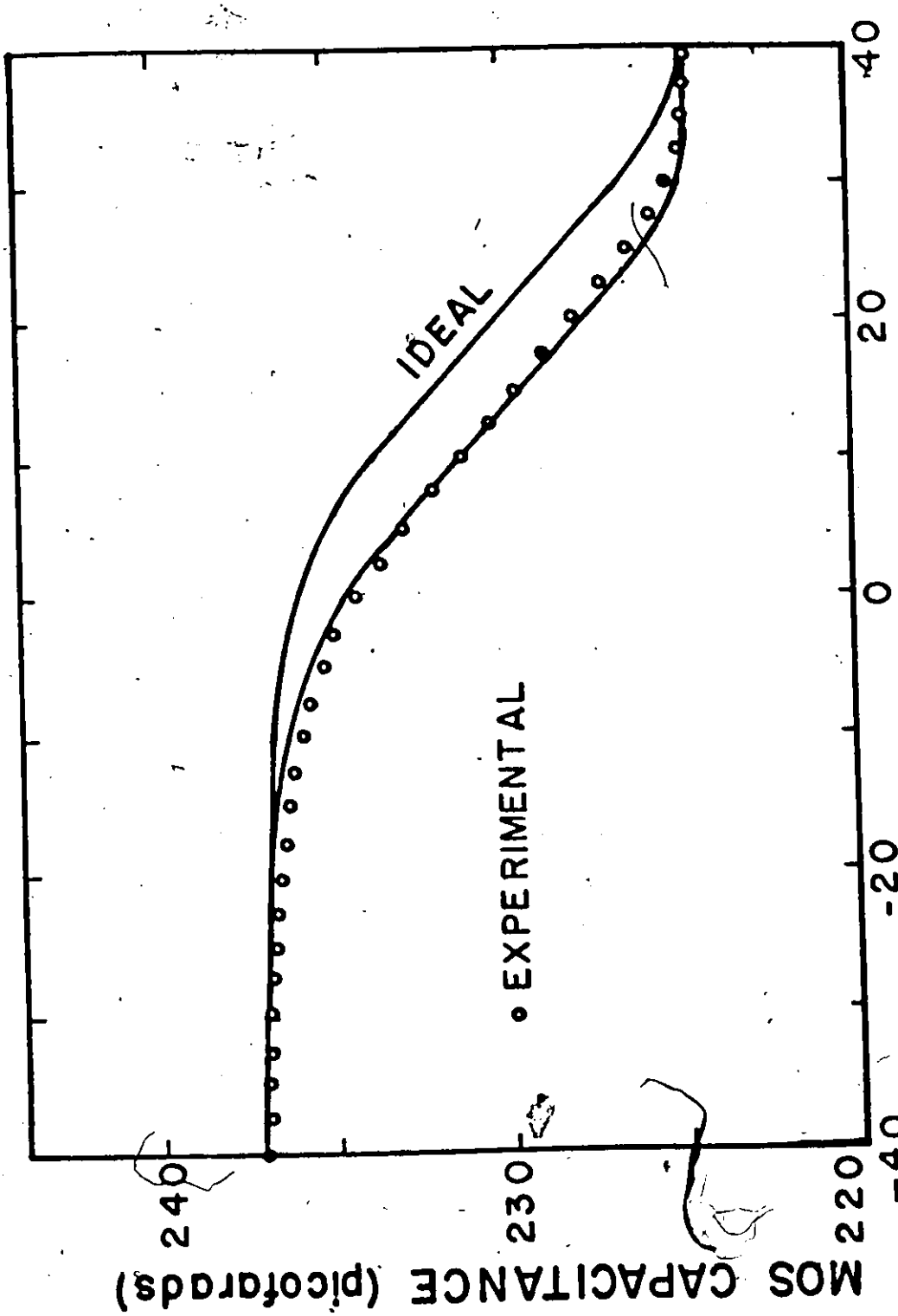


Figure 3.3. Experimental and ideal high frequency C-V curves

TABLE 3.1 MOS CAPACITOR DATA

Device Number	Wayne-Kerr Bridge C pf	Deviation	Cond. 10^{-8} mho	Boontan 77 A-R Capacitance Bridge offset 205 pf capacitance in pf at different bias voltage -40V	0	+40V	Dev.	Dielectric Breakdown Applied Voltage V	Field 10^6 V/cm	Flat Band Voltage Volt	Inversion Potential Volt	Q_{SS} 10^{11} charge carriers/cm^2	n_{SS} 10^{11} charge carriers/cm^2
2	235.07	+2.9	0.03	19.8	30.0	32.6	+2.7	70	4.7	-8.5	32.5	2.79	8.08
3	234.61	+2.4	0.07	19.9	29.5	32.1	+2.2			-9.25	31.5	4.26	7.71
4	237.52	+5.3	0.02	22.3	32.2	35.0	+5.1	70	4.7	-9	30.5	5.73	5.88
5	236.43	+4.2	0.02	21.5	31.2	33.9	+4.0	70	4.7	-7.0	33.5	1.32	7.34
7	231.25	-0.9	0.04	16.0	26.1	28.6	-1.3	65	4.3	-9.5	30.5	5.73	6.61
8	229.58	-3.6	0.02	15.0	24.6	27.3	-2.6	70	4.7	-7.5	32.75	2.42	6.98
9	232.82	+0.6	0.08	17.6	27.5	29.9	0.0	70	4.7	-10.75	29.75	6.83	7.34
10	233.62	+1.4	0.03	19.1	28.6	31.8	+1.9	65	4.3				
11	229.78	-2.4	0.04	15.0	24.9	27.7	-2.2	70	4.7	-8	31.5	4.26	6.88
12	225.78	-6.4	0.06	11.1	20.8	23.6	-6.3	70	4.7	-7.5	31.5	4.26	5.14
13	232.49	+0.3	0.03	17.0	27.1	29.7	-0.2	80	5.3	-6	34	0.59	6.61
14	233.78	+1.6	0.05	18.1	28.4	30.6	+0.7	65	4.0	-8	31.5	4.26	5.88
15	234.15	+2.0	0.05	19.1	28.9	31.4	+1.5	60	4.0				
16	230.54	-1.7	0.11					blew at 60 V.					
17	226.53	-5.7	0.05	10.9	21.6	23.9	-6.0	80	5.3	-7.5	30.5	5.73	3.67
18	231.70	-0.5	0.03	17.8	26.9	30.1	+0.2	80	5.3				
19	234.50	+2.3	0.05	20.0	29.6	32.1	+2.2	60	4.0	-8.25	32.0	3.53	6.98
20	229.65	-2.5	0.05	15.3	24.9	27.8	-2.1	70	4.7	-7.25	33.5	2.06	7.71
21	228.78	-4.4	0.02										
22	229.54	-2.7	0.05	15.6	24.7	27.7	-2.2	55	3.7				
23	235.33	+3.1	0.06	19.9	30.1	33.0	+3.1	70	4.7				
24	234.98	+2.8	0.05	19.9	30.0	32.8	+2.9	70	4.7				
25	233.87	+1.7	0.05	18.8	29.1	31.9	+2.0	75	4.7				
26	219.77		0.03	7.7	16.0	19.8		65	4.3				
27	231.46	+0.7	0.05	17.0	26.8	29.1	+0.8	75	5.0	-8	33.75	1.69	9.18
28	234.61	+2.4	0.03					75	5.0				
29	233.44	+1.2	0.04										
30	226.78	-5.4	0.02	13.1	22.2	25.0	-4.9	80	5.3				
Average or σ	232.2	3.16	0.04	222.40	232.8	234.92	3.09	70	4.7	8.1	31.95	3.70	6.73

accurate measurements of C and G with an adjustable amplitude (usually 25 mv p-p) and an adjustable frequency (most measurements at 10 KHz). This system would readily take a bias. Figure 3.3 shows an experimental C-V curve determined using this system.

The results from all systems agreed within ±1%.

3.2.3 The Impurity Concentration at the Surface of the Silicon

The type and concentration of the dopant in the silicon was determined from the experimental C-V curves. Either the slope of the C-V curve or the difference between C_{ox} and the high frequency inversion capacitance (C_{min}) could yield the doping density, the slope was not used because surface states were present. The experimental C-V curves indicated p-type material and, by comparison with standard curves[10,16,17], the doping density was determined to be greater than 5×10^{17} atoms/cm^3 (the maximum doping density considered by the curves[10,16,17]).

Jund and Poirier[19] give the relationship

$$C_{slim} = \frac{C_{ox}}{(C_{ox}/C_{min}) - 1} \qquad 3.2.3$$

and by extrapolating the graph of C_{slim} vs. doping density[19], a value of doping density of 2×10^{18} was determined.

Curve fitting using the computer program[18] yielded a doping density of 1.98×10^{18} atoms/cm^3.

3.2.4 Non-Ideal Behaviour

While the ideal MOS capacitor is a useful concept, it is never

observed experimentally. The ideal curve is always perturbed and distorted by work function difference, oxide charge, and fast surface states. These factors and their effect on the C-V curve are considered in the following sections.

3.2.4.1 Work Function Difference

The difference in work function between the metal field plate and the semiconductor results in an effective voltage being applied between them (see Fig. 3.4)

$$\phi'_{MS} = \phi_M - (\chi + E_G/2 + \psi_B) \qquad 3.2.4$$

where ϕ'_{MS} is the metal-semiconductor work function difference, ϕ_M is the metal work function, χ is the electron affinity of the semiconductor, E_G is the energy gap at room temperature (1.12 eV[20]), and ψ_B is the bulk potential. Deal et al[21] made a study of the metal work function by photoresponse and MOS capacitance measurements and their results, along with those from vacuum measurements, are presented in Table 3.2.

For the experimental MOS capacitor ϕ'_{MS} equals - 1.10 eV from Deal et al[21] and -0.92 eV from vacuum measurements.[22,23] Since Deal et al[21] measurements were performed on a system similar to the one used in this experiment, silicon and a thermal oxide, the value of -1.10 eV was used for ϕ'_{MS}.

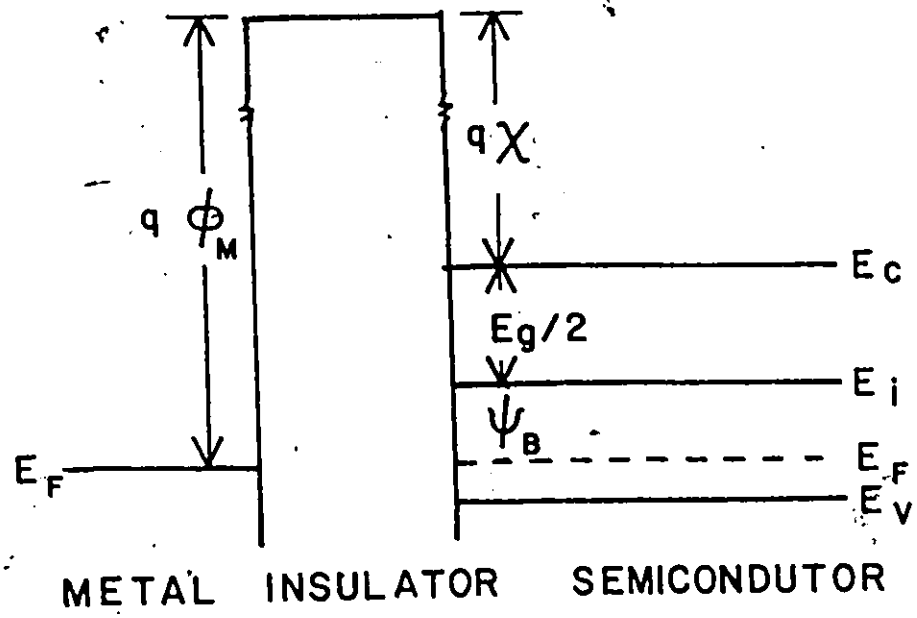


Figure 3.4 The energy band diagram of a MOS structure illustrating the metal-semiconductor work function difference

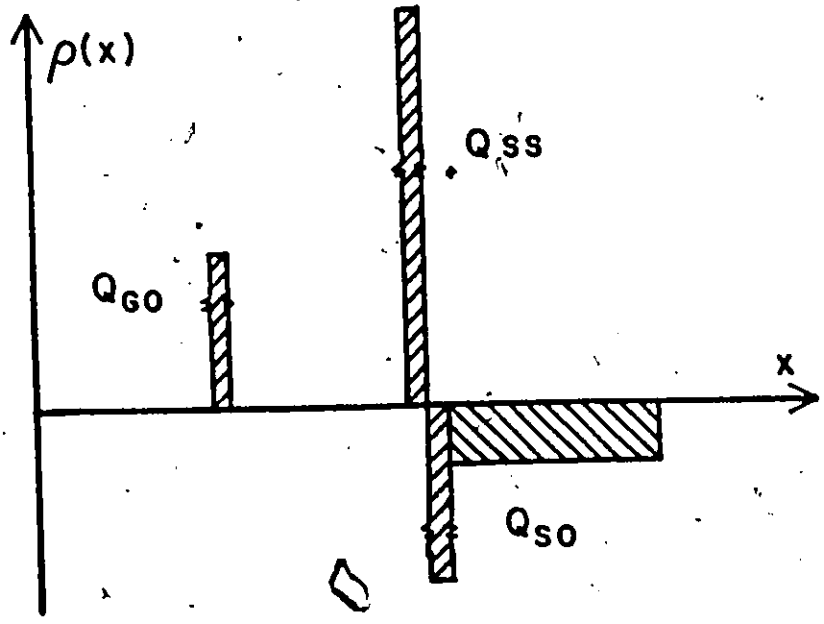


Figure 3.5 The charge distribution of a MOS structure due to a charge in the oxide

TABLE 3.2

METAL WORK FUNCTION (VOLTS)

Metal	Φ_m(C-V)	Φ_m(Photoresponse)	Φ_m(Vacuum work function)
Mg	3.35	3.15	3.7
Al	4.1[a]	4.1	4.25
Ni	4.55	4.6	4.5
Cu	4.7	4.7	4.25
Au	5.0	5.0	4.8
Ag	5.1	5.05	4.3
X		4.13	4.05

[a] Value of Φ_m for Al(4.1 volts) is the sum of the barrier height (3.2 volts) and SiO_2 affinity (0.9 volts) (after Deal et al, Ref. 21)

3.2.4.2 Oxide Charge

A charge in the oxide of an MOS capacitor induces charges in the metal and the semiconductor as in Fig. 3.5. The proportion of the charge in the semiconductor relative to the metal depends on the location of the charge in the oxide. In this section only the effects of the charge on C-V are considered.

The effect of a constant fixed oxide charge (Q_{SS}) on the C-V curve is the same as the metal-semiconductor work function difference.

The value of Q_{SS} was determined from the experimental results by the relationship

$$\Delta V_I = \phi_{MS} + Q_{SS}/C_{ox} \qquad 3.2.5$$

where ΔV_I is the difference between theoretical and experimental inversion potential, proposed by Grove et al[12] and modified by Deal et al.[27] Table 3.1 shows both the experimental inversion potential and the calculated value of Q_{SS} which was $3.7 \pm 2.1 \times 10^{11}$ charge carriers/cm^2.

Mobile oxide charge or fluctuation in Q_{SS} results in a shift in the C-V curve. However, because the amount of charge is not uniform in distance, or constant as time and bias change, different portions of the C-V curve are shifted varying amounts. This results in C-V curve distorted in shape from the ideal case. Several authors[24,25,26] consider these effects.

No hysteresis was observed in the experimental C-V curves. Consequently, no mobile oxide charge need be considered.

3.2.4.3 Surface States

Surface states or interface states are defined as energy levels within the forbidden band gap at the semiconductor-insulator interface which can exchange charges with the semiconductor in a short time. The surface state distribution is considered to be a continuum with peaks near the band edges.[28]

The charging or discharging of the interface states as the bias voltage is varied results in changes in the depletion layer width if Poissons's Equation is to be satisfied. These changes in the depletion layer width result in a small signal capacitance which differs from the ideal case and a distorted C-V curve.

3.2.5 The Measurement of Surface States

3.2.5.1 Introduction

Since the reliability and stability of all semiconductor devices are intimately related to their surface conditions, a knowledge of the density and energy distribution of surface states is of great importance in device operation. An excellent discussion of surface states is found in the book, Semiconductor Surfaces[28] Different means of determining the density and the energy distribution of surface states from MOS capacitor measurements are considered next.

3.2.5.2 The High Frequency Method

Terman[30] proposes a high frequency or differential method of determining the surface state density by comparing ideal and experimental high frequency C-V curves. The energy distribution of the surface states is determined by graphical differentiation of the difference between the theoretical and experimental C-V curves. Zaininger and Warfield[31] consider the approximations and assumptions of Terman's method and state that it is of limited value, primarily due to the graphical differentiation.

Terman's method was attempted and while the graphical differentiation was not possible, an estimate of the total surface state density was made. Table 3.1 gives the flatband and inversion potential for a number of devices. The value of the fast surface density, n_{SS}, was determined using the relationship proposed by Deal et al[27]

$$\Delta V_{FB} - \Delta V_I = q\, n_{SS}/C_{ox} \qquad 3.2.6$$

where ΔV_{FB} and ΔV_I are the difference between ideal and experimental C-V curves at flatband and inversion respectively. n_{SS} was calculated and the results are presented in Table 3.1. The mean value of n_{SS} was found to be 6.2×10^{11} states/cm^2 with a standard deviation (σ) of 4×10^{10} states/cm^2.

3.2.5.3 The Low Frequency Method

Berglund[32] proposes a low frequency or integral method which determines both the density and energy distribution of surface states and surface potential by comparing experimental and ideal low frequency curves. This method is enjoying a surge of popularity with the use of quasi-static

techniques[24,33,34] of determining low frequency C-V curves from the current response when a linear voltage ramp is applied. Kooman[35] determines the surface potential by measuring the voltage across an MOS capacitor when a constant current is applied. Kuhn[34], however, states the accuracy of the quasi-static C-V decreases as the doping density increases.

Measurements on the MOS capacitor using the quasi-static technique were unsuccessful because of the high doping density.

Clayton[36] reports on a conventional system to generate very low frequency C-V curves but, even using his actual system, it was not possible to generate a low frequency curve.

Since no low frequency C-V curves were measured, it was not possible to determine n_{SS} by this method.

3.2.5.4 The Conductance Method

The conductance method proposed by Nicollian and Goetzberger[25] determines the surface state properties from measurements of the conductance (G) as a function of bias voltage for different test frequencies, using an equivalent discrete component model for the MOS capacitor. Deulung et al[26] extend the device model using different approximations. This method is very time consuming and only covers a limited portion of the band gap.

The C-K-C system (see Section 3.2.2) was used and a G-V curve similar in shape to those reported[25] was observed at 10 KHz. At lower frequencies, the signal to noise ratio was such that no G-V curve was possible.

At higher frequencies, the detector sensitivity decreased and no G-V curves were possible. No detailed calculations were possible from only the one G-V curve.

3.2.5.5 The Static Method

The static method proposed by Grey and Brown[37,38] and Arnold[39] determines the density and energy distribution of the surface states from measurements of C-V curves at different temperatures. As the temperature changes, the Fermi level moves, thus changing the occupancy of the surface states. This means the change in C-V curves with temperature is directly related to the number of surface states in the energy increment where the occupancy changes.

No lateral shift was observed between the MOS C-V curves measured at room temperature and 77.4°K indicating a small number of surface states in the energy increment examined. This method fails for heavily doped material because the Fermi level is a very weak function of temperature[40] resulting in a very small energy increment.

3.2.5.6 Conclusions

It was extremely difficult to determine the density and energy distribution of surface states on heavily doped semiconductors using the MOS capacitor. For the experimental MOS capacitor only a crude estimate of 6.2×10^{11} states/cm^2 for the total surface state density was possible.

3.2.6 Impurity Band Broadening

When Grey and Brown made the low temperature MOS C-V measurements, they observed not only a lateral shift due to surface states[37,38] but also a dip in the C-V curve due to the Fermi level crossing the impurity level.[41] This phenomenon was studied in detail.

Measurements were made of the MOS C-V using the C-K-C system at three fixed temperatures, the melting point of nitrogen (63.3°K), the boiling point of nitrogen (77.4°K) and the boiling point of argon (87.5°K). At each temperature, a dip was observed in the C-V curve. Theoretical calculations were made using the computer program[18] at each temperature assuming a delta function for the impurity band. The position of the theoretical and experimental dips on the C-V curves agreed but the theoretical dips were much sharper.

Kleppinger and Lindholm[42] propose a model of impurity band broadening to account for a number of experimental results for heavily doped material. This model was used in the calculations[18] and the resulting C-V curves had dips which were much closer to the experimental results. However, when the impurity band width was calculated to fit at one temperature, the results did not agree at the other two temperatures.

In cooperation with K.C. Lee, a theory[43] was developed for the intermediate region between low doping, where a delta function works, and degeneracy, where the model of Kleppinger and Lindholm[42] is valid. The impurity band is assumed to be gaussian in shape as proposed by Morgan[44] with the width determined by the screening length of a non-degenerate system.[45] Since the Fermi function is used in calculating the screening

length thus determining the impurity band structure which in turn controls the Fermi level, an iterative procedure must be used. Initially the Fermi function is evaluated using a delta function for the impurity band. This value is then used in determining the impurity band structure which in turn is used in evaluating a new Fermi function. Successive interations are applied until the system converges within any preset limits. Since the non-degenerate screening length is temperature dependent, the width of the impurity band is also temperature dependent. Using this model, theoretical C-V curves at each temperature were calculated[18] which had dips in excellent agreement with experiment.

3.2.7 The Inversion Layer Response

The response of the inversion layer is limited by the generation rate of minority carriers. Consequently, by studying the response of the inversion layer the generation mechanism and minority carrier lifetime can be determined. As these are critical parameters in the operation of all semiconductor devices, the test procedures employed were examined in detail.

3.2.7.1 The Small Signal Response

Whether the inversion layer follows the small AC signal or not determines whether the C-V curve returns to C_{ox} or remains at C_{min}. Lehovec and Slobodsky[46] give a theoretical AC model for the MOS capacitor which Hofstein and Warfield[47] use to determine which mechanism dominates the generation rate and the appropriate lifetime.

The low frequency response was never observed in this experiment so this procedure could not be applied.

3.2.7.2 The Transient Response

When a positive bias is rapidly applied to an MOS capacitor, the device initially goes into deep depletion and then relaxes back to C_{min} as minority carriers are generated. This effect was proposed[19,48,49,50] as a means of determining the minority carrier generation lifetime. Later workers[51,52,53] introduced modifications in experimental procedures or analysis.

In general, this is a very powerful technique but, for this device, the change from deep depletion to C_{min} was only about 2%. No bridge was available to measure changes in capacitance this small as a function of time. Consequently, the lifetime was not determined by this method.

3.2.8 Conclusions

In general, MOS C-V was not useful in evaluating the properties of heavily doped layers because the capacitance change was so small; only 5.3% from C_{ox} to C_{min}.

The measured value of C_{ox} was 234.9 pf with a standard deviation (σ) of 3.1 pf indicating a uniform oxide. The change in capacitance from accumulation to inversion of 12.5 pf with σ of 0.07 pf indicated a uniform surface doping concentration of 2.0×10^{18} atoms/cm^3.

The fixed oxide charge (Q_{SS}) was determined to be $3.7 \pm 2.1 \times 10^{11}$

charge carriers/cm^2. Q_{SS} varied widely from device to device.

A crude estimate of the fast surface state density of 6.2×10^{11} states/cm^2 with σ of 4×10^{10} states/cm^2 was made but no details of the energy distribution were possible.

A new model of the impurity band broadening in heavily doped non-degenerate material was developed which explained the experimental low temperature C-V curves better than any model previously reported.

The minority carrier generation rate was not determined since neither the low frequency inversion charge response nor the pulse response were observed.

3.3 The Dielectric

3.3.1 Introduction

The dielectric layer was a thermal oxide formed on one side of the thin heavily doped layer being studied. The thermal oxide was an integral part of the MOS capacitor considered previously but formerly the primary interest was on the interface and semiconductor properties. In this section, the bulk properties of the dielectric layer are investigated. Of assistance was a review of oxide growth presented in Chapter 2 of Grove's book.[6]

3.3.2 Oxide Charge

Any charge in the oxide impairs its function as a dielectric. The types of charges and what can be done to minimize their effects were determined.

3.3.2.1 Fixed Oxide Charge

The fixed oxide charge (Q_{SS}) is a fundamental property of the oxide-semiconductor interface, initially attributed to "dirt" and "damage". However, subsequent investigations have shown, even under the cleanest of conditions, some Q_{SS} remains. In general Q_{SS} is positive. While its location within 200 Å of the interface and its experimental properties[27] are well known, no theoretical explanation of Q_{SS} is agreed upon.

Different anneal procedures to reduce the value of Q_{SS} are proposed.[5,27,54,55] The experimental devices were given a low temperature anneal[5] to reduce Q_{SS}. A low temperature anneal was selected because, at high temperature, the diffusion constants of impurities are larger. Dopant impurities redistribute and contaminent impurities increase.

The number of fixed oxide charges was determined to be 3.7 ± 2.1 $10^{11}/cm^2$ in Section 3.2.4.2.

3.3.2.2 Mobile Oxide Charge

Mobile charges in the oxide has been one of the most severe problems facing MOS devices. In fact, stability problems related to these effects delayed the devices becoming commercial realities for over five years. Oxides which are not stable make test data questionable and the devices virtually useless.

Snow and Deal[56] present an excellent review article on this area.

(i) Mobile Ions

Mobile ions are the worst source of instability since the SiO_2 lattice is open for their movement. Two ions, suggested to be the source

of these instabilities, are hydrogen and sodium.

Hofstein[57] reported observing both H^+ and Na^+ from radio-tracer work but Raider and Flitsch[58], were unable to duplicate the observations of H^+. McCaughan[59] explained Hofstein's results[57] as due to the radio-activity of the isotope he selected.

Sodium is accepted as the mobile ion and its behaviour is well known.[60,61,62,63] Kerr et al[64] first reported that a layer of phospho-silicate glass (PSG) on top of the thermal oxide would stabilize the dielectric. This stabilization is due to the PSG acting as a getter for the sodium and later papers give more details.[4,65,66,67,68]

An initial set of devices was fabricated which did not receive a PSG treatment. The resulting MOS capacitors were very unstable with a hysteresis loop of 20 ± 5 V at room temperature corresponding to 2.5×10^{12} mobile ions/cm^2. These devices were discarded as useless.

The second group of devices did receive the PSG treatment and no hysteresis was observed in the C-V at room temperature. After 15 min. at 200°C with biases of ±40 V, no shift was observed using the Wayne-Kerr bridge. This confirms that addition of the PSG resulted in a stable dielectric.

(ii) Polarization

Snow and Deal's [65] study of the properties of PSG revealed the glass itself polarized, introducing instability. Later workers[4,66,67,68] proved that a relatively thin layer of PSG with a moderate phosphorous content removes the sodium instability without introducing polarization. The layer used on the experimental devices appears to satisfy these conditions since no instability was observed.

(iii) Trapping

Trapping occurs when carriers are injected across the interface and are captured by traps in the dielectric. It is not observed in thermal oxides though often seen in deposited films, particularly silicon nitride. The review[56] considers this effect in detail. Trapping was not detected in the experimental devices.

3.3.3 Oxide Thickness

To completely characterize the dielectric layer, its thickness must be known.

The thickness of the dielectric (W_{ox}) is determined from

$$W_{ox} = A K_{ox} \varepsilon_o / C_{ox} \qquad 3.3.1$$

if the device area (A) and the relative dielectric constant of the oxide (K_{ox}) are known. A was defined by the mask to be 1.0 mm^2 while K_{ox} was determined from the literature. Hartman et al[69] gave K_{ox} of 3.78 and 5.8 for SiO_2 and SiO respectively. Snow and Deal[65] give 3.75-3.90 for thermal oxides and 4.0-4.1 for PSG. Grove[6] uses 3.9. The experimental results, that K_{ox} was independent of frequency from 1600 Hz to 1 MHz and temperature from 63.3° to 373°K, agree with the reported[65] properties of thermal oxides. Since the dielectric is basically a thermal oxide with a thin layer of PSG on top, a value for K_{ox} of 3.9 ± .1 was used. Combining this with the average value of C_{ox} from Table 3.1 gave W_{ox} of 1470 ± 75 Å.

The blank wafers which had been processed with the devices were measured on a Rudolph type 43603-200 E manual photoelectric ellipsometer

and the thickness found to be 2,215; 2,220; 2,218 Å using the calculations of Rowe.[70] These values indicate excellent agreement from wafer to wafer but, since the dielectric was not simply SiO_2, the absolute value was not correct. The McCrackin[71] program was used to consider the effect of the PSG and the thickness was found to be between 1900 and 2200 Å. In an attempt to eliminate the unknown in the optical constants, a source imaging multiple beam interferometer (the Sloan Instruments Angstrometer Model M-100) was used and gave a thickness of 2070 ± 150 Å. The results on the bulk wafers were consistent but do not agree with the values from the capacitance method.

Since the devices underwent metalization while the bulk wafers did not, this process was examined in detail. During the clean, after the base contact opening was defined, the wafer was dipped in HF to remove approximately 50 Å of oxide, formed during the peroxide clean. Both Snow and Deal[65] and Pliskin and Gnall[72] report the etch rate of PSG to be orders of magnitude faster than SiO_2 so most, if not all, of the PSG layer was removed from the devices.

White light was shone on both bulk wafers and devices and the oxide thickness determined from the observed colour using the values of Burger and Donovan.[73] The bulk wafers were a gold colour corresponding to approximately 2200 Å while the device was blue (Fig. 2.4) which corresponds to approximately 1500 Å.

Thus it appears that the difference between the thickness of the dielectric on the bulk wafers and the devices was due to the metalization process for the devices which removed most, if not all, of the PSG layer.

The results for each group were very consistent from sample to sample and between measurement techniques. The thickness of the dielectric layer on the experimental devices was 1470 ± 75 Å.

3.3.4 Dielectric Breakdown

The field at which the dielectric breaks down is of critical importance since it limits the operating range of any device using the dielectric.

There are three methods of determining the dielectric strength:

(1) repeated measurements on the same self-healing capacitor to determine the ultimate dielectric strength[74,75,76]

(2) measurements on a large number of devices for a statistical analysis of the initial breakdown[77]

(3) a non-destructive method where the field at a preset current level is used as an effective breakdown field.[78]

Osburn and Ormond[79] combine the first two methods using self-healing capacitors and noting the initial breakdown. This work is an excellent treatment of the effect of process parameters, PSG, and semiconductor material on the oxide breakdown strength.

Klein and Gafni[78] using method (3) found an effective breakdown field of 3-4 x 10^6 V/cm. Eldridge[77] reported breakdown fields of 6-8 x 10^6 V/cm and 8-11 x 10^6 V/cm for SiO_2 and PSG. Osburn and Ormond found a dependence of the breakdown field on the ramp rate; at a ramp rate of 20 x 10^6 V/cm-s, the breakdown field is 7.75 - 9.75 x 10^6 V/cm while at a ramp rate of 0.05 x 10^6 V/cm-s the breakdown field is 7.25 - 8.75 x 10^6 V/cm.

Since the devices were not self-healing and only a limited number were available, method (3) was used. The voltage was applied in 5 volt increments and current allowed to come to equilibrium after each step. The results are recorded in Table 3.1. The average applied voltage was 70 V corresponding to a field of 4.8×10^6 V/cm. To reduce the chance of accidental failure of the devices, a low current limit was selected resulting in a low breakdown field. Several devices were tested to breakdown and the results were 95 V or 6.5×10^6 V/cm. The initial breakdown field of SiO_2 layers is distributed over the entire range from 0 to the ultimate strength[77,79] but the addition of a thin layer of PSG removes the low and intermediate field breakdowns[77,79] This is attributed to the PSG filling pin holes which are believed to cause the breakdowns at less than ultimate strength. Tables 2.1 and 3.1 show very few low or intermediate level breakdowns indicating the effect of the PSG layer was not lost when most of the layer was etched away.

The devices tested had very few low or intermediate level breakdowns. The effective breakdown field was 4.8×10^6 V/cm. For the devices stressed to failure, the breakdown field was 6.5×10^6 V/cm. These values were on the lower limit of the range reported in the literature.

3.3.5 Conduction Through the Dielectric

The currents through the dielectrics are the major loss mechanism in capacitors. A leaky oxide in a MOS capacitor allows the inversion charge to leak away as fast as it is generated, resulting in a device which is permanently in deep depletion. For these reasons, the leakage currents

in these devices were studied in detail. Table 3.3 lists the conduction mechanisms in dielectrics which are discussed in several review articles.[80,81,82]

The current was measured for steps in bias of 10 V and the results plotted in Fig. 3.6 in a form to test the conduction mechanism. The linear relationship of log J vs $\sqrt{V}$ indicates either Schottky or Frankel-Poole emission. The theoretical slopes for Schottky or Frankel-Poole emission were calculated to be 1.91 and 3.82 respectively. The experimental slope was 1.83. These experimental results indicate a Schottky type slope but a prefactor that was certainly not the Richardson constant as reported elsewhere.[69,83,84,85]

Two models are proposed to explain these results. Stuart[83] and Servini and Jonscher[85] propose modified Frankel-Poole emission considering the structure of the oxide. O'Dwyer[86] reports machine calculations, using a model of the dielectric proposed by Frölich[87] involving traps in the oxide with Fowler-Nordheim emission at the interface, which gave results similar to the experimental observations. Pure Fowler-Nordheim emission is reported for SiO_2.[88,89,90]

It was concluded that Fowler-Nordheim emission occurred at all times but, if the trap density in the oxide exceeded a certain value, the conduction mechanism (involving the traps) proposed by O'Dwyer[86] dominates. The leakage current through the oxide was so small it did not affect the operation of the MOS capacitor. At 70 V bias in 1 s, approximately 1% of the inversion charge leaked away but the total generation time was only about 0.5 s so the layer remained in effective equilibrium.

TABLE 3.3

BASIC CONDUCTION PROCESSES IN INSULATORS

Process	Expression†	Voltage and Temperature Dependence‡
Schottky Emission	$J = A^*T^2 \exp \dfrac{-q(\phi_B - \sqrt{qE/4\pi\varepsilon_1})}{kT}$	$\sim T^2 \exp(+a\sqrt{V/T})$
Frenkel-Poole Emission	$J \sim E \exp \dfrac{-q(\phi_B - \sqrt{qE/\pi\varepsilon_1})}{kT}$	$\sim V \exp(+2a\sqrt{V/T})$
Fowler-Nordheim Emission	$J \sim E^2 \exp - \dfrac{4\sqrt{2m^*}\,(q\phi_B)^{3/2}}{3qhE}$	$\sim V^2 \exp(-b/V)$
Space-Charge-Limited	$J = \dfrac{8\varepsilon_1\mu V^2}{9d^3}$	$\sim V^2$
Ohmic	$J \sim E \exp(-\Delta E_{ae}/kT)$	$\sim V \exp(-c/T)$
Ionic Conduction	$J \sim \dfrac{E}{T} \exp(-\Delta E_{al}/kT)$	$\sim \dfrac{V}{T}\exp(-d'/T)$

†A^* = effective Richardson constant, ϕ_B = barrier height, E = electric field, ε_1 = insulator dynamic permittivity, m^* = effective mass, d = insulator thickness, ΔE_{ae} = activation energy of electrons, ΔE_{al} = activation energy of ions, and $a = \sqrt{q/(4\pi\varepsilon_1 d)}$.

‡$V = Ed$. Positive constants independent of V or T are b, c, and d'.

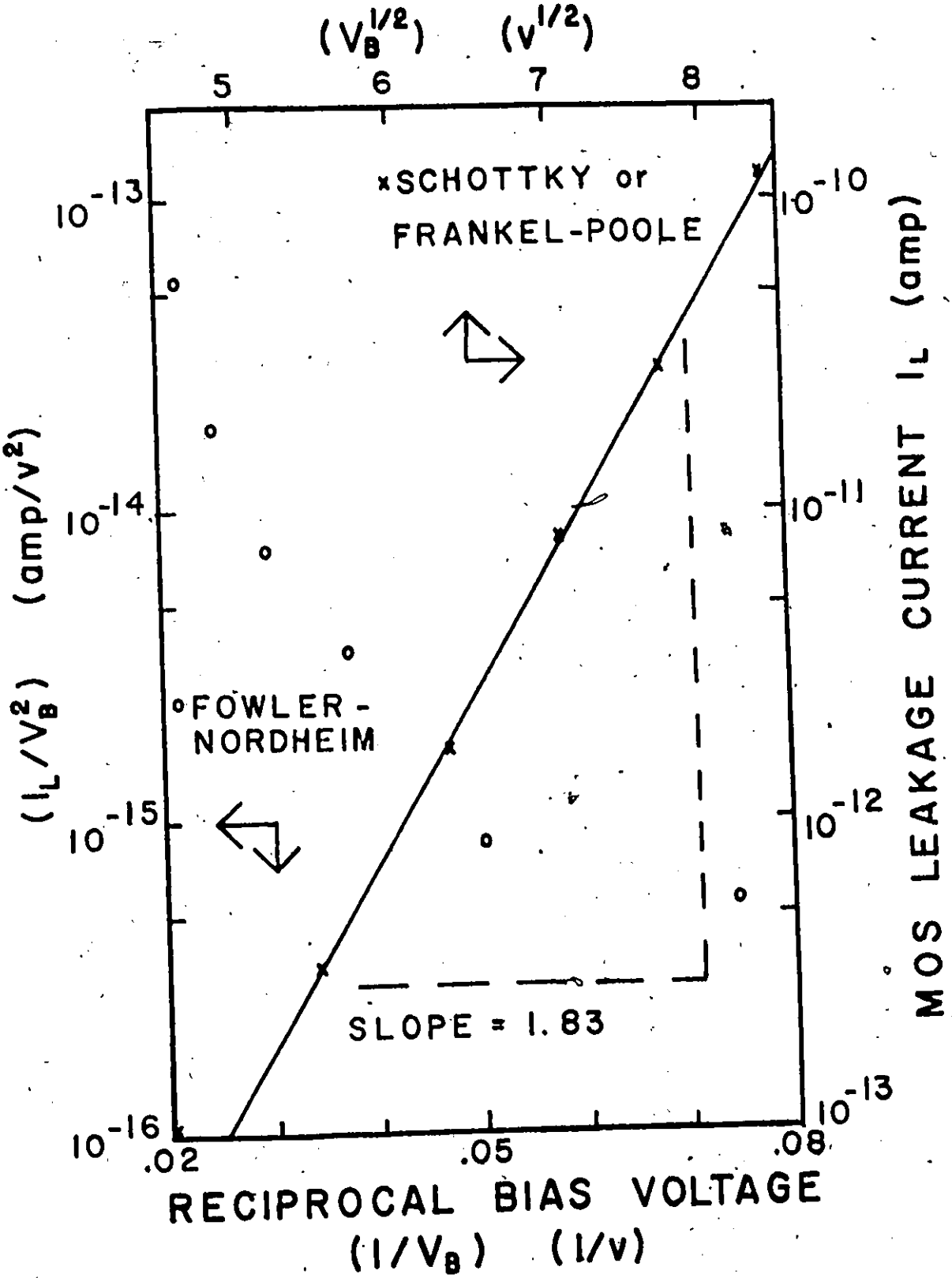


Figure 3.6 The current-voltage characteristic of the thermal oxide plotted to demonstrate the conduction mechanism

3.3.6 Conclusions

The dielectric was identified as thermal SiO_2 stabilized with phosphosilicate glass. Its properties were determined to be

thickness (W_{ox}) = 1470 ± 75 Å

relative dielectric constant (K_{ox}) = 3.9 ± 0.1

fixed oxide charge (Q_{ss}) = 3.7 ± 2.1 x 10^{11} charge carriers/cm^2

effective breakdown field = 4.8 x 10^6 V/cm

ultimate breakdown field = 6.5 x 10^6 V/cm

These properties are in excellent agreement with those reported in the literature for thermal SiO_2.

The layer was stable as indicated by no hysteresis in the C-V_g even under temperature bias stressing (± 40 V at 200°C for 15 minutes)

The leakage current through the oxide was an exponential function of the square root of the applied voltage. The current was so small, that for biases less than 70 V, it did not affect the operation of the MOS capacitor in inversion.

3.4 The Impurity Profile

3.4.1 Introduction

The electrical characteristics of semiconductor devices are primarily determined by the impurities incorporated into the body of the semiconductor and their spatial distribution.

The distribution of the electrically active impurities was investigated and profiles measured using several methods.

3.4.2 Theory of Diffusion

The impurity profile was predicted from the theory of diffusion as described in several books.[6,91,92]

The initial 900°C boron diffusion is considered to be a diffusion from an infinite source and produces a complementary error function with the surface concentration set by the solid solubility. The drive at 1200°C considers this layer to be a delta function at the surface with a fixed number of impurities (S) and the resultant impurity distribution, N(x,t), can be expressed as

$$N(x,t) = \frac{S}{\sqrt{\pi Dt}} e^{-\frac{x^2}{4Dt}} \qquad 3.4.1$$

where D is the diffusion constant, x is the distance and t is the time.

For this profile to be realized, the oxide must be a perfect barrier which no dopant can cross. Boron is known to diffuse outward[93,94,95] when an oxide is grown, resulting in an impurity profile with a dip at the surface.

The subsequent phosphorous diffusion at 1050°C on the back of the wafer does not seriously effect the boron distribution since the value of D in Eq. 3.4.1 at 1050°C is only 3% of that at 1200°C.[96]

3.4.3 Approximate Check on the Distribution

Measurements were made on one of the blank wafers processed with the devices. The sheet resistivity was 200 Ω/□ from four-point probe measurements. The junction depth was found to be 3.1 μm by beveling and staining.

These values were combined with the curves generated by Irwin[97] for a gaussian profile to determine the surface concentration of 3-3.5 x 10^{18} atoms/cm^3. This value agrees with that found by MOS C-V of 2 x 10^{18} atom/cm^3, particularly when an allowance was made for out diffusion. These results confirm the general form of the impurity profile.

3.4.4 C-V Profiling

C-V profiling[98,99,100] is enjoying considerable popularity because it is non-destructive, requires a relatively small area and direct reading instruments are commercially available. However, the distance over which the profile can be determined is limited by the avalanche breakdown of the semiconductor and is so small for heavily doped material that C-V profiling was not used.

3.4.5 Spreading Resistance Profiling

Spreading resistance[101,102,103] gives a complete profile on a small area, rapidly and to any depth. However, the equipment is expensive, calibration is difficult, computer analysis for interpretation is usually necessary and step sizes are normally larger than 500 Å.

The spreading resistance unit of Westinghouse Canada (a Solid-State Measurement ASR100) was used to determine the profile. The results on the shallow layer were unsatisfactory because they were non-reproducible, inconsistent with other measurement and the step size of 2,500 Å was too large. Similar observations were made by other investigators and the following changes were made by the manufacturer

(1) improved beveling technique to half the step size

(2) the use of smaller grains in beveling to reduce the depth of surface damage

(3) the head was lowered more slowly to decrease the penetration depth

These modifications greatly improved the observed results but the resulting profile lacked the detail achievable by the following technique.

3.4.6 Profiling by Sectioning

Profiling by sectioning involves successive measurements each followed by the removal of controlled layers of the semiconductor. Many different measuring techniques are used with sectioning. C-V is discarded for the same reasons as before (see Section 3.4.4). Radio-tracer counting [104,105] is used for many dopants but not boron, because it does not have an isotope with a convenient halflife. Tannenbaum[104] determined the impurity profile by differential sheet resistivity measurements. Johansson and Mayer[106] give an excellent description of using the Hall effect to determine the doping density. However, the Hall effect measurements are very time consuming and the geometry difficult to define. Determining the resistivity by the four-point probe[107,108,109] and converting to the dopant density by Irwin's curves[97] is rapid and inexpensive. Therefore, this technique was selected to determine the impurity profile.

The method of sectioning selected was anodic oxidation followed by etching of the oxide. In cooperation with H.B. Lo, a detailed study was made of the parameters affecting the anodization reaction to develop a

controlled reproducible sectioning process.[110] Constant current anodization was used with an electrolytic solution of ethylene glycol with 0.04N KNO_3, 0.5-3% water, 1-2 gm/liter $Al(NO_3)_3.9\ H_2O$. The back of the wafer was metalized, the electrolytic solution agitated and the wafer surface illuminated to ensure reproducible results. The amount of silicon removed was 2.23 ± 0.12 Å/V independent of current density between 2 and 8 ma/cm^2, temperatures between 3° and 50°C and silicon type and resistivity. For more details of sectioning and profiling see Lo et al.[110]

This sectioning technique, combined with the four-point probe and Irwin's curves[97], yielded the impurity profile of Fig. 3.7. This was the profile of a wafer which had undergone the same processing as the devices. The only difference was that the substrate was 1 Ω-cm instead of 2 Ω-cm. Also shown in Fig. 3.7 is an analytic expression developed to fit the experimental profile

$$N(x) = 1.45 \times 10^{19} e^{-x^2/1.315} - 1.2 \times 10^{19} e^{-x^2/0.95} \times e^{-x/10.83} - 6 \times 10^{15}. \qquad (3.4.2)$$

For points well away from the surface this expression is identical to Eq. 3.4.1 when the appropriate values of the constants are used.

3.4.7 Conclusions

The experimental profile (Fig. 3.7) was much better confirmation of Kato and Nishi's theory[95] that boron diffused out through the oxide

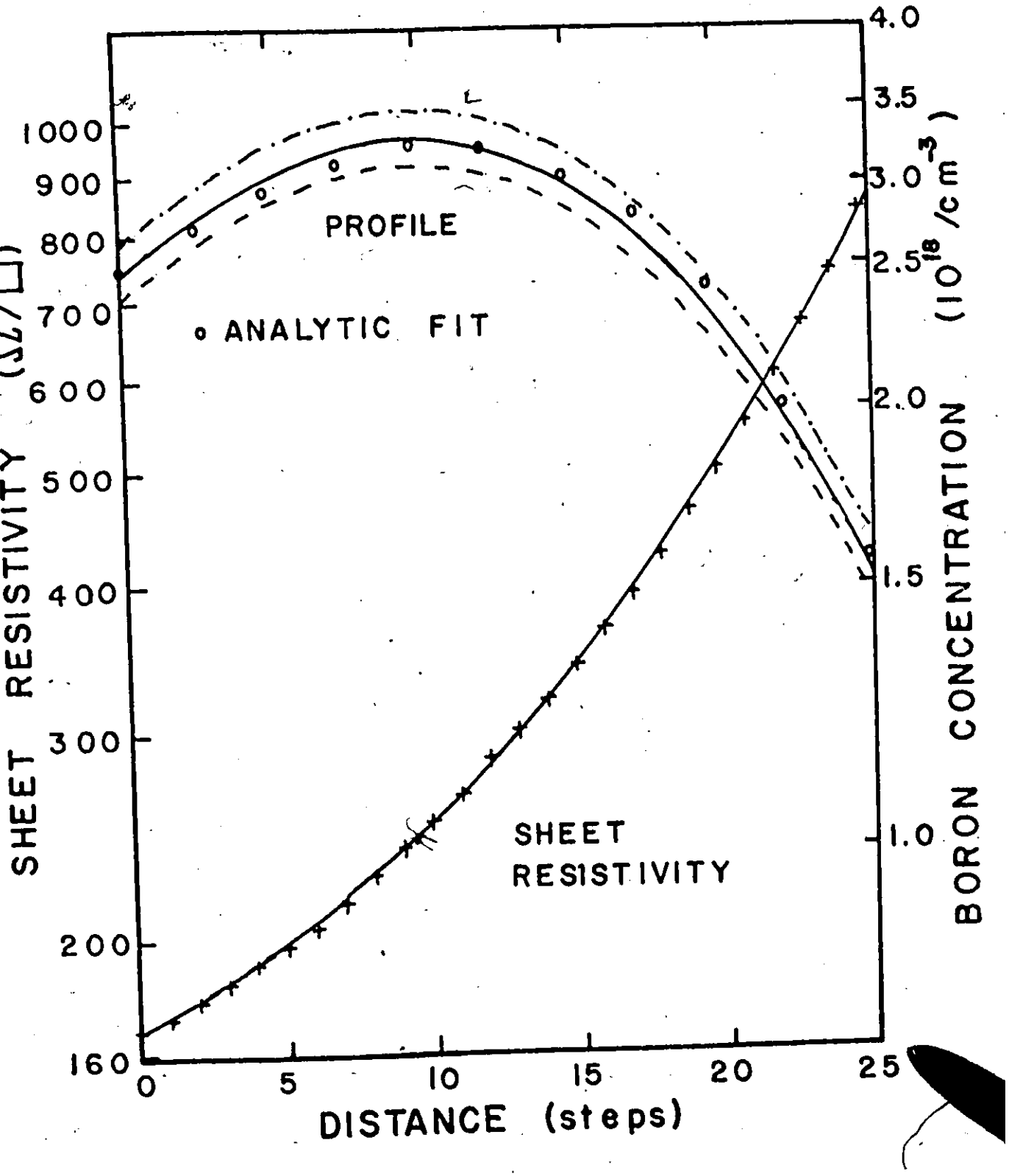


Figure 3.7 The impurity profile of the p^+ diffused layer

—·—·— 1 step = 600 Å

——— 1 step = 610 Å

— — — 1 step = 620 Å

during the drive, than their own data. Well away from the surface, the profile was gaussian, satisfying the theoretical expression (Eq. 3.4.1). Near the surface the profile dips away from the gaussian curve due to diffusion through the oxide. Both the surface concentration and the junction depth agree with the values determined on other wafers by MOS C-V and "bevel and stain" respectively.

3.5 Determination of the Substrate Parameters

3.5.1 Introduction

The device is fabricated on and is in part composed of a bulk semiconductor wafer or substrate. Consequently it is essential to determine as completely as possible the wafer's electrical properties.

A suitable procedure to determine the substrate properties[106,111,112,113] is a combination of Hall effect[114,115] and conductivity measurements.

3.5.2 Theory

The experimental data, Hall coefficient (R_H) and resistivity (ρ), may be converted to carrier concentration (n for electrons) and electron mobility (μ_n) by the following equations

$$n = r/qR_H \qquad 3.5.1$$

$$\mu_n = R_H/r\rho \qquad 3.5.2$$

where r is a factor due to incorrect averaging of quantum mechanical effects in deriving the equations.

For silicon, the value of r is neither 1 nor that predicted by simple theory but a much more complex function whose value must be determined experimentally. Wolfstirn[118] gives an average value for electrons of 1.25 while Runyan[92] with more data, finds r to be a function of resistivity and equal to 1.28 for 2 Ω-cm n-type material.

3.5.3 Experimental Procedure

A wafer from the same batch as the device substrates was cut into a bar type Hall sample using an ultrasonic cutter. This sample was placed in the automated Hall system described by Shewchun et al[116] and measurements were made over the temperature range of 25° to 300°K. The experimental results were fed directly into a computer which analysed the data and plotted carrier concentration, mobility and resistivity as a function of temperature.

3.5.4 Experimental Results

For a r value of 1, the room temperature resistivity, carrier concentration and mobility were 2.23 Ω-cm, 1.8×10^{15} atom/cm^3 and 1750 cm^2/v-s respectively. Between 150° and 300°K, the mobility was proportional to $T^{-1.83}$. The activation energy of the dopant was determined[40] to be 0.0457 eV, while Lee's method[117] gave the degree of compensation as 1.06×10^{14} atoms/cm^3.

Calculations using a value of 1.28 for r resulted in n of 2.3×10^{15} atoms/cm^3 and μ_n of 1370 cm^2/v-s.

3.5.5 Discussion

The supplier states the material was nominally 2 Ω-cm. Readings of resistivity were made by four-point probe, spreading resistance and Hall effect yielding 1.96, 2.5 and 2.23 Ω-cm respectively.

The carrier concentration was 2.3×10^{15} atoms/cm^3 from Hall effect while the four-point probe and spreading resistance probe resistivities were converted by Irwin's curves[97] to 2.6×10^{15} and 2×10^{15} atoms/cm^3.

The supplier stated the material was n-type and phosphorous doped. The Hall effect revealed a n-type dopant with an activation energy of 0.0457 eV. Conwell's[119] tables show the closest impurity to be phosphorous with an activation energy of 0.044 eV.

The Hall mobility of 1750 cm^2/v-s was higher than Morin and Maita[111] but consistent with the 1700-1750 cm^2/v-s of Krag[120] for better quality 2 Ω-cm n-type material. The temperature dependence of $T^{-1.83}$ does not agree with the quoted values from Morin and Maita[111] of $T^{-2.6}$ but is closer to Putley and Mitchell's[112] $T^{-2.0}$. However, a study of Morin and Maita's[111] Fig. 8 gives a slope of $T^{-1.8}$ between 150° and 300°K.

3.5.6 Conclusions

The substrate was n-type phosphorous doped (activation energy 0.0457 eV) with a resistivity of 2.23 Ω-cm. The impurity concentration was 2.3×10^{15} atoms/cm^3 and the compensation was 1.06×10^{14} atoms/cm^3. The electron mobility was 1370 cm^2/v-s with a temperature coefficient of $T^{-1.83}$.

These values agree with the supplier's specfications and the results

reported in the literature for similar material.

3.6 The P-N Junction

3.6.1 Introduction

A p-n junction diode is formed at the interface between the diffused layer and the substrate. Theoretical diode characteristics are calculated using a model of the diode and parameters determined either from the literature or by experiment. These results are compared with experimental diode characteristics to determine a self consistent model.

3.6.2 The Diode Capacitance-Voltage Relationship

3.6.2.1 Introduction

From Shockley's[121] original work, the capacitance of a p-n junction is divided into two types: the depletion capacitance which occurs at small forward and all reverse biases and the diffusion capacitance which occurs at large forward biases. This study is primarily concerned with the depletion capacitance.

3.6.2.2 Theory

The depletion capacitance is determined by solving Poisson's Equation (Eq. 3.2.1) in a manner analogous to an MOS capacitor.[6] Simple closed form solutions exist only for two impurity distributions, abrupt and linearly graded.[122] Lawrence and Warner[123] solve the equation for

gaussian and complementary error function distributions and present the results in a series of graphs. The diffusion capacitance is considered by several authors.[124,125]

The value of V used in calculating diode C-V is not just the applied voltage (V_A) but the sum of it and the diffusion potential (ψ_D)

Kennedy and O'Brien[126] calculate the diffusion potential of linearly graded junctions and present the results as a series of graphs. The derivative of the impurity profile evaluated at the junction depth gives an estimate of the impurity gradient which was used with the graph[126] to determine ψ_D of 0.66 eV at 23.5°C.

Wilson[127] calculated ψ_D for gaussian profiles and presents his results as a series of graphs. A value of 0.64 eV for ψ_D was determined from these curves[127] for the experimental impurity profile.

The value of 0.66 eV from Kennedy and O'Brien[126] was used for ψ_D because Wilson's[127] curves were widely spaced and no explicit temperature dependence was considered. However, the intrinsic carrier concentration (n_i) normalization partially covers the effect.

3.6.2.3 Experimental Results

The device was mounted in a copper block and placed in a cryostat. The capacitance was measured on a Boonton 75A-SB bridge (see Section 3.2.2) and the results are recorded in Table 3.4. Figure 3.8 shows both a typical experimental C-V plot and the theoretical values predicted by Lawrence and Warner.[123] From the data in Fig. 3.8, the following equations were derived for the capacitance (C) and the space charge width (W)

TABLE 3.4 REVERSE BIASED DIODE C-V

Reverse voltage		Capacitance (10^{-12} Farad)									
V_R	ψ_D+V_R	#7	#8	#9	#10	#12	#13	#14	#15	#17	#19
-.45	.21	514.0	499.0	476.8	495.6	492.4	494.9	484.5	500.0	485.6	499.2
-.40	.26	318.2	307.2	313.6	312.3	319.9	321.6	319.8	325.0	320.2	321.3
-.15	.41	202.8	201.5	201.7	197.4	204.4	206.8	204.2	207.2	204.7	202.8
0	.66	180.6	179.2	179.5	175.3	181.9	184.8	181.5	184.3	181.7	180.3
.45	1.11	145.0	143.8	143.8	140.3	145.7	148.3	145.1	148.0	145.8	144.4
.95	1.61	124.4	123.2	123.2	120.4	125.2	127.4	124.6	127.2	125.0	123.7
1.85	2.51	103.4	102.6	102.6	100.2	104.2	106.2	103.7	105.6	104.2	103.1
3.35	4.01	85.2	84.5	84.5	82.2	86.0	87.4	85.4	87.2	85.4	85.2
5.8	6.45	69.6	68.9	68.8	67.1	70.1	71.5	69.6	71.3	70.0	69.1
9.35	10.01	57.4	57.0	56.8	55.4	58.0	59.2	57.6	58.9	57.5	57.2
15.35	16.01	46.7	46.1	46.0	44.7	46.9	47.6	46.7	47.6	46.8	46.2
24.35	25.01	38.1	37.8	37.7	36.6	38.2	39.2	38.1	39.0	38.7	37.9
39.35	40.01	30.8	30.5	30.4	29.7	31.0	31.5	30.8	31.6	31.1	30.5

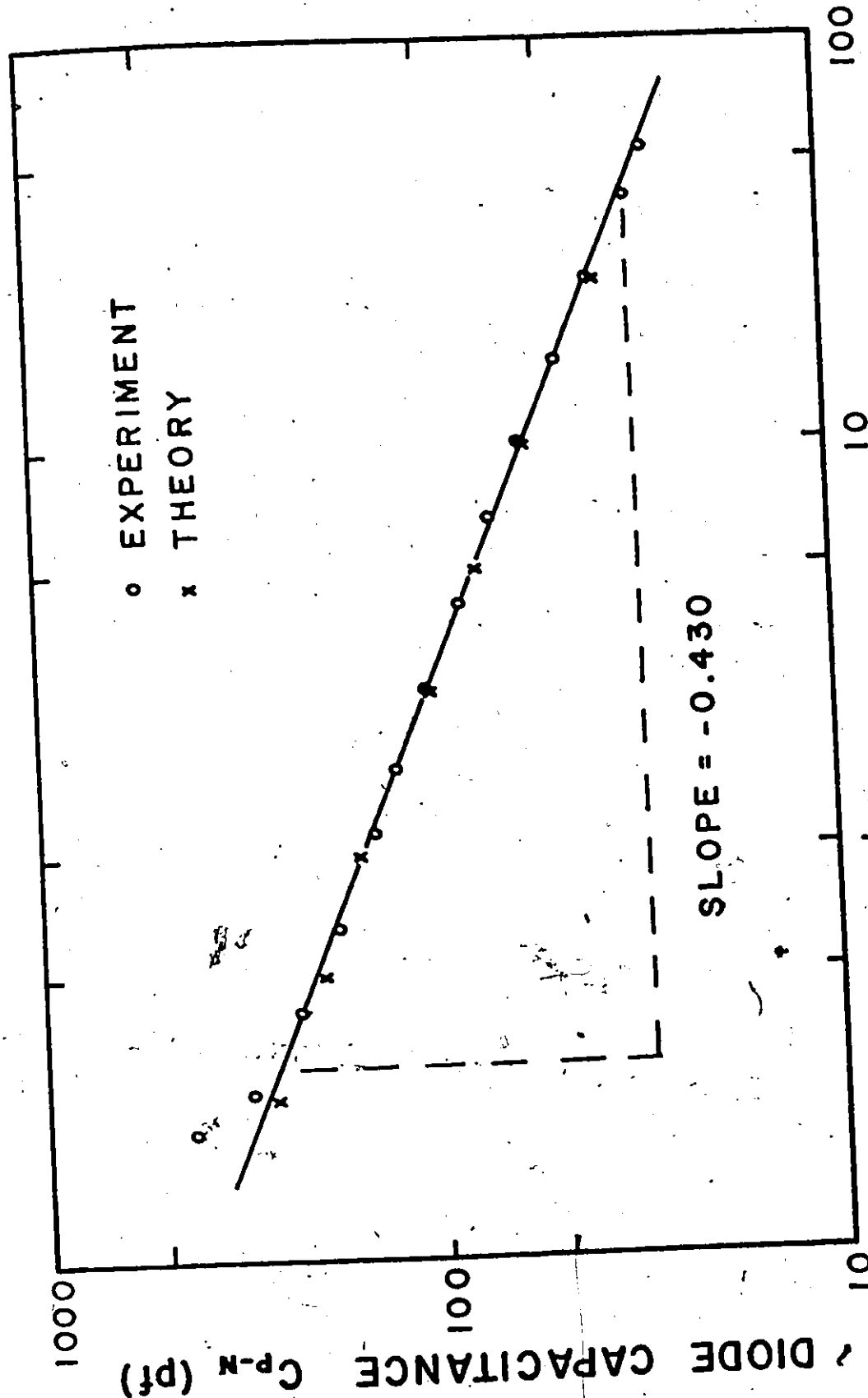


Figure 3.8 Theoretical and experimental C-V curves for a reverse biased p-n junction diode

$$C = 1.55 \times 10^{-10}(\psi_D - V_A)^{-.430} \quad f \qquad 3.6.1$$

$$W = 9.38 \times 10^{-5}(\psi_D - V_A)^{.430} \quad cm \qquad 3.6.2$$

3.6.2.4 Conclusions

The experimental data was very consistent from device to device. For example, at V_A of -9.35 volts, the standard deviation (σ) was 0.47%.

The fact that the curve remained linear at forward biases to approximately 1/2 ψ_D confirms the value of 0.66 for ψ_D.

In the depletion region the straight line was very close to the theoretical values.[123] In the region where diffusion capacitance dominates, the rise above the linear plot agreed qualitatively with theory.[124,125]

3.6.3 The Diode Forward Current-Voltage Relationship

3.6.3.1 Theory

Barber[128] shows that the forward current (J) of a p^+-n diode is the sum of the individual components

$$J = J_n + J_{r-g} + J_p \qquad 3.6.3$$

J_n is the electron diffusion current.[6,121]

$$J_n = q\left(\frac{D_n}{\tau_{no}}\right)^{1/2} n_{po}\left[\exp\left(\frac{qV_A}{kT}\right) - 1\right] \qquad 3.6.4$$

where D_n is the electron diffusitivity, τ_{no} is the low level electron

lifetime, n_{po} is the minority carrier (electron) density in the p-type material, k is Boltzmann's constant (8.62×10^{-5} eV/°K) and T is the absolute temperature (°K) Einstein's relationship

$$D = (kT/q)\,\mu \qquad 3.6.5$$

is used to relate diffusitivity and mobility.

J_{r-g}, the space-charge recombination current, is given by Sah, Noyce and Shockley[129] to be

$$J_{r-g} = \frac{2qn_i}{\sqrt{\tau_{po}\tau_{no}}} \frac{W \sinh(qV_A/2kT)}{(\psi_D - V_A)(q/kT)} f(b) \qquad 3.6.6$$

where

$$f(b) = \int_{z_1}^{z_2} \frac{dx}{z^2 + 2bz + 1} \qquad 3.6.7$$

$$b = \exp[\frac{-qV_A}{kT}] \cosh[\frac{E_t - E_i}{kT} + \frac{1}{2} \ln(\frac{\tau_{po}}{\tau_{no}})] \qquad 3.6.8$$

$$z_{1,2} = (\frac{\tau_{po}}{\tau_{no}})^{1/2} \exp\pm[(\psi_D - V_A)(q/2kT)] \qquad 3.6.9$$

τ_{po} is the low level hole lifetime, E_t is the trap level and E_i is the intrinsic Fermi level. These authors[129] consider f(b) for a symmetric junction (the doping density and lifetime are the same on both sides) and let $z_{1,2}$ go to 0 and ∞ respectively.

Choo[130] considers asymmetric effects (different doping densities

and lifetimes on each side of the junction). The equation is the same except for the limits $z_{1,2}$

$$z_1 = (\tau_{po}/\tau_{no})^{1/2} \exp(\psi_p - V_A/2)(q/kT) \qquad 3.6.10$$

$$z_2 = (\tau_{po}/\tau_{no})^{1/2} \exp(\psi_n - V_A/2)(q/kT) \qquad 3.6.11$$

where ψ_p and ψ_n are the values of the quasi Fermi levels at the p and n-type boundaries of the space-charge layer.

In an asymmetric junction, one of the diffusion currents (in this case J_p) becomes complicated by neutrality constraints when the injection level is high. Barber[128] gives an expression for all levels of injection

$$J_p = \frac{q D_p \left[\frac{2D_n}{(D_p + D_n)(\tau_{no} + \tau_{po})\tau_{po}}\right]^{1/2} n_i \left[\exp\frac{3qV_A}{2kT} - \exp\frac{qV_A}{2kT}\right]}{\left(\frac{D_p}{\tau_{po}}\right)^{1/2} \cdot \left[\exp\frac{qV_A}{kT} - 1\right] + \left[\frac{2 D_n D_p}{(D_p + D_n)(\tau_{no} + \tau_{po})}\right]^{1/2} \frac{n_{no}}{n_i} \exp\frac{qV_A}{2kT}} \qquad 3.6.12$$

where D_p is the hole diffusitivity and n_{no} is the majority carrier density (electrons) in the n-type material.

These expressions are used to calculate the theoretical forward current of the diode.

3.6.3.2 Determination of Parameters

The parameters necessary for further calculations, basically fall into two groups:

(1) Material properties which are essentially independent of processing. These can be found in the literature.

(2) Trap characteristics which are entirely process dependent and must be determined experimentally for the particular process lot.

3.6.3.2 (i) Material Properties

The material properties are intrinsic carrier concentration energy gap and mobility. Barber[131] reviews the first two of these.

Macfarland et al[20] is considered to give the most accurate value of energy gap for which

$$E_g = 1.205 - 2.8 \times 10^{-4}T \qquad 3.6.13$$

is a good approximation for temperatures greater than 250°K.

Putley and Mitchell's[112] experimental expression for intrinsic concentration

$$n_i = 3.10 \times 10^{16}T^{3/2} \exp(-0.603/kT) \qquad 3.6.14$$

agrees within 6% with Barber's[131] theoretical expression. It also agrees with more recent experimental work.[132,133]

A number of different authors[92,96,97,118,122,139] present graphs of hole and electron, majority and minority carrier mobilities as a function of resistivity or doping density. The shapes of the curves agree but the absolute values are not always the same. The curves of Wolf[96] were considered to be the best and were used in subsequent calculations.

3.6.3.2 (ii) Trap Characteristics

The forward and reverse currents in diodes are dependent on the recombination-generation process. It is assumed that recombination-generation centres of the Schockley-Read-Hall type[135], introduced during processing, dominate. The properties of these centres must be determined experimentally.

To completely characterize the recombination-generation centre, it is necessary to know the hole and electron low level lifetimes, τ_{po} and τ_{no} and the trap energy level E_t.

Kingston[136] and Lax and Neustadter[137] show that a lifetime (τ) may be determined from the current response of a diode pulsed from forward to reverse bias. They assume an abrupt one dimensional junction composed of two semi-infinite slabs; one of which the p-type, is considered to have much higher conductivity. Thus, the current is carried by holes in the n-type region. From these assumptions, they derive the following equation

$$\text{erf } (t_s/\tau)^{1/2} = 1/[1 + (I_F/I_R)] \qquad 3.6.15$$

where I_F and I_R are the forward and reverse currents and t_s is the time the current remained constant between the change in bias and decay.

Later workers extend the analysis to cover more general situations. Davidson[138] allows for finite material length by the equation

$$\text{erf } (t_s/\tau)^{1/2} = \frac{\tanh L}{1 + \frac{I_F}{I_R}} \qquad 3.6.16$$

where L is the thickness of the diode normalized by the minority carrier diffusion length. Different authors[139,140,141,142] consider the effects of a non-uniform impurity distribution in the n-type material. Mielke[143] shows that the effect of junction capacitance must be considered if the following expression is not satisfied

$$t_s >> V_f\, C/I_R \qquad 3.6.17$$

where V_f is the initial forward bias and C is the capacitance of the reverse bias diode. Kuno[144] introduces a different manner of considering the entire analysis.

The values of I_F, I_R and t_s for the experimental diode were measured to be 13.5, 11.0 ma and 6.5×10^{-8} s. The conductivity of the p-type region was much greater than the n-type which was uniformly doped except right at the junction. A value of 3.3 for L was calculated from the measured thickness of the n-type layer so

$$\tanh 3.3 = 0.997$$

and from Eq. 3.6.17

$$t_s = 6.5 \times 10^{-8} > V_f\, C/I_R = 6.6 \times 10^{-9}$$

Consequently, Eq. 3.6.15 was valid for this diode and was used to calculate

$$\tau = 3.67 \times 10^{-7}\ s$$

The lifetime (τ) was independent of the current level for low values of current. Since the current was entirely carried by holes, the measured lifetime was a hole lifetime. Combining these two facts, it was assumed that τ was the low level hole lifetime (τ_{po}).

For small values of forward bias, Eq. 3.6.6 dominates. If the current is measured and the diode area and f(b) are known, it is possible to solve Eq. 3.6.6 for τ_{no}.

The forward current at a bias of 0.1 V was 1.05×10^{-11} A. The diode area was determined to be the area of the boron diffusion mask (1.38×10^{-2} cm^2) plus the side wall area. The diffusion under the mask was assumed to be the same as the junction depth so the side wall area was represented by one quarter of the circumference of a circle, with a radius equal to the junction depth, times the perimeter of the boron diffusion (2.0×10^{-4} cm^2). The total diode area was 1.40×10^{-2} cm^2. f(b) was assumed to take its limiting value of $\pi/2$. Solving Eq. 3.6.6 using these values yielded a τ_{no} of 1.27×10^{-4} s.

The trap energy level (E_t) was determined next. Sah, Noyce and Schockley[129] give the reverse current (J_{rg-r}) for biases greater than 4 kT/q to be

$$J_{rg-r} = qWn_i\left[2\sqrt{\tau_{po}\,\tau_{no}}\;\cosh\left(\frac{E_t - E_i}{kT} + \frac{1}{2}\ln\left(\frac{\tau_{po}}{\tau_{no}}\right)\right)\right]^{-1} \qquad 3.6.18$$

Assuming a linear temperature dependence of E_i and E_t[145] then

$$\frac{d\ln(J_{rg-r}/T^{3/2})}{d(1/T)} = \frac{E_{go}}{2k} - \left(\pm\frac{|E_{to} - E_{io}|}{k}\tanh\left[\pm\frac{|E_{to} - E_{io}|}{kT}\right.\right.$$

$$+ \frac{1}{2} \ln\left(\frac{\tau_{po}}{\tau_{no}}\right)\Big| \qquad 3.6.19$$

The reverse current at 1.0 V reverse bias was measured as a function of temperature and $J_{rg-r}/T^{3/2}$ was plotted against 1/T in Fig. 3.9. The slope of the plot was 0.627 eV and knowing that

$$E_{io} = \frac{E_{go}}{2} = 0.6025 \text{ eV}^{(19)} \qquad 3.6.20$$

Eq. 3.6.19 was solved for E_{to}.

As a first approximation, $E_{to} - E_{io}$ was let equal 0 in the tanh term, therefore

$$\tanh\Big| + \frac{1}{2} \ln\left(\frac{\tau_{po}}{\tau_{no}}\right)\Big| = 0.993 \approx 1.0 \qquad 3.6.21$$

which gave

$$0.627 = \pm E_{go}/2 - (\pm)|E_{to} - E_{io}| \qquad 3.6.22$$

solving this equation

$$E_{to} = 0.627 \text{ or } 0.578 \text{ eV}$$

where all measurements were relative to the valence band.

Now a second iteration was made assuming the appropriate + or - signs and the two values of E_{to}

$$\text{for } (+)\ E_{to} = .578$$

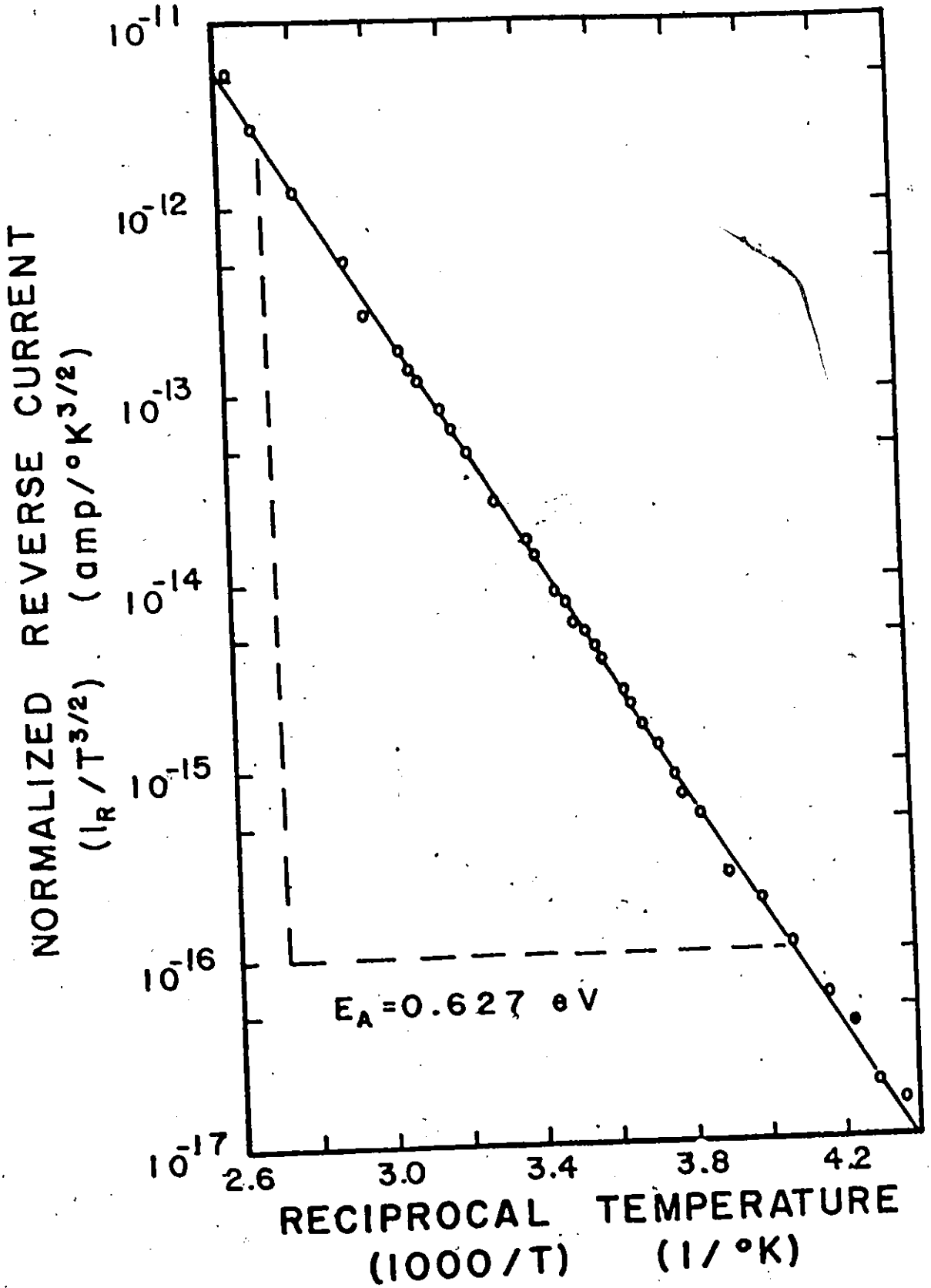


Figure 3.9 The variation of the reverse current of a p-n junction diode with temperature

$$\tanh\left| + \left|\frac{E_{to} - E_{io}}{kT}\right| + \frac{1}{2}\ln\left(\frac{\tau_{po}}{\tau_{no}}\right)\right| = 0.9518$$

for (-) $E_{to} = .627$

$$\tanh\left| - \left|\frac{E_{to} - E_{io}}{kT}\right| + \frac{1}{2}\ln\left(\frac{\tau_{po}}{\tau_{no}}\right)\right| = 0.9992$$

For E_{to} of 0.578 eV, the value of the tanh term changed, resulting in a different value of E_{to}. Using the (+) sign and the new value of E_{to} resulted in a new value of the tanh term. Each iteration diverged further so this value was discarded.

For E_{to} of 0.627 eV, the value of the tanh term was even closer to 1.0 so E_{to} of 0.627 eV was used in all further calculations.

Knowing E_{to} it was possible to calculate f(b) from Eq's 3.6.7, 3.6.8, 3.6.10 and 3.6.11. Using the calculated value of f(b) in Eq. 3.6.6 resulted in a new value of τ_{no} which in turn led to a new value of f(b). Following two iterations, the value of τ_{no} stabilized at 8.03×10^{-5} s.

The reverse currents are dominated by recombination-generation so, to confirm the properties of all devices are the same, the reverse current was measured at different voltages and the values presented in Table 3.5.

The trap characteristics τ_{po}, τ_{no} and E_t were determined to be 3.67×10^{-7} s, 8.03×10^{-5} s and 0.627 eV. These values strongly suggest the centre was gold which has an energy level of 0.62 eV[146] and a range of reported lifetime ratios[146] which include the experimental ratio. With gold as the recombination-generation centre, a hole lifetime of 3.67×10^{-7} s corresponds to a trap concentration of 2×10^{13} atoms/cm^3.[147]

TABLE 3.5 REVERSE BIASED DIODE I-V

Reverse Voltage	Current (10^{-11} amp)									
	#7	#8	#9	#10	#12	#13	#14	#15	#17	#19
.4	1.75	1.95	2.2	2.34	1.12	2.05	2.6	1.3	2.4	1.17
.63	2.45	2.6	2.92	3.00	1.5	2.8	3.38	1.75	3.15	1.56
1.00	3.2	3.4	3.9	4.00	2.03	3.81	4.52	2.35	4.25	2.09
1.60	4.4	4.6	5.25	5.4	2.78	5.45	6.1	3.1	5.73	2.82
2.50	5.8	6.0	6.9	7.1	3.7	7.6	8.1	4.2	7.68	3.7
4.00	7.8	8.1	9.3	9.4	5.1	11.5	11.0	5.6	10.5	5.08
6.30	10.5	11.0	12.5	12.7	7.0	17.3	15.0	7.6	14.0	6.83
10.00	14.5	14.9	16.8	16.8	9.72	25.0	20.5	10.5	18.9	9.4
16.00	19.8	20.2	22.8	22.5	14.4	37.0	29.7	14.7	25.7	13.3
25.00	27.	27.3	30.	29.8	20.4	56.0	41.4	20.4	34.1	20.2
40.00	38.0	37.7	42.0	40.6	30.0	90.0	60.0	29.4	48.2	29.5

3.6.3.3 Experimental Results and Calculations

The forward current-voltage characteristics were measured on an automated system where the current was increased in uniform logarithmic steps and the points plotted directly in Fig. 3.10.

Calculations were made using the theory of Section 3.6.3.1 and the results are presented in Table 3.6. The theoretical results were corrected for the effect of a series resistance of 10 Ω due to the bulk resistance of the n and p-type regions, the contact resistance and the resistance of the bonding wires, pins and leads. The theoretical I-V curve was also plotted in Fig. 3.10.

3.6.3.4 Conclusions

The following parameters were determined to characterize the diode.

$\psi_D = 0.66$ eV

$C = 1.55 \times 10^{-10} (\psi_D - V_A)^{-.430}$ f

$W = 9.15 \times 10^{-5} (\psi_D - V_A)^{.430}$ cm

$n_i = 3.10 \times 10^{16} T^{3/2} \exp(-0.603/kT)$ carrier/cm^3

$E_g = 1.205 - 2.8 \times 10^{-4} T$ eV

$\mu_p = 400$ cm^2/v-s

$\tau_{po} = 3.67 \times 10^{-7}$ s

$\tau_{no} = 8.03 \times 10^{-5}$ s

$E_{to} = 0.627$ eV

$A = 1.40 \times 10^{-2}$ cm^2

$T = 23.5°C$

TABLE 3.6 CALCULATED FORWARD DIODE CURRENT

Applied Voltage V_A(v)	b	f(b)	J_{r-g} (amp)	J_p (amp)	Corrected for Series Resistance	J_{total} (amp)
.02	1.87	.415	4.6×10^{-12}			4.6×10^{-12}
.05	1.10	.765	2.48×10^{-11}	2.42×10^{-12}		2.72×10^{-11}
.10	.390	1.27	1.05×10^{-10}	1.96×10^{-11}		1.25×10^{-10}
.15	.146	1.43	4.23×10^{-10}	1.41×10^{-10}		5.64×10^{-10}
.20	.055	1.48	1.19×10^{-9}	1.0×10^{-9}		2.19×10^{-9}
.25	.021	1.45	3.5×10^{-9}	7.07×10^{-9}		1.12×10^{-8}
.30	.0078	1.31	8.8×10^{-9}	5.0×10^{-8}		5.9×10^{-8}
.35				3.5×10^{-7}		3.5×10^{-7}
.40				2.5×10^{-6}		2.5×10^{-6}
.45				1.78×10^{-5}		1.78×10^{-5}
.50				1.24×10^{-4}		1.24×10^{-4}
.55				8.65×10^{-4}		8.65×10^{-4}
.60				5.95×10^{-3}	2.19×10^{-3}	2.19×10^{-3}
.63					3.6×10^{-3}	3.6×10^{-3}

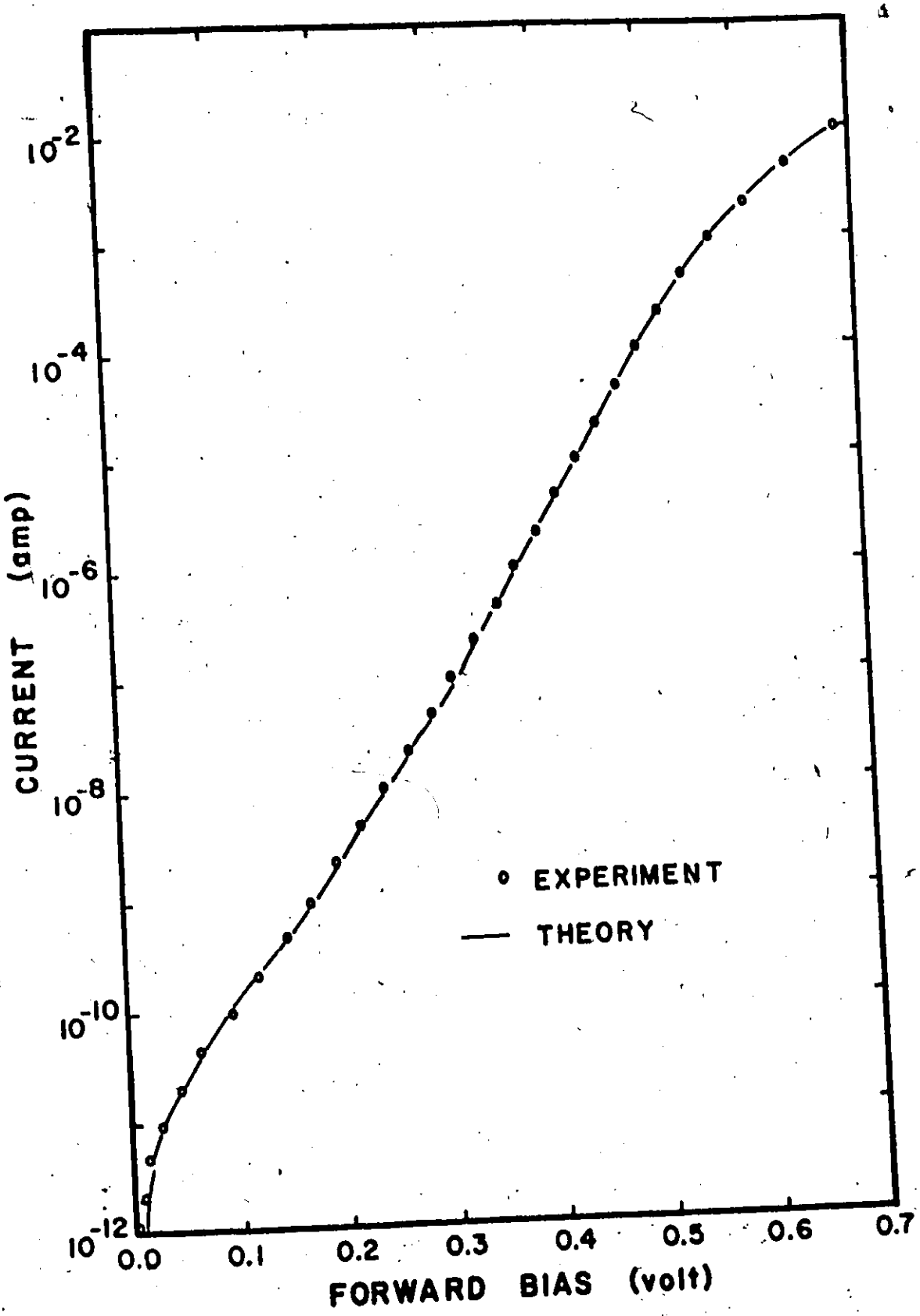


Figure 3.10 The theoretical and experimental I-V curves of a forward biased p-n junction

Theoretical data calculated using these parameters was found to be in excellent agreement with the experimental results (see Figure's 3.8 and 3.10).

The recombination-generation centres in the n-type material (the substrate)were assumed to be gold with a concentration of 2×10^{13} atoms/cm^3.

3.7 Conclusions

A characterization of the test structure by conventional proccedures was performed as completely as possible. The electrical properties of the dielectric, the substrate and the substrate heavily doped layer interface were determined accurately and comprehensively. The properties of the oxide-semiconductor interface could not be found and only a crude estimate of the total surface state density was possible. The electrical properties of the heavily doped layer could not be determined. Only the impurity profile and the impurity band broadening at the surface was determined using modifications of the conventional techniques developed during this project.

CHAPTER 4

THE MOSCET

4.1 Introduction

The conventional tests of Chapter 3 yielded the properties of the dielectric, the substrate, the interface between the heavily doped layer and the substrate and the impurity profile. However, the properties of the heavily doped layer and its interface with the oxide were still undefined. They may be determined by an experimental procedure, utilizing a new test structure.

The proposed test structure consists of an MOS capacitor formed over the thin heavily doped layer to be evaluated. This layer is of the opposite conductivity type to the substrate, thus a p-n junction is formed in the semiconductor. The MOS capacitor serves as a minority carrier emitter and the p-n junction as a minority carrier collector, thus forming an MOS capacitor emitter transistor, MOSCET. A cross-section of the MOSCET employed in this study is shown in Figure 2.4.

In operation, the p-n junction is reverse biased and becomes a minority carrier collector and the MOS capacitor is biased into inversion for a controlled length of time. During this time minority carriers are generated and form the inversion layer. A voltage pulse applied to the MOS capacitor causes it to release minority carriers from the inversion layer. These carriers cross the heavily doped layer under the combined influence of diffusion and internal fields to the p-n junction where the charge that

has not recombined during transit is collected.

For proper operation, the MOSCET structure must satisfy four conditions.

(1) The insulator thickness must be such that, at practical voltages, inversion can be realized for the given surface concentration of the heavily doped layer.

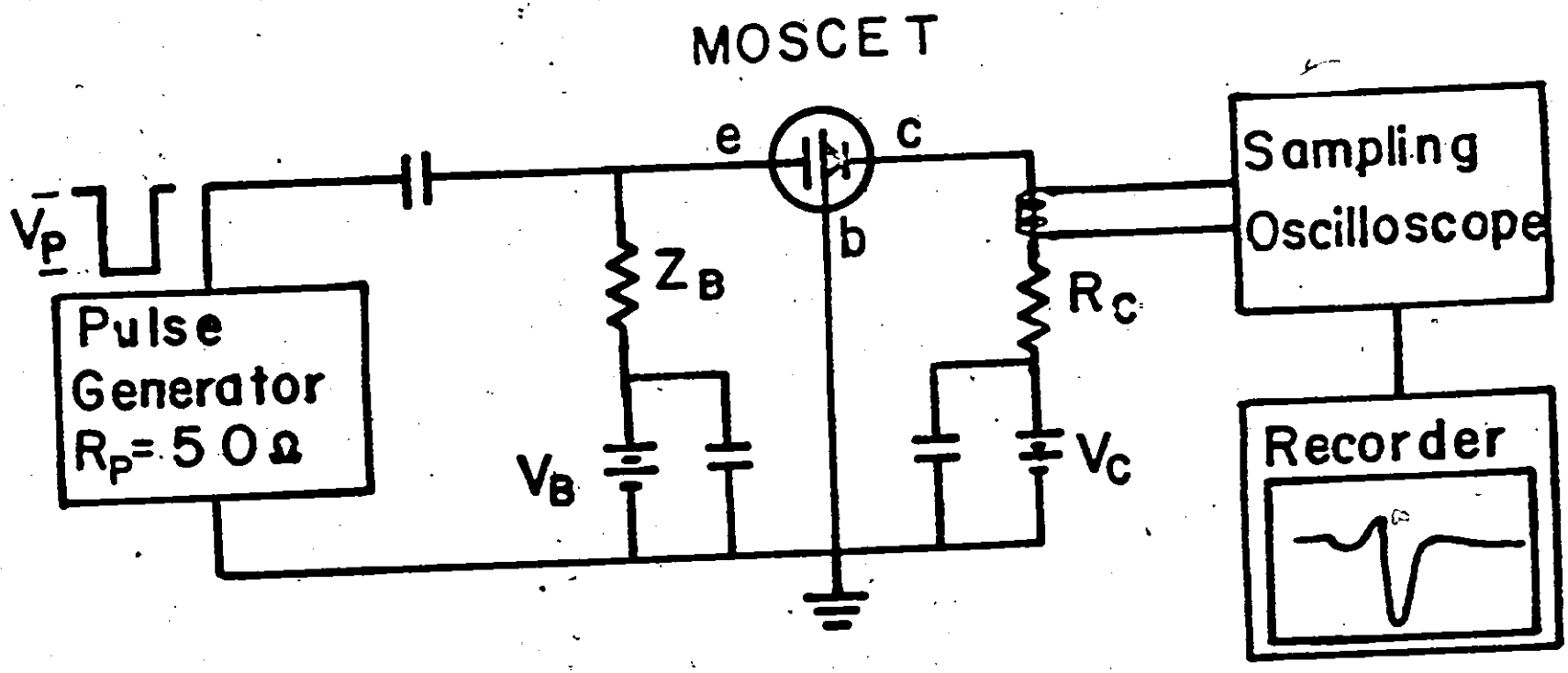
(2) The leakage through the insulator of the MOS capacitor must be so small that less than 0.1% of the inversion charge leaks away during the generation time.

(3) The width of the heavily doped layer must be such that a significant amount of the inversion charge can cross it before recombining.

(4) The heavily doped layer must be sufficiently wide that even under transient conditions, some neutral bulk remains between the depletion layers of the diode and the MOS capacitor.

4.2 The Measurement System

The experimental circuitry employed in these measurements is shown schematically in Fig. 4.1. A pulse generator having a risetime of less than 13 ns and capable of delivering 100 V into 50 Ω is capacitively coupled to the MOS emitter of the MOSCET. The value of Z_B is selected to terminate the pulse generator correctly. The MOS bias voltage can be set to any value by means of the DC supply, V_B, which is AC decoupled by a capacitor. The collector of the MOSCET is biased by the DC supply, V_C, and impedance matched for pulse measurements by R_C. The collected charge is observed by means of a current transformer in the collector circuit. The output of the current probe is fed directly to a sampling oscilloscope which in turn



PULSE CIRCUIT FOR Q-V MEASUREMENTS USING THE MOSCET

Figure 4.1 The MOSCET test circuit, schematic

drives an X-Y recorder. The collected charge is determined by measuring the area under the current-time curve using a polar planimeter. Not shown in the figure is the temperature chamber which controls the operating temperature of the MOSCET.

A photograph of the experimental equipment is shown in Fig. 4.2.

No single pulse generator would satisfy the requirement for pulse repetition rate, pulse amplitude and pulse risetime in this experiment. A group of instruments were interconnected to act as the pulse generator indicated in the schematic. A HP 214A Pulse Generator was the core of the system. This instrument would deliver ±100 V into 50 Ω with a risetime of less than 15 ns, a pulse width of 50 ns to 10 ms and an internal "reprate" of 10 Hz to 1 MHz. On the ranges up to 50 V, the internal impedance was 50 Ω while in the 100 V range, it was 1500 Ω. The 50 V range was used to give sufficient amplitude without the additional problems of reflection due to the change in source impedance. Because low frequency pulses were required, a HP 3310A Function Generator with a range of 0.0005 Hz to 5 MHz was used to trigger the HP 214A. Since the frequency dial accuracy of ±(1% of setting plus 1% of full scale) was not sufficient, a frequency counter, the HP 5300A Mainframe with a HP 5302A Universal 50 MHz Counter Moduale was used in the period mode to determine the time between pulses within .1%. The trigger output of the 214A was greater than 10 V open circuit and it repeatedly damaged the sampling scope trigger input. For this reason the SYNC output of the 3310A, which was greater than 4 V p-p open circuit, was used to trigger the scope. The variable attenuator of the 214A in the -50 V range changed the risetime from 13 to 10 ns as the

Figure 4.2 The experimental equipment employed

attenuation was increased from zero to maximum. Since a control of amplitude independent of risetime was desired, a HP 355A HF Attenuator (0 to 12 db in 1 db steps) was placed on the pulse output. This entire group of instruments constitutes the pulse generator of Fig. 4.1.

A high quality capacitor, the HP 10240A with a value of 0.1 μf and a p-p reflection of less than 5% when driven by a 100 ps risetime pulse in a 50 Ω system was used. This allowed the pulse through with a minimum of distortion while preventing DC bias on the MOS capacitor being applied to the pulse generator.

The pulse generator was effectively a current source which supplied a current producing the required voltage across 50 Ω. If the load was not 50 Ω this current was still supplied to the best of the pulse generator's ability resulting in a different output voltage. The MOSCET was a capacitive load on the pulse generator. For the faster pulse components, the impedance was less than 50 Ω while for the slower components, the impedance was much greater than 50 Ω. The resulting pulse, instead of a normal increase followed by a constant value, was a normal increase followed by a further ramp effect. To insure normal pulse shape, a matching network (Z_B) was introduced so the load on the pulse generator was always 50 Ω. First a resistor of approximately 20 Ω was placed in series with the MOSCET. Then a series combination of an inductor and a resistor were placed in parallel with the device to give an impedance which was approximately independent of frequency for the pulse's Fourier components. The sum of the resistors must be 50 Ω and the value of the inductor, which consisted of a few turns of wire around a pencil, was too small to measure.

The final matching was done by trial and error, by changing the resistor ratio and adding or subtracting turns from the inductor.

The DC supply, V_B, was a HP 6116A (0 to 100 V) with a 5 digit thumbwheel control accurate to 0.1% plus 1 mV.

A resistor (R_c) of about 35 Ω was selected by trial and error to maintain the collector circuit at 50 Ω.

The DC supply, V_c, was a HP 6206B (0 to 60 V) which was permanently set at 40 V. When different values of V_c were required, a second HP 6116A supply was used.

The current probe was a Tektronix CT-1/P6040 with a sensitivity of 5 mV/ma in a 50Ω system and an insertion impedance of 1 Ω shunted by approximately 5 μh when used with a 50 Ω termination.

The Sampling Oscilloscope consisted of a HP 141B Variable Persistance Mainframe, a HP 1424A Sampling Time Base and a HP 1410A Sampling Vertical Amplifier. Problems in the triggering system previously mentioned, resulted in a fixed delay between the trigger signal and the pulse. To display the signal on the proper time scale, it was necessary to use the expanded time scale which introduced extra jitter of 0.2% of the unexpanded sweep time per division. The current probe was attached to the 50 Ω input and large signals were attenuated by a General Radio GR874 20 db fixed attenuator. The lower limit of operation was determined by the time constant of a series combination of a capacitor and a FET in the sampling head. As the charge on the capacitor leaked away, the dot on the screen of the oscilloscope sagged and the curve became thick and "messy". The limit varied from head to head in the range 0.5 to 3 Hz. For repetition rates

above 10 Hz, the X-Y recorder was driven in the normal mode while below 10 Hz, the single shot mode was used.

The X-Y recorder consisted of a HP 7004A Mainframe with a HP 17171A DC Preamplifier Input Module on each axis. The scope output was set to 0.1 mV per division and the X-Y recorder was always operated in the calibrated mode to insure a simple relationship between the curves. The problem of sag in the scope could have been overcome by the use of a HP 17173A Null Detector Modual and a 17012B Point Plotter in the Y axis. However, the point plotter would not operate above 50 Hz and, since conversion was slow, this refinement was not used.

An Alpha #23 Polar Compensating Planimeter was used to determine the area between the curves.

The temperature chamber was a Statham Instrument SD60-1 modified to use liquid nitrogen as the coolant. The temperature range was -73.3° to 273.9°C with a control accuracy of 0.14°C. The temperature could be selected by either a 24 linear-inch calibrated dial or 3 push buttons which set preprogrammed values. The temperature settings were checked with a copper-constantan thermocouple. The temperatures determined by the thermocouple agreed with the values specified by the push buttons but the calibrated dial values were all 2° low. Except when temperature was being varied, all readings were made at 25°C using one push button.

The device, Z_B, R_c, the current probe and the by-pass capacitors (which were high quality 0.1 μf capacitors) were mounted on a small piece of vector board in close proximity to prevent parasitic effects. All of the interconnections except to the DC supplies, were made using 50 Ω

co-axial cable.

4.3 A Typical Response

A typical response of the device to a voltage pulse on the MOS capacitor is shown in Fig. 4.3. The upper curve, labelled $V_B = 0$ is the response when no inversion charge is present (the non-inversion response) and is essentially the second differential of the applied voltage pulse. If the differentiators are ideal, no net flow of charge is observed. When inversion charge is present, the resulting response is the lower curve, labelled $V_B = 36$. The shaded area between the two curves is equal to the inversion charge collected, Q_c. The position and area of the collected inversion charge pulse is determined by the transport properties between the interface and the collector and the proportion of the charge recombined during transit.

The actual amount of inversion charge released is largely dependant on the time between pulses and the bias voltage on the MOS capacitor.

The time between voltage pulses is important because the minority carriers which form the inversion layer require a finite time to be generated. Only a fraction will be generated in short periods. By measuring the charge collected as a function of the time between pulses, the generation rate can be determined.

Only inversion charge (Q_I) is detected by the MOSCET, consequently, until the MOS bias becomes close to the inversion potential, no charge is observed. Figure 4.4.shows a representation of the charge collected as a function of bias voltage on the MOS capacitor (a Q-V curve). Ideally

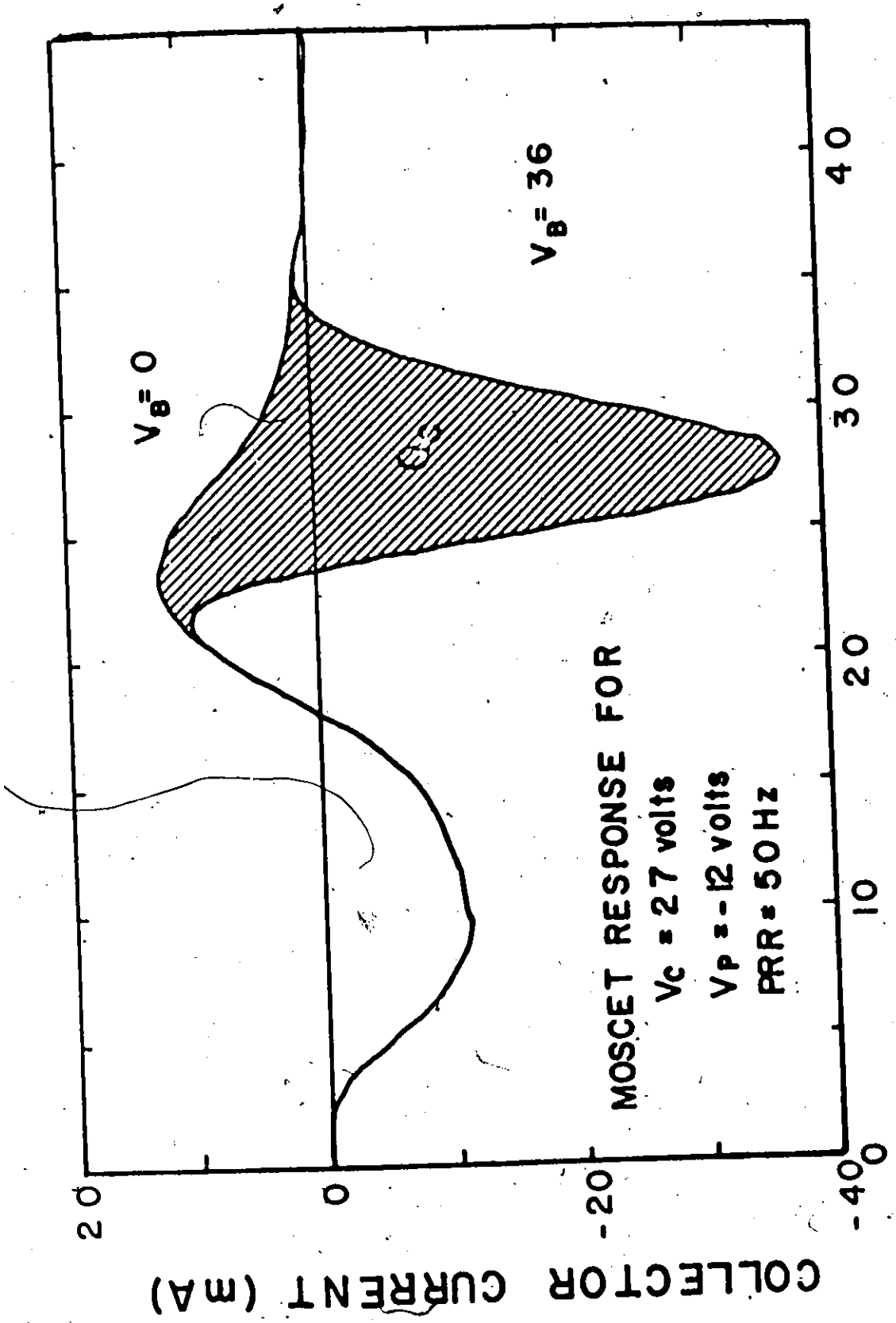


Figure 4.3 Typical transient response of the MOSCET

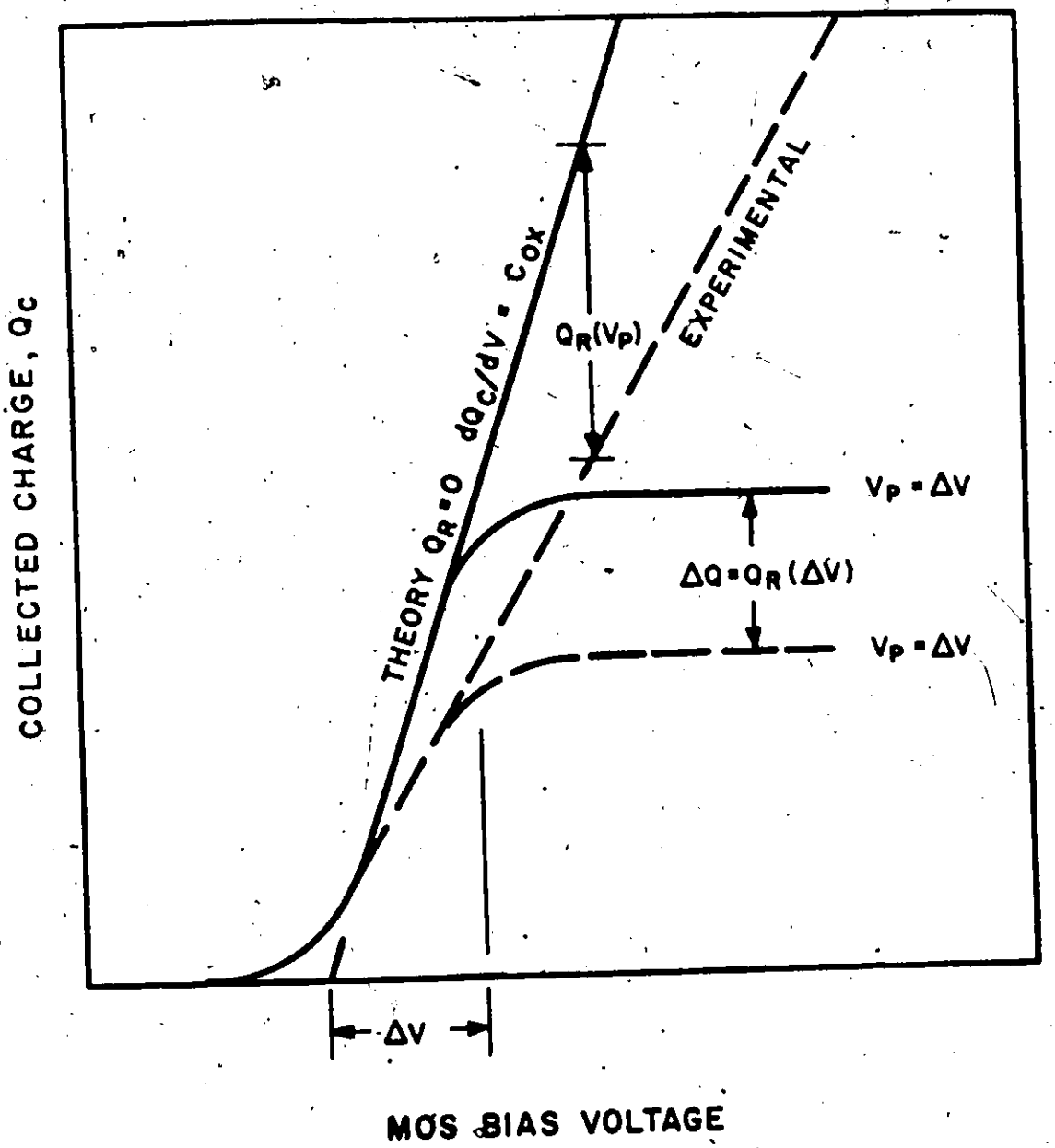


Figure 4.4 The inversion charge Q-V characteristics of a MOSCET

for biases much above the inversion potential, the charge becomes a linear function of voltage.. That is

$$d\ Q_I/dV = C_{ox} \qquad 4.3.1$$

The intercept of this straight line with the voltage axis is the inversion potential. For an ideal voltage pulse, one sufficient to pulse the device completely out of inversion, the Q-V curve would remain linear until breakdown. However, for finite voltage pulses, when the amplitude (ΔV) is insufficient to move the device out of inversion, the inversion charge released becomes a constant Q_{IS} where

$$Q_{IS} = C_{ox}\ \Delta V \qquad 4.3.2$$

When the effect of recombination is considered, the charge collected is reduced and curves similar to the one labelled experimental in Fig. 4.4 result. From this curve it can be seen that

$$Q_C = Q_I - Q_R \qquad 4.3.3$$

where Q_R is the charge recombined. However, by comparing the curves labelled theory and experiment, it is obvious that Eq. 4.3.3 will reduce to

$$Q_C = \alpha\ Q_I \qquad 4.3.4$$

where

$$\alpha \leq 1.0 \qquad 4.3.5$$

This relationship is true as long as the recombination lifetime is independent of number of carriers present (that is, only low-level recombination occurs).

4.4 Conclusions

Measurements on the MOSCET allow the determination of a number of the properties of a thin heavily doped layer and its interface with the oxide which were not previously possible.

The MOSCET allows the generation rate of minority carriers in the heavily doped layer to be measured. From this the generation mechanism and generation lifetime can be determined.

From the Q-V curve, the inversion potential was determined and the fixed oxide charge density may be calculated from the difference between the theoretical and experimental inversion potential.

By comparing theoretical and experimental Q-V curves, the ratio of charge collected to inversion charge released was determined and from this, the recombination lifetime could be calculated.

The shape and position of the inversion charge pulse is a function of the transport properties across the heavily doped layer. An analysis of the pulse can provide information about which factors are affecting the transport properties.

CHAPTER 5

THE TRANSIENT RESPONSE

5.1 Introduction

By studying the transient response of the MOSCET, the properties of the heavily doped layer and its interface with the oxide are revealed. To extract the physical parameters from the experimental results, it is necessary to have a complete theoretical understanding of the pulse response.

The theoretical transient response is initially evaluated for the case where no inversion charge is present. The inversion charge response is then calculated and the two combined to give the total transient response.

5.2 The Non-Inversion Response

The non-inversion response exists regardless of whether or not an inversion charge is present. The inversion charge, however, can only be determined by measuring the difference between the non-inversion and inversion waveforms (the shaded area of Fig. 4.3). The voltage across the MOS capacitor controls the amount of inversion charge released when a voltage pulse is applied to the emitter of the MOSCET but the voltage pulse across the MOS capacitor cannot be measured experimentally and

is calculated as part of the analysis of the non-inversion response. Therefore this calculation is the first step in determining the total transient waveform.

To calculate the transient response of a device it is necessary to know the external circuitry, the applied pulse waveform, and to have an adequate circuit model of the device.

5.2.1 The External Circuitry

The external circuitry is shown schematically in Fig. 4.1 while Fig. 5.1 shows the AC equivalent circuit. The components of this circuit, R_1, R_2, R_3, C_1, C_2 and C_3 were measured on a bridge. The source impedance of the pulse generator, R_s, and the insertion impedance of the current probe, P, were taken from the instrument specifications. The inductance, L, used in the matching network was so small it could not be measured on the bridge but was calculated to be 2×10^{-7} henries. Since the applied voltage pulse, V, was measured beyond the blocking capacitor, C_1, neither C_1 nor R_s were considered in the analysis. The AC current, I, measured by the current probe, was the total transient response. When no inversion charge was present, the non-inversion response was measured.

5.2.2 The Applied Voltage Pulse

A closed form solution for the non-inversion response offers advantages in programming because both the current waveform and the voltage

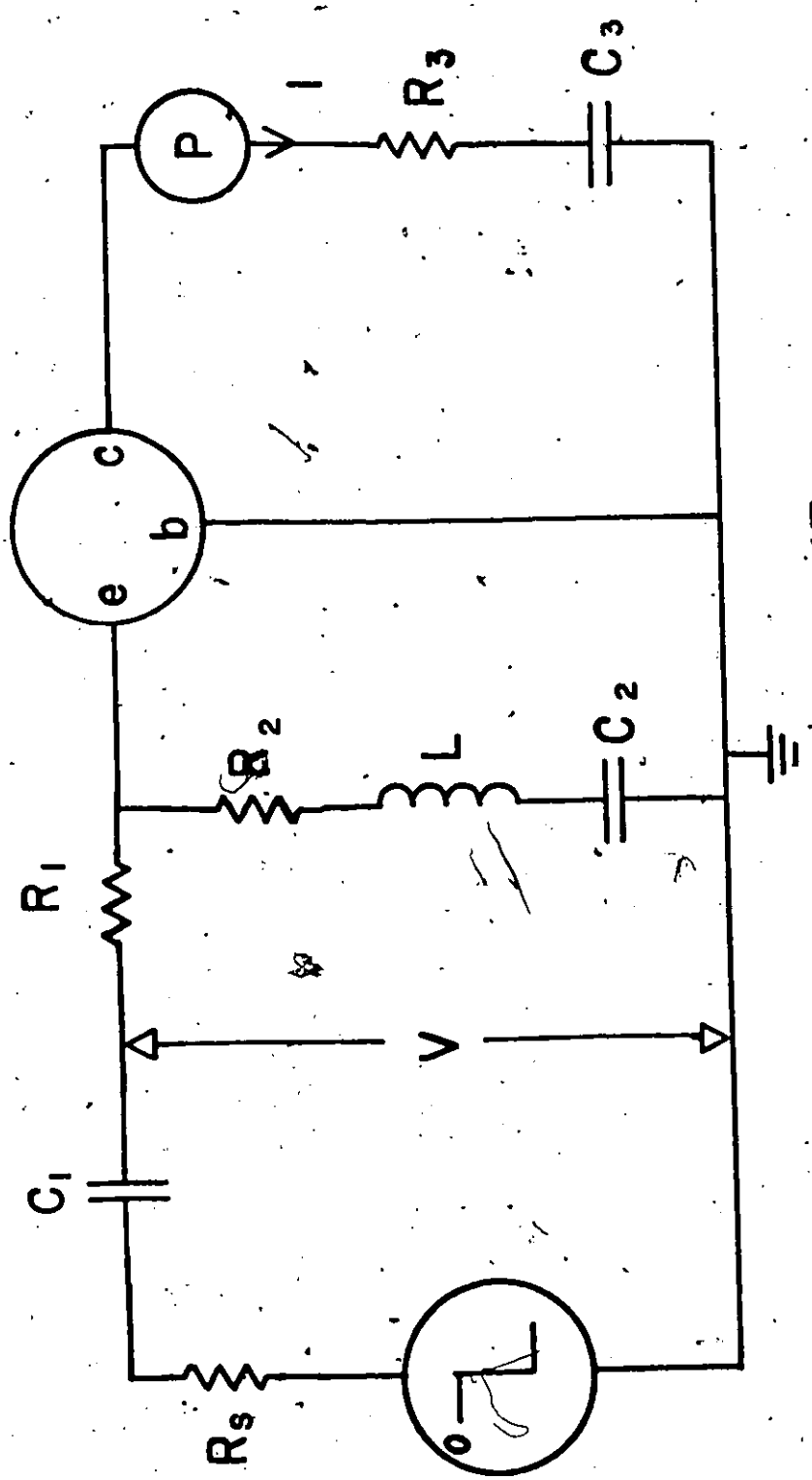


Figure 4.1 The AC equivalent test circuit

across the MOS capacitor are determined together. This solution requires an analytical expression for the applied voltage pulse. The expression is determined by considering V as the output of a network, when a step function is applied, and solving for the network transfer function using computer optimization techniques.

Initially a computer program written by Bereznai[148] was considered. This program gave a least squares fit to a general objective function for a two pole network. Regardless of the objective function selected, a satisfactory fit over only a limited portion of the waveform was possible.

A second program, written by Markettos[149], gave a least p. th fit using Fletcher's gradient technique[150] for a three pole network. A good overall fit was achieved for a p value of 10^3 (see Fig. 5.2). This expression was used to represent the applied voltage pulse in the calculations.

5.2.3 The Device Model

To achieve the object of this section, the development of a theoretical transient analysis to extract the material properties from the experimental results, it is necessary to derive a circuit model of the MOSCET, whose cross-section is shown in Fig. 2.5.

Both distributed and voltage dependent effects are present in the actual device but, in the first approximation these effects are ignored. In this case, the model consists of two capacitors and a resistor and is shown in Fig. 5.3(a). The MOS capacitor, C_{ox}, whose experimental values

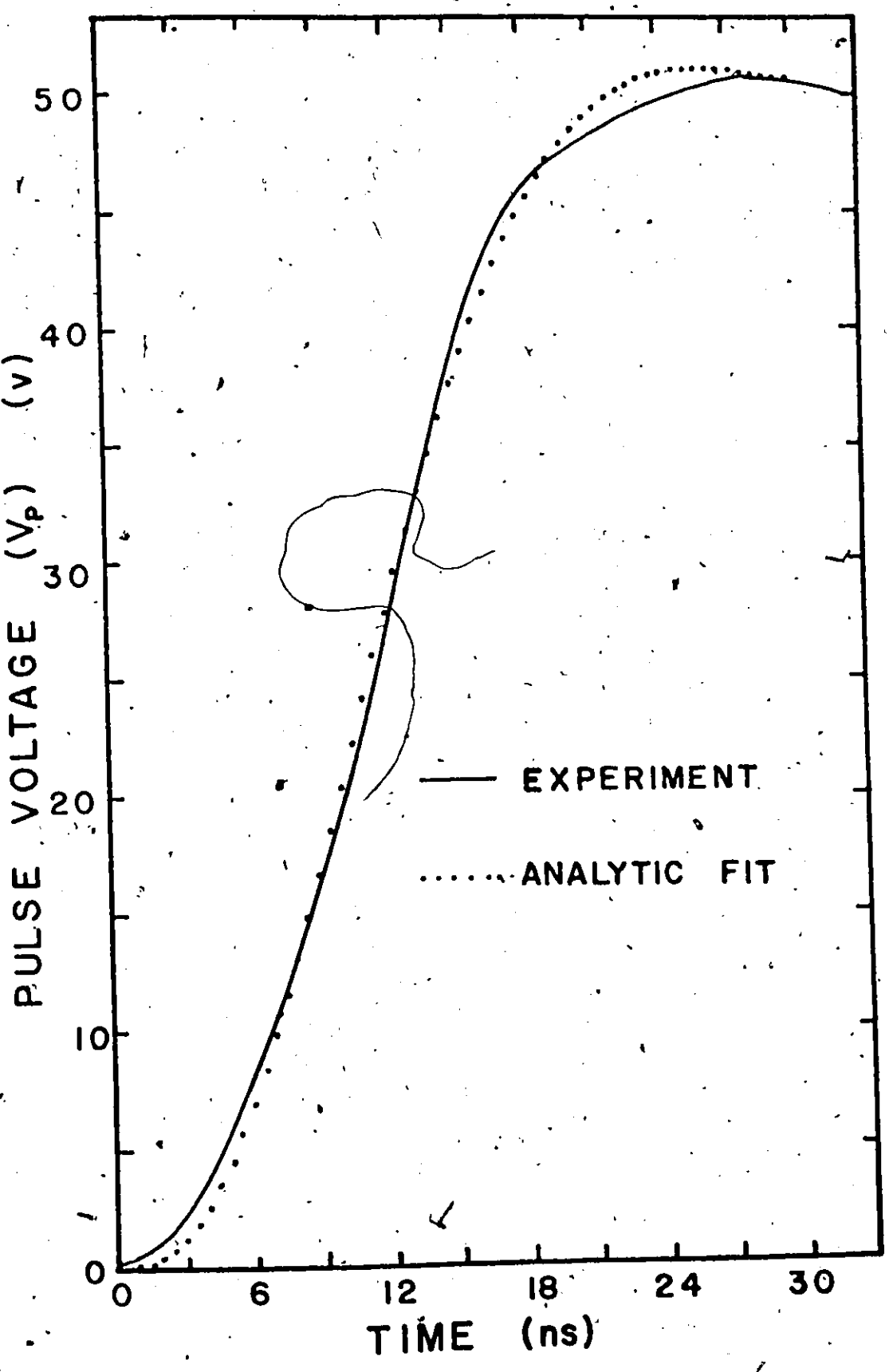
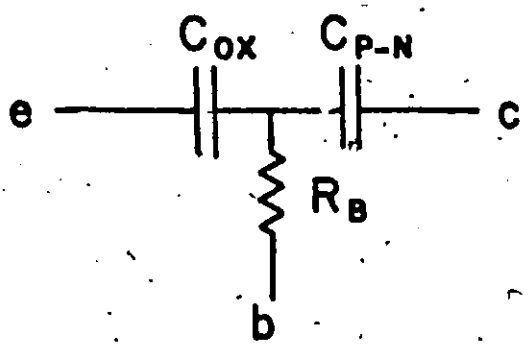
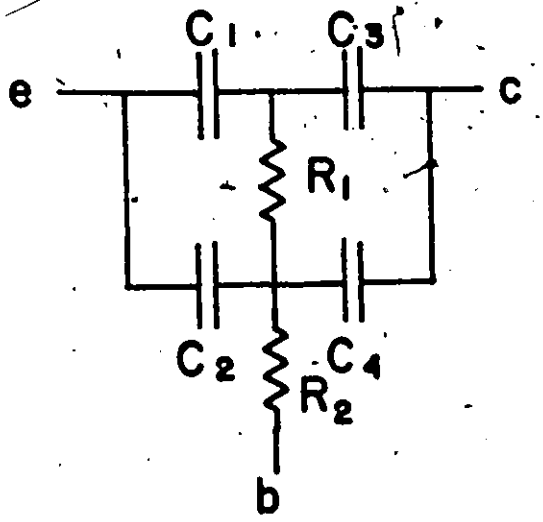


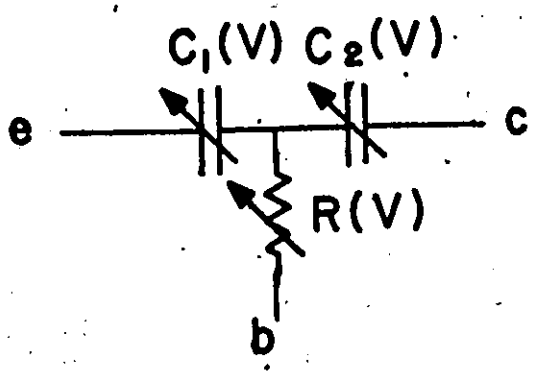
Figure 5.2 The experimental voltage pulse and the analytic fit



(a) The first approximation



(b) A second approximation considering distributed effects



(c) A second approximation considering voltage dependent components

Figure 5.3 Discrete component models of the MOSCET for the non-inversion response

are shown in Table 3.1, is the first capacitor. The second capacitor is the capacitance of the reverse biased p-n junction, C_{P-N}. The experimental results of Table 3.4 relate the value of C_{P-N} to the specific reverse bias voltages. The distributed base resistance, R_B, can not be measured and must be calculated from the following relationship.

$$R_B = \frac{\int i(x)\, R(x)\, dx}{\int i(x)\, dx} \qquad 5.2.1$$

The integrals of Eq. 5.2.1 are approximated by dividing the base into a number of concentric rings, calculating the resistance of each ring and summing the results.

Additional refinements which consider either distributed or voltage dependent effects are now considered.

Figure 5.3(b) shows a model which crudely considers the distributed nature of the MOSCET. The ratio of C_1:C_2 is selected arbitrarily but once selected it defines the ratio of C_3:C_4 and the values of R_1 and R_2.

$$C_1 + C_2 = C_{ox}$$
$$C_3 + C_4 = C_{P-N} \qquad 5.2.2$$

The values of R_1 and R_2 are calculated in the same manner as R_B.

Figure 5.3(c) shows a further model which considers the voltage dependence of the MOSCET. The voltage dependence of the MOS capacitor, $C_1(V)$, is shown in Fig. 3.3. The maximum change in capacitance with voltage is 6% for 80 V so, initially, $C_1(V)$ is considered equal to C_{ox}. As previously stated, the p-n junction capacitance, $C_2(V)$, is a strong function of the voltage (Fig. 3.8) which satisfies the expression

$$C_2(V) = 1.55 \times 10^{-10}(0.66 - V_A)^{-0.430} f \qquad 5.2.3$$

where V_A is the total applied voltage both DC and transient. The effect of depletion layer modulation on the base resistor is negligible so R(V) is equal to R_B.

5.2.4 Determination of the Non-Inversion Response

The model of Fig.5.3(a) was bread-boarded from discrete components, inserted into the test circuit, and the current waveform, I, measured. Figure 5.4 shows the measured response of a device and the bread-board model as well as the calculated curve. A computer program was written, using Laplace Transforms, which evaluated the response of the AC circuit (Fig. 5.1 including the device model of Fig. 5.3(a)) when the voltage pulse model (Fig. 5.2) was applied. The program determined not only the current waveform, I, but also the voltage across the MOS capacitor, V_p'.

The agreement between the measured pulse response of the device and the bread-board model (see Fig. 5.4) confirmed that the model was valid, providing the DC bias voltage on the p-n junction capacitor was large. The larger deviation for the calculated response was due to either the model of the voltage pulse (Fig. 5.2) or the AC equivalent circuit (Fig. 5.1). Calculations were undertaken using the computer program to test each of these possibilities. Initially the voltage pulse model was replaced by others derived using Bereznai's program.[148] Although better fits to the voltage pulse were achieved in specific regions, the overall fit was not as good.

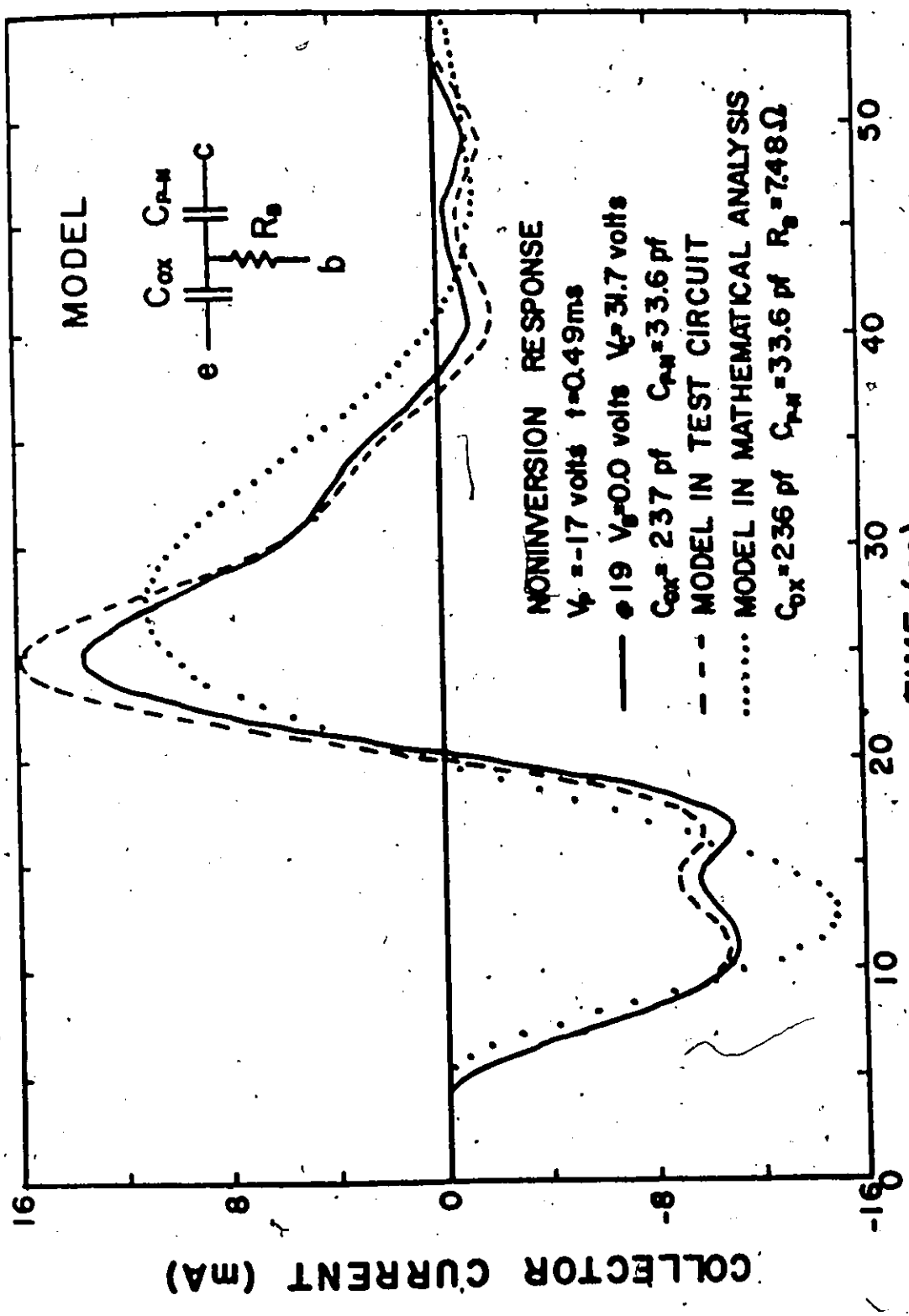


Figure 5.4 The theoretical and experimental non-inversion response of the MOSCET

It was noted, however, in the regions where the voltage pulse model was a better fit so was the calculated non-inversion response. Calculations of the non-inversion response were made, in which the equivalent circuit component values (particularly L) were varied over a considerable range but no overall improvement in the agreement between the calculated and experimental curves was observed. From these results it was concluded that the model of the voltage pulse was the limiting factor in the theoretical response. This was not at all unexpected as the non-inversion current response is essentially the second differential of the applied voltage waveform.

The results shown in Fig. 5.4 indicate that the simple model of the device is quite satisfactory in accounting for the normal non-inversion response. However, the other models were used to explain deviations from theory under particular conditions.

5.3 The Inversion Charge Response

5.3.1 Introduction

The device model (Fig. 5.3(a)) was extended to include an inversion charge by placing a voltage dependent current source in parallel with the p-n junction capacitor, C_{p-N}. The properties of the current source are determined by the release mechanism for minority carriers from the inversion layer, and their transport properties across the heavily doped layer. The voltage across the MOS capacitor, calculated in the non-

inversion analysis, controls the current generator. The values of the circuit components determine how the output of the current source (the inversion charge) is detected by the current probe.

5.3.2 The Transport Equation

The total electron current, J_n, in a semiconductor is

$$J_n = q(\mu_n\, nE + D_n\, \text{grad}\, n) \qquad 5.3.1$$

In this case E is the field due to the impurity gradient which is calculated from the relationship

$$E = \frac{-kT}{q}\,\frac{1}{N(x)}\,\frac{d\,N(x)}{dx} \qquad 5.3.2$$

Using the analytic expression derived in Chapter 3 for the impurity profile, N(x), (see Fig. 3.7) the internal field was calculated and the results are plotted in Fig. 5.5.

The continuity equation assuming no recombination or generation is

$$q\,\frac{\partial n}{\partial t} = \text{div}\, J_n \qquad 5.3.3$$

For the one dimension case; assuming that D_n is a constant, and that the Einstein relationship (Eq. 3.6.5) holds, Equations 5.3.1 and 5.3.3 combine to give

$$\frac{\partial n}{\partial t} = D_n\,\frac{\partial^2 n}{\partial x^2} + \mu_n\,\frac{\partial}{\partial x}(nE) \qquad 5.3.4$$

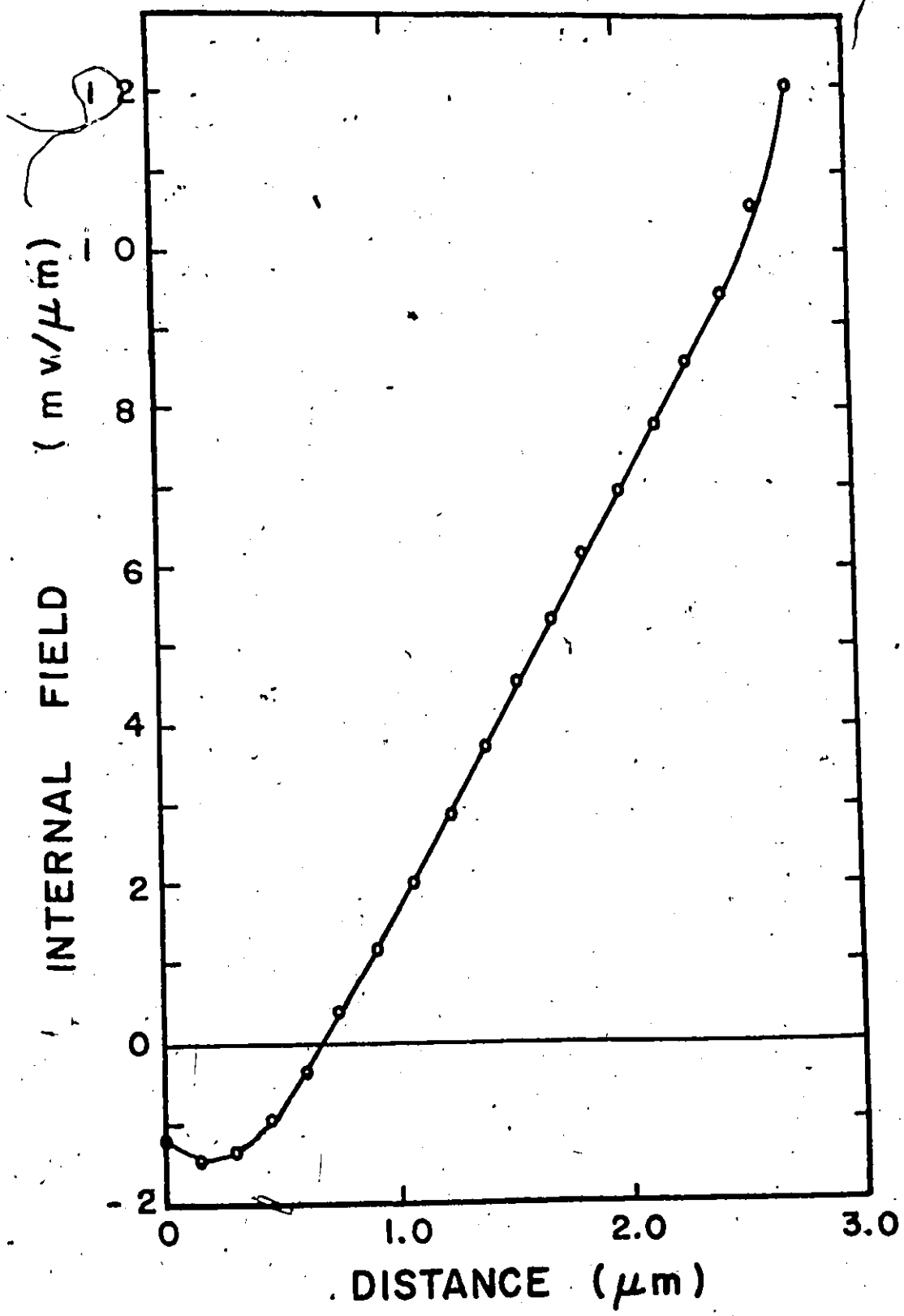


Figure 5.5 The internal field across the diffused layer

Boltaks[91] discusses solutions to this equation and from his work it is apparent that a closed form solution is not possible. Consequently finite difference techniques[151,152,153] were applied to Eq. 5.3.4. From Fig. 5.5, it can be seen that the internal field is small and has a zero crossing. Consequently, the finite difference formulation is simplified by assuming the field term is small, relative to the diffusion term, and the finite difference formulation of Eq. 5.3.4. can then be expressed as

$$n(x_o,t_o + \Delta t) = (1 - 2D_n \frac{\Delta t}{(\Delta x)^2})\, n(x_o,t_o) + D_n \frac{\Delta t}{(\Delta x)^2}\, n(x_o + \Delta x, t_o)$$
$$- \mu_n \frac{\Delta t}{\Delta x} E(x_o + \Delta x)\, n(x_o + \Delta x, t_o) + D_n \frac{\Delta t}{(\Delta x)^2}\, n(x_o - \Delta x, t_o)$$
$$+ \mu_n \frac{\Delta t}{\Delta x} E(x_o - \Delta x)\, n(x_o - \Delta x, t_o) \qquad 5.3.5$$

where, to achieve a stable solution with the assumption of a small field component, the following conditions

$$D_n \frac{\Delta t}{(\Delta x)^2} < 0.5 \qquad \text{(a)}$$
$$D_n \frac{\Delta t}{(\Delta x)^2} > \mu_n E \frac{\Delta t}{\Delta x} \qquad \text{(b)} \qquad 5.3.6$$
$$(1 - 2D_n \frac{\Delta t}{(\Delta x)^2}) \geq D_n \frac{\Delta t}{(\Delta x)^2} \qquad \text{(c)}$$

must be satisfied. Equation 5.3.6(a) is a relationship governing the values of the incremental distance, Δx, and time, Δt, for a stable solution. Equation 5.3.6(b) is a mathematical relationship which states the field term must be small relative to the diffusion term. Equation 5.3.6(c) applies a tighter

constraint on the incremental time and distance which allows terms to be cancelled.

From Fig. 3.7 an average impurity concentration is determined. Using Wolf's curves[96] this yields a value of 6.0 cm^2/s for the average electron diffusivity, D_n.

To determine the grid for the finite difference solution to the transport equation, it is necessary to know the distance, from the oxide-semiconductor surface to the edge of the depletion layer of the p-n junction diode, over which the equation applies. The depth of the metallurgical junction was determined during profiling (Section 3.4) and Lawrence and Warner's curves[126] relate the depletion layer width to the bias voltage on the diode. For the test structure, with 40 V reverse bias on the diode, the distance from the oxide semiconductor interface to the edge of the diode depletion layer was 2.7 μm. Selecting a grid with 12 points across this distance, the incremental distance, Δx, was

$$\Delta x = 2.45 \times 10^{-5} \text{ cm} \qquad 5.3.7$$

and to satisfy Eq. 5.3.6(a) and (c)

$$\Delta t = 3 \times 10^{-11} \text{ s} \qquad 5.3.8$$

The two boundary conditions are considered next. To apply the boundary conditions it is necessary to understand the finite difference formulation. At each point on the grid and during each increment of time, Δt, the charge has three options; it can remain at the point or move one

increment, Δx, in either direction. For diffusion, the amounts moving in either direction are equal. A superimposed field results in more charge moving in the direction of the field than against it. The boundary conditions consider what the charge does at the end points of the grid.

At the oxide-semiconductor boundary the component of charge moving towards the oxide must be considered. The surface may be considered a perfect absorber, in which case the charge remains at the surface, or a perfect reflector, in which case the charge bounces off and moves to the next grid point. Intermediate cases where the charge divides between these two extremes are easily considered.

At the diode boundary it is assumed that all charge reaching the edge of the depletion layer is collected immediately. This means all charge reaching the final grid point is removed from the system and the component of charge moving towards the surface from this point is always zero.

A computer program was written using the finite difference formulation of Eq. 5.3.5 to determine the charge collected as a function of the initial and boundary conditions.

To demonstrate the effect of the internal field Fig. 5.6 shows the charge collected with and without the internal field. These calculations were made, assuming, as an initial condition, a delta function of charge at the semiconductor-oxide interface and a perfect absorber as the boundary condition.

Figure 5.6 shows pulses with transit times of 2 and 4 ns respectively (the transit time to a point is defined as the time necessary for one half the released charge to reach that point). These results are consistent

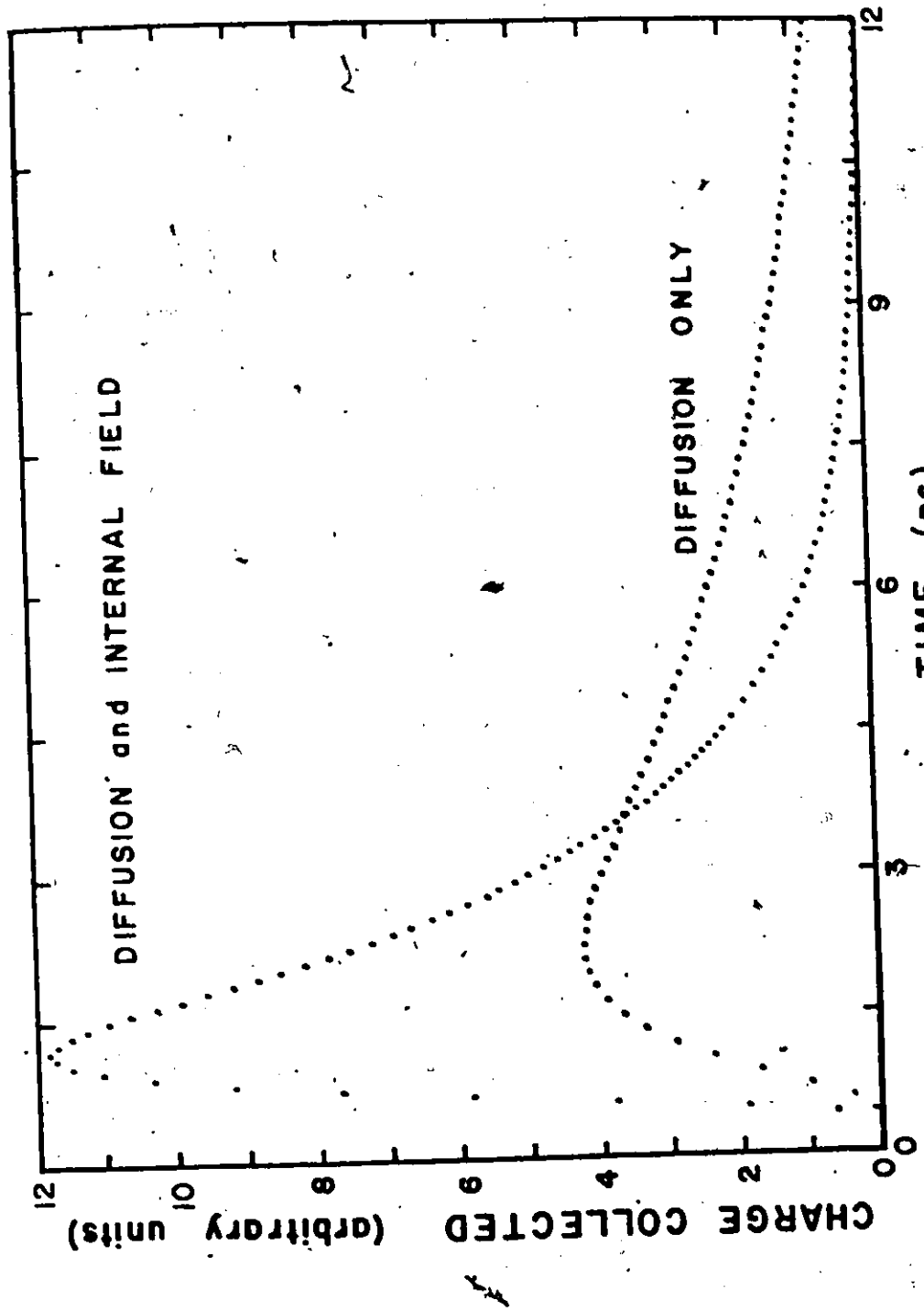


Figure 5.6 The calculated collected charge with and without internal fields. Initial conditions is a delta function at the surface. Boundary condition at the surface is a perfect absorber

with the calculated transit times of electrons across the bases of transistors.[154,155,156]

It is necessary to test whether the following assumptions, made in deriving the finite difference formulation of the transport equation, introduce significant errors. These assumptions are that the electron diffusivity, D_n, is a constant and that the field term is small relative to the diffusion term. The transit time was the criteria selected to evaluate the errors and Table 5.1 shows the transit time and percentage of the total transit time at each point calculated using the assumptions.

To test whether the variation in D_n which is a function of the doping density (see Fig. 3.7) affected the solution, the layer was divided into sections each of which had a different value of D_n. The transit times for each section were determined, the results summed and compared with the transit time for the constant value. The two values agreed within 5% which was quite acceptable. This was not surprising since the electron spent over 80% of its time in the first 1.5 μm where the variation of D_n from the constant value of 6.0 cm^2/s was small and approximately equal in either direction.

Since the field term calculated from the internal field of Fig. 5.5 was always less than the diffusion term, Eq. 5.3.8(b) was satisfied. However, it must be determined whether the field terms were sufficiently small to avoid significant errors. To accomplish this, the layer was divided into several regions with different perturbations being applied to the field. After a series of trial solutions, it was determined that the transit time calculated using the small field assumption, was accurate within 10% which

TABLE 5.1 TRANSIT TIMES ACROSS THE BASE

Distance (μm)	Perfect Absorber		Perfect Reflector	
	Transit Time (Δt)	% Total Transit Time	Transit Time (Δt)	% Total Transit Time
.245	5 - 6	8	0 - 1	1
.490	22 - 23	33	13 - 14	23
.735	37 - 38	54	27 - 28	47
.980	46 - 47	67	36 - 37	62
1.225	52 - 53	76	42 - 43	72
1.470	56 - 57	82	46 - 47	79
1.715		87	50 - 51	86
1.960	62 - 63	91	53 - 54	91
2.205	67 - 68	98	57 - 58	97
2.695	68 - 69	100	59 - 60	100

$\Delta t = 3 \times 10^{-11}$ ns

was acceptable. This was not unexpected since in the first 1 μm, where the electron spends over 60% of its time (Table 5.1), the field term was definitely small (less than 15% of the diffusion term) and it changed sign (see Fig. 5.5).

Having established the validity of this form of the transport equation, it was extended to include recombination as the charge crosses the diffused layer by assuming the following simple exponential recombination relation

$$n(t) = n_o e^{-t/\tau} \qquad 5.3.9$$

The fraction of the charge which has not recombined during an increment of time, Δt, is

$$m = e^{-\Delta t/\tau} \qquad 5.3.10$$

To include recombination in Eq. 5.3.5, all terms at time t_o are multiplied by m. With the finite difference form it is a simple matter to make m a function of x and to have a separate lifetime, τ, for each grid point. In particular, this allows an additional surface recombination component[161] to be considered.

5.3.3 The Release Mechanism

If the transit time is much larger than the risetime of the pulse, the charge may be assumed to be released as a delta function at zero time. The collected charge, as shown in Fig. 5.6, has a transit time of 2 ns while

the risetime of the pulse used was 20 ns. Thus this assumption can not be used and the voltage pulse shape must be considered explicitly.

One way to consider the shape of the voltage pulse is to divide it into a series of increments each of which releases an inversion charge proportional to its amplitude. The inversion charge pulse was calculated using the computer program described previously and this release mechanism. The calculated and experimental waveforms were compared and they did not agree. The calculated pulse started much earlier, rose more slowly to a lower peak and had longer and more gradual tail than the experimental pulse.

Three others[51,157,158] have considered the movement of inversion charge released when a pulse was applied to the MOS capacitor. Tomanek[157] used very large pulses sufficient to move the device well into accumulation and encountered no difficulties. The others[51,158] observed that the charge was greatly delayed and did not obey the simple recombination model when low amplitude pulses, insufficient to move the device into accumulation, were used. These results were explained by a diode-like model with a barrier at the surface.

This model of the release mechanism is used in the study. The model is derived for the case where the voltage pulse is only sufficient to move the device from one point in inversion to another. The surface potential does not change rapidly in inversion and it is assumed to be a constant (the inversion potential). The number of minority carriers, Δn, released per increment of time, Δt, is determined by the expression

$$\Delta n = n^* e^{-\phi_o(V_I - V_p'(t) + [Q_I(0) - Q_I(t)]/C_{ox})^2 \, q/kT} \qquad 5.3.11$$

The height of the barrier is the inversion potential, ϕ_I, and ϕ_o is defined to satisfy the relationship

$$\phi_I = \phi_o(V_I)^2 \qquad 5.3.12$$

so that, prior to a voltage pulse being applied, the device is in the normal equilibrium inversion configuration of Fig. 3.1(c). The values of the inversion potential, ϕ_I, and the inversion voltage, V_I, were determined using the MOS capacitor program.[18] The voltage across the MOS capacitor, $V_p'(t)$ was calculated during the non-inversion response and is plotted in Fig. 5.7. Also shown in Fig. 5.7 is a piece-wise linear fit used to represent $V_p'(t)$ in the computer calculations involving Eq. 5.3.11. Since the barrier must be lowered approximately half way before significant charge is released, it is not necessary to fit the beginning of V_p' well. It is only necessary to know the time between the beginning of the pulse and the fit so the non-inversion and inversion pulses can be joined together. The term $[Q_I(0) - Q_I(t)]/C_{ox}$ acts to restore the barrier to its equilibrium position as the charge crosses the barrier and leaves the inversion layer. The amount of charge which has left the surface at time, t, is $[Q_I(0) - Q_I(t)]$. The number of electrons, n*, which try to cross the barrier in Δt is given by the expression

$$n^* = Q_I(t)\, n/q \qquad 5.3.13$$

where n is the factor which determines how often each electron tries to

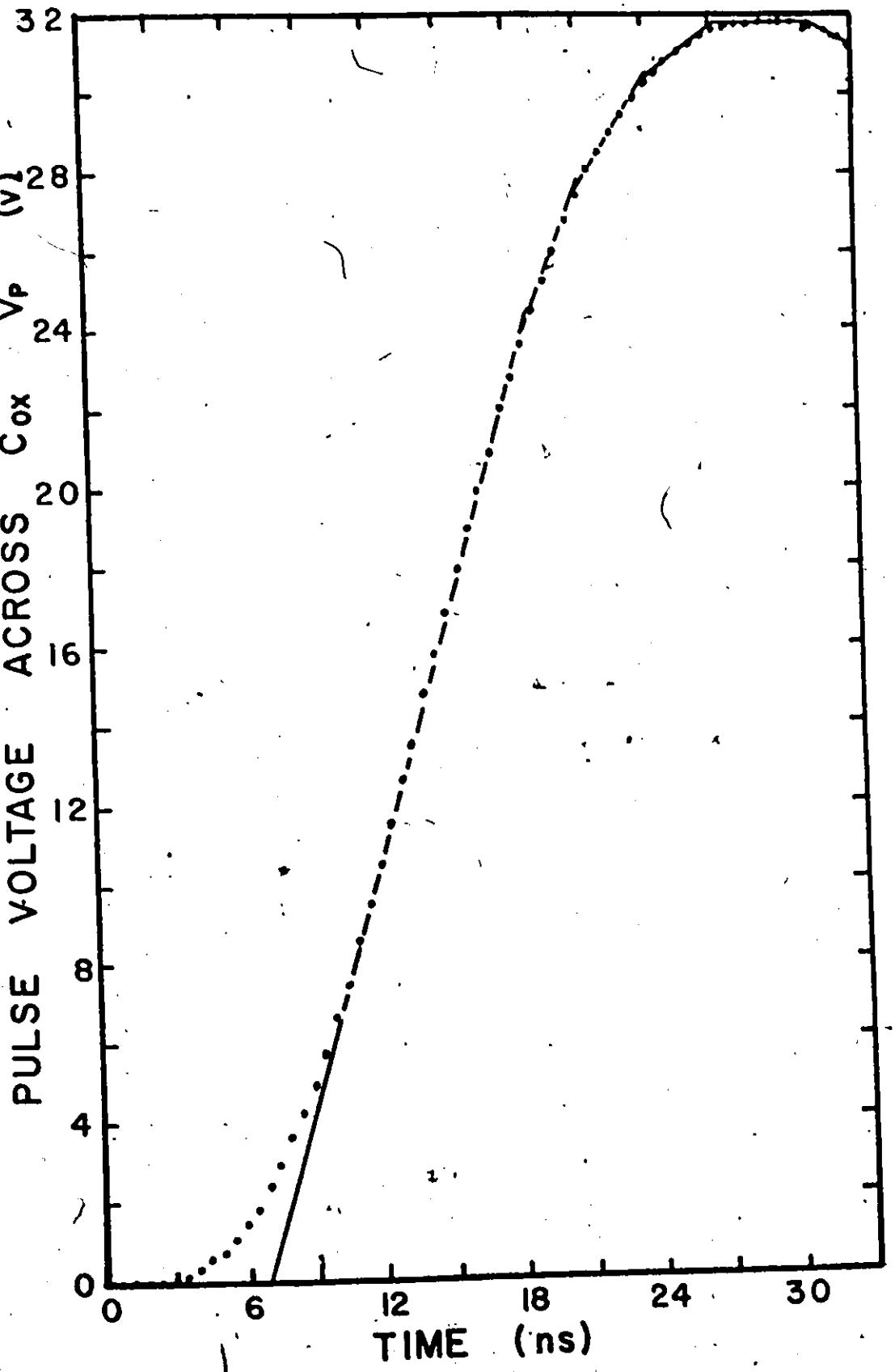


Figure 5.7 The calculated voltage pulse across the MOS capacitor and the piece-wise linear model used in programming (V_p = 50 v)

cross the barrier in Δt

$$n = \Delta t / t_d \qquad 5.3.14$$

where t_d is the dielectric relaxation time.

This model of the release mechanism was used to expand the finite difference computer solution to the transport equation.

5.3.4 The Circuit Response

Combining the release mechanism with the transport equation gives the response of the voltage dependent current source. However, this is not the pulse observed by the current probe. The observed pulse is the response of the network which must be related to the current source output.

When considering the circuitry involved in this analysis everything except the collector loop is ignored. Figure 5.8 shows the collector loop circuit. Since the charge from the current source must divide so the same voltage is present across the current source in each loop, the following equations must be satisfied

$$\Delta v = \frac{\Delta Q_1}{\Delta t} (R_B + R_3) \qquad 5.3.15$$

$$\Delta v = \frac{\Delta Q_2}{C_{P-N}} \qquad 5.3.16$$

$$\Delta Q_1 = \frac{\Delta Q_2 \, \Delta t}{C_{P-N}(R_B + R_3)} \qquad 5.3.17$$

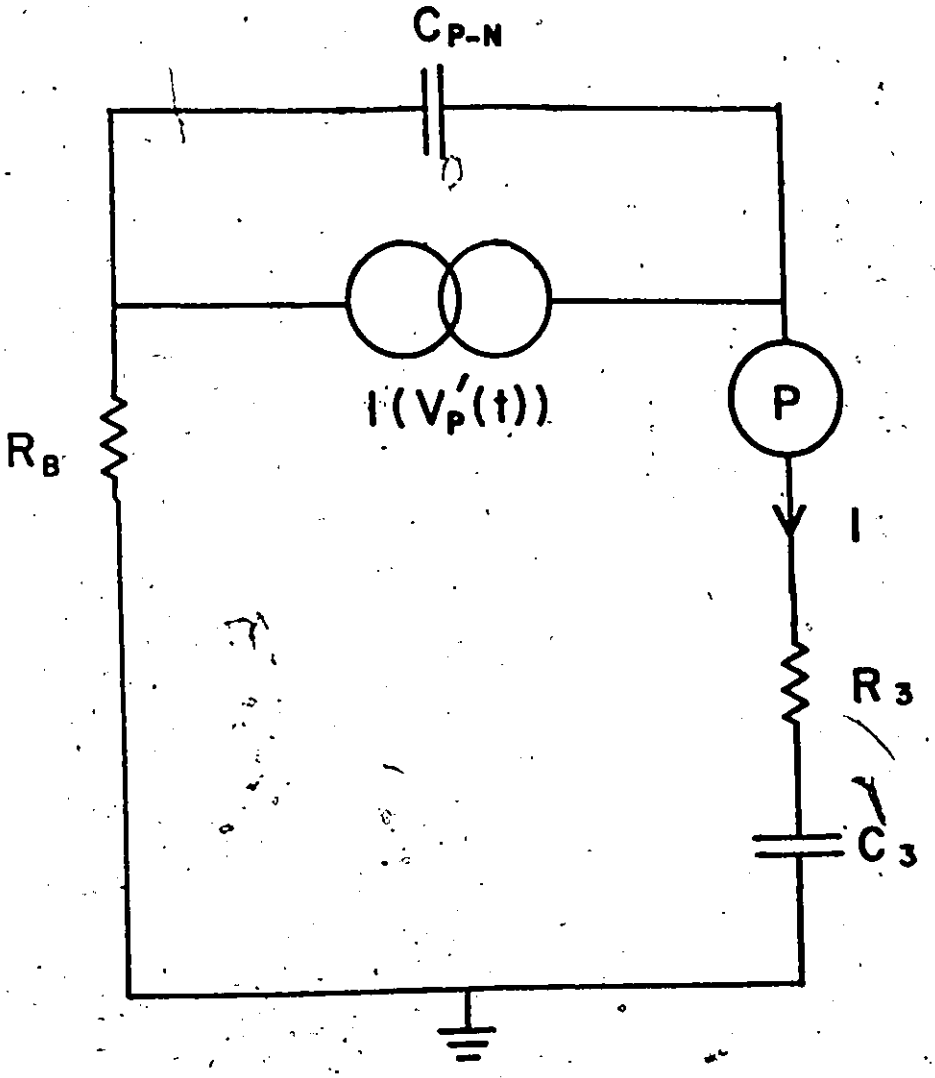


Figure 5.8 The collector circuit, including the voltage dependent current source

Equation 5.3.17 shows how the charge divides between the two loops. Since the current detected by the probe is $\Delta Q_1/\Delta t$, the inversion pulse can now be calculated.

The voltage dependence of the diode capacitor, C_{P-N}, could introduce an additional effect (see Lin[159]) but it was not considered significant.

5.3.5 Determination of the Inversion Charge Response

The computer program based on the release mechanism, transport properties, and recombination lifetime was used to determine the output of the current source. From this output and the collector circuit parameters, the inversion charge response was determined using Eq. 5.3.17. Figure 5.9 shows a calculated and an experimental inversion charge pulse. The excellent agreement between the calculated and experimental curves of Fig. 5.9 confirmed the theoretical analysis.

All of the values necessary to calculate the inversion response except the recombination lifetime were determined previously. The average recombination lifetime was determined by calculating theoretical curves for different lifetimes and comparing the results with experiment. The fit between theory and experiment in Fig. 5.9 established that the average recombination lifetime was 17 ns and that this value was accurate within ±20%.

An attempt was also made to determine the recombination lifetime across the layer when a surface component was present. A series of solutions were calculated in which the bulk lifetime increased as the surface

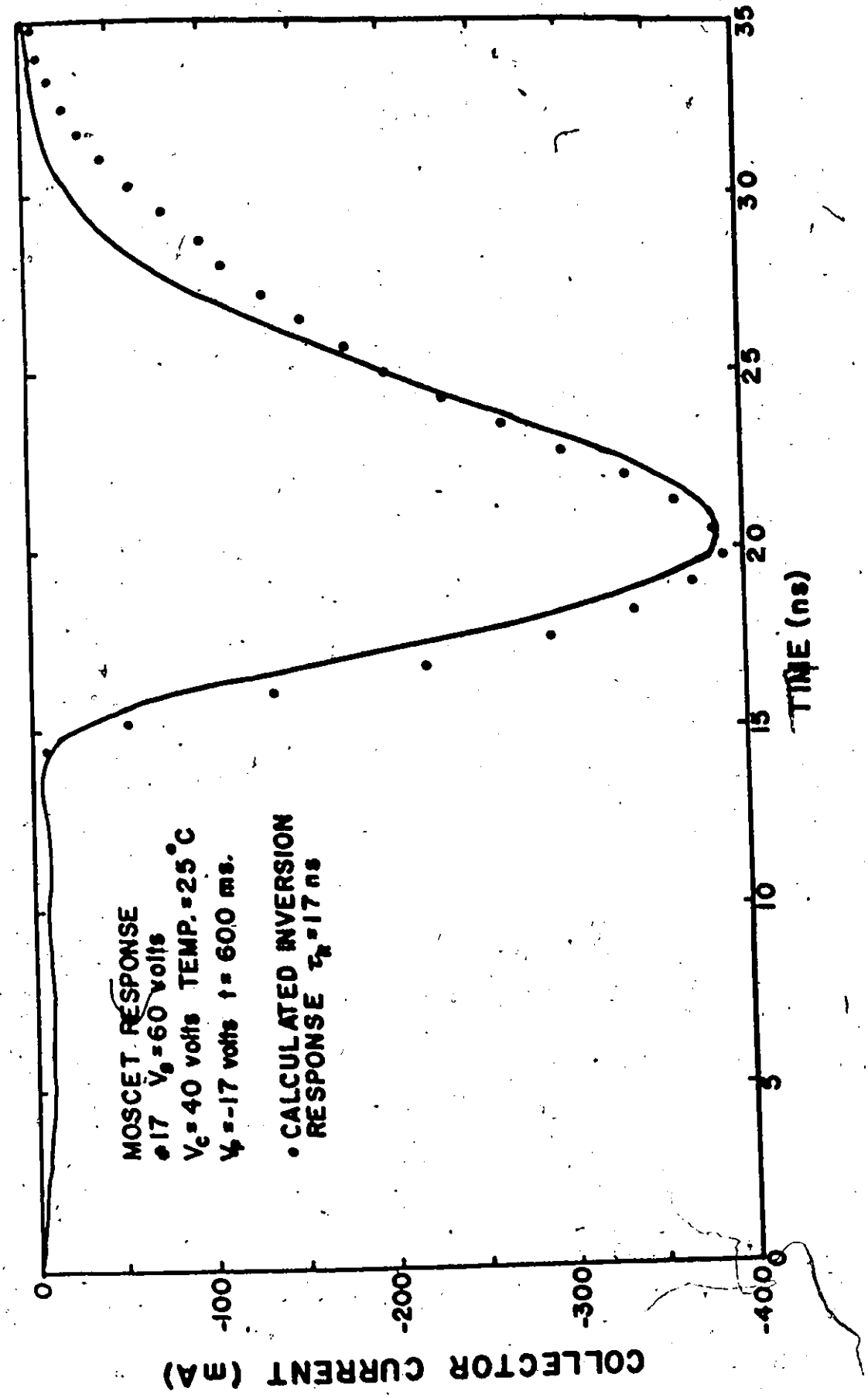


Figure 5.9 The calculated and experimental inversion response

recombination component increased. The shape of the theoretical pulse changed gradually but the overall fit between theory and experiment remained essentially constant. This is because the release mechanism at the surface controls the position and shape of the current source output. The circuit response of the collector circuit (the charging and discharging of the diode capacitor, C_{p-N}, through the total resistance, $R_B + R_3$) smooths and controls the observed charge pulse shape. The charge transport across the layer (during which recombination occurs) was so fast it has little effect on the pulse shape. The refinement, using surface and bulk lifetimes, did not improve the fit, so it was not used.

5.4 Conclusions

The first model (Fig. 5.3(a)) of the MOSCET was found to yield a non-inversion response in excellent agreement with experiment. In calculating the non-inversion response, the model of the voltage pulse was the accuracy limiting factor rather than the device model.

The calculated inversion pulse response was found to be in good agreement with the experimental results. The release mechanism at the interface determined the pulse position and influenced the pulse shape. The pulse shape is a strong function of the charging and discharging of the diode capacitor in the collector circuit. While the pulse shape was not sufficiently sensitive to the transport parameters (diffusion constant, internal field, surface boundary conditions and lifetime) that slight changes in these values could be detected, these parameters were important in the total solution.

CHAPTER 6

THE MOSCET RESULTS

The theoretical response of the MOSCET, for various external parameters, was calculated using the computer programs developed in the previous chapter. By comparing these with experimental results, the material properties of the thin heavily doped layer were determined.

6.1 The Non-Inversion Response

The first experimental quantity studied was the non-inversion response. To facilitate this study, it was necessary to define a parameter to characterize the response. The parameter selected was the charge in the second lobe of the non-inversion response, Q_{N-I}, determined by measuring the area under the curve using a polar planimeter.

Before proceeding further, the model of the MOSCET, used in calculating the non-inversion response, is reviewed because of its significance in this section. The model shown in Fig. 5.3(a) consists of the oxide capacitance of the MOS capacitor, C_{ox}, the reverse biased p-n junction capacitor, C_{p-N}, and the distributed base resistance, R_B.

6.1.1 Experimental Results and Discussion

First the uniformity of the devices was determined. Table 6.1 shows

TABLE 6.1 EXPERIMENTAL RESULTS FROM THE MOSCET

Device	Non-Inversion Charge 10^{-12} coulomb	Inversion Potential Volts	Fixed Oxide Charge 10^{11} states/cm^2	Q-V Slope pf	Generation Time Constant ms.	Activation Energy eV
E-7	102.75					
C-10	101.25	28.2	9.55	133.2		
B-13	95.8	31.4	4.85	137.3		
H-12	108.5	30.3	6.46	130.6	129	.397
G-15	110.0	31.4	4.85	136.4	115	.348
F-14	109.2	33.2	2.20	136.8	113	.380
I-17	110.1	29.8	7.20	135.4	117	.374
A-19	100.7	30.2	6.61	139.3	111	.364
K-4	109.25	30.7	5.88	141.4	85	.342
D-8	110.6	29.7	7.34	140.6	141	.342
L-5	107.2	30.9	5.58	139.1	104	.331
Average	105.9	30.6	6.02	137.0	114.4	.360
σ	5.0	1.3	1.93	3.3	16.5	.023
%σ	4.7	4.2	32.1	2.4	14.5	6.4

the non-inversion charge, Q_{N-I}, (measured at 25°C for V_B = 0 V, V_C = 40 V and V_p = -50 V) for the different devices. The agreement from device to device was good with a standard deviation, σ, of 4.7%. This value was larger than the σ value of 1.7% observed for both C_{ox} and C_{P-N} but the capacitance bridge used for these measurements was accurate to within a fraction of a percent while the accuracy of the system to determine the non-inversion charge was ±3%. When the measurement errors were considered, the observed deviation in Q_{N-I} was less than the deviation calculated from the device model by considering the deviation of the individual components. These results confirm that the non-inversion response was the same for all devices tested and the observed deviations were consistent with the theoretical model.

Since the model components, C_{ox}, C_{P-N}, and R_B are independent of the repetition rate of the applied voltage pulses the non-inversion response was also assumed to be independent. The non-inversion response was measured for pulse repetition rates between 1 and 1000 Hz and the curves were identical, confirming the assumption.

The temperature dependence of the non-inversion response was considered next. By studying the inverse Laplace Transformation used in calculating the non-inversion response, the resulting temperature dependence can be related to the temperature dependence of the model components. The two capacitors C_{ox} and C_{P-N} are independent while the temperature dependence of R_B is +0.2% per °C.[160] The numerator of the transform is a linear function of R_B while the denominator is a weaker function, consequently the temperature dependence should be positive and less than 0.2% per °C.

The non-inversion response was measured as a function of temperature (0° to 90°C in 10° steps). These results are shown in Fig. 6.1. The very small temperature dependence was determined using a least squares fit to the data. It was found to be

$$Q_{N-I} = 106.86 + 0.0537\ T \qquad 6.1.1$$

where T was in degrees C. The observed temperature dependence of +0.05% per °C confirmed the theoretical prediction.

The non-inversion response was measured as the MOS capacitor was biased from accumulation to the onset of inversion. The experimental results were constant, verifying the assumption that the non-inversion response is independent of the MOS capacitor bias voltage.

The non-inversion response was a very strong, but complex, function of the capacitance of the reverse biased p-n junction diode, C_{p-N}. Theoretical curves of the non-inversion response were calculated for different values of C_{p-N} and the results compared with the experimental curves. Although the absolute values did not agree, when the theoretical curve was matched to the experimental curve at C_{p-N} of 30 pf (Fig. 6.2) the excellent agreement between theory and experiment confirmed this dependence.

The theoretical analysis of the MOSCET predicts that the non-inversion response is a very strong function of the leading edge of the voltage pulse, V_p, since it is essentially the second differential of V_p. The differences in the non-inversion curves of Figures 4.3 and 5.4 which were generated by two different voltage pulses, with slightly different

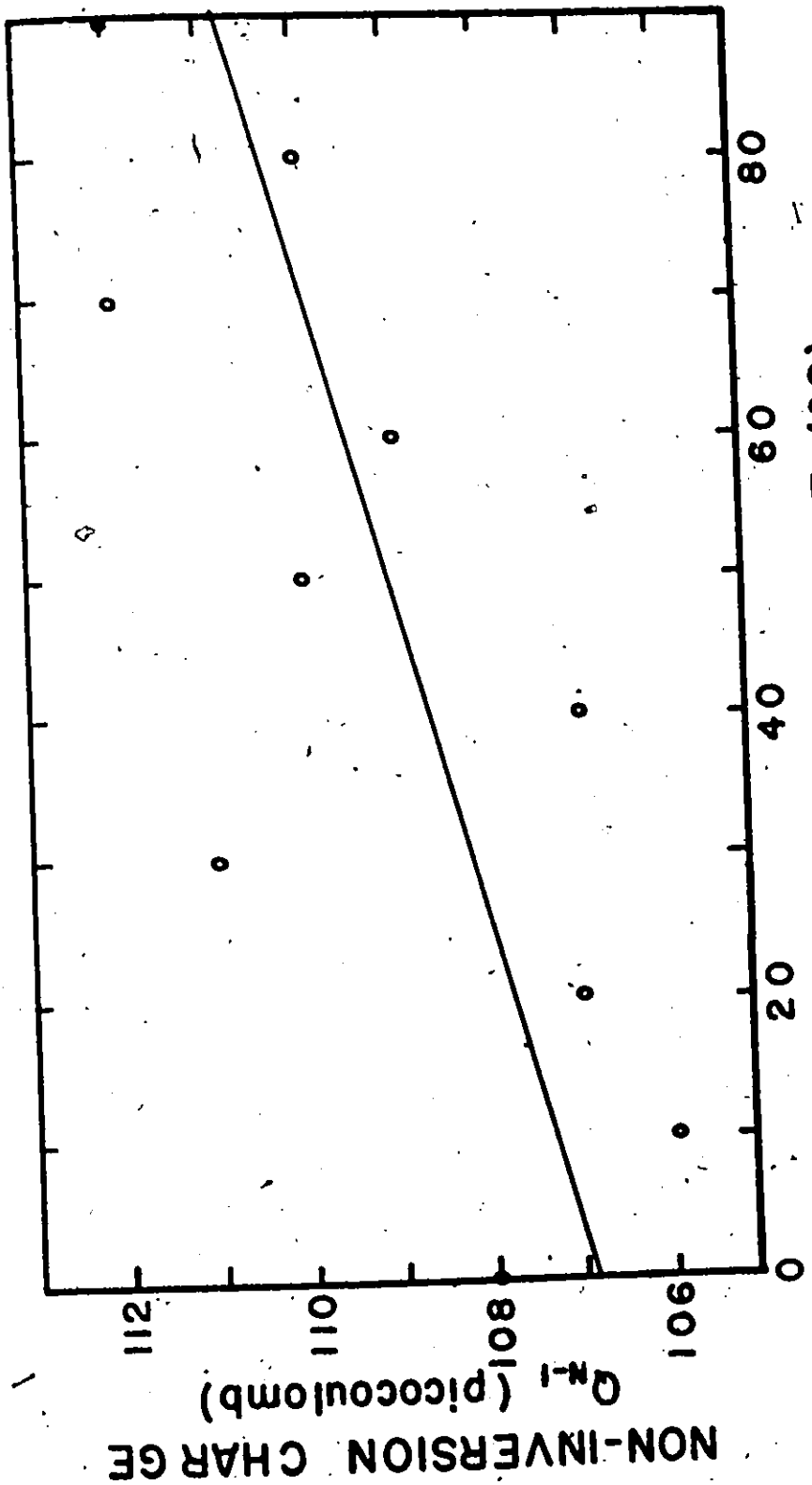


Figure 6.1 The variation of the non-inversion response with temperature

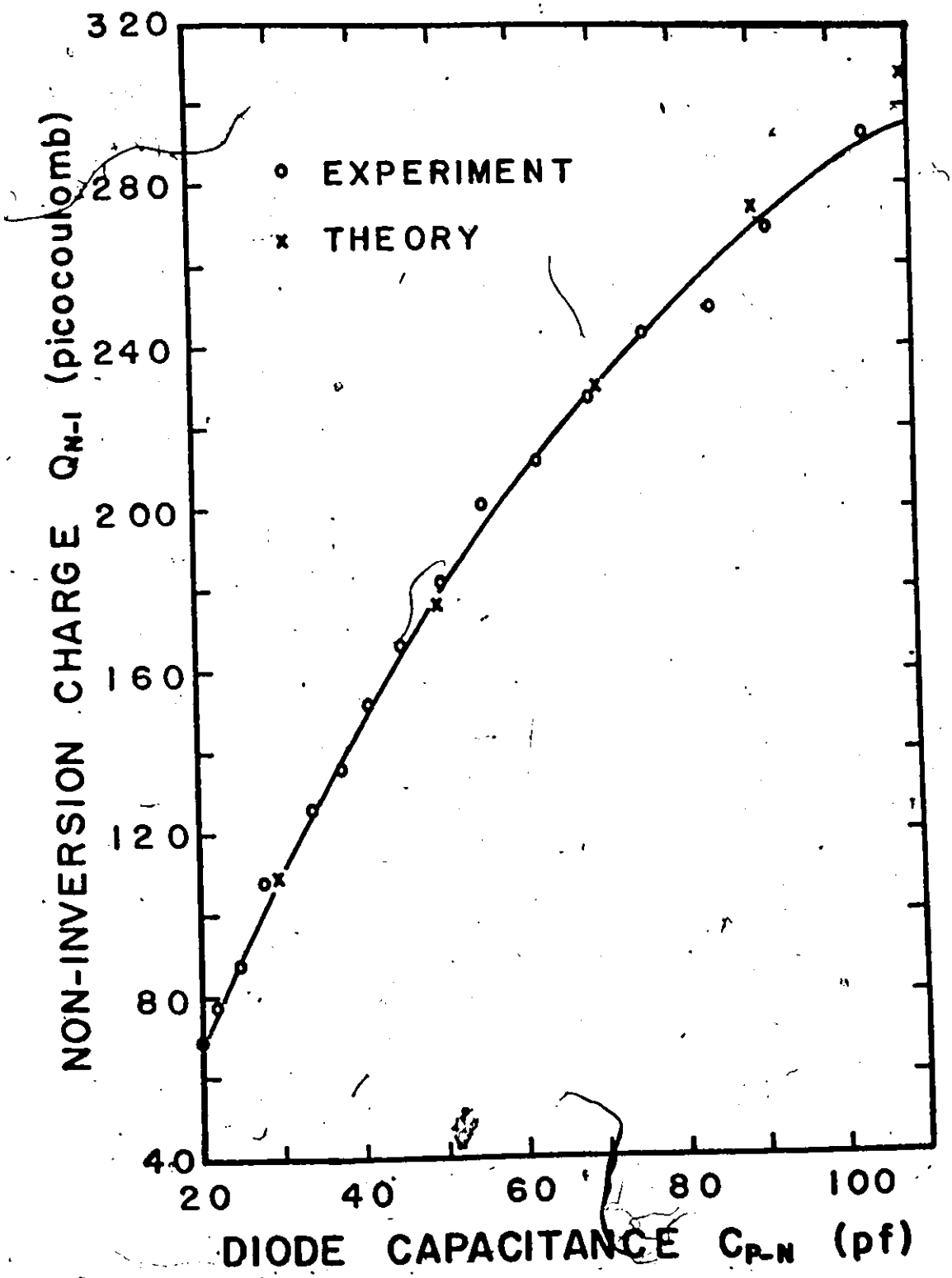


Figure 6.2 The effect of the reverse biased p-n junction capacitance on the non-inversion response

leading edges (11.5 and 13.5 ns risetimes), clearly show this strong dependence. However, until better modeling techniques are available for V_p, a good match between theory and experiment cannot be expected.

The theoretical analysis predicts that Q_{N-I} is a linear function of the amplitude of the applied voltage pulse, V_p. Figure 6.3 shows the measured values of Q_{N-I} as V_p was varied and the results satisfy the linear relationship predicted by theory.

6.1.2 Conclusions

The theoretical analysis of the non-inversion response based on the first model of the MOSCET (Fig. 5.3(a)) satisfactorily predicted the experimental results. However, the more complex models which consider distributed effects (Fig. 5.3(b)) and voltage dependent components (Fig. 5.3(c)) are worth considering briefly. It was established experimentally that,over the normal operating range, the distributed effect was much more important than the voltage dependent effect. Calculations using the distributed model (Fig. 5.3(b)) resulted in a slight improvement in the absolute fit but introduced no new information on device operation. These changes are not sufficient to warrant the complex calculations when the distributed model is used, particularly when the model of the applied voltage pulse, rather than the device model, limited the theoretical accuracy. Only when the DC bias voltage on the p-n junction capacitor, V_c, is small does the voltage dependent model become significant. It helps to account for the slight deviation between theory and experiment in Fig. 6.2 for large values

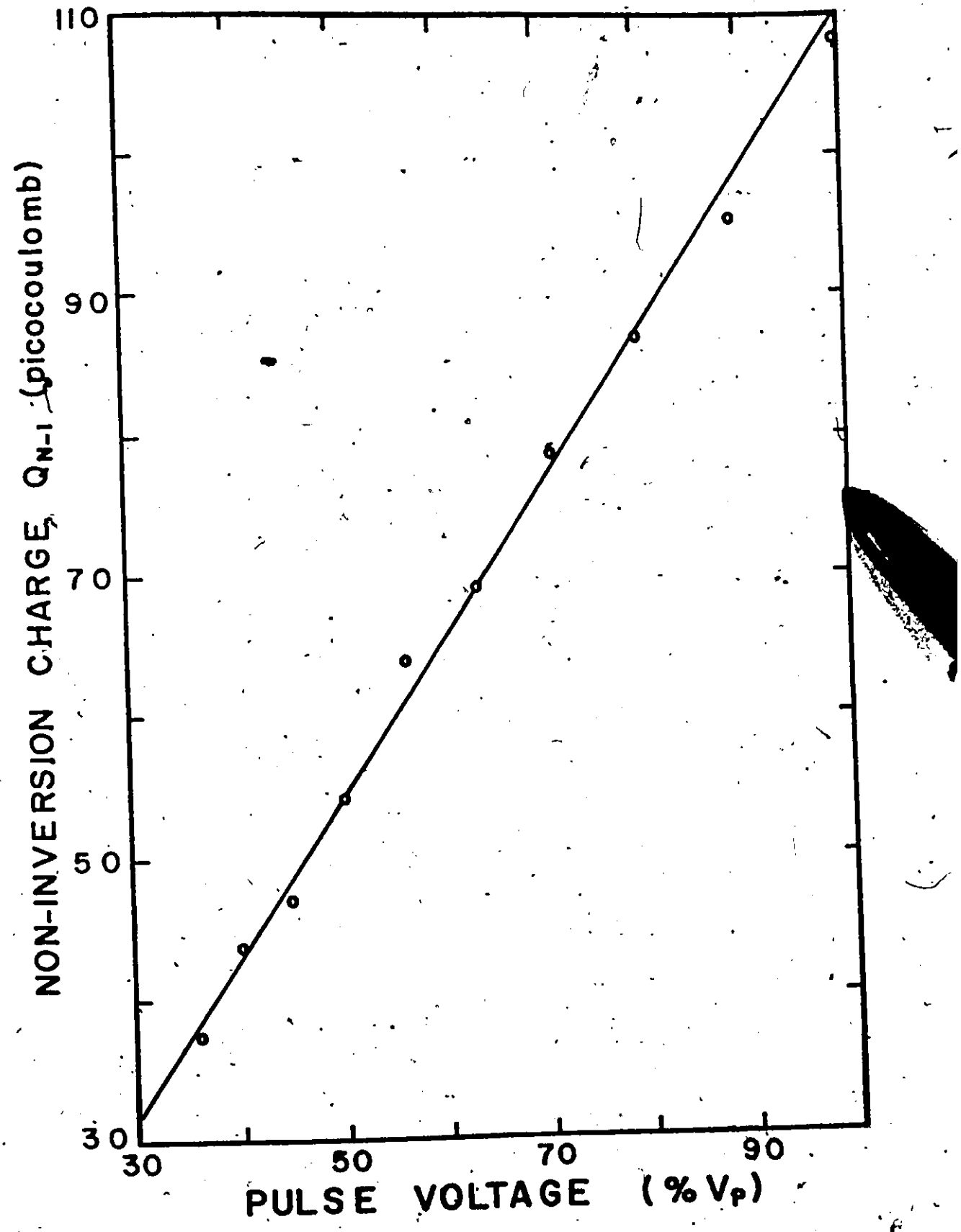


Figure 6.3 The non-inversion response as a function of the applied voltage pulse amplitude

of C_{P-N} (see Table 3.4 to relate C_{P-N} to V_c).

6.2 Generation

The minority carriers which form the inversion layer require a finite time to be generated. Figure 6.4 shows the charge collected, as a function of the time, between voltage pulses for three different MOS bias voltages. To extract information about the material properties from these curves, a model of the generation process is necessary.

6.2.1 Theory

In deriving this model, the existing literature on determining lifetime by MOS capacitors was used extensively. The most widely employed technique, the MOS capacitance-time (C-t) transient method, involving accumulation to inversion pulsing, was first proposed by Jund and Poirier[19] and by Grosvalet et al.[49] It was subsequently analyzed in greater detail by Zerbst[48] and by Heiman.[50] Recent publications[51,53,162,163,164] pertaining to the correct interpretation of the C-t transient were also studied. Other MOS capacitance techniques involving large signal inversion to accumulation pulsing[157,158] and a linear sweep technique[52,165] were also considered.

Following either Heiman[50] or Grosvalet et al[49], the total voltage, V_T, on the capacitor is

$$V_T = \frac{q\, W_{ox}}{K_{ox}\, \varepsilon_o} [N_A W + N_I] + \frac{qN_A W^2}{2K_s\, \varepsilon_o} \qquad 6.2.1$$

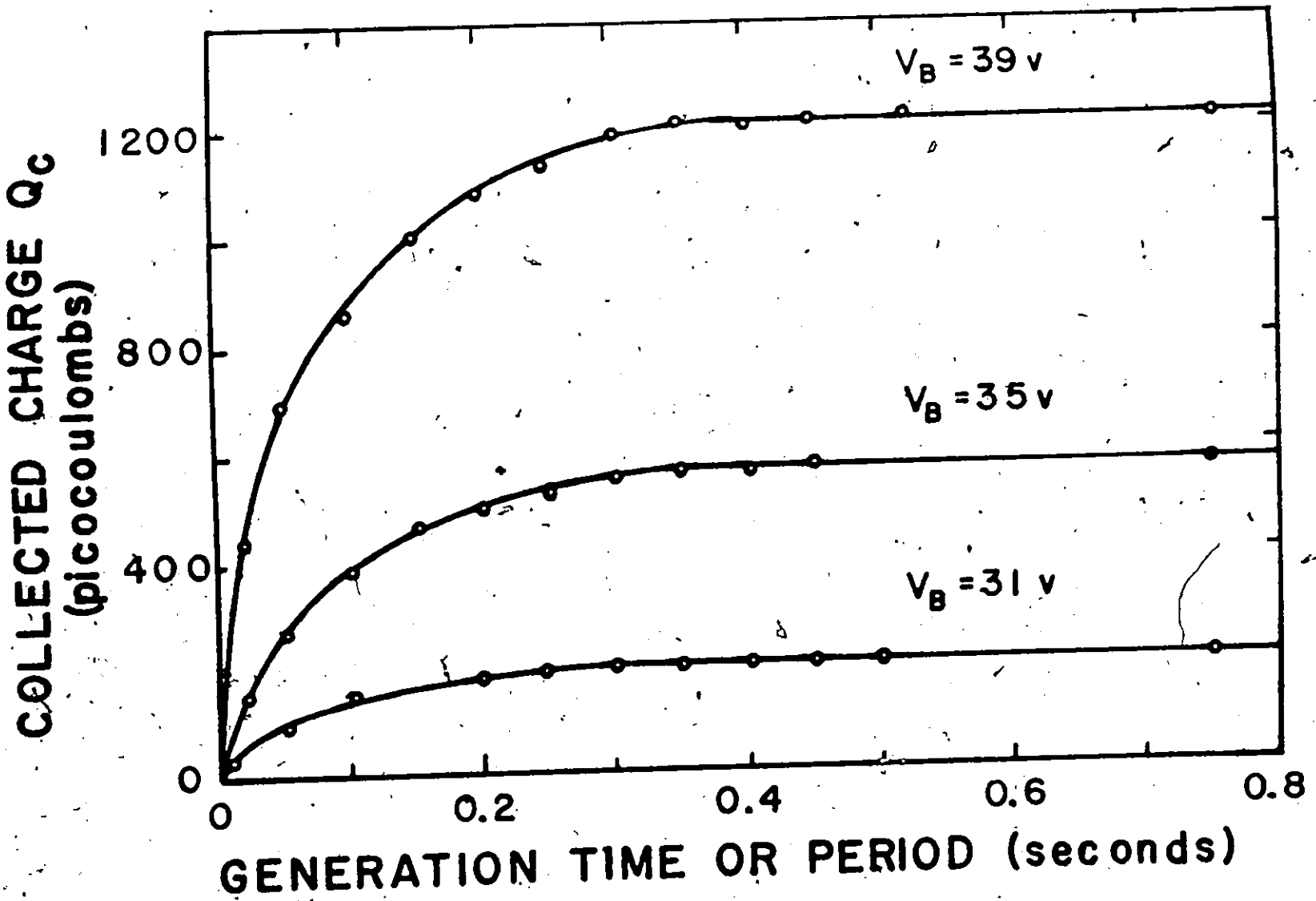


Figure 6.4 The inversion charge generation curves for three different values of MOS bias voltage

where W and W_{ox} are the width of the MOS depletion layer and the oxide respectively, K_{ox} and K_s are the relative dielectric constants of the oxide and the semiconductor, N_A is the acceptor impurity density and N_I is the number of charge carriers in the inversion layer. The transient response is

$$\frac{dV_T}{dt} = \frac{q\, W_{ox}}{K_{ox}\epsilon t_o}\left[N_A \frac{dW}{dt} + \frac{dN_I}{dt}\right] + \frac{q\, N_A\, W}{K_s\, \epsilon_o}\frac{dW}{dt} \qquad 6.2.2$$

After the voltage pulse is applied, $dV_T/dt = 0$, so

$$\frac{dN_I}{dt} = -N_A \frac{dW}{dt}\left[1 + \frac{K_{ox}}{K_s}\frac{W}{W_{ox}}\right] \qquad 6.2.3$$

also

$$\frac{dN_I}{dt} = -\sum_i G_i = G_1 + G_2 + G_3 + G_4 + G_5 \qquad 6.2.4$$

To proceed further, the different generation mechanisms represented by the G_i's must each be considered and finally an equation for the total generation in this device determined.

G_1 is generation in the depletion layer and obeys the relationship

$$G_1 = U(W - W_o) \qquad 6.2.5$$

Several different values of W_o are considered. Grosvalet et al[49] considered W_o to be zero while Heiman[50] lets W_o equal the equilibrium depletion layer width. Prince[162] uses a more complex formulation to arrive at a value intermediate to the others. The value due to Heiman[50] is used

in the following calculations. The generation rate, U, is of the Shockley-Read-Hall type[135] and Schroder and Nathanson[163] show that surface as well as bulk effects must be considered. This mechanism dominates for these devices.

G_2 is generation from the oxide-semiconductor surface directly under the metal field plate. Schroder and Guldberg[53] discuss this effect and show that

$$G_2 = S(N_I) \qquad 6.2.7$$

where $S(N_I)$ is a complex function of the inversion charge, N_I. This component of the total generation is small and is neglected in these calculations.

G_3 is bulk generation which satisfies the relationship

$$G_3 = K \qquad 6.2.8$$

where K is a constant. Schroder[164] discusses the properties of the constant including the effect of the back contact for thin layers. This component is not significant except at high temperatures or under external stimulation. Neither of these conditions are present in this project so G_3 is neglected.

G_4 is high field generation due to either tunneling or avalanche. These effects, studied by Goetzberger and Nicollian[166,167], require higher fields than are normally present in these devices so this component is neglected.

G_5 is generation from a surface which is depleted by ions in the oxide.[47,165] All prior test results indicate no ions were present, so this component is neglected.

Thus, the total generation for these devices is assumed to be in the non-equilibrium depletion layer, G_1. Subsituting Eq. 6.2.5 in Eq. 6.2.4 and setting the two equations for dN_I/dt (6.2.3 and 6.2.4) equal yields

$$U(W - W_o) = - N_A \frac{dW}{dt} \left[1 + \frac{K_{ox}}{K_s} \frac{W}{W_{ox}}\right] \qquad 6.2.9$$

Integrating Eq. 6.2.9 with $W^o = W'$ at $t = 0$ and $N_A/U = \tau_c$, the result is

$$- \frac{t}{\tau_c} = \left[1 + \frac{K_{ox}}{K_s} \frac{W_o}{W_{ox}}\right] \ln \left(\frac{W - W_o}{W' - W_o}\right) + \frac{K_{ox}}{K_s} \frac{W - W'}{W_{ox}} \qquad 6.2.10$$

if $W_{ox} >> W'$ (in this case, W_{ox} was determined in Section 3.3 to be 1475 Å and W' was calculated to be 300 Å) then Eq. 6.2.10 simplifies to

$$- \frac{t}{\tau_c} = \left[1 + \frac{K_{ox}}{K_s} \frac{W_o}{W_{ox}}\right] \ln \left(\frac{W - W_o}{W' - W_o}\right) \qquad 6.2.11$$

Now for the MOS capacitor the inversion charge, Q_I, is

$$Q_I(t) = q N_A(W' - W) \qquad 6.2.12$$

$$Q_I(\infty) = q N_A(W' - W_o)$$

substituting these relationships in Eq. 6.2.11 gives

$$- \frac{t}{\tau_c} = \left[1 + \frac{K_{ox}}{K_s} \frac{W_o}{W_{ox}}\right] \ln \left[\frac{Q_I(\infty) - Q_I(t)}{Q_I(\infty)}\right] \qquad 6.2.13$$

This expression relates the experimental quantity charge to the theoretical generation mechanism.

6.2.2 Experimental Results and Discussion

Figure 6.5 shows the charge term of Eq. 6.2.13 plotted to yield the generation time constant, τ_c. Table 6.1 gives the values of the generation time constant, τ_c, determined in this manner for the different devices at 25°C.

The derivation of the theoretical generation relationship assumes the process is independent of the bias voltage on the MOS capacitor, V_B. Figure 6.5 shows that τ_c is independent of V_B, indicating the theoretical assumption was valid. As well, the fact that τ_c was independent of V_B confirmed that neither tunneling or avalanche generation, G_4, were significant since each is field dependent, V_B/W_{ox}.

To study the generation mechanism in detail, a generation plot (Fig. 6.6) was determined at 22°C with the time between experimental points greatly reduced. It can be seen from Fig. 6.6 that the experimental results obey Eq. 6.2.13 after the first 50 ms. In this initial period the generation is more rapid than predicted by Eq. 6.2.13.

The derivation of the theoretical generation mechanism assumes no external source of electrons, particularly no injection from the reverse biased diode. This was confirmed when the experimental generation time constant, τ_c, was found to be independent of the bias voltage across the p-n junction diode, V_c.

The theoretical generation mechanism was assumed to be independent of the voltage pulse, V_p, applied to the MOS capacitor. The generation rate was determined as a function of the amplitude of V_p and the results

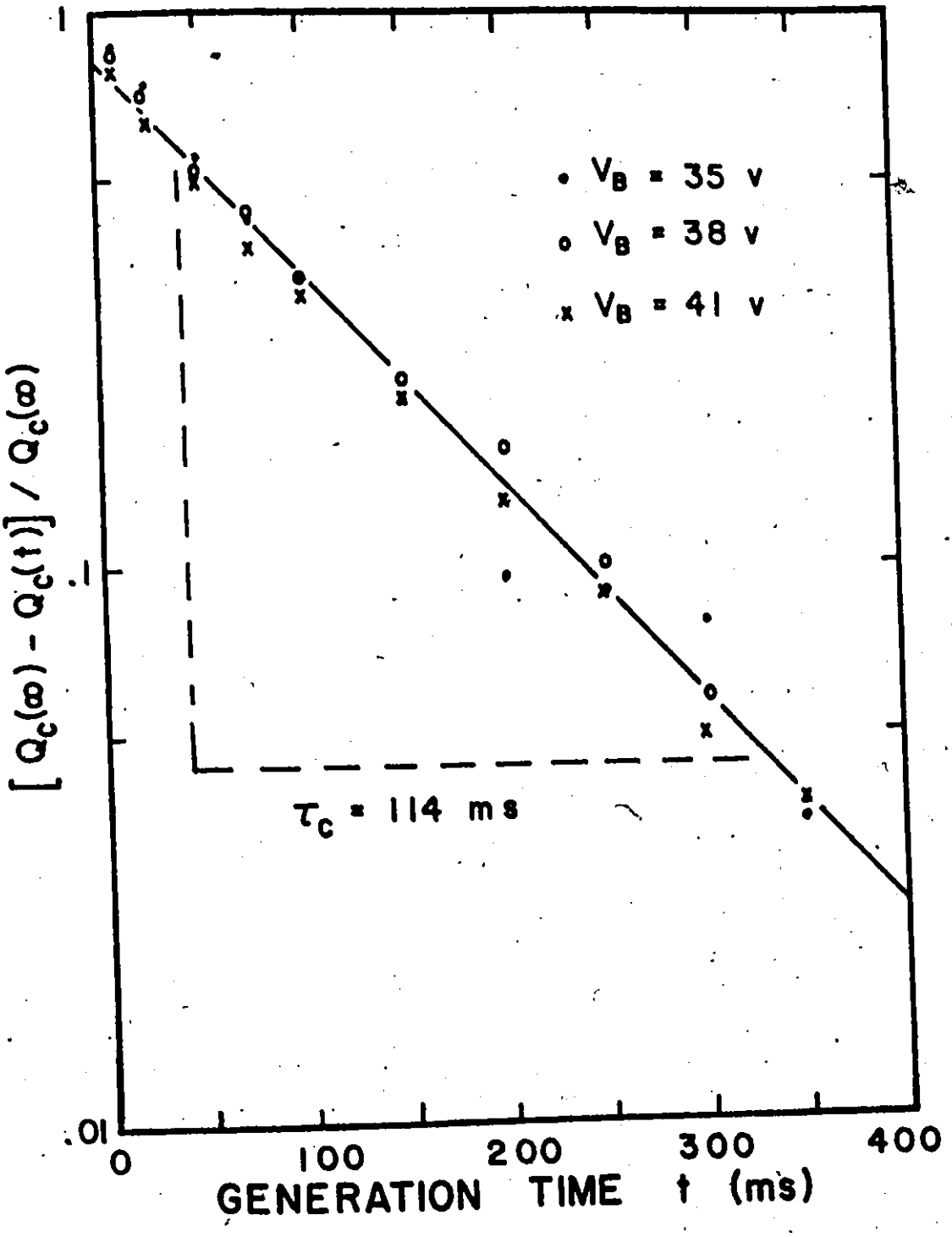


Figure 6.5 The inversion charge generation time for three different values of MOS bias voltage

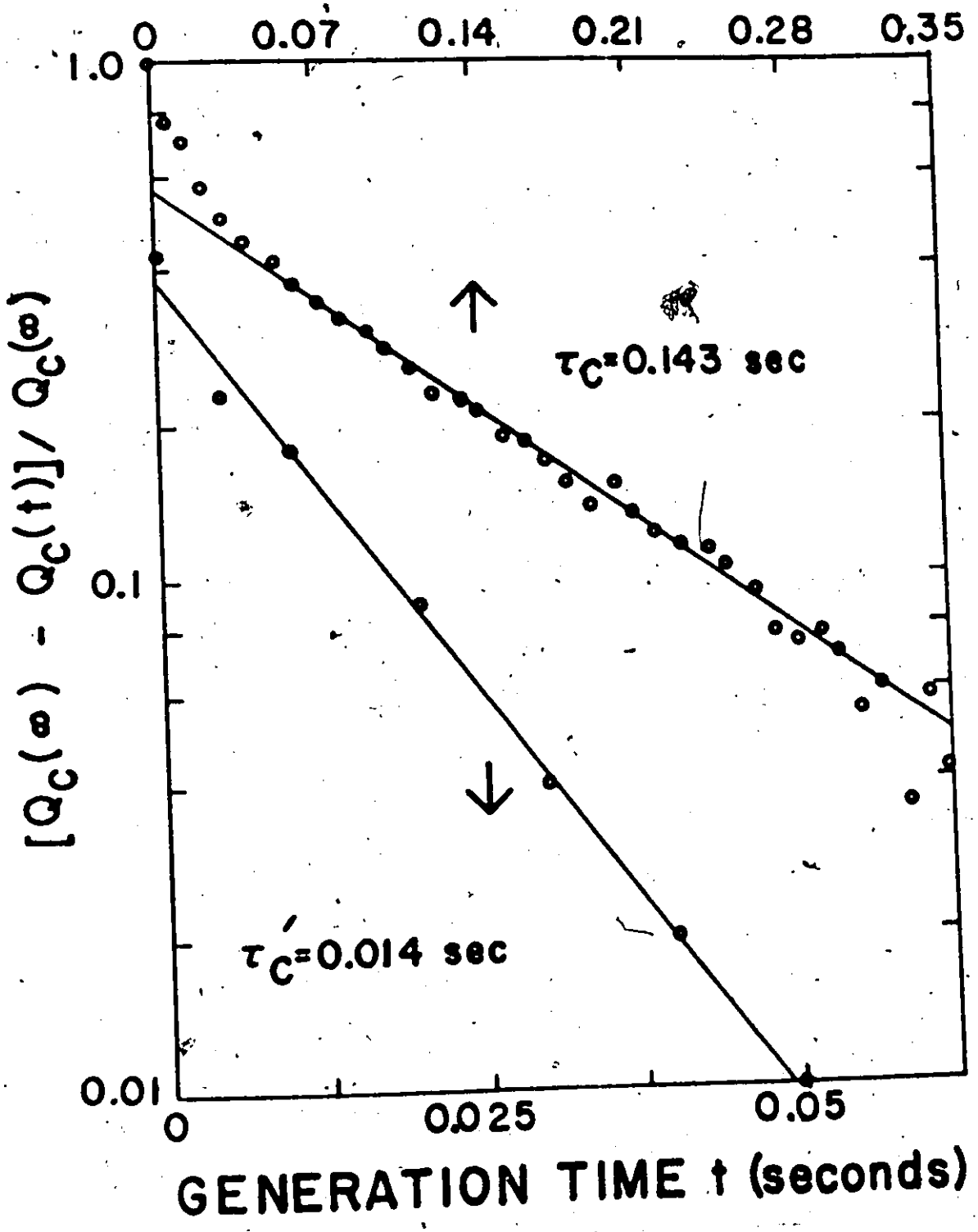


Figure 6.6 The inversion charge generation time at 22°C

are plotted in Fig. 6.7. The generation time constant, τ_c, is essentially constant (133 to 137 ms in Fig. 6.7) throughout the range of voltage pulse amplitudes. The voltage pulse is not only defined by its amplitude but also its risetime. Over the limited range of risetimes for V_p (11.5 - 13.5 ns) studied, τ_c was a constant. The experimental results confirm that the basic generation mechanism was independent of the voltage pulse applied to the emitter of the MOSCET.

As proposed by Grosvalet et al[49] the activation energy of the generation process can be determined from the temperature dependence of τ_c. Figure 6.8 shows the relationship between the normalized generation time and the reciprocal temperature from which the activation energy of 0.36 eV was determined. Table 6.1 includes the activation energy of the generation process for each device. The generation centre once more appears to be gold since the experimental energy level of 0.36 ± 0.04 eV was in excellent agreement with the gold level of 0.36 ± 0.001 eV[168] in p-type silicon.

Generation in the depletion layer of the MOS capacitor was assumed to be of the Shockley-Read-Hall type.[135] So, using the first approximation to this generation mechanism

$$U = n_i/2\tau \qquad 6.2.13$$

and knowing $\tau_c = N_A/U$, the generation lifetime, τ, was determined to be 4×10^{-10} s. From this lifetime, the gold concentration was determined to be 3×10^{16} atoms/cm^3.[147]

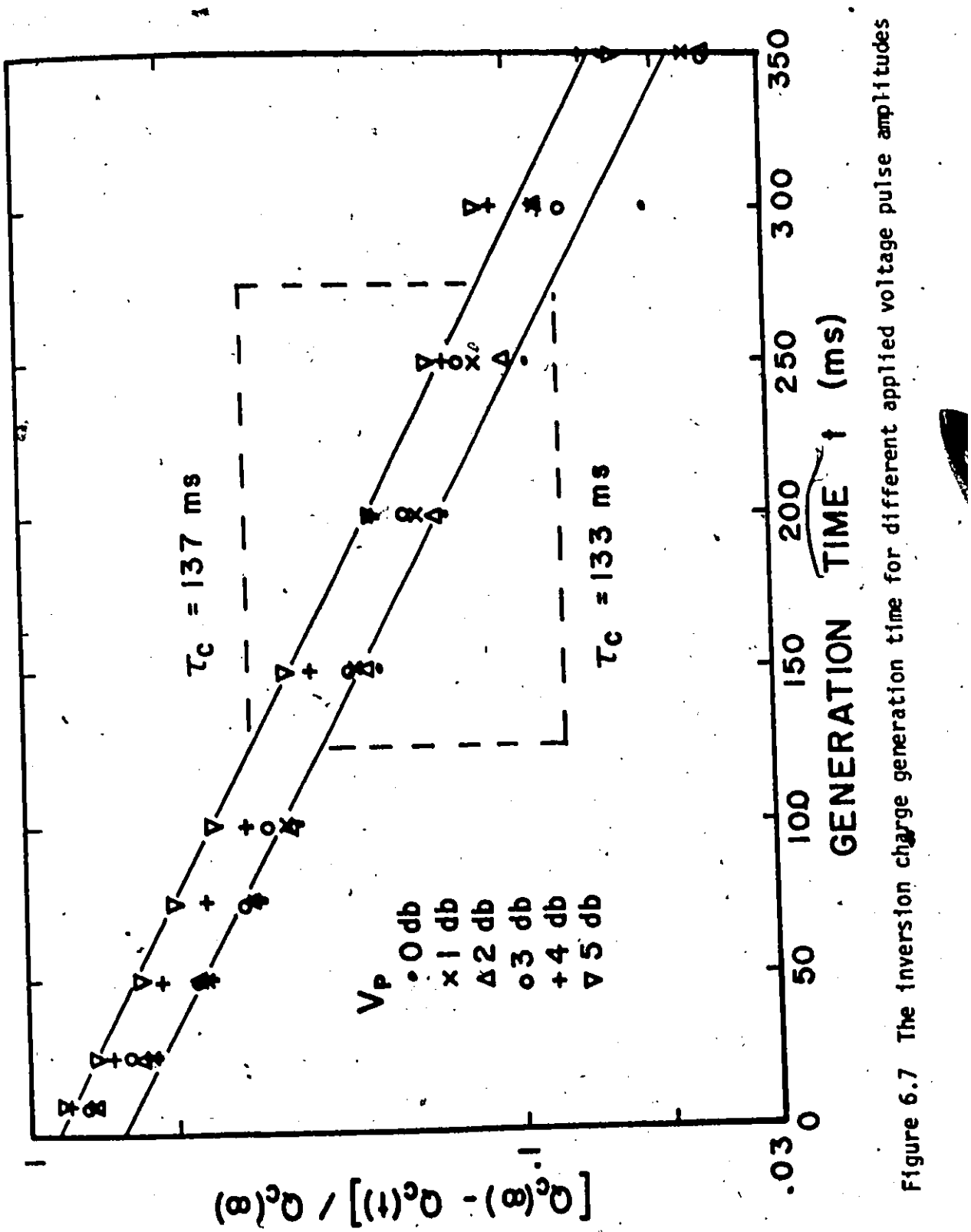


Figure 6.7 The inversion charge generation time for different applied voltage pulse amplitudes

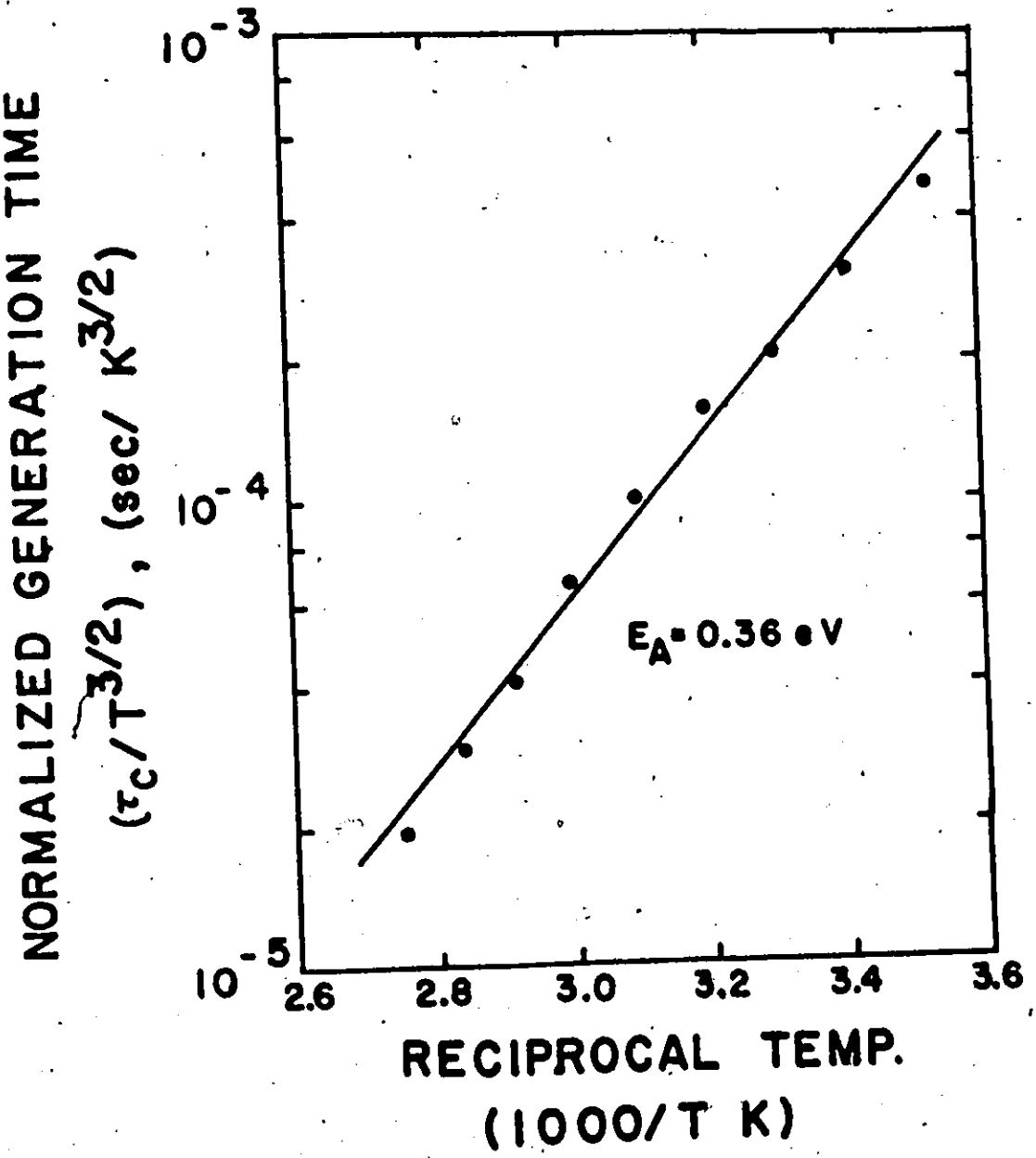


Figure 6.8 The variation of the generation time constant with temperature

The reason for the rapid generation in the first 50 ms of Fig. 6.6 is now considered. The difference between the experimental results and the theoretical relationship in the initial region is also plotted in Fig. 6.6. These results likewise satisfy an exponential relationship with a different time constant τ_c'. As the voltage pulse amplitude decreased, so did the initial rapid component. It can be seen in Fig. 6.7 that, when the pulse amplitude decreased 5 db, the rapid component was reduced to about 1/3 of its initial value. When the temperature was varied, the ratio of the time constant for the rapid component and the normal component, $\tau_c' : \tau_c$, remained a constant indicating the same activation energy for each process.

To account for this rapid component, generation from the surface under the capacitor field plate, G_2, was investigated. However, the strong dependence on the inversion charge, N_I, predicted by Eq. 6.2.7, was not observed (see Fig. 6.5, where N_I is proportional to V_B). Another possible source of this component was electrons released from surface states. Since the surface states are distributed in energy, no single activation energy is possible. This is contrary to the experimental results which show a distinct activation energy.

Two devices are listed in Table 6.1 which show no generation time constants and activation energies. The generation rate for these devices was 1 to 2 orders of magnitude faster than the other devices. This generation was a simple exponential function of time. The generation time constant, τ_c, was a strong function of the bias voltage on the MOS capacitor, V_B, and τ_c was independent of temperature. These results indicate the generation

mechanism was tunneling through defects in the oxide.

6.2.3 Conclusions

The dominant generation mechanism for these devices was Shockley-Read-Hall type centres[135] in the depletion layer of the MOS capacitor. The generation lifetime was determined to be 4×10^{-10} s and the energy level of the generation centre was 0.36 ± 0.04 eV. From these values, it was concluded that the generation centre was gold which was present to the limit of its solubility at the final processing temperature (3×10^{16} atoms/cm^3).[96]

No theoretical generation mechanism was found which would account for the initial rapid generation component.

6.3 The Inversion Charge

The inversion charge, Q_I, which cannot be measured directly, is determined from the measured collected charge, Q_C, by assuming the two are proportional with the difference between the released and collected charge, being due to recombination during transport. However, in studying the inversion charge, changes in the parameters may affect the transport conditions. Then the fraction recombined is changed altering the proportionality between Q_I and Q_C. These transport effects are considered in the next section.

6.3.1 Experimental Results and Discussion

The MOS capacitor computer program[18] was used to calculate the theoretical inversion charge, Q_I, as a function of the bias voltage across the MOS capacitor, V_B. Shown in Fig. 6.9 is a theoretical Q-V curve which begins just below the inversion potential and becomes linear with a slope of C_{ox} for values of bias much greater than the inversion potential. The intercept of this straight line with the voltage axis is the inversion potential. For an ideal voltage pulse, one always sufficient to move the device out of inversion, the curve continues linear until breakdown. However, for smaller voltage pulses, the curve saturates at a constant value, Q_{IS}, because the pulse amplitude is only sufficient to move the bias from one point in inversion to another. Also shown in Fig. 6.9, are a pair of experimental Q-V curves which clearly show the linear relationship ($V_p' = -17\ \Psi$) and the saturated curve ($V_p' = -10$ V) and thus confirm the theory.

The short curve at 35 V in Fig. 6.9 shows the actual position of the theoretical curve but it was shifted laterally in voltage to have the same inversion potential as the experimental results. This difference between ideal and experimental inversion potential is the voltage shift, ΔV, due to work function difference, ϕ_{MS}', and fixed oxide charge, Q_{SS}. Providing ϕ_{MS}' is known, a value of Q_{SS} can be determined using the relationship given by Grove et al[12]

$$\Delta V = -\phi_{MS}' + Q_{SS}/C_{ox} \qquad 6.3.1$$

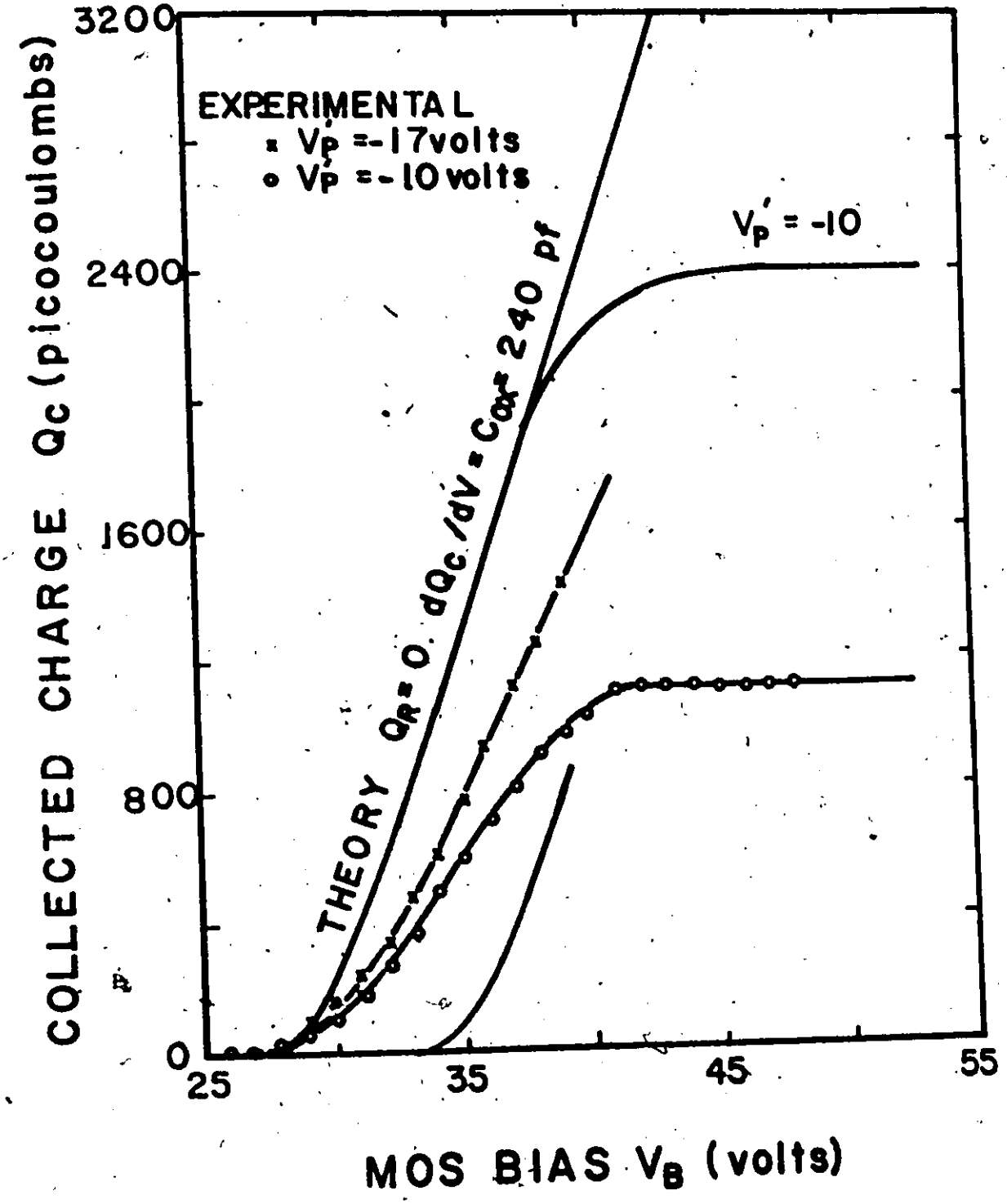


Figure 6.9 The effect of MOS bias voltage on the collected charge

Table 6.1 shows the experimental value of inversion potential for each device and the fixed oxide charge calculated using ϕ_{MS} of - 1.1 eV[21] and the average value of 235 pf for the oxide capacitance, C_{ox}.

Since the inversion charge is a direct function of the surface potential, measurements of Q_c can be used to monitor the stability of the insulator and its interface with the semiconductor. In the linear portion of the C-V curve any change in charge collected is proportional to the change in surface potential.

These devices were subjected to biases of ±40 V at 90°C for one hour and all demonstrated Q-V shifts corresponding to less than 1.5×10^{10} charge carriers/cm^2.

The fraction of the inversion charge which is collected can be determined if the effective capacitance of the device is known, since the ratio of the effective capacitance to the oxide capacitance, $C:C_{ox}$, is the same as the ratio of the collected charge to the inversion charge, $Q_c:Q_I$. The effective capacitance, C, is the slope of the experimental Q-V curve. Table 6.1 lists the slope for each device and the results are very consistent with a standard deviation, σ, of 2.4%. This deviation could be due to variations in recombination rate or the amount of charge released. If it were due to the charge released, the deviation of C_{ox} and C should be proportional. This was not observed, so the deviation must be primarily due to changes in the recombination rate.

A second method to calculate the effective capacitance involves the amount of charge collected when the Q-V curve saturates for small pulse amplitudes. Knowing the amplitude of the voltage pulse across the

MOS capacitor, V_p', the value of C_o can be calculated from Q_{IS} using the following relationship

$$C = Q_{IS}/V_p' \qquad 6.3.2$$

For the curve $V_p' = -10$ V of Fig. 6.9, the value of C derived from the slope method is 95 pf, while from Eq. 6.3.2, it is 96 pf. The excellent agreement between the two experimental values confirms that the methods are equivalent.

Since the inversion charge released is proportional to the amplitude of the voltage pulse applied, the saturated charge, Q_{IS}, released by a small amplitude pulse, should be proportional to the pulse amplitude. Figure 6.10 shows Q-V curves for different amplitudes of V_p. Ignoring small second order effects, due to transport properties changing, Q_{IS} is proportional to V_p as predicted by theory.

The inversion charge has a very weak temperature dependence, chiefly due to the variation of the energy gap. The temperature dependence of the collected charge is dominated by transport effects and will be considered in the appropriate section.

Theory predicts that the voltage applied to the reverse biased p-n junction diode, V_c, has no effect on the inversion charge. Figure 6.11 (which only shows the top 5% of Q_c) clearly reveals the collected charge, Q_c, is independent of V_c over an extended range, except for a small effect due to transport, confirming the theoretical prediction. However, for extremes in V_c, the linear relationship between Q_I and Q_c is no longer true due to the following effects.

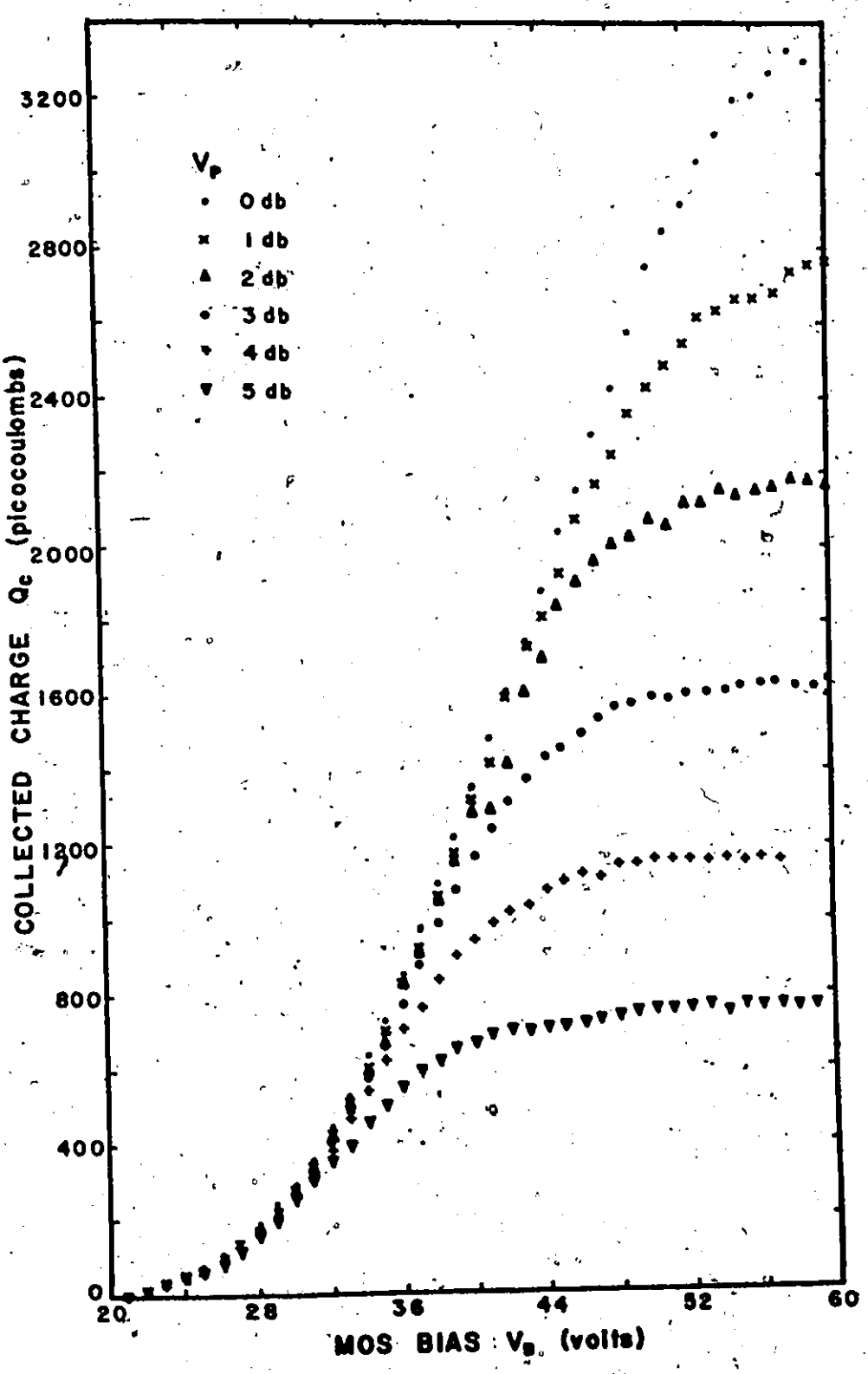


Figure 6.10 The collected charge versus MOS bias voltage for different applied voltage pulse amplitudes

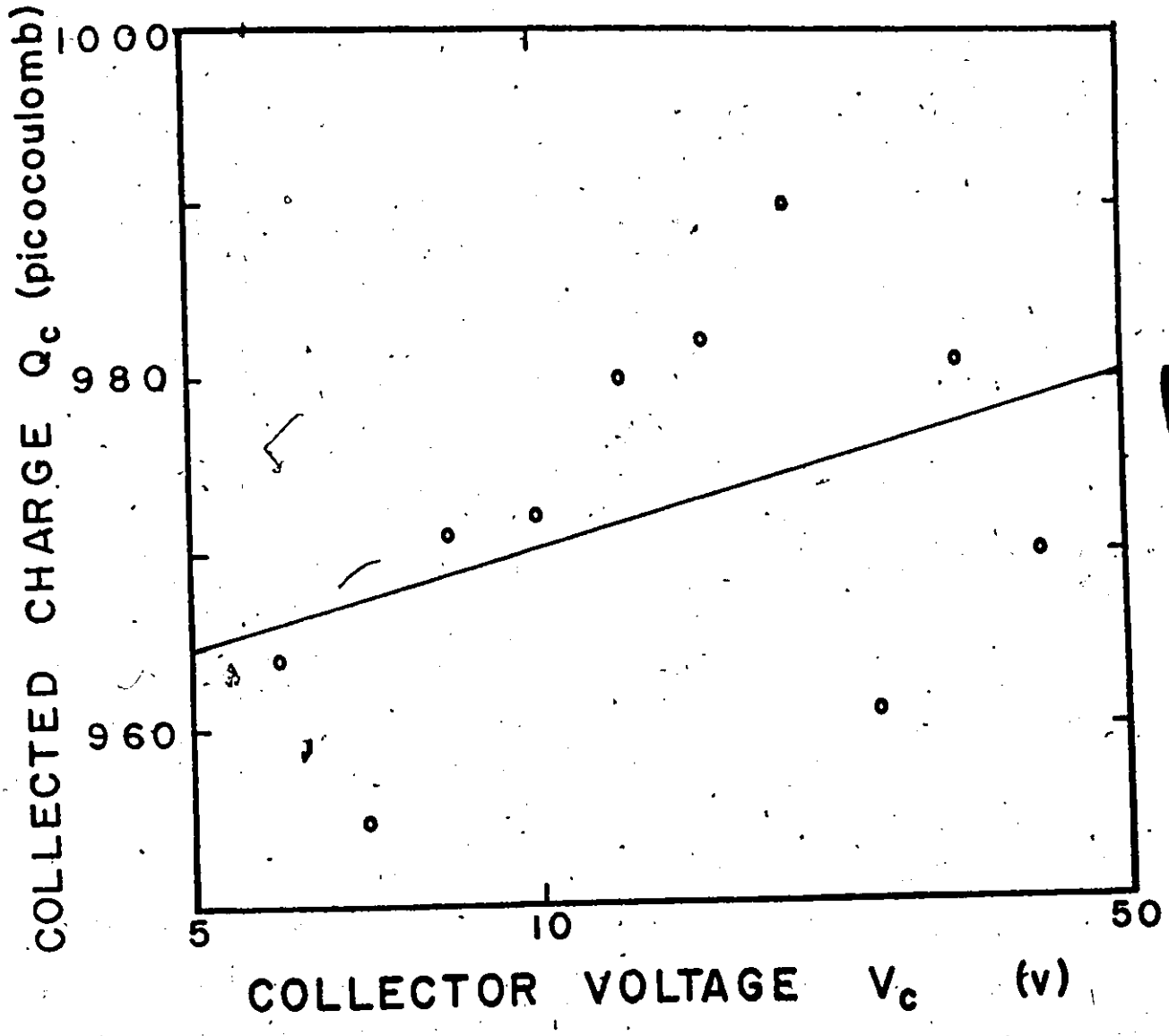


Figure 6.11 The collected charge at various reverse biased diode voltages

As described in the collector circuit response of Section 5.3.4, the inversion charge from the current source divides so the voltage around each loop is the same (see Fig. 5.8). The voltage due to the inversion charge flowing in the collector circuit reduces the total voltage across the p-n junction. When V_c is small, the voltage due to the inversion charge is sufficient to forward bias the diode. When this occurs, the collector efficiency decreases drastically and the total collected charge is reduced. The experimental results confirm that this occurs.

For large reverse biases on the diode, avalanche multiplication[169] occurs and the collected charge increases. Figure 6.12 shows the multiplication factor as a function of V_c.

Previous study of the Q-V curves concentrated on the region where V_B is greater than the inversion potential. Now the initial region will be considered. It can be seen in Fig. 6.9 that the shape of the theoretical and experimental curves differ. The theoretical curve was calculated for the case of an ideal MOS capacitor and the observed shape can be accounted for by either of two non-ideal effects, surface states or fluctuations in surface potential.

The theoretical Q-V curve for the surface state distribution of Goetzberger et al[28] was calculated.[18] The resulting Q-V curve was closer to the experimental shape. A much larger density of surface states, than was observed in the MOS capacitance results (Section 3.2.5.2) is required to account for the observed curve.

The effect of fluctuations in surface potential has been considered by several authors.[23,24,25] The most common cause of this effect

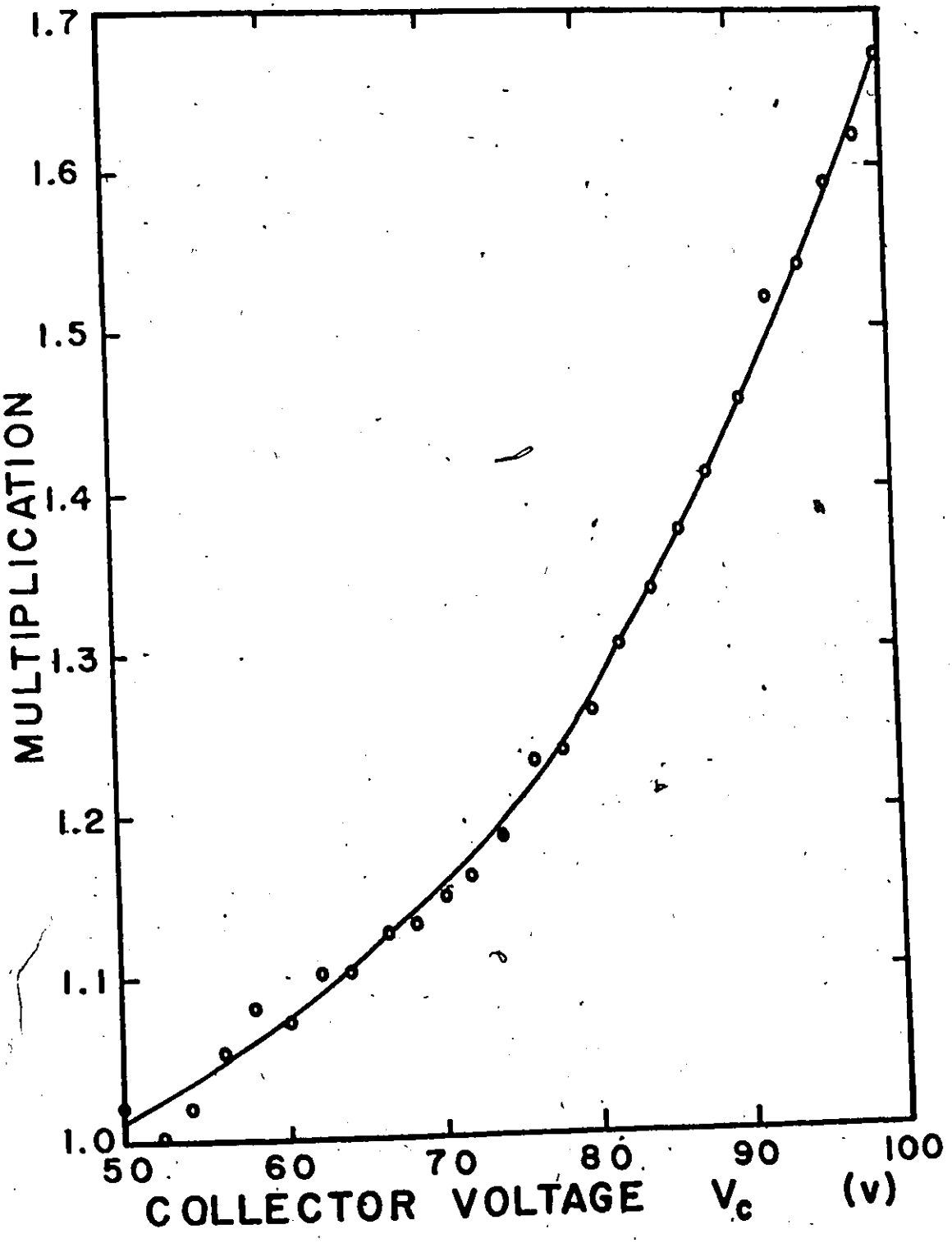


Figure 6.12 The multiplication factor as a function of the reverse biased diode voltage

is local variations in the fixed oxide charge, Q_{SS}. Large fluctuations in Q_{SS} were observed from device to device (see Table 6.1). This suggests that the same effects could occur in areas of an individual device and account for the observed results.

6.3.2 Conclusions

The experimental Q-V curves are a direct confirmation of the theoretical relationship between inversion charge and bias voltage for an MOS capacitor. The experimental results also confirm the theoretical predictions of the effects of varying the external parameters.

From measurements of the collected charge, the inversion potential (30.6 ± 2.6 V), the fixed oxide charge density ($6.02 \pm 3.8 \times 10^{11}$ states/cm^2) and the insulator stability (less than 1.5×10^{10} charge carriers/cm^2) were determined.

The experimental results show that surface states and fluctuations in surface potential were present. However, from the limited data available, these effects cannot be separated.

The MOSCET offers unique opportunities to study the onset of avalanche multiplication in the p-n junction diode since the value of the injected charge can be determined so accurately.

The MOSCET provides definite advantages in testing the insulator stability. To achieve the equivalent resolution by conventional C-V measurements, requires a measuring accuracy of 0.02%.

6.4 Transport

In this section the computer programs derived from transport theory in Chapter 5 were used to predict the inversion pulse position and shape as the experimental parameters were varied. The theoretical results were then compared with the observed experimental curves to check the transport analysis and determine the material properties.

The fact that the current detection system was not ideal, introduces additional effects which must be considered in the transport analysis. An ideal detector, capable of counting every individual electron, would allow the changes in charge collected to be directly related to the amount recombined. However, the noise level of 1mv for the sampling scope, meant that current levels below 0.2 ma could not be detected. Consequently, the charge detected was a function of the pulse shape. Although the total charge in each case was the same, more charge would be detected for sharp high amplitude pulses than lower amplitude pulses with longer tails.

6.4.1 Experimental Results and Discussions

Theory predicts that the bias voltage on the MOS capacitor, V_B, merely controls the amount of inversion charge present without changing the basic shape and position of the pulse. The experimental results were consistent with theory.

Theoretically, the bias voltage on the p-n junction diode, V_C, could affect the shape of the inversion charge pulse in three different ways.

(1) The non-inversion response is a very strong function of the capacitance of the reverse biased diode, C_{P-N}, (Fig. 6.2) which in turn is controlled by V_c (Fig. 3.8). Consequently, the voltage pulse, V_p', across the MOS capacitor, calculated during the non-inversion response, is also a function of V_c. Since V_p' controls the shape and position of the inversion charge pulse, this is also a function of V_c. However, a series of calculations were made, varying C_{P-N}, and the change in V_p' was so small this effect could be neglected.

(2) It was shown in Section 5.3.2 that the voltage across the diode, V_c, controls the depletion layer width and consequently the distance over which transport occurs. However, the change in distance travelled is small (0.2 μm or less in 3 μm total) and from Table 5.1, only about 1% of the total transit time is spent crossing this region. For this reason, this effect was also neglected.

(3) The voltage dependent current source used to represent the inversion response in the device model is placed in parallel with C_{P-N} (see Fig. 5.7). When C_{P-N} is increased (V_c decreased), the percentage of the released charge going to charge the capacitor, rather than through the collector circuit, is altered. This results in an inversion charge pulse with a lower peak, occurring later in time, and with a much longer tail. This is exactly what was observed experimentally. The slight decrease in the collected charge, Q_c, in Fig. 6.11, as V_c was decreased, was due to some charge in the longer tails of the pulses not being detected.

The voltage pulse, V_p, applied to the MOS capacitor, determines the shape and position of the inversion charge response. The actual control

of the inversion charge is exercised by the voltage pulse across the MOS capacitor, V_p', which is calculated during the non-inversion response from V_p. Theory predicts that, until the barrier in the release mechanism is lowered a set value, no inversion charge is observed. The experimental results confirm that for V_p less than 20 V, no inversion charge was detected. Knowing how much the barrier must be lowered before inversion charge was detected, the starting time of the inversion charge pulse was predicted for V_p' scaled down in 1 db steps (0 - 5 db). Experimental results over the same range confirm that the minimum barrier lowering before charge could be detected is almost constant. Theoretically, the more V_p' exceeds the value necessary for inversion charge to be detected, the sharper and higher the inversion pulse. Similarly, the faster V_p' increased after this minimum barrier lowering, the sharper and higher the inversion charge pulse. The observed experimental results confirm the theoretical variations in the inversion charge pulse shape.

The theoretical inversion response has three potential sources of temperature dependence.

(1) The components of the device model and the pulse circuit are temperature dependent. Consequently, V_p' calculated during the non-inversion response is temperature dependent. However, Fig. 6.1 indicates the temperature dependence of the non-inversion response was only 0.05% per °C, so this effect was not significant.

(2) The physical parameters of the transport equation are both temperature dependent

$$D_n = (kT/q)\,\mu_n \qquad 6.4.1$$

$$\mu_n E = \frac{\mu_n}{N(x)} \frac{kT}{q} \frac{dN(x)}{dx} \qquad 6.4.2$$

For this particular doping density, the electron mobility, μ_n, is essentially independent of temperature[96] and so is the impurity profile, N(x). Therefore, both D_n and $\mu_n E$ have the same linear temperature dependence. This means that as the temperature increases, the collected charge pulses should have the same shape but occur earlier. However, this would not account for the observed results.

(3) The release mechanism at the interface is strongly temperature dependent. The model being used is a barrier which is lowered by applying voltage until the electrons have sufficient thermal energy to cross it. Increasing the temperature increases the thermal energy, thus decreasing the amount of voltage which must be applied before the inversion charge is detected. Since the pulse position is controlled by the time the voltage pulse takes to overcome the barrier, with increased temperature less voltage is required to accomplish this, more voltage is available to hold the barrier open so a sharper, higher pulse results. The observed experimental results confirm the fact that the inversion charge pulse appears earlier and is much higher as the temperature is increased. Figure 6.13 shows the charge collected as a function of the temperature with a constant amount of inversion charge released.

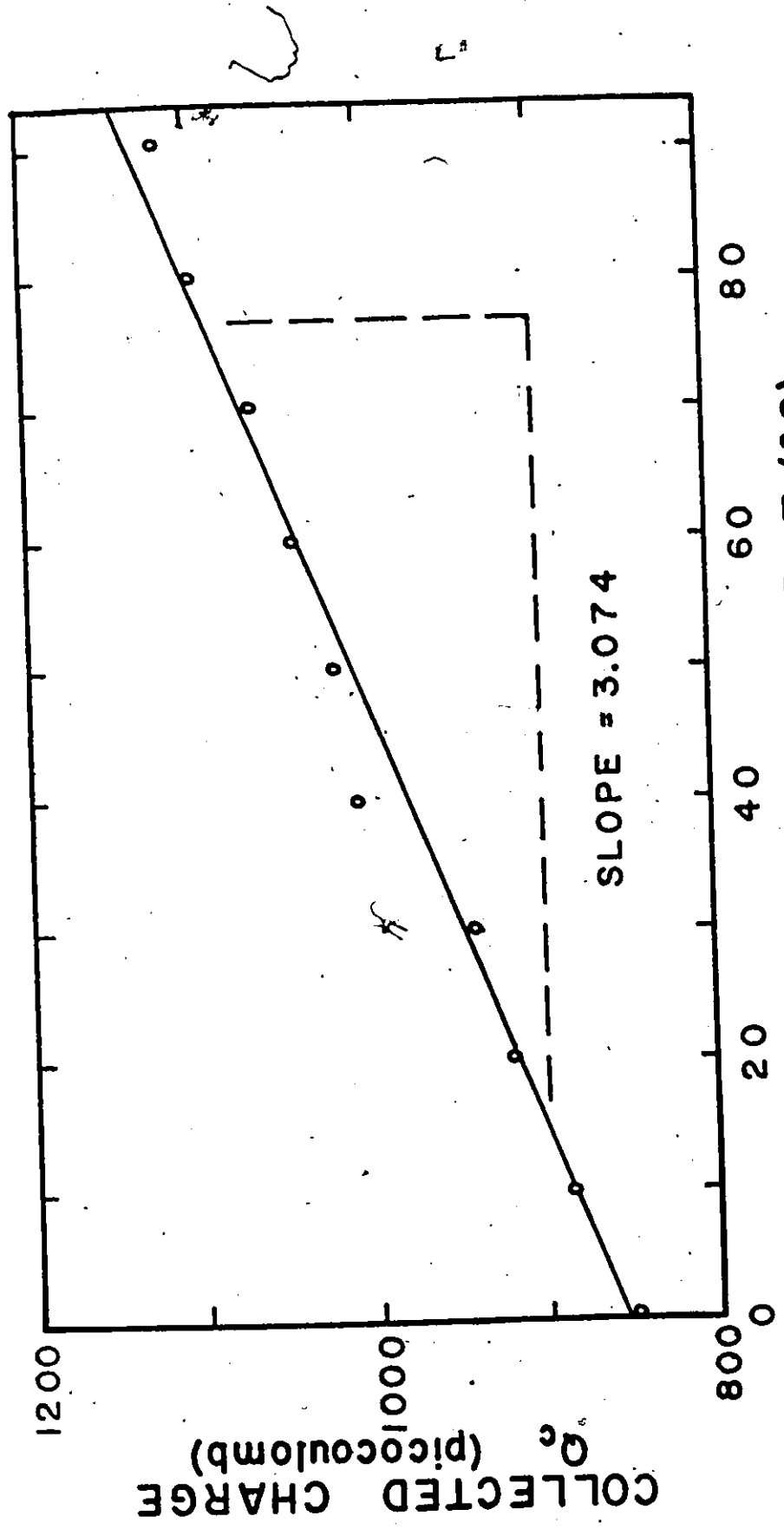


Figure 6.13 The variation of the collected charge with temperature

6.4.2 Conclusions

The experimental results confirm that the bias voltage across the MOS capacitor, V_B, merely scaled the inversion charge pulse while the applied voltage pulse across the MOS capacitor, V_p', through the release mechanism, controlled the pulse shape and position. The charging and discharging of the diode capacitor in the collector circuit dominated the observed response when the bias voltage across the diode, V_c, was varied. The observed temperature dependence of the collected charge pulse was due to the temperature dependence of the release mechanism.

6.5 Conclusions

Theoretical curves, based on the analysis in Chapter 5, fitted well with experimental results and by comparison of the theoretical and experimental curves, a number of material properties were determined.

Measurement on shallow heavily doped layers using the MOSCET yield.

(1) The minority carrier generation lifetime near the interface.

(2) The generation centre energy level.

(3) The average minority carrier recombination lifetime in the layer.

(4) The transport properties across the layer.

(5) The inversion potential.

(6) The fixed oxide charge density.

(7) The insulator stability.

The measured properties of the MOSCET were consistent from device to device (Table 6.1). The non-inversion charge, Q_{N-I}, the inversion potential, the Q-V slope (or effective capacitance) and the activation energy of the generation process all have standard deviations, σ, of less than 6.5%. The larger deviations in the generation time constant, τ_c, and the fixed oxide charge density, Q_{SS}, were anticipated since each was strongly dependent on processing and relatively large fluctuations from device to device, even from the same wafer, are normal occurrances.

In the heavily doped layer near the semiconductor-oxide interface, the average generation time constant was 114.4 ms and the activation energy of this process was 0.36 eV. A lifetime of 4×10^{-10} s was calculated from the time constant. The activation energy revealed the generation centre was gold. From the lifetime, the gold concentration was determined to be 3×10^{16} atoms/cm^3 which agreed with the solid solubility of gold at the final processing temperature. The charge collected was approximately 58% of the inversion charge released and the average recombination lifetime across the entire heavily doped layer was 17 ns.

The properties of the oxide-semiconductor interface were determined using the MOSCET. The average inversion potential was 30.6 V and the fixed oxide charge density was $6.0 \pm 3.8 \times 10^{11}$ states/cm^2. The effect of fast surface states and fluctuations in the surface potential were observed but the two effects could not be separated. The insulator stability was tested at ±40 V at 90°C for one hour and less than 1.5×10^{10} charge carriers/cm^2 were detected.

The MOSCET can be used to study the avalanche properties of p-n junction diodes as well as to characterize the thin heavily doped layer. Since the number of injected carriers is so well known, the MOSCET offers unique opportunities to study avalanche at low multiplication values.

CHAPTER 7

CONCLUSIONS AND RECOMMENDATIONS

The object of this project was the characterization of thin heavily doped layers in silicon. To accomplish this, it was necessary to determine the properties of the substrate and thermal oxide, which border the heavily doped layer, and their interfaces with it. A complete characterization of the layer was achieved using a combination of conventional and new techniques developed for this project. A 200 Ω/□ , 3 μm junction depth boron diffusion was considered a typical thin heavily doped layer and was studied in detail.

Conventional techniques completely characterized the dielectric, the substrate, and the substrate-diffused layer interface as well as providing some of the properties of the oxide-semiconductor interface and the heavily doped layer. However, to determine other properties of the heavily doped layer, it was necessary to improve on existing techniques.

The impurity profile was determined by differential sheet resistivity measurements using anodic oxidation and etching of the oxide as the sectioning technique and a four-point probe for determining the resistivity. Detailed study of the parameters affecting the anodization process was undertaken to provide a suitably uniform and reproducible sectioning technique. The resulting impurity profile was gaussian with a dip near the surface due to diffusion through the oxide and was in excellent agreement with theory. If mobility were of interest, it also could be determined by

substituting the Hall effect for the four-point probe.

From the experimental MOS C-V curves, the type of dopant and its concentration at the surface were determined. The impurity band structure was calculated from experimental low temperature C-V curves using a theoretical expression for temperature-dependent impurity band broadening developed in this project.

To complete the characterization of the heavily doped layer and its interface with the oxide, an experimental procedure utilizing a new test structure was introduced. The test structure consisted of an MOS capacitor formed over the thin heavily doped layer to be characterized which, in turn, formed one side of a p-n junction diode. The resulting structure was a MOS capacitor-emitter transistor (MOSCET). A theoretical model of the MOSCET was developed which allowed the following material properties to be determined from the experimental MOSCET response.

(1) The minority carrier generation lifetime near the interface.

(2) The generation-centre energy level.

(3) The average minority carrier recombination lifetime in the layer.

(4) The transport properties across the layer.

(5) The inversion potential.

(6) The fixed oxide charge density.

(7) The insulator stability.

Measurements on the MOSCET enabled some significant properties of thin heavily doped layers to be determined for the first time. While the interface properties could be derived from MOS C-V measurements, the MOSCET offered considerable advantages. For example, in monitoring

insulator stability, to achieve the same resolution by C-V would require two orders of magnitude better accuracy in the measuring equipment.

Combining the MOSCET results with those determined by conventional techniques completed the characterization of the thin heavily doped layer.

The recombination-generation centres observed throughout the test structure appeared to be gold. Since gold was not intentionally added, this must be a contaminent introduced during processing. Present practices are based on the n^+ layer acting as a getter, reducing the gold concentration throughout the structure. Although this was true in the substrate (2×10^{13} atoms/cm^3), the p^+ diffused layer retained the gold and, at the surface, the gold concentration was equal to the limit of solid solubility at the final processing temperature (2×10^{16} atoms/cm^3). To reduce the contamination, a different processing step should be considered. Current publications[170,171,172] report HCl cleaning increases the lifetime by removing recombination-generation centres as well as reducing the fixed oxide charge.

While this work has dealt with one particular thin heavily doped layer, the MOSCET technique can be applied to other layers, semiconductors and dielectrics providing the following conditions are satisfied.

(1) The dielectric must be able to withstand sufficient field to invert the semiconductor without breaking down. The field in the dielectric at inversion can be easily calculated using the depletion approximation (see Grove[6]). For silicon with a thermal oxide, the maximum concentration for which the MOSCET can be used is 1.5×10^{19} atoms/cm^3.

(2) The insulator thickness must be such that inversion can be achieved with practical voltages.

(3) The leakage through the insulator of the MOS capacitor must be so small that less than 0.1% of the inversion charge leaks away during the generation time.

(4) The width of the heavily doped layer must be such that a significant amount of the inversion charge can cross it before recombining.

(5) The heavily doped layer must be sufficiently wide that, even under transient conditions, some neutral bulk remains between the depletion layers of the diode and the MOS capacitor.

The observed transient response has a short duration (less than 100 ns) and a long time between pulses (approximately 1 s). This combination is difficult to achieve with current instrumentation. The probable trends in MOSCET measurements will result in increasing difficulties. Faster applied voltage pulses with risetimes of 0.5 ns or less would simplify the analysis since the non-inversion response would be completed before the inversion pulse arrived. This would reduce the duration of the transient to 10-20 ns. If better processing techniques were introduced, the period between pulses would increase because the time necessary to reach equilibrium is inversely proportional to the number of generation centres present.

The MOSCET offers unique opportunities in the study of avalanche multiplication in p-n junction diodes. With the very well defined amount of injected charge, the beginning of avalanche can be studied. However, the theoretical treatment necessary to determine the avalanche properties is very complex because the charge flowing in the collector circuit has the

effect of reducing the total voltage across the diode. Consequently, a negative feedback loop exists and the effective voltage to multiplication relationship must be determined theoretically. This analysis was not attempted and further study of this effect was left to future investigators.

While the MOSCET was a very useful tool in determining the exact properties of a thin heavily doped layer, its greatest value may be in the area of process control. Simple inspection of the raw MOSCET data would indicate any change in properties without detailed calculations. This would allow accidental changes in processing parameters to be detected quickly.

APPENDIX A

IMPROVEMENTS IN THE EQUIPMENT

If the MOSCET is to be used in further tests, an improvement in the device structure would be a better contact pad for the field plate of the MOS capacitor. This would greatly reduce the high percentage of devices which had the dielectric damaged during bonding.

If the MOSCET measurements are to be used in process monitoring several changes would be advantageous. The use of probe contacts, so the device can be tested while still part of the wafer, will allow the rapid detection of processing problems. The second would be in the measurement of the collected charge. An A-D converter synchronized with the sampling rate could be placed on the current output of the scope. The resulting digitized data could be fed directly to a computer and yield the collected charge almost instantaneously.

The new HP 184B Storage Oscilloscope with rapid write variable persistence offers a new means of determining the collected charge. This instrument would allow single shot measurements reducing the time for a Q_c - t curve, at 600 ms between pulses, from about 10 minutes to about 10 seconds. When the comparison of two curves is sufficient, this system offers considerable advantages. However, when a permanent record of the curve or the exact value of the collected charge are desired, this system presents a problem. Photography appears to be the most likely solution.

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