UNIFIED DC/SMALL-SIGNAL/LARGE-SIGNAL MICROWAVE DEVICE MODELING AND CIRCUIT OPTIMIZATION

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Abstract

This thesis presents an in-depth investigation of microwave FET device modeling and unified DC, small-signal and large-signal computer-aided design of microwave circuits.

Advances in microwave FET device modeling are reviewed. The physical, analytical and nonlinear empirical models and their relationship are discussed.

A new integrated DC and small-signal FET model parameter extraction approach is presented which simultaneously fits the FET model responses to the DC and small-signal measurements. Detailed formulas are derived to explore the relationship between the nonlinear DC equivalent circuit and the small-signal equivalent circuit linearized at given bias points.

A large-signal FET model parameter extraction approach is introduced. The power spectrum responses of the model are calculated employing the newly exploited harmonic balance (HB) technique for efficient nonlinear frequency-domain circuit simulation. State-of-the-art optimization tools are used to fit model responses to corresponding measurements. Special considerations are given to weighting factor assignment which takes into account the wide spread magnitude of the error functions in the optimization.

The HB technique for nonlinear frequency domain simulation of microwave circuits is discussed. The formulations of the HB equation, its Jacobian matrix and the related discrete Fourier transformation are described. A new approach for constructing the multiport matrix especially suitable for HB based circuit optimization is presented.

The theoretical background of the unified DC, small-signal and large-signal circuit simulation is investigated. Derivations of the inherent consistency between DC/small-signal simulation and general nonlinear HB simulation are presented. A novel circuit design concept is introduced which explores the seamless integration of DC/small-signal and large-signal circuit design with multi-dimensional specifications. Examples of simultaneous DC/small-signal/large-signal FET model parameter extraction and a small-signal broadband amplifier design are given to demonstrate the concept.

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Chapter 1

INTRODUCTION

Computer-aided design (CAD) of circuit systems in electrical engineering has been growing ever since its introduction in the late 1960's (Temes and Calahan 1967 [67]). Today, circuit CAD systems are applied in areas such as analog, digital, and microwave circuit design. They cover circuits ranging from simple and linear to sophisticated large-scale nonlinear systems.

In microwave engineering, commercial CAD software programs have been developed. Some of them are widely used by the microwave society, for example, the linear microwave circuit CAD systems *Touchstone* by EEsof Inc., [71] and *SuperCompact* by Compact Software Inc., [65]. Today, some of the programs offer the user a design environment to allow the user to enter an actual circuit schematic, i.e., geometrically enter a circuit element-by-element. The program can schematically capture the user input, convert it to a circuit file form, analyze the circuit, and produce the final layout for manufacturing. Such comprehensive software has substantially increased the quality and productivity of circuit designs.

Though the comprehensiveness of those CAD tools has been improved significantly compared with early CAD systems, the essential requirement of a good CAD system remains and will remain the same: accurate device models, efficient circuit simulation, and based upon these, powerful circuit optimization.

The field effect transistor (FET) device is one of the fundamental active elements used in microwave circuits. Analysis and modeling of the FET device has been of continuing research interest since it was introduced by Shockley in 1952 [59]. Theoretical studies of the device physics have been carried out by device engineers. With physical modeling, the behaviour of the FET device can be thoroughly analyzed. The physical model plays an important role in understanding the device mechanism. By using the geometrical, material and process parameters, the device characteristics can be predicted before the device is manufactured. The critical drawback of such physical models, however, is the computational intensity required in numerically solving field related problems. The analytical model, on the other hand, relates the device physical parameters to equivalent circuit elements. It is relatively simple and easy to implement. However, its application is largely limited by the conditions under which the model is derived by simplification.

The empirical model, namely, the FET equivalent circuit model, has been extensively used in circuit design area. Its simplicity and flexibility makes it more efficient in circuit simulation than the physical model. There are different levels of equivalent circuits suitable for different kinds of applications. Compared with physical or analytical models, the equivalent circuit model is usually determined after the device has been manufactured, since the parameters of the model are identified with the aid of device measurements.

The main interest in the equivalent circuit model is in the circuit structure, the circuit element characterization, and the way of determining the parameters of the model elements. Several nonlinear bias-dependent FET device models have been proposed, for example, the Materka and Kacprzak model [48]. In order to identify the model parameters for a particular device, it is customary to determine some parameters using DC measurements and others using AC (RF) small-signal measurements. Such a separate determination procedure may not yield a reliable model, because a parameter determined solely from DC measurements may not be suitable for microwave simulation, and the information contained

in AC measurements is not fully utilized.

For a circuit containing nonlinear elements, the small-signal response may be simulated using small-signal equivalent circuit models for those nonlinear elements, and the nonlinear time-domain response using nonlinear equivalent circuit models. Recently, a highly efficient frequency domain simulation technique, the harmonic balance (HB) technique, has been exploited, and implemented into some commercial software products, for example, *Libra* from EEsof Inc., [45] and *Microwave Harmonica* from Compact Software Inc., [49]. However, most of them are not coupled between small-signal simulation and large-signal simulation, which imposes restrictions on possible comprehensive design of a circuit containing nonlinear devices.

This thesis addresses itself to the topics of nonlinear empirical FET device modeling and unified DC, small-signal and large-signal circuit simulation and optimization. Emphasis will be given to nonlinear FET model parameter extraction.

In Chapter 2, we review the progress of the FET device modeling and model parameter extraction. Various approaches are reviewed, including physical, analytical and empirical device modeling. In physical device modeling, the 2-dimensional and quasi-static models are examined. General descriptions of analytical modeling and nonlinear empirical device modeling are provided. Comparisons are made between those different models, and their relationships are described.

Chapter 3 describes an approach of nonlinear FET model parameter extraction. Compared with the conventional approaches in the literature, this approach utilizes the functional relationship between DC and small-signal equivalent circuits of the FET model, and extracts the model parameters by simultaneously matching the model responses to the DC and multi-frequency small-signal measurements at many bias points. The uniqueness and reliability of the model are improved. Popular nonlinear FET equivalent circuit models with practical industrial measurement data are used to demonstrate the feasibility of the

approach.

To facilitate the nonlinear large-signal simulation, we discuss the HB technique in Chapter 4. The concept of HB simulation is illustrated. The formulation and the Jacobian matrix of the HB equation are provided, together with the discrete Fourier transformation which dynamically relates the nonlinear elements simulated in the time domain and the linear part of the circuit simulated in the frequency domain. Also, a new approach for constructing the linear multiport matrix is presented in Chapter 4. The approach is simple and efficient, and can be incorporated in the HB simulation to improve the performance when the HB simulation is integrated in a circuit optimization environment.

A large-signal FET model parameter extraction technique is shown in Chapter 5, where the parameters are determined under real (large-signal) working conditions. The application of the powerful nonlinear adjoint-based optimization, which employs the HB method as the nonlinear circuit simulation technique, is described. The approach simultaneously processes multi-bias, multi-power input, multi-fundamental-frequency excitations, and multiharmonic measurements to uniquely reveal the parameters of the FET model.

A new design strategy for microwave circuit design is presented in Chapter 6. The analytical relationship between DC/small-signal and frequency domain large-signal analyzes is derived. A consistent device model is used for both small-signal and large-signal circuit simulation and design. Unified circuit optimization can be performed with respect to multi-dimensional specifications, such as bias, frequency, input power, temperature, etc. In one example the nonlinear FET model parameters are extracted by simultaneously matching DC, small-signal and large-signal measurements. In the other example a small-signal broadband amplifier is designed with its upper-end of the dynamic range expanded.

The thesis is concluded in Chapter 7 with some suggestions for future research and development.

The author contributed substantially to the following original developments presented in this thesis:

1. Integrated nonlinear FET equivalent circuit model parameter extraction by simultaneously matching model responses to the DC and small-signal measurements, where the DC and small-signal equivalent circuits are functionally related.

2. Nonlinear large-signal FET equivalent circuit model parameter extraction using a HB based optimization technique.

3. An efficient approach to establish a linear circuit matrix for HB simulation.

4. Theoretical derivation of the consistency of DC/small-signal analysis and the frequency-domain nonlinear large-signal HB analysis.

5. Presentation of unified DC/small-signal/large-signal circuit design strategy.

6. Applications of unified circuit design for FET model parameter extraction and small-signal amplifier design.

Chapter 2

REVIEW OF FET DEVICE MODELING

2.1 INTRODUCTION

For circuit simulation, it is necessary to understand the behaviour of the devices used in the circuit. Device modeling, consequently, is of fundamental importance to circuit designs. The philosophy of device modeling is to establish a model such that it can produce the same output as the actual device would in a working environment.

Consider the nonlinear active MESFET device. A schematic description of the MESFET device is given in Figure 2.1. The device has wide applications in microwave engineering, such as amplifiers, mixers, etc. Various MESFET modeling approaches have been seen in the literature. A brief survey by Estreich (1987) [33] gives a schematic description of MESFET device modeling progress for monolithic microwave integrated circuits (MMICs).

Following the pioneering work done by Shockley (1952) [59], important developments in MESFET modeling may be divided into physical modeling, which simulates the actual device from the internal physical mechanism, empirical modeling, which simulates the actual device by approximating the external behaviours, and analytical modeling, which may be considered as one between physical modeling and empirical modeling. We review briefly these different modeling approaches in the following sections.

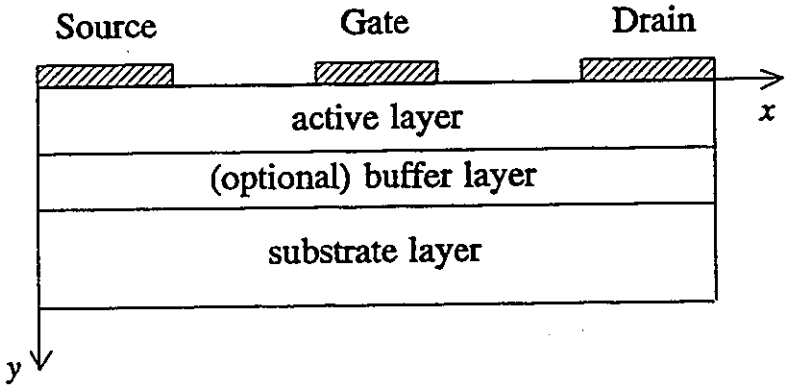


Figure 2.1: A schematic diagram of a MESFET device.

2.2 PHYSICAL MESFET DEVICE MODELING

The physical modeling approach may further be separated into 2-dimensional numerical and 2-dimensional quasi-static modeling approaches.

2.2.1 2-Dimensional Numerical Model

Consider the schematic MESFET diagram shown in Figure 2.1. By applying Poisson's equation and Boltzmann's transport equation, Reiser (1973) [57] presented a 2-D numerical model which simulates the MESFET device by using its geometrical and material parameters. There are two basic partial differential equations governing the behaviour of the device: the Poisson equation

$$\nabla^2\psi = -\frac{q}{\epsilon_0\epsilon_r}(N-n) \tag{2.1}$$

and the current continuity equation

$$\nabla \cdot J_n = q\frac{\partial n}{\partial t} \tag{2.2}$$

where ψ is the electric potential, ϵ_0 is the permittivity of free space, ϵ_r is the relative permittivity of the material, q is the electron charge, N represents the doping density (or

doping profile), n is the electron density distribution. These two equations are defined for the device active, buffer and substrate regions.

The conducting current density can be expressed as

$$J_n = q(n\mu E + D\nabla n) \tag{2.3}$$

where the electric field E is derived from

$$E = -\nabla\psi \tag{2.4}$$

and μ and D are electron mobility and diffusion coefficient, respectively. The doping density N is a function of geometric position. The electric potential ψ and the electron density distribution n are both functions of geometrical position and time.

The boundary conditions related to the Poisson and current continuity equations are taken such that (1) the electric potential and the electron density distribution at the drain, gate and source contacts are constant, (2) there is no current flowing through the boundary between the surrounding space and the material excluding the contacts, in other words, the gradient parts of either electric potential or electron density distribution perpendicular to the surface, except for the drain, gate and source contacts, are zero.

Finite difference or finite element techniques can be applied to numerically solve those two basic equations in time steps. The time domain solutions of the electric field E and electron density n can be used to compute the time domain drain and gate currents using (2.3)

$$J_t = J_n + \epsilon_0\epsilon_r\frac{\partial E}{\partial t} \tag{2.5}$$

where J_t stands for total current density, from which the time domain response of the device can be obtained.

The DC characteristic of the device can be obtained if the time-domain simulation reaches steady state. Using a step-response calculation together with Fourier transformation

[43], we can derive frequency domain small-signal Y parameters of the device at a given bias point from the time domain simulation, i.e., a small-signal equivalent circuit for the device can be determined and used for circuit simulation [57].

This 2-D numerical model provides detailed insight into device operation. It can theoretically be used for circuit simulation purposes. In practice, however, the most serious disadvantage which limits the application of this model has been the intensive computation time required for the time domain simulation. Also in Reiser's 2-D model, the velocity overshoot phenomenon which exists in the short-gate length FET was not considered.

Curtice *et al.* (1981) [25] and Snowden *et al.* (1987) [63] proposed a temperature model and a energy model, respectively, to incorporate the velocity overshoot phenomenon. Besides the electric potential and electron density distribution being considered as variables in the simulation, the electron temperature distribution is also included as a variable and iteratively solved together with the other two variables, i.e., ψ and n. The accuracy of the model is therefore improved, though at cost of even higher computational intensity.

On the other hand, an approach to approximate the effect of velocity overshoot was proposed by Thornber (1982) [68], Kizilyalli and Artaki (1989) [39]. The principle is based on the observation that velocity overshoot occurs at an area where the electric field has a large gradient with respect to the longitudinal direction. Hence a modification term proportional to the magnitude of the gradient of the electric field is introduced to approximate the effect of velocity overshoot, i.e.,

$$J_n = q\left(n\mu E + D\nabla n + n\mu L(E)\frac{\partial E}{\partial x}x^0\right) \tag{2.6}$$

where $L(E)$ is a length coefficient used to add the velocity overshoot effect to the current density J_n, x is the longitudinal coordinate parallel to the gate surface, x_0 is the unit vector in the x direction, and E is the Euclidian norm of E. Compared with the temperature or energy model, this approximation approach is simple and easy to implement. However, more

studies in this area are required, especially in the determination of the length coefficient $L(E)$.

2.2.2 2-Dimensional Quasi-Static Model

In order to take advantage of the 2-D numerical model while making it computationally feasible, a simplified 2-D model has been proposed by Khatibzadeh and Trew (1988) [38]. The so-called Trew model starts from the basic Poisson equation (2.1) and the current continuity equation (2.2). Instead of solving the electric potential $\psi(x,y)$ and the electron density distribution $n(x,y)$ directly, a functional form for $n(x,y)$ is assumed *a priori*. Therefore, ψ can be solved analytically.

Consider the active region of a MESFET used in the Trew model, as shown in Figure 2.2. The electron density distribution $n(x,y)$ is assumed

$$n(x,y) = [1 + \gamma(x - L_1)]\,T(d(x),y)N(y) \tag{2.7}$$

where γ is a model parameter, $T(d(x),y)$ is a transition function and $N(y)$ is the doping density which is assumed to be a function of y. The transition function $T(d(x),y)$ is defined as

$$T(d(x),y) = 1 - \frac{1}{1 + \exp\left[\dfrac{y - d(x)}{\lambda}\right]} \tag{2.8}$$

where $d(x)$ is the effective depletion-layer depth and λ is a model parameter describing the width of the transition region.

Similar to the 2-D numerical model, this model accepts arbitrary doping density N, and the drain and source currents can be calculated for given gate and drain biases. Since the electric potential ψ can be solved analytically due to the assumed electron density distribution $n(x,y)$, there is no numerical method involved in solving the partial differential equations. Thus, this model is much more efficient than the true 2-D numerical model.

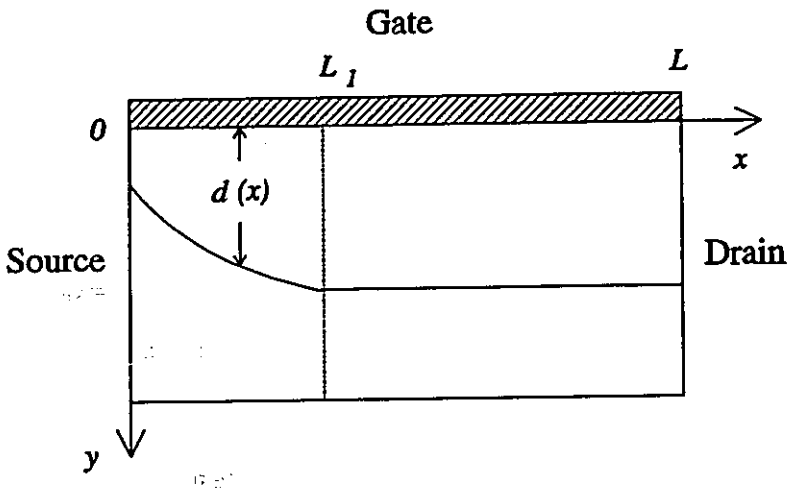


Figure 2.2: Active region of a MESFET.

Because of its relative efficiency and the ability to simulate the device from basic geometrical and material parameters, the model has been used in circuit designs, for example by Bandler *et al.* (1990) [20].

Due to the fact that the electron density distribution n is a function of time t as well as space x and y, an accurate time domain response can not be obtained theoretically. Thus, we term it a 2-D quasi-static model. On the other hand, the computation time required to simulate this model is still very long compared with the empirical model to be discussed in the next section.

2.3 NONLINEAR EMPIRICAL FET MODEL

The nonlinear empirical FET model, first proposed by Willing *et al.* (1978) [72], is a model which approximates the electrical behaviour of the FET device by an empirical equivalent circuit. The formation of the equivalent circuit is consistent with the physical structure and working mechanism of the FET, for instance, the circuit correspondence described by Pucel *et al.* [54].

Several different nonlinear empirical FET models have been proposed since Willing's

work. For instance, the Tajima model (1981) [66], the Materka model (1985) [48], the Curtice model (1985) [27] and the Statz model (1987) [64]. A basic nonlinear intrinsic FET model can be shown as in Figure 2.3, where C_{gs}, C_{dg}, C_{ds} and R_{in} can all be bias dependent as well as three nonlinear current sources i_{gs}, i_{dg}, and i_{ds}. Besides the slight differences in the circuit structure, the major differences between these models are in the expressions used to characterize the nonlinear circuit elements, most noticeably, the nonlinear current source i_{ds}. As an example, i_{ds} from the Curtice model reads

$$\begin{aligned} i_{ds} &= (A_0 + A_1 v_1 + A_2 v_1^2 + A_3 v_1^3)\tanh(\gamma v_d) \\ v_1 &= v_g(t-\tau)(1+\beta(V_{DS0} - v_d)) \end{aligned}$$

where A_0, A_1, A_2, A_3, β, γ, τ and V_{DS0} are model parameters, and i_{ds} from the Statz model is

$$\begin{aligned} i_{ds} &= \frac{\beta(v_g - V_T)^2}{1 + b(v_g - V_T)} \left\{ 1 - \left(1 - \frac{\alpha v_d}{3} \right)^3 \right\} (1 + \lambda v_d), \\ &\qquad \text{for } 0 < v_d < \frac{3}{\alpha} \\ i_{ds} &= \frac{\beta(v_g - V_T)^2}{1 + b(v_g - V_T)} (1 + \lambda v_d), \\ &\qquad \text{for } v_d \geq \frac{3}{\alpha} \end{aligned}$$

where β, V_T, b, α and λ are model parameters.

Extrinsic elements of a FET model may include the bond pad effect, the contact effect, the packaging effect, etc., for example, R_g, R_d, R_s, L_g, L_d and L_s shown in Figure 2.4. These elements are usually considered as bias-independent, i.e., linear elements.

The determination of the parameters of a nonlinear FET model has been discussed in the literature. The principle is to match the model responses as close to the device responses as possible, where the device responses are normally from actual device measurements, though simulation results from physical models may also be taken as simulated measurements.

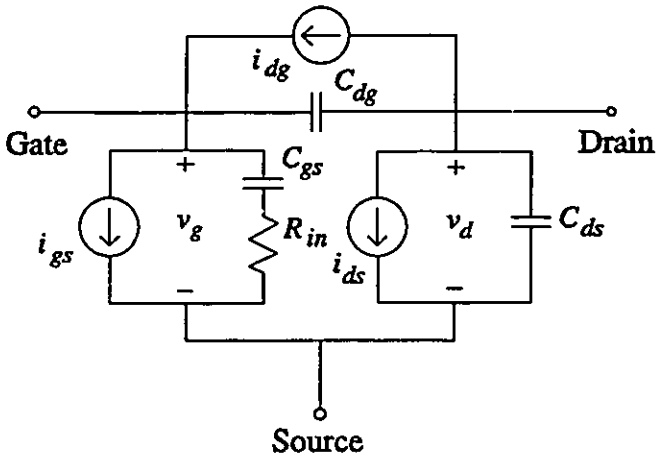


Figure 2.3: A basic nonlinear intrinsic FET model.

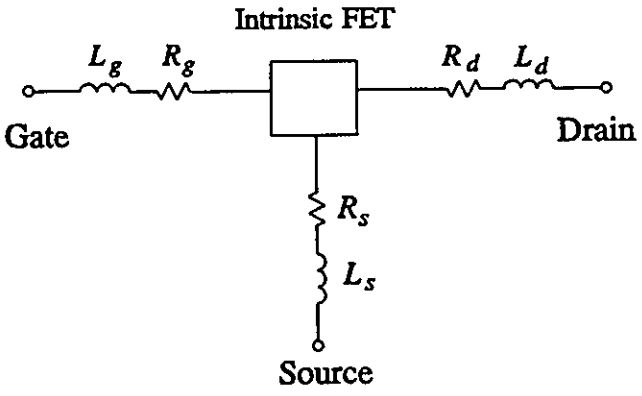


Figure 2.4: Basic extrinsic part of a FET model.

The measurements used for nonlinear FET model parameter extraction have been seen, in the literature, in the form of DC, small-signal S parameter, and large-signal load-pull measurements. Because of the indeterminacy of the parameters, different measurements are utilized for determining different sets of the total parameters of the model. Examples are listed as follows.

A. Utilizing DC Measurements

Fukui (1979) [34] developed a technique to extract R_g, R_d and R_s using DC measurements. The technique first determines the gate barrier built-in voltage by gate forward bias DC measurement. Then from the linear part of the DC I–V characteristics, $R_d + R_s$ can be obtained, as illustrated in Figure 5 of [34]. By measuring the forward gate current in three different ground connections, i.e., source and drain combined, source only and drain only, with applied voltages greater than the gate barrier built-in voltage, three resistance values can be obtained, including $R_g + R_d$ and $R_g + R_s$. Thus, R_g, R_d and R_s can be obtained.

The full range of DC I–V characteristics is commonly used for determining the parameters of i_{ds}, for example, by Curtice (1988) [28]. It has been noticed that the output conductance of a GaAs FET behaves quite differently between low and high frequency conditions. On the one hand, a series RC branch was suggested between the intrinsic drain and source to compensate the frequency dependency of the output conductance, as shown in Figure 2.5, by Camacho-Penalosa and Aitchison (1985) [23]. On the other hand, a special DC measurement technique operating at relatively high frequency was proposed, e.g., by Smith *et al.* (1986) [60] and Paggi *et al.* (1988) [51], to obtain more accurate DC I–V curves for high frequency purposes.

B. Utilizing Small-Signal Measurements

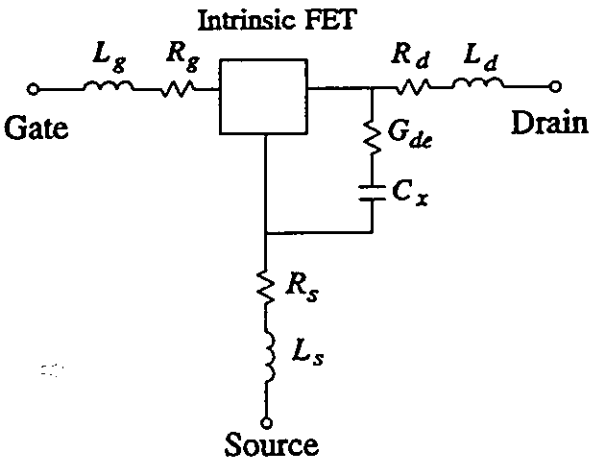


Figure 2.5: High frequency compensation branch (G_{de}, C_x) for the FET model.

Using small-signal measurements, Willing *et al.* (1978) [72] first treated the model as a linear small-signal model, and determined the small-signal parameters at various bias conditions. Then polynomial expressions were used to approximate the nonlinear elements of the model, and the coefficients of the polynomials were identified by matching individual polynomials to their corresponding extracted parameter curves.

To improve the identifiability of the model parameters, Curtice *et al.* (1984) [26] divided the small-signal S parameter measurements into *cold* and *hot* circumstances. Cold FET S parameter measurements correspond to zero drain-to-source bias conditions. The equivalent circuit is simplified to a two-port containing no active elements as shown in Figure 2.6. L_g, L_d, L_s and C_{ds} can be determined. Hot FET S parameter measurements are the normal S parameter measurements and are used for extracting parameters of the other capacitive elements.

C. Utilizing Large-Signal Load-Pull Measurements

Recently, Epstein *et al.* (1988) [32] proposed an approach to use large-signal load-pull measurements for FET model parameter extraction. Besides using the Fukui technique, DC I-V curve fitting, cold and hot S parameter measurements to extract model parameters

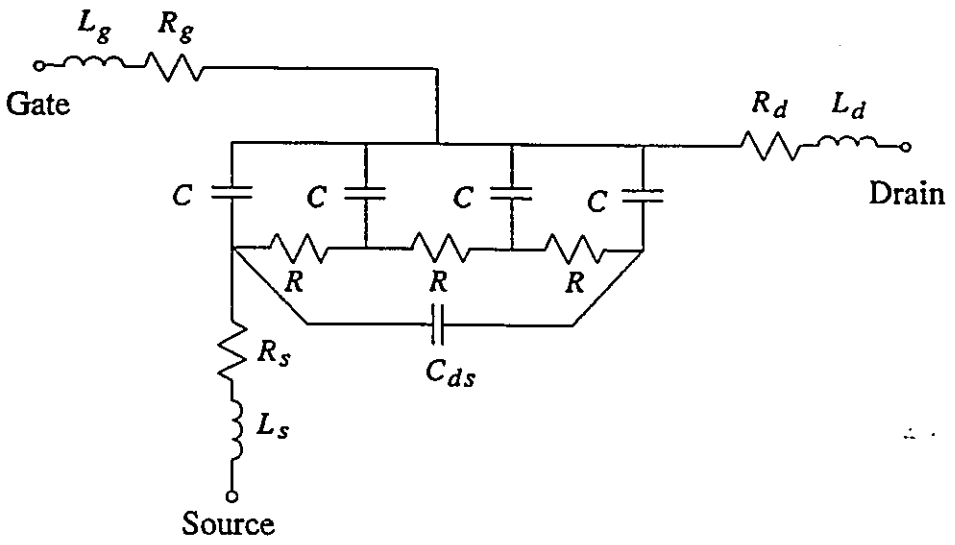


Figure 2.6: FET equivalent circuit at zero drain-to-source bias voltage.

separately, the final stage is to modify the parameters of i_{ds}, C_{gs}, C_{dg}, C_{ds} and G_{dc} by fitting the model power responses to the device load-pull power measurements. Harmonic balance simulation is used.

Summing up, unlike the physical model the parameters of the empirical model elements are determined *sequentially* in such a way that the model response is as close to the actual device response as possible. Because of this, the empirical model may accurately reproduce the device responses under different bias conditions, provided that the model is appropriate for the device to be modeled. Compared with the 2-D and 2-D quasi-static models, the empirical model is particularly suitable for circuit simulation. It is the kind of model which has been implemented in major commercial software programs, for example, the Curtice model in *Libra* [45] and *Microwave Harmonica* [49]. Another apparent advantage of the empirical model is that the model may well be suitable to different kinds of FETs, due to the empirical modeling principle.

For the empirical model, however, it is difficult to relate the model parameters to the device geometrical and material parameters. One empirical model may not be suitable

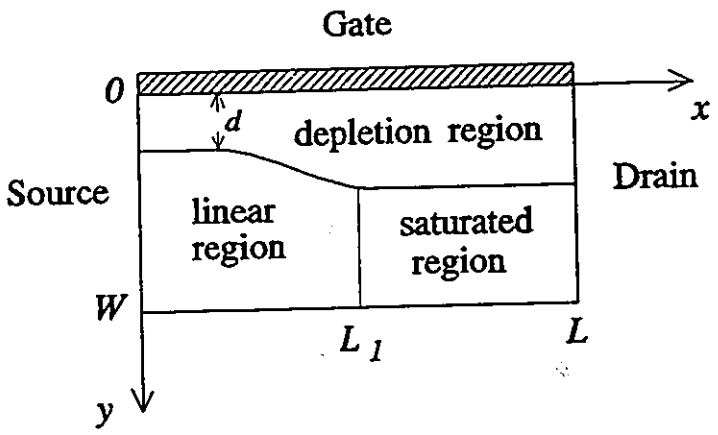


Figure 2.7: Active region of a MESFET for the analytical model.

for one particular device, since the empirical expression pattern may not be able to fit that particular device response pattern. On the other hand, the uniqueness of the model parameters may be improved by sequential parameter extractions, but the accuracy of the model may be hindered because of lack of freedom in fitting individual measurements.

2.4 ANALYTICAL MODEL

The analytical model can be considered as a model between the 2-D numerical model and the empirical model. It starts from the device physics point of view, using device physical parameters. Approximations are taken to reduce the complexity of the problem, so that analytical expressions for the equivalent circuit elements are derived. Different from the empirical model, the element expressions here use device geometrical and material parameters.

A perspective description of the analytical model was given by Pucel *et al.* (1975) [54]. Consider the intrinsic FET shown in Figure 2.7. The device is divided into a depletion region and a conducting channel, where uniform doping profile N is assumed for both regions.

In the depletion region, the electron density distribution $n = 0$, and the electric field is assumed to be transversal only, i.e., $E_y \gg E_x$ and therefore E_x is neglected in the depletion region. The conducting channel is divided into a linear region and saturated region according to the value of the longitudinal electric field E_x. $E_y = 0$ is assumed in the linear region, and constant electron density is assumed in the whole channel.

With those simplifications the channel current can be analytically derived [54]. Other elements in the equivalent circuit model are derived accordingly.

One of the basic phenomena, the velocity saturation phenomenon which was not considered by Shockley [59], was included in the model by Pucel *et al.* [54]. The calculation of the drain current, small-signal equivalent circuit parameters such as the gain g_m and the gate-to-source capacitance C_{gs} can be performed by closed form analytic formulas. However, there is a condition upon which the simplifications are based, i.e., the gate length L should be much larger than the channel thickness W.

Ladbrooke (1989) [42] developed an analytical model by including the short gate effect existing in submicron MESFETs which have become more popular. The active region of the device is extended by X in the Ladbrooke model, as illustrated in Figure 2.8. An approximate formula was given which relates the length X with device bias voltages as well as physical parameters. Other effects, such as the transversal field in the conducting channel and velocity overshoot, were also considered.

The advantages of the analytical model are its relative simplicity, and closed form analytical expressions which relate the model geometrical and material parameters to the equivalent circuit parameters. Circuit design using device geometrical and material parameters is possible. However, the simplifications required for the analytical model, for example, the assumptions for the doping density and the electron density distribution, limit the simulation accuracy and, therefore, the applications of the model.

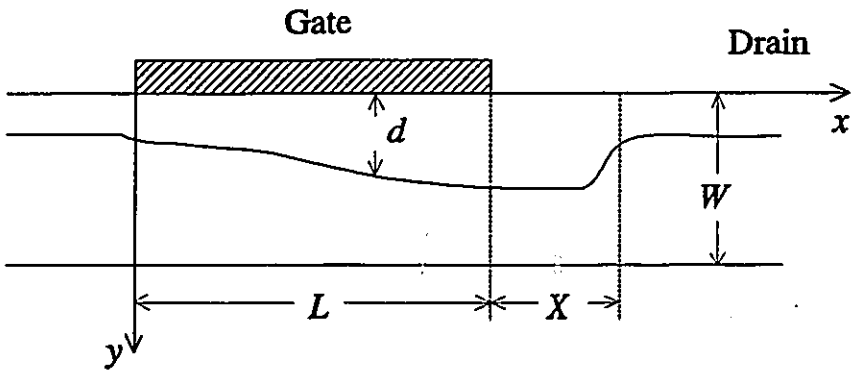


Figure 2.8: Schematic MESFET diagram for the Ladbrooke model.

2.5 RELATIONSHIP BETWEEN DIFFERENT MODELS

Examining the different FET models discussed in the previous sections, we may summarize their relationship in Figure 2.9. It can be seen from Figure 2.9 that the 2-D numerical, 2-D quasi-static and analytical models are directly related to the original device. They simulate the device using geometrical and material parameters. The empirical model, on the other hand, relates to the device via device measurements. The model is undefined without certain device response data which is normally from actual device measurements. In terms of circuit simulation, the empirical model is of superior efficiency over other models.

It is natural and has been seen in the literature to connect the empirical model to the physical parameters, i.e., to use the simulation results from the physical models as measurements, and determine the empirical model parameters from those simulated measurements, for example, the works by Reiser (1973) [57], by Ghione *et al.* (1989) [35], and by Pantoja *et al.* (1989) [52]. Since the simulated measurements can be obtained off-line, circuit designs can, therefore, be carried out at the physical device level. The feasibility of such an approach, however, depends upon the simulation time of the physical model if optimization at the device level is involved.

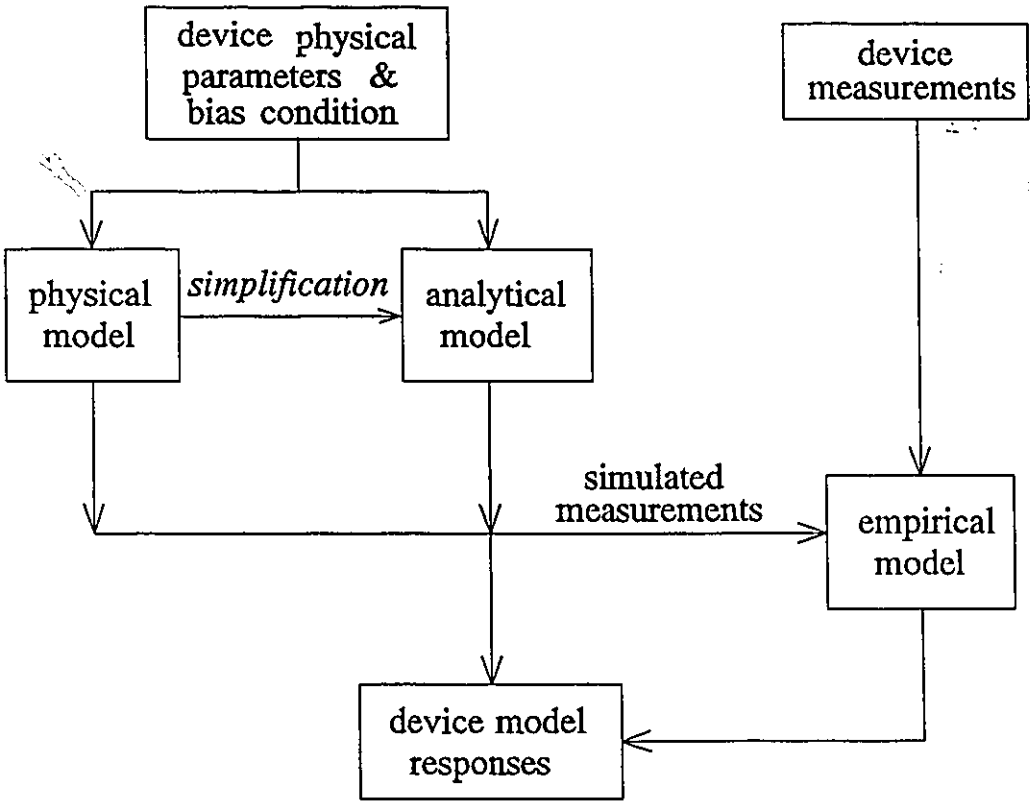


Figure 2.9: Relationship between different FET device models.

There is still another FET modeling approach, the Monte Carlo particle model, for example [50], which simulates the device down to a microscopic level, suitable for studying the device physics. We will not discuss the Monte Carlo model, for it is out of the scope of this thesis.

2.6 CONCLUDING REMARKS

In this chapter, we briefly reviewed microwave MESFET device modeling. Several modeling approaches were described, namely, physical, analytical and empirical modeling, and the relationships between them were illustrated.

It can be seen that the nonlinear empirical model, though indirectly related to the device geometrical and material parameters, is of superior efficiency in circuit simulation programs. When we apply the simulation results obtained from other physical models as simulated measurements to determine its parameters, the empirical model can effectively be used to predict the designed circuit behaviour without actual device measurements.

A principal interest of nonlinear empirical FET modeling is how to efficiently and reliably identify the parameters when the measurements are given. This is a principal theme in the following chapters. We will discuss nonlinear empirical FET model parameter extraction approaches and related circuit simulation techniques, since parameter extraction is one of the key aspects of applying the empirical model in microwave engineering.

Because of the characteristics of empirical modeling, we will not discriminate between devices in the following chapters.

Chapter 3

INTEGRATED FET MODEL PARAMETER EXTRACTION

3.1 INTRODUCTION

In Chapter 2, we reviewed several FET modeling approaches. We showed that the empirical model, due to its equivalent circuit format, is consistent with normal circuit simulation techniques, and therefore, is particularly efficient from the computational point of view. In circuit design involving optimization, the circuit needs to be repeatedly simulated, making the empirical model fundamentally important. In this chapter we develop a technique of extracting nonlinear empirical FET model parameters from DC and small-signal measurements.

Conventionally, the parameters are extracted by minimizing the difference between the model responses and the measurements. As discussed in Chapter 2, in order to alleviate indeterminacy as well as for simplicity, techniques have been implemented (e.g., Curtice and Ettenberg [27], Kondoh [40], Materka and Kacprzak [48]) which separate the DC, low-frequency, and high-frequency measurements and divide the model parameters into corresponding subsets. This defines a set of subproblems to be solved sequentially. Such a sequentially decoupled solution, however, may not be reliable: a parameter determined solely from DC measurements may not be suitable for the purpose of microwave simulation,

and the information contained in AC measurements is not fully utilized.

Bandler, Chen and Daijavad (1986) [5] proposed a multicircuit algorithm which can improve the uniqueness of the solution by simultaneously processing multiple sets of S-parameter measurements made under different bias conditions. However, the authors assumed for computational purposes that the model elements were either completely bias-independent or arbitrarily bias-dependent.

The approach presented in this chapter by Bandler, Chen, Ye and Zhang (1988) [10] not only attempts to match DC and AC measurements simultaneously, but also employs the DC characteristics of the device as constraints on the bias-dependent parameters. This enables us to use more efficiently the information contained in both DC and non-zero frequency measurements and reduce the degrees of freedom by imposing constraints on bias-dependent parameters, thus improving the identifiability and reliability of the parameters extracted.

In the following sections, we first demonstrate the feasibility and usefulness of integrating DC and AC modeling in one optimization problem. A simple RC circuit is used to illustrate the integrated modeling concept. The FET model parameter extraction optimization problem with both DC and AC responses is then formulated. Depending upon different situations, both ℓ_1 and ℓ_2 optimization techniques can be used for parameter extraction. The sensitivity calculation of the model responses employing adjoint analysis is described in detail, which significantly improves accuracy and efficiency compared with the conventional perturbation approach. Numerical examples are given to demonstrate the modeling approach.

3.2 FEASIBILITY OF INTEGRATED PARAMETER EXTRACTION

3.2.1 The Identifiability of Model Parameters

To illustrate identifiability of the model parameters, we utilize the concept of analog circuit fault diagnosis [4,5]. Consider a system with a complex-valued vector of responses

$$h(\phi) = [h_1(\phi) \ \cdots \ h_m(\phi)]^T$$

where $\phi = [\phi_1 \ \cdots \ \phi_n]^T$ is the parameter to be identified from the response $h(\phi)$, and we assume $m \geq n$.

It is shown by Bandler and Salama in [4] that, if

$$\nabla h^T(\phi) \left[\nabla h^T(\phi)\right]^T$$

is of full rank, the parameter ϕ is locally identifiable, where ∇ is the partial derivative operator $\partial/\partial\phi$. In other words, if

$$\text{Rank}\left(\nabla h^T(\phi) \left[\nabla h^T(\phi)\right]^T\right) = n \tag{3.1}$$

ϕ has unique local solution(s) when solved from the following nonlinear equations

$$f_j - h_j(\phi) = 0, \quad j = 1, \ldots, m$$

where f_j is the measured value of response $h_j(\phi)$.

It is not difficult to see that the measure of identifiability of ϕ in (3.1) is equivalent to testing the rank of the $m \times n$ Jacobian matrix

$$J = \left[\nabla h^T(\phi)\right]^T. \tag{3.2}$$

If the rank of matrix J is less than n, then ϕ will not be uniquely identifiable from h. Equation (3.1) also shows that by simultaneously processing DC and AC responses, we may

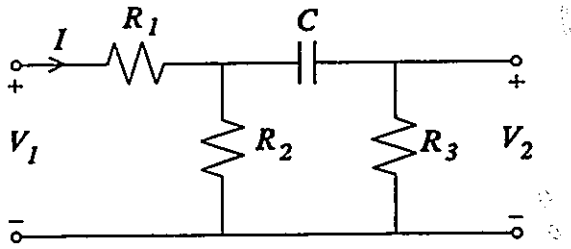


Figure 3.1: Simple RC linear circuit example.

increase the identifiability of ϕ, because the dimension m of $h(\phi)$ is increased compared with separately processing DC and AC responses.

3.2.2 A Simple RC Circuit Example

As an example to illustrate that combining DC and AC modeling is both feasible and useful for parameter extraction, let us examine the simple linear RC circuit shown in Figure 3.1. The unknown parameters are $\phi = [R_1\ R_2\ C]^T$. R_3 is assumed to be a known resistor. We also assume the responses to be the DC current I, under the DC excitation $V_1 = V_{DC}$, as

$$I = \frac{V_{DC}}{R_1 + R_2} \tag{3.3}$$

and the AC (complex) voltage V_2, under the AC excitation $V_1 = V_{AC}$, as

$$V_2 = \frac{V_{AC} R_2 R_3 sC}{sC(R_1R_2 + R_1R_3 + R_2R_3) + R_1 + R_2} \tag{3.4}$$

where s denotes the complex frequency variable. We discuss whether we can identify ϕ by utilizing DC and/or AC measurements.

1) DC Response Only

The corresponding Jacobian matrix of the DC response (3.3) is

$$J_{DC} = \left[\ -V_{DC}/(R_1 + R_2)^2 \quad -V_{DC}/(R_1 + R_2)^2 \quad 0\ \right]. \tag{3.5}$$

It is clear that rank $J_{DC} = 1$. Therefore R_1 and R_2 are not identifiable from the DC response I. This result is also straightforward intuitively.

2) AC Response Only

The corresponding Jacobian matrix of the AC response (3.4) can be derived as

$$J_{AC} = \begin{bmatrix} -D[s_1C(R_2+R_3)+1] & D[R_1(s_1CR_3+1)/R_2] & D[(R_1+R_2)/C] \\ \vdots & \vdots & \vdots \\ -D[s_mC(R_2+R_3)+1] & D[R_1(s_mCR_3+1)/R_2] & D[(R_1+R_2)/C] \end{bmatrix} \tag{3.6}$$

where s_i, $i = 1, \cdots, m$, indicate different frequencies, and

$$D = \frac{V_{AC}R_2R_3sC}{[sC(R_1R_2+R_1R_3+R_2R_3)+R_1+R_2]^2}.$$

Denoting the three columns of J_{AC} by J_1, J_2, and J_3, we can obtain

$$\frac{(R_2+R_3)}{R_1}J_2 + \frac{R_3}{R_2}J_1 - \frac{C}{(R_1+R_2)}J_3 = 0 \tag{3.7}$$

which means that the rank of J_{AC} is less than 3, no matter how many frequency points are used. Hence we cannot uniquely determine ϕ from the response V_2.

3) Combined DC and AC Responses

When we consider both DC and AC responses simultaneously then, combining (3.5) and (3.6), the Jacobian matrix becomes

$$J = \begin{bmatrix} -V_{DC}/(R_1+R_2)^2 & -V_{DC}/(R_1+R_2)^2 & 0 \\ -D[s_1C(R_2+R_3)+1] & D[R_1(s_1CR_3+1)/R_2] & D[(R_1+R_2)/C] \\ \vdots & \vdots & \vdots \\ -D[s_mC(R_2+R_3)+1] & D[R_1(s_mCR_3+1)/R_2] & D[(R_1+R_2)/C] \end{bmatrix}$$

which is of full rank for $m \geq 2$. This indicates that ϕ is identifiable from the response

$$h(\phi) = [I(\phi) \;\; V_2(\phi, s_1) \;\; \cdots \;\; V_2(\phi, s_m)]^T.$$

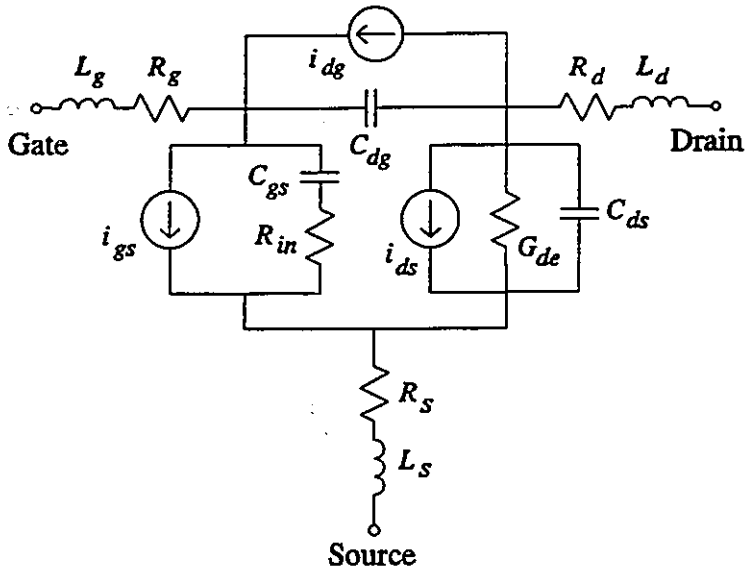


Figure 3.2: A typical nonlinear FET device equivalent circuit model.

3.3 NONLINEAR FET EQUIVALENT CIRCUIT MODEL

A typical nonlinear FET equivalent circuit model may be as shown in Figure 3.2 [70], which is composed of linear and nonlinear elements. i_{gs}, i_{ds} and i_{dg} are voltage-controlled nonlinear current sources, C_{gs}, C_{ds} and C_{dg} are nonlinear capacitances, R_{in} is a nonlinear resistance, R_g, R_d, R_s and G_{de} are linear resistances, L_g, L_d and L_s are linear inductors. There are various differences between various nonlinear models proposed in the literature. For example, C_{ds} may be considered as a linear element in some nonlinear models.

The linear and nonlinear elements in a nonlinear FET equivalent circuit are basically derived from the device physical structure. The part of the equivalent circuit which corresponds to the intrinsic part of the device is usually considered nonlinear, and the part which corresponds to the extrinsic part of the device linear. The parameters characterizing the elements of the circuit model are of principal interest, i.e., the goal of FET model parameter extraction.

We will present an approach to directly extract parameters of a nonlinear circuit

model from large-signal measurements in Chapter 5. In this chapter, we focus on an approach to extract those model parameters from simultaneous matching of DC and small-signal measurements. In such a situation, special consideration needs to be taken in the circuit simulation and optimization.

3.3.1 Classification of Model Parameters

In the case of DC and small-signal analysis, the model elements can be individually classified as bias-independent, unconstrained bias-dependent, or constrained bias-dependent, due to the nature of DC and small-signal simulations.

We can further separate the elements that appear in both DC and AC (small-signal) models from those appearing only in the AC model. For example, the gate resistance R_g in a FET equivalent circuit model appears in both DC and AC small-signal models, while the gate-to-source capacitance C_{gs} only appears in the AC small-signal model. Therefore, we define six subsets of model elements, denoted by $\boldsymbol{x}_a$, $\boldsymbol{x}_b$, $\boldsymbol{x}_c$, $\boldsymbol{x}_d$, $\boldsymbol{x}_e$ and $\boldsymbol{x}_f$, respectively, where $\boldsymbol{x}_a$ and $\boldsymbol{x}_b$ are bias-independent, $\boldsymbol{x}_c$ and $\boldsymbol{x}_d$ are unconstrained bias-dependent, and $\boldsymbol{x}_e$ and $\boldsymbol{x}_f$ are constrained bias-dependent. $\boldsymbol{x}_a$ and $\boldsymbol{x}_c$ appear in both the DC and AC models, whereas $\boldsymbol{x}_b$ and $\boldsymbol{x}_d$ affect only the AC small-signal equivalent circuit.

We use a superscript k to indicate a different bias point and the corresponding device model. Then, $\boldsymbol{x}_c^k$, $\boldsymbol{x}_d^k$, $\boldsymbol{x}_e^k$ and $\boldsymbol{x}_f^k$ belong only to the model under the kth bias, whereas $\boldsymbol{x}_a$ and $\boldsymbol{x}_b$ remain unchanged for different bias points. $\boldsymbol{x}_c^k$ and $\boldsymbol{x}_d^k$ are linear elements under the kth bias and have no effect at any other bias conditions.

We express the functional dependency of $\boldsymbol{x}_e$ and $\boldsymbol{x}_f$ on the bias condition by $\boldsymbol{x}_e^k = \boldsymbol{x}_e(\boldsymbol{\alpha}, \boldsymbol{V}^k)$ and $\boldsymbol{x}_f^k = \boldsymbol{x}_f(\boldsymbol{\alpha}, \boldsymbol{\beta}, \boldsymbol{V}^k)$, where $\boldsymbol{\alpha}$ and $\boldsymbol{\beta}$ are the coefficients of the constraints, and $\boldsymbol{V}^k = \boldsymbol{V}(\boldsymbol{x}_a, \boldsymbol{x}_c^k, \boldsymbol{\alpha})$ denotes the DC state variables (such as the voltages and currents) at the kth bias point. The coefficient $\boldsymbol{\alpha}$ affects the DC equivalent circuit but $\boldsymbol{\beta}$ does not.

Table 3.1 summarizes the foregoing definitions. Note that this kind of classification

Table 3.1:

DEFINITIONS OF THE MODEL PARAMETERS

Category	Notation	Brief definition
bias-independent	x_a	affects DC and AC circuits
	x_b	affects AC circuit
unconstrained bias-dependent	x_c^k	affects DC and AC circuits at the kth bias condition
	x_d^k	affects AC circuit at the kth bias condition
constrained bias-dependent	$x_e(\alpha, V^k)$	α affects DC and AC circuits
	$x_f(\alpha, \beta, V^k)$	β affects AC circuit only

$V^k = V(x_a, x_c^k, \alpha)$ denotes the DC state variables (such as the voltages and currents) under the kth bias condition.

is suitable for DC and small-signal simulations.

This categorization stems from the consideration of the physical device and a feasible model. It is clear that we need x_a and x_b to represent the elements which do not vary or vary only slightly with the bias conditions, such as the package capacitance and lead inductance of a FET. We need x_c^k and x_d^k to represent those bias-dependent elements whose functional bias dependency expressions may not be known or available; on the other hand x_c^k and x_d^k may be used to test or investigate the functional bias-dependent properties of the model elements.

Introducing $x_e(\alpha, V^k)$ and $x_f(\alpha, \beta, V^k)$ allows us to describe other bias-dependent elements whose bias-dependent properties can be expressed by functions or, as we refer to them, constraints. Such constraints may be derived from physical characteristics of the

device. They may be introduced empirically to simulate the pattern of the DC characteristic curves. They may also include mathematical expressions, such as polynomials. These constraints reduce the degrees of freedom in modeling, since the parameters of the elements x_e and x_f, namely α and β, are bias-independent.

In practical parameter extraction, some of the parameters may be available via direct measurement, for example, the method by Fukui [34]. In the general case, we use ϕ to denote the variables to be determined from parameter extraction. It is obvious that

$$\phi \in \{x_a, x_b, x_c, x_d, \alpha, \beta\}.$$

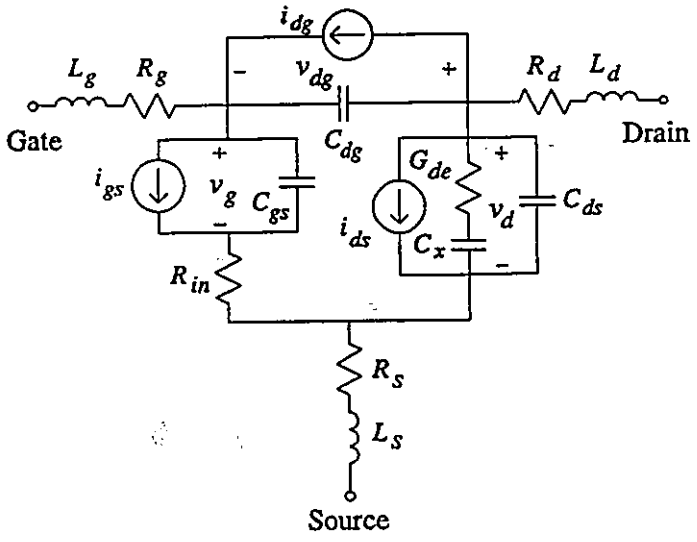
For one particular bias point and for one particular response, only some of the variables in ϕ are active while the rest have no effect on the response. For example, if $x_{cj}^k \in \phi$, x_{cj}^k has no effect on responses at bias-points other than those at the kth bias point.

3.3.2 A Practical FET Device Example

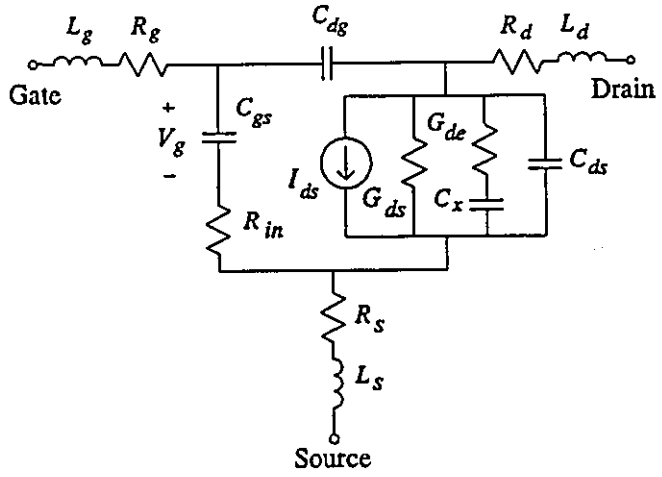
To illustrate the definitions presented in Section 3.3.1, we consider a typical nonlinear FET model of the type proposed by Materka and Kacprzak [48] which was later modified and included in *Microwave Harmonica* [49]. Here we do not include packaging effects into the model, but their consideration can be similarly taken into account. The model and its corresponding small-signal equivalent circuit are shown in Figure 3.3 (a) and (b), respectively.

In the Materka and Kacprzak model [49], the intrinsic nonlinear elements are defined as

$$\begin{aligned} i_{ds} &= F[v_g(t-\tau), v_d(t)]\left(1 + S_S \frac{v_d}{I_{DSS}}\right) \\ F(v_g, v_d) &= I_{DSS}\left(1 - \frac{v_g}{V_{P0} + \gamma v_d}\right)^{(E + K_E v_g)} \tanh\left(\frac{S_1 v_d}{I_{DSS}(1 - K_G v_g)}\right) \\ i_{gs} &= I_{G0}[\exp(\alpha_G v_g) - 1] \end{aligned}$$



(a)



(b)

Figure 3.3: (a) The Materka and Kacprzak nonlinear FET model and (b) the corresponding small-signal equivalent circuit.

$$i_{dg} = I_{B0}\exp[\alpha_B(v_{dg} - V_{BC})]$$

$$\begin{cases} R_{in} = R_{10}(1 - K_R v_g) \\ R_{in} = 0 \qquad\qquad \text{if } K_R v_g \geq 1 \end{cases}$$

$$\begin{cases} C_{gs} = C_{10}(1 - K_1 v_g)^{-1/2} + C_{1S} \\ C_{gs} = C_{10}\sqrt{5} + C_{1S} \qquad \text{if } K_1 v_g \geq 0.8 \end{cases}$$

and

$$\begin{cases} C_{dg} = C_{F0}(1 + K_F v_{dg})^{-1/2} \\ C_{dg} = C_{F0}\sqrt{5} \qquad \text{if } -K_F v_{dg} \geq 0.8 \end{cases}$$

There are two other bias-dependent elements which appear in the corresponding small-signal equivalent circuit, namely I_{ds} and G_{ds}, as illustrated in Figure 3.3 (b)

$$I_{ds} = g_m V_g e^{-j\omega\tau}$$

$$G_{ds} = \left.\frac{\partial i_{ds}}{\partial v_d}\right|_{v_g=V_{g0} \text{ and } v_d=V_{d0}}$$

where

$$g_m = \left.\frac{\partial i_{ds}}{\partial v_g}\right|_{v_g=V_{g0} \text{ and } v_d=V_{d0}}$$

and V_{g0} and V_{d0} are the DC solutions of v_g and v_d, respectively, at a bias point.

The linear extrinsic elements are taken as R_g, R_d, R_s, G_{de}, L_g, L_d, L_s, C_{ds} and C_x.

The corresponding parameters from the elements in the equivalent circuit read I_{DSS}, V_{P0}, γ, E, K_E, S_1, K_G, τ, S_S, I_{G0}, α_G, I_{B0}, α_B, V_{BC}, R_{10}, K_R, C_{10}, K_1, C_{1S}, C_{F0} and K_F from nonlinear elements, and R_g, R_d, R_s, G_{de}, L_g, L_d, L_s, C_{ds} and C_x from linear elements.

Table 3.2 gives a clear classification for all the elements and their corresponding parameters of the Materka and Kacprzak model.

Table 3.2:

PARAMETER CLASSIFICATIONS FOR THE MATERKA AND KACPRZAK FET MODEL

Category	Subset	Element	Parameters
bias-independent	x_a	R_g	R_g
		R_d	R_d
		R_s	R_s
	x_b	L_g	L_g
		L_d	L_d
		L_s	L_s
		C_{ds}	C_{ds}
		C_x	C_x
		G_{de}	G_{de}
unconstrained bias-dependent	x_c		
	x_d		
constrained bias-dependent	x_e	i_{ds}	$I_{DSS}, V_{P0}, \gamma, E, K_E, S_1, K_G, S_S$
		i_{gs}	I_{G0}, α_G
		i_{dg}	I_{B0}, α_B, V_{BC}
		R_{in}	R_{10}, K_R
	x_f	C_{gs}	C_{10}, K_1, C_{1S}
		C_{dg}	C_{F0}, K_F
		I_{ds}	$I_{DSS}, V_{P0}, \gamma, E, K_E, S_1, K_G, \tau, S_S$
		G_{ds}	$I_{DSS}, V_{P0}, \gamma, E, K_E, S_1, K_G, S_S$

(1) The DC state variables are the DC nodal voltages.

(2) $\alpha = [I_{DSS}\ V_{P0}\ \gamma\ E\ K_E\ S_1\ K_G\ S_S\ I_{G0}\ \alpha_G\ I_{B0}\ \alpha_B\ V_{BC}\ R_{10}\ K_R]^T$.

(3) $\beta = [\tau\ C_{10}\ K_1\ C_{1S}\ C_{F0}\ K_F]^T$.

(4) There are no entries in x_c and x_d, though we might consider R_{in} as x_c, and C_{dg} and C_{ds} as x_d.

3.4 MULTI-BIAS DC AND AC MODELING OPTIMIZATION

Assume that the DC and AC measurements are S^k_{DC} and $S^k_{\mathrm{AC}}(\omega_n)$, respectively, where ω_n, $n = 1,2,\ldots,N$, is a set of frequency points. Correspondingly, we assume $F^k_{\mathrm{DC}}(\phi)$ and $F^k_{\mathrm{AC}}(\phi,\omega_n)$ as the DC and AC model responses, respectively. Notice, as we discussed in the previous section, that a variable from an unconstrained bias-dependent element affects model responses only at the particular bias point where the element is defined.

The error functions corresponding to the DC model responses can be expressed as

$$e^k_{\mathrm{DC}j}(\phi) = w^k_{\mathrm{DC}j}\left[F^k_{\mathrm{DC}j}(\phi) - S^k_{\mathrm{DC}j}\right], \qquad (3.8)$$
$$j = 1,2,\ldots,M^k_{\mathrm{DC}};\ k \in K_{\mathrm{DC}}$$

where $w^k_{\mathrm{DC}j}$ is the weighting factor, M^k_{DC} is the number of DC measurements taken at the kth bias point, and K_{DC} is the set of bias points at which DC measurements are taken. The error functions corresponding to the AC model responses can be expressed as

$$e^k_{\mathrm{AC}j}(\phi,\omega_n) = w^k_{\mathrm{AC}j}\left[F^k_{\mathrm{AC}j}(\phi,\omega_n) - S^k_{\mathrm{AC}j}(\omega_n)\right], \qquad (3.9)$$
$$j = 1,2,\ldots,M^k_{\mathrm{AC}};\ n = 1,2,\ldots,N;\ k \in K_{\mathrm{AC}}$$

where $w^k_{\mathrm{AC}j}$ is the weighting factor, M^k_{AC} is the number of AC measurements taken at the kth bias point, and K_{AC} is the set of bias points at which AC measurements are taken.

If we use K to indicate the set of all bias points, then

$$K = K_{\mathrm{DC}} \cup K_{\mathrm{AC}} = \{1,2,\ldots,K_{\mathrm{bias}}\}. \qquad (3.10)$$

Usually M_{DC} could be the same for different k, $k \in K_{\mathrm{DC}}$, such as the number of DC current responses at different bias conditions. Similarly M^k_{AC} could be the same for different k, $k \in K_{\mathrm{AC}}$, such as the number of S parameter responses.

The integrated DC and small-signal parameter extraction optimization can be formulated as

$$\min_{\phi} \left(\sum_{k \in K_{\mathrm{DC}}} \sum_{j=1}^{M_{\mathrm{DC}}^k} \left| e_{\mathrm{DC}j}^k(\phi) \right|^p + \sum_{k \in K_{\mathrm{AC}}} \sum_{j=1}^{M_{\mathrm{AC}}^k} \sum_{n=1}^{N} \left| e_{\mathrm{AC}j}^k(\phi, \omega_n) \right|^p \right) \tag{3.11}$$

where the optimization variable is ϕ, and $p = 1$ or 2 corresponds to ℓ_1 or ℓ_2 optimization, respectively. The selection of ℓ_1 or ℓ_2 optimization depends on different application situations.

In order to calculate the model responses, we first solve the nonlinear DC circuit of the model using x_a, x_c^k, and α for $k \in K$, so that $F_{\mathrm{DC}}^k(\phi)$, if $k \in K_{\mathrm{DC}}$, can be determined. If $k \in K_{\mathrm{AC}}$, $x_c(\alpha, V^k)$ and $x_f(\alpha, \beta, V^k)$ are calculated with V^k obtained from the DC solution. Then $F_{\mathrm{AC}}^k(\phi, \omega_n)$, $n = 1, 2, \ldots, N$, can be determined.

3.5 GRADIENT COMPUTATION

The calculation of the derivatives of the error functions required by the optimization can be obtained by the perturbation method. However, since the equivalent circuit of the device model is usually not very complicated, it is both feasible and efficient to get them analytically by adjoint analyses. For the gradient of the objective function (3.11), we need to find the gradient of the model responses in (3.8) and (3.9).

3.5.1 Gradient for DC Response

For $j \in M_{\mathrm{DC}}^k$ and $k \in K_{\mathrm{DC}}$, $F_{\mathrm{DC}j}^k$ is a function of x_a, x_c^k, and α. Applying the nonlinear DC adjoint analysis [24], we can analytically calculate the derivative of a DC response with respect to a variable which affects the DC equivalent circuit.

Assume V^k is the state variable vector of the DC circuit at the kth bias point. Without loss of generality, we further assume that V^k is the nodal voltage vector of the DC circuit at the kth bias point. All the DC responses at this bias point are linear combinations

of V^k and independent external excitations. Therefore, it is sufficient to know the derivative of V^k with respect to (or simply, w.r.t.) a variable.

Let the nonlinear nodal equation be

$$f(V^k) = 0. \tag{3.12}$$

A nonlinear equation solving technique can be employed to obtain V^k, for example, the Newton-Raphson approach. From the classification of the parameters of the model, we know that f is a function of x_a, x_c^k, and α, $k \in K_{\mathrm{DC}}$.

To derive the derivative of V^k w.r.t. $\phi_i \in \{x_a, x_c^k, \alpha\}$, we express f as

$$f(\phi, V^k) = 0 \tag{3.13}$$

From Equation (3.13),

$$\left(\frac{\partial f^T}{\partial V^k}\right)^T \frac{\partial V^k}{\partial \phi_i} + \frac{\partial f}{\partial \phi_i} = 0$$

or we can write

$$\frac{\partial V^k}{\partial \phi_i} = -\left(\frac{\partial f^T}{\partial V^k}\right)^{-T} \frac{\partial f}{\partial \phi_i}.$$

Let V_n^k be the nth component of V^k, and u_n be a unity vector with 1 in the nth row. Then

$$\begin{aligned} \frac{\partial V_n^k}{\partial \phi_i} &= u_n^T \frac{\partial V^k}{\partial \phi_i} \\ &= -u_n^T \left(\frac{\partial f^T}{\partial V^k}\right)^{-T} \frac{\partial f}{\partial \phi_i} \\ &= -\left(\hat{V}_n^k\right)^T \frac{\partial f}{\partial \phi_i} \end{aligned} \tag{3.14}$$

where $\hat{V}_n^k$ is the solution of the adjoint system

$$\left(\frac{\partial f^T}{\partial V^k}\right) \hat{V}_n^k = u_n \tag{3.15}$$

and $\partial f / \partial \phi_i$ can be calculated either analytically or by perturbation.

3.5.2 Gradient for AC Responses

For $j \in M_{\mathrm{AC}}^k$ and $k \in K_{\mathrm{AC}}$, we know that the AC small-signal equivalent circuit is linear and the AC response $F_{\mathrm{AC}j}^k$ is a function of $\boldsymbol{x}_a$, $\boldsymbol{x}_b$, $\boldsymbol{x}_c^k$, $\boldsymbol{x}_d^k$, $\boldsymbol{x}_e^k$ and $\boldsymbol{x}_f^k$, where $\boldsymbol{x}_e^k = \boldsymbol{x}_e(\boldsymbol{\alpha}, V^k)$, $\boldsymbol{x}_f^k = \boldsymbol{x}_f(\boldsymbol{\alpha}, \boldsymbol{\beta}, V^k)$, and V^k is determined from the solution of the DC equivalent circuit corresponding to the kth bias point. Symbolically, we can express the AC small-signal response as

$$F_{\mathrm{AC}j}^k = f_j\left(\boldsymbol{x}_a, \boldsymbol{x}_b, \boldsymbol{x}_c^k, \boldsymbol{x}_d^k, \boldsymbol{x}_e(\boldsymbol{\alpha}, V^k), \boldsymbol{x}_f(\boldsymbol{\alpha}, \boldsymbol{\beta}, V^k)\right), \quad k \in K_{\mathrm{AC}}. \tag{3.16}$$

Therefore, we can use the chain rule to obtain the required derivatives:

$$\begin{aligned}
\frac{\partial F_{\mathrm{AC}j}^k}{\partial \phi_i} &= \frac{\partial f_j}{\partial \phi_i} + \frac{\partial V^{kT}}{\partial \phi_i}\frac{\partial \boldsymbol{x}_e^{kT}}{\partial V^k}\frac{\partial f_j}{\partial \boldsymbol{x}_e^k} + \frac{\partial V^{kT}}{\partial \phi_i}\frac{\partial \boldsymbol{x}_f^{kT}}{\partial V^k}\frac{\partial f_j}{\partial \boldsymbol{x}_f^k}, && \text{for } \phi_i \in \{\boldsymbol{x}_a, \boldsymbol{x}_c^k\} \\
\frac{\partial F_{\mathrm{AC}j}^k}{\partial \phi_i} &= \frac{\partial f_j}{\partial \phi_i}, && \text{for } \phi_i \in \{\boldsymbol{x}_b, \boldsymbol{x}_d^k\} \\
\frac{\partial F_{\mathrm{AC}j}^k}{\partial \phi_i} &= \frac{\partial \boldsymbol{x}_e^{kT}}{\partial \phi_i}\frac{\partial f_j}{\partial \boldsymbol{x}_e^k} + \frac{\partial V^{kT}}{\partial \phi_i}\frac{\partial \boldsymbol{x}_e^{kT}}{\partial V^k}\frac{\partial f_j}{\partial \boldsymbol{x}_e^k} \\
&\quad + \frac{\partial \boldsymbol{x}_f^{kT}}{\partial \phi_i}\frac{\partial f_j}{\partial \boldsymbol{x}_f^k} + \frac{\partial V^{kT}}{\partial \phi_i}\frac{\partial \boldsymbol{x}_f^{kT}}{\partial V^k}\frac{\partial f_j}{\partial \boldsymbol{x}_f^k}, && \text{for } \phi_i \in \boldsymbol{\alpha} \\
\frac{\partial F_{\mathrm{AC}j}^k}{\partial \phi_i} &= \frac{\partial \boldsymbol{x}_f^{kT}}{\partial \phi_i}\frac{\partial f_j}{\partial \boldsymbol{x}_f^k}, && \text{for } \phi_i \in \boldsymbol{\beta}
\end{aligned}$$

The derivative of f_j w.r.t. $\boldsymbol{x}_a$, $\boldsymbol{x}_b$, $\boldsymbol{x}_c^k$, $\boldsymbol{x}_d^k$, $\boldsymbol{x}_e$, and $\boldsymbol{x}_f$ for $k \in K_{\mathrm{AC}}$ on the right-hand side of the foregoing equations can be obtained by standard AC adjoint analysis, whereas the derivative of V^k with respect to $\boldsymbol{x}_a$, $\boldsymbol{x}_c^k$, and $\boldsymbol{\alpha}$ for $k \in K_{\mathrm{AC}}$ can be obtained by nonlinear DC adjoint analysis as described in Section 3.5.1.

3.6 PROGRAM STRUCTURE FOR INTEGRATED PARAMETER EXTRACTION

Without loss of generality, we select the DC response of the modeling circuit to be the drain and/or gate bias currents, and the AC response of the modeling circuit to

be S parameters. The program structure of a single iteration for parameter extraction optimization follows the natural sequence of the simulation, as listed in the steps below.

Step 0: Initialization

From available measurement data, determine M_{DC}^k, M_{AC}^k, K_{DC} and K_{AC}. $K = K_{\mathrm{DC}} \cup K_{\mathrm{AC}}$. Determine the initial value of ϕ. Set $K_{\mathtt{tmp}} = \emptyset$.

This step is only executed at the beginning of the iteration loop.

OPTIMIZATION LOOP (Step 1 — Step 6)

Step 1: DC simulation

For $k \in K$, find V^k by solving the nonlinear DC nodal equation (3.13). At the solution, $\hat{V}_n^k$ in (3.15) can be obtained, since the Jacobian matrix is available. Therefore, the gradient of V_n^k with respect to ϕ can be obtained, where $\partial f / \partial \phi_i$ in (3.14) can be computed either analytically or by perturbation.

Step 2: DC error function and gradient calculations

If $k \in K_{\mathrm{DC}}$, form the DC error functions and the corresponding derivatives according to Equation (3.8).

If $k \notin K_{\mathrm{AC}}$, go to *Step 5*.

Comment: The DC responses of the model are linear functions of the nodal voltages and bias sources. By the chain rule, the gradient of a DC response w.r.t. a variable can be easily calculated from the derivatives of the nodal voltages w.r.t. the variable.

Step 3: AC simulation

First, compute x_c^k from α and V^k, and compute x_f^k from α, β and V^k.

From the small-signal equivalent circuit, form the admittance matrix Y, transform it to an impedance matrix Z. Then transform Z to the S parameter matrix [30]. The

derivatives of individual S parameters w.r.t. small-signal equivalent circuit elements are calculated from linear AC adjoint analysis.

Step 4: AC error function and gradient calculations

The AC error functions can be easily formed from the computed S parameters according to (3.9).

The gradient calculation of AC error functions w.r.t. a variable is obtained from the derivatives of S parameters w.r.t. the variable. Derivative computation equations in Section 3.5.2 can be used, where $\partial f_j/\partial \phi_i$ for $\phi_i \in \{x_a, x_b, x_c^k, x_d^k\}$, $\partial f_j/\partial x_e^k$ and $\partial f_j/\partial x_f^k$ are obtained from *Step 3*, $\partial V^{kT}/\partial \phi_i$ for $\phi_i \in \{x_a, x_c^k, \alpha\}$ is obtained from *Step 1*. $\partial x_e^{kT}/\partial V^k$, $\partial x_e^{kT}/\partial \alpha$, $\partial x_f^{kT}/\partial V^k$, $\partial x_f^{kT}/\partial \alpha$ and $\partial x_f^{kT}/\partial \beta$ can be calculated either analytically or by perturbation.

Step 5: Error function calculation control

$K_{\texttt{tmp}} = K_{\texttt{tmp}} \cup \{k\}$. If $K_{\texttt{tmp}} \neq K$, go to *Step 1*. Otherwise, set $K_{\texttt{tmp}} = \emptyset$.

Step 6: Optimization iteration check

If the objective function value computed from (3.11) is higher than the specified tolerance, update the variables and go to *Step 1*.

Otherwise, stop.

3.7 EXAMPLES

In this section, we show examples of FET model parameter extraction using the approach presented in the previous sections. The Materka and Kacprzak nonlinear FET model [48,49] and the Curtice nonlinear FET model [27] are considered. The computer program used for these examples is *HarPE* [36], a nonlinear CAD program which contains this

integrated DC and small-signal parameter extraction technique. (The capability of large-signal parameter extraction of *HarPE* will be discussed in Chapter 5.) An HP 9000/300 workstation and a Sun Sparcstation 1 are used for the computations.

3.7.1 Case 1 — Materka and Kacprzak Model

Consider the Materka and Kacprzak model discussed in Section 3.3.2. The nonlinear FET equivalent circuit model and the corresponding small-signal equivalent circuit are shown in Figure 3.3(a) and (b), respectively. The total number of parameters characterizing the Materka and Kacprzak model including intrinsic and extrinsic parameters, from Table 3.2, is 30.

We use the DC drain current and S parameter data measured at three bias points from Ratheyon Company [56], used by Bandler *et al.* [9] as the measurement data, (see Table 3.3 for detailed descriptions). The error functions are defined according to (3.8) and (3.9). Here $K_{\rm DC} = K_{\rm AC} = \{1, 2, 3\}$ for three different bias points; $M^k_{\rm DC} = 1$ corresponding to the DC measurement on the drain current; $M^k_{\rm AC} = 8$ representing the real and imaginary parts of the S parameters; we choose $N = 9$ representing 9 frequency points from 2 to 18GHz, 2GHz apart. The weighting factors $w^k_{{\rm DC}j}$ and $w^k_{{\rm AC}j}$ are properly chosen to balance the DC and AC error functions. The total number of nonlinear error functions for this example is 219. $p = 1$ is chosen for ℓ_1 optimization.

Under normal small-signal operating conditions, the effects of i_{gs} and i_{dg} on model responses are negligible, because, as we can see from Figure 3.3(a), i_{gs} and i_{dg} are used to simulate the FET forward biasing and breakdown conditions, respectively. In other words, to characterize i_{gs} and i_{dg}, we need special measurement data. Therefore, due to the measurement data we have, we select approximate values for $I_{G0} = 0.5 \times 10^{-10}$A, $\alpha_G = 20{\rm V}^{-1}$, $I_{B0} = 0.5 \times 10^{-10}$A, $\alpha_B = 1{\rm V}^{-1}$, $V_{BC} = 20$V, and treat them as constants during the parameter extraction optimization.

Table 3.3:

MEASUREMENT DATA SET

Bias	DC drain current	Small-signal S parameters 2, 3, ..., 18GHz
$V_{GB} = 0.0$V, $V_{DB} = 4$V	0.177A	$S_{11}, S_{21}, S_{12}, S_{22}$
$V_{GB} = -1.74$V, $V_{DB} = 4$V	0.092A	$S_{11}, S_{21}, S_{12}, S_{22}$
$V_{GB} = -3.10$V, $V_{DB} = 4$V	0.037A	$S_{11}, S_{21}, S_{12}, S_{22}$

On the other hand, we also fix the linear capacitance C_x to be 2pF during the optimization, for the main purpose of using C_x is to provide compensation for the output conductance between DC and AC conditions.

The total number of variables, therefore, becomes 24.

The initial values and the values at the optimization solution are listed in Table 3.4. The DC model response at the solution is shown in Figure 3.4 and the small-signal S parameter responses at the three bias points are show in Figures 3.5, 3.6 and 3.7, respectively. Excellent matches of model responses to the measurement data can be observed.

To check whether we should consider I_{G0}, α_G, I_{B0}, α_B and V_{BC} as variables, we attempted further optimization which included those variables. As expected, it did not improve the match between the model responses and the measurements.

The circuit files at the starting point and final solution in *HarPE* accepted form are provided in Appendix A.1.1, where the related measurement data files are also provided.

To test the robustness of the parameter extraction approach, we randomly perturbed the starting point between 10 to 100 percent and restarted the optimization. In five such starting points, most of the parameters converged to the same solution with less than 6

Table 3.4:

PARAMETER VALUES OF THE FET MODEL

Parameter	Unit	Start	Solution
R_g	Ω	0.2	0.0010
L_g	nH	0.1	0.1267
R_d	Ω	0.7	0.3332
L_d	nH	0.04	0.0630
R_s	Ω	0.8	0.3833
L_s	nH	0.015	0.0118
G_{de}	1/Ω	0.001	0.0003
C_{ds}	pF	0.3	0.1920
I_{DSS}	A	0.19	0.1636
V_{P0}	V	−4.0	−3.7257
γ	-	−0.3	−0.1812
E	-	1.2	1.4130
K_E	1/V	0.02	0.0493
S_1	1/Ω	0.35	0.4172
K_G	1/V	−0.2	−0.1255
τ	pS	3.0	3.6715
S_S	1/Ω	0.004	0.0044
R_{10}	Ω	5.0	4.2415
K_R	1/V	0.05	0.0074
C_{10}	pF	0.4	0.5965
K_1	1/V	0.4	0.7325
C_{1S}	pF	0.01	0.0009
C_{F0}	pF	0.03	0.0225
K_F	1/V	−0.05	−0.1275

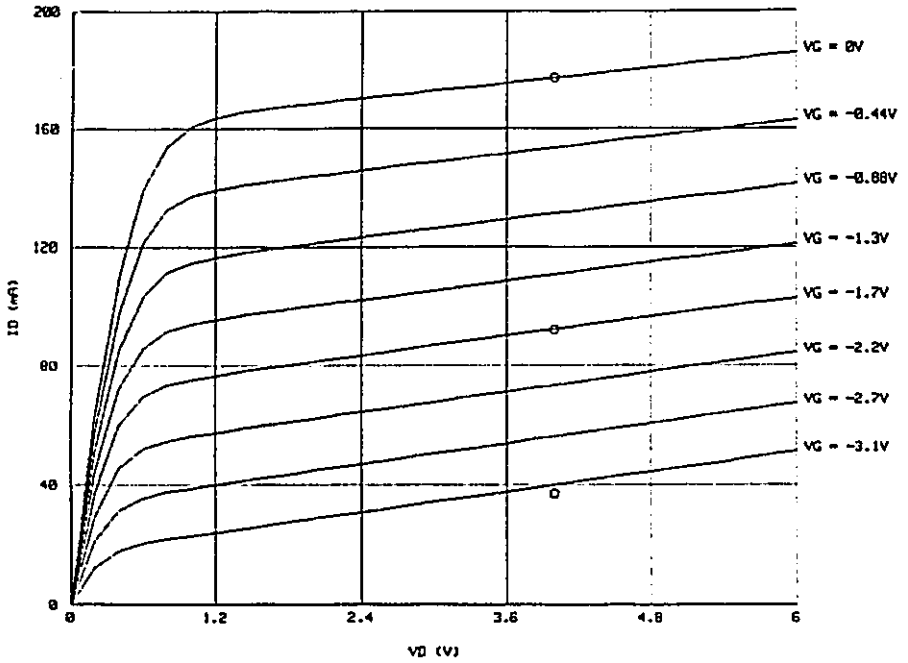


Figure 3.4: DC I–V curve after parameter extraction.

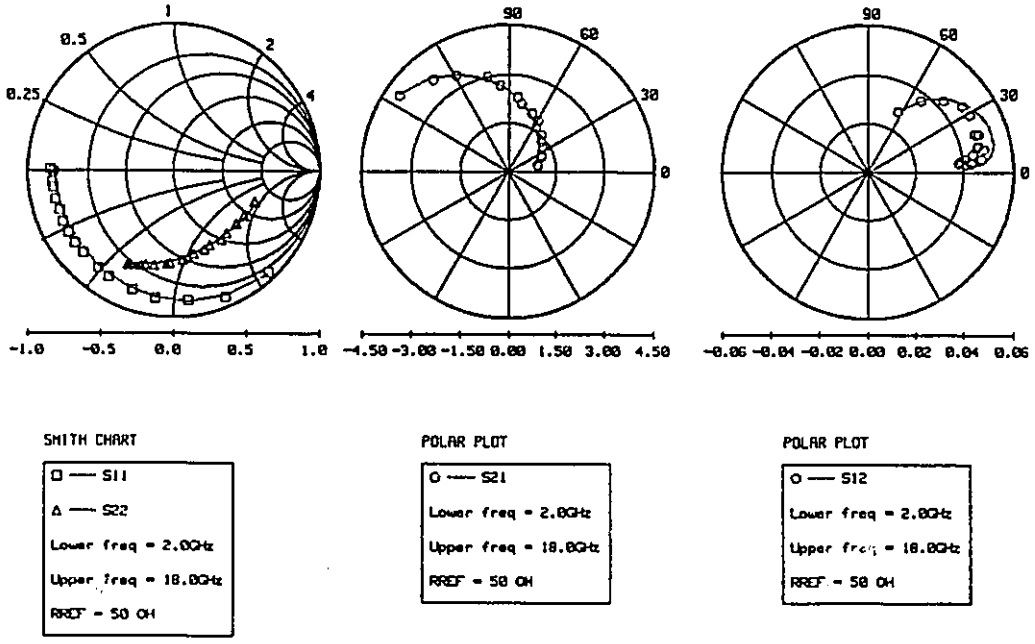


Figure 3.5: S parameters from 2GHz to 18GHz at bias $V_{GB} = 0.0$ and $V_{DB} = 4$V.

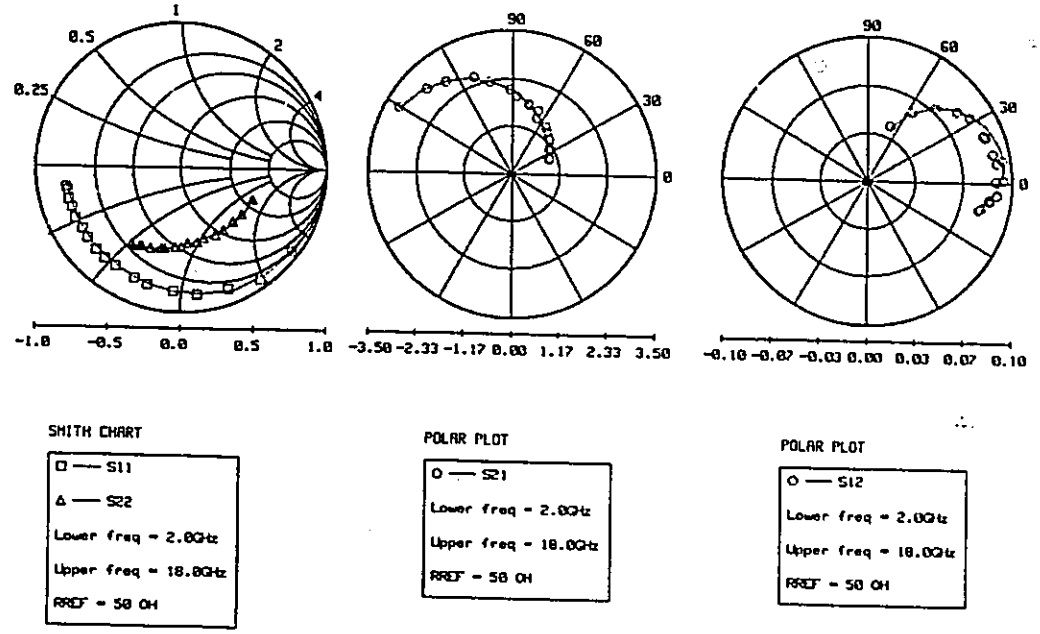


Figure 3.6: S parameters from 2GHz to 18GHz at bias $V_{GB} = -1.74$ and $V_{DB} = 4$V.

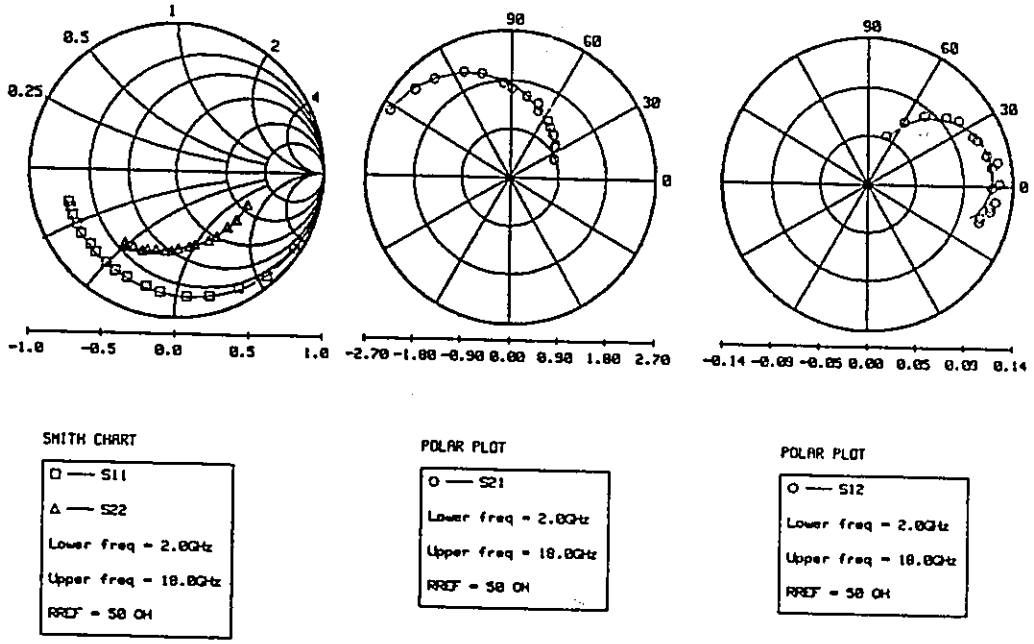


Figure 3.7: S parameters from 2GHz to 18GHz at bias $V_{GB} = -3.10$ and $V_{DB} = 4$V.

percent relative errors. Large errors were observed at R_d, G_{ds}, S_1, K_G, K_R and C_{1S}. Due to the very small absolute values of G_{ds}, K_R and C_{1S}, their effects on their corresponding elements are negligible.

Sensitivity analyses of the model responses w.r.t. the parameters were carried out. The results show that those parameters have relatively low sensitivities to the model responses, which means that they are more difficult to identify.

Mathematically, we can see from the nonlinear expression of i_{ds} that S_1 and K_G are used for providing a correct saturation point. Since the bias points we used for this example were taken from the well saturated region, the indeterminacy of S_1 and K_G are expected. This phenomenon was proved by examining the DC I–V curves at the solutions reached from those different starting points: there are quite obvious differences in the linear regions of the I–V curves, although the slopes and relative intervals of the I–V curves are very close at the bias points where measurements are available.

A numerical verification was performed to show the identifiability of S_1 and K_G. Additional DC drain currents at $V_{DB} = 0.333, 0.667, 1.0$ and 1.333V for $V_{GB} = 0.0, -1.74$ and -3.1V, respectively, from a DC simulation were used as simulated measurements in addition to the measurements listed in Table 3.3. The simulated DC measurement data is listed in Table 3.5. The same starting points obtained from the perturbation were optimized to match the augmented measurement. All five points converged to a single solution with relative parameter variance less than 2 percent, except for 8.2 percent for K_E and large errors for K_R and C_{1S}. Appendix A.1.2 lists the extended circuit and data files.

However, it should be pointed out that the Materka and Kacprzak model we have used here is modified by *Microwave Harmonica* [49]. It has more parameters than the original one [48]. On one hand, it requires more measurements to uniquely identify all its parameters than its original form; but on the other hand, it possesses more flexibility to fit actual devices.

Table 3.5:

EXTRA DC MEASUREMENT DATA FOR CASE 1

	Drain Current (A)		
V_{DB}(V)	$V_{GB} = 0.0$V	$V_{GB} = -1.74$V	$V_{GB} = -3.1$V
0.333	0.095	0.0536	0.0164
0.667	0.145	0.0708	0.0205
1.000	0.160	0.0749	0.0226
1.333	0.164	0.0771	0.0245

3.7.2 Case 2 — Curtice Model

In this example we demonstrate the parameter extraction approach for another popular nonlinear FET model, the Curtice model [27]. The equivalent circuit model is shown in Figure 3.8, where the intrinsic nonlinear elements are characterized as, [36]

$$i_{ds} = (A_0 + A_1 v_1 + A_2 v_1^2 + A_3 v_1^3)\tanh(\gamma v_d)$$

$$v_1 = v_g(t-\tau)\,(1+\beta(V_{DS0} - v_d(t))$$

$$i_{gs} = \begin{cases} I_S \exp\left(\frac{v_g}{N v_t} - 1\right) + G_{MIN} v_g & \text{for } v_g \geq -5N v_t \\ -I_S + G_{MIN} v_g & \text{for } -V_{BR} + 50v_t < v_g < -5N v_t \\ -I_S\left[\exp\left(-\frac{v_g + V_{BR}}{v_t}\right) + 1\right] + G_{MIN} v_g & \text{for } v_g \leq -V_{BR} + 50v_t \end{cases}$$

$$i_{gd} = \begin{cases} I_S \exp\left(\frac{v_{gd}}{N v_t} - 1\right) + G_{MIN} v_{gd} & \text{for } v_{gd} \geq -5N v_t \\ -I_S + G_{MIN} v_{gd} & \text{for } -V_{BR} + 50v_t < v_{gd} < -5N v_t \\ -I_S\left[\exp\left(-\frac{v_{gd} + V_{BR}}{v_t}\right) + 1\right] + G_{MIN} v_{gd} & \text{for } v_{gd} \leq -V_{BR} + 50v_t \end{cases}$$

$$v_t = \kappa \cdot T_0/q$$

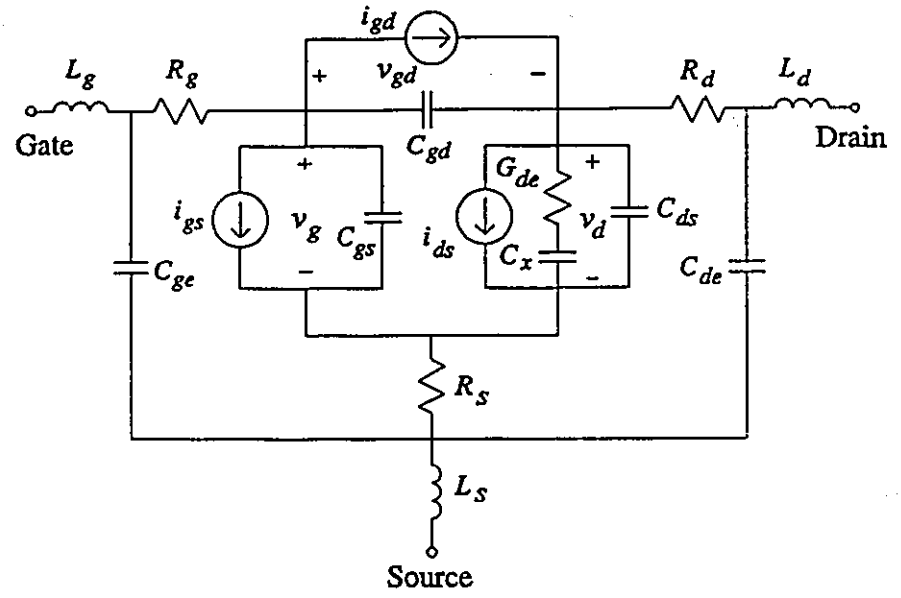


Figure 3.8: The Curtice and Ettenberg nonlinear FET model.

$$C_{gs} = \begin{cases} C_{GS0}\left(1-\frac{v_g}{V_{BI}}\right)^{-0.5} & \text{for } v_g < F_C V_{BI} \\ C_{GS0}(1-F_C)^{-0.5}\left(1+\frac{v_g - F_C V_{BI}}{2V_{BI}(1-F_C)}\right) & \text{for } v_g \geq F_C V_{BI} \end{cases}$$

$$C_{gd} = \begin{cases} C_{GD0}\left(1-\frac{v_{gd}}{V_{BI}}\right)^{-0.5} & \text{for } v_{gd} < F_C V_{BI} \\ C_{GD0}(1-F_C)^{-0.5}\left(1+\frac{v_{gd} - F_C V_{BI}}{2V_{BI}(1-F_C)}\right) & \text{for } v_{gd} \geq F_C V_{BI} \end{cases}$$

where $v_t \approx 0.026$V is the thermal voltage, ($\kappa = 1.38 \times 10^{-23}$ is the Boltzmann's constant, T_0 is the absolute temperature, and $q = 1.6 \times 10^{-19}$C is the electron charge), A_0, A_1, A_2, A_3, β, γ, τ, V_{DS0}, I_S, N, G_{MIN}, V_{BR}, C_{GS0}, V_{BI}, F_C, as well as C_{GD0} are model parameters.

The linear circuit elements are R_g, R_d, R_s, L_g, L_d, L_s, G_{de}, C_x, C_{ds}, C_{ge} and C_{de}.

We apply measurement data provided by Texas Instruments [69]. DC drain current and small-signal S parameter measurements from 1GHz to 15GHz at three bias points are

available, where the bias points are

$$(V_{GB} = -0.361\text{V}, V_{DB} = 2\text{V}),$$
$$(V_{GB} = -0.667\text{V}, V_{DB} = 4\text{V}),$$
$$(V_{GB} = -1.062\text{V}, V_{DB} = 6\text{V}).$$

We used the DC drain current and S parameter measurements from 1GHz to 15GHz with 2GHz apart at the three bias points, respectively, for the parameter extraction. ℓ_2 optimization is applied. See Appendix A.1.3 for circuit and data files.

Because of the very small sensitivities of the parameters I_S, G_{MIN} and V_{BR} to the model responses, we fix them at certain values during the parameter extraction, i.e., $I_S = 1.0 \times 10^{-14}$A, $G_{MIN} = 1.0 \times 10^{-7}$ $1/\Omega$ and $V_{BR} = 30$V.

Table 3.6 illustrates the starting point and the solution of the parameter extraction optimization. The DC I–V curves are shown in Figure 3.9, and the S parameter fits at all three bias points are depicted in Figures 3.10, 3.11 and 3.12, respectively. The fits of the model responses to the device measurements are very good.

This example demonstrates that in case of empirical device modeling we can choose different equivalent circuit models. One particular model may suit some devices but may not suit others. In practice, experiments should be carried and the optimum model should be selected for the particular device.

3.7.3 Selection of Starting Point for Optimization

The integrated parameter extraction optimization presented in this chapter is a nonlinear optimization problem. Usually, we expect to reach a local solution instead of a global minimum. Therefore choosing a good starting point is crucial for finding a good solution.

Table 3.6:

PARAMETER VALUES FOR CASE 2

Parameter	Unit	Start	Solution
R_g	Ω	4.0	5.7407
L_g	nH	0.3	0.3525
R_d	Ω	0.5	0.0100
L_d	nH	0.2	0.3062
R_s	Ω	2.0	3.6041
L_s	nH	0.08	0.0774
G_{de}	$1/\Omega$	0.0002	0.0022
C_x	pF	1.5	1.8842
C_{ds}	pF	0.1	0.0977
C_{ge}	pF	0.01	0.0038
C_{de}	pF	0.01	0.0050
A_0	A	0.15	0.0957
A_1	A/V	0.15	0.0969
A_2	A/V^2	−0.02	−0.0101
A_3	A/V^3	−0.02	−0.0251
γ	1/V	1.0	1.0698
β	–	0.03	0.0383
τ	pS	3.0	3.1821
V_{DS0}	V	2.0	1.7816
N	–	1.0	1.0000
C_{GS0}	pF	0.5	0.6144
V_{BI}	V	0.8	0.7991
F_C	–	0.7	0.7000
C_{GD0}	pF	0.092	0.0783

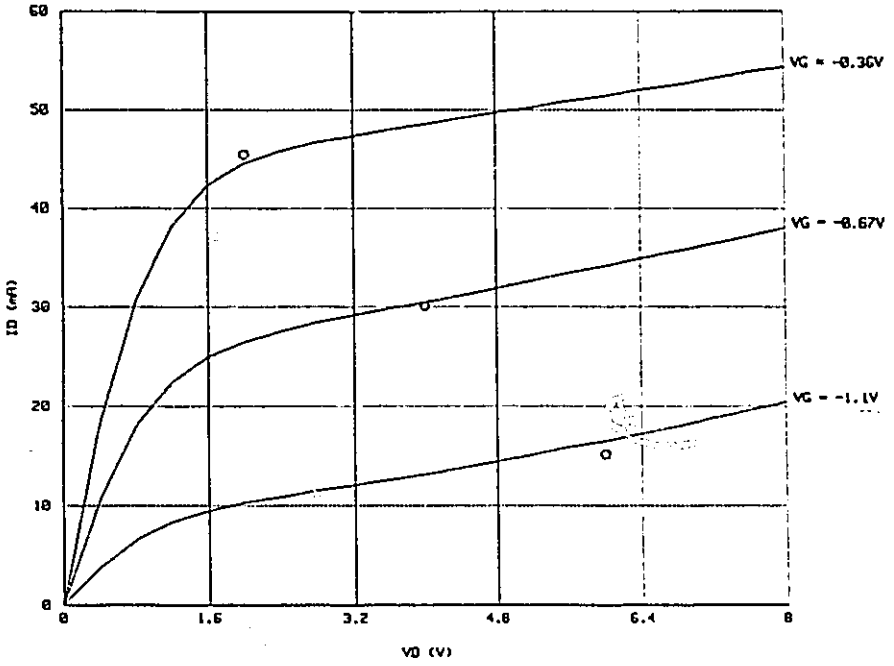


Figure 3.9: DC I–V curve at the solution of Case 2.

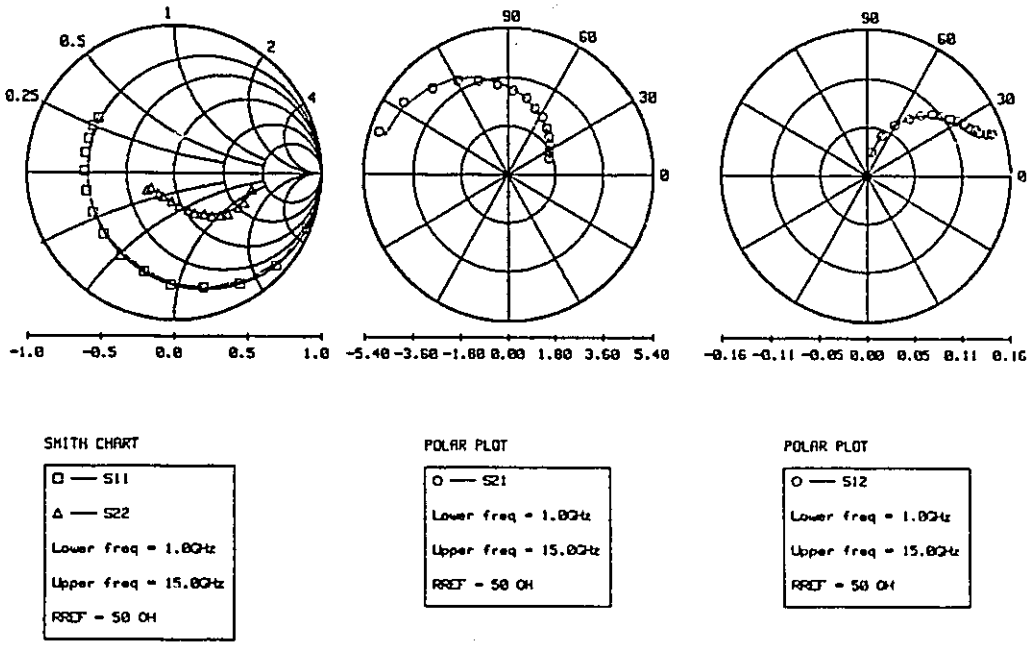


Figure 3.10: S parameter fits at the solution of Case 2 at bias point $V_{GB} = -0.361$V and $V_{DB} = 2$V.

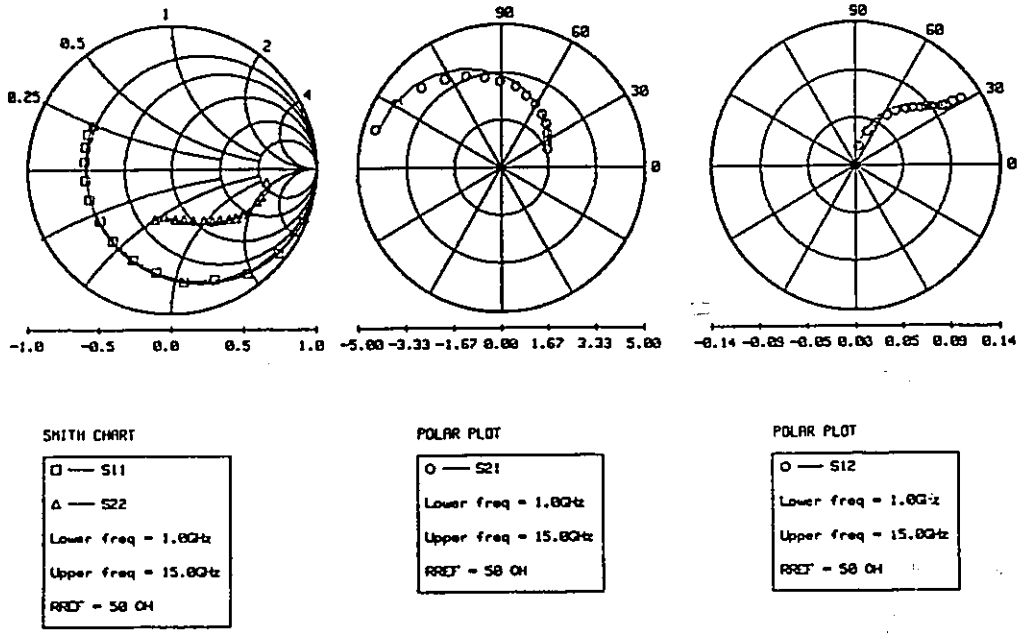


Figure 3.11: S parameter fits at the solution of Case 2 at bias point $V_{GB} = -0.667$V and $V_{DB} = 4$V.

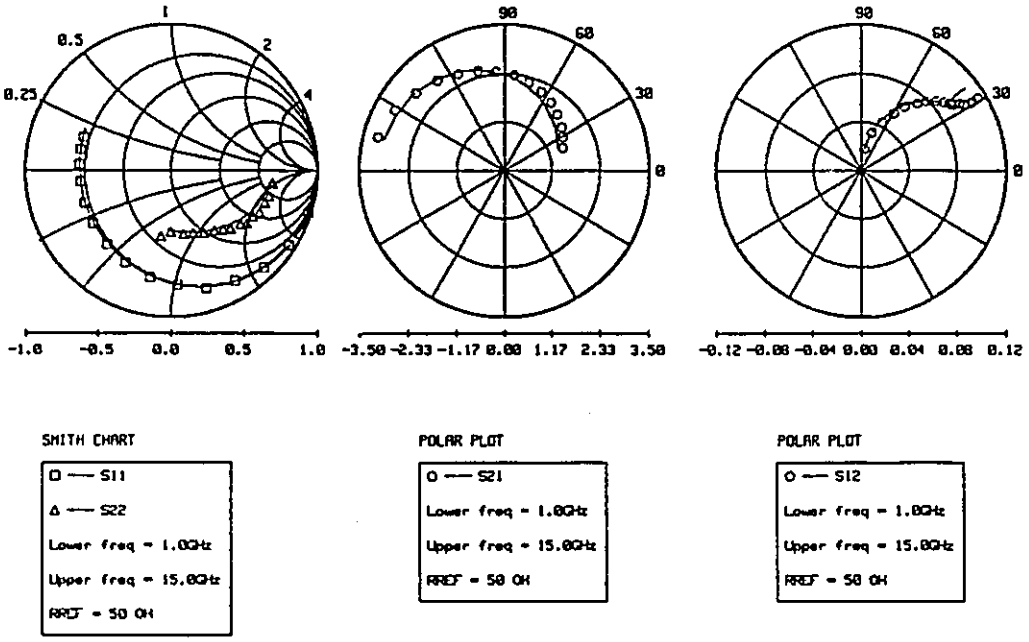


Figure 3.12: S parameter fits at the solution of Case 2 at bias point $V_{GB} = -1.062$V and $V_{DB} = 6$V.

There are several options we have used as guidelines for selecting starting points and optimization strategy.

1. Select extrinsic parameters in their usual value range. The parameters of the nonlinear elements can also be selected from their normal range, for example I_{DSS} in the Materka and Kacprzak model should be close to the saturated current when $v_g = 0$.

2. Perform first DC or AC measurement fit, and then adjust the partial solution as a starting point for the integrated parameter extraction optimization.

3. Perform sensitivity analysis for all the model parameters first. Choose the parameters which have higher sensitivities to the model responses as optimization variables and fix the others at their usual values. (See sequential model building by Bandler *et al.* in [10]).

3.8 CONCLUDING REMARKS

By introducing DC constraints and formulating the modeling process as a complete and integrated optimization problem, i.e., including simultaneously the DC and AC responses, we have improved the uniqueness and reliability of the extracted model parameters. Powerful ℓ_1 and ℓ_2 optimization techniques have been employed. All the required gradient can be provided through efficient adjoint analyses.

Practical FET models have been considered. FET modeling examples using the Materka and Kacprzak model and the Curtice model have been described in detail. They clearly demonstrate the feasibility of the new approach.

It should be noted, however, that when DC characteristics are used as constraints, they should be compatible with the actual device to be modeled; otherwise inappropriate DC constraints could cause large intrinsic discrepancies between the model responses and measurements. On the other hand, a more sophisticated model may meet the requirements

of more devices, but more uncertainties are also introduced which may cause some difficulties in the parameter extraction.

As to the prospects of the approach proposed in this chapter, we can see that

1. Because the model is in a nonlinear form, it can be used directly by the harmonic balance method, an efficient nonlinear frequency domain simulation technique which will be discussed in the next chapter.

2. We can establish a more reliable small-signal model when DC constraints are considered.

3. The approach is applicable to other device modeling problems since the proposed modeling principle is general.

Chapter 4

UTILIZING THE HARMONIC BALANCE TECHNIQUE

4.1 INTRODUCTION

For large-signal nonlinear circuit designs with active FET devices, we need accurate nonlinear large-signal FET device models. A logical way to characterize the nonlinear FET model is to extract model parameters using measurements taken in actual working environment. This means that we need to simulate the model for large-signal operating conditions. Due to the fact that large-signal measurements are practical for powers at different harmonics, an efficient frequency domain nonlinear circuit simulation technique is required.

To calculate the steady-state nonlinear circuit responses, we may use time domain simulation to obtain the time domain response of the model, and then transform it into the frequency domain. This approach is, however, very time consuming, and is not appropriate for frequency domain optimization.

The harmonic balance (HB) technique described by Kundert and Sangiovanni-Vincentelli (1986) [41] has offered an efficient way to simulate a nonlinear circuit in the frequency domain. The approach separates a nonlinear circuit into linear and nonlinear parts according to the nature of the circuit elements. The linear part of the circuit may

be simplified to a multi-terminal circuit and can be simulated efficiently in the frequency domain. The nonlinear part of the circuit, on the other hand, is simulated in the time domain. The connection between the simulations of linear and nonlinear parts of the circuit is through the discrete Fourier transformation. Because of its efficiency in nonlinear circuit simulation, the HB technique has been successfully used in nonlinear circuit optimization, e.g., by Bandler, Zhang, Ye and Chen in 1989 [12].

In this chapter, we give a brief description of the HB simulation method with its formulation, Jacobian matrix, and discrete Fourier transformation. We also introduce a simple approach of constructing the linear multiport matrix for HB simulation by Bandler, Ye and Song [15]. The approach is particularly useful if nonlinear circuit optimization is employed where the linear multiport matrix may need to be updated in every iteration, especially if partial perturbation is employed for gradient calculations.

The application of the HB simulation technique will be discussed in the following chapters.

4.2 NONLINEAR CIRCUIT SIMULATION USING THE HB METHOD

Consider a nonlinear circuit illustrated in Figure 4.1, where L represents the linear part of the circuit and N_i, $i = 1, \ldots, m$, the nonlinear parts of the circuit. Assume that the independent sources are connected to linear elements, and that the nonlinear circuit contains only voltage-controlled nonlinear elements. Also for simplicity, we assume that there are no nonlinear inductors in the circuit. Table 4.1 illustrates the convention of the notation used for HB simulation, which is consistent with the notation used by Kundert and Sangiovanni-Vincentelli [41] and Bandler, Zhang and Biernacki [11].

Table 4.1:

NOTATION AND DEFINITION

Notation	Definition
k, l, ℓ	harmonic indices
H	number of harmonics
t, ω	time, radian frequency
$x, \boldsymbol{x}$	time domain variable and its vector form
$X, \boldsymbol{X}$	frequency domain variable and its complex vector form
$X(k), \boldsymbol{X}(k)$	the kth harmonic component of X and $\boldsymbol{X}$
$\boldsymbol{X}$	$\begin{bmatrix} \boldsymbol{X}(0) \\ \boldsymbol{X}(1) \\ \cdots \\ \boldsymbol{X}(H) \end{bmatrix}$
$\bar{\boldsymbol{X}}$	$\begin{bmatrix} \boldsymbol{X}^R(0) \\ \boldsymbol{X}^R(1) \\ \cdots \\ \boldsymbol{X}^R(H) \\ \boldsymbol{X}^I(0) \\ \boldsymbol{X}^I(1) \\ \cdots \\ \boldsymbol{X}^I(H) \end{bmatrix}$

The index 0 represents the DC component, and the superscripts R and I stand for real and imaginary parts of a complex number, respectively.

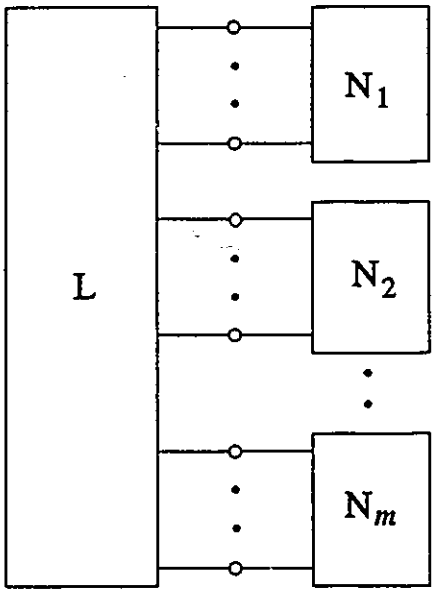


Figure 4.1: Diagram for illustrating circuit simulation using the HB technique.

Following [41] and [11], the HB equation can be expressed as

$$\mathcal{F}(V,k) = I_n(V,k) + j\Omega(k)Q_n(V,k) + Y(k)V(k) + I_s(k) = 0, \qquad (4.1)$$

$$k = 0, 1, \ldots, H$$

where k is the harmonic index representing the kth harmonic, H is the number of harmonics considered in the HB simulation, I_n represents the current from the nonlinear current sources,

$$\Omega(k) = \text{diag}\{\omega_k, \omega_k, \ldots, \omega_k\},$$

Q_n represents the charge from the nonlinear capacitors,

$$V = \left[V^T(0)\ V^T(1)\ \ldots\ V^T(H)\right]^T$$

is the voltage vector to be solved for, Y stands for the multiport admittance matrix of the linear subcircuit, and I_s is the equivalent current excitation from the external excitation sources. $\omega_0 = 0$ corresponds to the DC component in the HB equation.

We can express Equation (4.1) in the compact form

$$\mathcal{F}(V) = I_n(V) + j\Omega Q_n(V) + YV + I_s = 0, \tag{4.2}$$

where

$$\begin{aligned}
I_n(V) &= \left[I_n^T(V,0)\ I_n^T(V,1)\ \ldots\ I_n^T(V,H)\right]^T,\\
Q_n(V) &= \left[Q_n^T(V,0)\ Q_n^T(V,1)\ \ldots\ Q_n^T(V,H)\right]^T,\\
I_s &= \left[I_s^T(0)\ I_s^T(1)\ \ldots\ I_s^T(H)\right]^T,\\
\Omega &= \mathrm{diag}\{\Omega(0),\ \Omega(1),\ \ldots,\ \Omega(H)\},\\
Y &= \mathrm{diag}\{Y(0),\ Y(1),\ \ldots,\ Y(H)\}.
\end{aligned}$$

The Jacobian matrix of (4.2) is

$$\begin{aligned}
J &= \left(\frac{\partial \mathcal{F}^T(V)}{\partial V}\right)^T = \left(\frac{\partial I_n^T(V)}{\partial V}\right)^T + j\Omega\left(\frac{\partial Q_n^T(V)}{\partial V}\right)^T + Y\\
&= \begin{bmatrix}
\frac{\partial I_n^T(V,0)}{\partial V(0)} & \frac{\partial I_n^T(V,1)}{\partial V(0)} & \cdots & \frac{\partial I_n^T(V,H)}{\partial V(0)}\\
\frac{\partial I_n^T(V,0)}{\partial V(1)} & \frac{\partial I_n^T(V,1)}{\partial V(1)} & \cdots & \frac{\partial I_n^T(V,H)}{\partial V(1)}\\
\vdots & \vdots & \ddots & \vdots\\
\frac{\partial I_n^T(V,0)}{\partial V(H)} & \frac{\partial I_n^T(V,1)}{\partial V(H)} & \cdots & \frac{\partial I_n^T(V,H)}{\partial V(H)}
\end{bmatrix}^T\\
&\quad + j\begin{bmatrix}
\Omega(0) & & & \\
& \Omega(1) & & \\
& & \ddots & \\
& & & \Omega(H)
\end{bmatrix}\begin{bmatrix}
\frac{\partial Q_n^T(V,0)}{\partial V(0)} & \frac{\partial Q_n^T(V,1)}{\partial V(0)} & \cdots & \frac{\partial Q_n^T(V,H)}{\partial V(0)}\\
\frac{\partial Q_n^T(V,0)}{\partial V(1)} & \frac{\partial Q_n^T(V,1)}{\partial V(1)} & \cdots & \frac{\partial Q_n^T(V,H)}{\partial V(1)}\\
\vdots & \vdots & \ddots & \vdots\\
\frac{\partial Q_n^T(V,0)}{\partial V(H)} & \frac{\partial Q_n^T(V,1)}{\partial V(H)} & \cdots & \frac{\partial Q_n^T(V,H)}{\partial V(H)}
\end{bmatrix}^T\\
&\quad + \begin{bmatrix}
Y(0) & & & \\
& Y(1) & & \\
& & \ddots & \\
& & & Y(H)
\end{bmatrix}.
\end{aligned} \tag{4.3}$$

In practice, we solve the HB equation (4.2) by reorganizing it into a scalar form:

$$\begin{bmatrix} \mathcal{F}^R(V,0) \\ \mathcal{F}^R(V,1) \\ \vdots \\ \mathcal{F}^R(V,H) \\ \mathcal{F}^I(V,0) \\ \mathcal{F}^I(V,1) \\ \vdots \\ \mathcal{F}^I(V,H) \end{bmatrix} = \begin{bmatrix} I_n^R(V,0) \\ I_n^R(V,1) \\ \vdots \\ I_n^R(V,H) \\ I_n^I(V,0) \\ I_n^I(V,1) \\ \vdots \\ I_n^I(V,H) \end{bmatrix}$$

$$+ \begin{bmatrix} & & & & & -\Omega(0) & & & \\ & & & & & & -\Omega(1) & & \\ & & & & & & & \ddots & \\ & & & & & & & & -\Omega(H) \\ \Omega(0) & & & & & & & & \\ & \Omega(1) & & & & & & & \\ & & \ddots & & & & & & \\ & & & \Omega(H) & & & & & \end{bmatrix} \begin{bmatrix} Q_n^R(V,0) \\ Q_n^R(V,1) \\ \vdots \\ Q_n^R(V,H) \\ Q_n^I(V,0) \\ Q_n^I(V,1) \\ \vdots \\ Q_n^I(V,H) \end{bmatrix}$$

$$+ \begin{bmatrix} \mathbf{Y}^R(0) & & & & -\mathbf{Y}^I(0) & & & \\ & \mathbf{Y}^R(1) & & & & -\mathbf{Y}^I(1) & & \\ & & \ddots & & & & \ddots & \\ & & & \mathbf{Y}^R(H) & & & & -\mathbf{Y}^I(H) \\ \mathbf{Y}_I(0) & & & & \mathbf{Y}^R(0) & & & \\ & \mathbf{Y}^I(1) & & & & \mathbf{Y}^R(1) & & \\ & & \ddots & & & & \ddots & \\ & & & \mathbf{Y}^I(H) & & & & \mathbf{Y}^R(H) \end{bmatrix} \begin{bmatrix} V^R(0) \\ V^R(1) \\ \vdots \\ V^R(H) \\ V^I(0) \\ V^I(1) \\ \vdots \\ V^I(H) \end{bmatrix}$$

$$+ \begin{bmatrix} I_s^R(0) \\ I_s^R(1) \\ \\ I_s^R(H) \\ I_s^I(0) \\ I_s^I(1) \\ \vdots \\ I_s^I(H) \end{bmatrix} = 0 \tag{4.4}$$

or, simply

$$\bar{\mathcal{F}}(\bar{V}) = \bar{I}_n(\bar{V}) + \bar{\Omega}\bar{Q}_n(\bar{V}) + \bar{Y}\bar{V} + \bar{I}_s = 0 \tag{4.5}$$

where the superscripts R and I represent real and imaginary parts of the corresponding complex component, respectively. The corresponding Jacobian matrix can be derived as

$$\bar{J}(\bar{V}) = \left(\frac{\partial \bar{I}_n^T(\bar{V})}{\partial \bar{V}}\right)^T + \bar{\Omega}\left(\frac{\partial \bar{Q}_n^T(\bar{V})}{\partial \bar{V}}\right)^T + \bar{Y}. \tag{4.6}$$

Powell's algorithm for solving nonlinear equations [37,55] can be applied to solve (4.5), where the variable is $\bar{V}$. The algorithm is stable and has a good convergence rate.

4.3 DISCRETE FOURIER TRANSFORMATION FOR HB SIMULATION

In the HB equation (4.2), I_n and Q_n are expressed in the frequency domain. The computations of I_n, Q_n and their derivatives with respect to V, however, need to be in the time domain. The discrete Fourier transformation (DFT) is required to transform relevant quantities between time and frequency domains [41]. In this section, we discuss the discrete Fourier transformation used in solving the HB equation.

Consider first the calculations of $I_n(V,k)$ and $\frac{\partial I_n^T(V,k)}{\partial V(l)}$.

Define

$$a(k) = \begin{cases} 1 & k = 0 \\ 2 & k \neq 0 \end{cases}$$

The calculation of $I_n(V,k)$ can be implemented in the following procedure.

Step 1: Compute $v(t)$ samples from the inverse DFT (IDFT) of V

$$v(t) = \sum_{l=-H}^{H} \frac{1}{a(l)} V(l) e^{jl\omega_1 t}. \tag{4.7}$$

Comment: The relationship between the Fourier series coefficients and the phasors is discussed in the appendix of Maas [47]. $V(-l) = V^*(l)$, since $v(t)$ is a real function, where the asterisk represents complex conjugation.

Step 2: Compute the $i_n(t)$ samples from the $v(t)$ samples.

Comment: $i_n(t)$ can consist of nonlinear functions of $v(t)$.

Step 3: Compute $I_n(V,k)$ from the DFT of the $i_n(t)$ samples

$$I_n(V,k) = \frac{a(k)}{N_T}\sum_{\ell=1}^{N_T} i_n(\ell\Delta T)e^{-jk\omega_1\ell\Delta T} \tag{4.8}$$

where $N_T \geq 2H+1$ is the number of samples in the time domain, $\Delta T = \frac{T}{N_T}$, $T = 2\frac{\pi}{\omega_1}$, and ω_1 is the fundamental frequency.

The calculation of the term $\frac{\partial I_n^T(V,k)}{\partial V(l)}$ can be derived from (4.7) and (4.8) as

$$\begin{aligned}\frac{\partial I_n^T(V,k)}{\partial V(l)} &= \frac{a(k)}{N_T}\sum_{\ell=1}^{N_T}\frac{\partial i_n^T(\ell\Delta T)}{\partial V(l)}e^{-jk\ell\frac{2\pi}{N_T}} \\ &= \frac{a(k)}{N_T}\sum_{\ell=1}^{N_T}\frac{\partial v^T(\ell\Delta T)}{\partial V(l)}\frac{\partial i_n^T(\ell\Delta T)}{\partial v(\ell\Delta T)}e^{-jk\ell\frac{2\pi}{N_T}}.\end{aligned}$$

We know, from (4.7), that

$$\frac{\partial v^T(t)}{\partial V(l)} = \frac{1}{a(l)}e^{jl\omega_1 t}$$

and the time sample form

$$\begin{aligned}\frac{\partial v^T(\ell\Delta T)}{\partial V(l)} &= \frac{1}{a(l)}e^{jl\omega_1\ell\Delta T} \\ &= \frac{1}{a(l)}e^{jl\ell\frac{2\pi}{N_T}}.\end{aligned}$$

Hence, we have

$$\begin{aligned}\frac{\partial I_n^T(V,k)}{\partial V(l)} &= \frac{a(k)}{a(l)}\frac{1}{N_T}\sum_{\ell=1}^{N_T}\frac{\partial i_n^T(\ell\Delta T)}{\partial v(\ell\Delta T)}e^{-jk\ell\frac{2\pi}{N_T}}e^{jl\ell\frac{2\pi}{N_T}} \\ &= \frac{a(k)}{a(l)}\frac{1}{N_T}\sum_{\ell=1}^{N_T}\frac{\partial i_n^T(\ell\Delta T)}{\partial v(\ell\Delta T)}e^{-j(k-l)\ell\frac{2\pi}{N_T}}\end{aligned} \tag{4.9}$$

where $\frac{\partial i_n^T(\ell\Delta T)}{\partial v(\ell\Delta T)}$ can be derived and computed in the time domain.

The calculations of $Q_n(V,k)$ and $\frac{\partial Q_n^T(V,k)}{\partial V(l)}$ can be similarly derived. Let $q_n(t)$ be the time domain charge expression which can consist of nonlinear functions of $v(t)$. $Q_n(V,k)$ can be derived as

$$Q_n(V,k) = \frac{a(k)}{N_T}\sum_{\ell=1}^{N_T} q_n(\ell\Delta T)e^{-jk\ell\frac{2\pi}{N_T}} \tag{4.10}$$

and

$$\frac{\partial Q_n^T(V,k)}{\partial V(l)} = \frac{a(k)}{a(l)}\frac{1}{N_T}\sum_{\ell=1}^{N_T}\frac{\partial q_n^T(\ell\Delta T)}{\partial v(\ell\Delta T)}e^{-j(k-l)\ell\frac{2\pi}{N_T}}. \tag{4.11}$$

Therefore, the entries of the Jacobian matrix (4.3) can be determined.

The calculations of the corresponding scalar forms of the HB equation (4.5) and its Jacobian matrix (4.6) can be similarly obtained. See Kundert and Sangiovanni-Vincentelli for details [41].

4.4 AN EFFICIENT MULTIPORT MATRIX CONSTRUCTION APPROACH

In the HB equation (4.1) we need to construct the admittance matrix $Y(k)$ which corresponds to the linear part of the circuit. We can consider $Y(k)$ as a multiport admittance matrix where a port may have several terminals.

In circuit optimization the values of designable parameters change in every iteration. This in turn updates the circuit in every iteration. An efficient way to set up the multiport circuit matrix corresponding to the linear part of the circuit, or the linear subcircuit, is desirable. Different ways of constructing the matrix are available, e.g., the partial elimination of the internal nodes from the general nodal matrix of the circuit by Chau and Lin [24], etc. An alternative is to use a multiport matrix which takes into account Kirchhoff's current law (KCL) and eliminates one simulation variable for each nonlinear subcircuit or

port, therefore speeding up the simulation [12]. This approach is much simpler than the general approach in [24].

4.4.1 Multiport Matrix

Consider the general circuit in Figure 4.1, where without loss of generality we assume that N_i and N_l, $i \neq l$, $i,l = 1,\ldots,m$, do not have any common node. We use subscripts ij to indicate the jth node connecting N_i to the linear subcircuit L, and $i0$ the relative reference node of N_i. Since the treatnient of external excitation sources is the same as for the individual nonlinear subcircuit, we consider them as if they were from additional nonlinear subcircuits. The same assumptions for the nonlinear subcircuit are also applied to such source subcircuits, and we extend the index m to m_s, where $m_s = m+$ (number of source subcircuits). In the rest of this section, only one harmonic is considered, since the derivations for other harmonics are similar. Therefore, the harmonic index k corresponding to ω_k is omitted to simplify the notation.

Let the internal nodes of L be numbered rj, $j = 1,\ldots,b$. The indefinite nodal equation can be written as

$$Y_{\text{ind}} \begin{bmatrix} V_{10} \\ V_{11} \\ \vdots \\ V_{20} \\ V_{21} \\ \vdots \\ V_{m_s0} \\ V_{m_s1} \\ \vdots \\ V_{r1} \\ \vdots \\ V_{rb} \end{bmatrix} = \begin{bmatrix} I_{10} \\ I_{11} \\ \vdots \\ I_{20} \\ I_{21} \\ \vdots \\ I_{m_s0} \\ I_{m_s1} \\ \vdots \\ 0 \\ \vdots \\ 0 \end{bmatrix}$$

or

$$Y_{\text{ind}} V_{\text{node}} = I_{\text{node}} \tag{4.12}$$

where Y_{ind} is the indefinite nodal matrix.

First, we express Y_{ind} in its column vector form

$$Y_{\text{ind}} = \left[\begin{array}{cccccccccccc} Y_{10} & Y_{11} & \cdots & Y_{20} & Y_{21} & \cdots & Y_{m_s0} & Y_{m_s1} & \cdots & Y_{r1} & \cdots & Y_{rb} \end{array} \right]. \tag{4.13}$$

From Equation (4.12) we can get

$$Y' \begin{bmatrix} V_{10} \\ V_{11} - V_{10} \\ \vdots \\ V_{20} \\ V_{21} - V_{20} \\ \vdots \\ V_{m_s0} \\ V_{m_s1} - V_{m_s0} \\ \vdots \\ V_{r1} \\ \vdots \\ V_{rb} \end{bmatrix} = \begin{bmatrix} I_{10} \\ I_{11} \\ \vdots \\ I_{20} \\ I_{21} \\ \vdots \\ I_{m_s0} \\ I_{m_s1} \\ \vdots \\ 0 \\ \vdots \\ 0 \end{bmatrix}$$

or

$$Y'V' = I' \tag{4.14}$$

where

$$Y' = \left[\begin{array}{cccccccccccc} \sum_j Y_{1j} & Y_{11} & \cdots & \sum_j Y_{2j} & Y_{21} & \cdots & \sum_j Y_{m_sj} & Y_{m_s1} & \cdots & Y_{r1} & \cdots & Y_{rb} \end{array} \right],$$

$\sum_j Y_{ij}$ is the summation over all the columns corresponding to N_i, and $I' = I$.

Secondly we rewrite (4.14) with Y' in its row vector form

$$\begin{bmatrix} Y'_{10} \\ Y'_{11} \\ \vdots \\ Y'_{20} \\ Y'_{21} \\ \vdots \\ Y'_{m_s0} \\ Y'_{m_s1} \\ \vdots \\ Y'_{r1} \\ \vdots \\ Y'_{rb} \end{bmatrix} V' = I'$$

From Kirchhoff's current law (KCL), it is clear that

$$\sum_j I_{ij} = 0 \quad i = 1, 2, \ldots, m_s$$

where the summation is over all the terminals of N_i. Therefore, we can obtain

$$\begin{bmatrix} \sum_j Y'_{10} \\ Y'_{11} \\ \vdots \\ \sum_j Y'_{20} \\ Y'_{21} \\ \vdots \\ \sum_j Y'_{m_s0} \\ Y'_{m_s1} \\ \vdots \\ Y'_{r1} \\ \vdots \\ Y'_{rb} \end{bmatrix} V' = \begin{bmatrix} 0 \\ I_{11} \\ \vdots \\ 0 \\ I_{21} \\ \vdots \\ 0 \\ I_{m_s1} \\ \vdots \\ 0 \\ \vdots \\ 0 \end{bmatrix}$$

or

$$Y''V'' = I'' \tag{4.15}$$

where $\sum_j Y'_{ij}$ is the summation of all the rows corresponding to N_i, $i = 1,2,\ldots,m_s$, and $V'' = V'$.

Then the multiport matrix can be obtained by the following steps.

Step 1: Select a ground node to reduce Y'' to a full rank matrix. If m_s0 is selected to be the ground node, i.e., $V_{m_s0} = 0$, we delete the row and column in Y'' corresponding to m_s0.

Step 2: Similar to the Gauss elimination method, eliminate columns in Y'' corresponding to $i0$, $i = 1,2,\ldots,m_s - 1$, and rj, $j = 1,\ldots,b$, by using diagonal elements corresponding to the columns to be eliminated in Y''.

Step 3: Delete rows and columns in Y'' corresponding to $i0$, $i = 1,2,\ldots,m-1$, and rj, $j = 1,2,\ldots,b$.

The detailed matrix manipulation is explained via an example in the next subsection. The final form of the extended multiport matrix equation reads

$$Y_M \begin{bmatrix} V_{11} - V_{10} \\ V_{12} - V_{10} \\ \vdots \\ V_{21} - V_{20} \\ V_{22} - V_{20} \\ \vdots \\ V_{m_s1} - V_{m_s0} \\ V_{m_s2} - V_{m_s0} \\ \vdots \end{bmatrix} = \begin{bmatrix} I_{11} \\ I_{12} \\ \vdots \\ I_{21} \\ I_{22} \\ \vdots \\ I_{m_s1} \\ I_{m_s2} \\ \vdots \end{bmatrix}. \tag{4.16}$$

where Y_M stands for the extended multiport matrix which includes entries corresponding to external sources.

In order to derive the multiport matrix Y, voltage V and the equivalent excitation I_s required in the HB equation (4.2), we rewrite (4.16) by partitioning the actual multiport

and external excitation part as

$$\begin{bmatrix} Y_{pp} & Y_{pe} \\ Y_{ep} & Y_{ee} \end{bmatrix} \begin{bmatrix} V_p \\ V_e \end{bmatrix} = \begin{bmatrix} I_p \\ I_e \end{bmatrix}. \tag{4.17}$$

where subscripts p and e are used to indicate the actual multiport part and the external source part, respectively.

(1), V_e is the external source vector

If V_e is the external source vector, we can easily obtain

$$\begin{aligned} Y &= Y_{pp}, \\ V &= V_p, \\ I_s &= Y_{pe}V_e. \end{aligned}$$

(2), I_e is the external source vector

If I_e is the external source vector, it is not difficult to derive that

$$\begin{aligned} Y &= Y_{pp} - Y_{pe}Y_{ee}^{-1}Y_{ep}, \\ V &= V_p, \\ I_s &= Y_{pe}Y_{ee}^{-1}I_e. \end{aligned}$$

(3), the external sources have both voltage and current types

We rewrite (4.17) to include both voltage and current excitations

$$\begin{bmatrix} Y_{pp} & Y_{pe_1} & Y_{pe_2} \\ Y_{e_1p} & Y_{e_1e_1} & Y_{e_1e_2} \\ Y_{e_2p} & Y_{e_2e_1} & Y_{e_2e_2} \end{bmatrix} \begin{bmatrix} V_p \\ V_{e_1} \\ V_{e_2} \end{bmatrix} = \begin{bmatrix} I_p \\ I_{e_1} \\ I_{e_2} \end{bmatrix}. \tag{4.18}$$

where we assume V_{e_1} and I_{e_2} are voltage and current sources, respectively.

It can be derived that

$$\begin{aligned} Y &= Y_{pp} - Y_{pc_2} Y_{c_2c_2}^{-1} Y_{c_2p}, \\ V &= V_p, \\ I_s &= \left(Y_{pc_1} - Y_{pc_2} Y_{c_2c_2}^{-1} Y_{c_2c_1} \right) V_{c_1} + Y_{pc_2} Y_{c_2c_2}^{-1} I_{c_2}. \end{aligned}$$

Usually the number of external sources is very small. Therefore the computation of Y_{ee}^{-1} may not be of concern.

On the other hand, to simplify the calculation of circuit responses, we can formulate the multiport matrix by including zero voltage source(s) for current response(s) and/or zero current source(s) for voltage response(s).

4.4.2 An Example

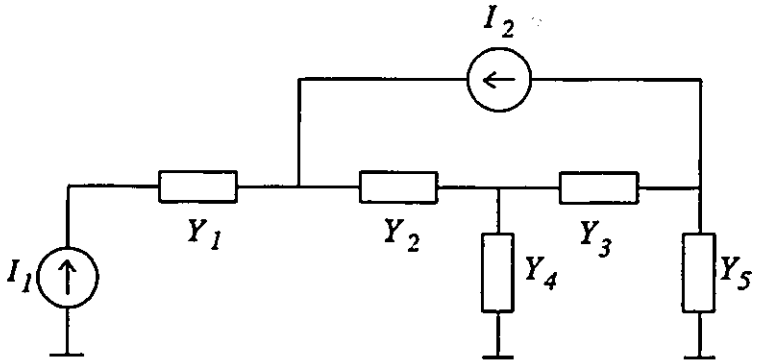
To illustrate the approach for constructing the multiport matrix, let us consider a simple circuit example, which has one current excitation I_1 and one two-terminal nonlinear element I_2, as shown in Figure 4.2.

Step 1: The indefinite nodal matrix of the linear part of the circuit is

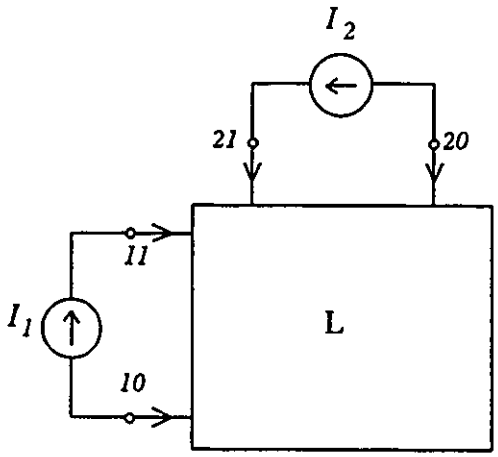
$$Y_{\text{ind}} = \begin{bmatrix} Y_4 + Y_5 & 0 & -Y_5 & 0 & -Y_4 \\ 0 & Y_1 & 0 & -Y_1 & 0 \\ -Y_5 & 0 & Y_3 + Y_5 & 0 & -Y_3 \\ 0 & -Y_1 & 0 & Y_1 + Y_2 & -Y_2 \\ -Y_4 & 0 & -Y_3 & -Y_2 & Y_2 + Y_3 + Y_4 \end{bmatrix}$$

Step 2:

$$Y' = \begin{bmatrix} Y_4 + Y_5 & 0 & -Y_5 & 0 & -Y_4 \\ Y_1 & Y_1 & -Y_1 & -Y_1 & 0 \\ -Y_5 & 0 & Y_3 + Y_5 & 0 & -Y_3 \\ -Y_1 & -Y_1 & Y_1 + Y_2 & Y_1 + Y_2 & -Y_2 \\ -Y_4 & 0 & -Y_2 - Y_3 & -Y_2 & Y_2 + Y_3 + Y_4 \end{bmatrix}$$



(a)



(b)

Figure 4.2: (a) Circuit diagram where I_1 and I_2 correspond to a circuit excitation and a nonlinear element in the circuit, respectively. (b) Diagram after separating the linear and nonlinear parts.

Step 3:

$$Y'' = \begin{bmatrix} Y_1+Y_4+Y_5 & Y_1 & -Y_1-Y_5 & -Y_1 & -Y_4 \\ Y_1 & Y_1 & -Y_1 & -Y_1 & 0 \\ -Y_1-Y_5 & -Y_1 & Y_1+Y_2+Y_3+Y_5 & Y_1+Y_2 & -Y_2-Y_3 \\ -Y_1 & -Y_1 & Y_1+Y_2 & Y_1+Y_2 & -Y_2 \\ -Y_4 & 0 & -Y_2-Y_3 & -Y_2 & Y_2+Y_3+Y_4 \end{bmatrix}$$

Step 4: Select 10 as the ground, therefore delete the row and column corresponding to node 10 from Y'',

$$\begin{bmatrix} Y_1 & -Y_1 & -Y_1 & 0 \\ -Y_1 & Y_1+Y_2+Y_3+Y_5 & Y_1+Y_2 & -Y_2-Y_3 \\ -Y_1 & Y_1+Y_2 & Y_1+Y_2 & -Y_2 \\ 0 & -Y_2-Y_3 & -Y_2 & Y_2+Y_3+Y_4 \end{bmatrix}$$

Step 5: Eliminate the column corresponding to node 20

$$\begin{bmatrix} \frac{Y_1(Y_2+Y_3+Y_5)}{\Delta_1} & 0 & -\frac{Y_1(Y_3+Y_5)}{\Delta_1} & -\frac{Y_1(Y_2+Y_3)}{\Delta_1} \\ -Y_1 & Y_1+Y_2+Y_3+Y_5 & Y_1+Y_2 & -Y_2-Y_3 \\ -\frac{Y_1(Y_3+Y_5)}{\Delta_1} & 0 & \frac{(Y_1+Y_2)(Y_3+Y_5)}{\Delta_1} & \frac{(Y_1Y_3-Y_2Y_5)}{\Delta_1} \\ -\frac{Y_1(Y_2+Y_3)}{\Delta_1} & 0 & \frac{(Y_1Y_3-Y_2Y_5)}{\Delta_1} & \frac{(Y_2+Y_3)(Y_1+Y_5)}{\Delta_1}+Y_4 \end{bmatrix}$$

where $\Delta_1 = Y_1+Y_2+Y_3+Y_5$, and then eliminate the column corresponding to $r1$

$$\begin{bmatrix} y_{11} & 0 & y_{12} & 0 \\ -Y_1 & Y_1+Y_2+Y_3+Y_5 & Y_1+Y_2 & -Y_2-Y_3 \\ y_{21} & 0 & y_{22} & 0 \\ -\frac{Y_1(Y_2+Y_3)}{\Delta_1} & 0 & \frac{(Y_1Y_3-Y_2Y_5)}{\Delta_1} & \frac{(Y_2+Y_3)(Y_1+Y_5)}{\Delta_1}+Y_4 \end{bmatrix}$$

where

$$\begin{aligned} y_{11} &= Y_1(Y_2+Y_3+Y_5)/\Delta_1 - [Y_1(Y_2+Y_3)/\Delta_1]^2/\Delta_2 \\ y_{12} &= -Y_1(Y_3+Y_5)/\Delta_1 + [(Y_1Y_3-Y_2Y_5)/\Delta_1][Y_1(Y_2+Y_3)/\Delta_1]/\Delta_2 \\ y_{21} &= y_{12} \\ y_{22} &= (Y_1+Y_2)(Y_3+Y_5)/\Delta_1 - [(Y_1Y_3-Y_2Y_5)/\Delta_1]^2/\Delta_2 \\ \Delta_2 &= (Y_2+Y_3)(Y_1+Y_5)/\Delta_1 + Y_4. \end{aligned}$$

Step 6: The extended multiport matrix equation is

$$\begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} V_{11} - V_{10} \\ V_{21} - V_{20} \end{bmatrix} = \begin{bmatrix} I_{11} \\ I_{21} \end{bmatrix} \tag{4.19}$$

where $V_{10} = 0$.

Compared with (4.17), we obtain

$$\begin{aligned} Y_{pp} &= y_{11} \\ Y_{pe} &= y_{12} \\ Y_{ep} &= y_{21} \\ Y_{ee} &= y_{22} \\ V_p &= V_{11} - V_{10} \\ V_e &= V_{21} - V_{20} \\ I_p &= I_{11} \\ I_e &= I_{21} \end{aligned}$$

from which we can establish the HB equation.

4.4.3 Discussion

We presented a simple approach to construct a multiport matrix for nonlinear circuit simulation by the HB method. The approach is efficient, for it only needs certain matrix row and column additions, and $b + m_s - 1$ matrix column eliminations, where the order of the matrix is $b +$ (total number of terminals between the linear circuit and m_s external ports). The approach is simple and therefore easy to program. It was successfully implemented in a large-signal parameter extraction program to be discussed in the next chapter, which exploits the HB technique as the nonlinear circuit simulation method.

4.5 CONCLUDING REMARKS

In this chapter, we described the implementation of the HB method, the recently exploited effective frequency domain nonlinear circuit simulation technique. The formulations of the HB equation were given, together with the computation of the corresponding

Jacobian matrix. An efficient approach to construct the multiport matrix for the linear part of a nonlinear circuit was proposed and illustrated by an example. The approach should be particularly useful in the case of circuit optimization where the linear multiport matrix needs to be updated in every iteration.

In the next chapter, we will utilize the HB technique as the simulation tool for nonlinear large-signal FET model parameter extraction, where the model parameters are identified under practical (large-signal) working conditions. In Chapter 6 we will further explore the properties of the HB equation.

Chapter 5

LARGE-SIGNAL FET MODEL PARAMETER EXTRACTION

5.1 INTRODUCTION

In Chapter 3, we presented a nonlinear FET model parameter extraction approach which simultaneously matches the model responses to DC and small-signal S parameter measurements. Compared with other conventional parameter extraction approaches which normally determine model parameters by sequentially fitting DC and small-signal measurements, the integrated DC/small-signal parameter extraction approach presented in Chapter 3 can provide more reliable model parameters.

However, when the model parameters are extracted solely from DC and small-signal measurement data, the model may not be accurate enough for high-frequency large-signal applications, though the model may provide accurate results under DC and/or small-signal operating conditions.

Parameter extraction employing large-signal power measurements has been seen in the literature. For example, Epstein *et al.* (1988) [32] used load-pull measurements to characterize GaAs MESFET devices. The approach modifies part of the model parameters, namely, the parameters of the nonlinear current source and nonlinear capacitive elements which have been obtained from DC and small-signal measurement fits, by fitting the model

response to the large-signal load-pull measurements. It offers an alternative to obtain a model suitable for large-signal applications. However, as we know, when the model is working under large-signal conditions, higher harmonics inevitably exist in the model response and contain important information of the nonlinearities of the device. The approach proposed by Epstein *et al.* [32] does not distinguish individual harmonics.

In this chapter, we present a nonlinear large-signal FET parameter extraction procedure by Bandler, Zhang, Ye and Chen [12] which utilizes spectrum measurements, including DC bias information and power output at different harmonics, under practical working conditions [46]. Besides multi-bias and multi-frequency excitations used in the approach presented in Chapter 3, multi-power input is introduced for large-signal parameter extraction. The harmonic balance (HB) simulation technique discussed in Chapter 4 is employed for fast nonlinear frequency domain simulation in conjunction with ℓ_1 [6] and ℓ_2 optimization for extracting the parameters of the nonlinear elements in the large-signal FET model. Powerful nonlinear adjoint analysis for sensitivity computation [11] is implemented with attendant advantages in computation time.

Numerical experiments will be discussed to show that all the parameters can be identified under practical large-signal conditions, and that including higher harmonics in large-signal parameter extraction is crucial to the reliability of the model. We will also show numerical results obtained in processing actual measurement data provided by Texas Instruments [69]. Good agreement between the measurements and the model responses is reached, demonstrating the feasibility of this parameter extraction approach.

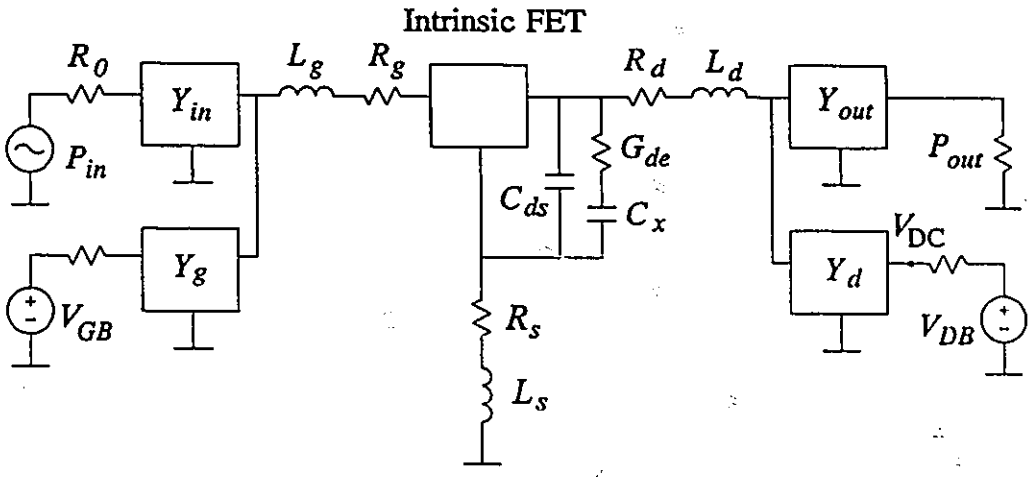


Figure 5.1: Circuit setup for large-signal multiharmonic FET measurement.

5.2 LARGE-SIGNAL MEASUREMENTS

Consider a FET model and its measurement environment shown in Figure 5.1, where Y_{in} and Y_{out} are input and output 2-ports, and Y_g and Y_d are gate and drain bias 2-ports, respectively. A large-signal power input P_{in} is applied to the circuit. The responses including DC and several harmonic components are measured.

In addition to the multi-bias, multi-frequency concept pioneered for small-signal parameter extraction by Bandler, *et al.* [5,10], we allow the circuit to be excited at different input power levels. The multi-harmonic measurements are taken at various combinations of bias points, fundamental frequencies and input power levels, contributing to the information needed for real large-signal parameter extraction. In the following discussion we use the term *bias-input-frequency combination* to indicate the modeling circuit working at a bias point with a particular input power level and at a particular fundamental frequency.

5.3 OPTIMIZATION FOR LARGE-SIGNAL PARAMETER EXTRACTION

Assume that for the jth bias-input-frequency combination, $j = 1,2,\ldots,M$, the

Jacobian matrix. An efficient approach to construct the multiport matrix for the linear part of a nonlinear circuit was proposed and illustrated by an example. The approach should be particularly useful in the case of circuit optimization where the linear multipert matrix needs to be updated in every iteration.

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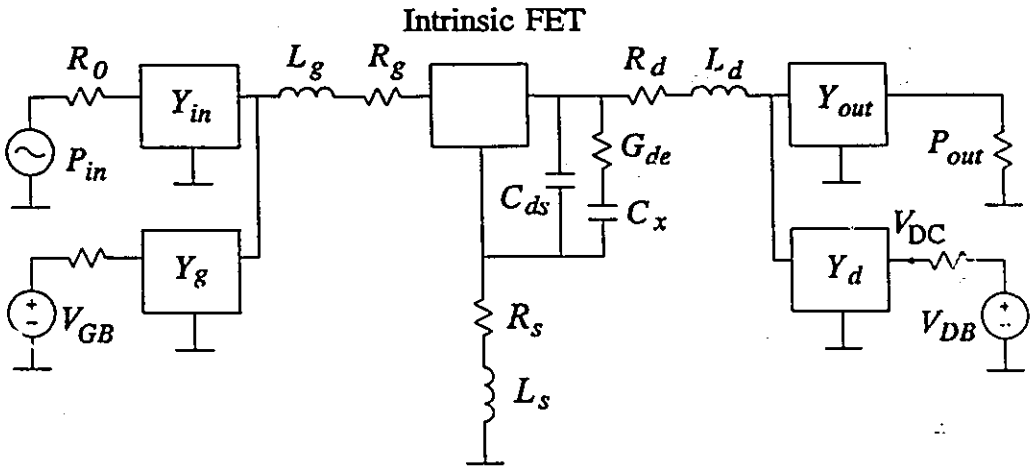

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5.3 OPTIMIZATION FOR LARGE-SIGNAL PARAMETER EXTRACTION

Assume that for the jth bias-input-frequency combination, $j = 1,2,\ldots,M$, the

measurement is

$$S_j = [S_j(0)\ S_j(\omega_{j1})\ \ldots\ S_j(\omega_{jH'})]^T \tag{5.1}$$

where M is the number of bias-input-frequency combinations, $S_j(0)$ is the DC component of the measurement, $S_j(\omega_{jk})$, $k = 1,2,\ldots,H'$, is the kth harmonic component at the jth bias-input-frequency combination, and H' is the number of harmonics contained in the measurements. $S_j(0)$ can be taken as the bias-related DC voltage or current, which varies at different fundamental frequencies and input levels even at a fixed bias point. When using power spectrum measurements, $S_j(\omega_{jk})$ denotes the kth harmonic of the output power spectrum measured at the jth bias-input-frequency combination. (The equivalent output voltage with phase information might also be employed [46]).

Corresponding to (5.1), the model response $F_j(\phi)$ can be expressed as

$$F_j(\phi) = [F_j(\phi,0)\ F_j(\phi,\omega_{j1})\ \ldots\ F_j(\phi,\omega_{jH'})]^T \tag{5.2}$$

where ϕ stands for the parameters of the model to be determined. The parameter extraction problem can be formulated as the following optimization problem:

$$\min_{\phi} \sum_{j=1}^{M} \left(w_{j0} \left| F_j(\phi,0) - S_j(0) \right|^p + \sum_{k=1}^{H'} w_{jk} \left| F_j(\phi,\omega_{jk}) - S_j(\omega_{jk}) \right|^p \right) \tag{5.3}$$

where w_{j0} and w_{jk} are weighting factors for DC and nonzero frequency error functions, respectively, and $p = 1$ or 2 corresponds to ℓ_1 or ℓ_2 optimization, respectively. Here we single out the DC error function to emphasize the difference between the DC measurements and the nonzero frequency measurements.

The criterion of optimization in (5.3) is to simultaneously match the model responses to the measurements at DC and several harmonics. It is clear that the usefulness of this parameter extraction approach depends on the effectiveness of calculating the model responses $F_j(\phi)$, $j = 1,2,\ldots,M$, and their derivatives. Due to the efficiency of the HB simulation

technique discussed in Chapter 4, such a nonlinear large-signal FET model parameter extraction is computationally feasible.

The magnitude of the circuit responses varies widely at different bias-input-frequency combinations and different harmonics. A balanced weight selection algorithm was developed to improve robustness and enhance convergence speed [12]. It will be discussed in Section 5.5. On the other hand, if harmonic measurements are made with output powers, the conditioning of the optimization problem can be further improved by converting output powers to equivalent output voltages.

5.4 NONLINEAR CIRCUIT SIMULATION AND GRADIENT CALCULATION

Let the nonlinear circuit for parameter extraction be partitioned into linear and nonlinear subcircuits, as illustrated in Figure 5.2. Assume that the multiport matrix Y of the linear subcircuit can be established, all the nonlinear elements are voltage-controlled, and there is no nonlinear inductor inside the intrinsic FET model. In the rest of this chapter, we will focus our discussions on the jth bias-input-frequency combination, therefore the corresponding subscript j will be omitted to simplify the notation. Other bias-input-frequency combinations can be treated similarly.

5.4.1 Nonlinear Circuit Simulation Using the HB Method

Following the definitions and the discussions in Chapter 4, the HB equation can be expressed as

$$\mathcal{F}(\phi, V(\phi), k) =$$

$$I_n(\phi, V(\phi), k) + j\Omega(k)Q_n(\phi, V(\phi), k) + Y(\phi, k)V(\phi, k) + I_s(\phi, k) = 0, \quad (5.4)$$

$$k = 0, 1, \ldots, H$$

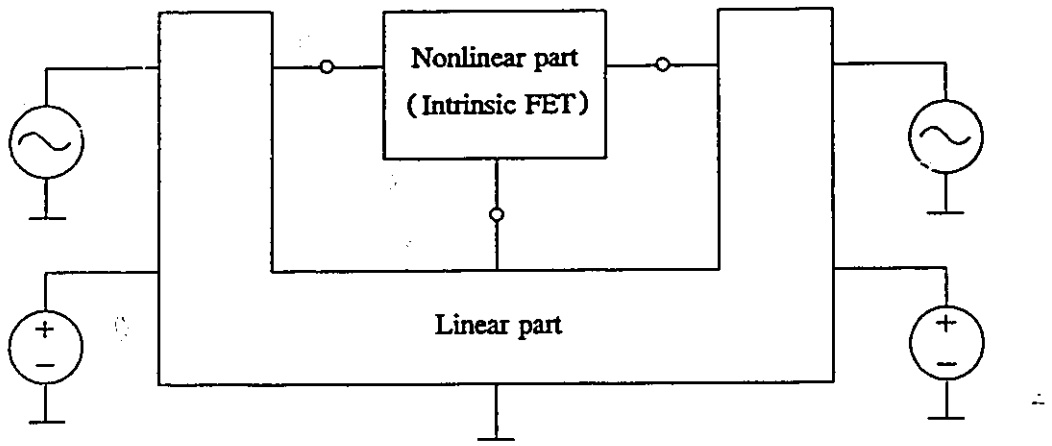


Figure 5.2: Block diagram for illustrating circuit simulation using the HB method.

where k is the harmonic index indicating ω_k, ϕ represents the optimization variables, i.e., the parameters to be determined including parameters of both linear and nonlinear elements, and H is the number of harmonics used in the HB simulation. It should be noticed that $H \geq H'$, (H' is the number of measured harmonics in (5.1)), and H can be different for different bias-input-frequency combinations. For higher accuracy H could be greater than H'.

The scalar form for the HB equation similar to (4.5) is

$$\bar{\mathcal{F}}(\phi, \bar{V}(\phi)) = \bar{I}_n(\phi, \bar{V}(\phi)) + \bar{\Omega}\bar{Q}_n(\phi, \bar{V}(\phi)) + \bar{Y}(\phi)\bar{V}(\phi) + \bar{I}_s(\phi) = 0. \qquad (5.5)$$

Note that in solving this HB equation (5.5), ϕ is constant and $\bar{V}(\phi)$ is the variable. See Chapter 4 for solving the HB equation (5.5).

After the solution for $\bar{V}(\phi)$ is reached, the model response $F(\phi)$ can be obtained as

$$F(\phi, \omega_k) = a^T(\phi, k)V(\phi, k) + b^T(\phi, k)E(k), \quad k = 0, 1, \ldots, H' \qquad (5.6)$$

where $a(\phi, k)$ and $b(\phi, k)$ are complex valued vectors determined from the linear subcircuit, and $E(k)$ corresponds to the external sources including the input power source and DC bias

sources.

5.4.2 Gradient Calculation by Nonlinear Adjoint Sensitivity Analysis

Let K_N be an index set indicating the total number of interfacing ports between the linear and nonlinear parts of the circuit, and $u_{n1}(k)$ and $u_{n2}(k)$ be unit vectors such that

$$\begin{aligned} V_n(\phi,k) &= V_n^R(\phi,k) + jV_n^I(\phi,k) \\ &= (u_{n1}(k) + ju_{n2}(k))^T \bar{V}(\phi), \quad \text{for } n \in K_N. \end{aligned}$$

The circuit response $F(\phi,\omega_k)$ from (5.6) can be rewritten as

$$F(\phi,\omega_k) = \sum_{n\in K_N} a_n(\phi,k)\,(u_{n1}(k) + ju_{n2}(k))^T\,\bar{V}(\phi) + b^T(\phi,k)E(k). \tag{5.7}$$

The derivative of $F(\phi,\omega_k)$ w. r. t. $\phi_i \in \phi$ is then

$$\begin{aligned} \frac{\partial F(\phi,\omega_k)}{\partial \phi_i} &= \sum_{n\in K_N} \frac{\partial a_n(\phi,k)}{\partial \phi_i}\left(u_{n1}^T(k) + ju_{n2}^T(k)\right)\bar{V}(\phi) \\ &+ \sum_{n\in K_N} a_n(\phi,k)\left(u_{n1}^T(k) + ju_{n2}^T(k)\right)\frac{\partial \bar{V}(\phi)}{\partial \phi_i} + \frac{\partial b^T(\phi,k)}{\partial \phi_i}E(k). \end{aligned} \tag{5.8}$$

To realize the foregoing derivative, we first derive from (5.5) that

$$\frac{\partial \bar{V}(\phi)}{\partial \phi_i} = -\bar{J}^{-1}(\phi,\bar{V}(\phi))\frac{\partial \bar{\mathcal{F}}(\phi,\bar{V}(\phi))}{\partial \phi_i} \tag{5.9}$$

where the Jacobian matrix

$$\bar{J}(\phi,\bar{V}(\phi)) = \left(\frac{\partial \bar{I}_n^T(\phi,\bar{V}(\phi))}{\partial \bar{V}(\phi)}\right)^T + \bar{\Omega}\left(\frac{\partial \bar{Q}_n^T(\phi,\bar{V}(\phi))}{\partial \bar{V}(\phi)}\right)^T + \bar{Y}(\phi)$$

which is available at the solution of the HB equation, and

$$\frac{\partial \bar{\mathcal{F}}(\phi,\bar{V}(\phi))}{\partial \phi_i} = \left(\frac{\partial \bar{I}_n(\phi,\bar{V}(\phi))}{\partial \phi_i} + \bar{\Omega}\frac{\partial \bar{Q}_n(\phi,\bar{V}(\phi))}{\partial \phi_i} + \frac{\partial \bar{Y}(\phi)}{\partial \phi_i}\bar{V}(\phi) + \frac{\partial \bar{I}_s(\phi)}{\partial \phi_i}\right)\Bigg|_{\bar{V}(\phi)=\text{const.}}$$

Multiplying both sides of (5.9) by $u_{n1}^T(k)$, we get

$$u_{n1}^T(k)\frac{\partial \bar{V}(\phi)}{\partial \phi_i} = -\hat{\bar{V}}_{n1}^T(\phi)\frac{\partial \bar{\mathcal{F}}(\phi, \bar{V}(\phi))}{\partial \phi_i} \tag{5.10}$$

where

$$\begin{aligned}\hat{\bar{V}}_{n1}^T(\phi) \;=\; & \Big[\Big(\hat{V}_{n1}^R(\phi,0)\Big)^T \;\; \Big(\hat{V}_{n1}^R(\phi,1)\Big)^T \;\; \dots \;\; \Big(\hat{V}_{n1}^R(\phi,H)\Big)^T \\ & \Big(\hat{V}_{n1}^I(\phi,0)\Big)^T \;\; \Big(\hat{V}_{n1}^I(\phi,1)\Big)^T \;\; \dots \;\; \Big(\hat{V}_{n1}^I(\phi,H)\Big)^T\Big]\end{aligned}$$

and is determined by solving the adjoint system

$$\bar{J}^T(\phi, \bar{V}(\phi))\hat{\bar{V}}_{n1}(\phi) = u_{n1}(k). \tag{5.11}$$

The actual computation will be simplified if we distinguish linear and nonlinear element parameters. For $\phi_i \in$ {linear element parameters},

$$\frac{\partial \bar{\mathcal{F}}(\phi, \bar{V}(\phi))}{\partial \phi_i} = \left[\frac{\partial \bar{Y}(\phi)}{\partial \phi_i}\bar{V}(\phi) + \frac{\partial \bar{I}_s(\phi)}{\partial \phi_i}\right]_{\bar{V}(\phi)=\text{const.}}$$

For $\phi_i \in$ {nonlinear element parameters},

$$\frac{\partial \bar{\mathcal{F}}(\phi, \bar{V}(\phi))}{\partial \phi_i} = \left[\frac{\partial \bar{I}_n(\phi, \bar{V}(\phi))}{\partial \phi_i} + \Omega\frac{\partial \bar{Q}_n(\phi, \bar{V}(\phi))}{\partial \phi_i}\right]_{\bar{V}(\phi)=\text{const.}}$$

$$\frac{\partial a_n(\phi,k)}{\partial \phi_i} \;=\; 0, \quad n \in K_N$$

and

$$\frac{\partial b(\phi,k)}{\partial \phi_i} \;=\; 0.$$

It is proved by Bandler *et al.* in [11] that if ϕ_i is a parameter of an element at branch b, then (5.10) becomes

$$u_{n1}^T(k)\frac{\partial \bar{V}(\phi)}{\partial \phi_i} =$$

$$\begin{cases} -\sum_{\ell=0}^{H} \text{Real}\left[\hat{V}_b(\phi,\ell)V_b^*(\phi,\ell)G_{bi}^*(\phi,\ell)\right] & \text{if } b \in \{\text{linear elements}\} \\ -\sum_{\ell=0}^{H} \text{Real}\left[\hat{V}_b(\phi,\ell)G_{bi}^*(\phi,\ell)\right] & \text{if } b \in \{\text{nonlinear current sources}\} \\ -\sum_{\ell=0}^{H} \text{Imag}\left[\hat{V}_b(\phi,\ell)G_{bi}^*(\phi,\ell)\right] & \text{if } b \in \{\text{nonlinear capacitors}\} \end{cases}$$

where $\hat{V}_b(\phi,\ell)$ and $V_b(\phi,\ell)$ are the voltages of branch b at harmonic ℓ and are obtained from $\hat{\bar{V}}_{n1}(\phi,\ell)$ and $\bar{V}(\phi,\ell)$, respectively, the superscript * stands for complex conjugate, and $G_{bi}(\phi,\ell)$ denotes the sensitivity expression of the element containing ϕ_i. The computation of $G_{bi}(\phi,\ell)$ for various circuit elements is listed in Table II of [11]. For nonlinear elements, $G_{bi}(\phi,\ell)$ is the ℓth Fourier coefficients of the partial derivative of the branch current $i_b(\phi,v(t))$ w.r.t. ϕ_i. For example, if branch b is the gate-to-source diode with characteristic

$$i_b(\phi,v(t)) = I_{G0}[\exp(\alpha_G v_b(t)) - 1]$$

and $\phi_i = \alpha_G$, we will have

$$\frac{\partial i_b(\phi,v(t))}{\partial \phi_i} = I_{G0} v_b(t)\exp(\alpha_G v_b(t))$$

and

$$G_{bi}(\phi,\ell) = \frac{1}{N_T}\sum_{m=0}^{N_T-1}\frac{\partial i_b(\phi,v(m\Delta T))}{\partial \phi_i} e^{-j\frac{\ell m\cdot 2\pi}{N_T}}$$

where discrete Fourier transformation is used, $N_T \geq (2H+1)$ is the number of samples in the time domain within one period T, $\Delta T = T/N_T$, and $T = 1/$(fundamental frequency of this particular bias-input-frequency combination).

Since u_{n1} and u_{n2} are similar unit vectors, the derivations in (5.10) and (5.11) can be similarly applied to

$$u_{n2}^T(k)\frac{\partial \bar{V}(\phi)}{\partial \phi_i} = -\hat{\bar{V}}_{n2}^T(\phi)\frac{\partial \bar{\mathcal{F}}(\phi,\bar{V}(\phi))}{\partial \phi_i} \tag{5.12}$$

where

$$\bar{J}^T(\phi,\bar{V}(\phi))\hat{\bar{V}}_{n2}(\phi) = u_{n2}(k). \tag{5.13}$$

However, from the software implementation and development point of view, it is inflexible to hard-code exact derivative terms for each individual nonlinear element. The

FAST technique proposed by Bandler *et al.* (1989) [13] can be employed to solve this problem. Instead of using exact analytic formulas, the *FAST* technique uses perturbation to calculate

$$\frac{\partial \bar{\mathcal{F}}(\phi, \bar{V}(\phi))}{\partial \phi_i} \approx \frac{\bar{\mathcal{F}}(\phi', \bar{V}(\phi)) - \bar{\mathcal{F}}(\phi, \bar{V}(\phi))}{\Delta \phi_i} = \frac{\bar{\mathcal{F}}(\phi', \bar{V}(\phi))}{\Delta \phi_i}$$

where $\bar{\mathcal{F}}(\phi, \bar{V}(\phi)) = 0$ at the HB solution, ϕ' equals ϕ except that ϕ_i is perturbed to $\phi_i + \Delta\phi_i$, and $\bar{V}(\phi)$ is fixed at the HB solution. The derivative term in (5.10) can be calculated, still taking advantage of the adjoint analysis. Only direct function value computation is required for the perturbation.

Summing up, we can see that the gradient of the nonlinear circuit response $F(\phi)$ w.r.t. ϕ can be calculated by nonlinear adjoint analysis which utilizes the existing Jacobian matrix from the solution of the HB equation to complete all the adjoint analysis. The equivalent conductances at the linear or nonlinear element level, such as $G_{bi}(\phi, \ell)$, or the perturbation of

$$\frac{\partial \bar{\mathcal{F}}(\phi, \bar{V}(\phi))}{\partial \phi_i}, \quad \phi_i \in \phi,$$

are the same for different adjoint systems, and therefore only need to be calculated once. Compared with the full perturbation method for gradient computations which requires solving one nonlinear circuit for each optimization variable, the nonlinear adjoint analysis not only provides the accurate gradient of the objective function, but more importantly, it significantly reduces the computation time and makes our parameter extraction approach computationally practical [11,13].

5.5 WEIGHT ASSIGNMENT PROCEDURE

In the large-signal parameter extraction approach presented in Section 5.3, the model response is optimized to match several harmonics at various bias-input-frequency combinations. Two difficulties must be overcome to optimize the objective function in (5.3): the magnitude differences between different harmonic measurements, and the differences between different bias-input-frequency combinations. Suitably chosen weighting factors can balance these differences and improve the convergence of the optimization. This weight assignment procedure assumes that (a) the possibility of having large measurement errors is small, (b) the power measurement has been converted to the magnitude of the output voltage, and (c) we want one harmonic in a bias-input-frequency combination to have the same opportunity to influence the objective function as the same harmonic at another bias-input-frequency combination.

A. Balance of a Harmonic between Different Bias-Input-Frequency Combinations

In (5.1) of Section 5.3, we have defined the kth harmonic measurement $S_j(\omega_{jk})$, where $j \in \{1,2,\ldots,M\}$ corresponds to the jth bias-input-frequency combination. Let $\bar{S}_k$ be the mean value of the kth harmonic measurement over M combinations:

$$\bar{S}_k = \frac{1}{M}\sum_{j=1}^{M} S_j(\omega_{jk}), \quad k = 0,1,\ldots,H'. \tag{5.14}$$

Since the measurement will not be zero, we can balance the kth harmonic by

$$w'_{jk} = \frac{\bar{S}_k}{S_j(\omega_{jk})}. \tag{5.15}$$

Minimum and maximum bounds can be imposed on w'_{jk}, for example, a simple linear mapping can be used within the kth harmonic if some $w'_{jk}, j = 1,\ldots,M$, lies outside the bound(s). A graphical description of a linear mapping is shown in Figure 5.3, where, for

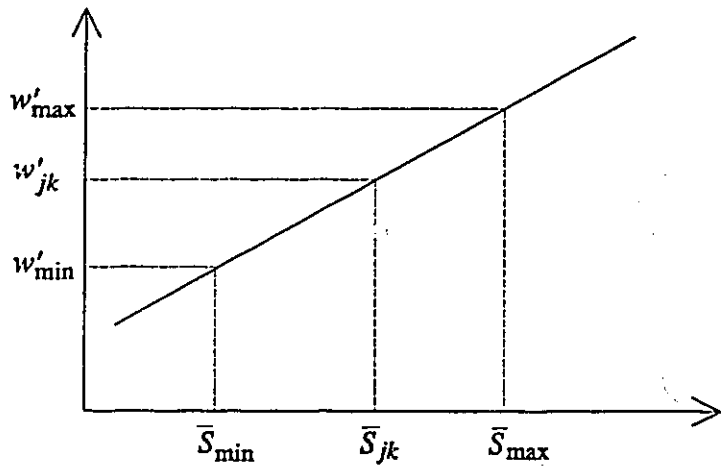


Figure 5.3: Linear mapping for balanced weight assignment.

illustration purposes, $w'_{\min}$ and $w'_{\max}$ denote minimum and maximum bounds, respectively,

$$\bar{S}_{\min} = \min_j \left\{ \frac{\bar{S}_k}{S_j(\omega_{jk})} \right\},$$

$$\bar{S}_{\max} = \max_j \left\{ \frac{\bar{S}_k}{S_j(\omega_{jk})} \right\},$$

$$\bar{S}_{jk} = \frac{\bar{S}_k}{S_j(\omega_{jk})}.$$

B. Balance between Different Harmonics

In practice we may want to emphasize some harmonics over others, e.g., the lower harmonic measurements may be emphasized due to their larger magnitudes and therefore higher measurement accuracy. This requires adjustment between different harmonics. Let W_k be the weight adjustment factor for the kth harmonic. Then the weighting factors for the optimization problem (5.3) can be expressed as

$$w_{jk} = W_k w'_{jk} \frac{\bar{S}_1}{\bar{S}_k}, \quad k = 0, 1, \ldots, H' \tag{5.16}$$

where we take the mean value of the first harmonic measurement as a reference. As an

example, if we want to have equal emphasis on the DC and fundamental harmonic measurements and lower emphasis on higher harmonic measurements, we can choose $W_k = 1$ for $k = 0$ and 1, and $W_k = B^{-k}$ for $k = 2, \ldots, H'$ where $B > 1$.

5.6 PROGRAM STRUCTURE FOR LARGE-SIGNAL PARAMETER EXTRACTION

The key part of the program for large-signal parameter extraction is the error function and its gradient computation section inside the optimization loop for a given ϕ. This section consists basically of three parts: the HB simulator, the error function and its gradient formulations.

For each bias-input-frequency combination, HB simulation is first applied to the modeling circuit. The scalar form of the HB equation (5.5) is formed and $\bar{V}$ is solved by Powell's nonlinear equation solving technique [55]. With the HB solution $\bar{V}$, the model response $\boldsymbol{F}$ defined in (5.6) can be obtained.

The error function at the bias-input-frequency combination is formed by the difference between $\boldsymbol{F}$ and the corresponding measurement data $\boldsymbol{S}$. See (5.3).

To calculate the gradient of the error function, we first extract the the Jacobian matrix used in solving the HB equation. After LU factorization, consecutive forward and backward substitutions are applied to obtain all the adjoint voltages. See (5.11) and (5.13) for u_{n1} and u_{n2} for all $n \in K_N$. On the other hand, the *FAST* technique may be utilized to determine

$$\left.\frac{\partial \bar{F}(\phi, \bar{V}(\phi))}{\partial \phi_i}\right|_{\bar{V}(\phi)=\text{const.}}$$

Thus, the gradient described in (5.8) can be realized, where, if ϕ_i is a parameter of the linear elements,

$$\frac{\partial a_n(\phi, k)}{\partial \phi_i}$$

$$\frac{\partial b(\phi, k)}{\partial \phi_i}$$

can be obtained by simple perturbation on the linear part of the circuit, though they may be available when $\partial \bar{\mathcal{F}}(\phi, \bar{V}(\phi))/\partial \phi_i$ is computed.

5.7 NUMERICAL EXAMPLES

Three cases are discussed in this section. In Case 1, we will show the theoretical aspects of this large-signal parameter extraction approach, i.e., the robustness, reliability and efficiency. Case 2 describes a numerical experiment of matching the Materka and Kacprzak FET model [49] to the Curtice FET model [27]. In Case 3, we will use measurement data from Texas Instruments [69] to extract the large-signal FET model parameters, where we use the Curtice FET model. Exact gradient computation is applied in Case 1 and Case 2. *FAST* is used in Case 3 for gradient computation.

5.7.1 Case 1 — Test of Robustness, Reliability and Efficiency

In this case, we use the Materka and Kacprzak model discussed in Section 3.3.2 as the nonlinear FET model. All the nonlinear elements of the model were described in Section 3.3.2. The modeling circuit is illustrated in Figure 5.4.

In order to better demonstrate the properties of the large-signal parameter extraction approach, we assume that the linear elements of the model have been determined by other methods, for instance, by small-signal S parameter matching. We use the parameter values of the linear elements from Case 1 of [12]:

$$\begin{aligned}[R_g\ L_g\ R_s\ L_s\ R_d\ L_d\ C_{ds}\ G_{de}\ C_x] \;=\; &[0.0119\Omega\ 0.1257\text{nH}\ 0.3740\Omega\ 0.0107\text{nH} \\ &0.0006\Omega\ 0.0719\text{nH}\ 0.1927\text{pF}\ 0.0023\ 1/\Omega\ 1.5\text{pF}]\end{aligned}$$

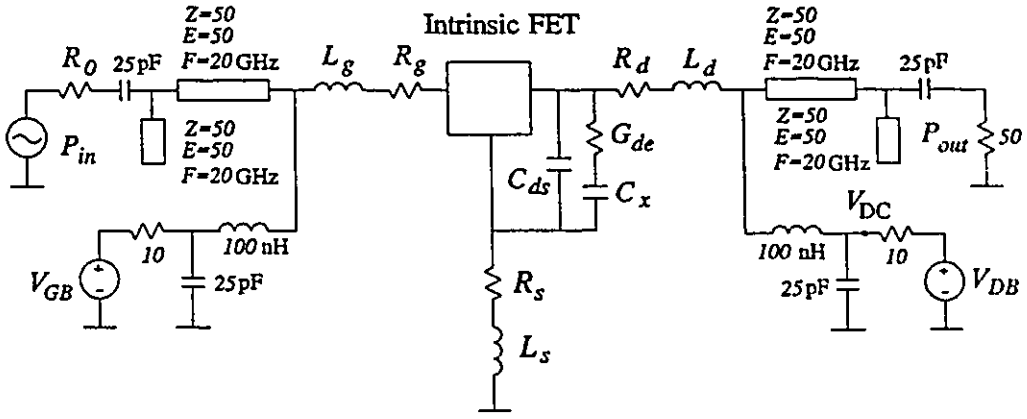


Figure 5.4: Modeling circuit for Case 1 and Case 2.

The parameters to be identified, i.e., the optimization variables, are

$$\begin{aligned}\phi \;=\; & [I_{DSS}\; V_{P0}\; \gamma\; E\; K_E\; S_1\; K_G\; \tau\; S_S\; I_{G0}\; \alpha_G\; I_{B0}\; \alpha_B \\ & R_{10}\; K_R\; C_{10}\; K_1\; C_{1S}\; C_{F0}\; K_F]^T\,. \end{aligned} \tag{5.17}$$

Notice that the model parameter V_{BC} is not included in the variable list, because it is not independent (see proof in Appendix B).

In the HB equation, the voltage-controlled nonlinear capacitors are represented by voltage-controlled nonlinear charge expressions. The derivations of q_{gs} and q_{dg} from C_{gs} and C_{dg}, respectively, are illustrated in Appendix C.

During the optimization the nonlinear circuit is solved using the HB method, where the excitation of the circuit is the available input power P_{in}, which can be converted to an equivalent input voltage source V_{in} by

$$P_{in} = \frac{|V_{in}|^2}{8R_0} \tag{5.18}$$

where $R_0 = 50\Omega$ is the source impedance.

First, we assume that the solution of the model, ϕ, is known. Such a solution is found in Table 5.1 under Case 1.

Table 5.1:

PARAMETER VALUES OF THE INTRINSIC PART OF THE MATERKA AND KACPRZAK FET MODEL

		Parameter values	
Parameter	Unit	Case 1	Case 2
I_{DSS}	A	0.1888	0.0521
V_{P0}	V	−4.3453	−1.267
γ	–	−0.3958	−0.0877
E	–	2.0	1.269
K_E	1/V	0.0	−0.3224
S_1	1/Ω	0.0972	0.0731
K_G	1/V	−0.1678	−0.6482
τ	pS	3.654	5.322
S_S	1/Ω	0.0	4.462×10^{-5}
I_{G0}	A	0.5×10^{-9}	8.782×10^{-9}
α_G	1/V	20.0	34.04
I_{B0}	A	0.5×10^{-9}	5.960×10^{-12}
α_B	1/V	1.0	4.245
V_{BC}	V	0.0*	20.0*
R_{10}	Ω	4.4302	0.0361
K_R	1/V	0.0	9.892×10^{-3}
C_{10}	pF	0.6137	1.066
K_1	1/V	0.7686	1.531
C_{1S}	pF	0.0	0.0314
C_{F0}	pF	0.0416	1.321
K_F	1/V	0.0	1.638

*: the value is fixed during optimization

The circuit is simulated at four bias points:

$$V_{GB} = -0.5\text{V} \quad V_{DB} = 2\text{V},$$
$$V_{GB} = -2.0\text{V} \quad V_{DB} = 2\text{V},$$
$$V_{GB} = -0.5\text{V} \quad V_{DB} = 5\text{V},$$
$$V_{GB} = -2.0\text{V} \quad V_{DB} = 5\text{V}.$$

At each bias point three input power levels

$$P_{in} = 5, 10, 15\text{dBm},$$

and two fundamental frequencies

$$f_1 = 1, 2\text{GHz}$$

are applied, respectively. There are a total of 24 bias-input-frequency combinations. Six harmonics are considered in the HB simulation. The output power P_{out} and the DC voltage V_{DC} of the simulation results are then used as the *simulated* measurements. This corresponds to the situation of no model deficiencies.

To examine the robustness of the approach, we generated several starting points by uniformly perturbing the assumed solution by 20 to 40 percent and optimized them with the ℓ_1 norm, i.e., $p = 1$ in (5.3). The circuit response $F_j(\phi)$ in (5.2) was computed using six harmonics ($H = 6$).

When there is no measurement error, i.e., the exact simulation results obtained at the assumed solution are used as the measurement data, optimization from all the starting points converged to the known solution exactly when we included the first three, two or one harmonics (plus DC) in the objective function, i.e., $H' = 3$, 2, or 1 in (5.3), respectively. However, it has been observed that the speed of convergence is usually faster when more harmonics are considered in the optimization.

To simulate a real measurement environment, we added 10 percent normally distributed random noise to the simulated measurements. The same starting points were

Table 5.2:

MATCH ERRORS BETWEEN THE MEASUREMENTS AND MODEL RESPONSES FOR CASE 1

	P_{out} matching errors (%)		
Harmonic match	$(H'=1)$	$(H'=2)$	$(H'=3)$
First harmonic	−0.53	−0.84	−1.08
Second harmonic	21.32	7.58	6.77
Third harmonic	−37.48	−14.36	−9.31

H' =1, 2, or 3 corresponds to the number of harmonics included in the objective function (5.3), and the comparisons here are made at bias point (V_{GB} = −2V, V_{DB} = 2V), available input power P_{in} = 10dBm and fundamental frequency f_1 = 1GHz.

optimized with the ℓ_2 norm, i.e., $p = 2$ in (5.3), and the same conditions were tested. When $H' = 3$ or 2 in (5.3), all the starting points converged to virtually one solution close to the assumed solution and gave a very good match to the measurements with noise. When $H' = 1$, however, we did not achieve convergence to a single solution close to the assumed solution. At these solutions, the matches to the measurements with noise at DC and fundamental harmonic are better than those achieved when $H' = 3$ or 2, but poor matches at the second, third and/or higher harmonics exist. Table 5.2 shows the matching errors at one of the bias-input-frequency combinations at the solutions obtained when $H' = 1, 2$ and 3 in the objective function.

From these experiments, we can see that with this approach which uses large-signal measurement data the nonlinear parameters can theoretically be determined even when $H' = 1$ in (5.3). In practice when the model is not perfect and the measurements contain

errors, it is necessary to include higher harmonic measurements in the nonlinear large-signal model parameter extraction. This not only improves convergence, but more importantly, it results in a more reliable model.

Two different starting points were used to compare the CPU execution time with and without nonlinear adjoint analysis for gradient computation. To reach the ℓ_1 objective function value of about 1.0×10^{-3} for another example having 16 bias-input-frequency combinations, 20 variables and 64 error functions, the Fortran program with the adjoint analysis runs approximately 10 times faster than that without adjoint analysis (about 200 sec. vs 2000 sec. on a VAX 8650 computer.)

5.7.2 Case 2 — Fitting to the Curtice Model

Here we use a set of data generated by the Curtice model [27] which was discussed in Section 3.7.2. The circuit is similar to that of Figure 5.4 except that the intrinsic FET is replaced by the intrinsic part of the Curtice model. Some of the parameters of the Curtice model are taken from [28, Figure 13]. See Table 5.3. The parameters in the linear part of the circuit are the same as those in Case 1.

We selected 32 bias-input-frequency combinations, as shown in Table 5.4. The first three harmonics were assumed as measurement data. Any output signal below -30dBm was discarded. There were 111 error functions in total.

To extract the parameters of the Materka and Kacprzak FET model, ℓ_2 optimization was applied and the result is listed under the Case 2 column in Table 5.1. Figure 5.5 illustrates the modeling results at a bias point other than those considered in the optimization. Excellent agreement is observed.

As for Case 1, parameters at the solution were perturbed uniformly by 20 to 40 percent and reoptimized. Of six starting points, four converged to the same solution with little variances in R_{10} and K_R. The other two converged to different local solutions with

Table 5.3:

PARAMETERS OF THE CURTICE MODEL USED FOR CASE 2

Parameter	Unit	Value
A_0	A	0.05185
A_1	A/V	0.04036
A_2	A/V^2	−0.009478
A_3	A/V^3	−0.009058
β	–	0.04062
γ	1/V	1.608
τ	pS	5.0
V_{DS0}	V	4.0
I_S	A	1.05×10^{-9}
N	–	1.0
G_{MIN}	$1/\Omega$	0.0
V_{BR}	V	20
C_{GS0}	pF	1.1
V_{BI}	V	0.7
F_C	–	0.5
C_{GD0}	pF	1.25

see Curtice [28]

Table 5.4:

INPUT LEVELS USED WITH DIFFERENT FUNDAMENTAL FREQUENCIES AND DIFFERENT BIASES FOR CASE 2

	P_{in} (dBm)			
(V_{GB}, V_{DB})	$f_1 = 0.5$GHz	$f_1 = 1.0$GHz	$f_1 = 1.5$GHz	$f_1 = 2.0$GHz
$(-0.3, 3)$	0, 4	0, 4	0, 4	0, 4
$(-0.3, 7)$	0, 4	0, 4	0, 4	0, 4
$(-1.0, 3)$	0	0	0	0
$(-1.0, 7)$	0	0	0	0
$(-0.5, 3)$	-	8	8	-
$(-0.5, 7)$	8	8	8	8

f_1 denotes the fundamental frequency

higher final objective function values.

Figure 5.6 shows the characteristics of the drain-to-source nonlinear current sources of the Curtice model and the Materka and Kacprzak model, and again we have reached an excellent match. Notice that only six bias points are used in the optimization, even less than the total number of parameters for this current source. However, since we modeled under actual large-signal conditions, employing higher harmonic measurements, a much larger range of information has been covered than individual points on the DC I–V curve can provide.

5.7.3 Case 3 — Processing Measurement Data from Texas Instruments

Actual GaAs FET large-signal power measurement data was obtained from Texas Instruments [69], from which the measurements taken at 12 bias-input-frequency combinations were used for nonlinear parameter extraction. Figure 5.7 depicts the modeling circuit where we select the Curtice nonlinear FET model [27] as the intrinsic FET described in Section 3.7.2. Table 5.5 illustrates the bias-input-frequency combinations in detail. At each combination, the DC bias current and up to three RF harmonic output power measurements are available.

Optimization with the ℓ_2 norm was performed to extract the parameters. The modeling circuit is simulated using four harmonics. There are 24 optimization variables including parameters of linear and nonlinear elements. Because of the very low sensitivities to the circuit responses, the parameters I_S, G_{MIN} and V_{BR} are not considered as optimization variables, so as to improve the condition of the optimization. Appendix A.2.1 gives the circuit and data files in *HarPE* format.

Table 5.6 lists the initial starting point and the solution. Figure 5.8 shows the match at the solution between the model responses and measurements at one of the bias points taken into account in the optimization, while Figure 5.9 shows the match at a bias point

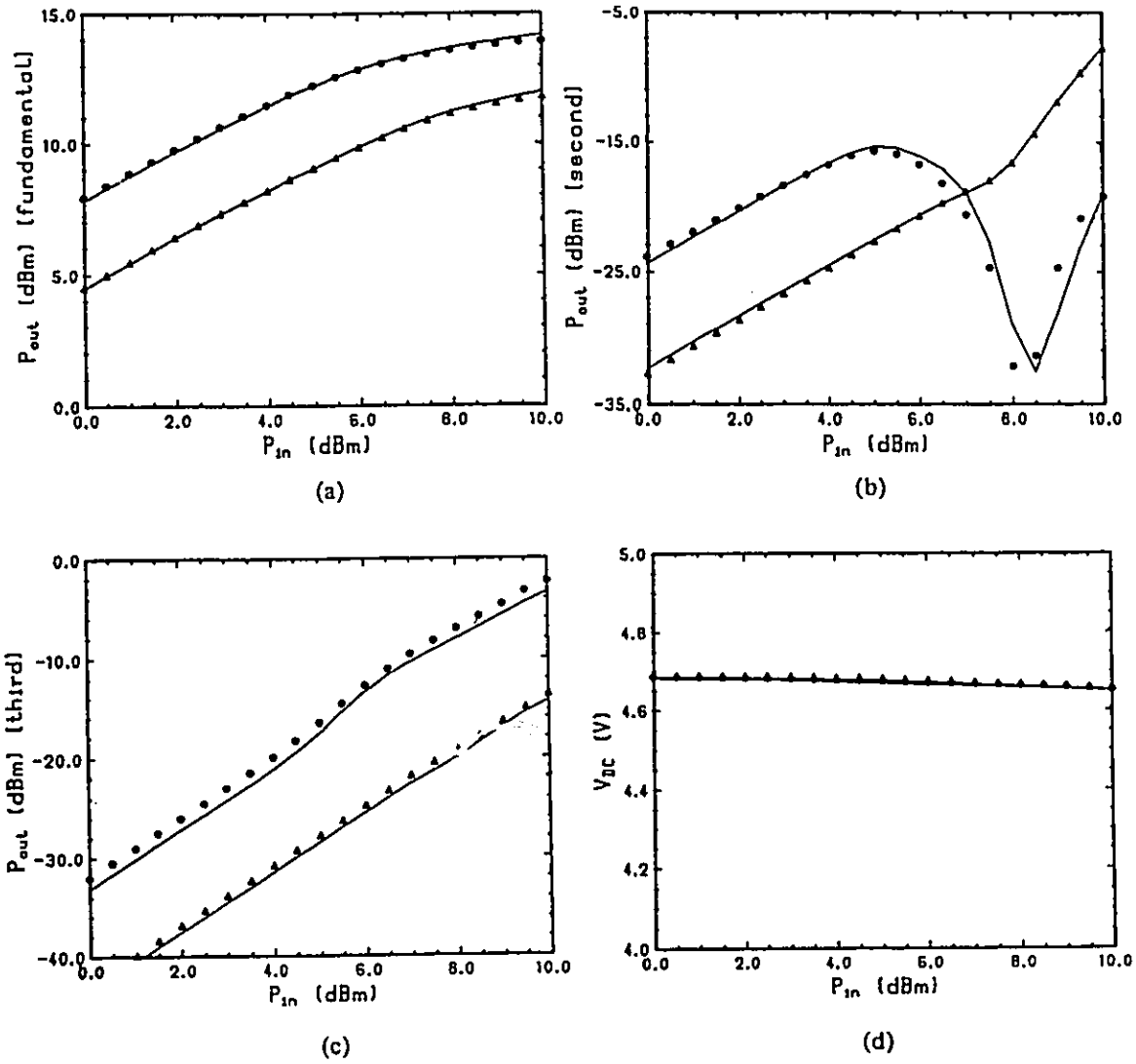


Figure 5.5: Agreement between the (Materka) model response and the simulated measurements (using the Curtice model) at $V_{GB} = -0.5$V and $V_{DB} = 5$V in Case 2. Solid lines represent the computed model response. Circles denote the simulated measurements at fundamental frequency 0.5GHz and triangles the simulated measurements at fundamental frequency 1.5GHz. (a) Fundamental component, (b) second harmonic component, (c) third harmonic component and (d) DC component of the output.

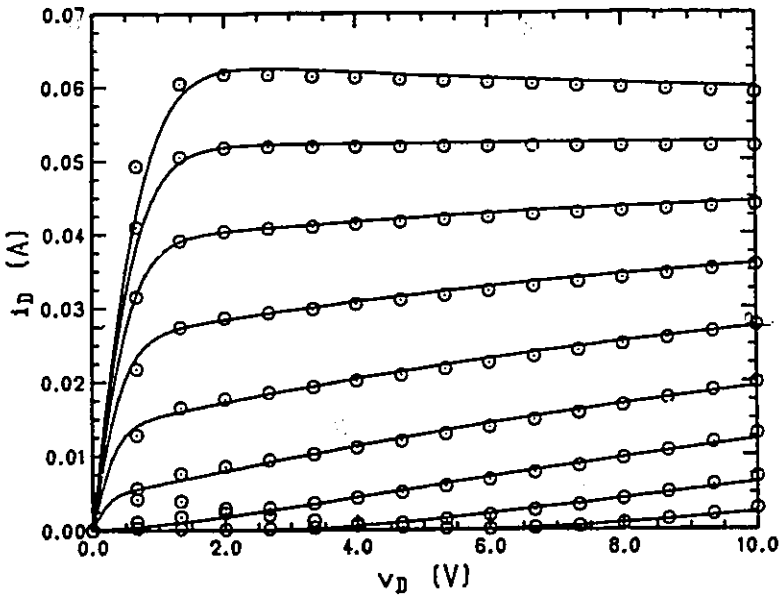


Figure 5.6: Agreement between the DC characteristics of the Materka and Kacprzak model and the simulated measurements (from the Curtice model) for Case 2.

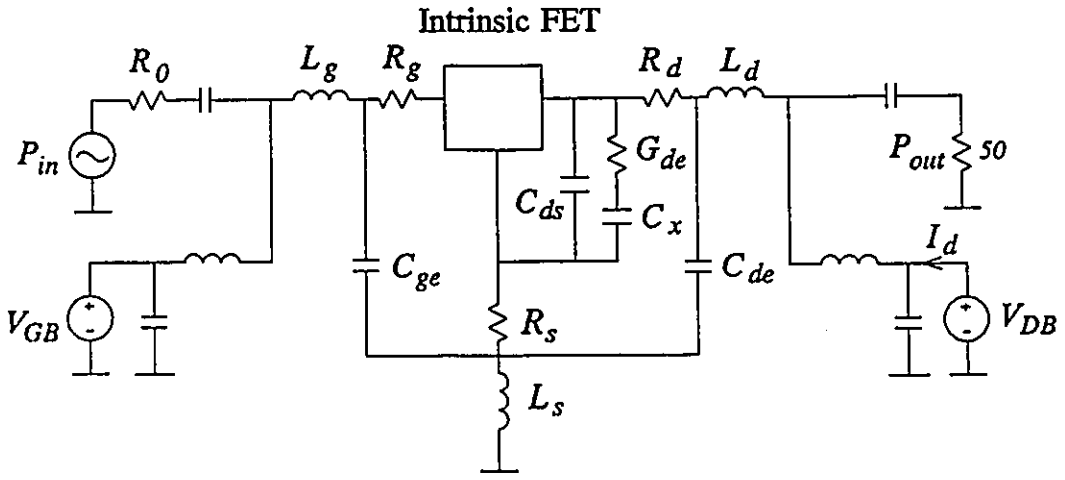


Figure 5.7: Modeling circuit for Case 3.

Table 5.5:

BIAS-INPUT-FREQUENCY MEASUREMENT COMBINATIONS FOR CASE 3

	$P_{in} = -15, -5, 5$ dBm	
	$f_1 = 0.2$GHz	$f_1 = 6.0$GHz
Bias 1 (V_{GB}, V_{DB})	$(-0.373, 2)$	$(-0.372, 2)$
Bias 2 (V_{GB}, V_{DB})	$(-1.072, 6)$	$(-1.073, 6)$
f_1 means fundamental frequency		

not included in the optimization. Good agreement at both bias points is observed.

Figure 5.10 depicts the I-V characteristics of the drain-to-source nonlinear current source at the solution. Notice that this set of curves is obtained from large-signal parameter extraction, not from typical DC I-V curve fitting.

5.8 CONCLUDING REMARKS

An accurate nonlinear large-signal parameter extraction approach has been presented in this chapter, where not only DC bias and fundamental frequency, but also higher harmonic responses have been used. The HB method for nonlinear circuit simulation, adjoint analysis for nonlinear circuit sensitivity calculation and state-of-the-art optimization methods have been applied. Improvements to the convergence of the optimization process, such as balanced weight assignment, have been discussed. Numerical results have demonstrated that the method is both theoretically and computationally feasible, i.e., the method can reliably and efficiently determine the parameters of the linear and nonlinear elements of the FET models under actual large-signal operating conditions. Numerical results have also

Table 5.6:

PARAMETER VALUES OF THE CURTICE MODEL FOR CASE 3

Parameter	Unit	Parameter values	
		Start	Solution
R_g	Ω	4	4.0272
L_g	nH	0.3	0.2178
R_d	Ω	0.5	1.5447
L_d	nH	0.2	0.3726
R_s	Ω	2	0.7019
L_s	nH	0.08	0.0449
G_{de}	$1/\Omega$	0.0002	0.0018
C_x	pF	1.5	5.4350
C_{ds}	pF	0.1	0.2441
C_{gc}	pF	0.01	0.0104
C_{de}	pF	0.01	0.0109
A_0	A	0.15	0.0729
A_1	A/V	0.15	0.0714
A_2	A/V^2	−0.02	−0.0010
A_3	A/V^3	−0.02	−0.0108
γ	1/V	1.0	1.5937
β	–	0.03	0.0379
τ	pS	3.0	3.1637
V_{DS0}	V	2.0	1.8984
I_S	A	1.0×10^{-14} *	1.0×10^{-14} *
N	–	1.0	1.3807
G_{MIN}	$1/\omega$	1.0×10^{-7} *	1.0×10^{-7} *
V_{BR}	V	30*	30*
C_{GS0}	pF	0.5	0.6362
V_{BI}	V	0.8	0.8987
F_C	–	0.7	0.7580
C_{GD0}	pF	0.092	0.0838

*: the value is fixed during optimization

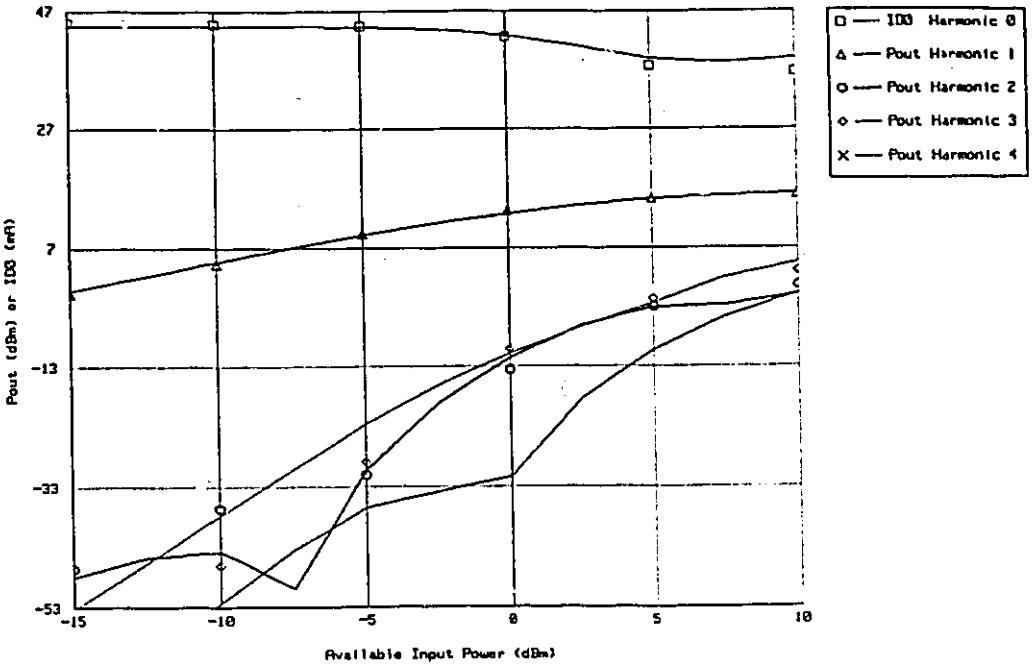


Figure 5.8: Agreement between the Curtice model responses and the measurements from Texas Instruments at fundamental frequency 0.2GHz, and bias point $V_{GB} = -0.373$V and $V_{DB} = 2$V.

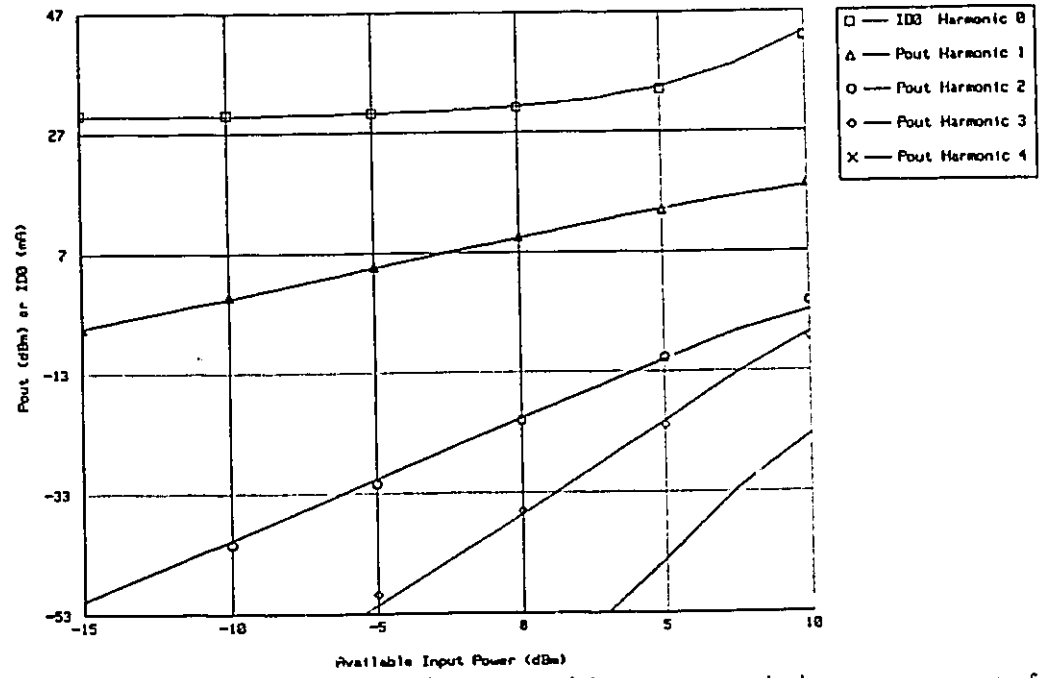


Figure 5.9: Agreement between the Curtice model response and the measurements from Texas Instruments at fundamental frequency 6GHz, and bias point $V_{GB} = -0.673$V and $V_{DB} = 4$V.

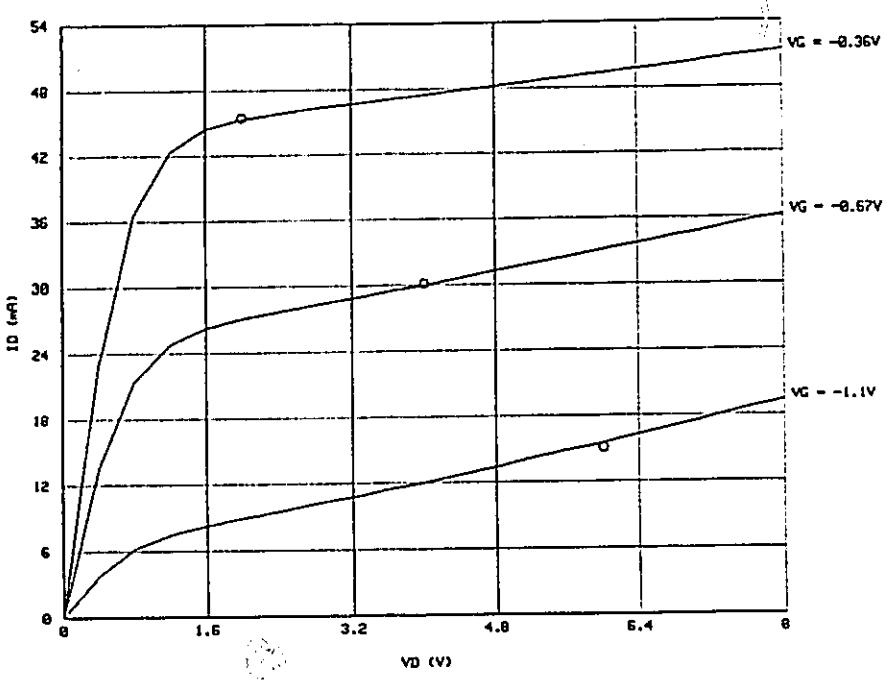


Figure 5.10: DC characteristics of the Curtice model after the optimization to match the large-signal measurement data provided by Texas Instruments. $V_G = -0.361, -0.667$ and -1.062, and V_D is from 0 to 8V.

shown that under multi-bias, multi-power input and multi-frequency excitations, spectrum measurements can effectively reflect the nonlinearities of the model and improve model reliability when used in nonlinear large-signal model parameter extraction.

Chapter 6

UNIFIED CIRCUIT SIMULATION AND DESIGN

6.1 INTRODUCTION

For the purpose of circuit analysis, the conventional DC/small-signal simulation technique has been widely used for circuits operating under small-signal conditions. The approach is simple and efficient from the computational point of view. In the case of nonlinear frequency domain steady-state circuit simulation, the harmonic balance (HB) technique [11,41] has become increasingly accepted. Besides improved accuracy, the HB technique dramatically improves the efficiency of the simulation compared with the time-domain simulation technique which derives the frequency domain responses from time-domain responses. Some available CAD software can offer both DC/small-signal and HB simulations. However, these two parts are disjoint, making optimum consistent circuit design results tedious to attain.

In this chapter, we explore the inherent analytical relationship between DC/small-signal analysis and HB analysis as initiated by Bandler, Biernacki, Chen, Song, Ye and Zhang [21]. Based on the descriptions of the HB analysis in Chapter 4, we verify that DC/small-signal analysis is, in fact, a special case of HB analysis for sufficiently small input signals. Consistent device models can then be used and other factors affecting the behaviour

of circuits such as bias, temperature, etc., can be simultaneously taken into account during circuit simulation, and hence circuit optimization.

A numerical example is used to illustrate the theoretical derivations. Two other application examples demonstrate that consistent results can be achieved which meet design specifications both for small and large signals. The approach offers superior results with respect to those obtained by considering small- and large-signal operations independently from each other.

6.2 UNIFIED CIRCUIT SIMULATION

6.2.1 Harmonic Balance Simulation Under Small-Signal Conditions

From Chapter 4, we know that the HB equation for nonlinear circuit simulation can be expressed as (4.1), i.e.,

$$\mathcal{F}(V,k) = I_n(V,k) + j\Omega(k)Q_n(V,k) + Y(k)V(k) + I_s(k) = 0, \qquad (6.1)$$
$$k = 0, 1, \ldots, H$$

or,

$$\mathcal{F}(V) = I_n(V) + j\Omega Q_n(V) + YV + I_s = 0,$$

where

$$\begin{aligned}
V &= \left[V^T(0)\ V^T(1)\ \ldots\ V^T(H)\right]^T, \\
I_n(V) &= \left[I_n^T(V,0)\ I_n^T(V,1)\ \ldots\ I_n^T(V,H)\right]^T, \\
Q_n(V) &= \left[Q_n^T(V,0)\ Q_n^T(V,1)\ \ldots\ Q_n^T(V,H)\right]^T, \\
I_s &= \left[I_s^T(0)\ I_s^T(1)\ \ldots\ I_s^T(H)\right]^T, \\
\Omega &= \mathrm{diag}\{\Omega(0),\ \Omega(1),\ \ldots,\ \Omega(H)\}, \\
Y &= \mathrm{diag}\{Y(0),\ Y(1),\ \ldots,\ Y(H)\}.
\end{aligned}$$

V is the variable vector to be solved for in the HB equation, usually the node voltages at the nodes connecting the linear and nonlinear parts of the circuit, $I_n(V)$ represents the current of nonlinear resistive elements and voltage controlled nonlinear current sources in the circuit, $Q_n(V)$ the charges of nonlinear capacitors, Ω contains all the harmonic frequencies included in HB simulation, Y is the multiport admittance matrix describing the linear part of the circuit, and I_s contains the equivalent current excitation sources.

Using inverse discrete Fourier transformation, we have, from (4.7),

$$v(t) = \sum_{l=-H}^{H} \frac{1}{a(l)} V(l) e^{jl\omega_1 t} \tag{6.2}$$

where $a(l)$ is defined as

$$a(l) = \begin{cases} 1 & l = 0 \\ 2 & l \neq 0 \end{cases}$$

ω_1 is the fundamental frequency, and $V(-l) = V^*(l)$, since $v(t)$ is a real function. The time invariant and variant parts can be separated as

$$v(t) = V(0) + \Delta v(t) \tag{6.3}$$

where

$$\Delta v(t) = \frac{1}{2}\left[\sum_{l=-H}^{-1} V(l) e^{jl\omega_1 t} + \sum_{l=1}^{H} V(l) e^{jl\omega_1 t}\right]. \tag{6.4}$$

The nonlinear current vector in the time domain $i_n(t)$ is

$$i_n(t) = i_n(v(t)).$$

Under small-signal operation, i.e., $\|\Delta v(t)\| \approx 0$, $i_n(t)$ can be expressed using the first-order Taylor series approximation

$$i_n(t) \approx i_n(V(0)) + \left(\frac{\partial i_n^T(v(t))}{\partial v(t)}\right)^T \Bigg|_{v(t)=V(0)} \Delta v(t)\,. \tag{6.5}$$

Since we know from (4.8)

$$I_n(V,k) = \frac{a(k)}{N_T}\sum_{\ell=1}^{N_T} i_n(\ell\Delta T)e^{-jk\ell\frac{2\pi}{N_T}} ,$$

under small-signal conditions $I_n(V,k)$ becomes

$$I_n(V,k) = \frac{a(k)}{N_T}\sum_{\ell=1}^{N_T}\left[i_n(V(0)) + \left(\frac{\partial i_n^T(v(t))}{\partial v(t)}\right)^T\Bigg|_{v(t)=V(0)} \Delta v(\ell\Delta T)\right] e^{-jk\ell\frac{2\pi}{N_T}} \qquad (6.6)$$

$$k = 0, 1, \ldots, H.$$

For $k = 0$,

$$\begin{aligned} I_n(V,0) &= i_n(V(0)) + \frac{1}{N_T}\left(\frac{\partial i_n^T(v(t))}{\partial v(t)}\right)^T\Bigg|_{v(t)=V(0)} \sum_{\ell=1}^{N_T}\Delta v(\ell\Delta T) \\ &= i_n(V(0)) \end{aligned} \qquad (6.7)$$

where, according to (6.4),

$$\begin{aligned} \frac{1}{N_T}\sum_{\ell=1}^{N_T}\Delta v(\ell\Delta T) &= \frac{1}{2N_T}\left[\sum_{l=-H}^{-1}\left(V(l)\sum_{\ell=1}^{N_T} e^{jl\omega_1\ell\Delta T}\right) + \sum_{l=1}^{H}\left(V(l)\sum_{\ell=1}^{N_T} e^{jl\omega_1\ell\Delta T}\right)\right] \\ &= \frac{1}{2N_T}\left[\sum_{l=-H}^{-1}\left(V(l)\sum_{\ell=1}^{N_T} e^{jl\ell\frac{2\pi}{N_T}}\right) + \sum_{l=1}^{H}\left(V(l)\sum_{\ell=1}^{N_T} e^{jl\ell\frac{2\pi}{N_T}}\right)\right] \\ &= 0. \end{aligned}$$

For $k \neq 0$,

$$I_n(V,k) = \left(\frac{\partial i_n^T(v(t))}{\partial v(t)}\right)^T\Bigg|_{v(t)=V(0)} V(k) \qquad (6.8)$$

where we have used

$$\frac{2}{N_T}\sum_{\ell=1}^{N_T} e^{-jk\ell\frac{2\pi}{N_T}} = 0, \quad \text{for } k \neq 0,$$

and

$$\frac{2}{N_T}\sum_{\ell=1}^{N_T}\Delta v(\ell\Delta T)e^{-jk\ell\frac{2\pi}{N_T}}$$

$$= \frac{2}{N_T}\sum_{\ell=1}^{N_T}(V(0)+\Delta v(\ell\Delta T))\,e^{-jk\ell\frac{2\pi}{N_T}}$$

$$= \frac{2}{N_T}\sum_{\ell=1}^{N_T} v(\ell\Delta T)e^{-jk\ell\frac{2\pi}{N_T}}$$

$$= V(k), \qquad k=1,\ldots,H.$$

It is important to notice from (6.7) that $I_n(V,0)$ is determined by $V(0)$ only, and from (6.8) that $I_n(V,k)$, $k\neq 0$, is determined by $V(k)$ as well as $V(0)$.

Similar conclusions can be obtained for $q_n(t)$ and $Q_n(V)$, i.e.,

$$Q_n(V,0) \;=\; q_n(V(0)) \tag{6.9}$$

and

$$Q_n(V,k) = \left(\frac{\partial q_n^T(v(t))}{\partial v(t)}\right)^T\Bigg|_{v(t)=V(0)} V(k) \qquad \text{for } k\neq 0 \tag{6.10}$$

where $q_n(t)=q_n(v(t))$ is the time-domain expression of $Q_n(V)$.

We have derived that the HB equation (6.1) under small signals, or simply HBSS, has such a property that $\mathcal{F}(V,0)$ depends only on $V(0)$, and $\mathcal{F}(V,k)$ for $k\in\{1,\ldots,H\}$ depends on $V(0)$ and $V(k)$. This suggests that we should be able to solve the HBSS equation by first solving $\mathcal{F}(V,0)$ for $V(0)$, and then $\mathcal{F}(V,k)$ for $V(k)$, $k\in\{1,\ldots,H\}$.

6.2.2 Jacobian Matrix For HB Simulation Under Small-Signal Conditions (HBSS)

Consider first the derivative of $I_n(V,k)$ w.r.t. $V(l)$. It is clear from (6.5) that

$$\frac{\partial i_n^T(t)}{\partial v(t)} = \frac{\partial i_n^T(v(t))}{\partial v(t)}\Bigg|_{v(t)=V(0)} = \text{constant}.$$

The derivative of $I_n(V,k)$ w.r.t. $V(l)$ can be obtained from (4.9),

$$\frac{\partial I_n^T(V,k)}{\partial V(l)} \;=\; \frac{a(k)}{a(l)}\frac{1}{N_T}\frac{\partial i_n^T(v(t))}{\partial v(t)}\Bigg|_{v(t)=V(0)}\sum_{\ell=1}^{N_T} e^{-j(k-l)\ell\frac{2\pi}{N_T}}$$

$$= \begin{cases} \left.\frac{\partial i_n^T(v(t))}{\partial v(t)}\right|_{v(t)=V(0)} & k=l,\ k,l=0,1,\ldots,H \\ \mathbf{0} & k\neq l,\ k,l=0,1,\ldots,H \end{cases} \tag{6.11}$$

Similarly, the derivative of $Q_n(V)$ is

$$\frac{\partial Q_n^T(V,k)}{\partial V(l)} = \begin{cases} \left.\frac{\partial q_n^T(v(t))}{\partial v(t)}\right|_{v(t)=V(0)} & k=l,\ k,l=0,1,\ldots,H \\ \mathbf{0} & k\neq l,\ k,l=0,1,\ldots,H \end{cases} \tag{6.12}$$

The Jacobian matrix in (4.3) of Chapter 4 is then simplified to

$$\begin{aligned} J(V) &= \left(\frac{\partial I_n^T(V)}{\partial V}\right)^T + j\Omega\left(\frac{\partial Q_n^T(V)}{\partial V}\right)^T + Y \\ &= \begin{bmatrix} \frac{\partial I_n^T(V,0)}{\partial V(0)} & \mathbf{0} & \cdots & \mathbf{0} \\ \mathbf{0} & \frac{\partial I_n^T(V,1)}{\partial V(1)} & \cdots & \mathbf{0} \\ \vdots & \vdots & \ddots & \vdots \\ \mathbf{0} & \mathbf{0} & \cdots & \frac{\partial I_n^T(V,H)}{\partial V(H)} \end{bmatrix}^T \\ &\quad + j\begin{bmatrix} \Omega(0) & & & \\ & \Omega(1) & & \\ & & \ddots & \\ & & & \Omega(H) \end{bmatrix} \begin{bmatrix} \frac{\partial Q_n^T(V,0)}{\partial V(0)} & \mathbf{0} & \cdots & \mathbf{0} \\ \mathbf{0} & \frac{\partial Q_n^T(V,1)}{\partial V(1)} & \cdots & \mathbf{0} \\ \vdots & \vdots & \ddots & \vdots \\ \mathbf{0} & \mathbf{0} & \cdots & \frac{\partial Q_n^T(V,H)}{\partial V(H)} \end{bmatrix}^T \\ &\quad + \begin{bmatrix} Y(0) & & & \\ & Y(1) & & \\ & & \ddots & \\ & & & Y(H) \end{bmatrix}. \end{aligned} \tag{6.13}$$

It is obvious that under small-signal conditions the Jacobian matrix tends to be block diagonal, i.e.,

$$J(V) = \text{diag}\{J(V,0),\ J(V,1),\ \ldots,\ J(V,H)\} \tag{6.14}$$

where

$$J(V,k) = \left(\frac{\partial I_n^T(V,k)}{\partial V(k)}\right)^T + j\Omega(k)\left(\frac{\partial Q_n^T(V,k)}{\partial V(k)}\right)^T + Y(k), \quad k = 0,1,\ldots,H. \tag{6.15}$$

It is also clear from (6.11), (6.12) and (6.15) that $J(V,k)$, for $k = 0,1,\ldots,H$, depends only on $V(0)$. In other words, when $V(0)$ is given, $J(V,k)$, for $k = 0,1,\ldots,H$, becomes a constant matrix. This is consistent with the conclusion of the previous subsection.

6.2.3 Consistency of DC/Small-Signal/Large-Signal Analysis

With the derivations in the previous two subsections, we discuss the solution of the HB equation under small-signal condition (HBSS).

First, we can solve for $V(0)$ from

$$\mathcal{F}(V,0) = I_n(V,0) + Y(0)V(0) + I_s(0) = 0 \tag{6.16}$$

where $\Omega(0) = 0$ is considered.

By substituting $I_n(V,0) = i_n(V(0))$ into (6.16), we obtain

$$i_n(V(0)) + Y(0)V(0) + I_s(0) = 0 \tag{6.17}$$

which is the normal DC equation characterizing the DC steady state of the nonlinear circuit.

With the solution of $V(0)$ from (6.17), $V(k)$ can be sequentially solved from

$$\mathcal{F}(V,k) = I_n(V,k) + j\Omega(k)Q_n(V,k) + Y(k)V(k) + I_s(k) = 0 \tag{6.18}$$

for $k = 1,\ldots,H$, because $\mathcal{F}(V,k)$ depends only on $V(k)$ as well as $V(0)$ which is already available. Applying (6.8) and (6.10), (6.18) becomes

$$\left(\frac{\partial i_n^T(v(t))}{\partial v(t)}\right)^T\Bigg|_{v(t)=V(0)} V(k) + j\Omega(k)\left(\frac{\partial q_n^T(v(t))}{\partial v(t)}\right)^T\Bigg|_{v(t)=V(0)} V(k) + Y(k)V(k) + I_s(k) = 0$$

i.e.

$$\left[\left(\frac{\partial i_n^T(v(t))}{\partial v(t)}\right)^T\Bigg|_{v(t)=V(0)} + j\Omega(k)\left(\frac{\partial q_n^T(v(t))}{\partial v(t)}\right)^T\Bigg|_{v(t)=V(0)} + Y(k)\right] V(k) + I_s(k) = 0 \tag{6.19}$$

where

$$\left(\frac{\partial i_n^T(v(t))}{\partial v(t)}\right)^T\Bigg|_{v(t)=V(0)}$$

and

$$\left(\frac{\partial q_n^T(v(t))}{\partial v(t)}\right)^T\Bigg|_{v(t)=V(0)}$$

are small-signal parameters of the nonlinear elements i_n and q_n computed at bias point $V(0)$, respectively. It is not difficult to see that (6.19) is the small-signal analysis equation of the small-signal equivalent circuit derived from the nonlinear circuit.

Equations (6.17) and (6.19) verify that DC/small-signal analysis is a special case of HB analysis with sufficiently small input signals, and hence the inherent consistency between DC/small-signal and the HB analyses. It should be emphasized, however, that while there exist techniques for DC/small-signal simulation that do not require explicit AC excitations, an AC excitations is indispensable to use HB for small-signal simulation.

6.2.4 Numerical Verification

As an example to illustrate the consistency of DC/small-signal analysis and the HB analysis, consider the single FET circuit shown in Figure 6.1 which was discussed in Section 5.7.3, where the Curtice nonlinear FET model [27] is used as the intrinsic FET. 50Ω source and load resistances are used to provide matched conditions.

In order to utilize the available software system *HarPE* [36], we calculate $|S_{21}|$ by the conventional DC/small-signal analysis, and on the other hand, calculate the fundamental harmonic power output for different input power levels using the HB analysis. Then $|S_{21}|$

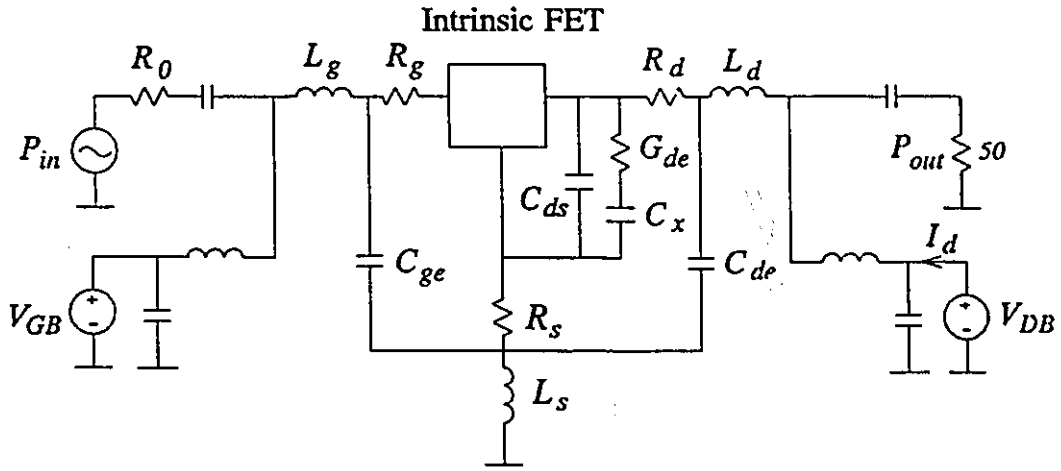


Figure 6.1: Single FET circuit with the Curtice nonlinear intrinsic FET model.

is compared with the square root of the matched transducer power gain [44] of this circuit, i.e., $\sqrt{P_{out}/P_{in}}$, where P_{in} is the power available from the source and P_{out} is the power absorbed by the load. A brief description of the relationship between $|S_{21}|$ and $\sqrt{P_{out}/P_{in}}$ is given in Appendix D.

The *HarPE* circuit file is listed in Appendix A.3.1. Four harmonics, the default in the program, are used in the nonlinear simulation. Comparison is performed at fundamental frequency $f_1 = 10$GHz and bias point $V_{GB} = -0.6$V, $V_{DB} = 4$V.

Figure 6.2 illustrates the relative error of $\sqrt{P_{out}/P_{in}}$ w.r.t. $|S_{21}|$, while the corresponding power spectrum response is shown in Figure 6.3. It is observed that when the input power P_{in} is small enough the high harmonics are negligibly small compared with the fundamental harmonic and the relative error shown in Figure 6.2 is close to zero. The error increases with the increase of the input power level. On the other hand, however, when the input power becomes too small, the error increases as well. This is because as the input power becomes too small, numerical errors inherent in the HB analysis become dominant, as shown in Figure 6.3. The good approximation range is more than 40dB. This example clearly demonstrates the foregoing theoretical derivations.

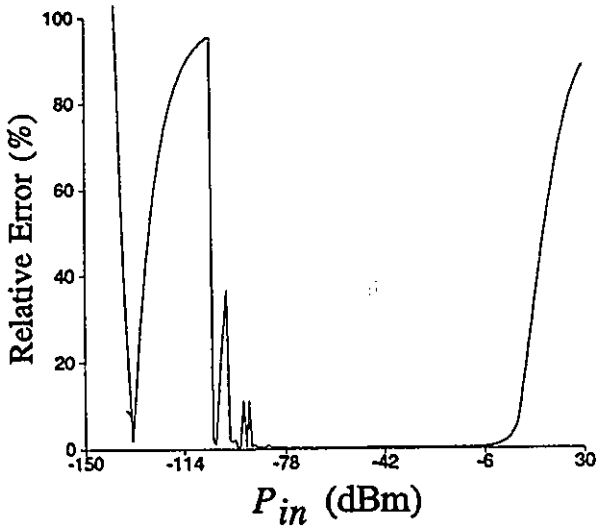


Figure 6.2: Relative error between the matched transducer power gain calculated by HB and $|S_{21}|$ by small-signal analysis with respect to different available input power levels. The bias point is $V_{GB} = -0.6$V and $V_{DB} = 4$V, and the fundamental frequency is 10GHz.

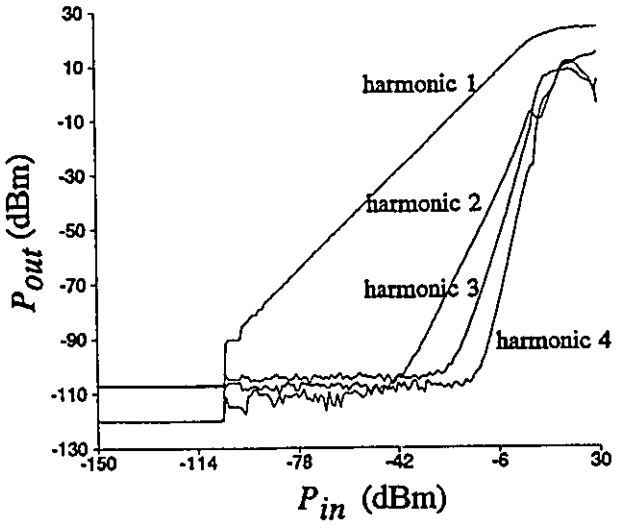


Figure 6.3: Spectrum response of the single FET circuit. The bias point is $V_{GB} = -0.6$V and $V_{DB} = 4$V, and the fundamental frequency is 10GHz.

6.2.5 Remark

In this section, a detailed derivation has been given to show the inherent relationship between the conventional DC/small-signal analysis and HB analysis. A single FET circuit example is used to illustrate the theoretical derivations.

In the foregoing manner, we have unified DC, small-signal and steady-state large-signal circuit simulation. Consistent device models can be used for both small- and large-signal circuit design, implying that a circuit design can be carried out with specifications ranging from small-signal to large-signal domains.

6.3 UNIFIED CIRCUIT DESIGN

Assume that S_{DC}, S_{AC} and S_{LS} are DC, small-signal and large-signal specifications, respectively. Let corresponding circuit responses be $F_{DC}(\phi)$, $F_{AC}(\phi)$ and $F_{LS}(\phi)$, respectively, where ϕ is the design variable consistent for DC, small-signal and large-signal domains. ϕ can include not only usual variables such as resistors, capacitors, transmission lines, etc., but also other possible parameters such as temperature, bias voltages, etc.

Let $e_{DC}(\phi)$, $e_{AC}(\phi)$ and $e_{LS}(\phi)$ be error functions in the DC, small-signal and large-signal domains, respectively. The error functions can be formulated from the differences between S_{DC} and $F_{DC}(\phi)$, S_{AC} and $F_{AC}(\phi)$, and S_{LS} and $F_{LS}(\phi)$, depending on different applications [1,8]. The circuit design problem can then be expressed as a single optimization problem, i.e., the minimization of

$$e(\phi) = \begin{bmatrix} e_{DC}(\phi) \\ e_{AC}(\phi) \\ e_{LS}(\phi) \end{bmatrix} . \tag{6.20}$$

The distinctive feature of the formation of (6.20) is that the circuit under design can be optimized to meet multi-dimensional specifications simultaneously. This is realized because

the circuit can now be simulated in a multi-dimensional space spanned seamlessly by frequency, input power, bias conditions, and/or other possible quantities such as temperature, etc.

For example, in a device model parameter extraction case, $S_{\rm DC}$, $S_{\rm AC}$ and $S_{\rm LS}$ represent the DC, small-signal and large-signal measurements of the device, respectively. And $F_{\rm DC}(\phi)$, $F_{\rm AC}(\phi)$ and $F_{\rm LS}(\phi)$ represent the corresponding DC, small-signal and large-signal responses, respectively. The objective is to make the model responses as close to the measurements as possible. Therefore, we choose

$$e_{\rm DC}(\phi) = W_{\rm DC}(F_{\rm DC}(\phi) - S_{\rm DC}) \tag{6.21}$$

$$e_{\rm AC}(\phi) = W_{\rm AC}(F_{\rm AC}(\phi) - S_{\rm AC}) \tag{6.22}$$

$$e_{\rm LS}(\phi) = W_{\rm LS}(F_{\rm LS}(\phi) - S_{\rm LS}) \tag{6.23}$$

where $W_{\rm DC}$, $W_{\rm AC}$ and $W_{\rm LS}$ are diagonal weighting matrices with diagonal weighting factors $w_{{\rm DC}i}$, $w_{{\rm AC}j}$ and $w_{{\rm LS}k}$ for DC, small-signal and large-signal responses/measurements, respectively. The model parameter ϕ is to be optimized to minimize the ℓ_1 or ℓ_2 norm of the error functions $e(\phi)$.

The circuit simulation and optimization procedure can be briefly explained in Figure 6.4. Here we consider one bias point, since multiple bias points can be treated in the similar way. When a circuit is given, there are two simulation branches available: DC/small-signal simulation and the HB simulation. (We will not discuss time-domain simulation here.) Depending on the simulation requirements or optimization specifications, we choose one or both from the two.

In the DC/small-signal simulation branch, we first solve the DC equivalent circuit of the nonlinear bias-dependent circuit. The DC responses and the DC quiescent point are determined from the DC solution. The bias-dependent small-signal parameters can be

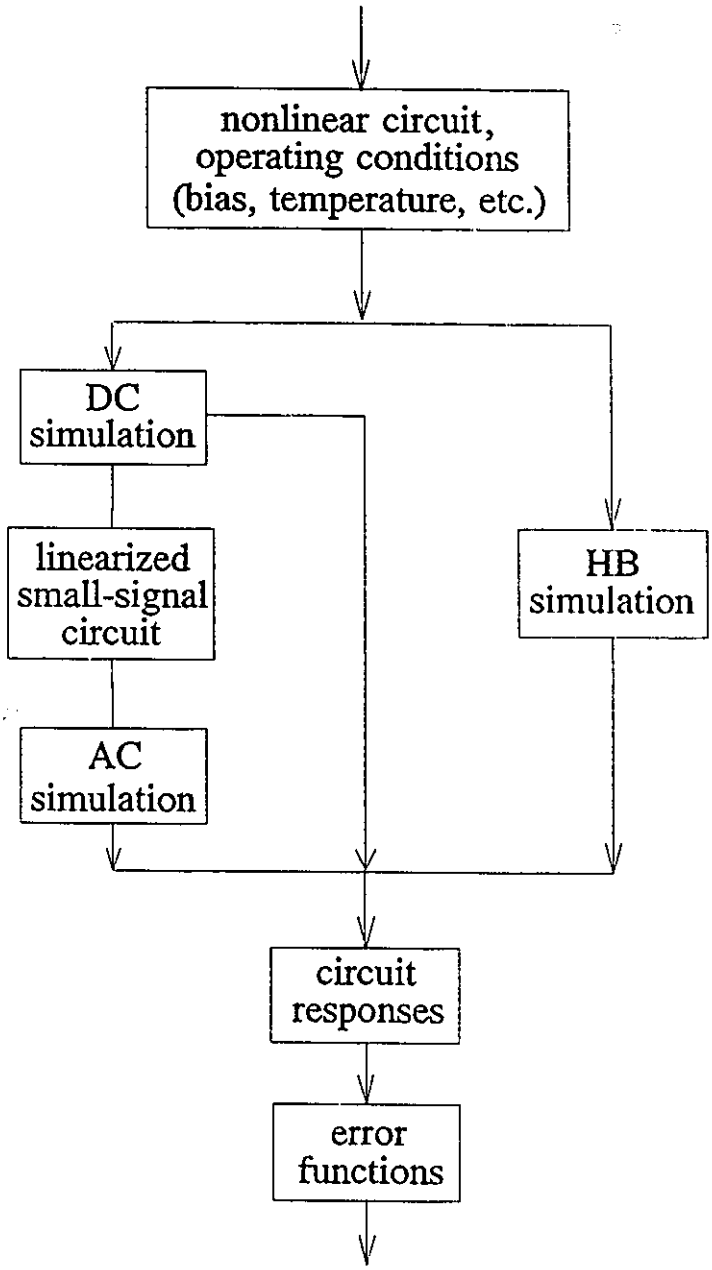


Figure 6.4: Block diagram for illustrating the unified circuit design.

computed. The AC small-signal simulations can be subsequently performed.

In the HB simulation branch, the nonlinear steady-state frequency-domain circuit responses are calculated, provided that the circuit input power or voltage level and the fundamental frequency are given. The output of the HB simulation can be voltages and/or powers of different harmonics at different nodes and/or ports.

Obviously we need HB simulation for the circuit response F_{LS}. To calculate F_{DC} and/or F_{AC}, we can use either DC/small-signal simulation or the HB simulation, because, as we have shown in Section 6.2, they are equivalent. However, if the magnitude of the input is of no importance, using DC/small-signal simulation is preferable to HB simulation, because the DC/small-signal simulation is a decoupled version of the HB simulation and, therefore, more efficient. But the HB simulation becomes indispensable when the dynamic range of the circuit is of concern even for a small-signal circuit design.

6.4 EXAMPLE 1 — FET MODEL PARAMETER EXTRACTION

We apply the unified circuit optimization concept to extract the FET model parameters by simultaneously matching DC, small-signal and large-signal measurements provided by Texas Instruments [69]. The circuit diagram is the same as Figure 6.1, where we use the Curtice nonlinear intrinsic FET model [27]. As we discussed in Section 3.7.2, there are 27 variables in total. The parameters from the intrinsic part of the equivalent circuit are

$$\{ A_0, A_1, A_2, A_3, \beta, \gamma, \tau, V_{DS0}, I_S, N, G_{MIN}, V_{BR}, C_{GS0}, V_{BI}, F_C, C_{GD0} \}$$

and the parameters from the extrinsic part

$$\{R_g, R_d, R_s, L_g, L_d, L_s, G_{de}, C_x, C_{ds}, C_{ge}, C_{de} \}.$$

However, due to the very low sensitivities of the parameters I_S, G_{MIN} and V_{BR} to the model responses, we fix them during the parameter extraction: $I_S = 1.0 \times 10^{-14}$A, $G_{MIN} =$

1.0×10^{-7} $1/\Omega$ and $V_{BR} = 30$V.

DC and small-signal measurements at three bias points, and spectrum measurements at two bias points are used for parameter extraction. The details are listed in Table 6.1.

Corresponding to (6.20), e_{DC} represents the 3 error functions between measured and modeled DC drain bias current, e_{AC} the 192 error functions between measured and modeled S parameters, and e_{LS} the 48 error functions between measured and modeled harmonic output powers. The total number of error functions is 243.

The circuit files before and after parameter extraction optimization are listed in Appendix A.3.2. Table 6.2 lists the results reached after ℓ_2 optimization, where for comparison purposes we also list the solutions from Section 3.7.2 and Section 5.7.3. The solution from Section 3.7.2 is listed under 'DC/Small', obtained by simultaneously matching the DC and small-signal parts of the measurements. The solution from Section 5.7.3 is listed under 'Large', reached by matching the large-signal part of the measurements only. Three cases are discussed in the following to compare the DC, small-signal and large-signal fits by the solutions listed in Table 6.2.

A. DC Response Comparison

The DC simulations from the three solutions are shown in Figures 6.5, 6.6 and 6.7, respectively, where the measurement data is represented by circles. The matching to the DC measurement is included in all three cases, and the DC fits are all good, though more DC measurements would be preferable.

B. Small-Signal Response Comparison

The comparison is made at the bias point $V_{GB} = -0.667$V and $V_{DB} = 4$V, and at 15 frequency points from 1GHz to 15GHz with 1GHz apart. Figures 6.8, 6.9 and 6.10 illustrate the S parameter fits from the three solutions, respectively. The fit achieved by

Table 6.1:

MEASUREMENT SETS USED FOR PARAMETER EXTRACTION IN EXAMPLE 1

DC measurements	
response type	drain current
bias conditions	$V_{GB} = -0.361$V $V_{DB} = 2$V $V_{GB} = -0.667$V $V_{DB} = 4$V $V_{GB} = -1.062$V $V_{DB} = 6$V
Small-signal measurements	
response types	magnitudes and phase of 4 S parameters
bias conditions	$V_{GB} = -0.361$V $V_{DB} = 2$V $V_{GB} = -0.667$V $V_{DB} = 4$V $V_{GB} = -1.062$V $V_{DB} = 6$V
frequencies (GHz)	1, 3, 5, 7, 9, 11, 13, 15
Large-signal measurements	
response types	DC drain current, output powers at the fundamental, second and third harmonics
bias conditions ($f_1 = 0.2$GHz)	$V_{GB} = -0.373$V $V_{DB} = 2$V $V_{GB} = -1.072$V $V_{DB} = 6$V
bias conditions ($f_1 = 6.0$GHz)	$V_{GB} = -0.372$V $V_{DB} = 2$V $V_{GB} = -1.073$V $V_{DB} = 6$V
input power (dBm)	$-15, -5, 5$

Table 6.2:

SOLUTIONS OF THE PARAMETER EXTRACTION IN EXAMPLE 1

Para.	Unit	Start	DC/Small	Large	DC/Small/Large
R_g	Ω	4.0	5.7407	4.0272	4.9820
L_g	nH	0.3	0.3525	0.2178	0.2782
R_d	Ω	0.5	0.0100	1.5447	0.0210
L_d	nH	0.2	0.3062	0.3726	0.3545
R_s	Ω	2.0	3.6041	0.7019	3.7562
L_s	nH	0.08	0.0774	0.0449	0.7386
G_{de}	1/Ω	0.0002	0.0022	0.0018	0.0026
C_x	pF	1.5	1.8842	5.4350	2.5872
C_{ds}	pF	0.1	0.0977	0.2441	0.0932
C_{ge}	pF	0.01	0.0038	0.0104	0.0062
C_{de}	pF	0.01	0.0050	0.0109	0.0053
A_0	A	0.15	0.0957	0.0729	0.0940
A_1	A/V	0.15	0.0969	0.0714	0.0968
A_2	A/V^2	−0.02	−0.0101	−0.0010	−0.0021
A_3	A/V^3	−0.02	−0.0251	−0.0108	−0.0176
γ	1/V	1.0	1.0698	1.5937	1.2926
β	–	0.03	0.0383	0.0379	0.0324
τ	pS	3.0	3.1821	3.1637	2.5460
V_{DS0}	V	2.0	1.7816	1.8984	1.2716
N	–	1.0	1.0000	1.3807	0.6938
C_{GS0}	pF	0.5	0.6144	0.6362	0.6707
V_{BI}	V	0.8	0.7991	0.8987	1.1354
F_C	–	0.7	0.7000	0.7580	0.6928
C_{GD0}	pF	0.092	0.0783	0.0838	0.0736

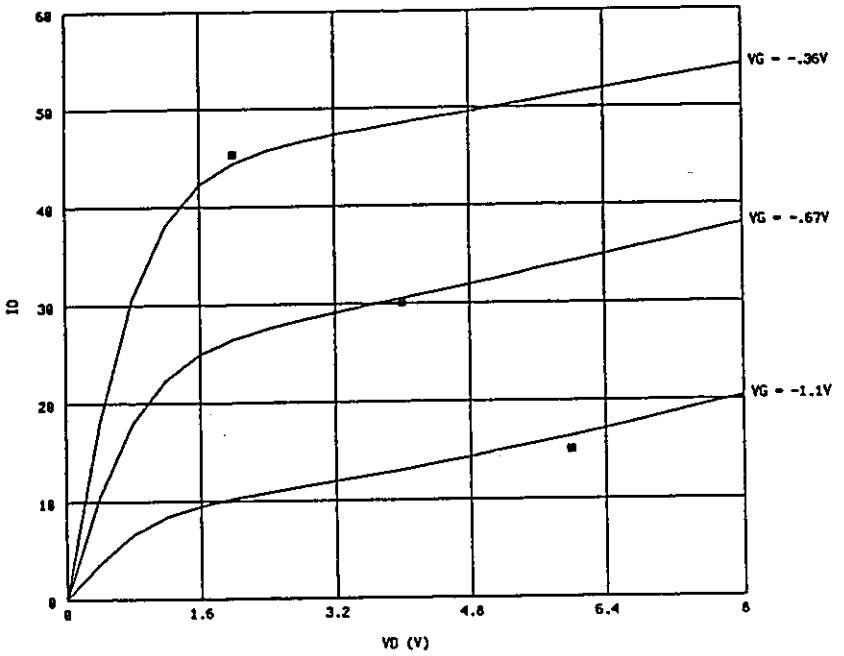


Figure 6.5: DC agreement between model and measurements at the solution obtained from DC/small-signal measurement fitting.

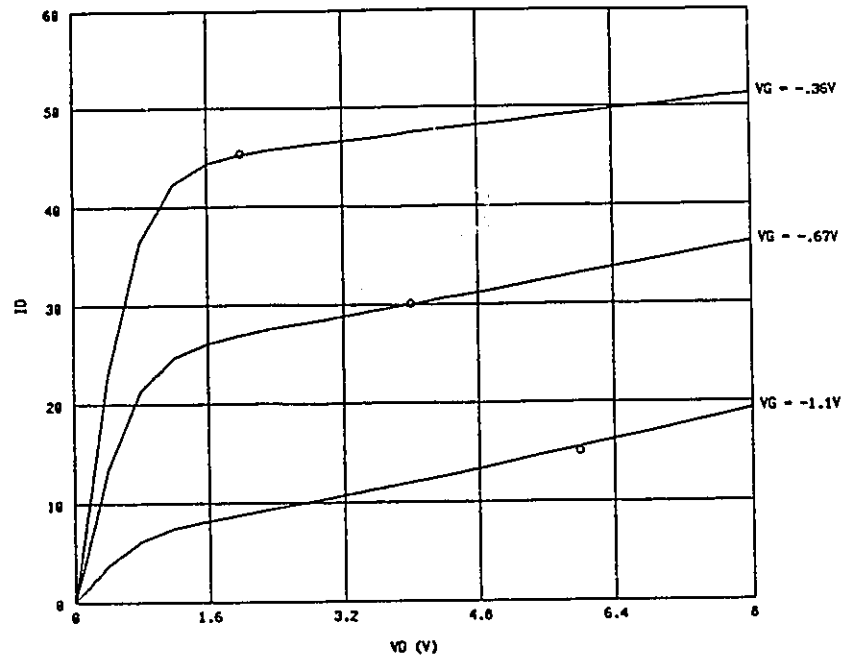


Figure 6.6: DC agreement between model and measurements at the solution obtained from large-signal measurement fitting.

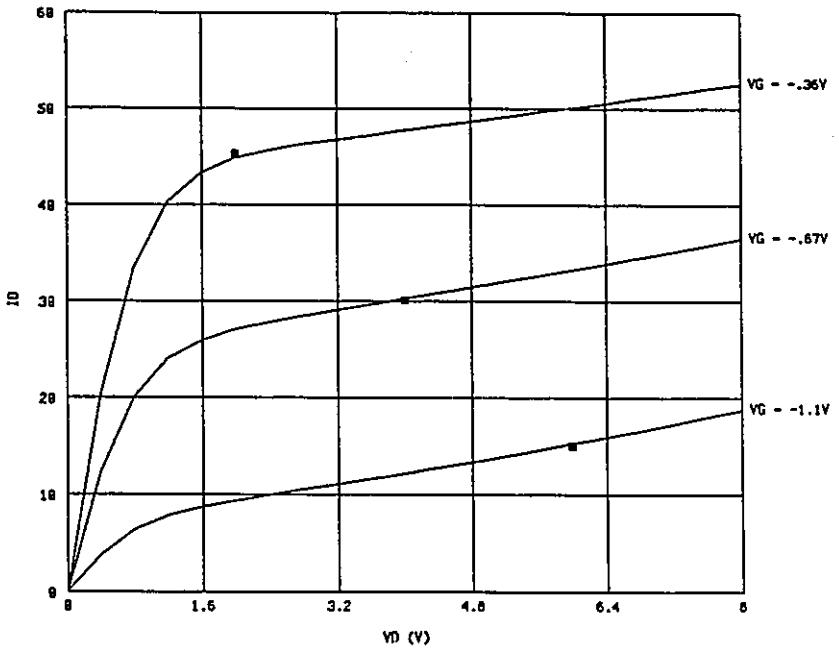


Figure 6.7: DC agreement between model and measurements at the solution obtained from simultaneous DC/small-signal and large-signal fitting.

DC/small-signal measurement matching is excellent, as shown in Figure 6.8. A very good fit can also be seen in Figure 6.10 obtained by simultaneous DC/small-signal and large-signal measurement matching. A poor fit shown in Figure 6.9, however, can be observed at the solution by large-signal measurement matching.

C. Large-Signal Response Comparison

This comparison is made at the solutions from the large-signal measurement fit and the simultaneous DC/small-signal and large-signal measurement fit. (We do not include the solution from the DC/small-signal measurement fit, since not enough DC measurement data is available to characterize the nonlinear drain-to-source current source in the model.) The two solutions are simulated at a bias-frequency combination which was not included in the parameter extraction optimization. Figures 6.11 and 6.12 show the modeled power spectra and measured power spectra. Close fits from both solutions can be observed.

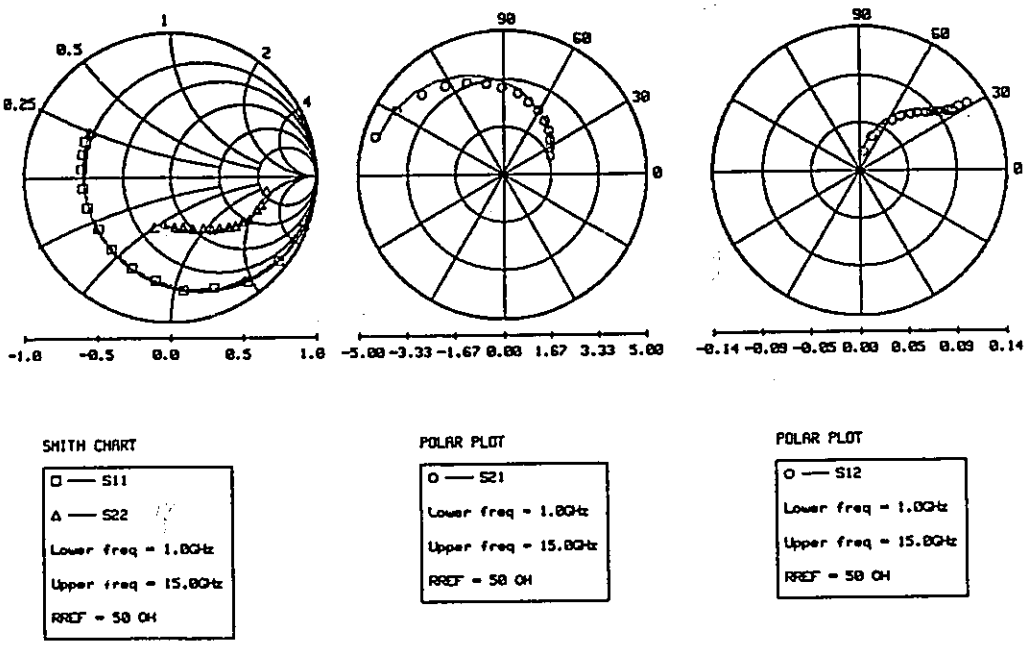


Figure 6.8: Agreement between model responses and S parameters at bias $V_{GB} = -0.667$V and $V_{DB} = 4$V. The model is obtained from DC and small-signal measurement fitting.

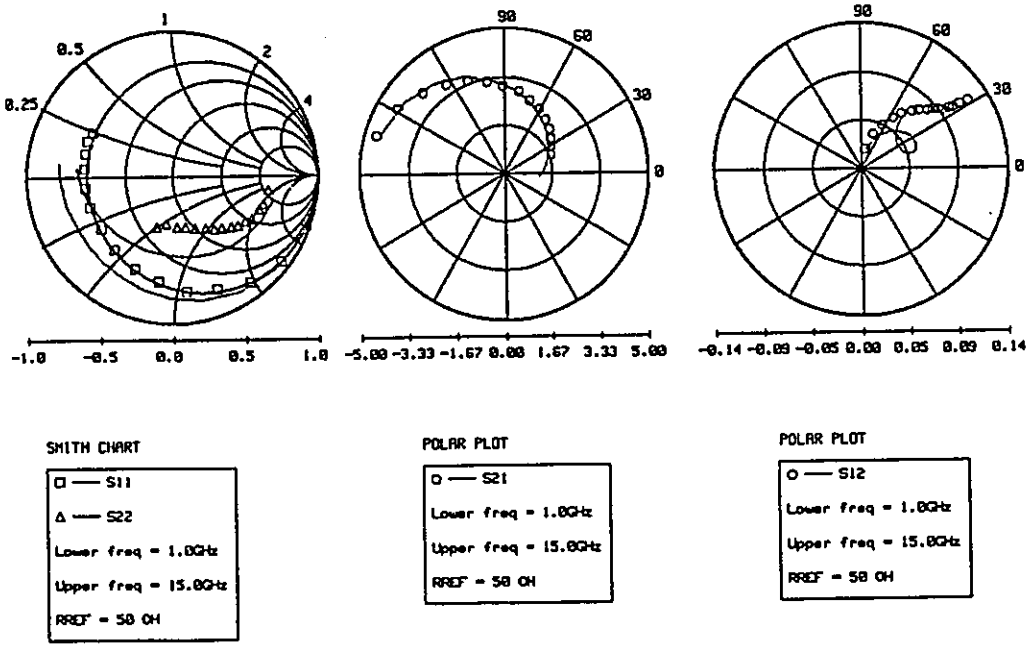


Figure 6.9: Agreement between model responses and S parameters at bias $V_{GB} = -0.667$V and $V_{DB} = 4$V. The model is obtained from large-signal measurement fitting.

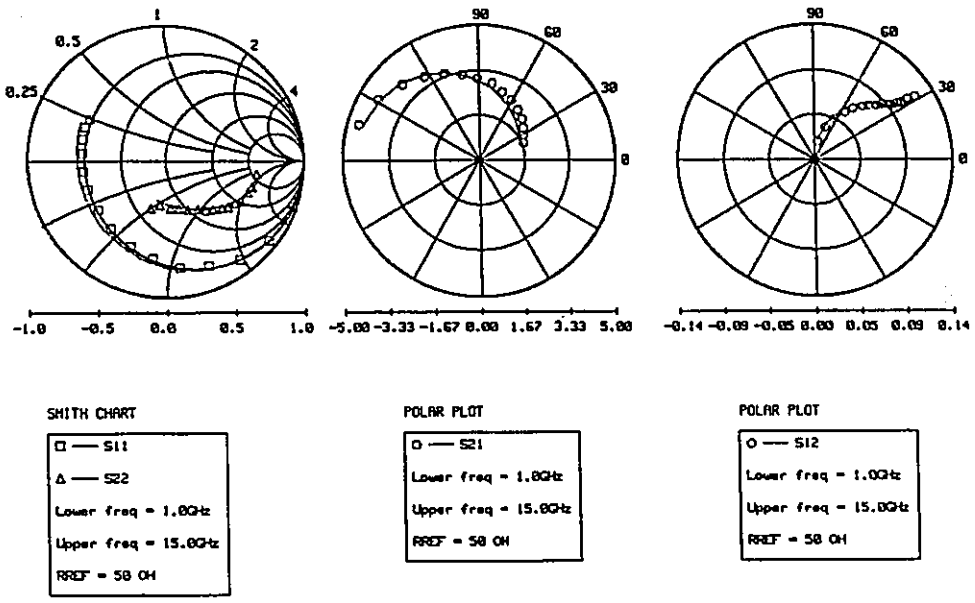


Figure 6.10: Agreement between model responses and S parameters at bias $V_{GB} = -0.667$V and $V_{DB} = 4$V. The model is obtained from simultaneous DC, small- and large-signal measurement fitting.

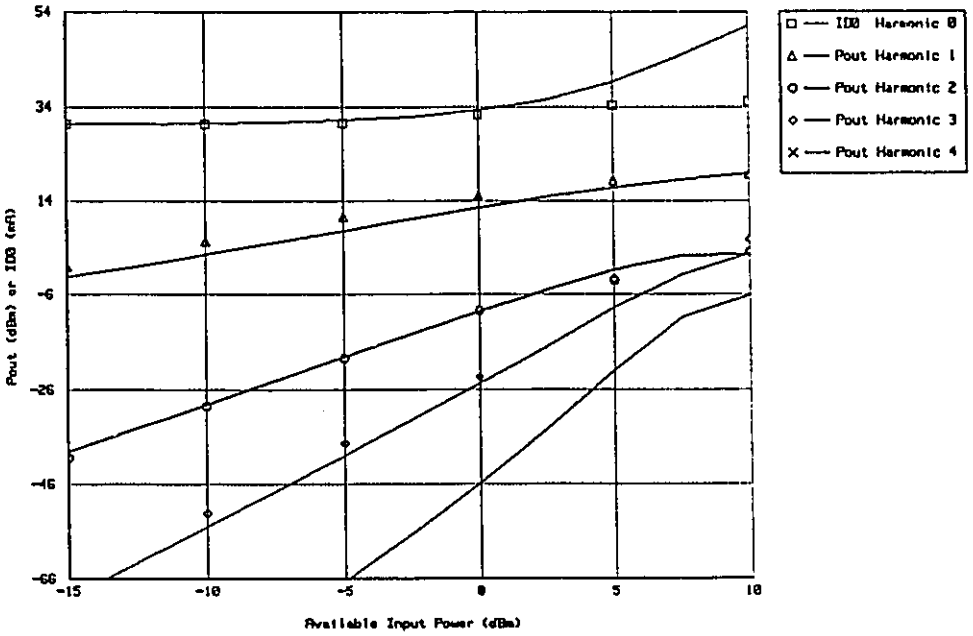


Figure 6.11: Agreement between model responses and large-signal measurements at fundamental frequency 2GHz and bias $V_{GB} = -0.667$V and $V_{DB} = 4$V. Solid lines represent responses of the model extracted from large-signal measurement fitting.

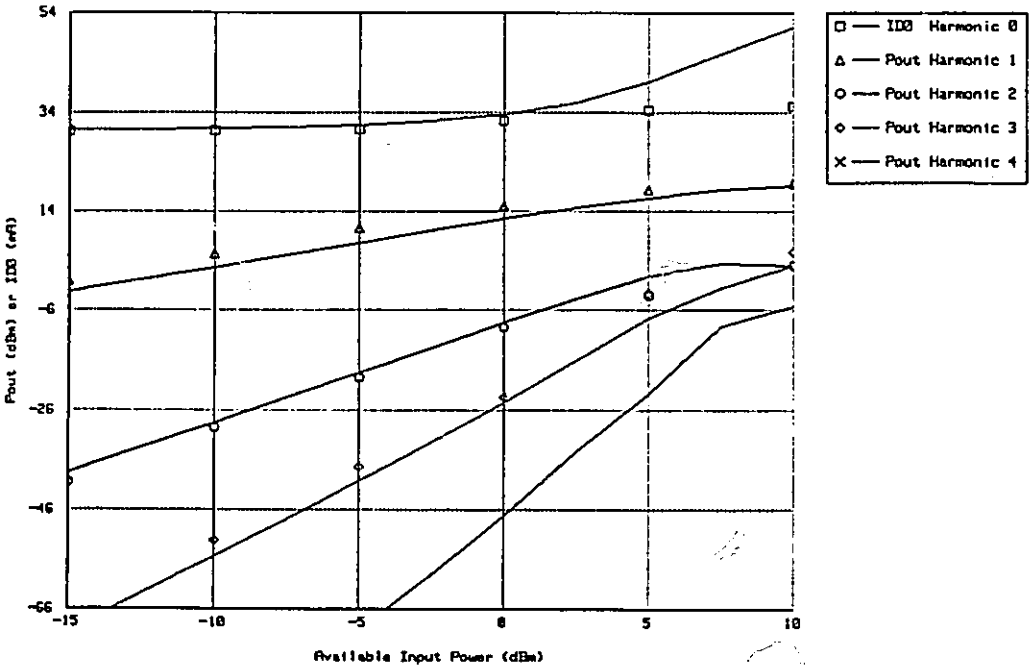


Figure 6.12: Agreement between model responses and large-signal measurements at fundamental frequency 2GHz and bias $V_{GB} = -0.667$V and $V_{DB} = 4$V. Solid lines represent responses of the model extracted from simultaneous DC, small-signal and large-signal measurement fitting.

It has been shown from the above comparisons that simultaneous DC, small-signal and large-signal device modeling can offer a good result when a comprehensive device model is required and the model parameters have effects on both small- and large-signal performance.

6.5 EXAMPLE 2 — SMALL-SIGNAL AMPLIFIER DESIGN

We design a single FET small-signal broadband amplifier [53]. The circuit diagram is shown in Figure 6.13. The Curtice nonlinear FET model is used whose parameter values are taken from Example 1 of [21], as listed in Table 6.3. We assume the specifications for the amplifier to be

$$\text{GAIN} = 8 \pm 0.5\text{dB}$$
$$|S_{11}| \leq 0.4$$
$$|S_{22}| \leq 0.4$$
$$|S_{12}| \leq 0.15$$

at frequencies 4, 5, 6, 7 and 8GHz. The FET model parameters are fixed, and the design variables are 11 element parameters in the matching network. The two bias voltages are allowed to be optimized by introducing another 2 resistors in the bias network. The circuit file is listed in Appendix A.3.3. Minimax optimization [3] is employed in the circuit design.

First, we design the amplifier by the conventional small-signal approach at a predetermined bias point selected approximately in the middle of the FET DC I-V curve. All the specifications can be met at the optimal solution under small-signal conditions. Then, we exploit our new design strategy to include the upper-end of the dynamic range of the amplifier in addition to the small-signal specifications. Specifically, we add specifications to extend the gain of the amplifier at input available power levels -10, -5 and 0dBm, and

Table 6.3:

FET MODEL PARAMETER VALUES FOR EXAMPLE 2

Parameter	Unit	Values
R_g	Ω	4.8135
L_g	nH	0.2836
R_d	Ω	0.0100
L_d	nH	0.3421
R_s	Ω	2.9178
L_s	nH	0.0818
G_{de}	$1/\Omega$	0.0026
C_x	pF	2.1167
C_{ds}	pF	0.0885
C_{ge}	pF	0.0062
C_{de}	pF	0.0052
A_0	A	0.0867
A_1	A/V	0.0871
A_2	A/V^2	−0.0020
A_3	A/V^3	−0.0154
γ	1/V	1.2618
β	–	0.0307
τ	pS	3.0186
V_{DS0}	V	1.4366
I_S	A	1.0105×10^{-14}
N	–	0.7459
G_{MIN}	$1/\Omega$	1.0003×10^{-7}
V_{BR}	V	29.9266
C_{GS0}	pF	0.5614
V_{BI}	V	1.4918
F_C	–	0.6983
C_{GD0}	pF	0.0754

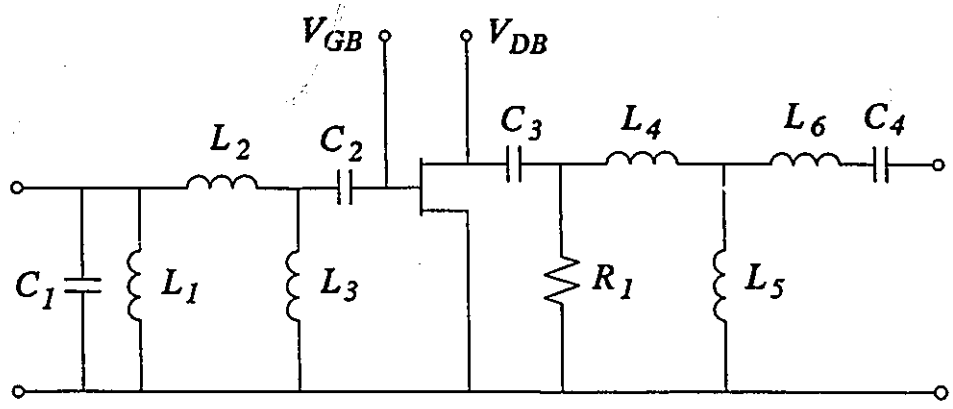


Figure 6.13: 4-8GHz small-signal broadband amplifier.

enforce second and third harmonic output power levels to be at least 40dB below the fundamental output power. All small- and large-signal specifications result in 85 error functions. We also allow the bias circuits to be optimized. All small-signal/large-signal specifications are met at the solution. The circuit file at the solution of the unified small- and large-signal design is also provided in Appendix A.3.3. The starting point and the solutions reached by small-signal design and combined small- and large-signal design are listed in Table 6.4.

Figures 6.14 and 6.15 show the results. In Figure 6.14, the gain response surfaces are depicted over fundamental frequency 2 to 10GHz and input available power -35 to 5dBm. It can be seen that the gain surface in Figure 6.14(b) which corresponds to the combined small- and large-signal optimization solution is flatter and provides a wider area which meets the gain specification.

Figure 6.15 depicts the second harmonic error surface over the same range. Any excursion above the flat part of the surface means that the second harmonic output power is less than 40dB below the fundamental output power. From Figure 6.15(a), we can see that the error becomes nonzero when the input power becomes higher than -10dBm, while in Figure 6.15(b) the zero error area extends to 0dBm input power, the area upon which we have imposed additional specifications.

Table 6.4:

SOLUTIONS OF THE SMALL-SIGNAL AMPLIFIER DESIGN IN EXAMPLE 2

Para.	Unit	Start	Small	Combined Small/Large
L_1	nH	0.38	2.10029	3.43241
L_2	nH	0.8	0.966804	1.00777
L_3	nH	1.46	4.57303	5.74427
L_4	nH	0.6	1.86403	0.959309
L_5	nH	2.5	5.66217	6.55463
L_6	nH	0.8	0.683743	0.891978
C_1	pF	0.83	0.669529	0.543859
C_2	pF	5.0	11.6326	10.3448
C_3	pF	1.85	0.243977	0.294873
C_4	pF	0.5	0.332975	0.497582
R_1	Ω	500	214.343	175.224
R_{GS}	Ω	20	20*	37.7326
R_{DS}	Ω	50	30*	48.4858

*: the value is fixed during the optimization.

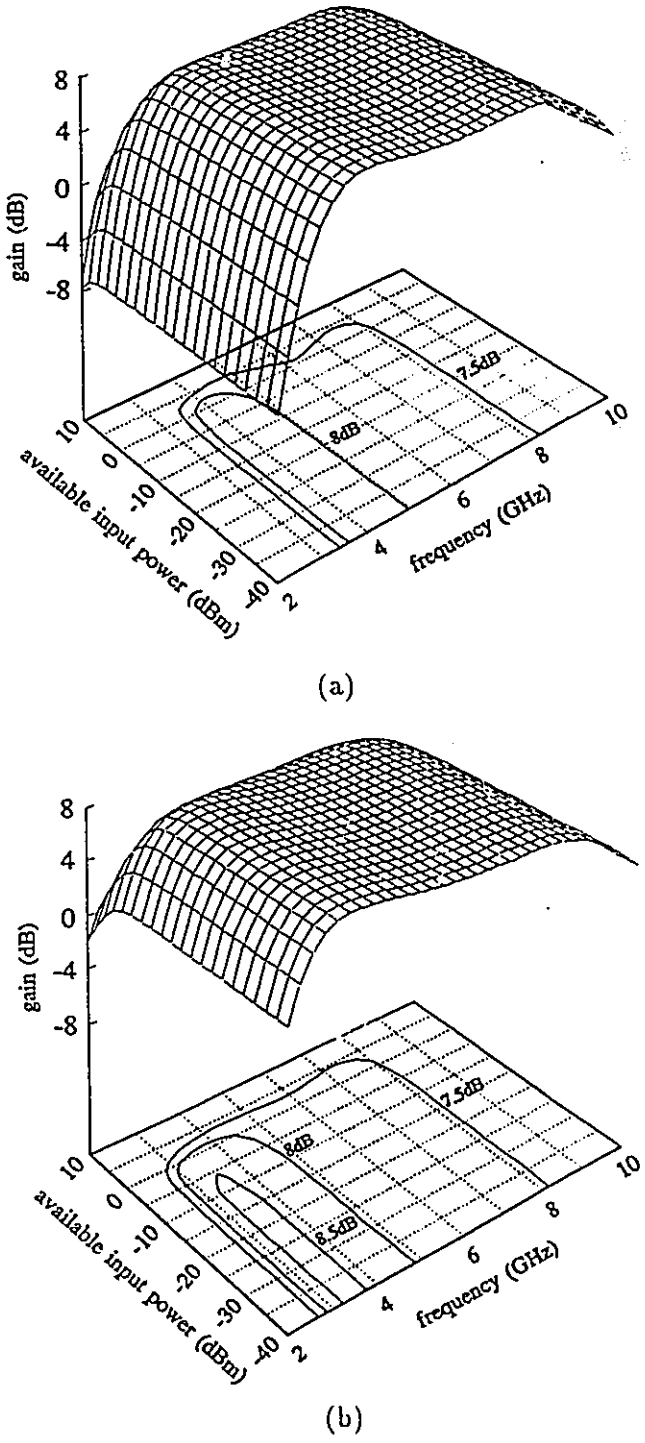
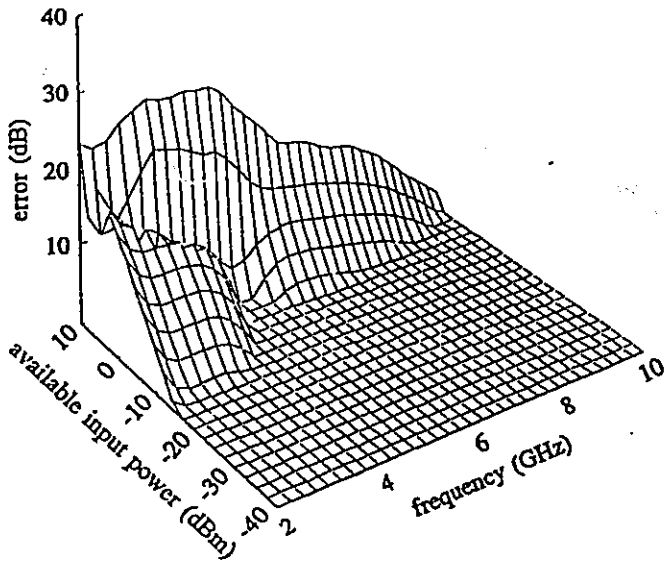
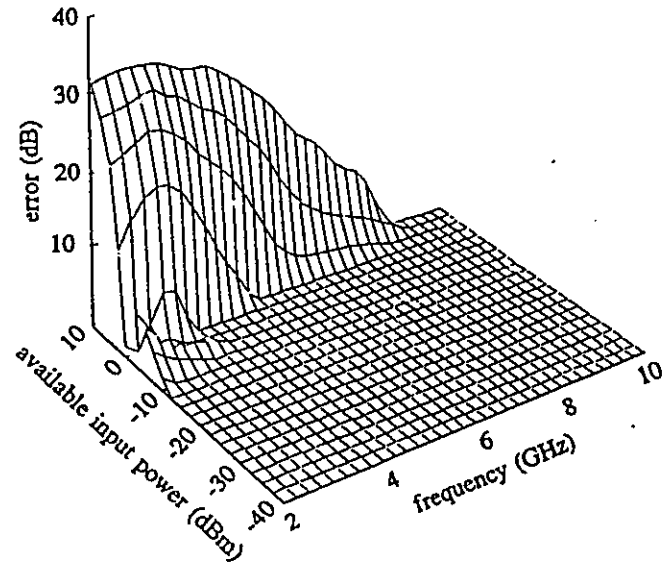


Figure 6.14: (a) The gain response surface simulated at the solution obtained by small-signal design. (b) The gain response surface simulated at the solution obtained by simultaneous small- and large-signal design. Contours indicate the specification of 8 ± 0.5dB.



(a)



(b)

Figure 6.15: The error surfaces of the second harmonic output power with respect to the design specification. (a) Simulation at the solution obtained by conventional small-signal design. (b) Simulation at the solution by simultaneous small- and large-signal design.

6.6 CONCLUDING REMARKS

In this chapter, we have presented the theoretical derivation demonstrating the inherent consistency between DC, small-signal and large-signal simulations. We have shown that DC/small-signal simulation is a special case of the HB simulation. The theoretical basis has been established for simultaneous DC, small-signal and large-signal circuit optimization. Possible applications of the unified circuit design approach have been demonstrated through a FET model parameter extraction example and a small-signal amplifier design example. To sum up, we can see that

1. The unification of small- and large-signal analyses and optimization guarantees designs which simultaneously meet DC/small-signal/large-signal specifications.

2. An expanded set of design variables is permitted. Besides linear elements, design variables can include nonlinear elements, controllable operating parameters, such as bias, etc. Therefore, the nonlinearity of the circuit at different levels can be effectively exploited.

3. Design specifications can be expanded from the traditional frequency dimension into a multidimensional space [2] spanned by frequency, bias, input power, and/or other possible quantities such as temperature, etc.

4. For parameter extraction, the DC, small-signal and large-signal data are explicitly traded off resulting in a model suitable for both small-signal and large-signal applications.

Chapter 7

CONCLUSIONS

This thesis has presented the application of powerful optimization techniques in microwave device modeling and circuit design. Specific attention has been paid to nonlinear circuit simulations. The formulation of the optimization problem has been addressed, including objective functions and their gradient calculations.

In device modeling, or more specifically, nonlinear empirical FET model parameter extraction, we have introduced two new approaches. Different from the conventional approach which extracts model parameters sequentially, the new integrated parameter extraction approach presented in Chapter 3 formulates the modeling process as a complete and integrated optimization problem, simultaneously fitting the DC and small-signal RF responses of the model to the corresponding device measurements. The uniqueness and reliability of the device model have been improved, though an appropriate mathematical form of the nonlinear expressions for the nonlinear FET device model is important to insure a good fit.

The FET model parameter extraction approach presented in Chapter 5 utilizes large-signal multiharmonic measurements. Not only the DC bias and fundamental frequency, but also the input power level are combined to provide measurement data which fully explores the nonlinearity of the FET device. Because the model parameters are extracted from practical nonlinear large-signal operating conditions, the approach is particularly suitable

for nonlinear circuit applications. The success of this large-signal parameter extraction depends on the effectiveness of the nonlinear frequency-domain circuit simulation. To that purpose, we have successfully employed the harmonic balance (HB) simulation technique for this large-signal parameter extraction.

The HB simulation technique as reviewed in Chapter 4 has been considered as a highly efficient nonlinear frequency-domain simulation technique. It is particularly suitable for nonlinear microwave circuit simulation, because there are usually a few nonlinear active devices in the circuit and only a few harmonics need to be considered in the simulation. The formulation of the HB equation has been reviewed, and the formation of its Jacobian matrix has been illustrated. As part of the HB simulation, a simple approach has been proposed for constructing the linear multiport matrix of the linear part of the circuit. It is efficient and easy to implement, especially useful when the linear matrix needs to be repeatedly updated in circuit optimization.

Another important contribution of this thesis is in the unification of DC/small-signal and the HB nonlinear (large-signal) simulation. As presented in Chapter 6, the inherent relationship between DC/small-signal simulation and the HB nonlinear frequency-domain simulation has been derived in detail. It has been shown that the DC/small-signal simulation is a special case of the HB simulation when the input signal level is sufficiently small. The significant implication of this unification is that consistent device models can be used for DC, small-signal and nonlinear large-signal simulations. Therefore, we have opened a new stage that the circuit can be designed to meet multidimensional specifications, i.e., a single optimization problem can be formulated with error functions from DC, small-signal and large-signal circuit responses. For example, specifications can be expanded from the traditional frequency dimension to dimensions of bias, frequency, input power, temperature, etc.

Two examples have been discussed in Chapter 6 to demonstrate the application of

the unified circuit simulation and optimization. The first one is FET model parameter extraction where the FET model is optimized to fit simultaneously DC, small-signal and large-signal measurements. The model extracted showed good agreement with all DC, small-signal and large-signal measurements, which means a more reliable and comprehensive model for circuit designs. The second example shows the usefulness of the unified circuit design. A small-signal broadband amplifier has been designed using the unified small- and large-signal circuit design concept. The specifications correspondingly were given in both small- and large-signal domain. The upper-end of the dynamic range of the amplifier was effectively extended.

The theoretical results presented in this thesis have been demonstrated by circuit examples and implemented in the microwave CAD system *HarPE* which is being used by the microwave industry. Though the examples shown in this thesis are limited, the principles pioneered in this thesis can be applied to general situations, such as nonlinear model parameter extraction for devices other than FETs. It is felt that this thesis can contribute substantially to the subject of microwave device modeling, of great interest to microwave engineers. It is also felt that a new beginning will be opened for microwave circuit design which employs the higher level design strategy based on the unified circuit simulation and optimization concept.

A number of problems related to the topics in this thesis are worth further research and development.

1. In Chapter 2, we have reviewed physical device modeling of MESFETs. Physical device modeling simulates the device behaviour from device geometrical, material and

process parameters. In contrast with parameter extraction, this approach can characterize the device before it is actually manufactured. In other words, the controllable physical parameters of the device could be design variables in circuit optimization. This is of particular importance to the monolithic microwave integrated circuit (MMIC) design. Considering the quasi-static nature of the present Khatibzadeh and Trew model [38] and the extremely computationally intensive 2-dimensional physical model, it would be of great interest to microwave engineers that a sufficiently accurate and computationally efficient physics based FET model be developed. It may be achieved either by a new model, a novel implementation to achieve efficiency, advances in computer technology, or the combination of them. With such a model, a circuit design would not only be able to optimizable linear elements, but also active devices. Therefore we would have more flexibility to achieve an optimum design.

2. Yield-driven or cost-driven circuit design has become increasingly important. To perform yield- or cost-driven circuit design, we must have valid statistical device models. For example, statistical FET models at the equivalent circuit level and measurement data level have been seen in the literature. However, such approaches either have difficulty to correctly reflect the statistical behaviour of the device or need a very large data base to keep all the individual equivalent circuit models or samples extracted from the measurement data sets. Further, there is no obvious connection between the model and the physical parameters where the statistics occur. Initial investigations have been conducted by Bandler, Biernacki, Chen, Song, Ye and Zhang [22] to employ a physics based MESFET model for statistical device modeling. Promising results have been obtained. It would be valuable to continue the research on physics based statistical device modeling, including active and passive devices, to substantially improve the design quality and provide useful information for the manufacturing process. One

crucial question in this research direction is that reliable and efficient physical device models should be developed, such that the model could be employed for practical circuit design.

3. Another aspect of FET device modeling is its noise modeling. In microwave circuit design, low noise is an important feature to pursue. The noise figure of a FET device depends not only on its model parameters but also on its operating conditions, i.e., the noise model should be bias and frequency dependent. An accurate nonlinear bias/frequency dependent noise model would be necessary to reach an optimum low noise figure for the circuit. Furthermore, it would be desirable to relate the the device noise properties with the device physical parameters. There is literature on this subject. But further investigation is needed.

4. In Chapter 6 we have theoretically described the unified circuit simulation. With such a consistent simulation and, therefore, optimization capability, a much more comprehensive circuit design can be achieved. The potential of the circuit can be fully exploited to reach the optimum, especially for circuits with nonlinear active devices. In the Example 2 of Chapter 6, we demonstrated a small-signal broadband amplifier design, where we used the harmonic output power to express the gain of the circuit. It would be of interest to further explore the application of this unified circuit design. Accurate device models which might be bias, frequency, or temperature dependent would be employed. It would be very useful to derivate formulas of various specifications expressed in different working environments.

5. The HB technique has received great interest. However, research to improve the HB technique is still a very important subject to microwave engineering. For example,

   - it should be possible to apply sparse matrix techniques to reduce the memory

requirement and improve efficiency;

- we may apply the unified DC, small-signal and large-signal simulation concept to assure a good starting point for HB simulation, because we may start from DC and multiharmonic small-signal simulation, and sequentially extrapolate the solution when we increase the input power. It would be of interest to investigate the effects of different extrapolation schemes on the HB equation convergence, etc.

Appendix A

CIRCUIT AND DATA FILES

In preparing the numerical examples used in the thesis, we have used *HarPE* [36]. The circuit files and data files presented here are in *HarPE* accepted forms.

A.1 CIRCUIT AND DATA FILES FOR EXAMPLES IN CHAPTER 3

A.1.1 Case 1

A. The Circuit File Before Optimization

```
!  Example  ex11_p2.ckt
!  nonlinear FET model parameter extraction using DC and S parameter
!  measurements with DC constraints.
!  Model used: Materka and Kacprzak nonlinear FET model.
!
Model

   Extrinsic2     1 2 3 4 5

    LG:   ?0.1NH?      RG :  ?0.001 0.2 10?    RD:   ?0.001 0.7 10?
    LD:   ?0.04NH?     RS :  ?0.001 0.8 10?    LS:   ?0.015NH?
    GDS:  ?0.001?      CX :  2.0PF             CDS:  ?0.3PF ?;

   FETM      1 2 3

    IDSS:  ?0.19?     VP0:  ?-4.0?   GAMMA:  ?-0.3?
    E:     ?1.2 ?     KE:   ?0.02?   SL:     ?0.35?
    KG:    ?-0.2?     TAU:  ?3.0ps?  SS:     ?0.004?
    IG0:   0.5E-10    ALPHAG: 20     IB0:    0.5E-10   ALPHAB: 1  VBC: 20
    R10:   ?5.0?     KR: ? 0.05?
    C10:   ?0.4PF?   K1: ? 0.40?     C1S: ?0.01PF?
    CF0:   ?0.03PF?  KF: ?-0.05?;

  2por    4  5;
```

```
end

Data
  #include "spar_1.dat"
end

Sweep
! S-parameter simulation

  FREQ: from 2GHZ to 18ghz step=1ghz VG: 0.0 -1.74 -3.1  VD: 4;

! DC IV simulation

  VG: 0.0 -0.44 -0.88 -1.32 -1.74 -2.2 -2.65 -3.1 VD: from 0 to 6 n=30;

end

Specification
! AC specification

  FREQ: from 2GHZ to 18GHZ step 2GHZ VG: 0.0   VD: 4
        RS11 IS11 RS21 IS21 RS12 IS12 RS22 IS22;
  FREQ: from 2GHZ to 18GHZ step 2GHZ VG: -1.74 VD: 4
        RS11 IS11 RS21 IS21 RS12 IS12 RS22 IS22;
  FREQ: from 2GHZ to 18GHZ step 2GHZ VG: -3.1  VD: 4
        RS11 IS11 RS21 IS21 RS12 IS12 RS22 IS22;

! DC specification

  VG: 0.0 -1.74 -3.1 VD: 4  ID W=25;

end
```

B. The Circuit File After Optimization

```
!  Example  ex11_p2.11
!  nonlinear FET model parameter extraction using DC and S parameter
!  measurements with DC constraints.
!  Model used: Materka and Kacprzak nonlinear FET model.
!
Model

   Extrinsic2     1 2 3 4 5

    LG:  ?0.126737NH?    RG : ?0.001 0.001 10?    RD:  ?0.001 0.333231 10?
    LD:  ?0.0629551NH?   RS : ?0.001 0.383313 10? LS:  ?0.0117648NH?
    GDS: ?0.000262994?   CX : 2.0PF               CDS: ?0.191975PF ?;

   FETM     1 2 3

    IDSS: ?0.163632?   VPO:  ?-3.7257?    GAMMA: ?-0.181157?
    E:   ?1.41297 ?    KE:   ?0.04926?    SL:    ?0.417197?
    KG:  ?-0.125549?   TAU:  ?3.67149ps?  SS:    ?0.00443111?
    IG0: 0.5E-10       ALPHAG: 20      IB0:  0.5E-10   ALPHAB: 1  VBC: 20
    R10: ?4.24146?     KR: ? 0.00743649?
    C10: ?0.596486PF?  K1: ? 0.732501?    C1S: ?0.000902093PF?
```

```
    CFO: ?0.0225464PF? KF: ?-0.127494?;

  2por    4  5;

end

Data
#include "spar_1.dat"
end

Sweep
! S-parameter simulation

  FREQ: from 2GHZ to 18ghz step=1ghz VG: 0.0 -1.74 -3.1  VD: 4;

! DC IV simulation

  VG: 0.0 -0.44 -0.88 -1.32 -1.74 -2.2 -2.65 -3.1 VD: from 0 to 6 n=30;

end

Specification
! AC specification

  FREQ: from 2GHZ to 18GHZ step 2GHZ VG: 0.0   VD: 4
        RS11 IS11 RS21 IS21 RS12 IS12 RS22 IS22;
  FREQ: from 2GHZ to 18GHZ step 2GHZ VG: -1.74 VD: 4
        RS11 IS11 RS21 IS21 RS12 IS12 RS22 IS22;
  FREQ: from 2GHZ to 18GHZ step 2GHZ VG: -3.1  VD: 4
        RS11 IS11 RS21 IS21 RS12 IS12 RS22 IS22;

!DC specification

  VG: 0.0 -1.74 -3.1 VD: 4  ID W=25;

end
```

C. Data File [56]

```
! FILE: SPAR1.DAT
! SEPT. 30/88
! 4V VDS/0V VGS/177MA IDS
!                              S-PARAMETERS
parameter vg=0 vd=4;
format freq(GHz) MS11 PS11 MS21 PS21  MS12   PS12    MS22    PS22;
  2 0.9546  -46.72  4.0405  145.54  0.0291   62.95  0.6010  -21.43
  3 0.9392  -66.98  3.6149  129.27  0.0388   52.47  0.5808  -32.82
  4 0.8944  -83.24  3.3323  118.50  0.0458   42.58  0.5718  -39.93
  5 0.8789  -97.95  2.9539  102.85  0.0507   33.91  0.5701  -48.94
  6 0.8598 -108.88  2.6428   95.28  0.0518   28.76  0.5808  -54.82
  7 0.8460 -120.97  2.2946   82.85  0.0517   18.44  0.5683  -63.42
  8 0.8388 -127.78  2.0989   78.94  0.0503   18.99  0.5845  -68.54
  9 0.8340 -137.66  1.9225   67.49  0.0505   12.84  0.5867  -75.58
 10 0.8350 -143.32  1.7984   58.95  0.0525   10.51  0.6089  -79.69
 11 0.8326 -149.51  1.5910   56.35  0.0499   12.37  0.6166  -83.21
 12 0.8326 -155.26  1.5106   46.49  0.0507    6.11  0.6360  -91.66
 13 0.8196 -161.01  1.3838   40.82  0.0473    8.76  0.6427  -93.39
```

```
 14 0.8301 -166.19  1.2945   34.54  0.0466    4.40  0.6633 -101.10
 15 0.8242 -172.00  1.1615   24.82  0.0442    3.98  0.6718 -106.42
 16 0.8332 -174.63  1.1335   23.98  0.0436    7.27  0.6845 -108.67
 17 0.8190 -179.96  0.9365   11.88  0.0408    5.08  0.7045 -113.75
 18 0.8394 -180.64  0.9688    8.12  0.0420    6.08  0.7098 -115.22

parameter vg=-1.74 vd=4;
format freq(GHz) MS11 PS11 MS21 PS21  MS12   PS12    MS22   PS22;
  2 0.9585  -36.75  3.1389  150.53  0.0408   66.80  0.5439  -23.91
  3 0.9457  -54.12  2.8906  135.84  0.0567   56.58  0.5303  -36.95
  4 0.9004  -67.99  2.7296  125.90  0.0688   47.29  0.5204  -45.35
  5 0.8847  -82.22  2.4969  111.25  0.0787   37.94  0.5232  -55.70
  6 0.8597  -92.49  2.2895  103.05  0.0836   32.18  0.5309  -62.13
  7 0.8375 -104.76  2.0371   91.36  0.0868   21.53  0.5177  -71.76
  8 0.8262 -111.74  1.8851   86.36  0.0873   20.33  0.5312  -76.63
  9 0.8144 -122.27  1.7462   75.87  0.0896   12.49  0.5321  -84.21
 10 0.8145 -128.60  1.6536   66.69  0.0951    9.33  0.5543  -88.84
 11 0.8080 -134.73  1.4918   64.58  0.0906    7.99  0.5553  -92.92
 12 0.8023 -141.64  1.4118   53.94  0.0942    0.67  0.5692  -99.86
 13 0.7920 -146.83  1.3213   49.51  0.0890    0.20  0.5759 -102.41
 14 0.8003 -153.41  1.2339   42.40  0.0905   -5.70  0.5958 -109.06
 15 0.7885 -159.07  1.1325   33.85  0.0856   -8.18  0.6067 -114.76
 16 0.7926 -162.96  1.0965   32.61  0.0857   -9.30  0.6098 -115.86
 17 0.7871 -167.84  0.9808   21.65  0.0811  -13.31  0.6270 -121.67
 18 0.7972 -169.40  0.9671   20.98  0.0799  -14.38  0.6318 -120.02

parameter vg=-3.1 vd=4;
format freq(GHz) MS11 PS11 MS21 PS21   MS12   PS12    MS22   PS22;
  2   .9614  -32.46  2.5494  152.25   .0491   68.66   .5383  -24.26
  3   .9490  -48.34  2.3749  138.14   .0691   58.95   .5287  -37.94
  4   .9026  -60.84  2.2681  128.46   .0853   49.75   .5227  -46.46
  5   .8840  -74.37  2.1038  114.14   .0993   40.23   .5255  -57.50
  6   .8604  -84.23  1.9597  105.74   .1070   34.70   .5312  -64.10
  7   .8324  -96.28  1.7474   93.93   .1124   23.84   .5203  -74.55
  8   .8145 -103.10  1.6293   88.90   .1147   22.02   .5292  -79.12
  9   .7972 -113.68  1.5213   78.38   .1191   13.54   .5331  -87.56
 10   .7953 -120.22  1.4587   68.97   .1275    9.82   .5479  -91.61
 11   .7859 -126.03  1.3230   66.72   .1225    8.00   .5523  -96.66
 12   .7767 -133.54  1.2602   55.70   .1286     .46   .5566 -102.75
 13   .7621 -138.24  1.1803   51.49   .1214   -1.44   .5681 -108.18
 14   .7681 -145.50  1.1179   44.23   .1252   -7.09   .5876 -111.68
 15   .7587 -151.00  1.0290   35.72   .1211  -10.03   .5939 -117.61
 16   .7610 -155.48  1.0001   33.95   .1213  -12.09   .5907 -118.18
 17   .7570 -160.04   .8957   23.17   .1145  -16.18   .5972 -123.92
 18   .7594 -162.61   .8860   21.81   .1139  -18.16   .6233 -121.86

format vg    vd   id;
       0.0   4.0  0.177
     -1.74   4.0  0.092
     -3.10   4.0  0.037
```

A.1.2 Case 1 — Extended with Simulated Data

A. The Circuit File Before Optimization

```
! Example  ex21_p2.ckt
```

```
!  nonlinear FET model parameter extraction using DC and S parameter
!  measurements with DC constraints.
!  Model used: Materka and Kacprzak nonlinear FET model.
!
Model

   Extrinsic2     1 2 3 4 5

    LG:   ?0.1NH?      RG :  ?0.001 0.2 10?    RD:   ?0.001 0.7 10?
    LD:   ?0.04NH?     RS :  ?0.001 0.8 10?    LS:   ?0.015NH?
    GDS:  ?0.001?      CX :  2.0PF             CDS:  ?0.3PF ?;

   FETM      1 2 3

    IDSS:  ?0.19?    VP0:  ?-4.0?   GAMMA:  ?-0.3?
    E:     ?1.2 ?    KE:   ?0.02?   SL:     ?0.35?
    KG:    ?-0.2?    TAU:  ?3.0ps?  SS:     ?0.004?
    IG0:   0.5E-10   ALPHAG: 20     IB0:   0.5E-10   ALPHAB: 1  VBC: 20
    R10:   ?5.0?    KR: ? 0.05?
    C10:   ?0.4PF?  K1: ? 0.40?     C1S: ?0.01PF?
    CF0:   ?0.03PF? KF: ?-0.05?;

  2por    4  5;

end

Data
#include "SPAR_2.DAT"
end

Sweep
! S-parameter simulation

  FREQ: from 2GHZ to 18ghz step=1ghz VG: 0.0 -1.74 -3.1  VD: 4;

! DC IV simulation

  VG: 0.0 -0.44 -0.88 -1.32 -1.74 -2.2 -2.65 -3.1 VD: from 0 to 6 n=30;

end

Specification
! AC specification

  FREQ: from 2GHZ to 18GHZ step 2GHZ VG: 0.0   VD: 4
        RS11 IS11 RS21 IS21 RS12 IS12 RS22 IS22;
  FREQ: from 2GHZ to 18GHZ step 2GHZ VG: -1.74 VD: 4
        RS11 IS11 RS21 IS21 RS12 IS12 RS22 IS22;
  FREQ: from 2GHZ to 18GHZ step 2GHZ VG: -3.1  VD: 4
        RS11 IS11 RS21 IS21 RS12 IS12 RS22 IS22;

! DC specification

  VG:    0.     VD: 0.333 0.667 1.0 1.333 4  ID W=25;
  VG: -1.74     VD: 0.333 0.667 1.0 1.333 4  ID W=25;
  VG: -3.10     VD: 0.333 0.667 1.0 1.333 4  ID W=25;

end
```

B. The Circuit File After Optimization

```
!  Example  ex21_p2.11
!  nonlinear FET model parameter extraction using DC and S parameter
!  measurements with DC constraints.
!  Model used: Materka and Kacprzak nonlinear FET model.
!
Model

   Extrinsic2     1 2 3 4 5

    LG:  ?0.128019NH?   RG : ?0.001 0.00100004 10?  RD: ?0.001 0.386245 10?
    LD:  ?0.0630276NH?  RS : ?0.001 0.377397 10?    LS: ?0.0117225NH?
    GDS: ?0.000241532?  CX : 2.0PF                  CDS: ?0.191869PF ?;

   FETM     1 2 3

       IDSS: ?0.163183?   VPO:  ?-3.72591?   GAMMA:  ?-0.182544?
       E:    ?1.40776 ?   KE:   ?0.04744?    SL:     ?0.418858?
       KG:   ?-0.127857?  TAU:  ?3.61612ps?  SS:     ?0.00444728?
       IGO: 0.5E-10      ALPHAG: 20      IBO: 0.5E-10   ALPHAB: 1  VBC: 20
       R10: ?4.36605?     KR: ? 2.89814e-05?
       C10: ?0.593941PF?  K1: ? 0.737071?     C1S: ?0.00176953PF?
       CFO: ?0.0225293PF? KF: ?-0.12673?;

  2por    4  5;

end

Data
  #include "SPAR_2.DAT"
end

Sweep
! S-parameter simulation

  FREQ: from 2GHZ to 18ghz step=1ghz VG: 0.0 -1.74 -3.1  VD: 4;

! DC IV simulation

  VG: 0.0 -0.44 -0.88 -1.32 -1.74 -2.2 -2.65 -3.1 VD: from 0 to 6 n=30;

end

Specification
! AC specification

  FREQ: from 2GHZ to 18GHZ step 2GHZ VG: 0.0   VD: 4
        RS11 IS11 RS21 IS21 RS12 IS12 RS22 IS22;
  FREQ: from 2GHZ to 18GHZ step 2GHZ VG: -1.74 VD: 4
        RS11 IS11 RS21 IS21 RS12 IS12 RS22 IS22;
  FREQ: from 2GHZ to 18GHZ step 2GHZ VG: -3.1  VD: 4
        RS11 IS11 RS21 IS21 RS12 IS12 RS22 IS22;

! DC specification

  VG:    0.     VD: 0.333 0.667 1.0 1.333 4  ID W=25;
  VG: -1.74     VD: 0.333 0.667 1.0 1.333 4  ID W=25;
```

```
  VG: -3.10      VD: 0.333 0.667 1.0 1.333 4  ID W=25;

end
```

C. Data File [56]

```
! FILE: SPAR_2.DAT
! SEPT. 30/88
! 4V VDS/0V VGS/177MA IDS
!                                S-PARAMETERS
parameter vg=0 vd=4;
format freq(GHz) MS11 PS11 MS21 PS21  MS12   PS12    MS22   PS22;
  2 0.9546  -46.72  4.0405  145.54  0.0291   62.95  0.6010  -21.43
  3 0.9392  -66.98  3.6149  129.27  0.0388   52.47  0.5808  -32.82
  4 0.8944  -83.24  3.3323  118.50  0.0458   42.58  0.5718  -39.93
  5 0.8789  -97.95  2.9539  102.85  0.0507   33.91  0.5701  -48.94
  6 0.8598 -108.88  2.6428   95.28  0.0518   28.76  0.5808  -54.82
  7 0.8460 -120.97  2.2946   82.85  0.0517   18.44  0.5683  -63.42
  8 0.8388 -127.78  2.0989   78.94  0.0503   18.99  0.5845  -68.54
  9 0.8340 -137.66  1.9225   67.49  0.0505   12.84  0.5867  -75.58
 10 0.8350 -143.32  1.7984   58.95  0.0525   10.51  0.6089  -79.69
 11 0.8326 -149.51  1.5910   56.35  0.0499   12.37  0.6166  -83.21
 12 0.8326 -155.26  1.5106   46.49  0.0507    6.11  0.6360  -91.66
 13 0.8196 -161.01  1.3838   40.82  0.0473    8.76  0.6427  -93.39
 14 0.8301 -166.19  1.2945   34.54  0.0466    4.40  0.6633 -101.10
 15 0.8242 -172.00  1.1615   24.82  0.0442    3.98  0.6718 -106.42
 16 0.8332 -174.63  1.1335   23.98  0.0436    7.27  0.6845 -108.67
 17 0.8190 -179.96  0.9365   11.88  0.0408    5.08  0.7045 -113.75
 18 0.8394 -180.64  0.9688    8.12  0.0420    6.08  0.7098 -115.22

parameter vg=-1.74 vd=4;
format freq(GHz) MS11 PS11 MS21 PS21  MS12   PS12    MS22   PS22;
  2 0.9585  -36.75  3.1389  150.53  0.0408   66.80  0.5439  -23.91
  3 0.9457  -54.12  2.8906  135.84  0.0567   56.58  0.5303  -36.95
  4 0.9004  -67.99  2.7296  125.90  0.0688   47.29  0.5204  -45.35
  5 0.8847  -82.22  2.4969  111.25  0.0787   37.94  0.5232  -55.70
  6 0.8597  -92.49  2.2895  103.05  0.0836   32.18  0.5309  -62.18
  7 0.8375 -104.76  2.0371   91.36  0.0868   21.53  0.5177  -71.76
  8 0.8262 -111.74  1.8851   86.36  0.0873   20.33  0.5312  -76.63
  9 0.8144 -122.27  1.7462   75.87  0.0896   12.49  0.5321  -84.21
 10 0.8145 -128.60  1.6536   66.69  0.0951    9.33  0.5543  -88.84
 11 0.8080 -134.73  1.4918   64.58  0.0906    7.99  0.5553  -92.92
 12 0.8023 -141.64  1.4118   53.94  0.0942    0.67  0.5692  -99.86
 13 0.7920 -146.83  1.3213   49.51  0.0896    0.20  0.5759 -102.41
 14 0.8003 -153.41  1.2339   42.40  0.0905   -5.70  0.5958 -109.06
 15 0.7885 -159.07  1.1325   33.85  0.0856   -8.18  0.6067 -114.76
 16 0.7926 -162.96  1.0965   32.61  0.0857   -9.32  0.6098 -115.86
 17 0.7871 -167.84  0.9808   21.65  0.0811  -13.31  0.6270 -121.67
 18 0.7972 -169.40  0.9671   20.98  0.0799  -14.38  0.6318 -120.02

parameter vg=-3.1 vd=4;
format freq(GHz) MS11 PS11 MS21 PS21  MS12    PS12    MS22   PS22;
  2  .9614  -32.46  2.5494  152.25   .0491   68.66   .5383  -24.26
  3  .9490  -48.34  2.3749  138.14   .0691   58.95   .5287  -37.94
  4  .9026  -60.84  2.2681  128.46   .0853   49.75   .5227  -46.46
  5  .8840  -74.37  2.1038  114.14   .0993   40.23   .5255  -57.50
  6  .8604  -84.23  1.9597  105.74   .1070   34.70   .5312  -64.10
```

```
  7  .8324  -96.28  1.7474   93.93   .1124   23.84   .5203  -74.55
  8  .8145 -103.10  1.6293   88.90   .1147   22.02   .5292  -79.12
  9  .7972 -113.68  1.5213   78.38   .1191   13.54   .5331  -87.56
 10  .7953 -120.22  1.4587   68.97   .1275    9.82   .5479  -91.61
 11  .7859 -126.03  1.3230   66.72   .1225    8.00   .5523  -96.66
 12  .7767 -133.54  1.2602   55.70   .1286     .46   .5566 -102.75
 13  .7621 -138.24  1.1803   51.49   .1214   -1.44   .5681 -108.18
 14  .7681 -145.50  1.1179   44.23   .1252   -7.09   .5876 -111.68
 15  .7587 -151.00  1.0290   35.72   .1211  -10.03   .5939 -117.61
 16  .7610 -155.48  1.0001   33.95   .1213  -12.09   .5907 -118.18
 17  .7570 -160.04   .8957   23.17   .1145  -16.18   .5972 -123.92
 18  .7594 -162.61   .8860   21.81   .1139  -18.16   .6233 -121.86

format vg    vd   id;
       0.0   4.0  0.177
      -1.74  4.0  0.092
      -3.10  4.0  0.037

! HarPE Version 1.4 for HP 9000/300 workstations
! Circuit File: /users/shen/harpe/thesis/ex11/ex11_p2.11
! Thu Sep 27 20:43:51 1990
! DC Data (I-V Characteristics)
!
! PARAMETER VG=0V;
! FORMAT VD(V) ID(mA);
    0    0.0000          0
    0    0.1667       0.052
    0    0.3333       0.095
    0    0.5000       0.126
    0    0.6667       0.145
    0    0.8333       0.155
    0    1.0000       0.160
    0    1.1667       0.163
    0    1.3333       0.164

! PARAMETER VG=-1.74V;
! FORMAT VD(V) ID(mA);
   -1.74    0.0000          00
   -1.74    0.1667      0.0313
   -1.74    0.3333      0.0536
   -1.74    0.5000      0.0654
   -1.74    0.6667      0.0708
   -1.74    0.8333      0.0734
   -1.74    1.0000      0.0749
   -1.74    1.1667      0.0761
   -1.74    1.3333      0.0771

! PARAMETER VG=-3.1V;
! FORMAT VD(V) ID(mA);
   -3.1     0.0000          00
   -3.1     0.1667      0.0104
   -3.1     0.3333      0.0164
   -3.1     0.5000      0.0191
   -3.1     0.6667      0.0205
   -3.1     0.8333      0.0216
   -3.1     1.0000      0.0226
   -3.1     1.1667      0.0235
   -3.1     1.3333      0.0245
```

A.1.3 Case 2

A. The Circuit File Before Optimization

```
!
!  Example  small.ckt
!  nonlinear FET model parameter extraction using DC and S parameter
!  measurements with DC constraints.
!  Model used: Curtice nonlinear FET model.
!
Model

   Extrinsic2     1 2 3 4 5

        LG:   ?0.3NH?      RG:   ?0.01 4 10?        RD:   ?0.01 0.5 10?
        LD:   ?0.2NH?      RS:   ?0.01 2 10?        LS:   ?0.08NH?
        GDS:  ?0.2e-3?     CX:   ?1.5PF?            CDS:  ?0.1PF?
        CGE:  ?0.01PF?     CDE:  ?0.01PF?;
   FETC     1 2 3

       A0:    ?0  0.15   0.3?  A1:   ? 0.15 ?
       A2:    ? -0.02?         A3:   ?-0.02?
       GAMMA: ? 1 ?            BETA: ?0.03?             TAU: ?3PS?
       VDS0:  ?0  2 6?         IS:   1e-14              N:   ?1?
       CGS0:  ? 0.5PF?         CGD0: ?0.092PF?          FC : ?0.7 ?
       GMIN:  1.0E-07          VLI:  ?0.8?              VBR:  30 ;

  2por    4  5;

end

Data
#include "spar_3.dat"
end

Sweep
! S-parameter simulation

  FREQ: from 1GHZ to 15ghz step=1ghz VG: -0.361 VD: 2;
  FREQ: from 1ghz to 15ghz step=1ghz VG: -0.667 VD: 4;
  FREQ: from 1ghz to 15ghz step=1ghz VG: -1.062 VD: 6;

! DC IV simulation

  VG: -1.062 -0.667 -0.361 VD: from 0 to 8 n=20;

end

Specification
! AC specification

  FREQ: 1GHZ 3ghz 5ghz 7ghz 9ghz 11ghz 13ghz 15GHZ VG: -0.361 VD: 2
        RS11 IS11 RS21 IS21 RS12 IS12 RS22 IS22;
  FREQ: 1GHZ 3ghz 5ghz 7ghz 9ghz 11ghz 13ghz 15GHZ VG: -0.667 VD: 4
        RS11 IS11 RS21 IS21 RS12 IS12 RS22 IS22;
  FREQ: 1GHZ 3GHZ 5GHZ 7GHZ 9GHZ 11GHZ 13GHZ 15GHZ VG: -1.062 VD: 6
        RS11 IS11 RS21 IS21 RS12 IS12 RS22 IS22;
```

```
! DC specification
  VG: -0.361 VD: 2 ID w=20;
  VG: -0.667 VD: 4 ID w=20;
  VG: -1.062 VD: 6 ID w=20;

end
```

B. The Circuit File After Optimization

```
!
!  Example  small.12
!  nonlinear FET model parameter extraction using DC and S parameter
!  measurements with DC constraints.
!  Model used: Curtice nonlinear FET model.
!
Model

   Extrinsic2     1 2 3 4 5

       LG:   ?0.352492NH?     RG:  ?0.01 5.7407 10?   RD:   ?0.01 0.01 10?
       LD:   ?0.306222NH?     RS:  ?0.01 3.60413 10?  LS:   ?0.0774401NH?
       GDS:  ?0.00218366?     CX:  ?1.88423PF?        CDS:  ?0.0977131PF?
       CGE:  ?0.00375491PF?   CDE: ?0.00495952PF?;

   FETC      1 2 3

       A0:    ?0  0.0957286   0.3?  A1:    ? 0.0969376 ?
       A2:    ? -0.0101484?         A3:    ?-0.0251131?
       GAMMA: ? 1.06983 ?           BETA: ?0.0382614?   TAU: ?3.1821PS?
       VDSO:  ?0  1.78158 6?        IS:   1e-14         N:   ?1?
       CGSO:  ? 0.614364PF?         CGDO: ?0.0783114PF? FC : ?0.7 ?
       GMIN:  1.0E-07               VBI:  ?0.799076?    VBR:  30 ;

  2por    4  5;

end

Data
#include "spar_3.dat"
end

Sweep
! S-parameter simulation

  FREQ: from 1GHZ to 15ghz step=1ghz VG: -0.361 VD: 2;
  FREQ: from 1ghz to 15ghz step=1ghz VG: -0.667 VD: 4;
  FREQ: from 1ghz to 15ghz step=1ghz VG: -1.062 VD: 6;

! DC IV simulation

  VG: -1.062 -0.667 -0.361 VD: from 0 to 8 n=20;

end

Specification
! AC specification
```

```
  FREQ: 1GHZ 3ghz 5ghz 7ghz 9ghz 11ghz 13ghz 15GHZ VG: -0.361 VD: 2
        RS11 IS11 RS21 IS21 RS12 IS12 RS22 IS22;
  FREQ: 1GHZ 3ghz 5ghz 7ghz 9ghz 11ghz 13ghz 15GHZ VG: -0.667 VD: 4
        RS11 IS11 RS21 IS21 RS12 IS12 RS22 IS22;
  FREQ: 1GHZ 3GHZ 5GHZ 7GHZ 9GHZ 11GHZ 13GHZ 15GHZ VG: -1.062 VD: 6
        RS11 IS11 RS21 IS21 RS12 IS12 RS22 IS22;

! DC specification
  VG: -0.361 VD: 2 ID w=20;
  VG: -0.667 VD: 4 ID w=20;
  VG: -1.062 VD: 6 ID w=20;

end
```

C. Data File [69]

```
! File: spar_3.dat
!       S-parameter and DC measurement at 3 bias points
!
PARAMETER VG =-.361  VD=2  ;
FORMAT FREQ MS11  PS11    MS21    PS21     MS12    PS12     MS22  PS22 ;
 1.000GHZ  .979  -22.5   5.0751   162.3    .0256    79.0    .545  -11.8
 2.000GHZ  .934  -42.2   4.7006   146.2    .0469    67.9    .523  -22.9
 3.000GHZ  .878  -58.9   4.2603   132.1    .0629    60.0    .503  -28.3
 4.000GHZ  .807  -75.3   3.9184   119.0    .0773    52.4    .470  -37.1
 5.000GHZ  .762  -91.2   3.6107   107.5    .0885    47.3    .434  -41.9
 6.000GHZ  .700 -106.8   3.3358    96.2    .0987    41.9    .396  -48.8
 7.000GHZ  .666 -122.3   3.0926    86.1    .1063    38.0    .356  -53.5
 8.000GHZ  .629 -138.8   2.8748    75.5    .1128    33.5    .308  -62.2
 9.000GHZ  .609 -153.6   2.6407    66.5    .1182    30.4    .272  -68.7
10.000GHZ  .605 -168.7   2.4540    57.5    .1230    26.8    .224  -80.3
11.000GHZ  .608  179.0   2.2632    48.9    .1267    24.1    .198  -92.9
12.000GHZ  .612  166.9   2.0907    41.3    .1315    22.1    .180 -111.8
13.000GHZ  .624  157.9   1.9134    33.4    .1351    20.1    .178 -123.9
14.000GHZ  .637  149.9   1.7770    27.6    .1419    18.7    .188 -144.4
15.000GHZ  .631  143.8   1.6584    20.3    .1481    17.9    .218 -146.9
!16.000GHZ  .636  139.0   1.5500    15.7    .1588    17.2    .217 -158.3
!17.000GHZ  .620  134.3   1.4801     9.7    .1710    16.8    .257 -157.6
!18.000GHZ  .607  130.7   1.4068     5.3    .1872    16.0    .240 -159.4
!19.000GHZ  .594  123.9   1.3722     -.7    .2078    15.6    .268 -161.7
!20.000GHZ  .569  119.3   1.3164    -5.0    .2320    13.3    .251 -161.4

PARAMETER VG = -.667  VD=4;
FORMAT FREQ MS11  PS11    MS21    PS21     MS12    PS12     MS22  PS22;
 1.000GHZ  .983  -20.2   4.5734   163.5    .0187    80.2    .675   -8.7
 2.000GHZ  .945  -38.1   4.2792   148.5    .0344    70.4    .659  -17.1
 3.000GHZ  .898  -53.4   3.9170   135.0    .0459    63.3    .642  -21.5
 4.000GHZ  .830  -68.4   3.6557   122.4    .0574    56.4    .623  -28.4
 5.000GHZ  .787  -83.2   3.4163   111.1    .0657    52.4    .592  -32.0
 6.000GHZ  .723  -97.8   3.2070   100.0    .0734    47.4    .568  -37.1
 7.000GHZ  .683 -112.8   3.0142    90.0    .0791    44.4    .534  -40.7
 8.000GHZ  .638 -128.7   2.8536    79.4    .0846    40.9    .497  -46.3
 9.000GHZ  .609 -143.9   2.6537    70.1    .0891    38.8    .465  -51.1
10.000GHZ  .598 -159.5   2.5056    60.6    .0935    36.7    .423  -57.3
11.000GHZ  .597 -172.7   2.3270    51.5    .0960    35.0    .390  -65.5
```

```
12.000GHZ  .601  174.7   2.1758    43.3    .1024    34.0    .362  -75.3
13.000GHZ  .614  165.1   2.0045    35.0    .1063    33.4    .351  -84.4
14.000GHZ  .627  157.2   1.8696    28.6    .1134    32.5    .329  -97.2
15.000GHZ  .622  151.0   1.7376    20.6    .1216    31.7    .367 -106.5
!16.000GHZ  .625  146.2   1.6303    15.8    .1331    31.9    .349 -113.8
!17.000GHZ  .611  141.6   1.5467     9.2    .1456    32.0    .401 -120.8
!18.000GHZ  .596  138.0   1.4606     5.0    .1644    31.9    .396 -121.7
!19.000GHZ  .582  132.6   1.4213     -.7    .1852    32.2    .425 -126.9
!20.000GHZ  .554  127.7   1.3582    -4.8    .2130    30.0    .418 -127.7

PARAMETER VG=-1.062  VD=6;
FORMAT FREQ MS11  PS11   MS21     PS21     MS12    PS12     MS22  PS22;
 1.000GHZ  .985  -17.0   3.1547   165.5   .0170    80.8    .711   -7.2
 2.000GHZ  .959  -32.4   3.0073   151.8   .0318    72.6    .702  -14.8
 3.000GHZ  .928  -45.8   2.8134   139.2   .0433    65.6    .691  -18.8
 4.000GHZ  .873  -59.5   2.6908   126.9   .0545    58.9    .681  -25.5
 5.000GHZ  .840  -73.1   2.5725   116.0   .0633    54.5    .654  -29.0
 6.000GHZ  .783  -86.7   2.4720   104.9   .0718    49.3    .638  -34.5
 7.000GHZ  .744 -100.7   2.3723    94.7   .0777    45.9    .608  -37.9
 8.000GHZ  .698 -115.6   2.2970    83.8   .0840    41.7    .577  -43.7
 9.000GHZ  .661 -130.3   2.1698    73.9   .0882    38.7    .550  -48.4
10.000GHZ  .638 -145.6   2.0892    64.0   .0921    36.3    .515  -54.1
11.000GHZ  .629 -159.1   1.9755    54.2   .0943    34.3    .485  -61.7
12.000GHZ  .619 -172.5   1.8688    45.4   .0987    33.2    .460  -70.2
13.000GHZ  .625  176.4   1.7409    36.2   .1016    31.7    .447  -78.4
14.000GHZ  .631  166.7   1.6368    28.8   .1084    30.7    .421  -89.2
15.000GHZ  .630  159.1   1.5321    20.3   .1138    31.0    .454  -98.3
!16.000GHZ  .633  153.2   1.4356    14.6    .1232    31.8    .430 -105.6
!17.000GHZ  .624  147.9   1.3622     7.5    .1335    31.8    .478 -113.8
!18.000GHZ  .610  143.3   1.2863     2.8    .1499    32.4    .473 -116.4
!19.000GHZ  .600  136.3   1.2522    -3.6    .1689    33.2    .498 -122.7
!20.000GHZ  .574  130.8   1.1922    -7.9    .1938    31.9    .499 -124.9

FORMAT   VG     VD  ID(MA);
       -.361    2    45.3
       -.667    4    30
      -1.062    6    15
```

A.2 CIRCUIT AND DATA FILES FOR EXAMPLES IN CHAPTER 5

A.2.1 Case 3

A. The Circuit File Before Optimization

```
!
!  Example  large.ckt
!  nonlinear FET model parameter extraction using large-signal power
!  spectrum measurements.
!  Model used: Curtice nonlinear FET model.
!
Model
```

```
  Extrinsic2     1 2 3 4 5

     LG:   ?0.3NH?      RG:   ?0.01 4 10?        RD:   ?0.01 0.5 10?
     LD:   ?0.2NH?      RS:   ?0.01 2 10?        LS:   ?0.08NH?
     GDS:  ?0.2e-3?     CX:   ?1.5PF?            CDS:  ?0.1PF?
     CGE:  ?0.01PF?     CDE:  ?0.01PF?;

  FETC     1 2 3

     A0:    ?0  0.15   0.3?  A1:   ? 0.15 ?
     A2:    ? -0.02?         A3:   ?-0.02?
     GAMMA: ? 1 ?            BETA: ?0.03?             TAU: ?3PS?
     VDS0:  ?0  2 6?         IS:   1e-14              N:   ?1?
     CGSC:  ? 0.5PF?         CGD0: ?0.092PF?          FC : ?0.7 ?
     GMIN:  1.0E-07          VBI:  ?0.8?              VBR:  30 ;

  2por    4  5;

end

Data
! power spectrum measurement data
#include "fetb_02.dat"
#include "fetb_2.dat"
#include "fetb_6.dat"
end

Sweep
! HB simulation

  FREQ: 0.2GHZ PIN: from -15DBM to 10DBM step=5DBM   VG: -0.373 VD: 2;
  FREQ: 0.2GHZ PIN: from -15DBM to 10DBM step=5DBM   VG: -0.674 VD: 4;
  FREQ: 0.2GHZ PIN: from -15DBM to 10DBM step=5DBM   VG: -1.072 VD: 6;
  FREQ: 2GHZ   PIN: from -15DBM to 10DBM step=5DBM   VG: -0.363 VD: 2;
  FREQ: 2GHZ   PIN: from -15DBM to 10DBM step=5DBM   VG: -0.667 VD: 4;
  FREQ: 2GHZ   PIN: from -15DBM to 10DBM step=5DBM   VG: -1.070 VD: 6;
  FREQ: 6GHZ   PIN: from -15DBM to 10DBM step=5DBM   VG: -0.372 VD: 2;
  FREQ: 6GHZ   PIN: from -15DBM to 10DBM step=5DBM   VG: -0.673 VD: 4;
  FREQ: 6GHZ   PIN: from -15DBM to 10DBM step=5DBM   VG: -1.073 VD: 6;

! DC IV simulation

  VG: -1.062 -0.667 -0.361 VD: from 0 to 8 n=20;

end

Specification
! Power spectrum specification

  FREQ: 0.2GHZ   PIN: -15DBM -5DBM 5DBM VG: -0.373 VD: 2
                 ID0 POUT1 POUT2 POUT3;
  FREQ: 0.2GHZ   PIN: -15DBM -5DBM 5DBM VG: -1.072 VD: 6
                 ID0 POUT1 POUT2 POUT3;
  FREQ: 6GHZ     PIN: -15DBM -5DBM 5DBM VG: -0.372 VD: 2
                 ID0 POUT1 POUT2 POUT3;
  FREQ: 6GHZ     PIN:  -15DBM -5DBM 5DBM VG: -1.073 VD: 6
                 ID0 POUT1 POUT2 POUT3;
```

```
end
```

B. The Circuit File After Optimization

```
!
!  Example  large.12
!  nonlinear FET model parameter extraction using large-signal power
!  spectrum measurements.
!  Model used: Curtice nonlinear FET model.
!
Model

   Extrinsic2     1 2 3 4 5

       LG:  ?0.217761NH?     RG:  ?0.01 4.02715 10?   RD:  ?0.01 1.54468 10?
       LD:  ?0.372611NH?     RS:  ?0.01 0.701857 10?  LS:  ?0.0448909NH?
       GDS: ?0.00181856?     CX:  ?5.43504PF?         CDS: ?0.244114PF?
       CGE: ?0.010369PF?     CDE: ?0.0109153PF?;

   FETC     1 2 3

       A0:    ?0  0.0729183   0.3?  A1:   ? 0.071381 ?
       A2:    ? -0.00100215?        A3:   ?-0.0108366?
       GAMMA: ? 1.59368 ?           BETA: ?0.0379071?     TAU: ?3.16368PS?
       VDS0:  ?0  1.89835 6?        IS:   1e-14           N:   ?1.38071?
       CGS0:  ? 0.636163PF?         CGD0: ?0.0837511PF?   FC : ?0.758025 ?
       GMIN:  1.0E-07               VBI:  ?0.898689?      VBR:  30 ;

  2por    4  5;

end

Data
! power spectrum measurement data
#include "fetb_02.dat"
#include "fetb_2.dat"
#include "fetb_6.dat"
end

Sweep
! HB simulation

  FREQ: 0.2GHZ PIN: from -15DBM to 10DBM step=5DBM   VG: -0.373 VD: ?;
  FREQ: 0.2GHZ PIN: from -15DBM to 10DBM step=5DBM   VG: -0.674 VD: ?;
  FREQ: 0.2GHZ PIN: from -15DBM to 10DBM step=5DBM   VG: -1.072 VD: 6;
  FREQ: 2GHZ   PIN: from -15DBM to 10DBM step=5DBM   VG: -0.363 VD: 2;
  FREQ: 2GHZ   PIN: from -15DBM to 10DBM step=5DBM   VG: -0.667 VD: 4;
  FREQ: 2GHZ   PIN: from -15DBM to 10DBM step=5DBM   VG: -1.070 VD: 6;
  FREQ: 6GHZ   PIN: from -15DBM to 10DBM step=5DBM   VG: -0.372 VD: 2;
  FREQ: 6GHZ   PIN: from -15DBM to 10DBM step=5DBM   VG: -0.673 VD: 4;
  FREQ: 6GHZ   PIN: from -15DBM to 10DBM step=5DBM   VG: -1.073 VD: 6;

! DC IV simulation

  VG: -1.062 -0.667 -0.361 VD: from 0 to 8 n=20;

end
```

```
Specification
! Power spectrum specification

  FREQ: 0.2GHZ    PIN: -15DBM -5DBM 5DBM VG: -0.373 VD: 2
                  IDO POUT1 POUT2 POUT3;
  FREQ: 0.2GHZ    PIN: -15DBM -5DBM 5DBM VG: -1.072 VD: 6
                  IDO POUT1 POUT2 POUT3;
  FREQ: 6GHZ      PIN: -15DBM -5DBM 5DBM VG: -0.372 VD: 2
                  IDO POUT1 POUT2 POUT3;
  FREQ: 6GHZ      PIN:  -15DBM -5DBM 5DBM VG: -1.073 VD: 6
                  IDO POUT1 POUT2 POUT3;

end
```

C. Data Files [69]

fetb_02.dat

```
!  File: FETB_02.DAT
!  FET power spectrum measurement data
!  fundamental freq is 0.2 GHz
!
 PARAMETER VG = -0.373  VD = 2  FREQ = 0.2GHZ;
 FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
      +10.0     +15.8      +0.4       +3.0       36.5
       +5.0     +15.1       -3.0       -1.7       37.6
        0.0     +13.1      -13.6      -10.2       42.6
       -5.0      +9.3      -31.1      -28.3       44.5
      -10.0      +4.3      -36.6      -46.2       44.8
      -15.0      -0.8      -46.6      -59.9       45.0
 PARAMETER VG = -0.674  VD = 4  FREQ = 0.2GHZ;
 FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
      +10.0     +20.1      +3.3       +5.9       49.7
       +5.0     +17.6      +3.0       -11.0      39.9
        0.0     +12.9       -6.2      -23.5       33.0
       -5.0      +8.3      -16.4      -37.1       30.8
      -10.0      +3.3      -26.4      -50.9       30.2
      -15.0      -1.7      -36.8      -99.9       30.0
 PARAMETER VG = -1.072  VD = 6  FREQ = 0.2GHZ;
 FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
      +10.0     +19.9     +11.2       -9.3       43.9
       +5.0     +15.0      +4.2      -24.3       26.9
        0.0     +10.1       -4.2      -37.7       19.3
       -5.0      +5.0      -13.7      -50.9       16.4
      -10.0       0.0      -23.7      -99.9       15.4
      -15.0      -5.2      -33.7      -99.9       15.0
```

fetb_2.dat

```
!  File: FETB_2.DAT
!  FET power spectrum measurement data
!  fundamental freq is 2 GHz
!
 PARAMETER VG = -0.363  VD = 2  FREQ = 2GHZ;
```

```
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
      +10.0     +14.5      +6.8       -1.1       26.1
       +5.0     +13.9      +4.1       -4.3       29.7
        0.0     +12.3      -0.5       -8.1       37.9
       -5.0      +9.8     -11.5      -17.7       43.1
      -10.0      +5.6     -26.5      -37.1       44.7
      -15.0      +0.2     -38.5      -54.7       45.3
PARAMETER VG = -0.667  VD = 4  FREQ = 2GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
       +10.0     +19.3      +3.0       +5.6       35.1
        +5.0     +18.1      -3.0       -2.4       34.1
         0.0     +15.0      -9.6      -23.6       32.0
        -5.0     +10.3     -19.6      -37.7       30.3
       -10.0      +5.3     -29.7      -52.3       30.1
       -15.0      -0.2     -40.6      -67.6       30.1
PARAMETER VG = -1.07  VD = 6  FREQ = 2GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
       +10.0     +21.4      +6.3       -0.3       36.8
        +5.0     +17.1      +1.4      -20.3       25.2
         0.0     +12.3      -6.7      -30.9       18.8
        -5.0      +7.3     -16.0      -44.0       16.2
       -10.0      +2.3     -25.9      -56.6       15.3
       -15.0      -3.3     -36.9      -99.9       15.0
```

fetb_6.dat

```
!  File: FETB_6.DAT
!  FET power spectrum measurement data
!  fundamental freq is 6 GHz
!
PARAMETER VG = -0.372  VD = 2  FREQ = 6GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
       +10.0     +15.1      +2.4       -5.7       38.9
        +5.0     +13.0      -5.2      -11.9       42.3
         0.0      +9.6     -19.5      -27.3       44.3
        -5.0      +4.9     -32.4      -45.6       44.7
       -10.0       0.0     -42.7      -60.1       44.9
       -15.0      -5.2     -52.8      -99.9       45.1
PARAMETER VG = -0.673  VD = 4  FREQ = 6GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
       +10.0     +18.1      -1.5       -7.3       42.8
        +5.0     +13.9     -10.7      -22.1       34.0
         0.0      +9.5     -21.2      -36.1       31.0
        -5.0      +4.6     -31.5      -49.9       30.2
       -10.0      -0.3     -41.4      -62.1       30.0
       -15.0      -5.5     -54.4      -99.9       30.0
PARAMETER VG = -1.073  VD = 6  FREQ = 6GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
       +10.0     +16.1      +1.9      -10.2       31.2
        +5.0     +11.7      -5.8      -20.6       21.3
         0.0      +7.3     -14.8      -33.5       17.1
        -5.0      +2.4     -24.6      -47.8       15.6
       -10.0      -2.6     -34.4      -61.1       15.1
       -15.0      -7.8     -46.9      -99.9       15.0
```

A.3 CIRCUIT AND DATA FILES FOR EXAMPLES IN CHAPTER 6

A.3.1 Circuit File for the Example in Section 6.2.4

```
!  Example  1
!  Demonstration of the consistency of DC/small-signal analysis
!  and nonlinear harmonic balance analysis.
!  Model used: Curtice nonlinear FET model.
!
EXPRESSION
   POWER_RATIO= SQRT(POUTW1/PINW);
END

MODEL

   EXTRINSIC2     1 2 3 4 5

        LG:   0.3NH      RG:   4          RD:   0.5
        LD:   0.2NH      RS:   2          LS:   0.08NH
        GDS:  0.2E-3     CX:   1.5PF      CDS:  0.1PF
        CGE:  0.01PF     CDE:  0.01PF;

   FETC     1 2 3

       A0:    0.15       A1:    0.15       A2:    -0.02      A3:   -0.02
       GAMMA: 1          BETA:  0.03       TAU: 3PS
       VDS0:  2          IS:    1E-14      N:   1
       CGS0:  0.5PF      CGD0:  0.092PF    FC : 0.7
       GMIN:  1.0E-07    VBI:   0.8        VBR: 30 ;

  2POR    4  5;

END

SWEEP
! HB SIMULATION

  FREQ: 5GHZ  PIN: FROM -150DBM TO 30DBM STEP=2DBM  VG: -0.6 VD: 4
        POWER_RATIO;
  FREQ: 10GHZ  PIN: FROM -150DBM TO 30DBM STEP=2DBM  VG: -0.6 VD: 4
        POWER_RATIO;

! S-PARAMETER SIMULATION

  FREQ: FROM 1GHZ TO 15GHZ STEP=1GHZ VG: -0.6 VD: 4;

END
```

A.3.2 Example 1

A. The Circuit File Before Optimization

```
!
```

```
!  Simultaneous DC/small-signal/large-signal optimization to
!  fit DC, S parameter and power spectrum measurement.
!  Model used: Curtice nonlinear FET model.
!  Starting point
!
Model

   Extrinsic2     1 2 3 4 5

        LG:   ?0.3NH?       RG:   ?0.01 4 10?        RD:   ?0.01 0.5 10?
        LD:   ?0.2NH?       RS:   ?0.01 2 10?        LS:   ?0.08NH?
        GDS:  ?0.2e-3?      CX:   ?1.5PF?            CDS:  ?0.1PF?
        CGE:  ?0.01PF?      CDE:  ?0.01PF?;
   FETC     1 2 3

       A0:     ?0  0.15   0.3?  A1:    ? 0.15 ?
       A2:     ? -0.02?         A3:    ?-0.02?
       GAMMA: ? 1 ?             BETA: ?0.03?              TAU: ?3PS?
       VDS0:  ?0  2 6?          IS:   1e-14               N:   ?1?
       CGS0:  ? 0.5PF?          CGD0: ?0.092PF?           FC : ?0.7 ?
       GMIN:  1.0E-07           VBI:  ?0.8?               VBR:  30 ;

  2por    4  5;

end

Data
! power spectrum measurement data

#include "fetb_02.dat"
#include "fetb_2.dat"
#include "fetb_6.dat"
#include "spar_3.dat"
end

Sweep
! HB simulation

  FREQ: 0.2GHZ PIN: FROM -15DBM TO 10DBM STEP=5DBM   VG: -0.373 VD: 2;
  FREQ: 0.2GHZ PIN: FROM -15DBM TO 10DBM STEP=5DBM   VG: -0.674 VD: 4;
  FREQ: 0.2GHZ PIN: FROM -15DBM TO 10DBM STEP=5DBM   VG: -1.072 VD: 6;
  FREQ: 2GHZ   PIN: FROM -15DBM TO 10DBM STEP=5DBM   VG: -0.363 VD: 2;
  FREQ: 2GHZ   PIN: FROM -15DBM TO 10DBM STEP=5DBM   VG: -0.667 VD: 4;
  FREQ: 2GHZ   PIN: FROM -15DBM TO 10DBM STEP=5DBM   VG: -1.070 VD: 6;
  FREQ: 6GHZ   PIN: FROM -15DBM TO 10DBM STEP=5DBM   VG: -0.372 VD: 2;
  FREQ: 6GHZ   PIN: FROM -15DBM TO 10DBM STEP=5DBM   VG: -0.673 VD: 4;
  FREQ: 6GHZ   PIN: FROM -15DBM TO 10DBM STEP=5DBM   VG: -1.073 VD: 6;

! S-parameter simulation

  FREQ: FROM 1GHZ TO 15GHZ STEP=1GHZ VG: -0.361 VD: 2;
  FREQ: FROM 1GHZ TO 15GHZ STEP=1GHZ VG: -0.667 VD: 4;
  FREQ: FROM 1GHZ TO 15GHZ STEP=1GHZ VG: -1.062 VD: 6;

! DC IV simulation

  VG: -1.062 -0.667 -0.361 VD: FROM 0 TO 8 N=20;
```

```
end

Specification

  FREQ: 0.2GHZ    PIN: -15DBM -5DBM 5DBM VG: -0.373 VD: 2
                  IDO POUT1 POUT2 POUT3;
  FREQ: 0.2GHZ    PIN: -15DBM -5DBM 5DBM VG: -1.072 VD: 6
                  IDO POUT1 POUT2 POUT3;
  FREQ: 6GHZ      PIN: -15DBM -5DBM 5DBM VG: -0.372 VD: 2
                  IDO POUT1 POUT2 POUT3;
  FREQ: 6GHZ      PIN:  -15DBM -5DBM 5DBM VG: -1.073 VD: 6
                  IDO POUT1 POUT2 POUT3;
  FREQ: 1GHZ 3GHZ 5GHZ 7GHZ 9GHZ 11GHZ 13GHZ 15GHZ VG: -0.361 VD: 2
        RS11 IS11 RS21 IS21 RS12 IS12 RS22 IS22;
  FREQ: 1GHZ 3GHZ 5GHZ 7GHZ 9GHZ 11GHZ 13GHZ 15GHZ VG: -0.667 VD: 4
        RS11 IS11 RS21 IS21 RS12 IS12 RS22 IS22;
  FREQ: 1GHZ 3GHZ 5GHZ 7GHZ 9GHZ 11GHZ 13GHZ 15GHZ VG: -1.062 VD: 6
        RS11 IS11 RS21 IS21 RS12 IS12 RS22 IS22;
  VG: -0.361 VD: 2 ID;
  VG: -0.667 VD: 4 ID;
  VG: -1.062 VD: 6 ID;

end
```

B. The Circuit File After Optimization

```
!
!  Simultaneous DC/small-signal/large-signal optimization to
!  fit DC, S parameter and power spectrum measurement.
!  Model used: Curtice nonlinear FET model.
!  Optimization solution
!
!Expression
!
Model

   Extrinsic2     1 2 3 4 5

     LG:  ?0.278213NH?    RG:  ?0.01 4.98203 10? RD: ?0.01 0.0210134 10?
     LD:  ?0.35449NH?     RS:  ?0.01 3.75622 10? LS: ?0.0738567NH?
     GDS: ?0.00259503?    CX:  ?2.5872PF?        CDS:?0.09319PF?
     CGE: ?0.00620253PF?  CDE: ?0.00533742PF?;

   FETC      1 2 3

     A0:  ?0  0.0940242 0.3?  A1:   ? 0.09684 ?
     A2:  ? -0.00206275?      A3:   ?-0.0175659?
     GAMMA: ? 1.29258 ?       BETA: ?0.0323823?    TAU: ?2.54601PS?
     VDS0: ?0  1.27158 6?     IS:   1e-14          N:   ?0.693781?
     CGS0: ? 0.670685PF?      CGD0: ?0.0735939PF?  FC : ?0.652801 ?
     GMIN: 1.0E-07            VBI:  ?1.13538?      VBR:  30 ;

  2por    4  5;

end
```

```
Data
! power spectrum measurement data

#include "fetb_02.dat"
#include "fetb_2.dat"
#include "fetb_6.dat"
#include "spar_3.dat"
end

Sweep
! HB simulation

  FREQ: 0.2GHZ PIN: FROM -15DBM TO 10DBM STEP=5DBM   VG: -0.373 VD: 2;
  FREQ: 0.2GHZ PIN: FROM -15DBM TO 10DBM STEP=5DBM   VG: -0.674 VD: 4;
  FREQ: 0.2GHZ PIN: FROM -15DBM TO 10DBM STEP=5DBM   VG: -1.072 VD: 6;
  FREQ: 2GHZ   PIN: FROM -15DBM TO 10DBM STEP=5DBM   VG: -0.363 VD: 2;
  FREQ: 2GHZ   PIN: FROM -15DBM TO 10DBM STEP=5DBM   VG: -0.667 VD: 4;
  FREQ: 2GHZ   PIN: FROM -15DBM TO 10DBM STEP=5DBM   VG: -1.070 VD: 6;
  FREQ: 6GHZ   PIN: FROM -15DBM TO 10DBM STEP=5DBM   VG: -0.372 VD: 2;
  FREQ: 6GHZ   PIN: FROM -15DBM TO 10DBM STEP=5DBM   VG: -0.673 VD: 4;
  FREQ: 6GHZ   PIN: FROM -15DBM TO 10DBM STEP=5DBM   VG: -1.073 VD: 6;

! S-parameter simulation

  FREQ: FROM 1GHZ TO 15GHZ STEP=1GHZ VG: -0.361 VD: 2;
  FREQ: FROM 1GHZ TO 15GHZ STEP=1GHZ VG: -0.667 VD: 4;
  FREQ: FROM 1GHZ TO 15GHZ STEP=1GHZ VG: -1.062 VD: 6;

! DC IV simulation

  VG: -1.062 -0.667 -0.361 VD: FROM 0 TO 8 N=20;

end

Specification

  FREQ: 0.2GHZ   PIN: -15DBM -5DBM 5DBM VG: -0.373 VD: 2
                 ID0 POUT1 POUT2 POUT3;
  FREQ: 0.2GHZ   PIN: -15DBM -5DBM 5DBM VG: -1.072 VD: 6
                 ID0 POUT1 POUT2 POUT3;
  FREQ: 6GHZ     PIN: -15DBM -5DBM 5DBM VG: -0.372 VD: 2
                 ID0 POUT1 POUT2 POUT3;
  FREQ: 6GHZ     PIN:  -15DBM -5DBM 5DBM VG: -1.073 VD: 6
                 ID0 POUT1 POUT2 POUT3;
  FREQ: 1GHZ 3GHZ 5GHZ 7GHZ 9GHZ 11GHZ 13GHZ 15GHZ VG: -0.361 VD: 2
        RS11 IS11 RS21 IS21 RS12 IS12 RS22 IS22;
  FREQ: 1GHZ 3GHZ 5GHZ 7GHZ 9GHZ 11GHZ 13GHZ 15GHZ VG: -0.667 VD: 4
        RS11 IS11 RS21 IS21 RS12 IS12 RS22 IS22;
  FREQ: 1GHZ 3GHZ 5GHZ 7GHZ 9GHZ 11GHZ 13GHZ 15GHZ VG: -1.062 VD: 6
        RS11 IS11 RS21 IS21 RS12 IS12 RS22 IS22;
  VG: -0.361 VD: 2 ID;
  VG: -0.667 VD: 4 ID;
  VG: -1.062 VD: 6 ID;

end
```

C. Measurement Data Files

The measurement data files are the same as those listed in Appendices A.1.3 and A.2.1.

A.3.3 Example 2

A. Circuit File Before Optimization

```
!  Example 2
!  Small-signal broadband amplifier design.
!  Model used: Curtice cubic symmetrical model.
!  Only small-signal optimization.

Expression
!  |S21| in dB.  Upper spec and lower spec for |S21|
!  where |S21| is calculated equivalently by power ratio.
   Power_Ratio1 = 20*log10(sqrt( POUTW1 / PINW ));
   Power_R_U    = sqrt(POUTW1 / PINW) - 2.6607;
   Power_R_L    = 2.3714 - sqrt(POUTW1 / PINW);

!  |S11| <= 0.4
   M1 = MS11 - 0.4;

!  |S21| in dB
   M2 = 20*log10(MS21);
!  Upper and lower spec for |S21|
!  equivalent to 7.5dB <= |S21 <= 8.5dB.
   M21= MS21 - 2.6607;
   M22= 2.3714 - MS21;

!  |S12| <= 0.15
   M3 = MS12 - 0.15;

!  |S22| <= 0.4
   M4 = MS22 - 0.4;
end
!
Model

   SRL  @int_gate   @gate        R=4.81347  L=0.283635NH;
   SRL  @int_drain  @drain       R=0.01     L=0.342137NH;
   SRL  @int_source @ground      R=2.91775  L=0.0818002NH;
   SRC  @int_drain  @int_source  R=383.82   C=2.11667PF;
   CAP  @int_drain  @int_source  C=0.0885082PF;

!  bias circuits

   SRL  @gate1     @gate   R=1     L=1000NH;
!  RES  @gate_bias @gate1  R=20;              ! if bias VGB is fixed.
   RES  @gate_bias @gate1  R=?20?;            ! if bias VGB is variable.

   RES  @gate1     @ground R=20;
```

```
!  SRL  @drain_bias @drain  R=30   L=1000NH;  ! if bias VDB is fixed.
   SRL  @drain_bias @drain  R=?50? L=1000NH;  ! if bias VDB is variable.

!  input/output circuits

   CAP  @face_g  @gate  C=?5PF?;
   CAP  @face_d  @drain C=?1.85PF?;

!  matching network for input

   SRL  @face_g  @input   R=0.01 L=?0.8NH?;
   SRL  @face_g  @ground  R=0.01 L=?1.46NH?;
   SRL  @input   @ground  R=0.01 L=?0.38NH?;
   CAP  @input   @ground  C=?0.83PF?;

!  matching network for output

   RES  @face_d  @ground  R=?500?;
   SRL  @face_d  @match_1 R=0.01 L=?0.6NH?;
   SRL  @match_1 @ground  R=0.01 L=?2.5NH?;
   SRL  @match_1 @match_2 R=0.01 L=?0.8NH?;
   CAP  @match_2 @output  C=?0.5PH?;


   FETC     @int_gate @int_drain @int_source

       A0:     0.0866824      A1:    0.0870791
       A2:    -0.00199355     A3:   -0.0153648
       GAMMA:  1.26183        BETA:  0.0307202        TAU: 3.01859PS
       VDS0:   1.43656        IS:    1.01059e-14      N:   0.745935
       CGS0:   0.561425PF     CGD0:  0.0754285PF      FC : 0.698336
       GMIN:   1.00034e-07    VBI:   1.49176          VBR: 29.9266;

    2BIASPORT @gate_bias @ground @drain_bias @ground;
    2POR  @input @output;

end

Data
! power spectrum measurement data
! This data file is only used for display purposes.
#include "spct3.dat"
end

Specification

  freq: from 4ghz to 8ghz step=1ghz  pin: -10dbm vg: -0.8 vd: 7
        pout2 < -42dBm pout3 < -42dBm Power_R_U <0  Power_R_L <0;
  freq: from 4ghz to 8ghz step=1ghz  pin:  -5dbm vg: -0.8 vd: 7
        pout2 < -37dBm pout3 < -37dBm Power_R_U <0  Power_R_L <0;
  freq: from 4ghz to 8ghz step=1ghz  pin:   0dbm vg: -0.8 vd: 7
        pout2 < -32dBm pout3 < -32dBm Power_R_U <0  Power_R_L <0;

  freq: from 4ghz to 8ghz step=1ghz  vg:-0.8 vd:7
        M1 <0 M21 <0 M22 <0 M3 <0 M4 <0;

end
```

```
Sweep
! HB simulation
 freq: from 3ghz to 10ghz step=0.5ghz PIN: -20dbm vg=-0.8 vd=7 harm=5
       power_ratio1 Power_R_U   Power_R_L;
 freq: from 3ghz to 10ghz step=0.5ghz PIN: -10dbm vg=-0.8 vd=7 harm=5
       power_ratio1 Power_R_U   Power_R_L;
 freq: from 3ghz to 10ghz step=0.5ghz PIN:  -5dbm vg=-0.8 vd=7 harm=5
       power_ratio1 Power_R_U   Power_R_L;
 freq: from 3ghz to 10ghz step=0.5ghz PIN:   0dbm vg=-0.8 vd=7 harm=5
       power_ratio1 Power_R_U   Power_R_L;
 freq: from 3ghz to 10ghz step=0.5ghz PIN:   5dbm vg=-0.8 vd=7 harm=5
       power_ratio1 power_R_U   Power_R_L;

! S-parameter simulation

   freq: from 1ghz to 20ghz step=0.5ghz  vg: -0.8 Vd: 7 M1 M2 M3 M4;

end
```

B. Circuit File after Combined Small- and Large-Signal Optimization

```
!  Example 2
!  Small-signal broadband amplifier design.
!  Model used: Curtice cubic symmetrical model.
!  Combined small-signal and large-signal optimization.
!
Expression
!  |S21| in dB.  Upper spec and lower spec for |S21|
!  where |S21| is calculated equivalently by power ratio.
   Power_Ratio1 = 20*log10(sqrt( POUTW1 / PINW ));
   Power_R_U    = sqrt(POUTW1 / PINW) - 2.6607;
   Power_R_L    = 2.3714 - sqrt(POUTW1 / PINW);

!  |S11| <= 0.4
   M1 = MS11 - 0.4;

!  |S21| in dB
   M2 = 20*log10(MS21);
!  Upper and lower spec for |S21|
!  equivalent to 7.5dB <= |S21 <= 8.5dB.
   M21= MS21 - 2.6607;
   M22= 2.3714 - MS21;

!  |S12| <= 0.15
   M3 = MS12 - 0.15;

!  |S22| <= 0.4
   M4 = MS22 - 0.4;
end
!
Model

   SRL  @int_gate   @gate        R=4.81347  L=0.283635NH;
   SRL  @int_drain  @drain       R=0.01     L=0.342137NH;
   SRL  @int_source @ground      R=2.91775  L=0.0818002NH;
```

```
   SRC  @int_drain  @int_source  R=383.82   C=2.11667PF;
   CAP  @int_drain  @int_source  C=0.0885082PF;

!  bias circuits

   SRL  @gate1      @gate    R=1         L=1000NH;
   RES  @gate_bias  @gate1   R=?37.7326?;
   RES  @gate1      @ground  R=20;
   SRL  @drain_bias @drain   R=?48.4858?    L=1000NH;

!  input/output circuits

   CAP  @face_g  @gate  C=?10.3448PF?;
   CAP  @face_d  @drain C=?0.294873PF?;

!  matching network for input

   SRL  @face_g  @input   R=0.01 L=?1.00777NH?;
   SRL  @face_g  @ground  R=0.01 L=?5.74427NH?;
   SRL  @input   @ground  R=0.01 L=?3.43241NH?;
   CAP  @input   @ground  C=?0.543859PF?;

!  matching network for output

   RES  @face_d  @ground  R=?175.224?;
   SRL  @face_d  @match_1 R=0.01 L=?0.959309NH?;
   SRL  @match_1 @ground  R=0.01 L=?6.55463NH?;
   SRL  @match_1 @match_2 R=0.01 L=?0.891978NH?;
   CAP  @match_2 @output  C=?0.497582PH?;


   FETC     @int_gate @int_drain @int_source

       A0:     0.0866824      A1:    0.0870791
       A2:    -0.00199355     A3:   -0.0153648
       GAMMA:  1.26183        BETA:  0.0307202        TAU: 3.01859PS
       VDS0:   1.43656        IS:    1.01059e-14      N:   0.745935
       CGS0:   0.561425PF     CGD0:  0.0754285PF      FC : 0.698336
       GMIN:   1.00034e-07    VBI:   1.49176          VBR: 29.9266;

    2BIASPORT @gate_bias @ground @drain_bias @ground;
    2POR  @input @output;

end

Data
! power spectrum measurement data
! This data file is only used for display purposes.
#include "spct3.dat"
end

Specification

  freq: from 4ghz to 8ghz step=1ghz  pin: -10dbm vg: -0.8 vd: 7
        pout2 < -42dBm pout3 < -42dBm Power_R_U <0  Power_R_L <0;
  freq: from 4ghz to 8ghz step=1ghz  pin:  -5dbm vg: -0.8 vd: 7
        pout2 < -37dBm pout3 < -37dBm Power_R_U <0  Power_R_L <0;
  freq: from 4ghz to 8ghz step=1ghz  pin:   0dbm vg: -0.8 vd: 7
```

```
       pout2 < -32dBm pout3 < -32dBm Power_R_U <0  Power_R_L <0;

  freq: from 4ghz to 8ghz step=1ghz  vg:-0.8 vd:7
       M1 <0 M21 <0 M22 <0 M3 <0 M4 <0;

end

Sweep
! HB simulation
 freq: from 3ghz to 10ghz step=0.5ghz PIN: -20dbm vg=-0.8 vd=7 harm=5
       power_ratio1 Power_R_U   Power_R_L;
 freq: from 3ghz to 10ghz step=0.5ghz PIN: -10dbm vg=-0.8 vd=7 harm=5
       power_ratio1 Power_R_U   Power_R_L;
 freq: from 3ghz to 10ghz step=0.5ghz PIN:  -5dbm vg=-0.8 vd=7 harm=5
       power_ratio1 Power_R_U   Power_R_L;
 freq: from 3ghz to 10ghz step=0.5ghz PIN:   0dbm vg=-0.8 vd=7 harm=5
       power_ratio1 Power_R_U   Power_R_L;
 freq: from 3ghz to 10ghz step=0.5ghz PIN:   5dbm vg=-0.8 vd=7 harm=5
       power_ratio1 power_R_U   Power_R_L;

! S-parameter simulation

   freq: FROM 1ghz TO 20ghz STEP=0.5GHZ  vg: -0.8 vd: 7 m1 m2 m3 m4;

end
```

C. Data File for Example 2

This data file is only used for display purposes, i.e., to give references to the responses of the amplifier.

```
 PARAMETER VG = -0.8  VD = 7  FREQ = 3GHZ;
 FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
        -30.0      -22.0     -62       -62       30.0
 PARAMETER VG = -0.8  VD = 7  FREQ = 4GHZ;
 FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
        -30.0      -22.0     -62       -62       30.0
 PARAMETER VG = -0.8  VD = 7  FREQ = 5GHZ;
 FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
        -30.0      -22.0     -62       -62       30.0
 PARAMETER VG = -0.8  VD = 7  FREQ = 6GHZ;
 FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
        -30.0      -22.0     -62       -62       30.0
 PARAMETER VG = -0.8  VD = 7  FREQ = 7GHZ;
 FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
        -30.0      -22.0     -62       -62       30.0
 PARAMETER VG = -0.8  VD = 7  FREQ = 8GHZ;
 FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
        -30.0      -22.0     -62       -62       30.0
 PARAMETER VG = -0.8  VD = 7  FREQ = 10GHZ;
 FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
        -30.0      -22.0     -62       -62       30.0
```

```
PARAMETER VG = -0.8  VD = 7  FREQ = 3GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
       -20.0       -12.0      -52       -52        30.0
PARAMETER VG = -0.8  VD = 7  FREQ = 4GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
       -20.0       -12.0      -52       -52        30.0
PARAMETER VG = -0.8  VD = 7  FREQ = 5GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
       -20.0       -12.0      -52       -52        30.0
PARAMETER VG = -0.8  VD = 7  FREQ = 6GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
       -20.0       -12.0      -52       -52        30.0
PARAMETER VG = -0.8  VD = 7  FREQ = 7GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
       -20.0       -12.0      -52       -52        30.0
PARAMETER VG = -0.8  VD = 7  FREQ = 8GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
       -20.0       -12.0      -52       -52        30.0
PARAMETER VG = -0.8  VD = 7  FREQ = 10GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
       -20.0       -12.0      -52       -52        30.0

PARAMETER VG = -0.8  VD = 7  FREQ = 3GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
       -10.0       -2.0       -42       -42        30.0
PARAMETER VG = -0.8  VD = 7  FREQ = 4GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
       -10.0       -2.0       -42       -42        30.0
PARAMETER VG = -0.8  VD = 7  FREQ = 5GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
       -10.0       -2.0       -42       -42        32.0
PARAMETER VG = -0.8  VD = 7  FREQ = 6GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
       -10.0       -2.0       -42       -42        32.0
PARAMETER VG = -0.8  VD = 7  FREQ = 7GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
       -10.0       -2.0       -42       -42        32.0
PARAMETER VG = -0.8  VD = 7  FREQ = 8GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
       -10.0       -2.0       -42       -42        32.0
PARAMETER VG = -0.8  VD = 7  FREQ = 10GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
       -10.0       -2.0       -42       -42        32.0

PARAMETER VG = -0.8  VD = 7  FREQ = 3GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
       -5.0         3.0       -37       -37        30.0
PARAMETER VG = -0.8  VD = 7  FREQ = 4GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
       -5.0         3.0       -37       -37        30.0
PARAMETER VG = -0.8  VD = 7  FREQ = 5GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
       -5.0         3.0       -37       -37        32.0
PARAMETER VG = -0.8  VD = 7  FREQ = 6GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
       -5.0         3.0       -37       -37        32.0
PARAMETER VG = -0.8  VD = 7  FREQ = 7GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
```

```
      -5.0      3.0      -37      -37       32.0
PARAMETER VG = -0.8  VD = 7  FREQ = 8GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
      -5.0      3.0      -37      -37       32.0
PARAMETER VG = -0.8  VD = 7  FREQ = 10GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
      -5.0      3.0      -37      -37       32.0

PARAMETER VG = -0.8  VD = 7  FREQ = 3GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
      10.0      18.0      -22      -22       30.0
PARAMETER VG = -0.8  VD = 7  FREQ = 4GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
      10.0      18.0      -22      -22.0       30.0
PARAMETER VG = -0.8  VD = 7  FREQ = 5GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
      10.0      18.0      -22      -22.0       30.0
PARAMETER VG = -0.8  VD = 7  FREQ = 6GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
      10.0      18.0      -22      -22.0       30.0
PARAMETER VG = -0.8  VD = 7  FREQ = 7GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
      10.0      18.0      -22      -22.0       30.0
PARAMETER VG = -0.8  VD = 7  FREQ = 8GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
      10.0      18.0      -22      -22.0       30.0
PARAMETER VG = -0.8  VD = 7  FREQ = 10GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
      10.0      18.0      -22      -22       30.0

PARAMETER VG = -0.8  VD = 7  FREQ = 3GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
      0.0       8.0      -32      -32       30.0
PARAMETER VG = -0.8  VD = 7  FREQ = 4GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
      0.0       8.0      -32      -32.0       30.0
PARAMETER VG = -0.8  VD = 7  FREQ = 5GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
      0.0       8.0      -32      -32.0       30.0
PARAMETER VG = -0.8  VD = 7  FREQ = 6GHZ;
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      0.0       8.0      -32      -32.0       30.0
PARAMETER VG = -0.8  VD = 7  FREQ = 7GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
      0.0       8.0      -32      -32.0       30.0
PARAMETER VG = -0.8  VD = 7  FREQ = 8GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
      0.0       8.0      -32      -32.0       30.0
PARAMETER VG = -0.8  VD = 7  FREQ = 10GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
      0.0       8.0      -32      -32       30.0

PARAMETER VG = -0.8  VD = 7  FREQ = 3GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
      5.0      13.0      -27      -27       30.0
PARAMETER VG = -0.8  VD = 7  FREQ = 4GHZ;
FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
      5.0      13.0      -27      -27.0       30.0
```

```
 PARAMETER VG = -0.8  VD = 7  FREQ = 5GHZ;
 FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
       5.0     13.0     -27      -27.0       30.0
 PARAMETER VG = -0.8  VD = 7  FREQ = 6GHZ;
 FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
       5.0     13.0     -27      -27.0       30.0
 PARAMETER VG = -0.8  VD = 7  FREQ = 7GHZ;
 FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
       5.0     13.0     -27      -27.0       30.0
 PARAMETER VG = -0.8  VD = 7  FREQ = 8GHZ;
 FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
       5.0     13.0     -27      -27.0       30.0
 PARAMETER VG = -0.8  VD = 7  FREQ = 10GHZ;
 FORMAT PIN(DBM) POUT1(DBM) POUT2(DBM)  POUT3(DBM) IDO(MA);
       5.0     13.0     -27      -27       30.0

PARAMETER VG =-0.8  VD=7  ;
FORMAT FREQ MS11 PS11   MS21     PS21     MS12  PS12    MS22  PS22 ;
 3.000GHZ  .35  -58.9   2.5119   132.1    .1    60.0    .35  -28.3
 4.000GHZ  .35  -58.9   2.5119   132.1    .1    60.0    .35  -28.3
 5.000GHZ  .35  -58.9   2.5119   132.1    .1    60.0    .35  -28.3
 6.000GHZ  .35  -58.9   2.5119   132.1    .1    60.0    .35  -28.3
 7.000GHZ  .35  -58.9   2.5119   132.1    .1    60.0    .35  -28.3
 8.000GHZ  .35  -58.9   2.5119   132.1    .1    60.0    .35  -28.3
 9.000GHZ  .35  -58.9   2.5119   132.1    .1    60.0    .35  -28.3
10.000GHZ  .35  -58.9   2.5119   132.1    .1    60.0    .35  -28.3
11.000GHZ  .35  -58.9   2.5119   132.1    .1    60.0    .35  -28.3
12.000GHZ  .35  -58.9   2.5119   132.1    .1    60.0    .35  -28.3
13.000GHZ  .35  -58.9   2.5119   132.1    .1    60.0    .35  -28.3
14.000GHZ  .35  -58.9   2.5119   132.1    .1    60.0    .35  -28.3
15.000GHZ  .35  -58.9   2.5119   132.1    .1    60.0    .35  -28.3
16.000GHZ  .35  -58.9   2.5119   132.1    .1    60.0    .35  -28.3
```

Appendix B

RELATIONSHIP BETWEEN I_{B0} AND V_{BC} IN THE MATERKA MODEL

For the drain-to-gate diode of the Materka and Kacprzak FET model (see Figure 3.3 (a)), we have

$$i_{dg} = I_{B0} \exp\left[\alpha_B (v_{dg} - V_{BC})\right]. \tag{B.1}$$

This can be rewritten as

$$i_{dg} = I_{B0} \exp\left(\alpha_B v_{dg}\right) \cdot \exp\left(-\alpha_B V_{BC}\right) \tag{B.2}$$

or

$$i_{dg} = I'_{B0} \exp\left(\alpha_B v_{dg}\right) \tag{B.3}$$

where

$$I'_{B0} = I_{B0} \exp\left(-\alpha_B V_{BC}\right). \tag{B.4}$$

For a given value of I'_{B0} there is no unique solution for I_{B0} and V_{BC}. In other words, only one of the two parameters I_{B0} and V_{BC} is independent. Therefore, we can fix V_{BC} and optimize I_{B0} during parameter extraction.

Appendix C

NONLINEAR CHARGE EXPRESSIONS FOR THE MATERKA MODEL

In Chapter 3, we discussed the Materka and Kacprzak nonlinear FET model. The nonlinear capacitors C_{gs} and C_{dg} are characterized by the expressions

$$\begin{cases} C_{gs} = C_{10}(1 - K_1 v_g)^{-1/2} + C_{1S} \\ C_{gs} = C_{10}\sqrt{5} + C_{1S} \qquad \text{if } K_1 v_g \geq 0.8 \end{cases} \tag{C.1}$$

and

$$\begin{cases} C_{dg} = C_{F0}(1 + K_F v_{dg})^{-1/2} \\ C_{dg} = C_{F0}\sqrt{5} \qquad \text{if } -K_F v_{dg} \geq 0.8 \end{cases} \tag{C.2}$$

In the harmonic balance simulation procedure we use charge expressions for the nonlinear capacitors instead of capacitance expressions. From the definition of the nonlinear capacitor we know that

$$C(v) = \frac{dq(v)}{dv}. \tag{C.3}$$

Therefore,

$$q(v) = \int C(v)\, dv. \tag{C.4}$$

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$$C(v) = \frac{dq(v)}{dv}. \tag{C.3}$$

Therefore,

$$q(v) = \int C(v)\, dv. \tag{C.4}$$

Consider the nonlinear capacitor C_{gs}. For $K_1 v_g < 0.8$,

$$\begin{aligned} q_{gs}(v_g) &= \int C_{10}(1 - K_1 v_g)^{-1/2}\, dv_g + C_{1S} v_g + C_{2S} \\ &= -\frac{2C_{10}}{K_1}(1 - K_1 v_g)^{1/2} + C_{1S} v_g + C_{2S} \end{aligned} \tag{C.5}$$

and for $K_1 v_g \geq 0.8$,

$$q_{gs}(v_g) = \left(C_{10}\sqrt{5} + C_{1S}\right) v_g + C_{3S} \tag{C.6}$$

where C_{2S} and C_{3S} are constants to be determined.

Suppose $q_{gs} = 0$ when $v_g = 0$. Then from (C.5), we get

$$q_{gs}(0) = -\frac{2C_{10}}{K_1} + C_{2S} = 0$$

i.e.,

$$C_{2S} = \frac{2C_{10}}{K_1}.$$

Substituting C_{2S} back into (C.5), we obtain

$$\begin{aligned} q_{gs}(v_g) &= \frac{2C_{10}}{K_1}\left(1 - (1 - K_1 v_g)^{1/2}\right) + C_{1S} v_g \\ &= \frac{2C_{10}}{K_1}\frac{1 - (1 - K_1 v_g)}{1 + (1 - K_1 v_g)^{1/2}} + C_{1S} v_g \\ &= \left(\frac{2C_{10}}{1 + (1 - K_1 v_g)^{1/2}} + C_{1S}\right) v_g \end{aligned}$$

C_{3S} can be determined from the continuity assumption of q_{gs}. Consider the situation when $K_1 v_g = 0.8$, or $v_g = 0.8/K_1$. By combining (C.5) and (C.6),

$$-\frac{2C_{10}}{K_1}(1 - 0.8)^{1/2} + C_{1S}\frac{0.8}{K_1} + C_{2S} = \left(C_{10}\sqrt{5} + C_{1S}\right)\frac{0.8}{K_1} + C_{3S}$$

from which C_{3S} can be solved as

$$C_{3S} = \frac{C_{10}}{K_1}\left(2 - 2\sqrt{0.2} - 0.8\sqrt{5}\right).$$

Therefore,

$$q_{gs}(v_g) = \left(\frac{2C_{10}}{1+(1-K_1v_g)^{1/2}} + C_{1S}\right) v_g \tag{C.7}$$

for $K_1 v_g < 0.8$, and

$$q_{gs}(v_g) = \left(C_{10}\sqrt{5} + C_{1S}\right) v_g + C_{3S} \tag{C.8}$$

for $K_1 v_g \geq 0.8$, where

$$C_{3S} = \frac{C_{10}}{K_1}\left(2 - 2\sqrt{0.2} - 0.8\sqrt{5}\right).$$

Similar derivations can be applied to C_{dg}. The result is

$$q_{dg}(v_{dg}) = \left(\frac{2C_{F0}}{1+(1+K_F v_{dg})^{1/2}}\right) v_{dg} \tag{C.9}$$

for $-K_F v_{dg} < 0.8$, and

$$q_{dg}(v_{dg}) = C_{F0}\sqrt{5} v_{dg} + C_{F1} \tag{C.10}$$

for $-K_F v_{dg} \geq 0.8$, where

$$C_{F1} = \frac{2C_{F0}}{K_F}\left(\frac{3}{\sqrt{5}} - 1\right).$$

Appendix D

POWER SPECTRUM EXPRESSION FOR $|S_{21}|$

Consider a general two-port circuit as shown in Figure D.1. Assume that $Z_s = Z_{01} = R_s$ and $Z_L = Z_{02} = R_L$, which corresponds to the matched transducer power gain condition [44]. By definition of S parameters,

$$b_1 = S_{11}a_1 + S_{12}a_2$$

$$b_2 = S_{21}a_1 + S_{22}a_2$$

where

$$a_1 = \frac{V_1^+}{\sqrt{Z_{01}}} \qquad a_2 = \frac{V_2^+}{\sqrt{Z_{02}}}$$

$$b_1 = \frac{V_1^-}{\sqrt{Z_{01}}} \qquad b_2 = \frac{V_2^-}{\sqrt{Z_{02}}}$$

S_{21} can be determined by

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} = \left.\sqrt{\frac{Z_{01}}{Z_{02}}}\,\frac{V_2^-}{V_1^+}\right|_{V_2^+=0} \tag{D.1}$$

From the assumption that $Z_L = Z_{02} = R_L$, we have $V_2^+ = 0$ and $V_2^- = V_2$, and from $Z_s = Z_{01} = R_s$ and the definition of the available input power, $V_1^+ = V_s/2$. Therefore,

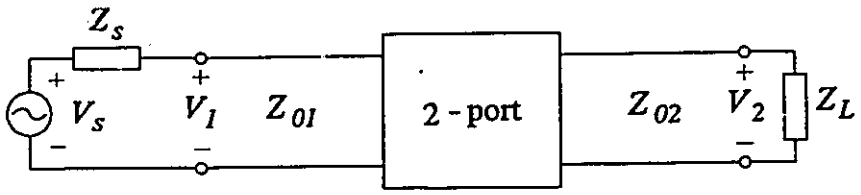

Figure D.1: A general two-port circuit.

$$S_{21} = 2\sqrt{\frac{R_s}{R_L}}\,\frac{V_2}{V_s}\,. \tag{D.2}$$

On the other hand, the output power measured at R_L is

$$P_{out} = \frac{|V_2|^2}{2R_L} \tag{D.3}$$

and the available input power from the source is

$$P_{in} = \frac{|V_s/2|^2}{2R_s}\,. \tag{D.4}$$

Therefore, we obtain the relationship between S_{21} and P_{in} and P_{out} by relating (D.2 - D.4)

$$|S_{21}| = \sqrt{\frac{P_{out}}{P_{in}}} \tag{D.5}$$

under the conditions $Z_s = Z_{01} = R_s$ and $Z_L = Z_{02} = R_L$.

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