

**SCHOTTKY CONTACTS TO INDIUM PHOSPHIDE
AND THEIR APPLICATIONS**

by

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To my wife, Helen

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ABSTRACT

InP and related materials have become important materials for applications in many electronic and photonic devices because of their high electron mobilities and high saturation electron drift velocities. InGaAs and InGaAsP, grown lattice matched to InP, are the materials of choice for making light sources and detectors in the wavelength range of 1.3 - 1.6 μm for the present day high data rate, long haul, fibre-optic communication systems. InGaAs metal-semiconductor-metal (MSM) photodetectors, InGaAs high-electron mobility transistors (HEMTs) and their monolithic integration as photoreceivers are promising devices for opto-electronic integrated circuits (OEICs). In the fabrication of the InGaAs MSM-PDs and HEMTs, good Schottky contacts are critical to achieve high performance, such as low dark current and high breakdown voltage, of the devices. However, the Schottky barrier height of metal/InGaAs contacts is only about 0.2 - 0.3 eV, which is not high enough for device applications. InP was chosen as the contact material in our fabrications of InGaAs MSM-PDs and HEMTs because of its compatibility in growth and lattice matched to $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$.

In this research, the following investigations were carried out to understand the physics of the InP Schottky barrier, to obtain good Schottky contacts to InP, and to improve the performance of the InP/InGaAs MSM-PDs.

1) It was found that the current-voltage characteristics of metal(s)-InP Schottky contacts depart from the behavior predicted for the thermionic emission model. To explain these barrier anomalies, a modified current-voltage relationship was developed based on the inhomogeneous Schottky barrier.

2) A systematic investigation on metallization schemes shows that the Schottky barrier height of metal(s)-InP ranges from 0.38 to 0.5 eV, depending on the metal(s) and deposition techniques and the surface conditions of the InP. Among them, Au/Ti/Pt produces the highest barrier height while Au/Ni/Pt has the best uniformity in metal(s)-InP Schottky contacts. To further increase the Schottky barrier height, a thin $\text{In}_{1-x}\text{Ga}_x\text{P}$ (x ranges from 0.1 to 0.3) layer of 100 - 200 Å grown on top of InP was employed. The barrier height obtained is found between 0.56 to 0.65 eV. The dark current is significantly reduced while the reverse breakdown voltage is increased from about 15 V to 20 V.

3) High-performance InGaAs MSM-PDs with InP as the barrier layer was fabricated. The MSM-PDs with a finger width of $2\mu\text{m}$, finger spacing of $2\mu\text{m}$, and an active area of $50\times 50\mu\text{m}^2$, have a dark current of about 200 nA at a bias of 10 V, a low capacitance of 0.2 pF, and breakdown voltages of about 15 V. A fairly high responsivity of 0.75 ± 0.05 A/W at $\lambda=1.3\mu\text{m}$ was obtained. The temporal response is characterized by a rise time of about 4.0 ± 0.2 ps, fall time of 8.0 ± 0.2 ps, and FWHM of 8.5 ± 0.2 ps which corresponds to a 3-dB frequency (unit current gain cut-off frequency), $f_{3\text{dB}}$, of 20 GHz. The performance is comparable to the best of those InGaAs MSM-PDs with InAlAs as the contact layer.

4) Because of the lateral conduction in MSM-PDs and the Fermi-level pinning in InP due to surface states, the surface conditions play an important role in device performance. Surface passivation using $(\text{NH}_4)_2\text{S}_x$ solution was successfully implemented to improve the performance of InGaAs/InP MSM-PDs.

Table of Contents

Chapter 1 INTRODUCTION

1.1	Technical Importance of InP and Related Materials	1
1.2	Schottky Contacts to InP	2
1.2.1	Classic Models	2
1.2.2	Mechanisms of Barrier Formation	5
I)	Linear Interface Model	6
II)	Metal Induced Gap States (MIGS) Model	6
III)	Unified Defect Model (UDM)	7
IV)	Effective Work Function Model	7
1.3	Conduction Mechanisms in Schottky Barriers	8
1.4	Summary of the Research Described in This Thesis	9
1.4.1	Conduction Mechanisms in InP Schottky Barrier	9
1.4.2	Metallization Schemes for Metal-InP Schottky Contacts	10
1.4.3	Surface Passivation of InP	10
1.4.4	Barrier Enhancement on InP Using $\text{In}_{1-x}\text{Ga}_x\text{P}$	11
1.4.5	Design, Fabrication, and Characterization of InGaAs MSM-PDs	12
I)	Barrier Enhancement Layer	13
II)	Optimization of Fabrication Processes	14
II)	Sulfur Passivation	15
1.5	Organization of The Thesis	15

**Chapter 2 SCHOTTKY-BARRIER ANOMALIES
AND BARRIER INHOMOGENEITIES**

2.1 Introduction	17
2.2 Conduction Mechanisms in InP Schottky Barriers	19
2.2.1 Current Transport Theory	19
I) Thermionic Emission	22
II) Diffusion Theory	23
III) Generalized Theory	24
IV) Image-Force Lowering	26
2.2.2 Tunneling Through the Barrier	27
2.2.3 Recombination in the Depletion Region	29
2.3 Inhomogeneous Barrier Model	31

Chapter 3 SCHOTTKY CONTACTS TO $\text{In}_{1-x}\text{Ga}_x\text{P}$

3.1 Introduction	36
3.2 Experimental Procedures	38
3.2.1 Fabrication of Schottky Diodes	38
I) Sample Cleaning	39
II) Sample Patterning	39
III) Metallization	40
IV) Thermal Annealing	41
3.2.2 Characterization of Schottky Diodes	41
3.3 Results and Discussion	44
3.3.1 Metallization Schemes	44

3.3.2	Ideality Factor Greater Than Unity	47
	I) Leakage Current from Contact Edge	47
	II) Image-Force Lowering	48
	III) Tunneling Through the Barrier	49
	IV) Recombination in the Depletion Region	50
	V) The Effects of an Interfacial Layer	52
3.3.3	Characteristics of InP Schottky Diodes	54
3.3.4	Barrier Inhomogeneities in InP Schottky Barriers	62
3.3.5	In _{1-x} Ga _x P/InP Schottky Diodes	73

Chapter 4 SULFUR PASSIVATION OF InP SURFACE

4.1	Introduction	83
	4.1.1 Technical Importance of Surface Passivation	83
	4.1.2 Theory of Surface Passivation	84
	4.1.3 Applications of Sulfur Passivation	86
4.2	Experimental Procedures	88
4.3	Results and Discussion	91
	4.3.1 InP Substrates	91
	4.3.2 InP Schottky Diodes	99
	4.3.3 InP MIS Diodes	101
	4.3.4 InP MSM-PDs	103
	4.3.5 InGaAs MSM-PDs	104

**Chapter 5 InGaAs METAL-SEMICONDUCTOR-
METAL (MSM) PHOTODETECTORS**

5.1 Introduction	106
5.1.1 Technical Importance of InGaAs MSM-PDs	106
5.1.2 Barrier Enhancement Layers	107
5.1.3 MSM-PD Modeling and Simulation	110
5.1.4 Fabrication of MSM-PDs	111
5.1.5 Monolithic Integration of MSM-PDs with FETs	111
5.2 MSM Theory	114
5.2.1 1D MSM-PD	115
5.2.2 2D MSM-PD	122
5.3 Experimental Procedures	127
5.3.1 Device Fabrication	127
I) Sample Cleaning	128
II) Dielectric Layer Growth	128
III) Sample Patterning	129
IV) Metallization	131
V) Etching	132
VI) Passivation	133
VII) Thermal Annealing	133
5.3.2 Characterization	134
5.4 Results and Discussion	138
5.4.1 Metallization Schemes	138
5.4.2 Capacitance	142

I) Depletion of the Device	142
II) Thermal Annealing	145
III) Sulfide Passivation	147
5.4.3 Dark Current	151
I) Flat Band Voltage	151
II) Saturation Dark Current	152
III) “Soft Breakdown”	158
IV) Barrier Enhancement	160
V) Field-Assisted Tunneling	162
VI) Surface Passivation	162
5.4.4 Photoresponse of MSM-PDs	170
I) I-V Characteristics	170
II) Internal Gain	172
III) Responsivity	174
5.4.5 Quantum Efficiency	176
Chapter 6 CONCLUSION	180

List of Figures

Figure	Caption	Page
2.2-1	Carrier transport processes in a forward-biased Schottky barrier.	20
2.2-2	Electron quasi-Fermi level in a forward-biased Schottky barrier.	21
2.2-3	Image-force lowering of Schottky barrier.	27
2.2-4	Field and thermionic-field emission under forward bias.	28
2.3-1	Schematic of a metal-semiconductor interface where some regions have barrier heights lower than the mean value.	31
2.3-2	Schematic of energy diagram of a metal-semiconductor contact.	32
3.2-1	A schematic of the cross section of an InP Schottky diode.	38
3.2-2	Schematic set-up of the low temperature measurement system.	42
3.3-1	The Schottky barrier heights of metal(s)-InP contacts annealed at 300°C, 400°C, and 500°C for 20 seconds.	44
3.3-2	The ideality factors of metal(s)-InP contacts annealed at 300°C, 400°C, and 500°C for 20 seconds.	45
3.3-3	Dark current of InP Schottky diode as a function of perimeter of the contact with temperature and reverse bias voltage as parameters.	48
3.3-4	(a) Ideality factor and (b) barrier height caused by image-force lowering as a function of reverse bias voltage with temperature as a parameter.	49
3.3-5	Schottky barrier height lowered by field-assisted tunneling effects.	50
3.3-6	Calculated thermionic emission current density (solid lines) and recombination current density (dashed lines) under reverse bias.	51
3.3-7	(a) Schottky barrier height lowered by effects of an interfacial layer (SiO ₂ , 10Å); and (b) the related ideality factor, n (D_s , is $2 \times 10^{13} \text{ eV}^{-1} \text{ cm}^{-2}$).	53
3.3-8	Forward I - V characteristics of an InP Schottky diode at temperatures from 120 to 330K.	54
3.3-9	Semi-log plots of the forward I - V of an InP Schottky diode at temperatures from 120 to 330K.	55

3.3-10	Measured Schottky barrier heights from forward I - V data at temperatures from 120 to 330K.	55
3.3-11	Measured ideality factor from forward I - V data at temperatures from 120 to 330K.	56
3.3-12	The Richardson plot (open circles) of forward I - V data of an InP Schottky diode. For an ideal Schottky diode, the plot is expected to be linear.	56
3.3-13	The Richardson plot of reverse-biased I - V data at -0.1V.	57
3.3-14	Plots of I/C^2 vs V_r in a temperature range of 120 to 330K.	59
3.3-15	Schottky barrier height obtained from C - V measurement decreases slightly as temperature increases.	60
3.3-16	Schottky barrier heights obtained from C - V and I - V data as a function of temperature.	60
3.3-17	Plot of $(\phi_b^{C-V}(0, T) - \phi_b^{I-V}(0, T))$ as a function of q/kT	66
3.3-18	The ideality factor, n_1 , obtained from experimental data by eq.(2.4-23) at various temperatures.	67
3.3-19	The ideality factors, n_1 and n_2 , are shown together as a function of temperature.	68
3.3-20	The Richardson plots of forward I - V data of an InP Schottky diode.	69
3.3-21	The Richardson plots of reverse-biased I - V data at -0.1V.	69
3.3-22	Schottky barrier heights, $SBH(0,0)$, obtained by temperature dependent C - V , forward- and reverse-biased I - V measurements.	72
3.3-23	The ideality factor, n , is shown as a function of temperature for InP Schottky diodes with different contact areas.	72
3.3-24	The ideality factors of $In_{1-x}Ga_xP$ Schottky diodes increase dramatically as temperature is lowered, and are relatively constant at around room temperature.	74
3.3-25	Barrier heights of $In_{1-x}Ga_xP$ Schottky diodes, $SBH(0,0)$, measured as a function of the compositional factor, x	74
3.3-26	Measured standard deviation of the barrier height as a function of the compositional factor, x , in $In_{1-x}Ga_xP$ Schottky diodes.	75
3.3-27	Zero-bias barrier heights of $In_{1-x}Ga_xP$ Schottky diodes as a function of the compositional factor, x , measured at room temperature.	75

3.3-28	Ideality factors, n , of $\text{In}_{1-x}\text{Ga}_x\text{P}$ Schottky diodes as a function of the compositional factor, x , measured at room temperature.	77
3.3-29	The Richardson constant, A^* , measured at 300K, varies with the compositional factor, x , in $\text{In}_{1-x}\text{Ga}_x\text{P}$ Schottky diodes.	77
3.3-30	(a) Forward-biased and (b) reverse-biased characteristics of the $\text{InP}/\text{InGaAs}/n^+\text{-InP}$ Schottky diodes with (solid) and without (dashed) $\text{In}_{1-x}\text{Ga}_x\text{P}$ barrier enhancement layer on top.	82
4.3-1 a&b	Auger electron spectra of InP (sample #1): a) as received; b) after 30 second sputtering. The InP sample was passivated by $(\text{NH}_4)_2\text{S}_x$, 600 W tungsten light illumination, for 20 minutes.	92
4.3-1 c&d	Auger electron spectra of InP (sample #2): c) as received; d) after 30 second sputtering. The InP sample was passivated by $(\text{NH}_4)_2\text{S}_x$, 600 W tungsten light illumination, for 20 minutes, then was annealed at 300°C for 20 seconds.	93
4.3-1 e&f	Auger electron spectra of InP (sample #3): e) as received; f) after 30 second sputtering. The InP sample was passivated by $(\text{NH}_4)_2\text{S}$ at room temperature for 45 minutes.	94
4.3-1 g&h	Auger spectra of InP (sample #4) without any sulfide passivation: g) as received; h) after 30 second sputtering.	95
4.3-2a	Room temperature photoluminescence of InP.	96
4.3-2b	Low temperature photoluminescence of InP.	97
4.3-3	PL spectra of $n^+\text{-InP}$ (A) and $p^+\text{-InP}$ (B) treated with different conditions.	98
4.3-4	Photoluminescence spectra of InP with and without surface sulfur passivation.	99
4.3-5	Barrier height of metal/InP Schottky diodes measured as a function of the metal work function before and after sulfur passivation.	100
4.3-6	Capacitance of an InP Schottky diode as a function of the bias voltage with frequency as a parameter. Sulfur passivation (open symbols) reduces the frequency dependence, compared to that of untreated device (filled symbols).	102
4.3-7	Capacitance of an InP MIS diode as a function of the bias voltage with frequency as parameter. Sulfur passivation (open symbols) reduces the frequency dependence, compared to that of the untreated device (filled symbols).	103
5.2-1	Schematic of an InGaAs MSM-PD.	114

5.2-2	Schematic of a 1D MSM-PD (a) and its energy-band diagram (b).	116
5.2-3	(a) Electric field and (b) potential profile of a 1D MSM-PD.	117
5.2-4	Schematic of a 2D MSM-PD. A unit cell is defined (0ABX ₁) for two-dimensional modeling and numerical analysis.	126
5.3-1	Experimental set-up for MSM-PDs' DC photoresponse measurements.	135
5.3-2a	Experimental set-up of the opto-electro sampling measurement system used to measure the temporal response of MSM-PDs.	136
5.3-2b	Schematic of the opto-electro sampling head used in MSM-PDs' temporal response measurement system.	137
5.4-1	a) SEM micrograph of an InGaAs MSM-PD (2×2). b) SEM micrograph of the active area of an InGaAs MSM-PD (2×2).	141
5.4-2	Capacitance of a typical InGaAs MSM-PD (2×2). The barrier layer is InP with a thickness of 500Å.	142
5.4-3	Calculated flat-band voltage of a 1D InGaAs MSM-PD as a function of carrier concentration for different thicknesses of the absorption layer.	143
5.4-4	Capacitance of InGaAs MSM-PDs (2×2) processed in different ways.	146
5.4-5	Capacitance of InGaAs MSM-PDs (2×2) with and without sulfur passivation.	147
5.4-6	AES spectra of InP passivated by (NH ₄) ₂ S _x : a) as received; b) after 30 second sputtering.	149
5.4-7	Photoluminescence of InP at room temperature.	150
5.4-8a	Dark current of a typical InGaAs MSM-PD (2×2) as a function of bias voltage at 300K.	151
5.4-8b	Photoresponse of a typical InGaAs MSM-PD (2×2).	152
5.4-9a	Dark current of an InGaAs MSM-PD (2×2) at temperatures from 120 to 330K.	155
5.4-9b	Dark current of an InGaAs MSM-PD (2×2) on a semi-log scale.	155
5.4-9c	The Richardson plot of an InGaAs MSM-PD (2×2) at 300K.	156
5.4-10	Dark currents of InGaAs MSM-PDs processed in different ways.	157
5.4-11	"Soft breakdown" characteristics of an InGaAs MSM-PD (2×2) in a temperature range of 80 - 360K.	158

5.4-12	Breakdown voltage as a function of temperature: a) InGaAs MSM-PD; b) APD.	159
5.4-13	Dark current as a function of reverse bias voltage of (a) InP/InGaAs and (b) In _{0.85} Ga _{0.15} P/InP/InGaAs Schottky diodes.	161
5.4-14	Dark currents of InGaAs MSM-PDs (2×2) with and without sulfur passivation.	165
5.4-15a	Dark currents of an InGaAs MSM-PD (2×2) at temperatures from 120 to 330 K. The MSM-PD was passivated by sulfide solution.	166
5.4-15b	Dark currents (in log scale) of an InGaAs MSM-PD (2×2) at temperatures from 120 to 330K. The MSM-PD was passivated by sulfide solution.	167
5.4-15c	Dark currents of an InGaAs MSM-PD (2×2) before and after sulfur passivation. Currents were measured at temperatures from 120 to 330 K.	167
5.4-16	Dark currents of InGaAs MSM-PDs (a) with and (b) without sulfur passivation. Currents were measured after the devices had been exposed to air for some time. ...	169
5.4-17	Photoresponses of InGaAs MSM-PDs (2×2) fabricated by different processes.	171
5.4-18	Photoresponses of an InGaAs MSM-PD (2×2) before and after sulfur passivation. ..	173
5.4-19	Responsivity of InGaAs MSM-PDs as a function of the power of the incident laser light beam.	175
5.4-20	Calculated quantum efficiency of InGaAs MSM-PDs at wavelengths of (a) 1.3μm and (b)1.55μm.	177

List of Tables

Table	Caption	Page
3.2-1	Parameters of metallization	40
3.3-1	Barrier heights of InP Schottky diodes	71
3.3-2	Barrier parameters of $\text{In}_{1-x}\text{Ga}_x\text{P}$ Schottky diodes extracted from the inhomogeneous barrier model	79
3.3-3	Barrier parameters of $\text{In}_{1-x}\text{Ga}_x\text{P}$ ($x = 0.3$) Schottky diodes	80
3.3-4	Barrier heights, ideality factors, reverse leakage currents, and breakdown voltages of the $\text{In}_{1-x}\text{Ga}_x\text{P}$ Schottky diodes	81
4.3-1	InP samples for sulfur passivation	91
4.3-2	Schottky barrier heights of different metals deposited on InP obtained from I - V measurements	100
4.3-3	Barrier height and ideality factor of Au/Ni/Pt - InP Schottky diodes	101
4.3-4	Dark currents of InP MSM-PDs	104
5.2-1	Symbols	123
5.2-2	Parameters and their meanings	123
5.2-3	Heterointerface parameters	125
5.3-1	MSM-PD samples grown by GS-MBE	127
5.3-2	Configurations of Type #1 MSM-PDs	129
5.3-3	Configurations of Type #2 MSM-PDs	130
5.3-4	Parameters of metallization	131
5.3-5	Specification of laser diode	135

5.3-6	Calibration of laser diode	135
5.4-1	Metallization schemes of InP/InGaAs MSM-PDs	138
5.4-2	Results of InP/InGaAs MSM-PDs	140
5.4-3	Calculated capacitance of InGaAs MSM-PDs	144
5.4-4	Important parameters of most commonly used III/V compounds	154
5.4-5	Schottky barrier height of $\text{In}_{1-x}\text{Ga}_x\text{P}/\text{InP}$ Schottky contacts	160
5.4-6	a) Dark currents of InGaAs MSM-PDs	163
	b) Dark currents of InGaAs MSM-PDs passivated by sulfide solution	163
5.4-7	Schottky barrier heights of InP/InGaAs MSM-PDs	166
5.4-8	Dark currents and responsivity of InP/InGaAs MSM-PDs	175

Physical Constants

Quantity	Symbol/Unit	Value
Angstrom unit	\AA	$1 \text{\AA} = 10^{-10} \text{ m} = 10^{-8} \text{ cm}$ $= 10^{-4} \mu\text{m} = 10^{-1} \text{ nm}$
Boltzmann constant	k	$1.38066 \times 10^{-23} \text{ J/K}$
Elementary charge	q	$1.60218 \times 10^{-19} \text{ C}$
Electron rest mass	m_0	$0.91095 \times 10^{-31} \text{ kg}$
Electron volt	eV	$1 \text{ eV} = 1.6021810^{-19} \text{ J}$
Permeability in vacuum	μ_0	$1.25663 \times 10^{-8} \text{ H/cm}$
Permittivity in vacuum	ϵ_0	$8.85418 \times 10^{-14} \text{ F/cm}$
Planck constant	h	$7.62617 \times 10^{-34} \text{ J-s}$
Speed of light in vacuum	c	$2.99792 \times 10^{10} \text{ cm/s}$
Standard atmosphere		$1.01325 \times 10^5 \text{ Pa}$
Thermal voltage at 300K	kT/q	0.0259 V
Wavelength of 1-eV quantum	λ	$1.23977 \mu\text{m}$

List of Symbols

Symbol	Physical Meaning	Unit
A	Richardson constant, corresponding to free-electron mass	$\text{Acm}^{-2}\text{K}^{-2}$
A^*	Richardson constant, corresponding to effective mass in semiconductor	$\text{Acm}^{-2}\text{K}^{-2}$
A^{**}	value of A^* corrected for quantum-mechanical reflection and phonon backscattering	$\text{Acm}^{-2}\text{K}^{-2}$
b	temperature coefficient of ϕ_{bn}	eV/K
C	differential capacitance per unit area ($= dQ/dV$)	Fcm^{-2}
C_d	capacitance per unit area associated with depletion region	Fcm^{-2}
C_{ox}	capacitance per unit area associated with interfacial oxide layer	Fcm^{-2}
C_r	capacitance per unit area	Fcm^{-2}
C_t	capacitance per unit area associated with deep traps	Fcm^{-2}
C_ϕ	constant (eq.(1-10))	eV
D_n	diffusion constant for electrons in n-type semiconductor	cm^2/s
D_h	diffusion constant for holes in n-type semiconductor	cm^2/s
D_s	density of surface states	$\text{eV}^{-1}\text{m}^{-2}$
e_n	probability per unit time of trap emitting an electron	s^{-1}
e_p	probability per unit time of trap emitting a hole	s^{-1}
E	electric field strength	Vcm^{-1}
E_c	energy of bottom of conduction band in semiconductor	eV
ΔE_c	conduction band discontinuity in heterostructure	eV
E_F	Fermi energy	eV
E_F^m	Fermi level in metal	eV
E_F^s	Fermi level in semiconductor	eV
E_{Fn}	quasi-Fermi level in the semiconductor	eV

E_g	energy gap of semiconductor	eV
E_i	intrinsic Fermi level of semiconductor	eV
E_m	maximum of electric field in the barrier	Vcm ⁻¹
E_t	energy of trap	eV
E_V	energy of top of valence band	eV
E_n	(eq.(2.2-24))	eV
E_{oo}	(eq.(2.2-21))	eV
f_s	probability of occupation of interface state	
h	Planck's constant	J-s
I	current	A
I_d	reverse leakage current of Schottky diodes, or dark current of MSM photodetectors	A
J	current density	Acm ⁻²
J_n	reverse saturation current density	Acm ⁻²
J_e	current density due to electrons	Acm ⁻²
J_h	current density due to holes	Acm ⁻²
J_{sm}	current density from semiconductor to metal	Acm ⁻²
J_{ms}	current density from metal to semiconductor	Acm ⁻²
J_{ie}	current density due to thermionic emission	Acm ⁻²
J_r	current density due to recombination in depletion region	Acm ⁻²
J_{ro}	(eq.(2.2-29))	Acm ⁻²
J_g	current density due to generation in depletion region	Acm ⁻²
k	Boltzmann's constant	J/K
l	mean free path of electrons	m
L	thickness of quasi-neutral region, or thickness of the semiconductor in a 1D MSM structure	m
L_e	diffusion length of electrons	m

m	free-electron mass	kg
m_n		kg
m^*	effective mass of electrons in semiconductor	kg
m_r	relative electron mass to m_n	
n	density of electrons in conduction band of semiconductor or ideality factor	cm^{-3}
n_1	ideality factor	
n_2	ideality factor	
n_i	intrinsic electron concentration	cm^{-3}
n_m	electron density at x_m	cm^{-3}
n_n	electron density at x_m under quasi-equilibrium condition	cm^{-3}
N_c	effective density of states in conduction band of semiconductor	cm^{-3}
N_d	donor density	cm^{-3}
N_{ss}	interface state density per unit area per energy eV	$\text{eV}^{-1}\text{cm}^{-2}$
N_t	trap density	cm^{-3}
N_v	effective density of states in valence band of semiconductor	cm^{-3}
p	density of holes in valence band of semiconductor	cm^{-3}
p_0	equilibrium density of holes at edge of depletion region	cm^{-3}
q	magnitude of electronic charge	C
Q_d	charge per unit area due to uncompensated donors	Ccm^{-2}
Q_h	charge per unit area due to holes	Ccm^{-2}
Q_m	charge per unit area on surface of metal	Ccm^{-2}
Q_{ss}	charge per unit area due to surface states	Ccm^{-2}
S	area of contact	cm^2
S_b	coefficient of barrier height dependent on metal work function	
T	absolute temperature	K
T_n	temperature parameter	K

U	generation rate in semiconductor	$\text{cm}^{-3}\text{s}^{-1}$
\bar{v}	mean thermal velocity of electrons or holes	cms^{-1}
v_d	diffusion velocity	cms^{-1}
v_r	recombination velocity	cms^{-1}
V	applied bias voltage (positive for forward bias)	V
V_B	breakdown voltage	V
V_d	diffusion voltage or "band bending"	V
V_{d0}	diffusion voltage at zero bias	V
V_i	potential drop across interfacial layer	V
V_r	reverse biase (= - V)	V
V_{RT}	reach-through voltage, eq.(5.2-5)	V
V_{FB}	flat-band voltage, eq.(5.2-6)	V
w	width of depletion region	Å
x_m	position of maximum of barrier	Å
α	coefficient of barrier height dependent on electric field	cm
α_σ	coefficient of σ_s^2 dependent on temperature	$(\text{eV})^2/\text{K}$
α_ϕ	temperature dependent coefficient of barrier height	eV/K
β	= q/kT	$(\text{eV})^{-1}$
γ	(eq.(1-4))	
δ	thickness of interfacial layer	Å
ϵ_0	permittivity of free space	F/cm
ϵ_i	permittivity of interfacial layer (= $\epsilon_r\epsilon_0$)	F/cm
ϵ_{ir}	relative permittivity of interfacial layer	
ϵ_s	static permittivity of semiconductor (= $\epsilon_r\epsilon_0$)	F/cm
ϵ_s'	high-frequency permittivity of semiconductor	F/cm
ϵ_{sr}	relative permittivity of semiconductor	

ξ_n	quasi-Fermi level (or imref) for electrons	eV
ξ_p	quasi-Fermi level (or imref) for holes	eV
λ	wavelength of light wave	nm
μ_n	mobility of electrons	$\text{cm}^2/\text{V}\cdot\text{s}$
μ_p	mobility of holes	$\text{cm}^2/\text{V}\cdot\text{s}$
ν	frequency of light wave	Hz
ξ	$= E_c - E_F^s$	eV
ρ_2	bias dependent coefficient of barrier height	eV/V
ρ_3	bias dependent coefficient of σ_s^2	$(\text{eV})^2/\text{V}$
σ_n	capture cross-section for electrons	cm^2
σ_p	capture cross-section for holes	cm^2
σ_r	standard deviation in Gaussian distribution of the barrier height	eV
τ_r	recombination time in the depletion region	s
τ_{re}	recombination time for electrons	s
τ_{rh}	recombination time for holes	s
τ	carrier transit time in MSM photodetectors	s
τ_e	transit time for electrons	s
τ_h	transit time for holes	s
τ_p	hole life time in semiconductor	s
τ_n	electron life time in semiconductor	s
ϕ_b	height of Schottky barrier (measured from E_F^m)	eV
$\overline{\phi_b}$	mean value of barrier height	eV
ϕ_{bn}	barrier height at zero-bias	eV
ϕ_b^u	barrier height for zero-electric field (flat-band barrier height)	eV
ϕ_{bn}''	flat-band barrier height for n-type semiconductor	eV

ϕ_e	effective barrier height ($=\phi_h - \Delta\phi_h$)	eV
ϕ_{eo}	effective barrier height at zero-bias	eV
ϕ_m	work function of metal	eV
ϕ_s	work function of semiconductor	eV
ϕ_o	neutral level for surface states	eV
$\Delta\phi_{bi}$	lowering of barrier due to image force	eV
$(\Delta\phi_{bi})_o$	image-force lowering at zero-bias	eV
χ_s	electron affinity of semiconductor	eV
ψ	electrostatic potential	V
ω_b	angular frequency of bias modulation	
ω_t	angular frequency of test signal	

Note: MKS units are used throughout in this thesis. All energies are measured in eV, so that the magnitude of the potential energy of an electron associated with its electrostatic potential is equal to the potential measured in volts.

Chapter 1

INTRODUCTION

1.1 TECHNICAL IMPORTANCE OF InP AND RELATED MATERIALS

Indium phosphide and related alloys, especially InGaAs and InGaAsP, have become important materials for applications in many electronic and photonic devices because of their high electron mobilities and high-saturation electron-drift velocities. The ternary alloy, InGaAs [Jalali, 1992], and the quaternary alloy, InGaAsP [Dutta, 1992], grown lattice matched to InP, are the materials of choice for making light sources and detectors in the wavelength range of 1.3 - 1.6 μm for the present-day high-data-rate, long-haul, fibre-optic communication systems [Soole, 1991]. High-speed electronic devices, such as heterojunction bipolar transistors (HBTs) [Jalali, 1992] and high-electron mobility transistors (HEMTs) [Guan, 1995, Mesquida Küsters, 1995, Hur, 1995] are being realized from InGaAs/InP and InGaAs/InAlAs heterostructures. Recently, high performance InP-based optoelectronic integrated circuits (OEICs), such as metal-semiconductor-metal photodetector and high-electron-mobility transistors (MSM-HEMTs) [Hong, 1991,

Chang, 1991, Fay, 1996] and p-i-n photodetectors and field-effect-transistors (PIN-FETs) [Park, 1993, Akatsu, 1993] as photoreceivers have been fabricated monolithically.

Compared to GaAs, InP has a higher peak electron-drift velocity and a higher breakdown electric field. These facts yield advantages of InP over GaAs for the fabrication of low-noise and high-power Schottky gate FETs. In addition, InGaAs and InGaAsP, which are promising materials for long wavelength communication optoelectronic devices, can be grown lattice matched to InP. Moreover, InGaAsP can be engineered in band gap energy for novel structures.

However, serious drawbacks of InP are the low Schottky barrier height of metal contacts and the difficulty in surface quality control. These result in increased Schottky gate leakage currents, and a degradation of the device performance.

1.2 SCHOTTKY CONTACTS TO InP

1.2.1 Classic Model

According to the Schottky-Mott model [Schottky], the barrier height, ϕ_b , of an ideal intimate metal-semiconductor contact is given by the difference of the metal work function, ϕ_m , and the semiconductor electron affinity, χ_s ,

$$\phi_b = \phi_m - \chi_s \quad (1-1)$$

Experimental results, however, rarely obey eq.(1-1). Bardeen [1947] attempted to explain the anomaly by proposing that the Fermi-level is "pinned" or "stabilized" by the

* Note: MKS units are used throughout in this thesis. All energies are measured in eV, so that the magnitude of the potential energy of an electron associated with its electrostatic potential is equal to the potential measured in volts.

surface states to an energy of ϕ_o (in eV) above the valence band. The Schottky barrier height is then given by

$$\phi_b = E_g - \phi_o \quad (1-2)$$

where E_g is the energy band gap of InP, and ϕ_o is called the "neutral energy level" .

In practice, experimental results of barrier-height measurements obey neither the Schottky-Mott model of eq.(1-1) nor the Bardeen model of eq.(1-2). Cowley and Sze [1965] proposed a more general model in which a thin interfacial layer is introduced between the metal and the semiconductor. The barrier height under flat-band conditions is given by

$$\phi_b^o = \gamma(\phi_m - \chi_s) + (1 - \gamma)(E_g - \phi_o) \quad (1 - 3)$$

where γ is a dimensionless parameter, defined as

$$\gamma \equiv \epsilon_i / (\epsilon_i + qN_{ss}\delta) \quad (1 - 4)$$

and q is the electron charge, ϵ_i and δ are the permittivity and thickness of the interfacial layer. The surface states are characterized by the density N_{ss} (per unit area per unit energy in eV) and the neutral level ϕ_o . Because the potential drops across the interfacial layer as well as the depletion region in the semiconductor, the real barrier height, ϕ_b , is not equal to ϕ_b^o at zero-bias. It is given by

$$\phi_b = \phi_b^o - \alpha E_m \quad (1 - 5)$$

where E_m is the maximum value of the electric field in the semiconductor, and α is a parameter with dimension of length and is given by

$$\alpha = \delta \epsilon_s / (\epsilon_i + qN_{ss} \delta) \quad (1 - 6)$$

The maximum electric field, E_m , is given by

$$E_m = [(2qN_D/\epsilon_s)(V_d - kT/q)]^{1/2} \quad (1 - 7)$$

where $V_d = \phi_b^o - \xi - V$ is the built-in potential. ξ is the energy (in eV) difference between the conduction band minimum and the quasi-Fermi level in the semiconductor, while V is the applied voltage. N_D is the carrier concentration in the semiconductor, k the Boltzmann constant, and T the temperature.

A distinct mechanism that can lead to a reduction in barrier height, $\Delta\phi_b$, is that of image-force-lowering, which is given by [Rhoderick, 1988]

$$\Delta\phi_b = \left(\frac{qE_m}{4\pi\epsilon_s} \right)^{1/2} \quad (1 - 8)$$

So, the barrier height is

$$\phi_b = \phi_b^o - \alpha E_m - \Delta\phi_b = \phi_{bo}^o - \Delta\phi_b \quad (1 - 9)$$

where $\phi_{bo}^o = \phi_b^o - \alpha E_m$ is the zero-bias barrier height without considering image-force lowering.

Schottky barrier heights of metals on InP were reported to have values from 0.36 to 0.56 eV [Robinson, 1985], almost independent of the metal work function. Instead, it was found that the barrier height is dependent on the InP substrate (carrier concentration and substrate crystal orientation), the method used to grow the epitaxial layer, and the surface cleaning processes.

Williams [Williams, 1978] demonstrated that chemical effects on vacuum cleaved (or so called atomically clean) InP (110) surfaces play an important role in determining ϕ_b . A clear dependence of ϕ_b on the reactivity of the metal with InP was found. Metals

such as Ni, Fe, and Al, which form compounds with phosphorus that are significantly more stable than InP yield contacts with low barrier heights and ohmic behavior. Metals such as Au, Ag, and Cu, which form phosphides that are less stable than InP produce barrier heights of about 0.5 eV. Brillson [Brillson, 1982] confirmed these observations and also showed that reactive metal-InP diodes exhibit an abrupt interface and predominant outdiffusion of In, while non-reactive metal-InP diodes exhibit diffuse interfaces and predominant outdiffusion of P.

However, the chemical effects are less pronounced on chemically etched surfaces [Hökelek, 1982] than on atomically clean surfaces mentioned above. It was found that the Schottky barrier height is more sensitive to the metal work function after the InP surface was passivated by a sulfur solution [Kwon, 1995a], which indicates that the sulfur treatment reduces the surface Fermi-level pinning.

1.2.2 Mechanisms of Barrier Formation

Although various Schottky devices have been designed and fabricated, the fundamental physical mechanisms governing the barrier formation are not well understood. For InP, GaAs and other III-V semiconductors, the Fermi level at the metal-semiconductor interface is found to be pinned and thus the barrier height is almost independent of the metal work function. Over the years, several models have been proposed to explain the Schottky barrier formation. The following gives a brief summary of the most important aspects of these models.

I) Linear Interface Model

Experimentally obtained values of the Schottky barrier height were found to lie between the Schottky-Mott model and the Bardeen model. Kurtin et al. [Kurtin, 1969] proposed a linear interface model where the barrier height, ϕ_b , was assumed to be linearly dependent on the work function of the metal.

$$\phi_b = S_\phi \phi_m + C_\phi \quad (1 - 10)$$

where S_ϕ is a dimensionless parameter that reflects the sensitivity of ϕ_b to the metal, and C_ϕ is a constant. S_ϕ was found to be strongly dependent on the chemical bonding in the semiconductor, and is close to unity for ionic materials and about 0.1 for covalently bonded materials, such as Ge, Si, GaAs and InP [Mead, 1966]. More recently, Schlüter showed that the validity of the parameter S_ϕ is in question [Schlüter, 1978].

II) Metal Induced Gap States (MIGS) Model

Heine [1965] and Tersoff [1984] suggested that the Fermi level pinning is an inherent property of ideal metal-semiconductor interfaces. Heine [1965] pointed out that any intrinsic electron states which may be present on a free semiconductor surface will be replaced by metal-induced gap states (MIGS) when metal is deposited on that surface. These MIGS are associated with the tails of the conduction electron wave functions in the metal which tunnel into the band gap of the semiconductor at the interface, with an attenuation length of the order of a few Angstroms (Å). This theory does not take into account the atomic structure and bonding at the interface.

III) Unified Defect Model (UDM)

Spicer and co-workers [1980] proposed that defects are generated near the semiconductor surface when the contact metal is deposited on that surface. These defects in turn lead to pinning of the Fermi-level. This is called the unified defect model (UDM). Hughes [1986] suggested that the pinning is caused by extrinsic defects in the semiconductor resulting from the incorporation of impurities or the deposited metal atoms into the semiconductor lattice. "Dangling bonds" at incoherent or semi-coherent metal-semiconductor interfaces were also suggested to be responsible for the Fermi-level pinning [Sankey 1985].

IV) Effective Work Function Model

Another approach to understanding the metal-semiconductor interface is the effective-work-function model proposed by Woodall [1981] and Freeouf [1981]. In this model, the Schottky barrier height, ϕ_b , is not determined by surface states but rather is related to the work functions of several different metallic-like phases at the metal-semiconductor interface.

All the models mentioned above have their limitations. At present, the formation mechanisms of the Schottky barrier are still not well understood. The progress in the preparation of ideal or near-perfect semiconductor surfaces by molecular beam epitaxy (MBE) and the progress in surface analysis techniques will provide more powerful tools to help in the understanding of the barrier formation and the Fermi-level pinning.

1.3 CONDUCTION MECHANISMS IN SCHOTTKY BARRIERS

The current-voltage characteristics of a Schottky diode are generally described by thermionic emission [Sze, 1981, Rhoderick, 1988]. Crowell and Sze [1966] modified the thermionic emission theory by including the effects of diffusion. Simmons and Taylor [1983] generalized the theory by defining proper boundary conditions. Modifications including drift and diffusion, image-force lowering, recombination in the depletion region, and field-assisted tunneling may be required to some extent, depending on the semiconductor structure and temperature.

For undoped or slightly doped n-type InP, thermionic emission dominates the current transport in the temperature range of 80 K - 360 K. Recombination in the depletion region may be important in semiconductors with relatively small band gap, high Schottky barrier, in low forward biases or in reverse biases, and at low temperatures [Wittmer, 1990, 1991]. Field-assisted tunneling is significant only in highly doped semiconductors and at very low temperatures [Padovani and Stratton, 1966, Crowell and Rideout, 1969]. The existence of an interfacial layer between the metal and the semiconductor, such as a thin oxide layer, may play an important role in the current transport in a Schottky diode. Growing the structure by MBE and keeping the grown structure from being exposed to air before metallization can minimize these effects.

For most Schottky diodes, both of Si [McCafferty, 1996, Wittmer, 1990, 1991, Aboelfotoh, 1991], InP [Tuck, 1982, Thomas 1992], GaAs [Nathan, 1996], and AlGaAs [Revva, 1993], departure from ideal thermionic emission has been observed. It was found that the ideality factor, n , increases dramatically when the temperature is lowered and

attains values much higher than unity at low temperatures. Moreover, the so-called Richardson plot commonly used to extract the Schottky barrier height was not linear. Instead, a modified Richardson plot explicitly including n which was used to extract the Schottky barrier height. For undoped or weakly doped semiconductors, it has been found that the departure can not solely be explained by image-force lowering, tunneling effects, or the recombination current in depletion region.

1.4 SUMMARY OF THE RESEARCH DESCRIBED IN THIS THESIS

1.4.1 Conduction Mechanism in InP Schottky Diodes

To explain the Schottky barrier anomalies, the inhomogeneous barrier model initially proposed by Werner [1991] was modified to describe the current-voltage characteristics of Schottky diodes by introducing another ideality factor and a mean virtual barrier height. In this modified model, the barrier height is assumed to have a Gaussian distribution about a mean value with a standard deviation which is both temperature and bias dependent. Instead of discussing the microscopic details of the barrier fluctuation, I am focusing on explaining the experimental current-voltage characteristics, such as the temperature-dependent ideality factors and the temperature-and-bias dependent barrier height. It will be shown that the modified Richardson plot is a direct result of such a model, as is the so-called “ T_0 Effect” under certain conditions. The details of this inhomogeneous model will be presented in Chapter 2. Experimental results on InP and $\text{In}_{1-x}\text{Ga}_x\text{P}/\text{InP}$ Schottky diodes will be given in Chapter 3.

1.4.2 Metallization Schemes for Metal-InP Schottky Contacts

A systematic investigation of metallization schemes for Schottky contacts to InP was implemented. Different metals, such as Au, Al, Ni, Ti, Pt, W, and their combinations, such as Au/Al, Au/Pt, Au/Ti, Au/Ti/Pt, Au/Pt/Ti, Au/Ni/Pt, Au/Pt/Ti/Pt, and Au/Ti/W were employed. The thermal stability of these metallization schemes was investigated by conducting rapid thermal annealing (RTA) of the structures. The Au-based metallization schemes were deposited by electron-beam evaporation in high vacuum conditions. Refractory metals and their nitride compounds were deposited using RF sputtering.

The results for various metallization schemes for Schottky diodes are discussed in Chapter 3. In Chapter 5, metallization schemes for MSM-PDs will be discussed.

1.4.3 Surface Passivation of InP

Although InP and related materials have promising potential applications in microelectronic and optoelectronic devices, the difficulty in controlling their surface states is a big drawback. As mentioned in previous sections, surface states in InP play a very fundamental role in the Schottky barrier formation and surface recombination velocity (SRV), and limit the performance of devices made from it. Passivation of InP surfaces has received much attention in the past ten years because it can tremendously improve the semiconductor surface electronic properties.

In our investigations, a sulfide solution, $(\text{NH}_4)_2\text{S}_x$, was used to passivate the InP surface. First, passivation conditions were optimized. Then, various passivation sequences as part of the device fabrication processes were investigated. Passivation of the

whole surface of the wafer, of only the active areas, of areas underneath the metal contacts, or after lift-off were carried out. Finally, various devices, such as InP Schottky diodes, InP MIS diodes, InP MSM-PDs and InP/InGaAs MSM-PDs were passivated by sulfur solutions. The performance of such sulfur-passivated devices was generally improved. Results are presented in Chapter 4. Sulfur passivation of InP/InGaAs MSM-PDs will be discussed in Chapter 5.

1.4.4 Barrier Enhancement on InP Using $\text{In}_{1-x}\text{Ga}_x\text{P}$

The barrier height of InP Schottky diodes is about 0.4 - 0.5 eV, which is not high enough for some device applications. Many methods were proposed to increase the InP Schottky barrier height, such as the fabrication of p^+/n -InP structures [Tyagi, 1993, Schwartz, 1986, Van Der Ziel, 1977, Roy, 1982], the incorporation of interfacial layers [Hattori, 1991], and the use of wide band gap materials such as $\text{In}_{1-x}\text{Ga}_x\text{P}$ [Pang, 1995, Kordoš, 1992, Gaonach, 1990]. The aim of using p^+/n -InP is to modify the band bending while the employment of an interfacial layer is basically to reduce the carrier tunneling through the M-S interface. The choice of $\text{In}_{1-x}\text{Ga}_x\text{P}$ as the barrier enhancement layer is made to take advantage of the $\text{In}_{1-x}\text{Ga}_x\text{P}$ wider band gap properties.

In our investigation, epitaxial layers of InP and $\text{In}_{1-x}\text{Ga}_x\text{P}$ with different composition factors, x , and thicknesses were grown by MBE on n^+ -InP substrates. Schottky diodes were made on such structures to evaluate the enhanced Schottky barrier heights, ideality factors, and current-voltage characteristics. Preliminary results of this investigation were

presented in 1995 [Pang .1995]. This project was orientated toward the design and fabrication of InP/InGaAs/InP MSM-PDs with InGaP as the barrier enhancement layer.

The current-voltage characteristics of $\text{In}_{1-x}\text{Ga}_x\text{P}$ were analyzed based on the model developed in Chapter 2. Results for $\text{In}_{1-x}\text{Ga}_x\text{P}$ /InP Schottky diodes are presented in Chapter 3. InGaAs/InP MSM-PDs with $\text{In}_{1-x}\text{Ga}_x\text{P}$ as the barrier layer are discussed in Chapter 5.

1.4.5. Design, Fabrication and Characterization of InGaAs MSM

Ultra-fast InGaAs MSM photodetectors in the wavelength range from 1.3 to 1.55 μm are in the focus of interest for long-haul optical fiber communication systems and interconnects, especially those with data transmission rates beyond 10 Gbits/s. This means that impulse response times in the range of 10 ps and bandwidths up to 100 GHz are required. Vertical *p-i-n* and Schottky photodiodes making use of InGaAs or GaAs as photoactive materials have been successfully fabricated to meet these requirements. The trend towards monolithical integration of optoelectronic circuits, however, has stimulated appreciable research activities directed towards the development of ultra-wide band planar photodetectors which can be easily fabricated and are compatible with the MESFET or HFET processes. The finger interdigitated MSM-PD is the potentially most promising candidate which meets these requirements. Due to its lower parasitic capacitance, high-speed performance, simplicity of fabrication, and compatibility with FETs in monolithical integration, MSM-PDs are getting more and more attention as photoreceivers in long-wavelength optical communication systems. Although an MSM-

PD has lower responsivity compared to a PIN photodetector. It still has a large responsivity-bandwidth product. Therefore, a large-area MSM-PD can still have reasonably high bandwidth and sensitivity.

The fabrication of photodetectors for the long-wavelength range using the InGaAs-InP material system is complicated by the relatively low Schottky barrier height (~ 0.2 eV) on InGaAs. This will result in large leakage current, low breakdown voltages, and photocurrent gain.

In the course of this work, several issues directly related to the fabrication of high quality MSM-PDs have been addressed.

I. Barrier Enhancement Layer

In order to overcome the problems of low barrier height and large leakage currents, the investigations of InGaAs MSM-PDs have been focused on devices with additional epitaxial cap layers having a larger bandgap than InGaAs. Such layers, which serve to enhance the Schottky barrier height, have been grown using materials both lattice-matched and lattice-mismatched to InGaAs, with a typical thickness of several hundred Angstroms.

Although InGaAs MSM-PDs using InAlAs as the barrier enhancement layer have good performance [Soole, 1989, Kuhl 1995, Kim, 1992, Wada 1989, Burroughes, 1992, Parker 1992], disadvantages remain and problems need to be overcome. The use of InAlAs has all the usual Al-related problems, such as: the occurrence of DX centers; aging and lack of etch control; high interface state density; oxide breakdown and

oxidation of the Al-rich material. Due to the large band offset, ΔE_c , of the InAlAs/InGaAs interface, significant charge accumulation occurs at the abrupt heterojunction which will slow down the device speed. In addition, the presence of Al in the ternary compound makes the metal-organic vapor-phase epitaxy (MOVPE) growth complicated.

In our investigation, undoped InP with thicknesses of 200 - 500 Å [Pang, 1994. Song and Pang, 1995] has been epitaxially grown by MBE as the barrier enhancement layer. The performance of InGaAs MSM-PDs with such barrier enhancement layers is comparable to that of the best ones with InAlAs as barrier layers.

To further increase the Schottky barrier height, additional $\text{In}_{1-x}\text{Ga}_x\text{P}$ ($x = 0.1$ to 0.3) with thicknesses of 100 - 300 Å on top of InP has been grown by MBE. The Schottky barrier height of such structures was significantly increased [Pang, 1995, Chyi, 1994]. The performance of InGaAs MSM-PDs with such $\text{In}_{1-x}\text{Ga}_x\text{P}/\text{InP}$ barrier layers was further improved, and lower dark current and higher breakdown voltage were obtained.

II. Optimization of Fabrication Processes

In the investigation of InGaAs MSMs with InP as the barrier layer, the design of the structures and the fabrication processes were optimized to achieve the best performance of the device, as indicated by low dark current, high breakdown voltage, high responsivity, high quantum efficiency, and high response speed. InP/InGaAs/InP MSM-PDs with different InGaAs and InP thicknesses were designed, fabricated and characterized.

In addition, the function of dielectric layers, such as SiO_2 or Si_3N_4 , grown by plasma enhanced chemical vapor deposition (CVD) or electron-cyclotron-resonance chemical vapor deposition (ECR-CVD), or deposited as spin-on-glass were investigated. Au-based metallization schemes deposited by e-beam evaporation or refractory metals and their nitrides deposited by rf sputtering were also investigated. Other processes, such as mesa-etch down and thermal annealing were studied.

III. Sulfur Passivation

Because the surface states in InP play an important role in the device performance, surface control using sulfur passivation was investigated. Although the responsivity of such sulfur passivated InP/InGaAs/InP MSMs slightly decreased, the dark current was greatly reduced and the internal gain was significantly minimized. No obvious change in the frequency response was observed. Performance after sulfur passivation is more consistent from device to device.

1.5 ORGANIZATION OF THE THESIS

The research described in this thesis composes four parts: 1) theoretical and experimental investigations of the conduction mechanisms in InP Schottky diodes; 2) Schottky contacts to InP and $\text{In}_{1-x}\text{Ga}_x\text{P}/\text{InP}$ structures; 3) sulfur passivation of InP surfaces; and 4) design, fabrication and characterization of InP/InGaAs/InP MSM-PDs. The focus is to understand the physics of carrier transport mechanisms in InP Schottky barriers and related devices. The investigation of metallization, surface sulfur passivation

and barrier enhancement using $\text{In}_{1-x}\text{Ga}_x\text{P}$ is implemented to improve the performance of Schottky contacts. Applications of all these aspects were realized in the design, fabrication and characterization of InGaAs MSM-PDs using InP or $\text{In}_{1-x}\text{Ga}_x\text{P}/\text{InP}$ as the barrier enhancement layer(s).

Chapter 2 discusses the current transport mechanisms in InP Schottky barriers. An inhomogeneous barrier model, initially proposed by Werner [1991], is modified by introducing another ideality factor and a mean virtual barrier height to explain the experimental current-voltage characteristics and barrier anomalies of InP Schottky contacts. In Chapter 3, measurement techniques and the related experimental set-ups are described. Experimental results of Schottky contacts to InP and $\text{In}_{1-x}\text{Ga}_x\text{P}/\text{InP}$ are discussed using the modified model described in Chapter 2. Issues such as the effects of different metallization schemes and thermal annealing are discussed. Barrier enhancement of InP Schottky diodes using $\text{In}_{1-x}\text{Ga}_x\text{P}$ as barrier enhancement layer is investigated. The surface passivation of InP using sulfide solutions is discussed in Chapter 4. Applications of this surface sulfur passivation to InP Schottky diodes, MIS diodes, InP MSM-PDs and InP/InGaAs MSM-PDs are examined. In Chapter 5, a systematic investigation of InGaAs MSM-PDs is presented, which includes the design, fabrication, and characterization of InGaAs MSMs using InP or InGaP/InP as the barrier enhancement layer. Effects of sulfur passivation of such devices are also discussed in this chapter. Finally, a summary of the thesis is given in Chapter 6.

Chapter 2

CONDUCTION MECHANISMS IN SCHOTTKY BARRIERS

2.1 INTRODUCTION

The current density -voltage characteristic of a Schottky diode is generally described by thermionic emission [Sze, 1981]

$$J = J_0 [\exp(qV/nkT) - 1] \quad (2.1-1)$$

where q is the electron charge. V the applied voltage, k the Boltzmann constant. T the temperature, n the ideality factor, and J_0 the saturation current density given by

$$J_0 = A^* T^2 \exp(-q\phi_b/kT) \quad (2.1-2)$$

where A^* is the Richardson constant. For an ideal Schottky diode, the ideality factor, n , is unity, and the barrier height ϕ_b (in eV) is independent of temperature and bias voltage. The saturation current density, J_0 , and the ideality factor, n , can be obtained from the intercept and the slope of a plot of $\ln J$ vs V , respectively, in the form

$$\ln J = \ln J_0 + qV/nkT. \quad (2.1-3)$$

If A^* is known, the Schottky barrier height can be calculated after J_0 is determined from eq.(2.1-3),

$$\phi_b = \frac{kT}{q} \cdot \ln\left(\frac{A^* T^2}{J_0}\right). \quad (2.1-4)$$

In practice, A^* is unknown, and temperature dependent I - V measurements are employed to determine the barrier height, ϕ_b , and the Richardson constant A^* . The barrier height and the Richardson constant can be extracted by linear fitting to the Richardson plot.

$$\ln\left(\frac{J_0}{T^2}\right) = \ln A^* - \frac{q}{kT} \phi_b . \quad (2.1-5)$$

For most (both Si [Tung, 1992] and III-V semiconductors [Wittmer, 1994]) Schottky diodes, however, departure from ideal thermionic emission has been observed. It was found that the ideality factor, n , increases dramatically when the temperature is lowered (and is much larger than unity at low temperatures). Moreover, the conventional Richardson plot of $\ln(J_0/T^2)$ vs $1/T$ is not linear. Instead, a modified plot of $\ln(J_0/T^2)$ vs $1/nT$, which is linear, is used to extract the Schottky barrier height. For undoped or weakly doped semiconductors, it has been found that this departure can not be explained by image-force lowering, tunneling effects, or the recombination current in depletion region.

To explain these Schottky barrier anomalies, many models have been established such as interface states [Levine, 1971, Crowell, 1977], interfacial layers [Wu, 1980 & 1981, Türüt, 1992, Ikoma, 1993, Chattopadhyay, 1994], and barrier inhomogeneities [Werner, 1991, Tung, 1991& 1992]. Among these models, the barrier inhomogeneities model seems most successful in explaining the barrier anomalies. Werner et al. [Werner, 1991] developed the potential distribution model and obtained an analytic expression for the ideality factor. Tung [Tung, 1991& 1992] assumed an inhomogeneous barrier and obtained an expression of the current-voltage relationship for the inhomogeneous barrier.

Unfortunately, there are too many parameters in their model to be determined experimentally. They also failed to address why and how the modified Richardson plot is used, or the physics behind it. Furthermore, when the modified Richardson plot was used, the barrier height was not specified.

In the following, a general theory of the current conduction mechanisms in Schottky barrier is briefly described, then a modified current-voltage relationship based on barrier inhomogeneities, initially proposed by Werner [1991], is introduced. In this model, the Schottky barrier is assumed to be nonuniform, and the probability density of finding a certain barrier height, ϕ_b , has a Gaussian distribution about a mean value with a standard deviation which is both temperature and bias dependent. Instead of discussing the microscopic details of the barrier fluctuations, the focus lies on explaining the experimental current-voltage characteristics, such as the temperature-dependent ideality factors and the temperature-and-bias dependent barrier height. It will be shown that the modified Richardson plot is a direct result of such a modified model.

2.2 CONDUCTION MECHANISMS IN InP SCHOTTKY BARRIERS

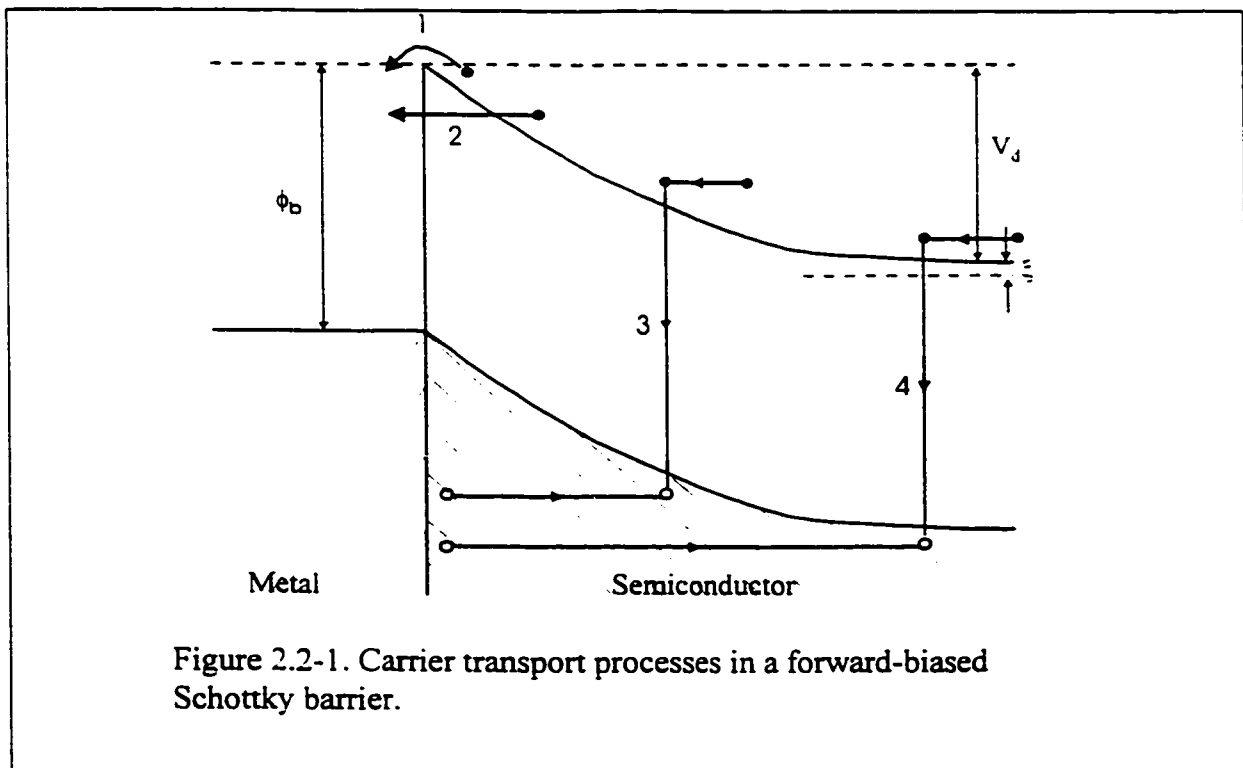
2.2.1 Current Transport Theory

Before discussing the carrier transport and the J - V characteristics of InP Schottky diodes, a brief introduction to the general theory that describes the current transport mechanisms in a Schottky diode is given below. For details of the Schottky barrier formation, the reader is referred to Sze [Sze, 1981] and Rhoderick [Rhoderick 1988].

In the following, all semiconductors are taken to be n-type InP unless otherwise specified. Figure 2.2-1 shows the various ways in which electrons can be transported across a metal-semiconductor junction under forward bias. These are:

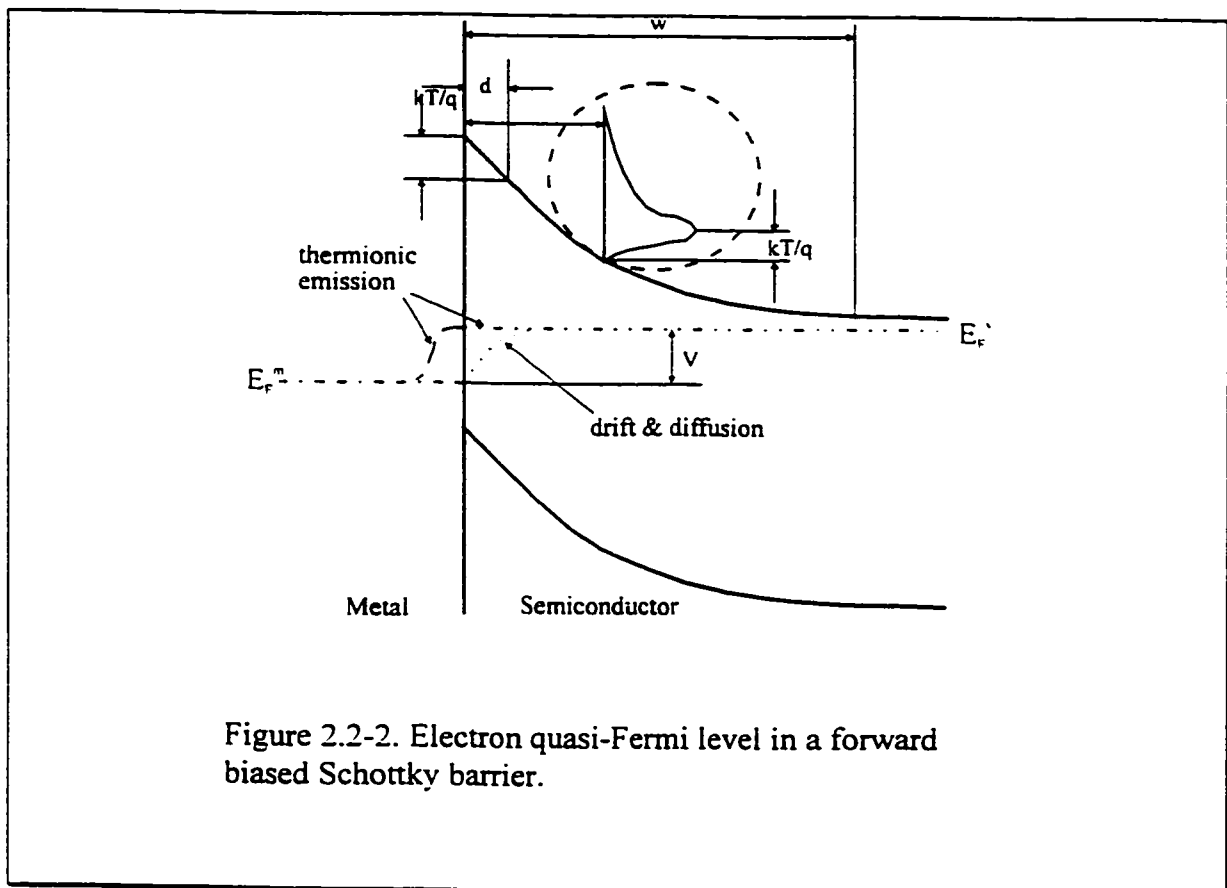
- (1) emission of electrons from the semiconductor over the top of the barrier into the metal;
- (2) quantum-mechanical tunneling through the barrier;
- (3) recombination in the space-charge region;
- (4) recombination in the neutral region (called "minority injection" or "hole injection").

There are two main processes that influence the electrons' transition across a metal-semiconductor (MS) junction. Before they can be emitted over the barrier into the metal, electrons must first be transported from the interior of the semiconductor to the interface.



This process of electrons traversing across the depletion region is governed by the usual mechanism of diffusion and drift in the electric field of the barrier. When the electrons arrive at the MS interface, their emission into the metal is governed by the rate of transfer across the boundary between the metal and the semiconductor. These two processes are effectively in series. The difference between these two theories is the behavior of the quasi-Fermi level for electrons in the conduction band of the semiconductor. It can be summarized as below:

- 1) According to thermionic emission theory, the quasi-Fermi level in the entire semiconductor is flat. It does not coincide with the metal Fermi level at the interface.



- 2) According to the diffusion theory, at the MS interface, the quasi-Fermi level of the semiconductor coincides with the Fermi level of the metal.

This difference in the positions of the quasi-Fermi levels is shown in Figure 2.2-2 [Rhoderick, 1988].

A. Thermionic Emission

In the thermionic emission theory, the effects of drift and diffusion in the depletion region are assumed to be negligible. This is equivalent to assuming an infinite mobility. The driving force ($d\mathcal{E}/dx$), the gradient of the quasi-Fermi level, is negligible. This implies that the quasi-Fermi level in the entire semiconductor is flat, which in turn implies that the concentration of electrons on the semiconductor side of the MS interface is increased by a factor of $\exp(qV/kT)$ when a bias voltage V is applied. The electron concentration on the semiconductor side of the MS interface is given by

$$n = N_c \exp[-q(\phi_b - V)/kT] \quad (2.2 - 1)$$

where N_c is the density of states of the conduction band in the semiconductor, ϕ_b the Schottky barrier height (in eV) of the metal semiconductor contact, and V the applied voltage.

The current density due to the thermionic emission of electrons over the MS barrier is given by [Sze, 1981]

$$J = J_o \cdot (e^{qV / kT} - 1) \quad (2.2 - 2)$$

with saturation current density, J_o ,

$$J_o = A^* T^2 \cdot e^{-\frac{q\phi_b}{kT}} \quad (2.2 - 3)$$

where $A^* = 4\pi m^* q k^2 / h^3$, is the Richardson constant, m^* is the effective electron mass, k the Boltzmann constant, and h the Plank's constant. For InP, $A^* = 9.2 \text{ Acm}^{-2} \text{K}^{-2}$ (n-type), and $60 \text{ Acm}^{-2} \text{K}^{-2}$ (p-type) [Katz, 1992].

B. Diffusion Theory

According to the diffusion theory, the electron concentration at the semiconductor side of the MS interface is given by

$$n = N_c \exp[-q(E_c - \xi_n)/kT] \quad (2.2 - 4)$$

where E_c (in eV) is the energy of the bottom of the conduction band, and ξ_n (in eV) is the quasi-Fermi level for electrons. The current density is given by

$$J = qn\mu E + qD_n \frac{dn}{dx} \quad (2.2 - 5)$$

where E is the electric field in the barrier, D_n the diffusion coefficient, and μ the electron mobility.

Making use of Einstein's relationship, $\mu/D_n = q/kT$, eq.(2.2-5) can be rewritten as

$$J = qn\mu \frac{d\xi_n}{dx} \quad (2.2 - 6)$$

The final current density - voltage relationship is given by [Rhoderick 1988]

$$J = J_o \cdot (e^{qV/kT} - 1) \quad (2.2 - 7)$$

where

$$J_o = q \cdot N_c \mu \cdot E_{\max} \cdot e^{-\frac{q\phi_b}{kT}} \quad (2.2 - 8)$$

The maximum field strength is given by $E_{\max} = qN_d w / \epsilon_s$, where w is the depletion width and ϵ_s the permittivity of the semiconductor.

C. The Generalized Theory

The combined thermionic emission/drift-diffusion theory was first introduced by Crowell and Sze [1966]. In this theory, one defines an effective recombination velocity, v_r , at the potential maximum. The current density due to electrons emitted over the barrier is given by

$$J = q(n_m - n_o)v_r \quad (2.2 - 9)$$

where n_m is the electron density at x_m (position of potential maximum) when the current is flowing (bias voltage is applied) and is given by

$$n_m = N_c \exp[-q(\phi_b - E_{Fn}(x_m))/kT] \quad (2.2 - 10)$$

where $E_{Fn}(x_m)$ is the quasi-Fermi level (unit in eV) at x_m under bias V , and n_o is the electron density at x_m under quasi-equilibrium condition (if it were possible to reach equilibrium without altering the magnitude or position of the potential energy maximum), and is given by

$$n_o = N_c \exp(-q\phi_b/kT) \quad (2.2 - 11)$$

Letting the diffusion current be equal to the emission current, Crowell and Sze obtained the final expression for electron current density

$$J = \frac{qN_c v_r}{1 + v_r / v_d} \cdot e^{-\frac{q\phi_b}{kT}} \cdot (e^{-\frac{qV}{kT}} - 1) \quad (2.2 - 12)$$

where

$$v_d = \left\{ \int_{x_m}^w \frac{q}{\mu kT} \cdot e^{-q(\phi_b - E_c) / kT} \cdot dx \right\}^{-1} \quad (2.2 - 13)$$

For a Maxwellian distribution of electrons and an ideal thermal emitter, the effective recombination velocity is given by

$$v_r = \frac{A^* T^2}{qN_c} \quad (2.2 - 14)$$

Simmons and Taylor [1983] generalized the theory of conduction in a Schottky barrier by defining a new boundary condition for n_m . They suggested that eq.(2.2-10) were incorrect. Instead, the electron concentration at any point in the depletion region was obtained by solving the drift and diffusion equations. This is given by (here the coordinator was reset so that the metal is at the left side and the semiconductor at the right side of the MS interface)

$$n(x) = n(0) \cdot e^{-\beta[\psi(0) - \psi(x)]} + \frac{J}{qD_n} \cdot e^{+\beta\psi(x)} \cdot \int_0^x e^{-\beta\psi(x)} dx \quad (2.2 - 15)$$

where $\psi(x)$ is the electrostatic potential, $n(0)$ is the electron density at the MS interface (on the semiconductor side). At the edge of the depletion region, the electron concentration $n(w)$ is equal to the donor concentration (n-type, fully ionized).

$$n(w) = N_d = N_c \cdot e^{-q\xi_n / kT} \quad (2.2 - 16)$$

Letting $x=w$ in eq.(2.2-15), one can obtain $n(0)$ by combining eq.(2.2-15) and eq.(2.2-16).

$$n(0) = N_d \cdot e^{\beta\psi(0)} - \frac{J}{qD_n} \cdot e^{\beta\psi(0)} \cdot \int_0^w e^{-\beta\psi(x)} dx \quad (2.2 - 17a)$$

$$= N_c \cdot e^{-q(\phi_b - E_{Fn})/kT} - \frac{J}{qD_n} \cdot e^{\beta\psi(0)} \cdot \int_0^w e^{-\beta\psi(x)} dx \quad (2.2 - 17b)$$

The difference between the Simmons & Taylor and Crowell & Sze model is that eq.(2.2-10) is replaced by eq.(2.2-17). In Simmons & Taylor's model, the final current density is given by

$$J = \frac{qN_c \cdot e^{-q\phi_b/kT} \cdot (e^{-\beta V} - 1)}{v_{th}^{-1} + v_e^{-1}} \quad (2.2 - 18)$$

where $v_e = 2D_n\beta[qN_d(V_{d0} - V)/2\varepsilon_s]^{1/2}$, and v_{th} is the same as v_r in eq.(2.2-14).

D. Image-Force Lowering

The diagram of the barrier is shown in Figure 2.2-3 when image-force lowering is considered [Sze, 1981]. The image-force lowering of the barrier height and the ideality factor are given by [Rhoderick 1988]

$$\Delta\phi_{bi} = \left[\frac{q^3 N_d}{8\pi^2 (\varepsilon_s')^2 \varepsilon_s} (\phi_b - V - \xi - \frac{kT}{q}) \right]^{1/4} \quad (2.2 - 19)$$

$$\frac{1}{n} = 1 - \frac{1}{4} \left(\frac{q^3 N_d}{8\pi^2 (\varepsilon_s')^2 \varepsilon_s} \right)^{1/4} \left[(\phi_b - V - \xi - \frac{kT}{q}) \right]^{-3/4} \quad (2.2 - 20)$$

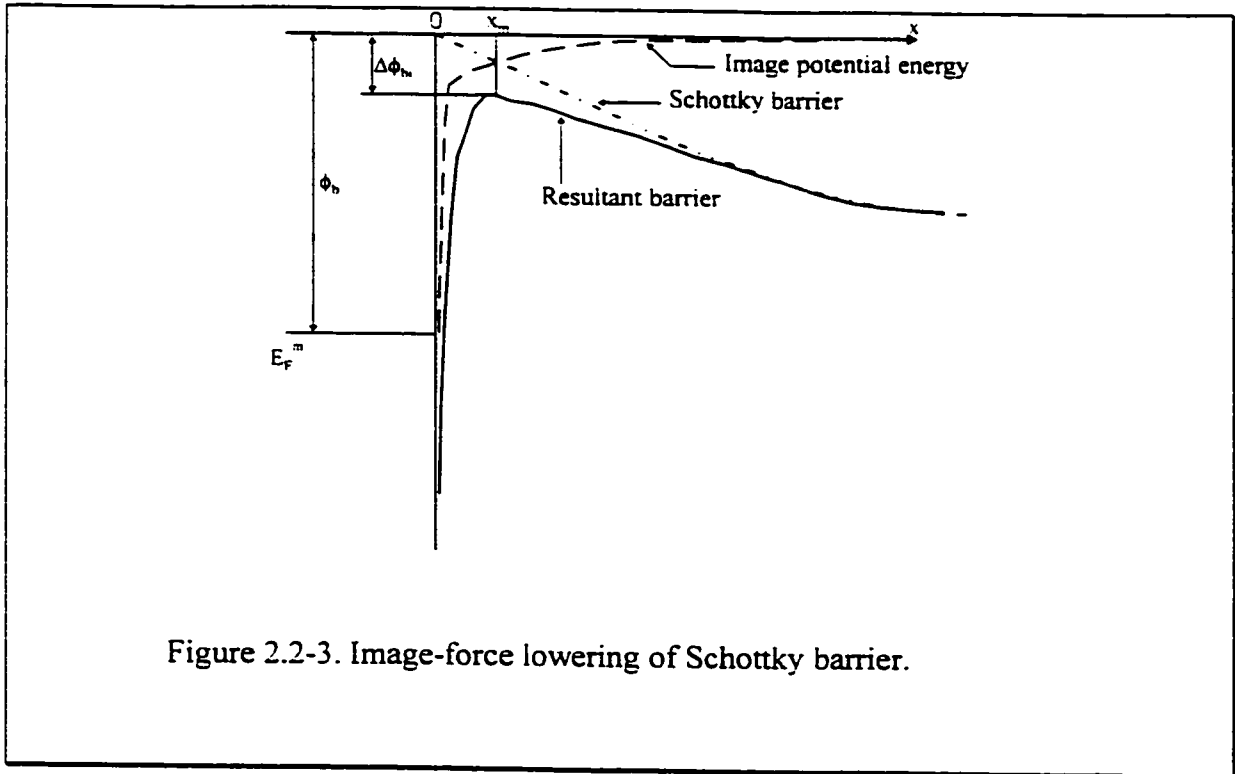


Figure 2.2-3. Image-force lowering of Schottky barrier.

where ϵ_s' is the high-frequency permittivity of the semiconductor, while ϵ_s is the static permittivity, $\epsilon_s = \epsilon_{sr} \epsilon_0$, and ϵ_{sr} is the dielectric constant of the semiconductor (for InP, $\epsilon_{sr} = 12.4$) and ϵ_0 is the free space permittivity.

2.2.2. Tunneling Through the Barrier

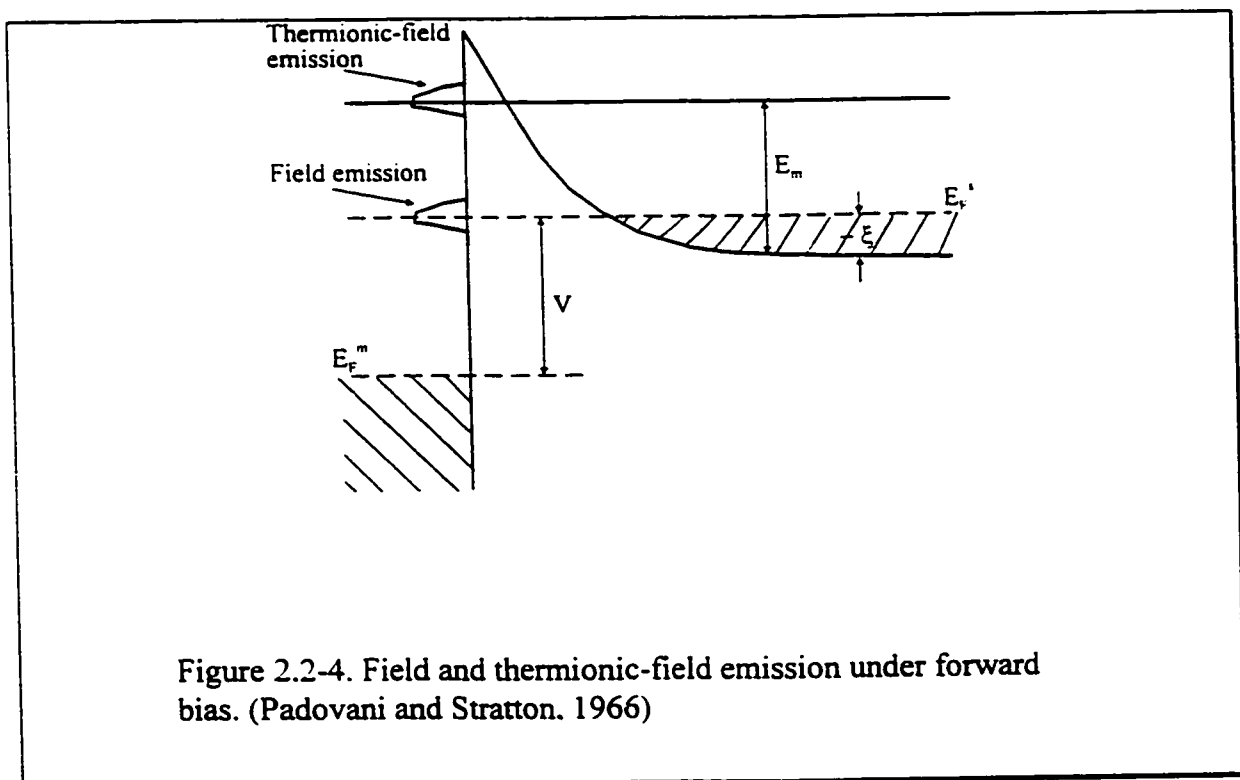
The tunneling mechanism in a Schottky barrier is depicted in Figure 2.2-4. [Rhoderick 1988]. A parameter E_{00} (unit in eV) is commonly used to characterize the tunneling effect, which is defined [Padovani and Stratton. 1966] as

$$E_{00} = \frac{h}{4\pi} \left(\frac{N_d}{m^* \epsilon_s} \right)^{1/2} \quad (2.2 - 21)$$

where m^* is the effective mass of the electrons in the semiconductor. ϵ_s is the permittivity of the semiconductor. N_d the electron concentration in the semiconductor. If $kT \gg E_{00}$, the thermionic emission dominates the carrier transport mechanism. If $kT \approx E_{00}$, the thermionic-field emission is more important. If $kT \ll E_{00}$, then field emission is the main cause for carrier transport across the metal-semiconductor interface. This is usually the case in highly doped semiconductors and/or at very low temperatures. The equivalent barrier lowering caused by thermionic-field emission for moderately doped semiconductors is

$$\Delta\phi_b \approx \left(\frac{3}{2}\right)^{2/3} (E_{00})^{2/3} (V_d)^{1/3} = \left(\frac{3}{2}\right)^{2/3} (E_{00})^{2/3} \left(\phi_b - V - \xi - \frac{kT}{q}\right)^{1/3}. \quad (2.2 - 22)$$

In the case of tunneling, the current density- voltage relationship is represented as



$$J = J_s \exp(V / E_o) [1 - \exp(-qV / kT)] \quad (2.2 - 23)$$

where

$$E_o = E_{oo} \coth(qE_{oo} / kT) \quad (2.2 - 24)$$

The ideality factor, n , can be written as

$$n = qE_o / kT = (qE_{oo} / kT) \coth(qE_{oo} / kT) \quad (2.2 - 25)$$

2.2.3. Recombination in the Depletion Region

The recombination in the space-charge region in a Schottky diode usually takes place via localized states and the most effective centers are those with energies lying near the center of the forbidden gap according to Shockley and Read [1952] and Hall [1952] (SRH), similar to a p-n junction. According to SRH, the recombination rate in the depletion region is given by

$$U = \frac{np - n_i^2}{\tau_n(n + n_i) + \tau_p(p + n_i)} \quad (2.2 - 26)$$

where τ_n and τ_p are the electron and hole life times in the semiconductor, respectively. In eq.(2.2-26), only one trap level located at the middle of the band gap and coinciding with the intrinsic level is assumed. The recombination current density component is given by

$$J_r = q \cdot \int_0^w U(x) dx \quad (2.2 - 27)$$

If simplifications for $n, p \gg n_i$, and $\tau_n = \tau_p = \tau$ can be made, the recombination current density for small forward bias is given by [Sah et al. 1957, Woods 1994]

$$J_r = J_{r0} \exp(qV / 2kT) [1 - \exp(-qV / kT)] \quad (2.2 - 28)$$

where

$$J_{r0} = qn_i w / 2 \tau_r \quad (2.2 - 29)$$

and n_i is the intrinsic electron concentration. $n_i = (N_c N_v)^{1/2} \exp(-E_g / 2kT)$, w is the depletion width

$$w = (2\epsilon_s / q N_d)^{1/2} [q(\phi_B - V - \xi - kT/q)]^{1/2}. \quad (2.2 - 30)$$

and τ_r is the carrier lifetime within the depletion region.

Including thermionic emission and recombination processes, the total current density is given by

$$J = J_{te} + J_r = J_{t0} [\exp(qV/kT) - 1] + J_{r0} \exp(qV/2kT) [1 - \exp(-qV/kT)] \quad (2.2 - 31a)$$

$$= [J_{t0} \exp(qV/kT) + J_{r0} \exp(qV/2kT)] [1 - \exp(-qV/kT)] \quad (2.2 - 31b)$$

J_{te} is the thermionic emission current density given in eq.(2.2-2) as J , while J_{t0} is same as J_0 given in eq.(2.2-3). The ratio of recombination to thermionic current is approximately given by

$$J_r / J_{te} = q(N_c N_v)^{1/2} w / (2A^{**} T^2 \tau_r) \exp[-q(E_g + V - 2\phi_B) / 2kT]. \quad (2.2 - 32)$$

The above equation shows that the recombination is more important in high barriers, in materials of short lifetime, at low temperatures, and at small forward bias voltages.

2.3 INHOMOGENEOUS BARRIER MODEL

As was mentioned in §2.1 and will be shown in Chapter 3, the current density-voltage characteristics of InP Schottky diodes depart from behavior described by eq.(2.1-1) for ideal thermionic emission. This departure is much more significant at low temperatures. The Richardson plot,

$$\ln(J_o / T^2) = \ln A^* - \frac{q\phi_b}{kT} \quad (2.3 - 1)$$

commonly used to extract the barrier height, ϕ_b , and the Richardson constant, A^* , is expected to be a linear line for $\ln(J_o/T^2)$ vs $1/T$. Experimental results, however, show that $\ln(J_o/T^2)$ vs $1/T$ is not a linear line. Furthermore, both the ideality factor, n , and the barrier height, ϕ_b , are temperature dependent. Examinations (shown in Chapter 3) show

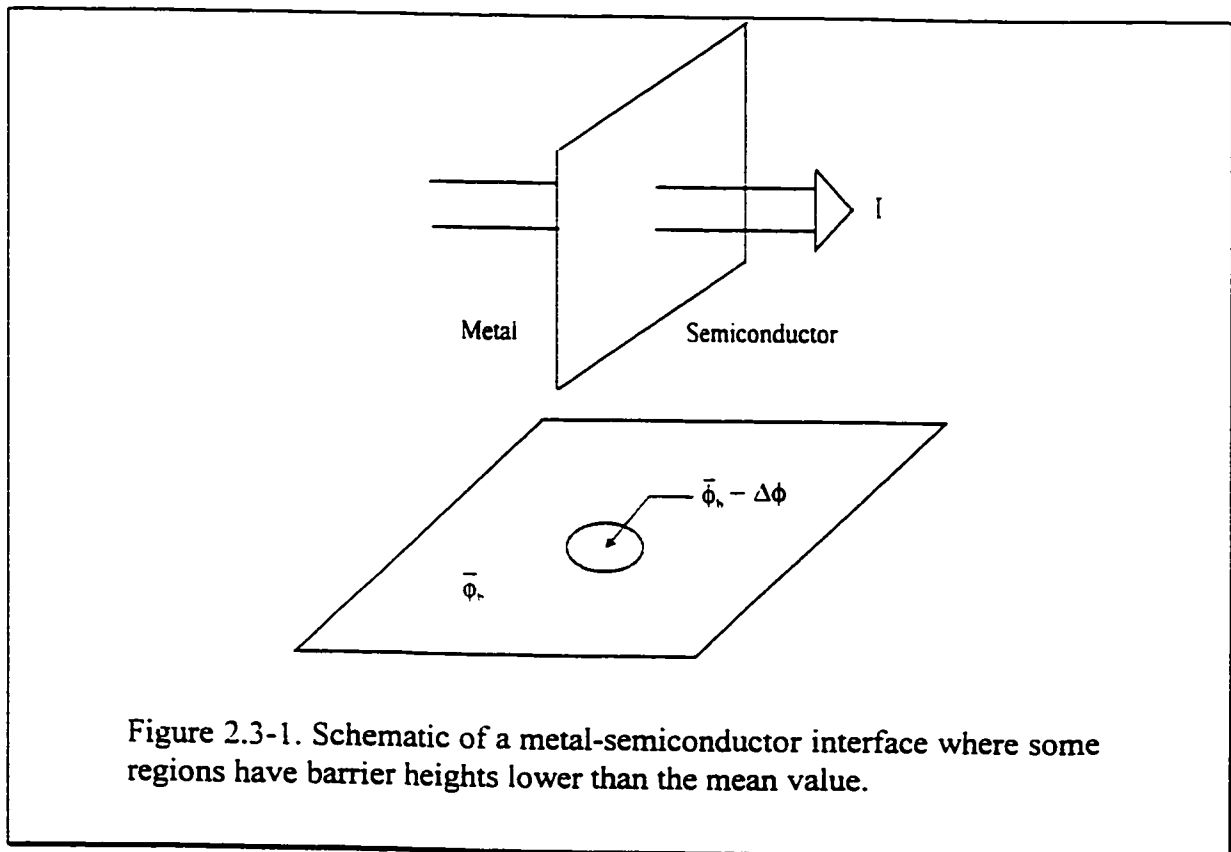


Figure 2.3-1. Schematic of a metal-semiconductor interface where some regions have barrier heights lower than the mean value.

that image-force lowering, effects of tunneling through the Schottky barrier, and recombination current in the depletion region can not account for this departure. To explain this departure, a modified J - V characteristics are developed based on inhomogeneous barriers.

In the following analysis, we adopt the approach first proposed by Werner et al. [1991] and assume that the metal-semiconductor contact is not uniform. In some regions, the Schottky barrier height has a deviation $\Delta\phi$ from the mean barrier height, $\bar{\phi}_b$ (unit in eV), as is shown in Figure 2.3-1. Rather than going into the detailed analysis of the spatial distribution of the built-in potential and barrier height, we will deal with a

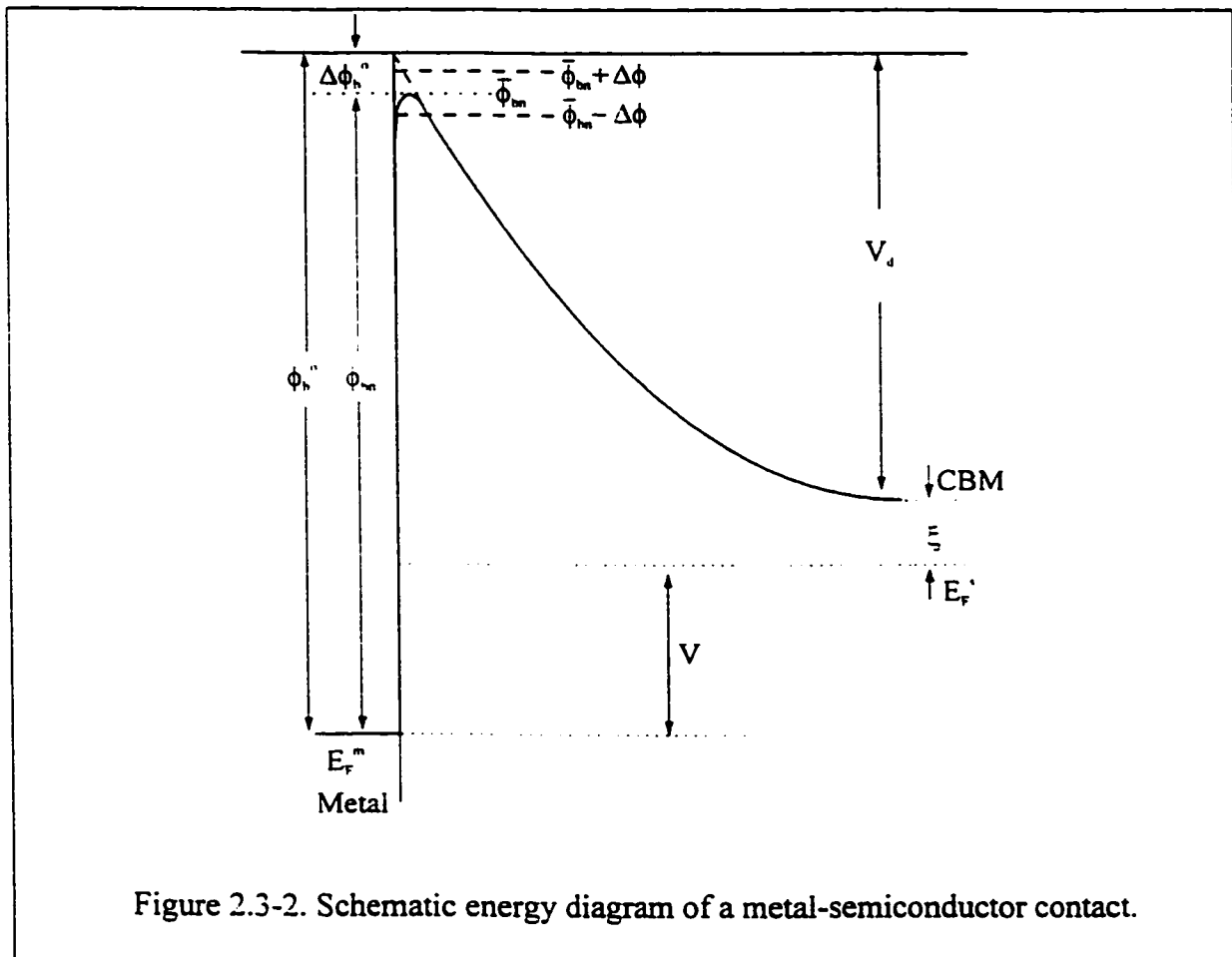


Figure 2.3-2. Schematic energy diagram of a metal-semiconductor contact.

Gaussian distribution of the potential and barrier height over the whole contact where the barrier height has a mean value of $\bar{\phi}_b$ with a standard deviation. σ_s .

For the thermionic emission model, at a given built-in potential V_d , the current density from the semiconductor to the metal is represented as

$$j_{sm}(V_d) = A^* T^2 e^{-q\xi/kT} e^{-qV_d/kT}, \quad (2.3 - 2)$$

and the current density from the metal to the semiconductor is

$$j_{ms} = A^* T^2 e^{-q\phi_b/kT}, \quad (2.3 - 3)$$

where the barrier height, ϕ_b , is related to the built-in potential, V_d , through $\phi_b = V_d + \xi + V$. Considering the Gaussian potential distribution, the total current density from the semiconductor to the metal is given by the integration over the entire possible range of the V_d values [Werner, 1991]:

$$J_{sm} = A^* T^2 e^{-q\xi/kT} e^{-q(\bar{V}_d - \frac{\sigma_s^2}{2kT/q})/kT} \quad (2.3 - 4)$$

By introducing an effective potential, V_d^j , to eq.(2.3-4), the current density can be represented as

$$J_{sm} = A^* T^2 e^{-q\xi/kT} e^{-qV_d^j/kT}, \quad (2.3 - 5)$$

with

$$V_d^j = \bar{V}_d - \frac{\sigma_s^2}{2kT/q}. \quad (2.3 - 6)$$

Similarly, one can get

$$j_{ms} = A^* T^2 e^{-q\phi_b^j / kT}, \quad (2.3 - 7)$$

and

$$\phi_b^j = \bar{\phi}_b - \frac{\sigma_s^2}{2kT/q}, \quad (2.3 - 8)$$

The superscript j in the above equations indicates that the corresponding parameters are governing the $J - V$ characteristics in the inhomogeneous metal-semiconductor contact.

The current density due to thermionic emission including the potential distribution is given by

$$j = A^* T^2 e^{-q\phi_b(V,T) / kT} (e^{qV / kT} - 1), \quad (2.3 - 9)$$

where

$$\phi_b(V,T) = \bar{\phi}_b(V,T) - \frac{\sigma_s^2(V,T)}{2kT/q}. \quad (2.3 - 10)$$

In summary, by considering the barrier inhomogeneities, the $J-V$ characteristics of the Schottky contact were represented by Werner et al [1991] as

$$J = A^* T^2 e^{-\frac{q\bar{\phi}_b(0,0)}{nkT}} \frac{qV}{(e^{nkT} - 1)}, \quad (2.3 - 11)$$

where $\bar{\phi}_b(0,0)$ is a virtual barrier energy corresponding to the barrier height measured at zero-bias and at zero-temperature.

Since eq. (2.3-11) contains contributions from two fundamentally different current sources, we feel that the *a priori* assumption of a single ideality factor, n , may not be justified. Therefore, in our analysis, we will use a more general form, containing two ideality factors, n_1 , and n_2 :

$$J = A^* T^2 e^{-\frac{q\bar{\phi}_b(0.0)}{n_1 kT}} \left(e^{\frac{qV}{n_2 kT}} - 1 \right). \quad (2.3 - 12)$$

Our experimental data will be analyzed according to eq.(2.3-12). We will show in the next chapter how to obtain the parameters, n_1 and n_2 , that describe the barrier inhomogeneities. Based on the model discussed above, the barrier height, $\bar{\phi}_b(0.0)$, and the Richardson constant A^* , can be extracted from both forward- and reverse- biased $J - V - T$ measurements, and will be shown to be very consistent.

Chapter 3

SCHOTTKY CONTACTS TO $In_{1-x}Ga_xP$

3.1 INTRODUCTION

Indium phosphide has received much attention on account of its potential applications to microwave field-effect-transistors (FETs), laser diodes, photodiodes, solar cells, and InP-based optoelectronic integrated circuits (OEICs) [Katz, 1992]. InP has a higher peak electron drift-velocity and a higher breakdown electric field than GaAs, which is advantageous for the fabrication of low-noise and high power Schottky gate FETs. However, serious drawbacks of InP are the low Schottky barrier height and difficulties in surface quality control. These result in an increase in the Schottky gate leakage current and a degradation of the device performance.

Schottky barrier heights of InP were reported from 0.36 to 0.56 eV [Robinson, 1985], strongly dependent on the substrate (carrier doping level and substrate crystal orientation), the method used to grow the epitaxial layer, surface cleaning processes, and metallization schemes. Although the carrier transport in undoped or slightly doped n-InP is generally governed by the well established thermionic emission theory, departures from ideal behavior are commonly observed. As discussed in Chapter 2, the ideality factor, n ,

is found to be greater than unity and increases dramatically as the temperature is lowered. The conventional Richardson plot is found to be non-linear, too.

For actual device applications, a barrier height of about 0.4 - 0.5 eV is not high enough. Many methods were proposed to increase the InP Schottky barrier height, such as epitaxial structures of p^+/n -InP [Tyagi, 1993, Schwartz, 1986, Van Der Ziel, 1977, Roy, 1981], interfacial layers [Hattori, 1991], and high band gap materials such as $In_{1-x}Ga_xP$ [Pang, 1995, Kordoš, 1992, Gaonach, 1990]. The purpose of p^+/n -InP is to modify the band bending while interfacial layers are employed to reduce the carrier tunneling through the M-S interface. The choice of $In_{1-x}Ga_xP$ as the barrier enhancement layer is taking advantage of the wider band gap properties of InGaP.

In this Chapter, we are going to discuss our experimental I - V - T data of InP Schottky diodes. The current-voltage characteristics of InP Schottky diodes depart from ideal behavior of ideal thermionic emission. This departure can be well explained by the modified current-voltage relationship -inhomogeneous barrier model- established in Chapter 2. Experimental procedures are described in §3.2. In §3.3, the results of a systematic investigation of Schottky contacts to InP employing various metallization schemes and post-annealing procedures are presented. Discussion of the experimental results of InP and $In_{1-x}Ga_xP$ Schottky diodes are also given in this section.

Note: all energies (ϕ_b , ξ_n , E_c , E_v , E_{Fn} , E_g) are measured in eV, so the magnitude of the potential energy of an electron associated with its electrostatic potential is equal to the potential measured in volts.

3.2 EXPERIMENTAL PROCEDURES

3.2.1 Fabrication of Schottky Diodes

All samples were epitaxially grown by gas-source molecular-beam epitaxy (GSMBE, McMaster University) on n^- -InP ($N_d = 5 - 8 \times 10^{18} \text{ cm}^{-3}$) substrates. After chemical cleaning, an ohmic contact to the whole backside of the n^- -InP substrate was made by e-beam evaporation. The metallization scheme was Au/Ni/Ge with thicknesses of 1200Å, 500Å, and 250Å, respectively. Au alloyed contacts were formed subsequently by annealing at 400°C for 30 seconds. The wafers with ohmic contacts on the back were cleaned again by chemical solutions. The cleaned samples were patterned in different sizes with diameters of 600 μm (A), 400 μm (B), 200 μm (C), and 120 μm (D). The patterned samples were immediately loaded into the e-beam chamber for Schottky contact metallization. Au, Al, Ni, Ti, Pt, and their combinations were used as the contact

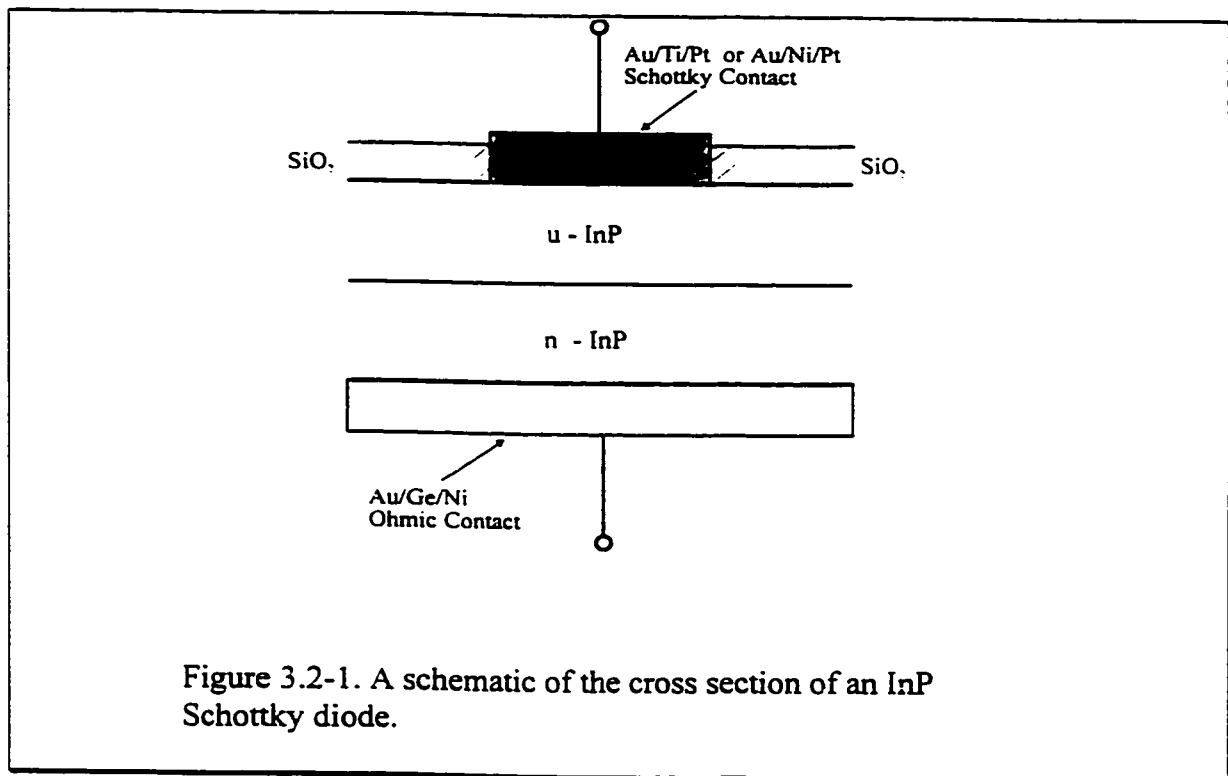


Figure 3.2-1. A schematic of the cross section of an InP Schottky diode.

schemes in my investigations. The fabrication was completed by a standard lift-off process. In some cases, the Schottky diodes were subjected to rapid thermal annealing (RTA) at temperatures from 300 to 500°C, for 20 to 60 seconds. A schematic of an InP Schottky diode (cross section) is shown in Figure 3.2-1.

I. Sample Cleaning

The MBE grown samples were chemically cleaned subsequently by trichlorethylene, acetone and methanol at 90°C for 5 minutes each, repeated once in the above clean solutions for another 5 minutes, then rinsed in flowing de-ionized water for 5 minutes, and finally blown dry by N₂.

In some cases, the sample was exposed to an O₂ plasma for 5 to 10 minutes. The rf power was 150 Watts and the chamber pressure was maintained at 2 mTorr. Then the samples underwent the regular chemical cleaning as described above.

The cleaned samples were dipped into HF:H₂O (1:10) for 10 to 20 seconds to remove the surface oxide.

II. Sample Patterning

1 μm of photoresist (PR 1808, Shipley) was spun on to the cleaned samples at a speed of 5000 RPM for 30 seconds. Then they were “soft-baked” at 120°C for 90 seconds using a hot-plate. Exposure was done with an ultra-violet light source at a wavelength of 365 nm and an intensity of 8.6 mW/cm², for about 4 to 6 seconds. The exposed samples were first dipped into a toluene solution for 5 to 7 minutes and immediately (kept from

water) "hard-baked" at 150°C for 90 seconds. The samples were developed using a solution consisting of Developer #351 (Shipley) and de-ionized water (1:5) at room temperature for 30 to 40 seconds. To ensure good developing, examinations under a microscope were taken frequently.

III. Metallization

The contact metals were deposited by electron beam evaporation (e-beam). The evaporator has two UHV chambers (UHV Instruments Ltd.), one loading chamber (or preparation chamber) and one deposition chamber. The base pressure in both chambers was less than 1×10^{-8} Torr. Usually, the samples were loaded into the preparation chamber immediately after patterning. Subsequently, the samples were transferred to the deposition chamber for metallization. Before metals were being deposited on the patterned samples, the metal targets were degassed for a few minutes to remove the surface oxide. During the target degassing, the samples were shielded by a shutter.

Table 3.2-1. Parameters of Metallization

Metal	Filament Current (A)	Deposition Rate (Å/s)	Time (minutes)	Thickness (Å)
Pt	1.53 - 1.56	2.5 - 3.0	2.5 - 3.2	500 Å
Ni	1.32 - 1.35	2.0 - 2.5	2.2 - 2.5	300 Å
Ti	1.31 - 1.33	2.0 - 2.5	2.1 - 2.5	300 Å
Au	1.38 - 1.41	4.0 - 5.0	5.5 - 6.5	1500 Å
Al	1.50 - 1.53	3.5 - 4.0	5.5 - 6.0	1000 Å
Ge	1.28 - 1.32	2.5 - 3.0	1.5 - 2.0	250 Å
W	1.56 - 1.60	3.0 - 3.5	5.5 - 6.5	1000 Å

Two most frequently used metallization schemes were Au/Ni/Pt and Au/Ti/Pt. First, 450-500Å Pt was deposited, followed by 250 - 300 Å Ni or Ti, then 1500 Å Au. During the deposition of metals, the stage (or sample holder) on which the samples were mounted was rotating to obtain uniform metal-semiconductor contacts. The parameters for Au, Ni, Ti, and Pt deposition are given in Table 3.2-1. When refractory metals or their compounds (mostly nitrides) were used, W, WN and TiN were deposited by rf sputtering [Pang, 1992, 1994], or by ECR-CVD [Boumerzoug, Pang et al. 1994] either on the whole sample surface or on patterned areas. W was also deposited by electron beam evaporation. In this case, a thin Ti layer was evaporated first on the sample to improve the adhesion of W to InP.

IV. Thermal Annealing

Thermal annealing was performed using a rapid thermal annealer (RTA) (AG Associates, Heatpulse 210, or Mini-Pulse). Some MBE grown device structures were annealed at 600°C for 5 seconds before device fabrication, while some Schottky diodes using Au based metallization schemes as electrode metals were annealed at 300°C, 400°C, and 500°C for 10 seconds. For samples with W, WN, TiN, and WTiN as electrode metals, the annealing temperature could be raised to 800°C for 10 to 30 seconds.

3.2.2 Characterization

Temperature dependent electrical characterization of InP Schottky diodes was conducted in a Low Temperature Micro Probe system (LTMP, MMR Technologies, Inc).

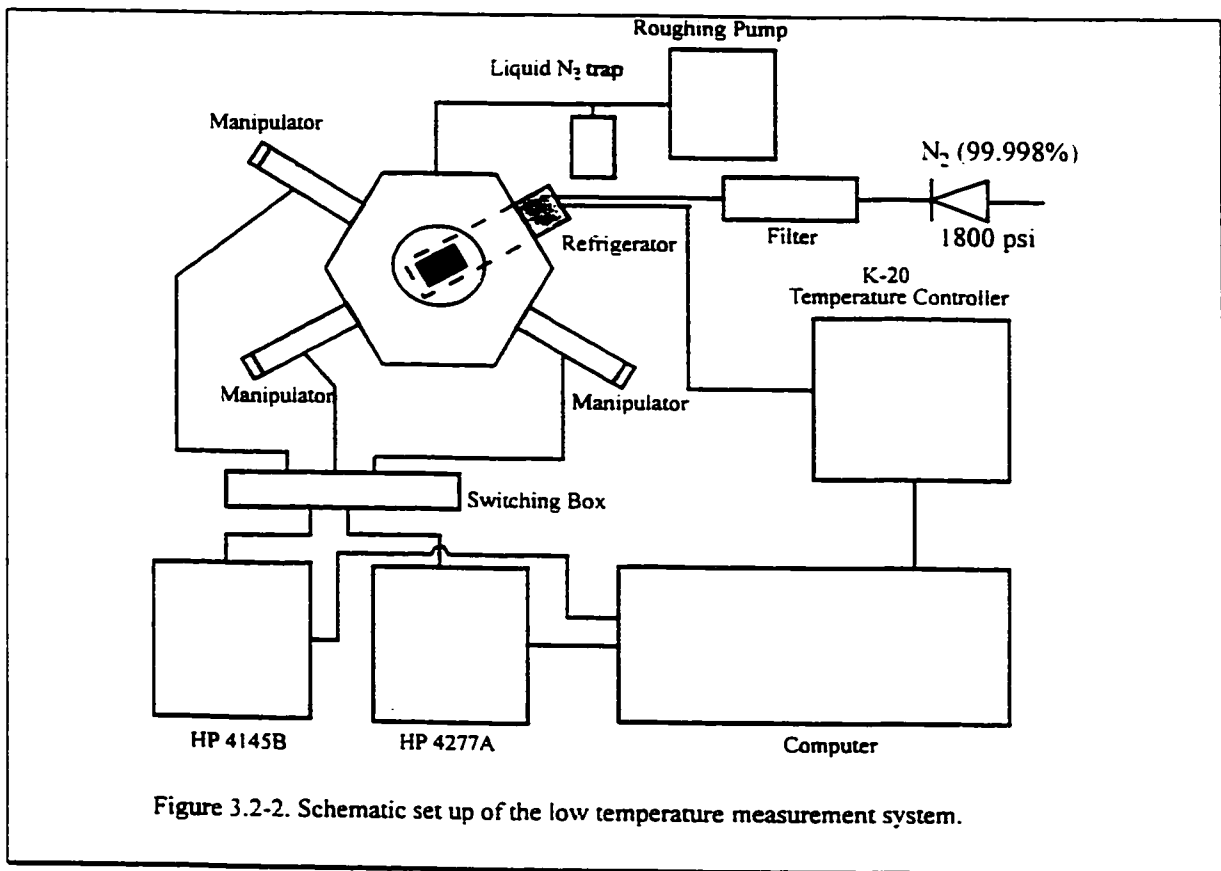


Figure 3.2-2. Schematic set up of the low temperature measurement system.

with an operational temperature range of 80K to 400K. The experimental set up is shown in Figure 3.2-2. The refrigerator utilizes the Joule-Thomson Effect using high pressure (1800 psi) and high purity nitrogen (99.998%) gas flow. The main chambers are equipped with three manually controlled micro-probes which are electrically connected to the measurement instrument (HP 4145B, HP 4277A). The temperature is controlled by a temperature controller (K-20, MMR Technologies, Inc.). Both the temperature control and the electrical (I - V and C - V) measurements are programmed by a computer. The vacuum chamber was pumped down to 1×10^{-4} Torr using a two-stage rotary mechanical pump and a liquid nitrogen trap. The operation is briefly described below:

Open the top window of LTMP system. then the Schottky devices were mounted onto the refrigerator coldstage using thermally and electrically conductive grease or epoxy. Close the window and run 500 psi nitrogen through the system including the refrigerator with the set point temperature at 325K for about 5 minutes to purge the moisture that may have been trapped in the system. Position the probes with assistance of microscope to electrically connect the electrodes of the device under test (DUT). Before turning on high pressure nitrogen, the chamber has to be pumped down to below 1×10^{-4} Torr. At this stage, turn on the high purity (99.998%) high pressure (1800 psi) nitrogen. Before flowing to the refrigerator, the nitrogen flow goes through a filter. The filter is filled with two different adsorbents which absorb the water vapor and hydrocarbons respectively. Replacement of the materials in the filter is necessary to get the temperature down to 80K. When the high pressure nitrogen flows through the system, the refrigerator starts to cool the system down. At normal conditions, it takes about 30 to 40 minutes for the system to reach about 80K from room temperature. The whole temperature range is 80K to 400K which is controlled by the K-20.

The temperature-dependent measurements can be conducted from high temperature to low temperature or from low to high temperatures with proper steps. The temperature can be stabilized at the set point with a minimum tolerance of 0.01K.

When temperature reaches and stabilizes at the set points, the computer program initializes the semiconductor analyzer (HP4145B) to start the current-voltage measurements and store the experimental data.

For voltage-capacitance measurements, a capacitance-conductance meter (LCZ meter, HP4277A) was used. In the capacitance measurements of the Schottky diodes, the frequency was set at 1MHz unless otherwise specified. At this high frequency, the contribution to the capacitance by surface states and/or traps are eliminated because they can only respond at low frequencies.

For more consistent results, data were averaged over those obtained from high-to-low and then from low-to-high voltage scans in both I - V and C - V measurements.

3.3 RESULTS AND DISCUSSION

3.3.1 Metallization Schemes

A variety of metallization schemes for Schottky contacts to InP were investigated [Pang, 1992, 1994, 1995], including Au, Al, Ni, Ti, Pt, W, TiN, and WN. Some results of

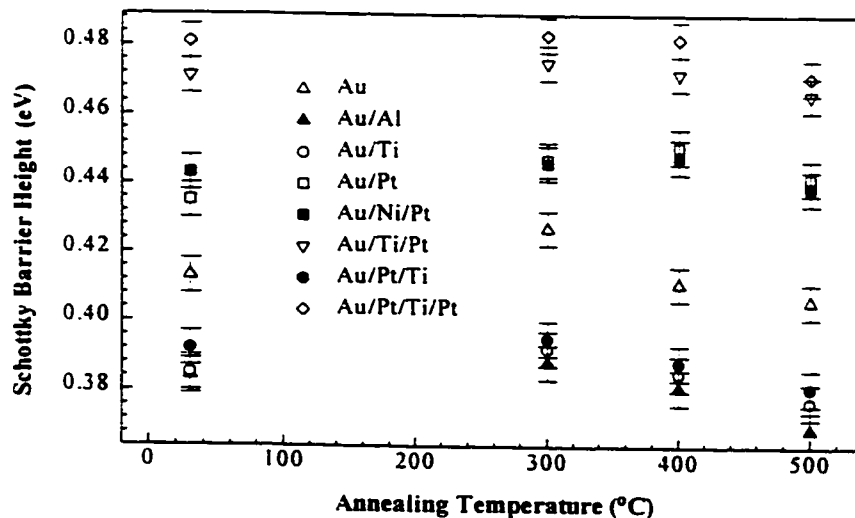


Figure 3.3-1. The Schottky barrier heights of metal(s)-InP contacts annealed at 300°C, 400°C, and 500°C for 20 seconds.

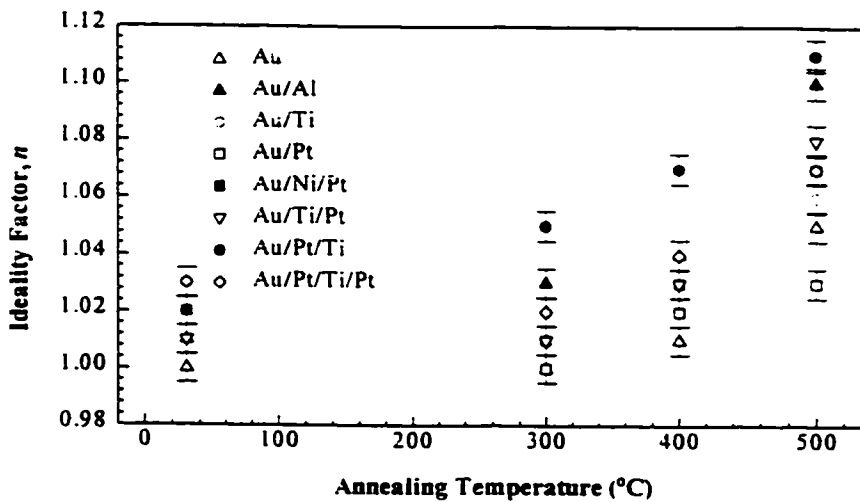


Figure 3.3-2. The ideality factors of metal(s)-InP contacts annealed at 300°C, 400°C, and 500°C for 20 seconds.

the Au-based metallization schemes are given in Figure 3.3-1 and Figure 3.3-2. As shown in Figure 3.3-1, Schottky contacts using Pt as the contact layer have the largest barrier heights. Among them, Au/Ni/Pt produced the best contacts in terms of uniformity and reproducibility.

For the Au-based metallization schemes, annealing at temperatures between 300°C and 400°C for 20 - 30 seconds slightly increases the barrier height (Figure 3.3-1) while the ideality factor does not increase significantly (Figure 3.3-2). Annealing at temperatures higher than 400°C degrades the performance of the InP Schottky diodes, the barrier height is reduced and the ideality factor increases dramatically. The effects are attributed to the diffusion of Au into the semiconductor and the outdiffusion of P from the semiconductor, which was confirmed by Auger electron spectroscopy (AES) depth profiling [Pang 1992].

In contrast to Au-based metallization schemes, Schottky contacts using W, WN and TiN have better thermal stability. They can be subjected to thermal annealing at 600°C - 800°C for 10 - 30 seconds [Pang 1992, 1994]. However, problems remain for InP Schottky devices using W, WN, and TiN as the metallization schemes. It is very difficult to deposit W using an e-beam evaporator because of the high melting point of W. TiN and WN are usually deposited by RF sputtering. Two problems must be considered when using RF sputter deposition: first, uniformity is a concern in case of large substrates being used; second, it is relatively difficult to obtain stoichiometric films which is important because it determines the conductivity of the WN and TiN films.

Another problem associated with sputtering is the potential damage to the InP surface. In InP device applications, this is a big drawback. As will be discussed in Chapter 5, InP MSM photodetectors using TiN and WN have lower dark currents and better thermal stability. However, the photoresponses are much smaller and more bias-dependent.

Deposition of TiN and WN using ECR-CVD was investigated [Boumerzoug, Pang, et al., 1994, 1995]. Compared to RF sputtering, ECR-CVD has lower ion energies, and therefore can reduce the damage to the InP surface. However, stoichiometry control, as in rf sputter deposition, is not easy. Surface contamination may be another drawback for ECR-CVD deposition of TiN and WN on InP. As mentioned in Chapter 2, and will be discussed in Chapters 4 and 5, surface control in InP is very important, especially for InP Schottky devices.

In the following, the metallization scheme used in InP Schottky diodes is Au/Ni/Pt and the diameter of the contact area is 200 μm unless otherwise specified. The residual carrier concentration in the undoped InP (epitaxially grown by MBE on a n^- -InP substrate with $N_d \sim 5 \times 10^{18} \text{ cm}^{-3}$) is about $2 \times 10^{15} \text{ cm}^{-3}$.

3.3.2 Ideality Factor Greater Than Unity

As mentioned in Chapter 2 and will be shown in next section, the ideality factor, n , departs from unit and is much greater than 1 at low temperatures. Before going into detail analysis of our experimental data using the inhomogeneous barrier model discussed in Chapter 2, we first briefly examine the contributions by many factors, which may cause the ideality factor to deviate from unity, such as contact edge leakage currents, image-force lowering, recombination currents in the depletion region, barrier tunneling and interfacial layer effects.

I. Leakage Current from Contact Edge

If the leakage current from contact edge is a major contribution to the excess current and the greater than unity ideality factor, then the dark current will be proportional to the perimeter of the contact [Sze, 1981]. Figure 3.3-3 shows the reverse leakage current of InP Schottky diodes as a function of contact perimeter with temperature as a parameter. As can be seen from the figure, the leakage current density is almost constant as the perimeter increases. This indicates that the edge leakage current is not the major cause of the excess current in our InP Schottky diodes.

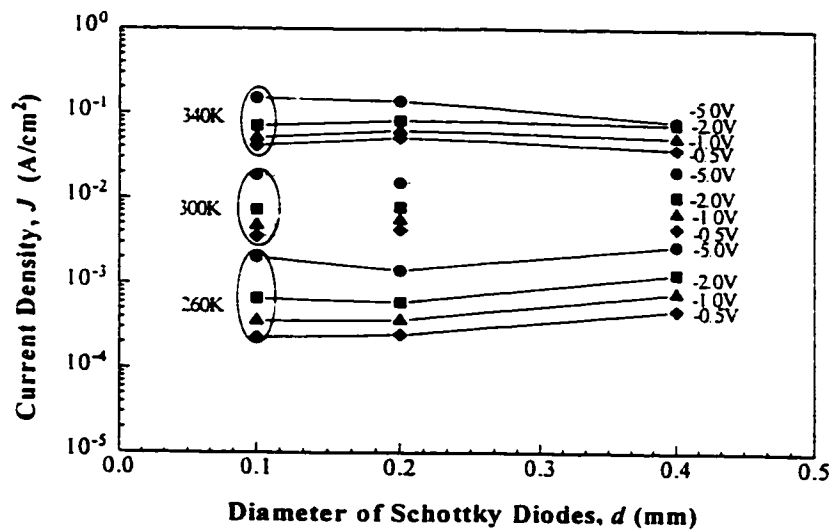


Figure 3.3-3. Dark current of InP Schottky diode as a function of perimeter of the contact with temperature and reverse bias voltage as parameters.

II. Image-Force Lowering

For an ideal Schottky contact, the effective barrier height is lowered by image-force effects. The barrier height and the ideality factor can then be calculated from eq.(2.2-19) and eq.(2.2-20). For InP, taking $\epsilon_s = \epsilon_s' = 12.4$, $N_d = 2 \times 10^{15} \text{ cm}^{-3}$, and $\phi_b = 0.5 \text{ eV}$, the calculated ideality factors and barrier lowerings are shown in Figure 3.3-4. In the temperature range of 90K to 360 K, $\Delta\phi_{bi}$ is about 0.015 - 0.030 eV while n lies between 1.001 - 1.009. Obviously, the image-force lowering itself cannot explain our experimental results.

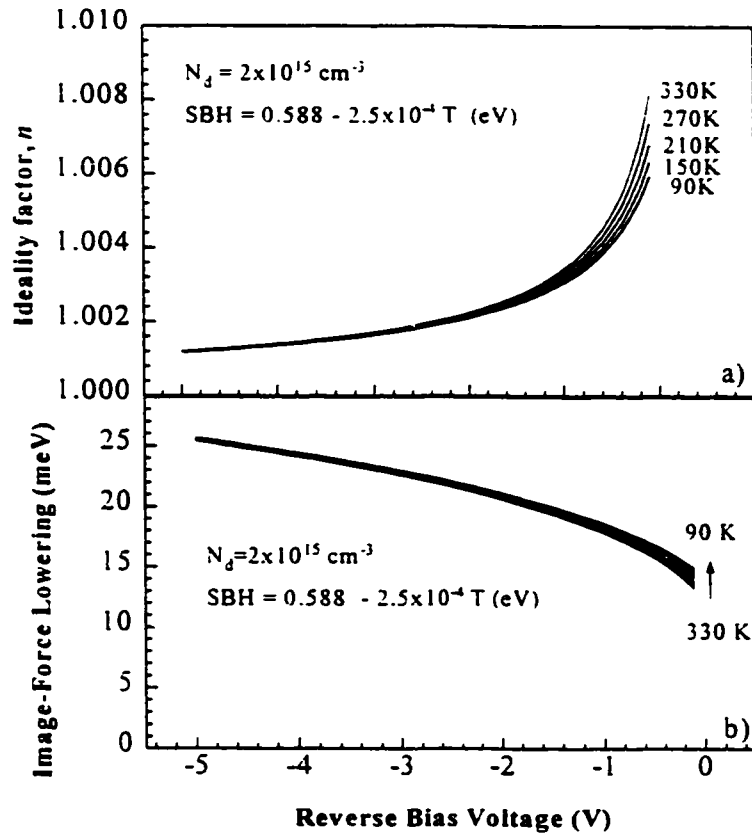


Figure 3.3-4. (a) Ideality factor and (b) barrier height caused by image-force lowering as a function of reverse bias voltage with temperature as a parameter.

III. Tunneling Through the Barrier

In the case of tunneling, the current - voltage relationship and the related characteristic parameters are represented by eq.(2.2-21) to eq.(2.2-25).

For InP, with $N_d = 2 \times 10^{15} \text{ cm}^{-3}$, $E_{00} \sim 8 \times 10^{-4} \text{ eV}$ which is much less than kT in the temperature range of 90 - 360 K. If $\phi_b = 0.5 \text{ eV}$, as is shown in Figure 3.3-5, the equivalent barrier lowering caused by thermionic-field emission for moderately doped

semiconductors. $\Delta\phi$ is about 0.01 - 0.03eV and n lies between 1.02 to 1.08. In general, the effects of tunneling are only significant in highly doped semiconductors and/or at very low temperature.

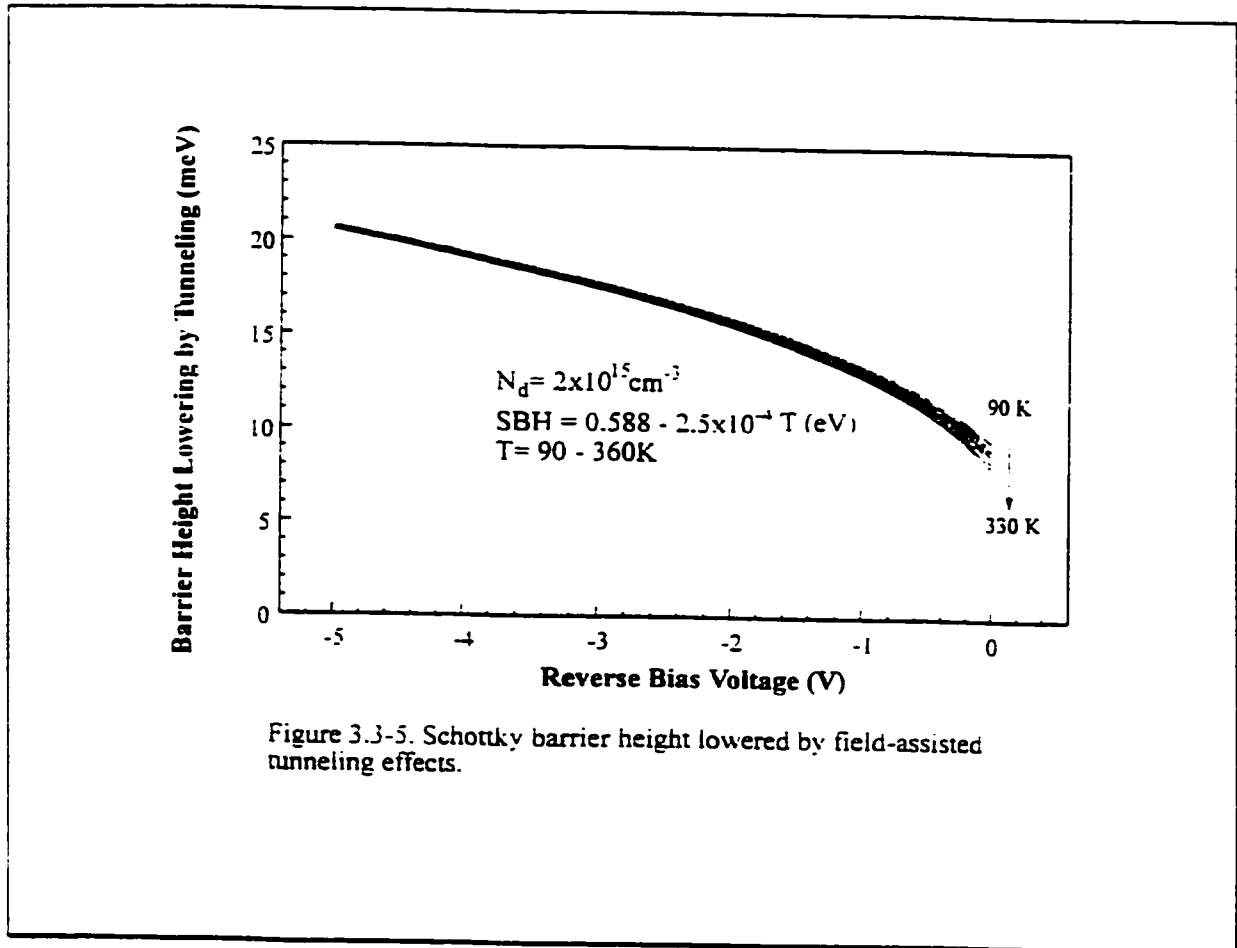


Figure 3.3-5. Schottky barrier height lowered by field-assisted tunneling effects.

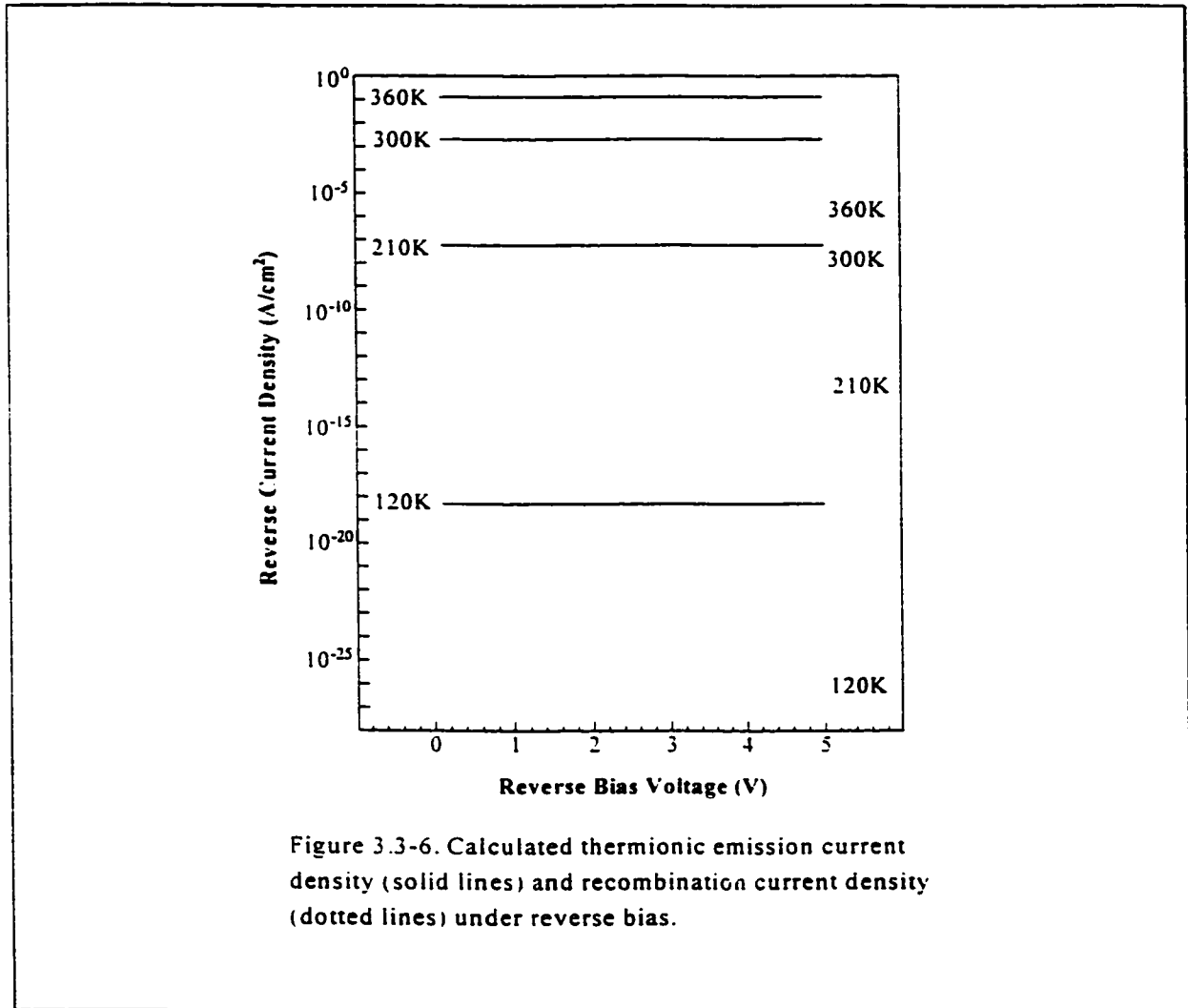
IV. Recombination in the Depletion Region

If we assume that there is only one trap level located in the middle of the band gap (same as the intrinsic level), then the recombination current density can be expressed by eqs.(2.2-28) and (2.2-29).

For InP. with $E_g = 1.35\text{eV}$. $\phi_b \sim 0.5\text{ eV}$. $\tau_r \sim 2 \times 10^{-9}\text{ s}$ [Ashour. 1995], the recombination current and the thermionic emission current are shown in Figure 3.3-6 as a function of reverse bias voltage with temperature as parameter. The recombination current density at room temperature is much smaller than the thermionic current density, and is even smaller at low temperatures. The ratio of recombination current density to thermionic current density is approximately given by

$$J_r / J_{te} = q(N_c N_v)^{1/2} w / (2A^{**} T^2 \tau_r) \exp[-q(E_g + V - 2\phi_b) / 2kT] . \quad (3.3 - 1)$$

The equation shows that the recombination is more important for high barriers, in



materials with short lifetime, at low temperatures, and at reverse bias or small forward bias. For Si with high barriers of about 0.8 eV, the recombination current is significant at low forward and reverse bias [Wittmer, 1990]. For InP, however, the recombination current, compared to the thermionic emission current, is negligible.

V. The Effects of an Interfacial Layer

Let us assume that there is a thin oxide layer between the metal and the semiconductor with a thickness, δ , and an interface state density, D_s ($\text{cm}^{-2}(\text{eV})^{-1}$). The barrier height can be expressed in eV as [Rhoderick, 1988]

$$\phi_b = \phi_{bo} - \Delta\phi_b = \phi_{bo} - \alpha E_{max} \quad (3.3 - 2)$$

where ϕ_{bo} is the barrier height without the interfacial layer, and α is given by

$$\alpha = \frac{\delta \cdot \epsilon_s}{\epsilon_i + q\delta D_s} \quad (3.3 - 3)$$

The equivalent barrier lowering is given by

$$\Delta\phi_b = \alpha E_{max} = \frac{\delta \cdot \epsilon_s}{\epsilon_i + q\delta D_s} E_{max} = \frac{q \cdot N_d \cdot w \cdot \delta}{(\epsilon_i + q\delta D_s)} \quad (3.3 - 4)$$

and the ideality factor caused by the interfacial layer is given by

$$n = 1 + \frac{\delta \cdot \epsilon_s}{w(q\delta D_s + \epsilon_i)} \quad (3.3 - 5)$$

For a SiO_2 interfacial layer of 10\AA , $\epsilon_i = 3.5$, the barrier lowering and ideality factor obtained from eq.(3.3-4) and eq.(3.3-5) are shown in Figures 3.3-7a and b. The effective

barrier lowering caused by the interfacial layer effects is less than 10 meV, and the ideality factor is less than 1.005.

In summary, the departure of the ideality factor from unity at low temperatures can not be completely explained in terms of contact peripheral leakage currents, image-force lowering, field-assisted tunneling through the barrier, recombination in the depletion region, and effects of interfacial layers.

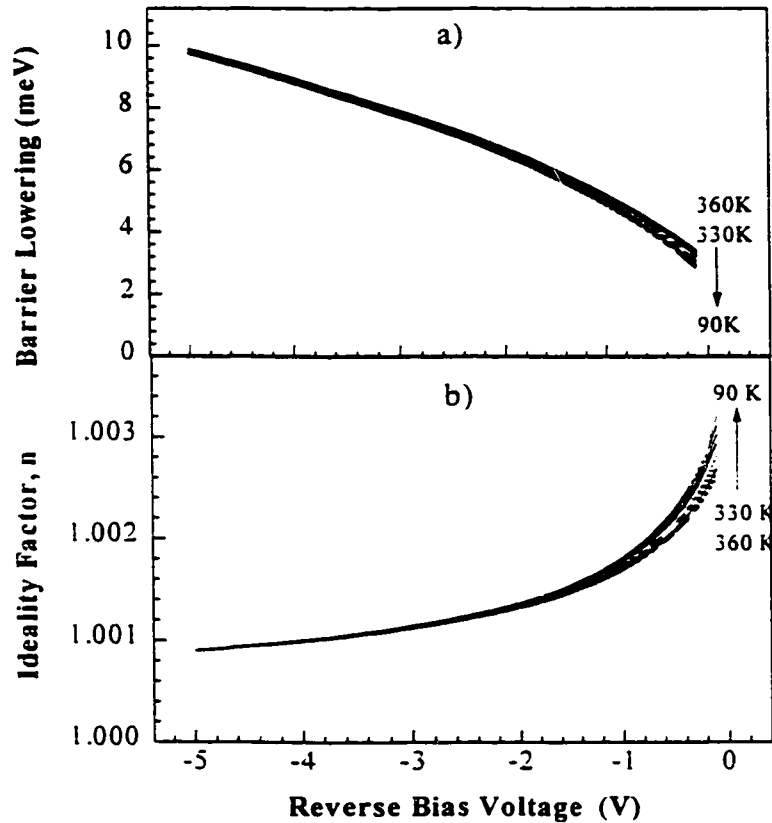


Figure 3.3-7. (a) Schottky barrier height lowered by effects of an interfacial layer (SiO_2 , 10Å) and (b) the related ideality factor, n . The interface state density, D_s , is $2 \times 10^{13} \text{ eV}^{-1} \text{ cm}^{-2}$.

3.3.3 Characteristics of InP Schottky Diodes

Figure 3.3-8 shows the current-voltage (I - V) characteristics of InP Schottky diodes measured at temperatures from 120 K to 330 K. Figure 3.3-9 shows $\ln J$ vs. V (see eq.(2.1-3)) for the same temperature range. According to ideal thermionic emission model, the Schottky barrier height (in eV) can be calculated from eq. (2.1-4) provided the Richardson constant, A^* , is known (for InP, $A^* = 9.2 \text{ Acm}^{-2}\text{K}^{-2}$).

$$\phi_{bn} = (kT/q) \ln(A^* T^2/J_0) \quad (3.3-6)$$

The Schottky barrier height obtained from eq.(3.3-1) at different temperatures is shown in Figure 3.3-10, while the ideality factor obtained from eq.(2.1-3) is shown in Figure 3.3-11. At about room temperature (say, 270 - 330K), the barrier height is relatively constant, and the ideality factor is close to unity. At low temperatures, however, the barrier height decreases significantly while the ideality factor increases dramatically.

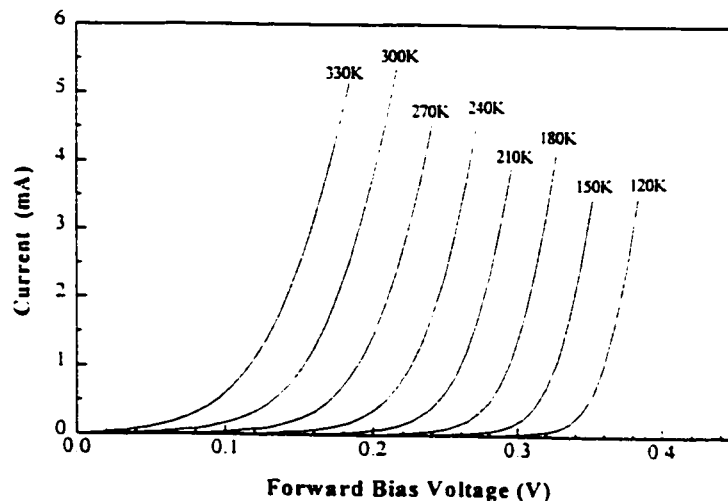


Figure 3.3-8. Forward I-V characteristics of an InP Schottky diode at temperatures from 120 to 330K.

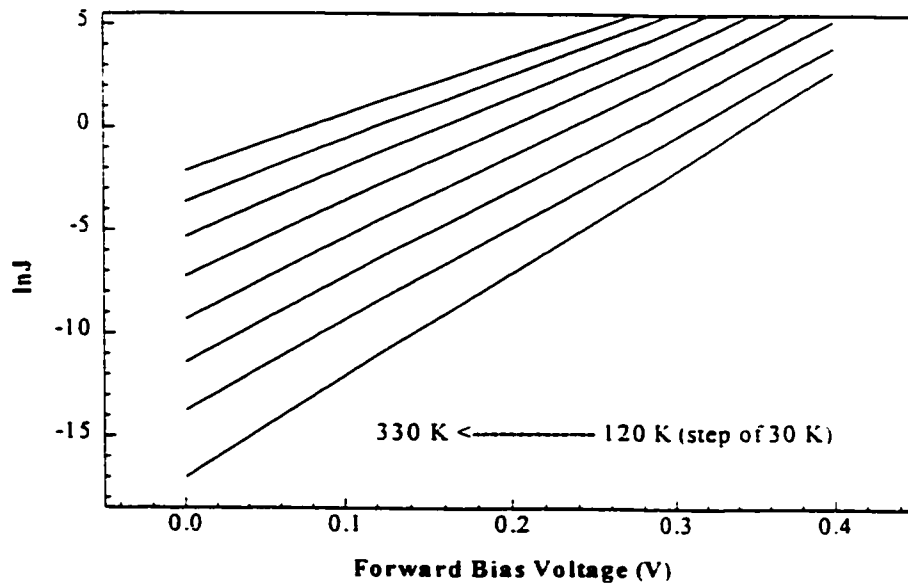


Figure 3.3-9. Semi-log plots of the forward I - V of an InP Schottky diode at temperatures from 120 to 330K.

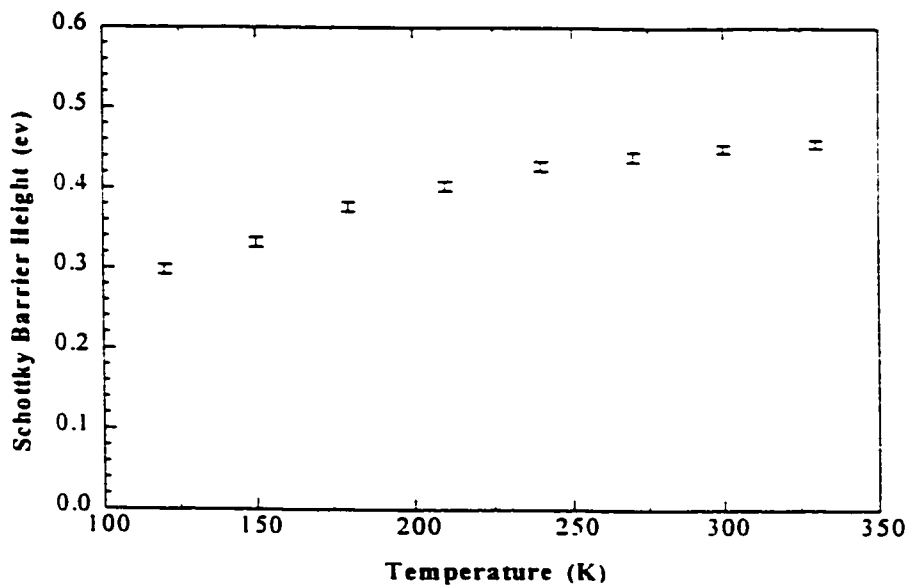


Figure 3.3-10. Schottky barrier height obtained by I-V measurement at temperatures from 120 to 330K.

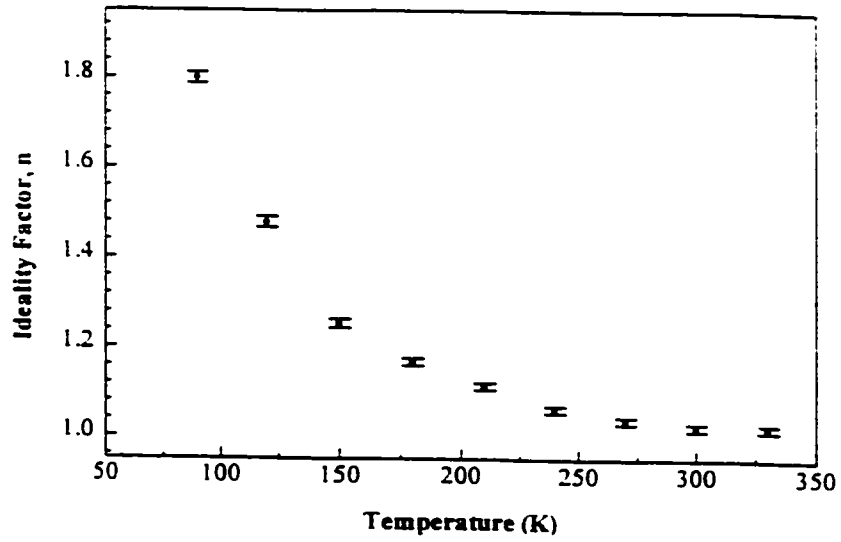


Figure 3.3-11. Measured ideality factor from forward I-V data at temperatures from 120 to 330K.

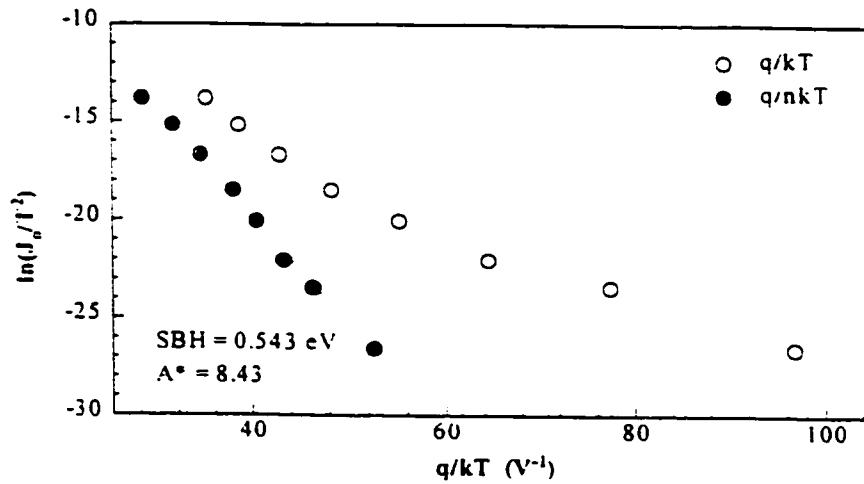


Figure 3.3-12. The Richardson plot (open circles) of Forward IV (FIVT) data of an InP Schotky diode. For an ideal Schotky diode, the plot is expected to be linear. Solid circles show the modified Richardson plot.

In practice, the effective Richardson constant, A^* , is unknown. In this case, the saturation current density, J_0 , is given by eq. (2.1-3) from the temperature-dependent $I - V$ measurements. The Richardson plot of $\ln(J_0/T^2)$ vs. $1/T$, as shown below (Figure 3.3-12)

$$\ln(J_0/T^2) = \ln A^* - q\phi_b/kT. \quad (3.3-7)$$

is used to extract the Schottky barrier height. The plot is expected to be linear for ideal thermionic emission. Therefore, the slope and the intercept of the above plot will result in the barrier height ϕ_b and the Richardson constant A^* . However, as is clear from Figure 3.3-12, the Richardson plot is not linear. Instead, a modified Richardson plot is linear.

$$\ln(J_0/T^2) = \ln A^* - q\phi_b/nkT. \quad (3.3-8)$$

The barrier height and the Richardson constant can then be obtained by fitting experimental data to eq(3.3-8). For reverse bias $I-V-T$ measurements, similar results are

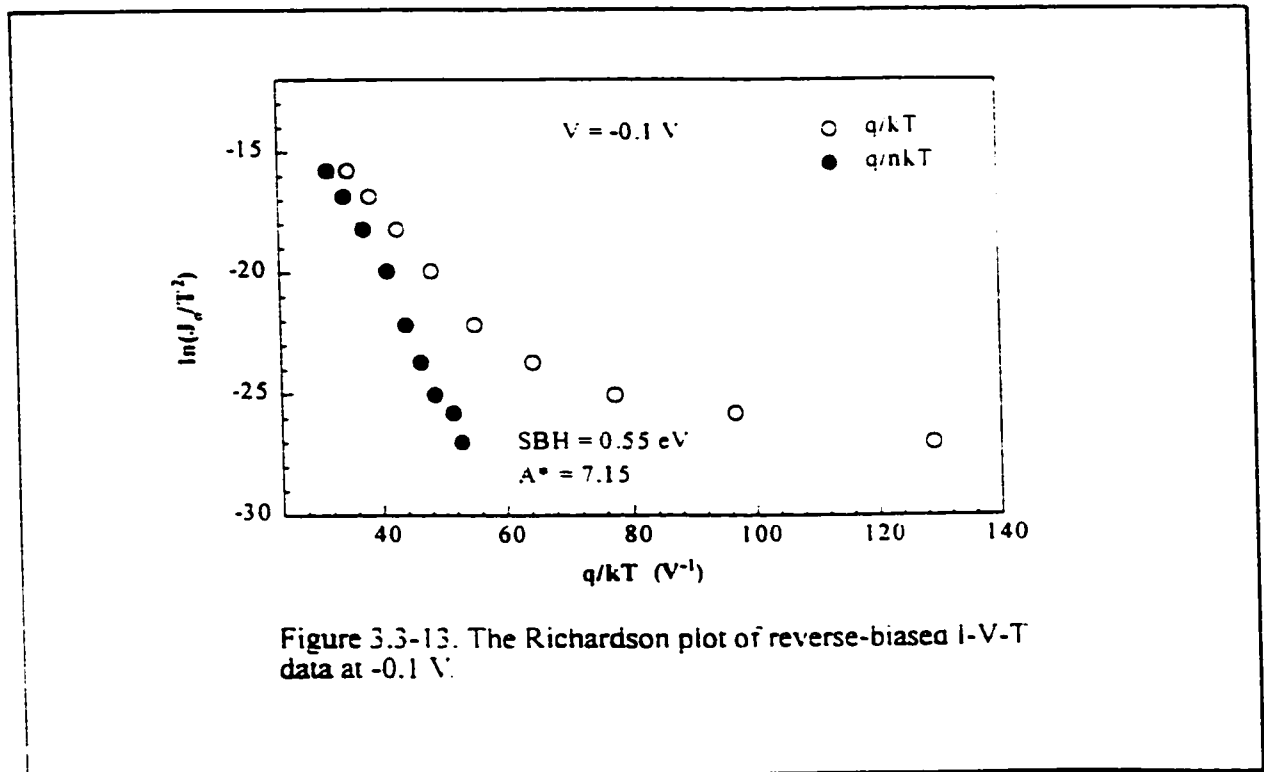


Figure 3.3-13. The Richardson plot of reverse-biased $I-V-T$ data at -0.1 V .

found and are shown in Figure 3.3-13.

According to the depletion approximation [Sze. 1981], the relationship between capacitance and bias voltage is given by

$$\frac{1}{C^2} = \frac{2}{q\epsilon_0\epsilon_{sr}N_d}(\phi_{bo} + V_r - \xi - \frac{kT}{q}) \quad (3.3 - 9)$$

where ϵ_0 is the permittivity in vacuum, ϵ_{sr} is the dielectric constant of the semiconductor (for InP, $\epsilon_{sr} = 12.4$), N_d is the carrier concentration in the semiconductor, ϕ_{bo} is the zero-bias barrier height in eV , and ξ is the energy (in eV) difference between the conduction band minimum and the quasi-Fermi level in the semiconductor.

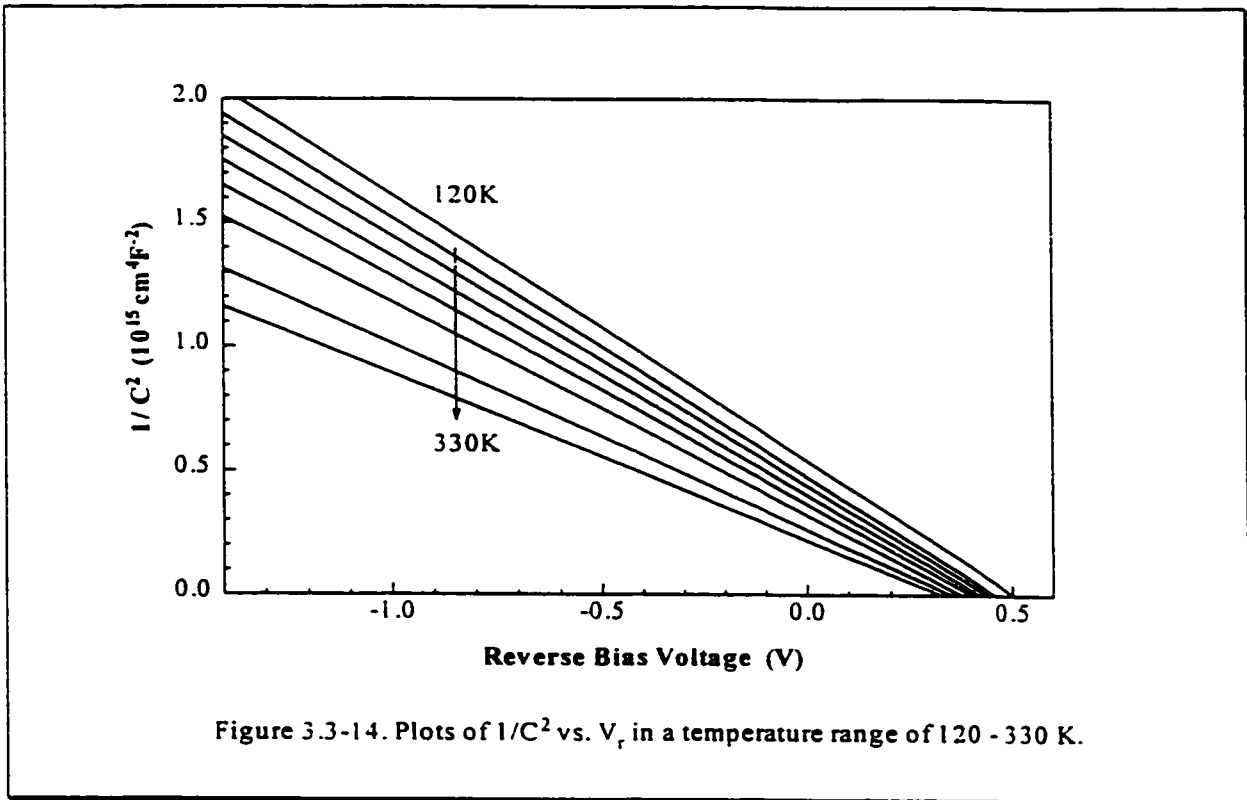
$$\xi = \frac{kT}{q} \ln\left(\frac{N_c}{N_d}\right) \quad (3.3 - 10)$$

where N_c is the density of states in the semiconductor conduction band and is given by

$$N_c = 2\left(\frac{2\pi m^* kT}{h^2}\right)^{3/2} \quad (3.3 - 11)$$

where m^* is the effective mass of electrons, k the Boltzmann constant, T the temperature in Kelvin, and h the Planck's constant.

Figure 3.3-14 shows plots of $1/C^2$ vs. reverse bias voltage, V_r , at temperatures from 80K to 360 K with steps of 20K, where C is the capacitance per unit area of the Schottky diode. The intercept of $1/C^2$ with the horizontal axis of V_r will give the flat-band voltage V_f , which is



$$V_I = (\phi_b^0 - \xi - kT/q) \quad (3.3 - 12)$$

So, the zero-bias Schottky barrier height, ϕ_b^0 , in eV obtained by the $C-V$ measurement is represented as

$$\phi_b^0 = \phi_b^{C-V}(0, T) = V_I + \xi + kT/q \quad (3.3 - 13)$$

where $\phi_b^{C-V}(0, T)$ indicates that the zero-bias barrier height is obtained from $C-V$ measurement at temperature of T . The barrier heights obtained from $C-V$ measurements at various temperatures are shown in Figure 3.3-15, and are found to be slightly temperature-dependent.

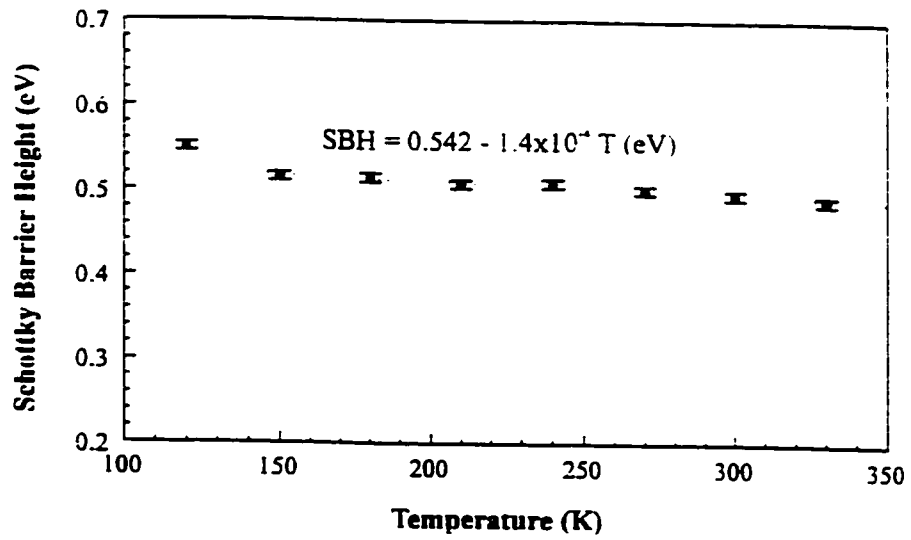


Figure 3.3-15. Schottky barrier height obtained from C-V measurement decreases slightly as temperature increases.

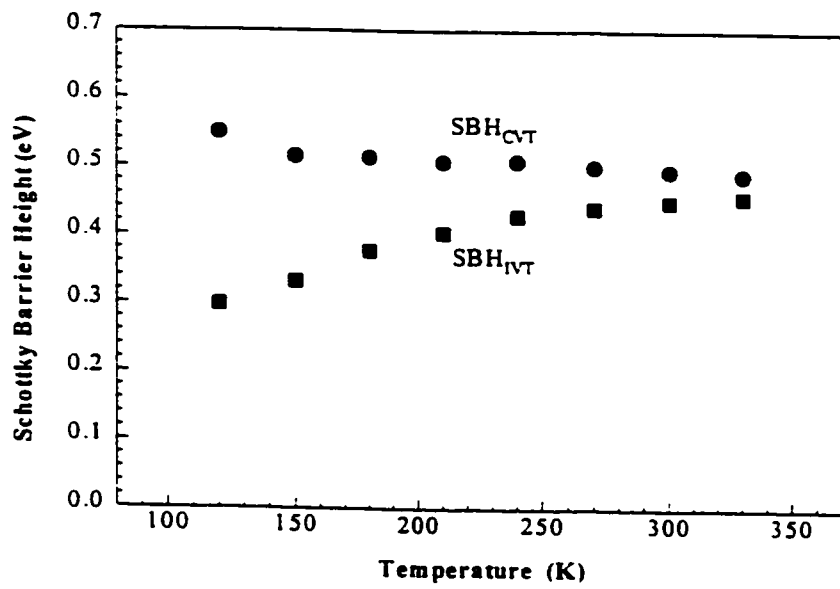


Figure 3.3-16. Schottky barrier heights obtained from C-I-T and I-I-T data as functions of temperature.

The Schottky barrier heights obtained from capacitance-voltage ($C-V$) measurements (SBH_{CVT}) at different temperatures together with those obtained from temperature-dependent current-voltage ($I-V-T$) measurements (SBH_{IVT}) are shown in Figure 3.3-16. The barrier height from $C-V-T$ decreases as the temperature increases while the barrier height from $I-V-T$ increases as temperature increases. As mentioned previously, because the ideality factor departs from unity at low temperatures, the barrier height obtained by $I-V-T$ must be corrected by the ideality factor at low temperatures as shown in eq.(3.3-8).

Two questions arise here. First, why does the ideality factor increase dramatically at low temperatures? Second, based on eq.(2.1-1) and eq.(2.1-2), a Richardson plot of eq.(3.3-7) instead of eq.(3.3-8) is expected. Reasons must be given when using eq.(3.3-8) to extract the barrier height and the effective Richardson constant.

In most semiconductors, the ideality factor of Schottky diode is found to be greater than unity and is temperature-dependent. At very low temperatures, the departure from unity is most significant. The barrier height is also to be found both temperature and bias dependent. This is called the barrier anomaly. Some people simply used a modified current-voltage relationship to fit their experimental data without any explanation.

$$J = A^* T^2 \exp(-\phi_b/nkT) \{ \exp[-qV/nkT] - 1 \} \quad (3.3-14)$$

$$\text{or} \quad J = A^* T^2 \exp[-\phi_b/k(T+T_0)] \{ \exp[-qV/k(T+T_0)] - 1 \} \quad (3.3-15)$$

where the ideality factor n is represented as

$$n = 1 + T_0/T \quad (3.3-16)$$

This is called the " T_0 Effect". T_0 is independent of temperature and has been reported to have values between 30 to 100 K in various Schottky diodes.

3.3.4 Barrier Inhomogeneities in InP Schottky Barriers

According to eq.(2.3-10), the barrier height measured by an $I-V$ experiment is equal to a certain mean value across the sample with a standard deviation $q\sigma_s^2/2kT$.

$$\phi_b^{I-V} \equiv \phi_b = \bar{\phi}_b - \frac{1}{2kT/q} \sigma_s^2 \quad (3.3 - 17)$$

It is reasonable to take the barrier height obtained by a $C-V$ measurement, ϕ_b^{C-V} , as the mean barrier height, $\bar{\phi}_b$, because the capacitance is basically determined by the depletion width and the $C-V$ measurement is an average effect. So,

$$\bar{\phi}_b(0, T) = \phi_b^{C-V}(0, T) \quad (3.3 - 18)$$

where $(0, T)$ means that the barrier height is obtained from measurements at zero-bias and at temperature of T . Then eq.(3.3-17) becomes

$$\phi_b^{C-V} - \phi_b^{I-V} = \frac{q\sigma_s^2}{2kT} \quad (3.3 - 19)$$

It is obvious from eq.(3.3-19) that the barrier height obtained from an $I-V$ measurement is always less than that obtained by $C-V$ measurements. since, for an inhomogeneous contact, the current mainly flows through the lower barrier regions.

If one expands $\bar{\phi}_b(0, T)$ into a Taylor series and takes only first order into account (linear fit),

$$\bar{\phi}_b(0, T) \equiv \phi_b^{C-V}(0, T) = \bar{\phi}_b(0, 0) + \alpha_\phi T \quad (3.3 - 20)$$

then from Figure 3.3-15, we obtain $\bar{\phi}_b(0.0) = \phi_b^{C-V}(0,0) = 0.542$ eV from the intercept with the Y-axis, which corresponds to the zero-bias barrier height at temperature $T = 0K$. A temperature coefficient of the barrier height, $\alpha_\phi = -1.4 \times 10^{-4}$ eV/K, is obtained from the linear fit to the experimental data.

Now, we analyze the current-voltage data using the inhomogeneous model discussed in Chapter 2. The $I - V$ characteristics of the Schottky diode at temperatures from 80 K to 360 K is shown in Figure 3.3-8. If we use the modified current-voltage developed from our inhomogeneous barrier model in Chapter 2 (eq.(2.3-12)), the $I-V$ characteristics are given by

$$J = J_o e^{-qV/n_2 kT} \quad (3.3 - 21)$$

where the saturation current density is given by

$$J_o = A^* T^2 e^{-q\phi_b^{I-V}(0,T)/kT} \quad (3.3 - 22)$$

From the $I - V$ data, we can extract the saturation current density, J_o , and the ideality factor, n_2 , according to eq.(3.3-21), which can be rewritten as

$$\ln J = \ln J_o - \frac{q}{n_2 kT} V \quad (3.3 - 23)$$

The semi-log plots of eq.(3.3-23) at various temperatures were shown in Figure 3.3-9. The intercept gives $\ln J_o$ while the slope will lead to the extraction of the ideality factor, n_2 . The ideality factors obtained by $I - V$ measurements according to eq.(3.3-23) at various temperatures were shown in Figure 3.3-11.

If we are concerned with the series resistance arising from the semiconductor substrate, a slight correction should be made to extract the ideality factor. In this case, the Schottky contact is considered to be a diode in series with a resistor. So, for the I - V measurement, the voltage drop across the Schottky diode, V_D , is corrected as

$$V_D = V - IR \quad (3.3 - 24)$$

where V is the external applied voltage. The I - V characteristics of the Schottky diode in eq.(3.3-21) becomes

$$J = J_0 e^{-q(V-IR)/n_2 kT} \quad (3.3 - 25)$$

where J_0 remains the same as in eq.(3.3-22). Eq.(3.3-25) can be written as

$$\ln J = \ln J_0 - \frac{q}{n_2 kT} V + \frac{qR}{n_2 kT} I = \ln J_0 - \frac{q}{n_2 kT} V + \frac{qSR}{n_2 kT} J \quad (3.3 - 26)$$

where $I = JS$, and S is the contact area of the Schottky diode.

After some manipulation, eq.(3.3-26) can be represented as

$$V = \frac{n_2 kT}{q} \ln J_0 - \frac{n_2 kT}{q} \ln J + SRJ \quad (3.3 - 27)$$

Differentiating eq.(3.3-27) with respect to $\ln J$ gives

$$\frac{dV}{d(\ln J)} = SRJ - \frac{n_2 kT}{q} \quad (3.3 - 28)$$

So, the resistance, R , and the ideality factor, n_2 , can be extracted from the I - V data measured at a temperature T according to eq.(3.3-28). In our investigations, the substrate used to make a good ohmic contact on the bottom is n^+ -InP with a carrier concentration of $5 \times 10^{18} \text{ cm}^{-3}$. The resistance of the substrate extracted from eq.(3.3-28) is found to be 2

- 4 Ω in temperature range from 180 - 330 K. At temperatures below 180K, the resistance was found to be about 20 - 23 Ω . The increase in resistance is attributed to carrier freeze-out at low temperatures. No changes in the ideality factors and the saturation current densities extracted from I - V - T data after correcting for the substrate series resistance were observed. This is due to the small substrate resistance and small forward bias voltage.

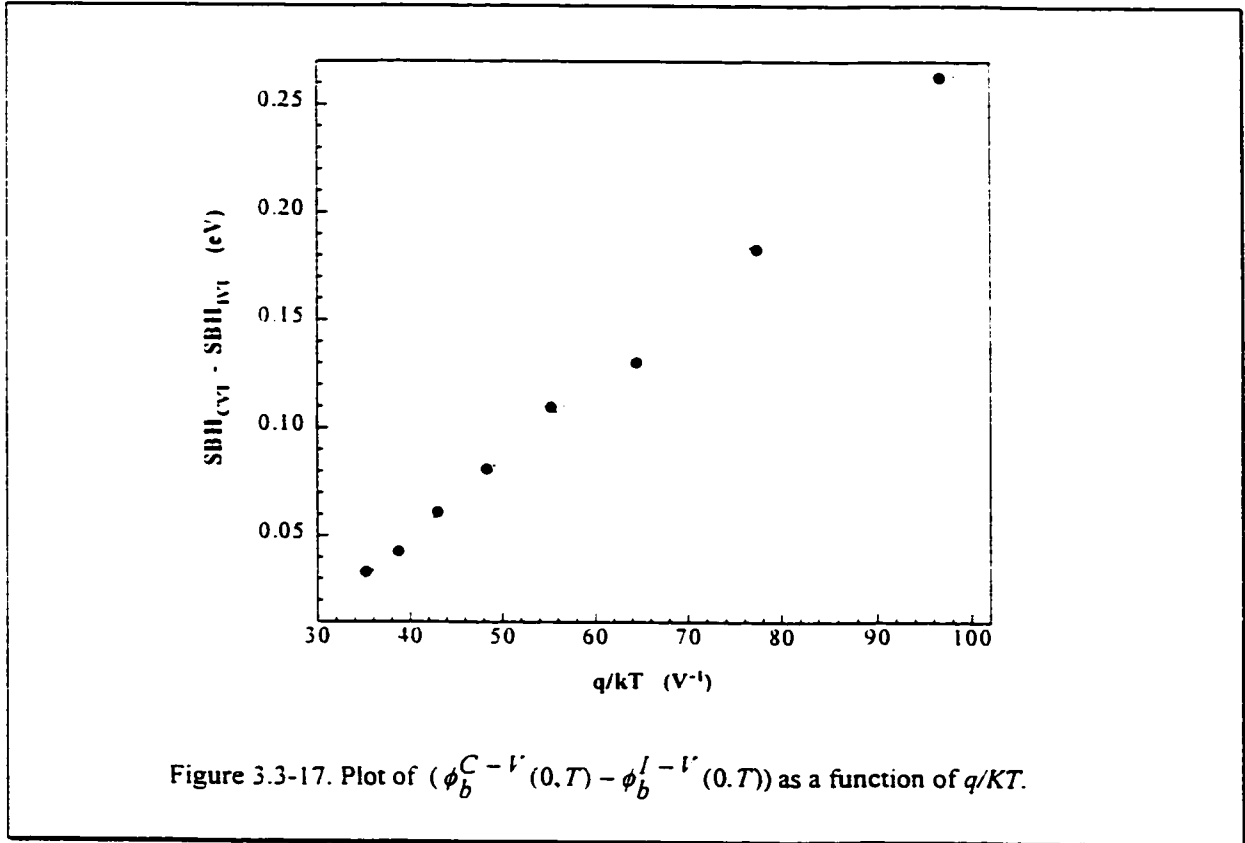
Based on the saturation current density extracted from I - V - T plots, one can calculate the zero-bias Schottky barrier height in eV from I - V data according to eq.(3.3-22).

$$\phi_b^{I-V}(0, T) = \frac{kT}{q} \ln\left(\frac{A^* T^2}{J_0}\right) \quad (3.3 - 29)$$

where the theoretical value of the Richardson constant, for InP, $A^* = 9.2 \text{ Acm}^{-2}\text{T}^2$ [Katz, 1994] was used. We will later show that the effective Richardson constant obtained from our experimental data is very close to this value. A 50% change in A^* will produce only a 3 to 10% change in the barrier height calculated by eq.(3.3-29) over the whole temperature range. The barrier height obtained from I - V data by eq.(3.3-29) is shown in Figure 3.3-10.

As was shown in Figure 3.3-16, the barrier heights obtained from I - V - T are not consistent with those from C - V - T . According to eq.(3.3-17) and eq.(2.3-20), the difference between the barrier heights obtained by C - V and I - V at zero-bias is given by

$$\phi_b^{C-V}(0, T) - \phi_b^{I-V}(0, T) = \frac{\sigma_s^2(0, T)}{2kT/q} = \frac{\sigma_s^2(0, 0) + \alpha_\sigma T}{2kT/q} = \frac{q}{kT} \frac{\sigma_s^2(0, 0)}{2} + \frac{q\alpha_\sigma}{2k} \quad (3.3 - 30)$$



This difference in barrier heights as a function of q/kT is shown in Figure 3.3-17. The slope of the linear fit to the data gives $\sigma_s^2(0.0) = 6.72 \times 10^{-3} \text{ (eV)}^2$, while the intercept gives the temperature coefficient, $\alpha_\sigma = -1.25 \times 10^{-5} \text{ (eV)}^2/\text{K}$. This corresponds to the inhomogeneous barrier having a mean zero-bias barrier height of $0.542 \pm 0.005 \text{ eV}$, with standard deviations of 82 meV, and 55 meV at $T=0$ and $T=300 \text{ K}$, respectively.

According to the inhomogeneous barrier model developed previously (eq.(2.3-12)), the $I-V$ characteristics of the Schottky contacts can be expressed as

$$J = A^* T^2 e^{-q\bar{\phi}_b(0.0)/n_1 kT} e^{qV/n_2 kT} \quad (3.3 - 31)$$

and the saturation current density

$$J_o = A^* T^2 e^{-q\bar{\phi}_b(0,0)/n_1 kT} \quad (3.3 - 32)$$

Comparing eq.(3.3-32) and eq.(3.3-22), the ideality factor, n_1 , can be expressed as

$$n_1 = \frac{\bar{\phi}_b(0,0)}{\phi_b^{I-V}(0,T)} \quad (3.3 - 33)$$

n_1 obtained from the above equation at various temperatures is shown in Figure 3.3-18 .

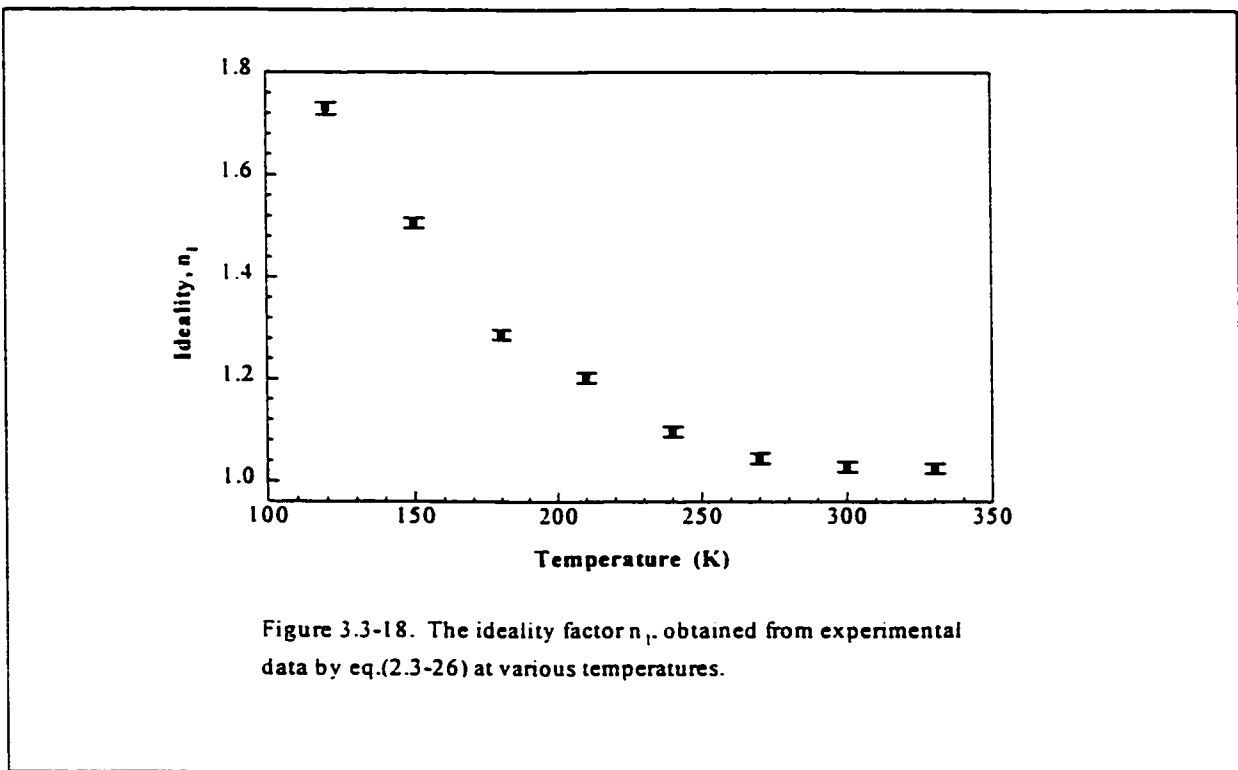
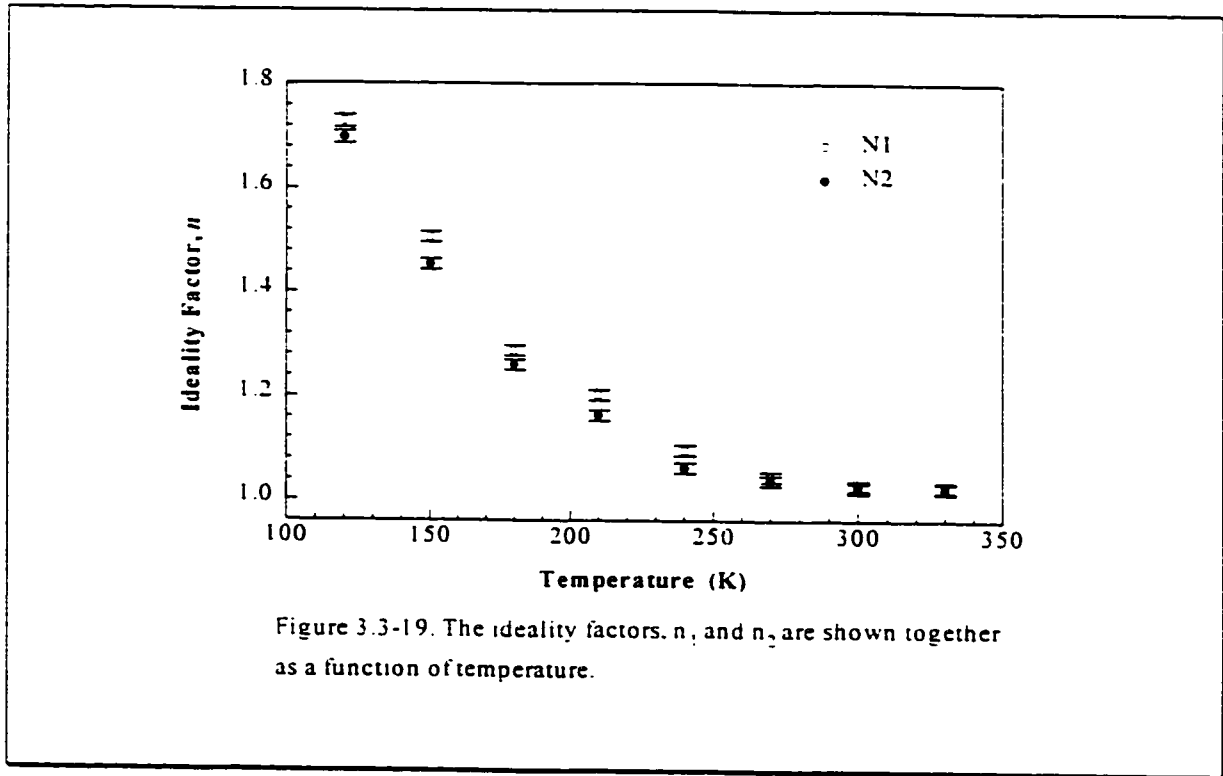


Figure 3.3-19 shows both n_1 and n_2 as a function of temperature and we can see that they are very close in value. However, they are by no means the same. According to the inhomogeneous barrier model, different current sources contribute to n_1 and n_2 as discussed in Chapter 2.



We conducted both forward-bias and reverse-bias $I - V$ measurements using the model we developed. First, for the forward biased $I - V$ measurements, we obtain a modified Richardson plot from eq.(3.3-32),

$$\ln\left(\frac{J}{T^2}\right) = \ln A^* - \frac{q}{n_1 k T} \bar{\phi}_b(0,0) \quad (3.3 - 36)$$

The result is shown in Figure 3.3-20. $\ln(J/T^2)$ vs. q/nkT is quite linear (for both n_1 and n_2). The zero-bias barrier height extracted from this plot is $\bar{\phi}_b(0,0) = 0.543 \pm 0.005$ eV, while the effective Richardson constant $A^* = 8.5 \pm 0.5$ $\text{Acm}^{-2}\text{K}^{-2}$. The effective barrier height, ϕ_b , at room temperature (300 K) is 0.501 ± 0.005 eV.

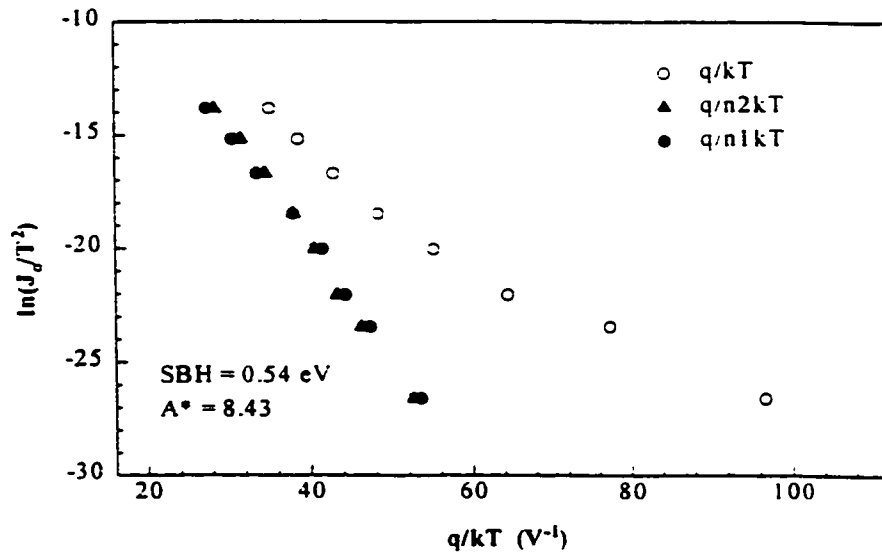


Figure 3.3-20. The Richardson plots of forward I - V - T data of an InP Schottky diode.

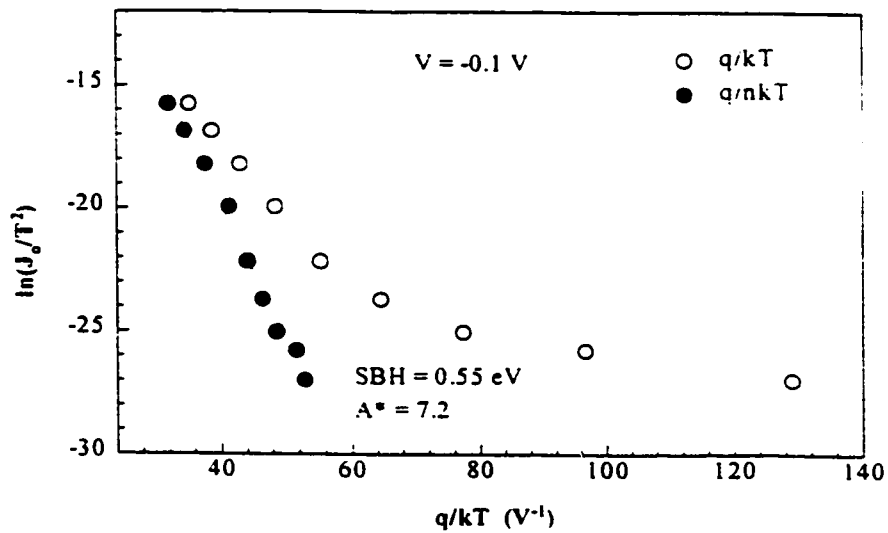


Figure 3.3-21. The Richardson plots of reverse-biased I - V - T data at -0.1 V.

For the reverse-biased I - V - T measurements, we directly measured the saturation current density J_0 , given by eq.(3.3-32), at different biases and different temperatures. A plot for $V = -0.1$ V is shown in Figure 3.3-21. The barrier height extracted from this plot is 0.546 ± 0.005 eV while the effective Richardson constant A^* is 7.2 ± 0.5 $\text{Acm}^{-2}\text{K}^{-2}$.

Based on the inhomogeneous barrier model, experimental data of the InP Schottky contacts are analyzed. The results are summarized in Table 3.3-1. In the table, B and C denote samples with different contact areas: B with a diameter of $400\mu\text{m}$ and C with $200\mu\text{m}$. As shown in Figure 3.3-22, $\phi_b(0,0)$ - the virtual barrier height at zero-bias voltage and zero temperature - is very consistent regardless of measurement type, while the value obtained by C - V measurements is slightly higher. The barrier heights and the ideality factors of samples B and C are almost the same. The temperature coefficient of the barrier height, α_ϕ , is about $-(1.4 - 1.5) \times 10^{-4}$ eV/K. The zero-bias barrier height at room temperature is 0.500 ± 0.005 eV. The bias dependent coefficient of the barrier height, ρ_2 , is about $-(1.9 - 2.1) \times 10^{-3}$ eV/V. Image-force lowering, field-assisted tunneling, and effects of the interfacial oxide layer may contribute to this bias dependence.

As is shown in Figure 3.3-23, the ideality factor increases dramatically as the temperature is lowered. In the range around room temperature (270 -330K), the ideality factor remains relatively constant. At 300K, n is about 1.05 and 1.07 for samples B and C, respectively. As discussed in Chapter 2, image-force lowering, tunneling, recombination and interfacial layers cannot account for this significant departure from unity of the ideality factor. Instead, an inhomogeneous barrier model can explain this behavior very well.

Table 3.3-1. Barrier Heights of InP Schottky Diodes

		B (400μm)	C (200μm)
$\phi_b^{CIT}(0,0)$	$[\pm 0.005 \text{ eV}]$	0.554	0.556
$\phi_b^{FIVT}(0,0)$	$[\pm 0.005 \text{ eV}]$	0.542	0.541
$\phi_b^{RIVT}(0,0)$	$[\pm 0.005 \text{ eV}]$	0.539	0.543
α_b	$[(\pm 0.1) \times 10^{-4} \text{ eV/K}]$	1.4	1.5
$\sigma_s^2(0,0)$	$[(\pm 0.5) \times 10^{-3} (\text{eV})^2]$	7.2	6.7
$\sigma_s(0,300)$	$[\pm 1.0 \text{ meV}]$	68	54
α_σ	$[(\pm 0.05) \times 10^{-5} (\text{eV})^2/\text{K}]$	-0.86	-1.25
ρ_2	$[(\pm 0.05) \times 10^{-3} \text{ eV/V}]$	-1.89	-2.11
ρ_3	$[(\pm 0.05) \times 10^{-3} (\text{eV})^2/\text{V}]$	-4.56	-5.42
A^*	$[(\pm 0.5) \text{ Acm}^{-2}\text{K}^{-2}]$	8.7	7.9
n	$[\pm 0.01]$	1.04	1.07
$\phi_b(0,300)$	$[\pm 0.01 \text{ eV}]$	0.50	0.50

For the Gaussian distribution of the inhomogeneous barrier height, the standard deviation of the barrier height, $\sigma_s(0,300)$, at room temperature is 68 and 55 meV for devices B and C, respectively. The square of the standard deviation, $\sigma_s^2(V,T)$, is both bias- and temperature- dependent. The temperature coefficient is -0.86 and $-1.25 \times 10^{-5} (\text{eV})^2\text{K}^{-1}$, while the bias coefficient is -4.56 and $-5.42 \times 10^{-3} (\text{eV})^2\text{V}^{-1}$, for devices B and C, respectively.

The Richardson constant obtained is 8.7 and 7.9 $\text{Acm}^{-2}\text{K}^{-2}$ for devices B and C, respectively. This value is close to the theoretical value of A^* for InP, which is 9.2

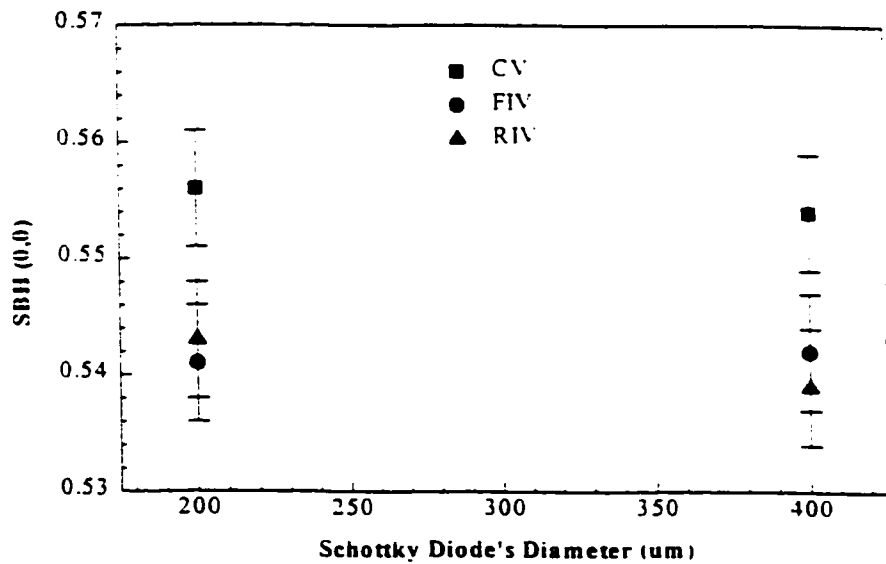


Figure 3.3-22. Schottky barrier heights, SBH(0,0), obtained by temperature dependent C-V, and forward- and reverse-biased I-V measurements.

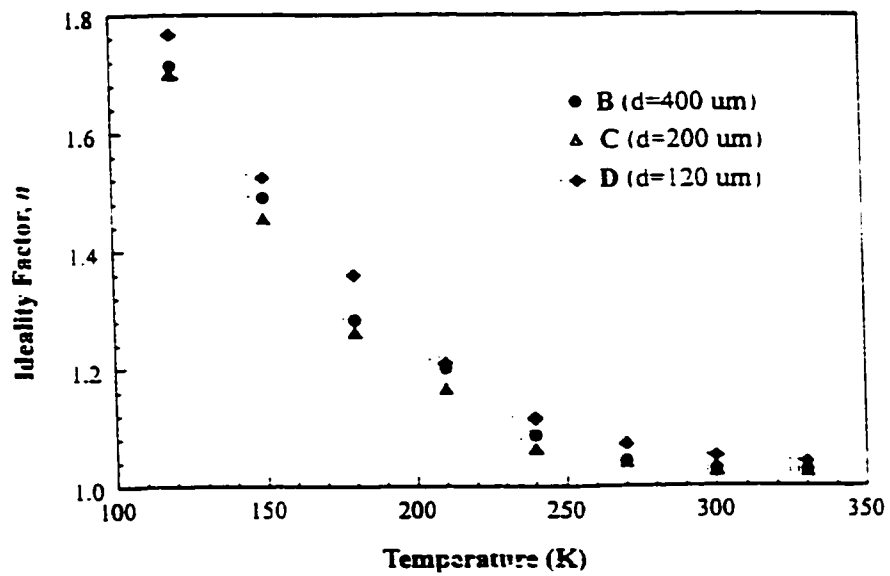


Figure 3.3-23. The ideality factor, n , is shown as a function of temperature for InP Schottky diodes with different contact areas.

$\text{Acm}^{-2}\text{K}^{-2}$ [Katz, 1992]. There is a wide discrepancy among the measured values of A^* for InP [Robinson, 1985], ranging from 10^{-2} to $10^1 \text{ Acm}^{-2}\text{K}^{-2}$. This wide discrepancy is attributed to the linear fitting to the Richardson plot which is generally nonlinear as discussed in Chapter 2.

3.3.5 $\text{In}_{1-x}\text{Ga}_x\text{P}/\text{InP}$ Schottky Diodes

The barrier height of n-InP Schottky diodes usually ranges from 0.38 - 0.50 eV, as discussed above and in previous Chapters. It depends on the InP substrate (growth, doping level), the contact metal(s), and surface states of the semiconductor. In some device applications, it is necessary to raise the barrier height further. As mentioned in Chapter 1, many approaches have been employed to enhance the barrier height. In our investigation, $\text{In}_{1-x}\text{Ga}_x\text{P}$ [Pang, 1995, Loualiche, 1989, 1990, Mesquida, 1995] was used, taking advantage of the wide band gap of GaP. The conduction band discontinuity of the $\text{In}_{1-x}\text{Ga}_x\text{P}/\text{InP}$ heterojunction was assumed to form the barrier to the electron flow, while the intimate contact metal- $\text{In}_{1-x}\text{Ga}_x\text{P}$ was expected to lead to a high Schottky barrier because of the larger band-gap of $\text{In}_{1-x}\text{Ga}_x\text{P}$ (between 2.24 eV ($x = 1$) and 1.35 eV ($x = 0$)).

Similar to InP, barrier anomalies were observed in $\text{In}_{1-x}\text{Ga}_x\text{P}$ Schottky diodes. The ideality factors increase dramatically as the temperature is lowered. The Richardson plot is not linear, but a modified Richardson plot is. A modified current-voltage relationship developed in Chapter 2, based on barrier inhomogeneities was used to extract the barrier

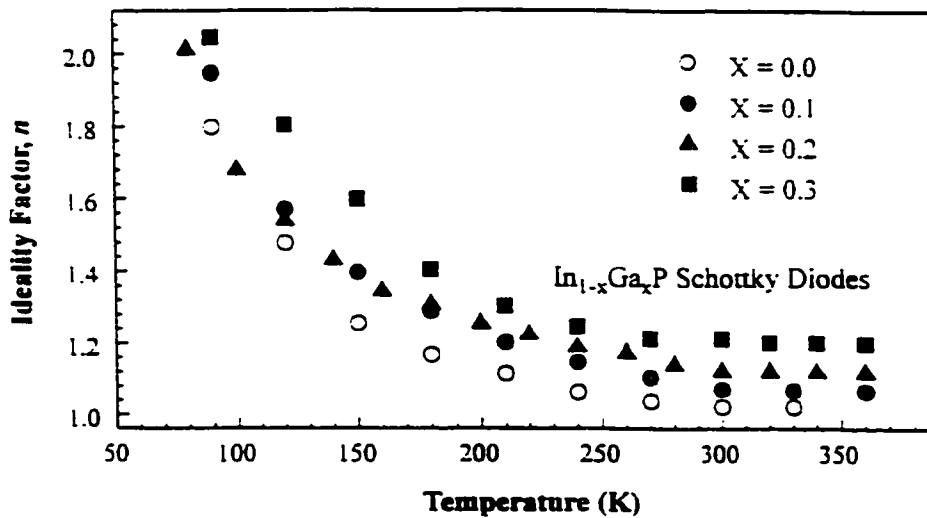


Figure 3.3 - 24. The ideality factors of $\text{In}_{1-x}\text{Ga}_x\text{P}$ Schottky diodes increase dramatically as the temperature is lowered, while at about room temperature they are relatively constant.

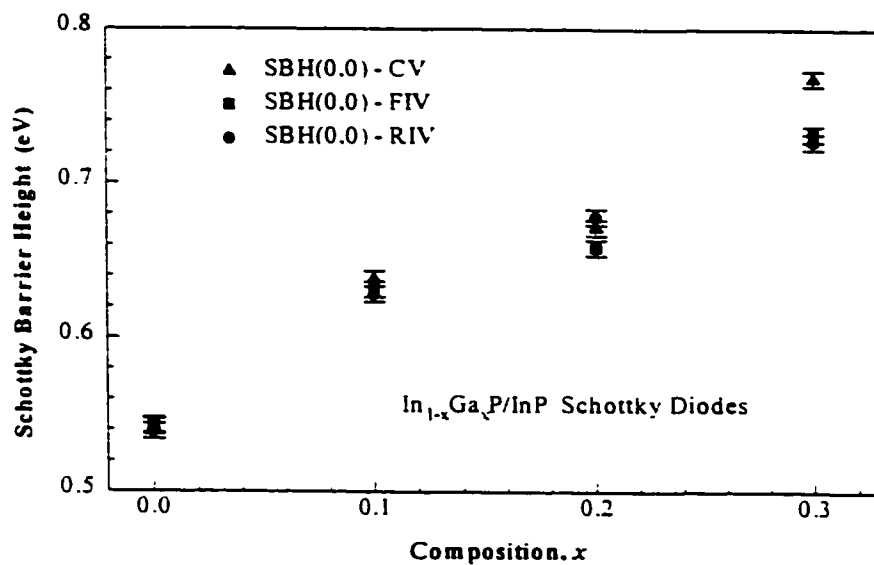


Figure 3.3-25. Barrier heights of $\text{In}_{1-x}\text{Ga}_x\text{P}$ Schottky diodes, SBH(0.0), measured as a function of the compositional factor, x .

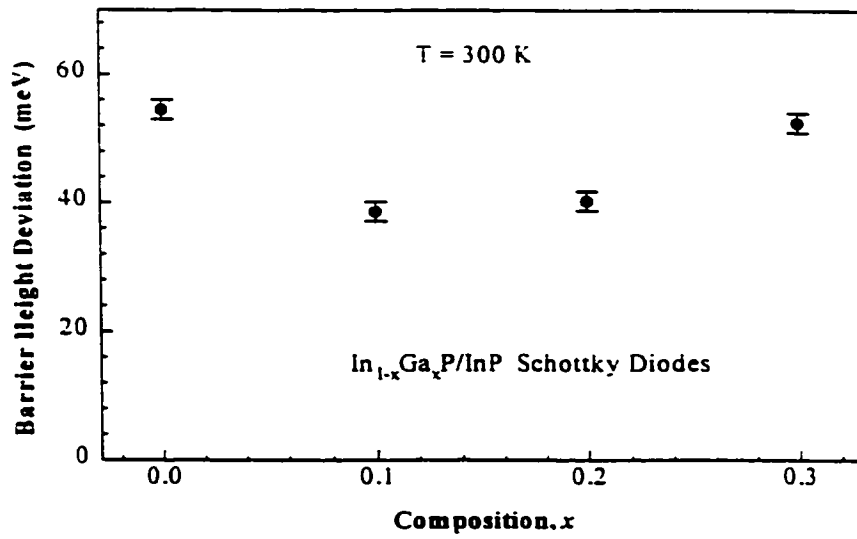


Figure 3.3-26. Measured standard deviation of the barrier height as a function of the compositional factor, x , in $\text{In}_{1-x}\text{Ga}_x\text{P}$ Schottky diodes.

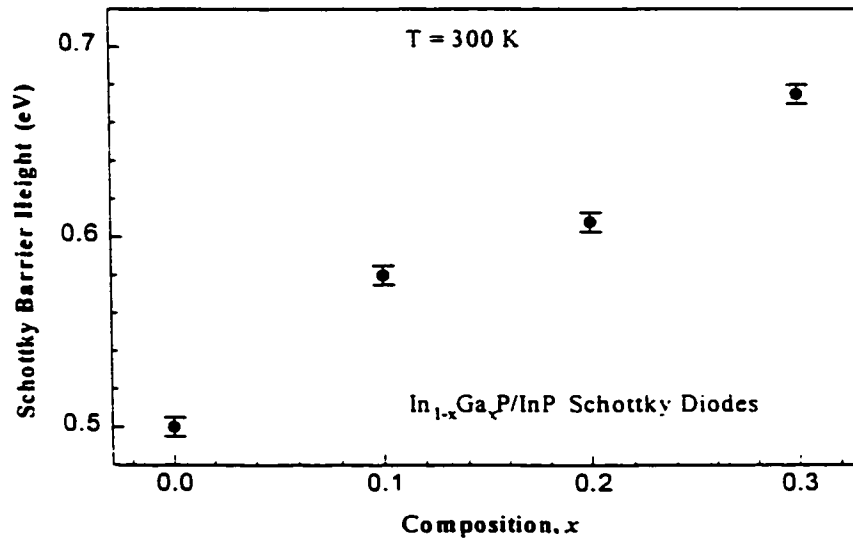


Figure 3.3-27. Zero-bias barrier heights of $\text{In}_{1-x}\text{Ga}_x\text{P}$ Schottky diodes as a function of x , measured at room temperature

heights and ideality factors. Figure 3.3-24 shows the ideality factors of $\text{In}_{1-x}\text{Ga}_x\text{P}$ Schottky diodes varying with temperature. At temperatures around 300K, the ideality factor remains relatively constant. The barrier parameter, $\phi_b(0,0)$, defined as the barrier height at zero-bias and at $T = 0$ K, increases as x increases. This is shown in Figure 3.3-25. The standard deviation of the Schottky barrier height measured at room temperature and extracted from the inhomogeneous barrier model is shown in Figure 3.3-26. Its value is between 40 to 55 meV. This is equivalent to about 10% fluctuation in the barrier height. The zero-bias barrier heights of the $\text{In}_{1-x}\text{Ga}_x\text{P}$ Schottky diodes at room temperature are shown in Figure 3.3-27 as a function of the compositional factor, x . Similar to the virtual barrier height, $\phi_b(0,0)$, $\phi_b(0,300)$, increases with x . This is attributed to the larger band gap in $\text{In}_{1-x}\text{Ga}_x\text{P}$ with a larger Ga concentration, x . The ideality factors of $\text{In}_{1-x}\text{Ga}_x\text{P}$ Schottky diodes at room temperature are shown in Figure 3.3-28. For InP ($x = 0$), the ideality factor is 1.04, close to unity. When x increases, the ideality factors increase to 1.21 at $x = 0.3$. Besides the stress produced by the lattice mismatch between InGaP and InP, other factors such as defects, dislocations, and atomic steps at the heterointerface and/or the surface of InGaP might be responsible for the increase in the ideality factor with x at room temperature [Loulliche, 1989]. As discussed in the previous Chapter, inhomogeneities at the metal-semiconductor interface also make the ideality factor depart from unity. As x increases, the conduction band discontinuity at the InGaP/InP heterojunction increases. This makes the tunneling probability through the barrier increase. This, in turn, makes the ideality factor increase from unity.

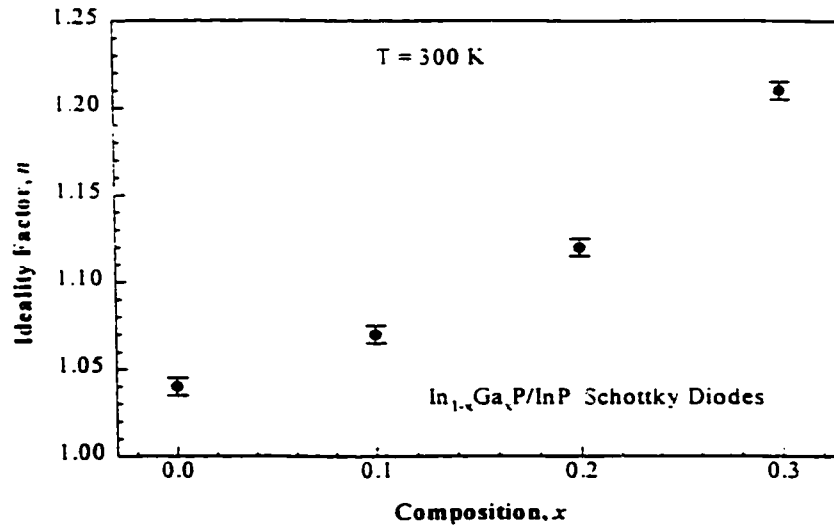


Figure 3.3-28. Ideality Factors, n , of $\text{In}_{1-x}\text{Ga}_x\text{P}$ Schottky diodes as a function of x , measured at room temperature.

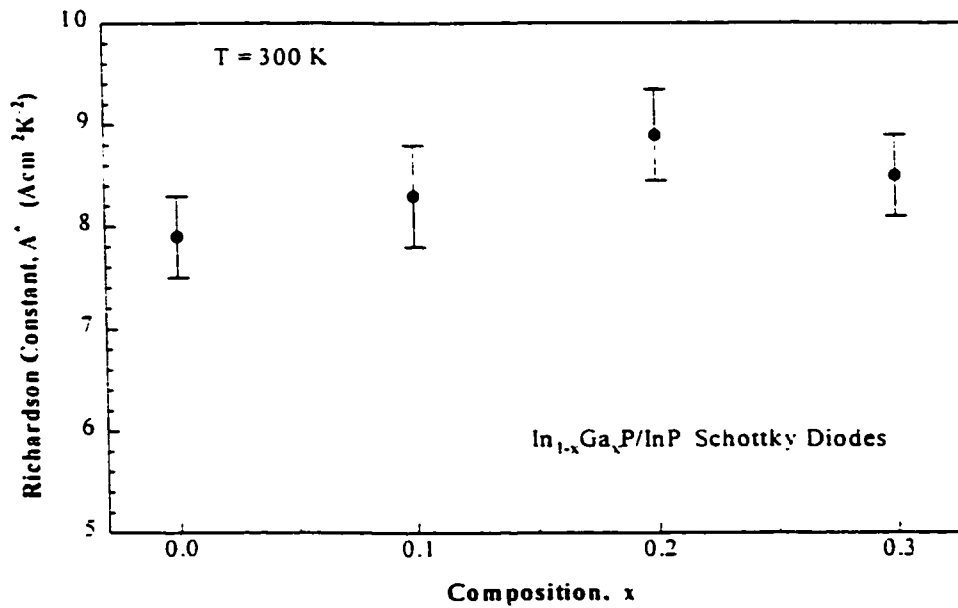


Figure 3.3-29. The Richardson constant, A^* , measured at 300 K, varies with the compositional factor, x , in $\text{In}_{1-x}\text{Ga}_x\text{P}$ Schottky diodes.

Figure 3.3-29 shows the Richardson constant of the $\text{In}_{1-x}\text{Ga}_x\text{P}$ Schottky diodes determined from the modified Richardson plot developed in Chapter 2. The value of A^* ranges from 7.5 to 9.5 $\text{Acm}^{-2}\text{K}^{-2}$ for x in the range of 0 to 0.3. Because the uncertainty is relatively large, it is hard to draw a conclusion from this plot. The theoretical value of A^* for n-InP is 9.2 $\text{Acm}^{-2}\text{K}^{-2}$, which is for ideal thermionic emission. Sze [Sze, 1981] predicted that the effective value of A^* might be reduced by a factor of 2 due to carrier scattering in the depletion region and the quantum mechanical reflection at the barrier. The reported values of A^* for n-InP show a large discrepancy, from 10^2 to 10^1 $\text{Acm}^{-2}\text{K}^{-2}$ [Robinson, 1985]. These discrepancies come from the linear fitting of the non-linear Richardson plot because the current transport departs from ideal thermionic emission. Using the modified I - V relationship developed in Chapter 2, relatively consistent A^* as well as ϕ_b^0 values could be obtained from our modified Richardson plot.

The I - V data of the InP and InGaP/InP Schottky contacts were systematically analyzed using the model discussed in Chapter 2. The results are given in Table 3.3-2. The barrier height has a negative temperature coefficient, α . For InP ($x = 0$), α is about -1.4×10^{-4} eV/K, and ranges from -1.8 to -3.1×10^{-4} eV/K for $x = 0.1$ to 0.3. The temperature-dependence of the barrier height mainly originates from the temperature dependence of the band gap. As discussed in Chapter 2, an inhomogeneous barrier with a Gaussian distribution of barrier heights also results in a temperature dependence of the barrier height. Other sources, such as carrier concentration, and carrier mobility may contribute to this temperature dependency as well.

**Table 3.3-2. Barrier Parameters of In_{1-x}Ga_xP Schottky Diodes
Extracted from the Inhomogeneous Barrier Model**

		x=0	x=0.1	x=0.2	x=0.3
$\phi_b^{CIT}(0,0)$	[[± 0.005 eV]	0.542	0.638	0.671	0.768
$\phi_b^{FIVT}(0,0)$	[[± 0.005 eV]	0.543	0.631	0.658	0.732
$\phi_b^{RIVT}(0,0)$	[[± 0.005 eV]	0.539	0.628	0.645	0.727
α	[$\pm 0.1 \times 10^{-4}$ eV/K]	-1.4	-1.8	-2.1	-3.1
$\sigma_s^2(0,0)$	[$\pm 0.05 \times 10^{-3}$ (eV) ²]	6.72	5.83	5.64	6.56
α_σ	[$\pm 0.05 \times 10^{-5}$ (eV) ² /K]	-1.25	-1.28	-1.34	-1.27
ρ_2	[$\pm 0.05 \times 10^{-3}$ eV/V]	-2.11	-1.60	-1.20	-8.56
ρ_3	[$\pm 0.05 \times 10^{-3}$ (eV) ² /V]	-5.42	-1.88	-6.27	-7.44
$\sigma_s(0.300)$	[± 1.0 meV]	54	38	40	52
N_d	[$\pm 0.5 \times 10^{15}$ cm ⁻³]	14.5	16.1	6.2	39.3
R	[± 0.5 Ω]	3.0	4.3	3.2	5.6
A^{**}	[± 0.5 Acm ⁻² K ⁻²]	7.9	8.3	8.8	8.5
n	[± 0.01]	1.04	1.07	1.12	1.21
$\phi_b(0.300)$	[± 0.01 eV]	0.50	0.58	0.61	0.68

It was also found that the bias coefficient of the barrier height, ρ_2 , is negative. This agrees qualitatively with effects of image lowering [Sze, 1981] and field-dependent effects of the interfacial layers [Rhoderick, 1988]. In contrast to the temperature coefficient, the measured value of the bias coefficient does not have a clear dependence on the compositional factor, x . For $x = 0$ to 0.3, the measured values are -1.2 to -8.6×10^{-3} eV/V, larger than that of image-force lowering which is about -10^{-4} to -10^{-3} eV/V.

Table 3.3-3 shows the results obtained for InGaP/InP ($x = 0.3$) Schottky diodes with different metallization schemes. Except for the ideality factor of the AuNiPt Schottky diode, which is 1.14 at 300 K, and thus much lower than those for AuPt and AuTiPt, all other parameters are very consistent. Once again, this indicates that the model discussed in Chapter 2 is successful.

The reverse leakage current of InGaP/InP Schottky diodes is reduced compared to that of InP Schottky diodes [Pang, 1995]. Table 3.3-4 shows the experimental results. The

**Table 3.3-3. Barrier Parameters of $\text{In}_{1-x}\text{Ga}_x\text{P}/\text{InP}$
($x=0.3$) Schottky Diodes**

	AuPt	AuNiPt	AuTiPt
$\phi_b^{CVT}(0,0)$ [± 0.01 eV]	0.77	0.76	0.76
$\phi_b^{FIVT}(0,0)$ [± 0.01 eV]	0.73	0.75	0.76
$\phi_b^{RIVT}(0,0)$ [± 0.01 eV]	0.73	0.72	0.75
α [$\pm 0.1 \times 10^{-4}$ eV/K]	-3.1	-2.6	-2.8
ρ_2 [$\pm 0.1 \times 10^{-3}$ eV/V]	-8.56	-7.61	-5.05
$\sigma_s^2(0,0)$ [$\pm 0.1 \times 10^{-3}$ (eV) ²]	6.56	6.82	9.12
α_σ [$\pm 0.05 \times 10^{-5}$ (eV) ² /K]	-1.27	-1.84	-2.49
ρ_3 [$\pm 0.05 \times 10^{-3}$ (eV) ² /V]	-7.44	-8.76	-9.84
$\sigma_s(0,300)$ [± 1.0 meV]	52	36	40
R [$\pm 0.5 \Omega$, @300K]	5.6	5.8	6.3
A^{**} [$\pm 0.5 \text{ Acm}^{-2}\text{K}^{-2}$]	8.5	7.8	8.9
n [± 0.01 , @300K]	1.21	1.14	1.22
$\phi_b(0,300)$ [± 0.01 eV]	0.69	0.67	0.68

Table 3.3-4 Barrier Heights, Ideality Factors, Reverse Leakage Currents, and Breakdown Voltages of the $\text{In}_{1-x}\text{Ga}_x\text{P}/\text{InP}$ Schottky Diodes

	$x = 0.0$	$x = 0.1$	$x = 0.2$	$x = 0.3$
ϕ_b° $[\pm 0.01 \text{ eV}]$	0.50	0.58	0.61	0.67
n $[\pm 0.01]$	1.04	1.07	1.12	1.21
I_c $[\pm 0.2\mu\text{A}, -2\text{V}]$	11.4	9.8	2.8	1.7
V_B $[\pm 0.2 \text{ V}]$	12.6	15.1	16.8	17.2

reverse leakage current is reduced from 11.4 μA for $x = 0$ (InP only) to 9.8 μA , 2.8 μA , and 1.7 μA for $x = 0.1$, 0.2 and 0.3, respectively. This is attributed to the increasing barrier height with larger x . The breakdown voltage, V_B , increases from about 12 V for InP ($x = 0.0$) to 15 - 18 V for InGaP/InP with x from 0.1 to 0.3. As will be discussed in Chapter 5, a thin layer of $\text{In}_{1-x}\text{Ga}_x\text{P}$ ($x = 0.1$) was epitaxially grown on top of InP to further increase the barrier height in fabricating InP/InGaAs/InP MSM photodetectors and InP/InGaAs/InP HEMTs. The performance of such devices is improved, having lower dark currents and higher breakdown voltages.

Figure 3.3-30 shows the I-V characteristics of InP/InGaAs/InP/ n^- -InP Schottky diodes with (solid lines) and without (dashed lines) $\text{In}_{1-x}\text{Ga}_x\text{P}$ ($x = 0.1$) barrier enhancement layer on top. This structure is the same as that used in fabricating InGaAs MSMs except for the semi-insulating (S.I.) InP substrate used in the MSM device. The forward I-V characteristics of the devices with and without $\text{In}_{1-x}\text{Ga}_x\text{P}$ layer are the same in the low bias region. At high biases, the I-V curve for the device with an $\text{In}_{1-x}\text{Ga}_x\text{P}$

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Chapter 4

SULFUR PASSIVATION OF InP

4.1 INTRODUCTION

4.1.1 Technical Importance of Surface Passivation

Although InP and related III-V compound semiconductors have promising potential for applications in optoelectronic integrated circuits (OEIC's) and in a variety of microwave and high-speed digital circuits, due to their high-saturation drift velocity, high mobility, and low ionization coefficients, some problems remain to be solved, particularly, the control of the surface properties. The use of passivation to control surface recombination has been shown to be important for heterojunction bipolar transistors (HBTs) [Sandroff, 1987, Nottenburg, 1988], solar cells [Carpenter, 1988a], and high power semiconductor lasers [Kawanishi, 1990].

As we discussed in Chapters 2 and 3 and will discuss in Chapter 5, surface states in InP play a very fundamental role in the Schottky barrier formation and surface recombination velocity (SRV), and limit the performance of devices made from it. Passivation of the InP surface has received much attention in the past ten years because it tremendously improves the semiconductor surface electronic properties.

Sulfur passivation of GaAs was first reported in 1987 [Sandroff et al]. In 1988, similar sulfur treatment was applied to, and was reported to be effective in surface

passivation of InP [Iyer et al, 1988]. Since then, sulfur passivation of InP has attracted much attention because of simple processing and good resulting performance. It was reported that sulfur passivation of InP can result in a reduction of surface Fermi-level pinning [S.D. Kwon, 1995], a reduction of the interface-state density in metal-insulator-semiconductor diodes (MIS) [A. Kapila, 1993], and a decrease of the surface recombination velocity [Yablonovitch 1987, Shikata, 1991]. Many sulfide passivation schemes, such as $(\text{NH}_4)_2\text{S}$ [Tao, 1992], $(\text{NH}_4)_2\text{S}_x$ [Han, 1996, Sugiyama 1995, Kwon 1995, Fukuda, 1994], S_2Cl_2 [Gao, 1995], sulfur containing Br_2/MeOH [Gao, 1995], $\text{Na}_2\text{S}\cdot 9\text{H}_2\text{O}$ [Bessolov, 1995], and $\text{P}_2\text{S}_5/(\text{NH}_4)_2\text{S}$ [Huang, 1993] have been proposed. Among them, $(\text{NH}_4)_2\text{S}_x$ is the most frequently used solution for InP surface passivation.

4.1.2 Theory of Sulfur Passivation

I. Dynamics

Bessolov et al. [Bessolov, 1993, 1995] proposed a model to describe the interaction of the sulfur ion in a solution with the valence electrons of a III-V (InP, GaAs, and GaP) semiconductor in the course of the sulfidizing process. In that model, the starting electronic structure of the semiconductor surface (prior to sulfidizing) and the energy state of the sulfur ion in solution both play an important role in the passivation process. During the interaction process, a change takes place in the electrochemical potential (Fermi level) of the semiconductor, which affects the electron work function at the surface.

The change of the semiconductor work function as a result of sulfidizing is a linear function of the starting work function value and the solution temperature. The amount of the change in the work function value varies in proportion to the negative of the starting electron work function value in the untreated semiconductor and depends on the treatment temperature. If the starting work function value in the semiconductor is equal to the effective electronegativity of the sulfur ion in solution, the work function of the semiconductor will not be changed by sulfidization. The effective electronegativity of the sulfur ion in solution depends on the ionicity of the chemical bonds of the semiconductor being treated.

II. Surface Structure

Tao obtained a highly stable crystalline S-passivated InP (100) surface by sulfur passivation [Tao, 1992]. XPS shows that the surface is terminated with a monolayer of sulfur, which forms bridge bonds only to indium. Sugiyama [Sugiyama 1995] found that $(\text{NH}_4)_2\text{S}$ treated InP (001) surfaces are completely terminated by S-In bonds after annealing at 400°C . P - S bonding was not found after passivation of the InP surface [Huang, 1993]. Treatment of InP (100) in $(\text{NH}_4)_2\text{S}$ and Br_2/MeOH solutions containing trace amount of S_2Cl_2 and $(\text{NH}_4)_2\text{S}$ significantly reduces the surface roughness of the as-received samples. These treated surfaces were also found to be free of oxide [Gao, 1995].

III. Chemical Bonds

Fukuda identified by XPS three different chemical states of sulfur ($\text{S}2_{\text{p}3/2}$ lines at 161.2, 162.0, and 163.4 eV) on the sample treated at room temperature [Fukuda 1994]. They correspond to sulfur in phosphorus sites (in the second layer of the InP (001)

surface), to sulfur bonded to indium on the first layer, and to elemental sulfur on sulfide. respectively. The $S2_{p_{3/2}} = 162.0$ eV peak becomes dominant with long-time exposure to atmosphere at RT. The 163.4 eV peak disappears after annealing the sample at 400°C. while the lines at 162.0 eV and 161.2 eV remain on the surface.

Desorption peaks of S atoms are observed at 460°C for S/InP in thermal desorption spectroscopy (TDS) spectra. Desorption of group V-elements, such as As and P atoms, is hindered by S passivation [Sugiyama 1995].

4.1.3 Applications of Sulfur Passivation

I. Schottky Diodes

The Schottky barrier height of sulfur treated Pt/n-InP Schottky diodes was increased by 0.15 eV while the reverse leakage current was reduced by one order of magnitude. A thin layer of In_2S_3 was formed at the interface which is believed to be responsible for the barrier height enhancement [Huang, 1993].

It was found that the Schottky barrier height is more sensitive to the metal work function after the InP surface was passivated [Kwon, 1995a]. This indicates that the sulfur treatment reduces the surface Fermi-level pinning.

II. MIS Diodes

Landheer found that polysulfide treatment reduced the bulk trap concentrations produced during contact annealing [Landheer, 1994]. The concentration of a bulk trap at 0.33 eV was reduced to below 10^{12} cm^{-3} and that of a 0.45 eV trap to a concentration of $5 \times 10^{13} \text{ cm}^{-3}$. The density of interface states close to the conduction band edge also

decreased with the polysulfide treatment. It is believed that after sulfur passivation of InP there were more stable group-III elements with actually no dangling bonds at the surface and the group-V (phosphorus) elements are buried in the third layer.

III. MSM-PDs

Sulfur passivation was employed in the fabrication of InP/InGaAs MSM photodetectors. It was reported [Han, 1994, Schade, 1994] that the dark current is 10 - 100 times lower, and the capacitance is 30% smaller after sulfur passivation. The improvement of the detector characteristics is understood in terms of Fermi level depinning at the metal-semiconductor interface, and the existence of a thin layer of InP_xS_y between the contact metal and the semiconductor due to the sulfur treatment. It is necessary to anneal the sulfur-treated substrates at 270°C to obtain such improved device characteristics. This is attributed to the formation of thermally stable In-S bonds. The photocurrent was found to be less dependent on bias voltage after passivation. This is attributed to the reduction of internal gain produced by field-dependent effects on InP surface.

In this chapter, passivation of InP surfaces using $(\text{NH}_4)_2\text{S}_x$ is discussed. Experimental details are given in §4.2. Results and a discussion of the sulfur passivated InP substrate, InP Schottky diodes, and InP MIS diodes are presented in §4.3. The sulfur passivation of InP/InGaAs MSM-PDs will be discussed in Chapter 5.

4.2 EXPERIMENTAL PROCEDURES

InP substrates were chemically cleaned as described in Chapter 2. Sulfur passivation was implemented using an ammonium polysulfide solution, $(\text{NH}_4)_2\text{S}_x$. The ammonium polysulfide solution was prepared as follows: 5 g of sulfur (S) were dissolved into 50 ml of a commercial ammonium sulfide solution, $(\text{NH}_4)_2\text{S}$; then flowing oxygen (O_2) was used to bubble the solution for 45 minutes. The following passivation procedure was used for the InP samples:

- 1) 3 ml of the above ammonium polysulfide solution, $(\text{NH}_4)_2\text{S}_x$, were diluted by 45 ml of de-ionized water, and stirred evenly before putting InP samples into the prepared solution.
- 2) The samples were dipped into HF (1:10) for 20 seconds, and then immediately put into the sulfide solution. This is to remove the surface oxide from the samples.
- 3) The solution was heated by a hot plate to 60°C .
- 4) During the passivation, the sulfide solution was illuminated by a 600 W tungsten lamp.
- 5) The passivation took about 15 minutes. After that, the passivated samples were removed from the sulfide solution, rinsed in fresh $(\text{NH}_4)_2\text{S}$ for 2 minutes, and then rinsed in de-ionized water and blown dry by N_2 .

In this investigation, sulfur passivations of InP surfaces for different samples in different ways were tested to obtain the best results. These are listed below.

I. InP Substrates

To find out the best conditions for the passivation of InP substrates, the following passivation recipes were tested:

- 1) $(\text{NH}_4)_2\text{S}_x$ solution, 60°C, 600 W tungsten light illumination, 20 minutes;
- 2) $(\text{NH}_4)_2\text{S}_x$ solution, 60°C, 600 W tungsten light illumination, 10 minutes;
- 3) commercial $(\text{NH}_4)_2\text{S}_x$ solution, 60°C, 35 minutes.

Samples passivated by the above methods were characterized by Auger electron spectroscopy (AES) and photoluminescence (PL). The results were compared to those obtained from as received (not sulfur passivated) InP substrates.

II. InP Devices

As will be shown in the next Section, it was found that passivation using $(\text{NH}_4)_2\text{S}_x$ at 60°C for 20 minutes was more effective than others. The passivation of InP devices, such as InP Schottky diodes, InP MIS diodes, InP MSM-PDs and InP/InGaAs MSM-PDs, was done under these conditions in different ways as listed below.

- 1) The whole sample surface was sulfide passivated after sample cleaning and before patterning;
- 2) The active areas, where SiO_2 if applicable was removed, were passivated;
- 3) Only the areas beneath the metal contact (or finger electrodes in MSM-PDs) were passivated. This was done after metal contacts were patterned;
- 4) Device passivation was performed after lift-off.

III. Characterization

AES, PL and electrical characterization were performed to analyze the effects of passivation. Auger analysis was carried out with a Perkin-Elmer Model PHI-600 Scanning Auger Microprobe using a 3 kV electron beam (77 nA beam current) rastered over a $200 \times 150 \mu\text{m}^2$ area. Sputtering was performed using a 3 kV Ar^+ ion beam rastered over a $1 \times 1 \text{mm}^2$ area. The sputter rate, under these conditions, was estimated as 42 nm/min for the SiO_2 layer. Auger surface survey scans were collected on the as-received surface and after a 30 second sputter. Elemental composition was obtained using the relative sensitivity factors supplied by the manufacturer.

Photoluminescence measurements were made using a 488 nm Ar^+ ion laser source at both room temperature and at 13.5K. In the PL measurements, 4 samples passivated in different ways were mounted on the same stage at the same time. For each sample, careful alignment of the laser beam was necessary to maximize the incident and the reflected laser power.

The experimental set up for electrical characterization is similar to that shown in Figure 3.2-2. The temperature range was from 80K to 360K. Capacitance - voltage measurements were carried out using an HP 4277A LCZ meter at a frequency ranging from 10 KHz to 1 MHz. Current - voltage measurements were conducted using an HP 4145B semiconductor analyzer. For both C-V and I-V measurements, voltage scans from high to low and from low to high were taken and resulting experimental data were averaged.

4.3 RESULTS AND DISCUSSION

4.3.1. InP Substrate

I. Auger Electron Spectroscopy (AES)

The InP samples used in the sulfur passivation are listed in Table 4-3.1. Figure 4-3.1 shows the Auger electron spectra of InP substrates (both as-received and after 30-second sputtering). Evidence of sulfur on the passivated InP surface was obtained as shown in Figure 4-3.1(a - f) . After 30 second sputtering, the sulfur atoms on the passivated InP surface were almost gone (or at least reduced significantly). For samples 3 and 4, 30 second sputtering almost removed the surface layers. Detected concentrations of In and P reached 50% which is the nominal composition of bulk InP. For samples 1 and 2, the In and P concentrations still do not reach their concentration in bulk material. Based on the experimental results, the oxygen concentration on the InP surface is less on the sulfur passivated samples (especially in samples 1 and 2) than on the untreated ones, while the concentration of carbon is much higher in the sulfur-passivated samples than the untreated ones. This could be the contamination from the sulfide solution during passivation.

Table 4.3-1. InP Samples for Sulfur Passivation

Sample #	Passivation Conditions
1	$(\text{NH}_4)_2\text{S}_x$, 60°C, 600 W tungsten light illumination, 20 minutes
2	same as #1, RTA@300°C, 20 seconds
3	$(\text{NH}_4)_2\text{S}$, room temperature, 45 minutes
4	without sulfur passivation

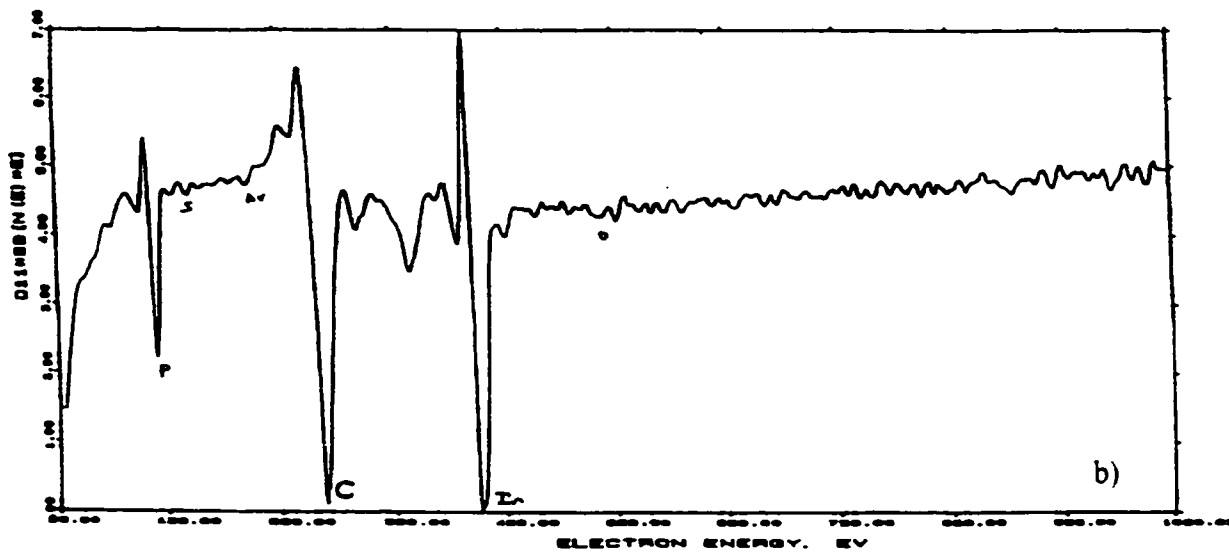
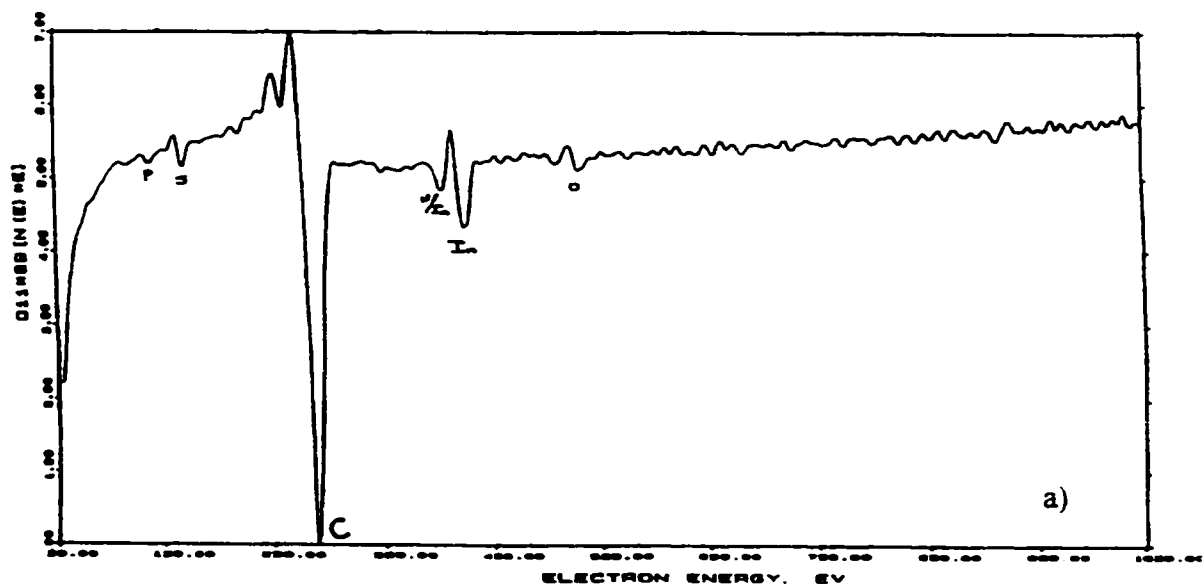


Figure 4.3-1a and b. Auger electron spectra of InP (sample #1): a) as received; b) after 30 second sputtering. The InP sample was passivated by $(\text{NH}_4)_2\text{S}_x$, 600 W tungsten light illumination, for 20 minutes

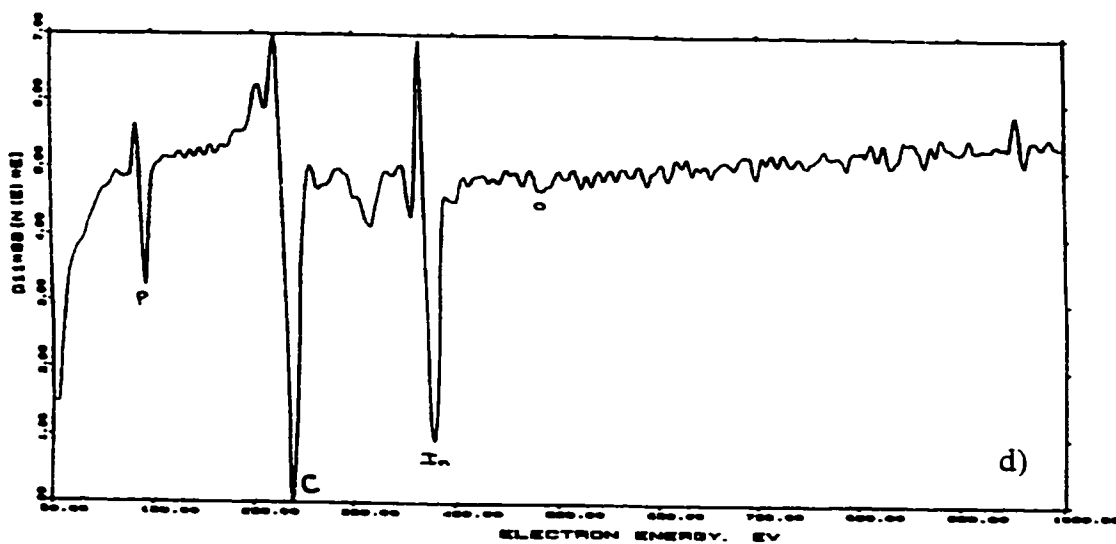
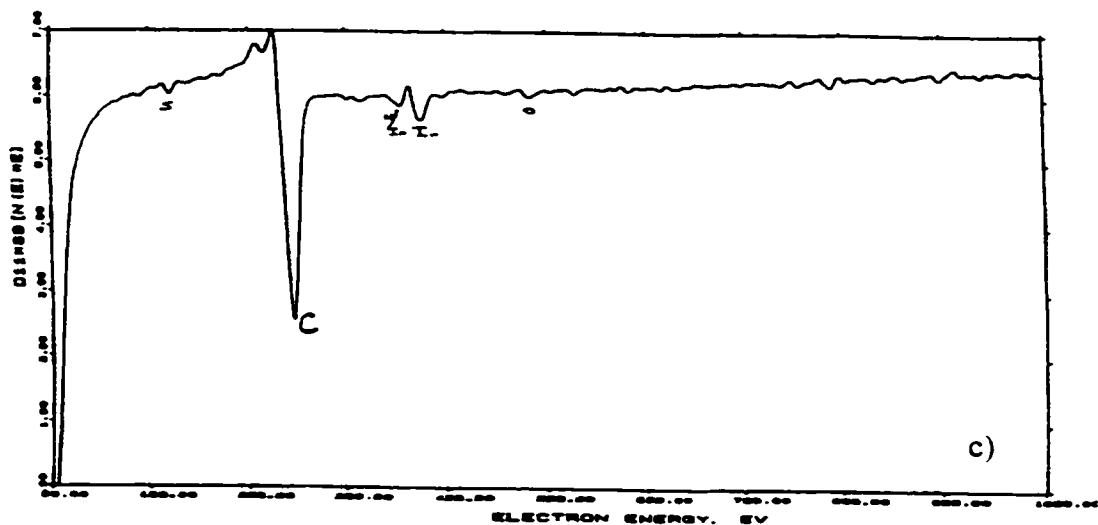


Figure 4.3-1c and d. Auger electron spectra of InP (sample #2): c) as received; d) after 30 second sputtering. The InP sample was passivated by $(\text{NH}_4)_2\text{S}_x$, 600 W tungsten light illumination, for 20 minutes, then was annealed at 300°C , 20s.

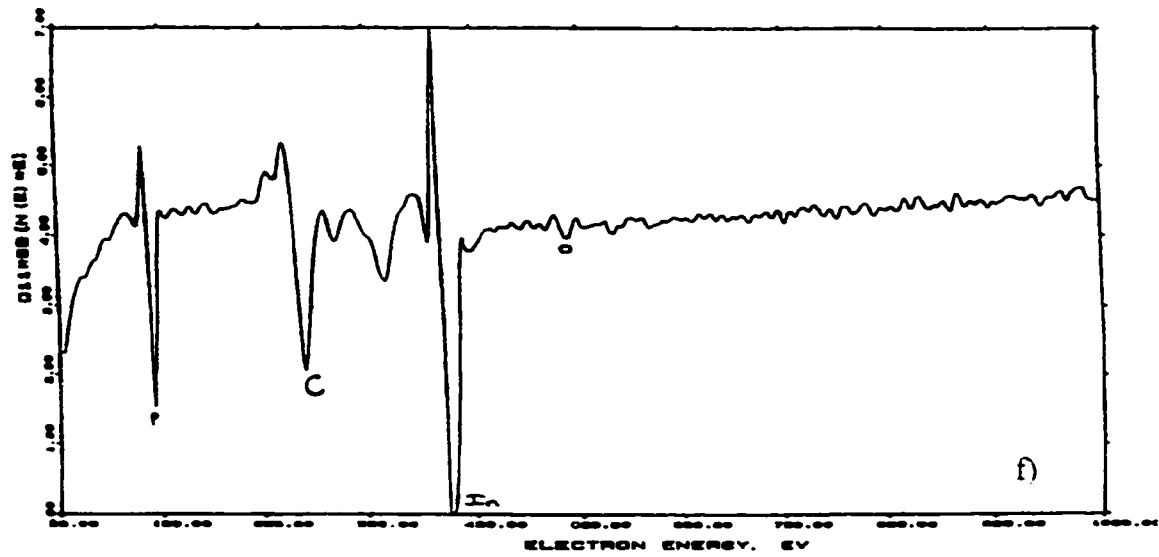
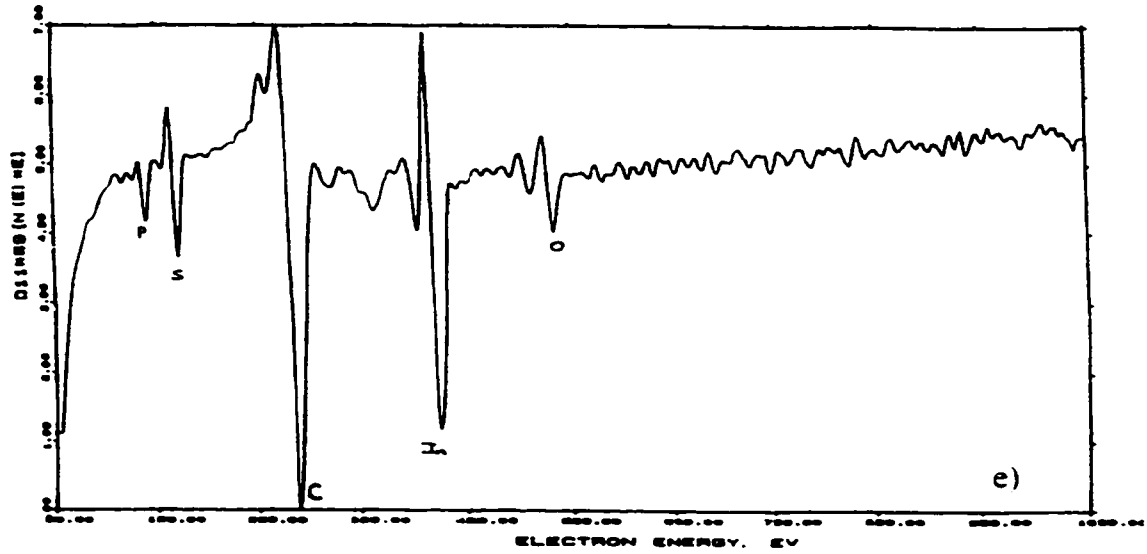


Figure 4.3-1e and f. Auger electron spectra of InP (sample #3): e) as received; f) after 30 second sputtering. The InP sample was passivated by $(\text{NH}_4)_2\text{S}$ at room temperature for 45 minutes.

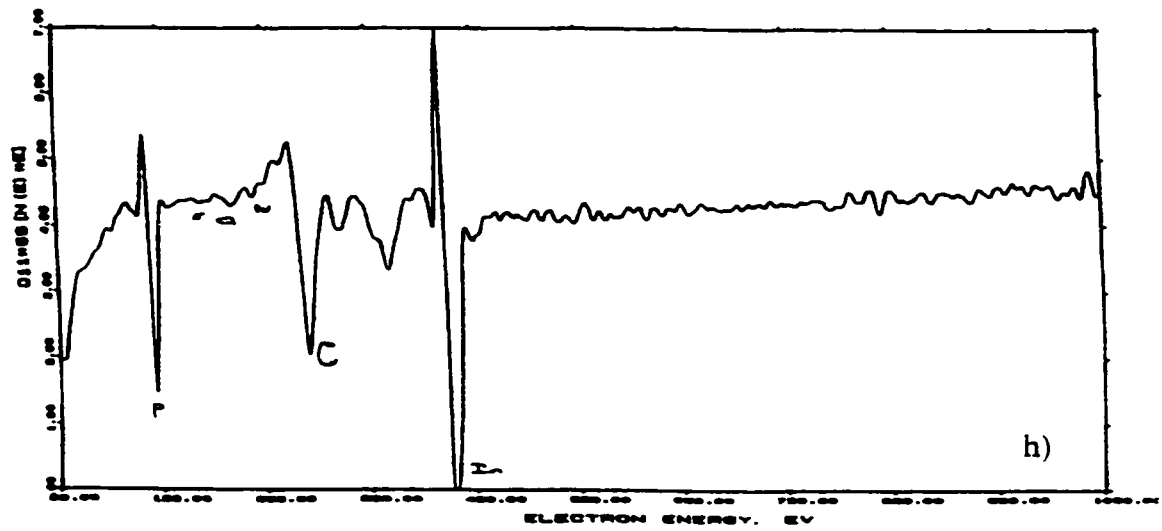
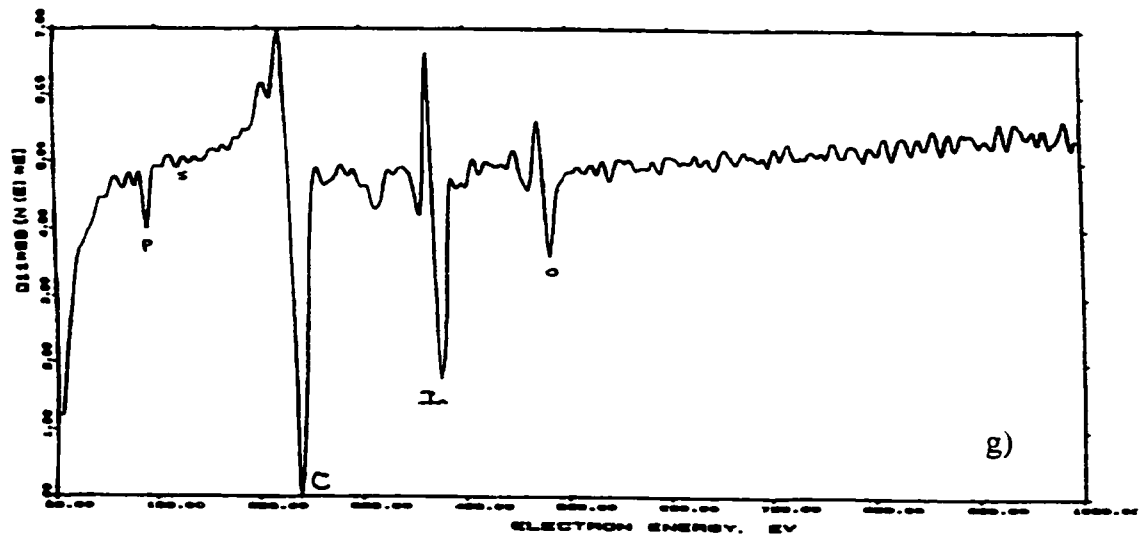


Figure 4.3-1g and h. Auger electron spectra of InP without any sulfide passivation (sample #4): g) as received: h) after 30 second sputtering.

II. Photoluminescence (PL)

1) Radiative Recombination, Conduction Band to Acceptors

Room-temperature photoluminescence spectra of the InP samples are shown in Figure 4-3.2a. The PL spectra are composed of broad, structureless emission bands. The peaks, centered at 1.342 eV ($\lambda = 925$ nm), are due to the radiative transition of electrons from the conduction band edge to acceptors. As is shown in the figure, the PL signals are much stronger from the sulfur-passivated InP samples than the untreated samples. This is a common observation in sulfur passivated InP [Han 1996], and similar observations were reported on GaAs [Besser, 1988, Shikata, 1991], and other III/V semiconductors [Ogiwa, 1991]. The increase of the PL intensities after sulfur treatment is due to the reduction of the surface nonradiative recombination velocity caused by the reduced

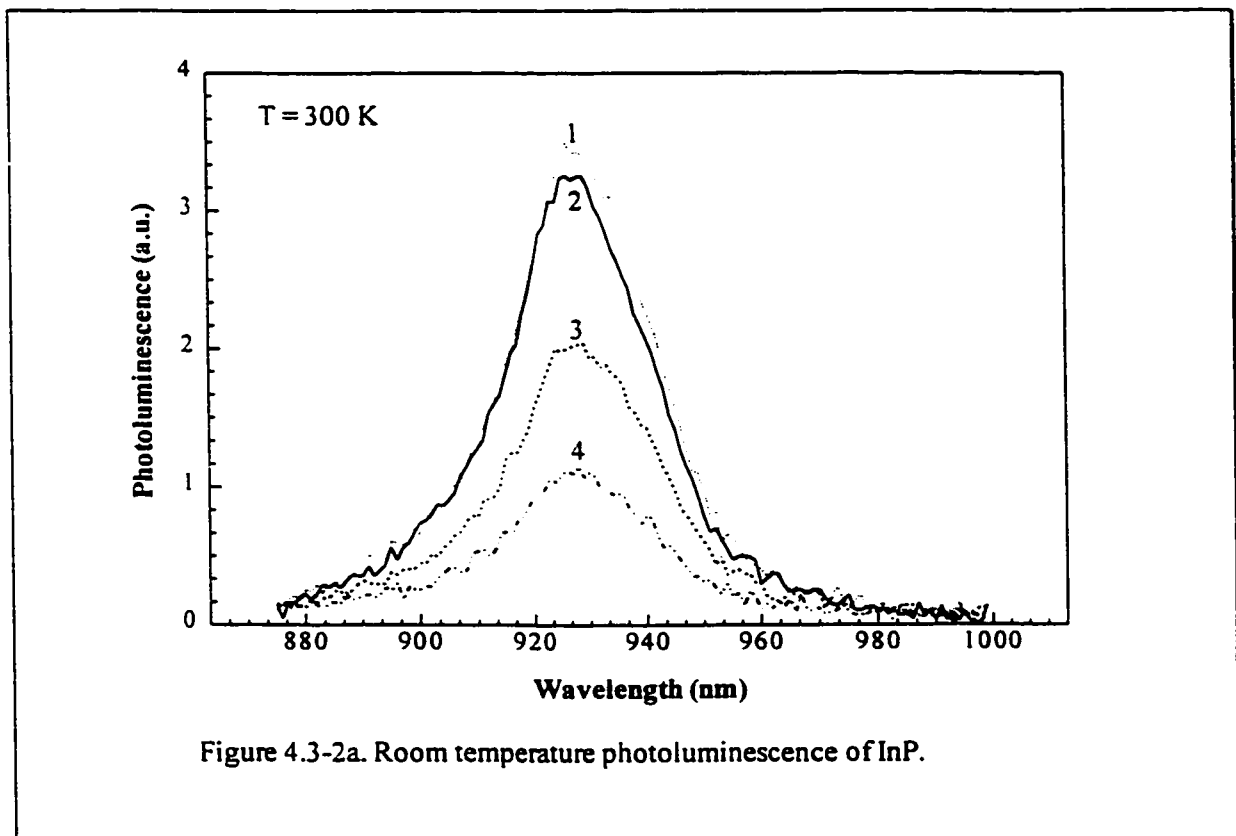
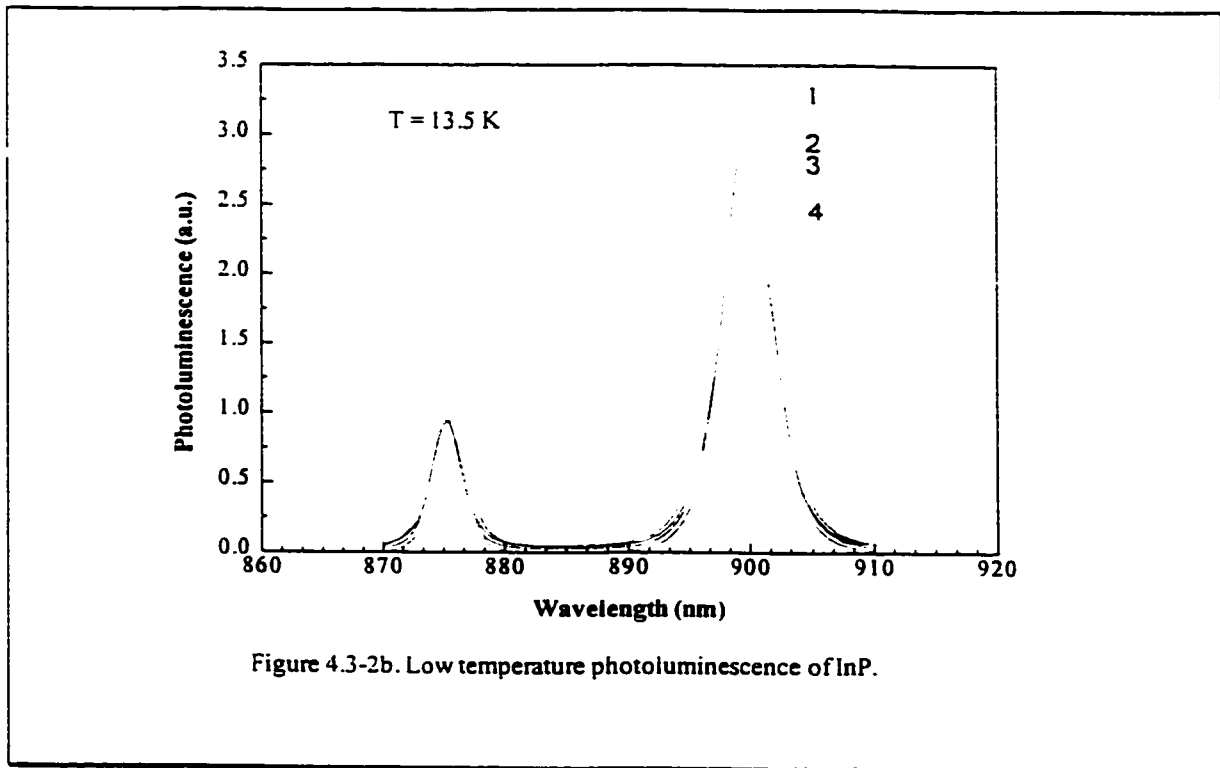


Figure 4.3-2a. Room temperature photoluminescence of InP.



surface states [Sandroff, 1989]. Similar trends were observed in low temperature PL, as is shown in Figure 4.3-2b. The peak centered at about 900 nm is due to the transition from the conduction band to acceptor while the one at 876 nm is due to the transition from conduction band to valence band.

2) Radiative Recombination via Surface States

Recently, it was reported [Han, 1996] that in the InP PL spectra there is a sub-peak centered at a lower energy position relative to the main PL peak (Figure 4-3-3a). After sulfur treatment, this PL band almost disappears (Figure 4-3-3b). This sub-PL band is attributed to the recombination via surface states. In my experiment, however, no such PL band was observed as is shown in Figure 4.3-4.

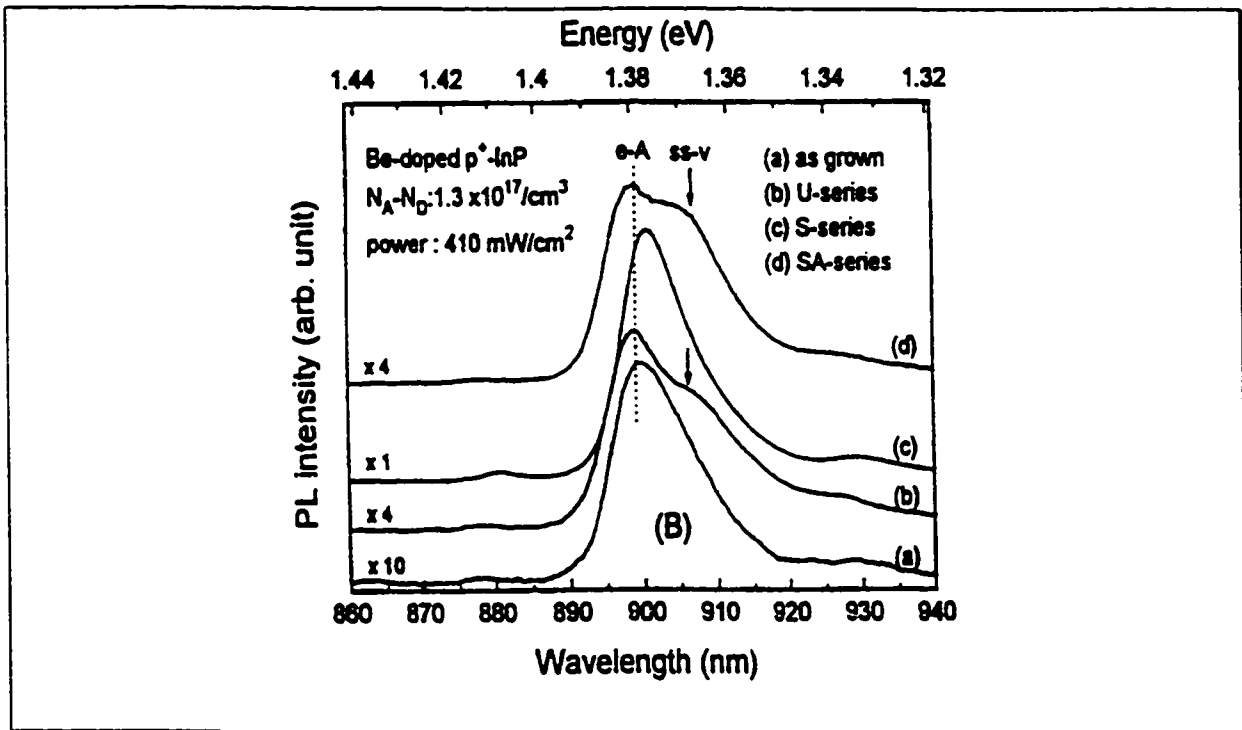
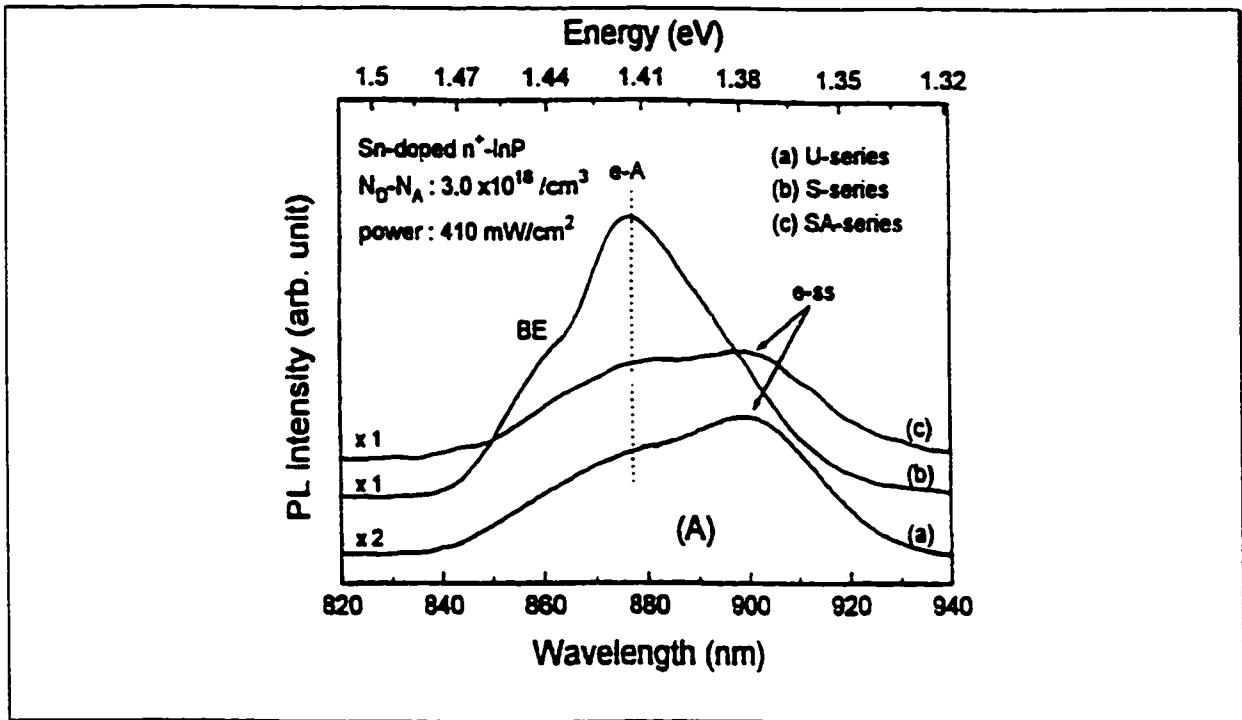
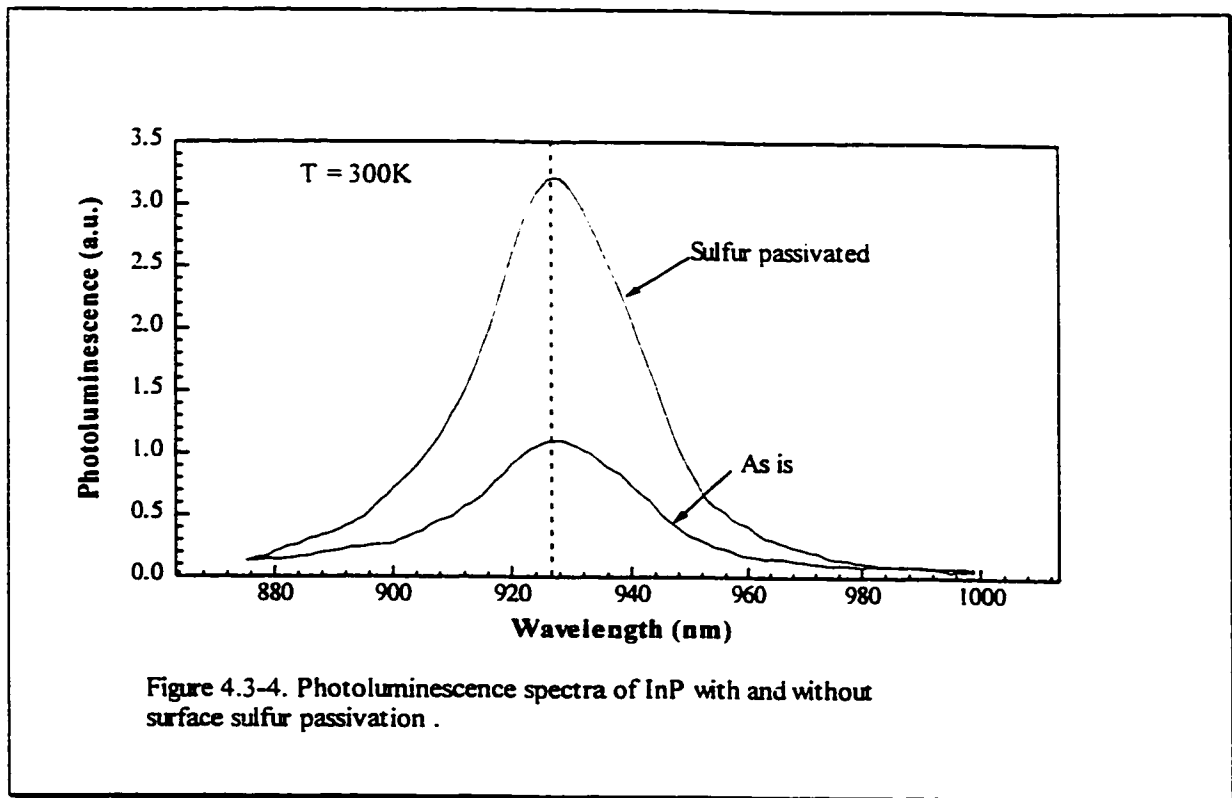


Figure 4.3-3. PL spectra of A) n^+ -InP and B) p^+ -InP treated under different conditions. The PL bands centered at 1.376 eV for n^+ -InP and at 1.367 eV for p^+ -InP disappear and reappear by the sulfide treatment and the subsequent annealing. U - untreated, S - sulfide treated, and SA - sulfide treated and annealed. (Han, 1996)



It is recognized that sulfur treatment produces a reduction in the surface recombination velocity (SRV). It is difficult to tell whether this effect is the result of the reduction in the density or in the capture cross section of the surface (interface) defects.

4.3.2. InP Schottky Diodes

Table 4.3-2 shows the results of different metallization schemes used in fabricating InP Schottky diodes. Surface sulfur passivation was done using $(\text{NH}_4)_2\text{S}_x$. As is shown in the Table, the effective barrier height is slightly increased with sulfur passivation while the ideality factor remains unchanged. The increase in the effective barrier height is attributed to (1) a reduction in the surface and interface states, and (2) the formation of a thin interfacial layer, In_xS_y , which reduces the carrier transport across the MS interface.

Table 4.3-2. Schottky barrier heights of different metals deposited on InP obtained from I - V measurements

	ϕ_b (± 0.01 eV)		n (± 0.01)	
	As - deposited	Sulfide passivated	As - deposited	Sulfide passivated
Au	0.41	0.42	1.00	1.01
Au/Al	0.38	0.40	1.01	1.01
Au/Ti	0.38	0.41	1.02	1.01
Au/Pt	0.43	0.45	1.02	1.02
Au/Ni/Pt	0.44	0.47	1.02	1.02
Au/Ti/Pt	0.47	0.48	1.01	1.02
Au/Pt/Ti	0.39	0.40	1.03	1.03
AuPt/Ti/Pt	0.48	0.50	1.03	1.02

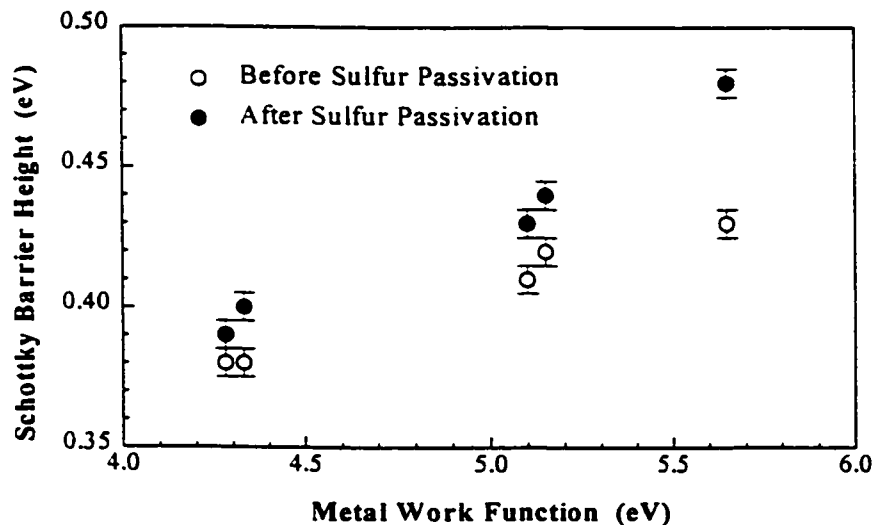


Figure 4.3-5. Barrier height of metal/InP Schottky diodes measured as a function of the metal work function before and after sulfur passivation.

It was reported [Robinson, 1985] that the Fermi-level is usually pinned in InP. Sulfur passivation causes the Fermi-level to unpin and makes the Schottky barrier height more dependent on the metal work function [Han, 1996]. Figure 4.3-5 shows this quite clearly.

**Table 4.3-3. Barrier Height and Ideality Factor
of Au/Ni/Pt-InP Schottky Diodes**

	As is	300°C, 30 s	300°C, 60 s	400°C, 30 s
ϕ_b (± 0.01 eV)	0.44	0.48	0.49	0.46
n (± 0.01)	1.02	1.02	1.03	1.06

As is shown in Table 4.3-3, the barrier height was found to slightly increase after thermal annealing at 300°C for 30 seconds, from 0.47 eV to 0.49 eV. No significant change was observed for annealing at 300°C for 60 seconds, but degradation was observed for annealing at 400°C for 30 seconds.

4.3.3. InP MIS Diodes

Frequency-dependent C-V measurements are most commonly used to determine the surface and interface state density of a metal-semiconductor (Schottky) diode or metal-insulator-semiconductor (MIS) diode. It is well known that the capacitance of the Schottky contact is extremely sensitive to the interface properties. This occurs because of the interface states, which respond differently to low and high frequencies. It is commonly accepted that the interface states cannot follow an a.c. signal at very high frequency. However, they respond to low frequency a.c. signals; therefore, the interface

states contribute to the capacitance measured at low frequency. The high-and-low (Hi-Lo) frequency technique was employed to determine the interface state density in Schottky diodes [Chattopadhyay, 1995] and in MIS diodes [Landheer et al., 1994]. In the Hi-Lo C-V technique, the high frequency is usually set to 1 MHz or higher, while the low frequency is usually about 1 Hz or lower (called quasi-static).

Due to limitations by the experimental facilities, the C-V measurements were only implemented in a frequency range of 10KHz - 1MHz. Although the interface state density could not be quantitatively determined, the dependency of the capacitance on frequency was monitored. Figures 4.3-6 and 4.3-7 show how the capacitance of a Schottky diode and a MIS diode, respectively, varies with the bias voltage, with the frequency as a parameter. In both cases, sulfur passivation reduces the frequency dependence of the

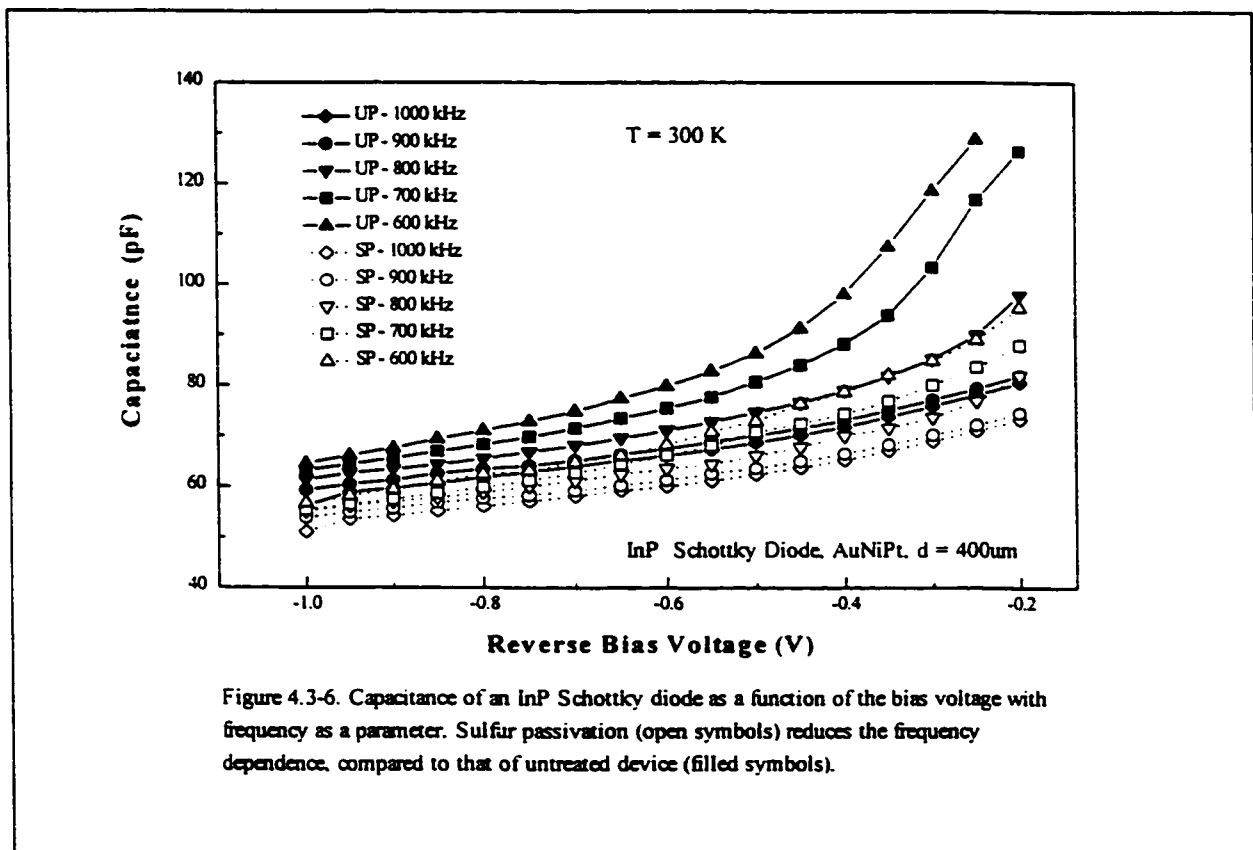


Figure 4.3-6. Capacitance of an InP Schottky diode as a function of the bias voltage with frequency as a parameter. Sulfur passivation (open symbols) reduces the frequency dependence, compared to that of untreated device (filled symbols).

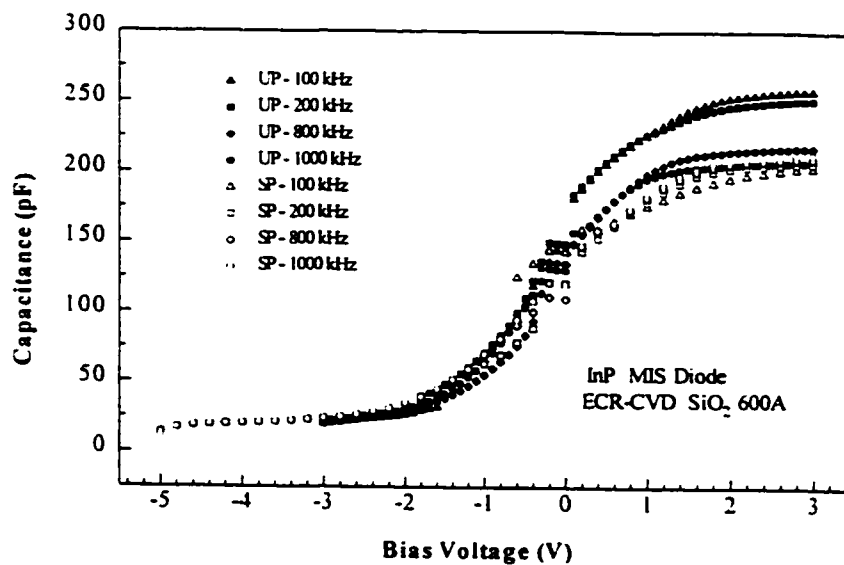


Figure 4.3-7. Capacitance of an MIS diode as a function of the bias voltage with frequency as parameter. Sulfur passivation (open symbols) reduces the frequency dependence, compared to that of the untreated device (filled symbols).

device's capacitance. This is attributed to the reduction of the interface state density after sulfur passivation. As will be seen in Chapter 5, it is observed that sulfur passivation also reduces the frequency dependence of InP MSM-PDs, similar to those of Schottky diodes and MIS diodes discussed above. It was reported [Landheer, 1994] that sulfur passivation reduced the interface state density (from $1 \times 10^{14} \text{ eV}^{-1} \text{ cm}^{-2}$ to about $2 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$) in InP MIS diodes.

4.3.4. InP MSM-PDs

InP wafers were used to fabricate MSM photodetectors with $2 \mu\text{m}$ finger width and $2 \mu\text{m}$ finger spacing. The dark currents and breakdown voltages of the InP MSM-PDs fabricated in different ways are shown in Table 4.3-4. No spin-on glass (SOG) was used

Table 4.3-4. Dark Currents of InP MSM-PDs

MSM-PD (2×2)	I_d (μA) @5V	I_d (μA) @10V	V_{BD} (V)
A0	4.5	6.5	> 20
A1	2.3	4.5	~ 20
B0	0.38	0.45	~ 18
B1	0.17	0.22	~ 16

in device A between the contact pads and semiconductor (InP). In device B, SOG was used. Devices A0 and B0 were not sulfur treated, while A1 and B1 were sulfur passivated. As can be seen from the Table, employment of SOG between the contact pads and the semiconductor can significantly reduce (by about one order of magnitude) the dark currents because of the reduction in the conduction areas. As will be discussed in Chapter 5, an alternative to this is the use of mesa etchdown to the SI InP substrate. In both cases (with and without SOG), passivation results in a reduction of the dark current by a factor of 2.

4.3.5. InGaAs MSM -PDs

The application of sulfur passivation in InGaAs MSM photodetectors was also investigated. The results are presented in Chapter 5. A brief summary is given below.

- 1) The saturation capacitance was slightly reduced after sulfur passivation. This is mostly attributed to the formation of an interfacial layer, In_xS_y , which is very stable.
- 2) The slope of the C-V plot of the untreated MSM is steeper than that of sulfur treated MSM, which indicates more interface states in the untreated device.
- 3) Sulfur passivation reduced the dark current by a factor of 2, from 400 - 500 nA to 200 - 300 nA for a $2\mu\text{m} \times 2\mu\text{m}$ device.
- 4) The I-V characteristics of sulfur passivated MSMs are more consistent from device to device.
- 5) The photoresponse from sulfur passivated MSMs is less bias dependent. This indicates that the effects of field-dependent factors, such as internal gain, are minimized by sulfur passivation.
- 6) Sulfur passivation does not affect the frequency response of MSM photodetectors, because the frequency response is mainly limited by the carrier transit time in a MSM devices.

Chapter 5

InGaAs METAL-SEMICONDUCTOR-METAL PHOTODETECTORS (MSM-PDS)

5.1 INTRODUCTION

5.1.1 Technical Importance of InGaAs Metal-Semiconductor-Metal (MSM)

Photodetectors

Ultra-fast photodetectors in the wavelength range from 1.3 to 1.55 μm are important in long-haul optical-fiber communication systems and interconnects, especially those with data transmission rates beyond 10 Gbits/s. This means that impulse response times in the range of 10 ps and bandwidths up to 100 GHz are required. Vertical p-i-n and Schottky photodiodes making use of InGaAs or GaAs as photoactive materials have been successfully fabricated to meet these requirements. The trend towards monolithic integration of optoelectronic circuits, however, has stimulated appreciable research activities directed towards the development of ultra-wide band planar photodetectors which can be easily fabricated and are compatible with metal-semiconductor field-effect-transistors (MESFET) or heterostructure field-effect-transistors (HFETs) processes.

The interdigitated metal-semiconductor-metal (MSM) photodetector is potentially the most promising candidate which meets these requirements. Due to its lower parasitic

capacitance, high-speed performance, simplicity of fabrication, and compatibility with field-effect transistors (FETs) in monolithic integration. MSM-PDs are getting more and more attention as the photoreceivers in long-wavelength optical communication systems. Although MSM-PDs have lower responsivity compared to PIN photodetectors, they still have large responsivity-bandwidth products. Therefore a large-area MSM-PD can still have reasonably high bandwidth and sensitivity.

MSM-PDs consist essentially of two back-to-back Schottky diodes realized by an interdigitated electrode pattern. Their performance is critically dependent on the quality of the Schottky contact.

The fabrication of photodetectors for the long wavelength range using the InGaAs-InP material system is complicated by the relatively low Schottky barrier height (~ 0.2 eV) on InGaAs. This will result in large leakage currents and low breakdown voltages.

5.1.2. Barrier Enhancement Layer

In order to overcome these problems (low barrier height and large leakage current), the investigations on InGaAs MSM-PDs have been focused on devices with additional epitaxial cap layers, having a larger bandgap than InGaAs. Such layers, which serve to enhance the Schottky-barrier height, have been grown using both lattice-matched and lattice-mismatched materials, to InGaAs with a typical thickness of several hundred Angstroms. Many barrier enhancement material systems have been investigated, such as lattice-matched $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ [Soole, 1989, Kuhl 1995, Kim, 1992, Wada 1989, Burroughes, 1992, Parker 1992], Fe-doped [Kuhl 1990, Hieronymi, 1994] or undoped

InP [Wei, 1990. Böttcher, 1992, Horstmann, 1995. Shi, 1992. Yang, 1990. Hieronymi 1993], AlGaAs [Hong, 1989], and even inserting a graded layer, or superlattice between the InGaAs and the cap layer [Wada, 1989. Parker, 1992. Burroughes, 1992]. p^- -InGaAs [Averin, 1993] and p^-/n - InP [Malachý, 1994] were also investigated as the barrier enhancement layers. So far, however, low-leakage current densities have only been demonstrated with Schottky-barrier enhancement layers such as InAlAs and InP grown lattice-matched to InGaAs.

Besides using InP substrates, InGaAs MSM-PDs were also grown on Si [Sasaki, 1994. Bartels, 1996] and on GaAs [Masum Choudhury, 1991, Gunapala, 1994].

I. InAlAs

Both MOCVD (OMVPE) grown [Soole, 1989, Parker 1992] and MBE grown [Wada, 1989, Kim, 1992, Burroughes, 1992] $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ material has yielded devices with good performance characteristics. $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ (lattice-matched) has an energy band gap, E_g , of 1.47 eV. The Schottky barrier height of a metal - InAlAs contact is relatively high at ~ 0.8 eV. Although InGaAs MSM-PDs using InAlAs as barrier enhancement layer have good performance, there are several problems to be overcome. The use of InAlAs has all the common Al-related problems, such as DX centers, aging and lack of etch control, high interface state density, oxide breakdown and oxidation of the Al-rich material. Due to the large conduction band discontinuity of the InAlAs/InGaAs interface, ΔE_c , significant charge storage occurs at the abrupt

heterojunction which will slow down the device speed. In addition, the presence of Al in the ternary compound makes the MOVPE-growth complicated.

II. InP

To avoid the Al-related problems when using InAlAs as barrier layer in an InGaAs MSM-PD, InP as the barrier enhancement layer has been intensively investigated [Wei, 1990, Böttcher 1992, Horstmann, 1995, Shi, 1992, Yang, 1990, Kuhl, 1990, Hieronymi, 1993 & 1994]. The Schottky barrier height on InP is about 0.4 - 0.5 eV.

Moreover, Fe-doped InP and Fe-doped InGaAs with high resistivity, has been grown on SI InP for the fabrication of MSM-PDs. In Fe-doped InP, the Fermi-level is pinned at the Fe-acceptor level and, consequently, Schottky barrier heights for both electrons and holes are raised to be about 0.68 eV [Yang, 1989], resulting in a reduced dark current of MSM-PDs. Because of the low residual carrier concentration in Fe-doped InP and Fe-doped InGaAs, low bias is sufficient to deplete the device. The capacitance at low bias is lower compared to that of undoped n-InP/InGaAs [Böttcher, et al., 1992].

Besides InP, a structure consisting of p^+/n - InP [Malacky, et al., 1994] was used as the barrier layer in an InGaAs MSM-PD. The InP layers were chosen in such a way that both are fully depleted without external bias. A Schottky barrier height of 0.64 - 0.66 eV for $p^+ = 2 \times 10^{18} \text{ cm}^{-3}$, $n = 2 \times 10^{15} \text{ cm}^{-3}$ was reported.

To further increase the Schottky barrier height, $\text{In}_{1-x}\text{Ga}_x\text{P}/\text{InP}$ as the barrier layers [Yuang, 1995a,b; Chyi, 1994] was investigated in InGaAs MSM-PDs. This makes use of the advantage of including a wide band gap material, $\text{In}_{1-x}\text{Ga}_x\text{P}$ ($E_g = 2.27 \text{ eV}$ for GaP).

The Schottky barrier height of such a structure was significantly increased from 0.43 eV (for InP only) to 0.73 eV ($\text{In}_{1-x}\text{Ga}_x\text{P}/\text{InP}$, $x = 0.25$) [Chyi, 1994].

5.1.3. MSM-PD Modeling and Simulation

The MSM-PD theory was first completely discussed by Sze [Sze, 1971] in which the current transport, including electron and hole currents, under low and high biases, was treated in detail based for a one-dimensional model for a Si MSM-PD.

In practical applications, InGaAs MSM-PDs are made as lateral structures, which are quite different from those described by Sze [Sze, 1971], and must be treated in a two-dimensional model. Several groups [Sano, 1990, Böttcher, 1992, Averin, 1996] have proposed two-dimensional models to solve Poisson's equation, the current continuity equation and related boundary conditions to give the properties of current transport. Unfortunately, as the two-dimensional structure is too complicated to give an analytical description, all such models are numerical or computerized ones. Two dimensional (2D)-ensemble Monte Carlo calculations [Sano, 1991] and numerical studies [Peterson, 1987] of MSM-PDs were commonly used.

In addition to capacitance, dark current, breakdown voltage, responsivity and quantum efficiency, speed is an important parameter of InGaAs MSM-PDs. Unlike other photodetectors, the speed of an InGaAs MSM-PD is mainly determined by the carrier-transit time due to its low capacitance and, therefore, small RC charging time. Soole and Böttcher analyzed the transport of electrons and holes to obtain the temporal response of an InGaAs MSM-PD based on the transit-time model [Soole, 1990, Böttcher, 1993].

Auston [Auston, 1983] analyzed the impulse response of photodetectors in transmission lines. The unit current gain cutoff frequency of MSM-PDs was analyzed using a 2D bipolar physical model by Ashour [Ashour, 1995]. Jeong [Jeong, 1995] investigated the frequency response of MSM-PDs, while Benterud [Benterud, 1993] conducted frequency-response measurements using an electro-optic modulator.

Other investigations, such as polarization and wavelength dependence of MSM-PDs [Kuta, 1994], surface sensitivity [Darling, 1990], photocurrent gain [Klingenstein, 1994], noise characterization [Soole, 1991, Parker, 1992], and absorption and index of refraction of InGaAs/InP photonic devices [Reid, 1993] have been addressed.

5.1.4. Fabrication

InGaAs MSM structures are commonly grown by MOCVD or MBE on semi-insulating InP substrates. Usually, an InP buffer layer of 2000 - 5000 Å is grown on the InP substrate before the active layer InGaAs. The thickness of InGaAs is typically from 1 to 2 µm in consideration of speed and efficiency. The top Schottky contact layer (or barrier enhancement layer) using InAlAs, InP or other materials is about 200 - 500 Å.

Au-based metallization schemes, such as Au/Ti, Au/Pt, Au/Ti/Pt, and Au/Pt/Ti are commonly employed to make the Schottky contacts. The contact electrodes are interdigitated-fingers. The finger width ranges from 1 to 5 µm while the finger spacing ranges from 1 to 10 µm. The active area is about 20×20 to 50×50 µm² in a square pattern, or a circular pattern with a diameter of 50 - 100 µm [Burroughes, 1992].

To minimize the finger shadowing and therefore increase the quantum efficiency, semi-transparent electrodes were used [Yuang, 1995]. Antireflection coatings, such as Si_3N_4 [Kim 1992, Wada, 1992], were employed to reduce the reflection of incident light and therefore increase the external efficiency.

The most commonly used dielectric layer to isolate the contact pads and the semiconductor are Si_3N_4 [Kim, 1992, Wada, 1992, Hong, 1989] or SiO_2 [Lee 1988, Ambree 1995], or even polymers [Lee 1988]. This isolation between metal contact pads and the semiconductor or from device to device can also be achieved by mesa etchdown [Soole, 1989, Hong, 1989].

The MSM-PDs are either front or back illuminated. The former technique which is simple and compatible with FET integration is the most commonly used. However, it was reported that the latter had higher responsivity [Kim, 1992, Hieronymi, 1994].

A MSM-PD is a lateral conduction device, and the surface layer plays an important role in the performance of the device. Surface passivation of MSM-PDs has been employed to improve the performance, such as dark current and internal gain. Sulfide solutions [Schade, 1994, Han 1994], Si_3N_4 [Lee, 1988, Kim, 1992, St Kollakowski 1994], SiO_2 [Lee, 1988, Ambree, 1995], polymers [Lee 1988], and even Al_2O_3 [Klockenbrink, 1994] were investigated for InGaAs MSM-PD surface passivation.

5.1.5 Monolithic Integration of MSM-PDs with FETs

Monolithic integration of InGaAs MSM-PD - FETs photoreceivers has been successfully achieved. MSM-HEMT transimpedance photoreceivers fabricated using

OMCVD grown InAlAs/InGaAs heterostructures on InP substrates [Chang, 1990] were reported to have bandwidths of 3 GHz. An integrated waveguide MSM-HEMT amplifier receiver using the InAlAs/InGaAs material system with a bandwidth of 820 MHz was obtained [Hong, 1989, 1991]. A four-channel receiver using InAlAs-InGaAs MSM-HEMTs for wavelength-division-multiplexing systems (WDM) which has a sensitivity of -25.2 dBm at a 1.2 Gb/s data rate was reported [Chang, 1991]. Harrang [Harrang, 1991] investigated the InAlAs/InGaAs HFET structure compatible with MSM integration, grown by MBE. With MSM layers beneath, it was found that the FETs had a transimpedance of 390 mS/mm, and a cutoff frequency of 30 GHz for a device with a 1.0 μm gate.

InGaAs MSM-FET photoreceivers using Fe-doped InP as barrier layer, grown by chemical beam epitaxy, were reported [Yang, 1990]. Although the discrete MSM-PDs and FETs themselves had good performance, the integrated photoreceiver had a bandwidth of only 200 MHz. This was attributed to the charge storage at the metal/InP and InP/InGaAs interfaces.

Details of the design and performance analysis of InP-based high-speed and high-sensitivity optoelectronic integrated receivers can be found in John [1994], while a discussion of monolithic integration of optical waveguide circuitry with III-V photodetectors for advanced lightwave receivers can be found in Deri [1993].

In this chapter, the results of measurements of InGaAs MSM-PDs using InP as the barrier layer grown by GS-MBE are presented. In section 5.2, a brief summary of MSM

theory is given. The experimental details of this investigation are given in Section 5.3. Results and a discussion are arranged in Section 5.4.

5.2 MSM-PD THEORY

A schematic of a MSM-PD is shown in Figure 5.2-1. When a bias is applied to the interdigitated finger electrodes, the semiconductor beneath the electrodes will be depleted. Currents will flow between the oppositely biased electrodes. The electron current will be determined by the Schottky barrier at the negatively biased electrode semiconductor contact (for simplicity, say Contact No 1), while the hole current is mainly determined by the Schottky barrier (for holes) at the forward biased electrode semiconductor contact (say, Contact No 2) which is more significant at high biases. When light illuminates the finger area (active area), photogenerated carriers will be

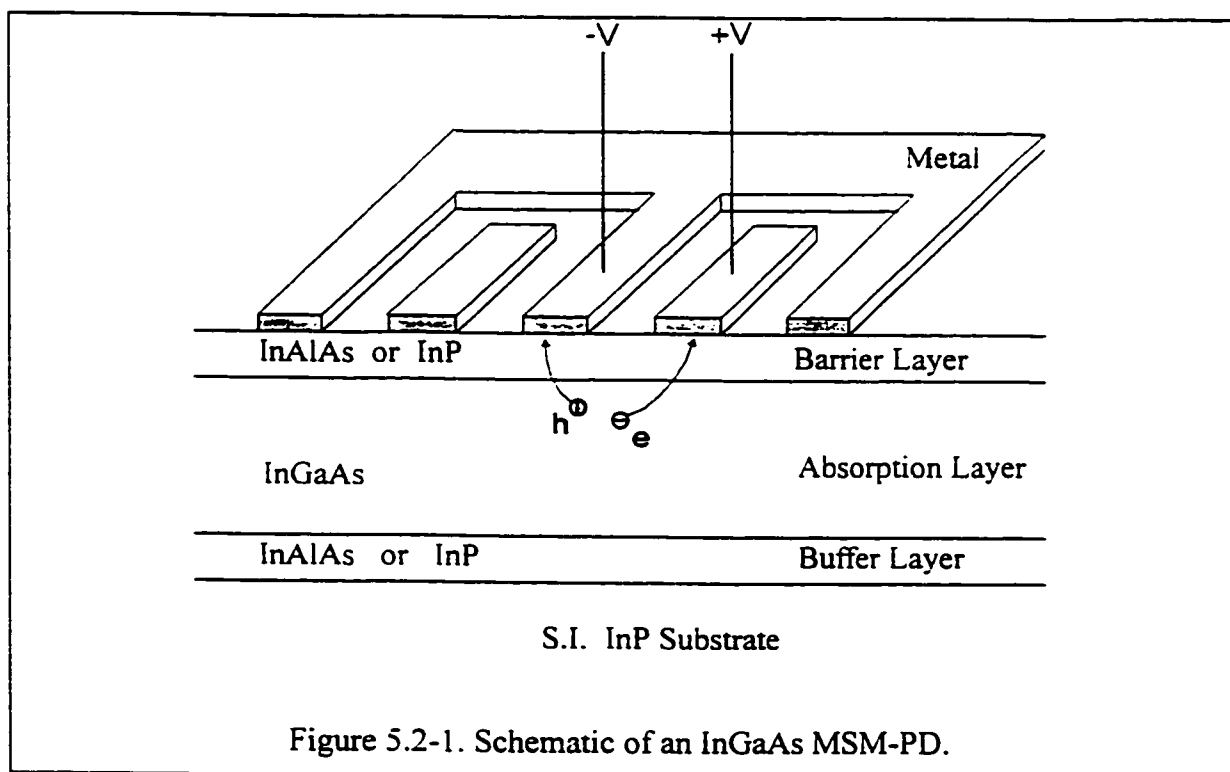


Figure 5.2-1. Schematic of an InGaAs MSM-PD.

separated by the electric field produced by the bias applied to the finger electrodes. Electrons will traverse to and be collected by the forward-biased electrode, while holes travel to the negatively biased electrode.

Although MSM-PDs can simply be considered as consisting of two back-to-back connected Schottky diodes, it is by no means a one-dimensional device. The carrier transport in a MSM-PD must be treated in a two-dimensional model. For a better understanding of the current transport in a MSM structure, the one-dimensional model developed by Sze [Sze, 1971] is briefly described, where some important parameters describing a MSM-PD were introduced. Two-dimensional models will be discussed in Section 5.2.2.

5.2.1 1D MSM-PD

A schematic of a one dimensional MSM-PD is shown in Figure 5.2-2. As is shown in Figure 5.2-2b, in thermal equilibrium, the built-in potential (band-bending) is given by

$$V_{Di} = \Phi_{ni} - \xi_i, \quad i = 1, 2 \quad (5.2-1)$$

where Φ_{ni} ($i = 1, 2$) is the electron Schottky barrier height at contacts 1 and 2, respectively. ξ_i is the energy difference between the conduction band minimum and the Fermi level in the semiconductor (in thermal equilibrium, the Fermi level in the metal is coincident with that in the semiconductor), and is given by

$$\xi = \frac{kT}{q} \ln\left(\frac{N_c}{N_d}\right) \quad (5.2 - 2)$$

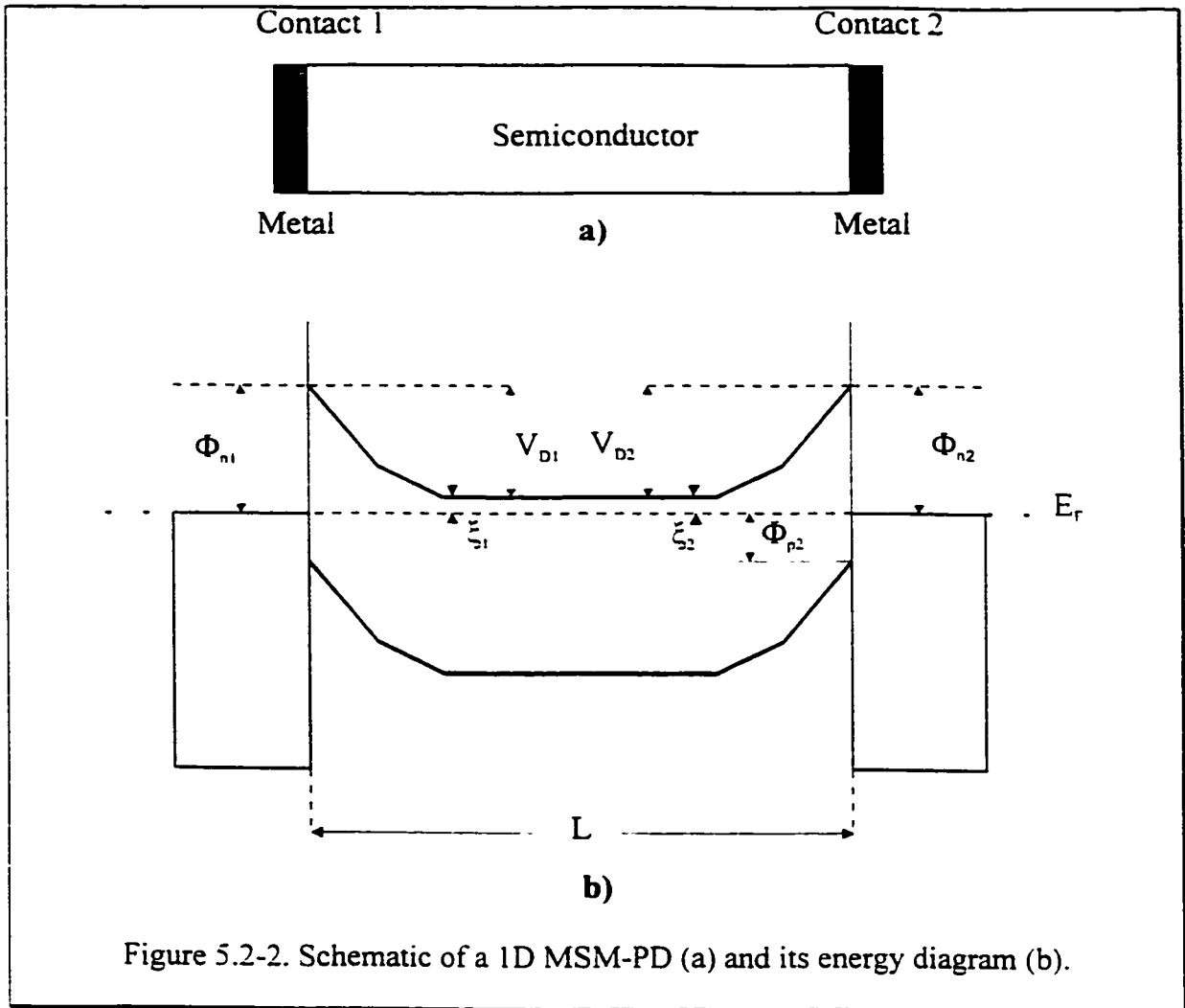


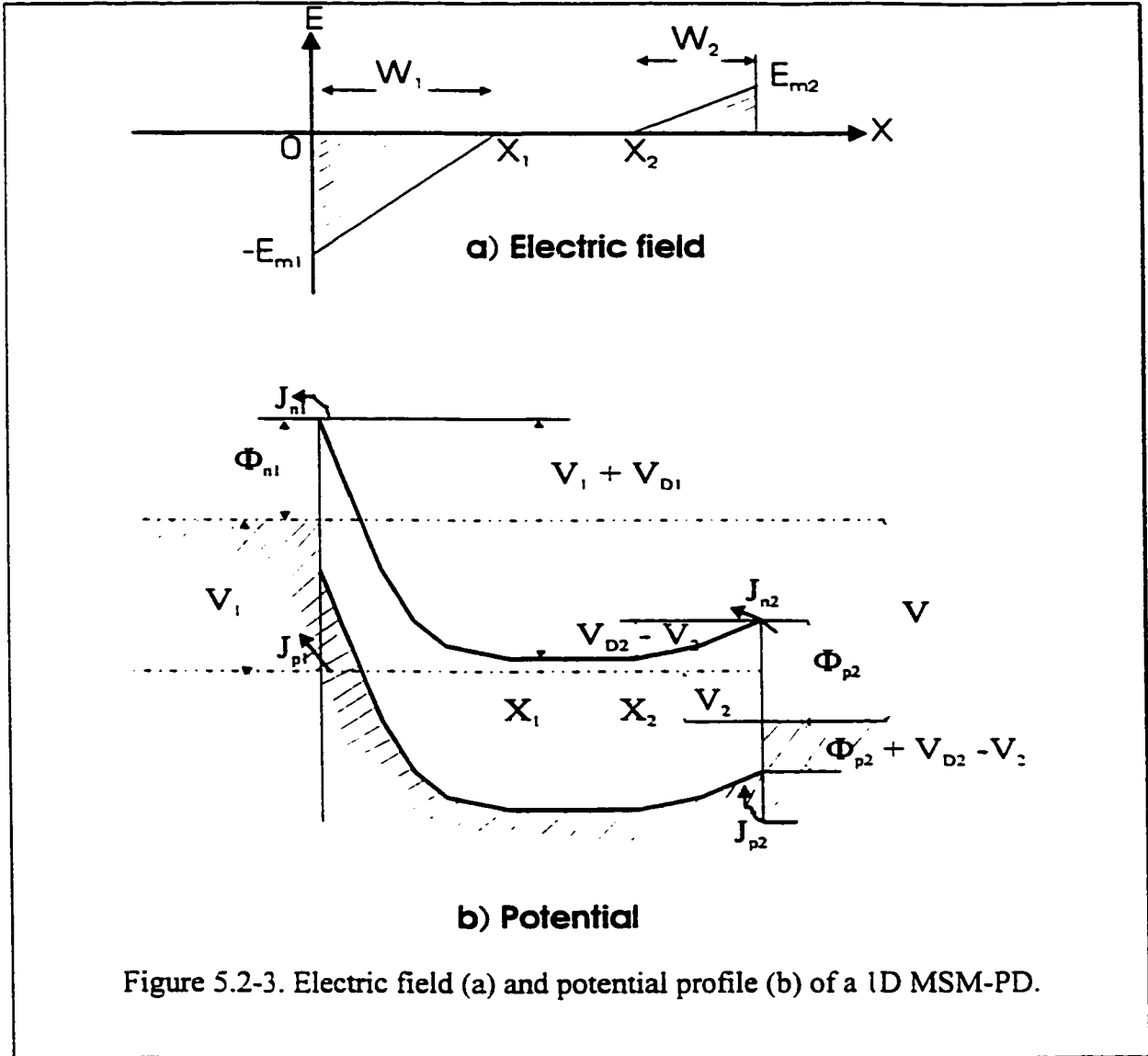
Figure 5.2-2. Schematic of a 1D MSM-PD (a) and its energy diagram (b).

where N_c is the density of states in the conduction band of the semiconductor, and N_d is the residual doping level.

When a voltage is applied to the 1D MSM-PD, it is shared between the two contacts, so that

$$V = V_1 + V_2 \quad (5.2 - 3)$$

Figure 5.2 - 3 shows the electric field (a) and the potential profile (b) of a 1D MSM-PD under bias V . As the bias increases, the depletion region (W_1) at the negatively biased contact increases, while the depletion region (W_2) at the forward biased contact decreases.



$$W_1 = \sqrt{\frac{2\epsilon_s}{qN_D}(V_1 + V_{D1})} \quad (5.2-4a)$$

$$W_2 = \sqrt{\frac{2\epsilon_s}{qN_D}(V_{D2} - V_2)} \quad (5.2-4b)$$

The overall depletion width, $W = W_1 + W_2$, increases with increasing bias voltage, V . The device is said to “reach through” when the depletion width W equals the separation

of the electrodes. L . This bias voltage is called "Reach-Through Voltage", V_{RT} , and is given by [Sze, 1971]

$$V_{RT} = \frac{qN_D}{2\epsilon_s} L^2 - (V_{D1} - V_{D2}) - L \left(\frac{2qN_D}{\epsilon_s} (V_{D2} - V_2) \right)^{1/2} \quad (5.2 - 5)$$

A further increase of the bias voltage will make $W_1 = L$, and $W_2 = 0$. At these conditions, the conduction band at contact 2 is flat. This voltage is called "Flat-band voltage", and is given by

$$V_{FB} = \frac{qN_D}{2\epsilon_s} L^2 - (V_{D1} - V_{D2}) \quad (5.2 - 6)$$

and

$$\Delta V_D = V_{D1} - V_{D2} \quad (5.2 - 6a)$$

The reverse electron current density J_{n1} for contact 1 is given by

$$J_{n1} = A_n^* \cdot T^2 \cdot e^{-\beta\Phi_{n1}} \cdot e^{\beta(\Delta\Phi_{n1} + \alpha_1 E_{m1})} \cdot (1 - e^{-\beta V_1}) \quad (5.2 - 7)$$

where A_n^* is the effective Richardson constant for electrons, T the temperature, $\beta = q/kT$, E_{m1} the maximum electric field (at $x=0$), α_1 the intrinsic barrier lowering coefficient, and $\Delta\Phi_{n1}$ the Schottky barrier lowering (in eV) given by

$$\Delta\Phi_{n1} = \sqrt{\frac{qE_{m1}}{4\pi\epsilon_s}} \quad (5.2 - 8)$$

with

$$E_{m1} = \sqrt{\frac{2qN_D}{\epsilon_s} (V_1 + V_{D1})} \quad (5.2 - 8a)$$

The forward electron current density J_{n2} at contact 2, is given by

$$J_{n2} = A_n^* \cdot T^2 \cdot e^{-\beta\Phi_{n2}} \cdot e^{\beta(\Delta\Phi_{n2} + \alpha_2 E_{m2})} \cdot (e^{\beta V_2} - 1) \quad (5.2 - 9)$$

where $\Delta\Phi_{n2}$ can be obtained from eq.(5.2 -8) with $(V_{D2} - V_2)$ replacing $(V_1 + V_{D1})$.

The hole current comes about because of the thermionic emission of holes from the forward-biased contact. The hole current density at contact 2 (forward biased) is given by

$$J_{p2} = A_p^* T^2 e^{-\beta(\Phi_{p2} + V_{D2} - V_2)} \quad (5.2 - 10)$$

The hole current at contact 1 is determined by the gradient of the hole concentration injected from contact 2, and the current density given by

$$J_{p1} = \frac{qD_p p_{n0} \tanh[(x_2 - x_1)L_p]}{L_p} (1 - e^{-\beta V_1}) + \frac{A_p^* T^2 e^{-\beta(\Phi_{p2} + V_{D2})}}{\cosh[(x_2 - x_1)/L_p]} (e^{\beta V_2} - 1) \quad (5.2 - 11)$$

The total current density can be expressed in different ways according to the bias voltage:

1) $V < V_{RT}$

At small bias voltages, $V < V_{RT}$, the total current density is given by

$$J = J_{n1} + J_{p1} = J_{ns} \cdot e^{\beta\Delta\Phi_{n1}} \cdot (1 - e^{-\beta V_1}) + \frac{qD_p p_{n0} \tanh[(x_2 - x_1)L_p]}{L_p} (1 - e^{-\beta V_1}) + \frac{A_p^* T^2 e^{-\beta(\Phi_{p2} + V_{D2})}}{\cosh[(x_2 - x_1)/L_p]} (e^{\beta V_2} - 1) \quad (5.2 - 12)$$

The hole current density injected from contact No.2, J_{p1} , is generally smaller than the electron current density, J_{n1} . So the total current density, $J \approx J_{n1}$.

2) $V_{RT} < V < V_{FB}$

At a bias voltage of V_{RT} , the device is completely depleted. but the current density is still small. With further increase in the bias voltage ($V_{RT} < V < V_{FB}$), the electron current density remains relatively small. However, the injected hole current density from the forward biased contact begins to increase rapidly as the hole barrier ($\Phi_{p2} + V_{D2} - V_2$) is lowered. In the bias range, $V_{RT} < V < V_{FB}$, the neutral region, $(x_2 - x_1)$, becomes zero, and the hole current density (eq.(5.2-11)) reduces to

$$J_{p1} = A_p^* T^2 e^{-\beta(\Phi_{p2} + V_{D2})} (e^{\beta V_2} - 1) \quad (5.2-13)$$

The total current density, $J = J_{n1} + J_{p1}$, is given by

$$J = J_{ns} \cdot e^{\beta \Delta \Phi_{n1}} + J_{ps} \left[e^{-\frac{\beta(V - V_{FB})^2}{4(V_{FB} + \Delta V_D)}} - e^{-\beta V_{D2}} \right] \quad (5.2 - 14)$$

3) $V > V_{FB}$

When the bias voltage reaches the flat-band voltage, $V = V_{FB}$, the hole current density reaches a critical value as the hole barrier approaches its limiting magnitude, Φ_{p2} .

The hole current density, at $V > V_{FB}$, is given by

$$J_{p1} = A_p^* T^2 e^{-\beta \Phi_{p2}} \quad (5.2-15)$$

Similar to the electron barrier at contact No.1, for bias voltages larger than V_{FB} , the barrier lowering effect must be taken into account. Then eq.(5.2-15) is expressed as

$$J_{p1} = A_p^* T^2 e^{-\beta\Phi_{p2}} e^{\beta\Delta\Phi_{p2}} \quad (5.2-15a)$$

where the hole barrier lowering is given by

$$\Delta\Phi_{p2} = \sqrt{\frac{qE_{m2}}{4\pi\epsilon_s}} = \sqrt{\frac{q(V - V_{FB})}{4\pi\epsilon_s L}} \quad (5.2 - 16)$$

Further increase in the bias voltage will only cause the current to increase slowly due to the field dependence of the Schottky barrier height. At this region, the total current is given by

$$J = J_{ns} e^{\beta\Delta\Phi_{n1}} + J_{ps} \quad (5.2 - 17)$$

where, $J_{ns} \equiv A_n^* T^2 e^{-\beta\Phi_{n1}}$, defined as electron saturation current density, and

$$J_{ps} \equiv A_p^* T^2 e^{-\beta\Phi_{p2}}, \text{ defined as hole saturation current density.}$$

At very high biases, the device breaks down causing the current to increase dramatically.

As described in eqs.(5.2-12, 14 and 17), the total current density in a MSM-PD consists of electron and hole currents. The hole current will be more significant at high biases, while for a Schottky diode, the current is mainly governed by majority carrier transport.

The capacitance of a 1D MSM-PD can be treated as that of two back-to-back connected Schottky diodes. For $V < V_{RT}$, $W < L$, the device is not completely depleted.

The capacitance (per unit area) is due to two capacitors in series

$$\frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_2} \quad (5.2 - 18)$$

where

$$C_1 \equiv \frac{\epsilon_s}{W_1} = \left[\frac{q\epsilon_s N_D}{2(V_1 + V_{D1})} \right]^{1/2} \quad (5.2 - 19a)$$

$$C_2 \equiv \frac{\epsilon_s}{W_2} = \left[\frac{q\epsilon_s N_D}{2(V_{D2} - V_2)} \right]^{1/2} \quad (5.2 - 19b)$$

When $V > V_{RT}$, the device is completely depleted, and the capacitance per unit area of a 1D MSM-PD is the same as that for a parallel plate capacitor:

$$C = \frac{\epsilon_s}{L} \quad (5.2 - 20)$$

This means that at high biases (after the device is completely depleted) the capacitance is saturated and independent of bias. The saturation capacitance is an important parameter for MSM photodetectors.

5.2.2 2D MSM-PD

For a real MSM device, the current transport is more complicated than that described in the previous section and a two-dimensional model must be used. Because of the complication of the structure, it is difficult to obtain an analytical description of the MSM-PDs. Instead numerical analysis and/or simulation is frequently used [Sano, 1990, Bottcher, 1992, Averin, 1996]. To describe the carrier behavior locally, Poisson's equation, the current-continuity equations, and a rate equation for charged traps must be solved. These equations are listed below, and the parameters are listed and explained in Tables 5.2-1 and 5.2-2.

Table 5.2 - 1. Symbols

Symbol		Unit	Symbol		Unit
n	electron concentration	cm ⁻³	q	electron charge	C
p	hole concentration	cm ⁻³	ε ₀	permittivity in vacuum	F/cm
n _i	intrinsic carrier concentration	cm ⁻³	ε _s	dielectric constant of semiconductor	
N _D	donor concentration	cm ⁻³	ψ	electric potential	V
N _A	acceptor concentration	cm ⁻³	E	electric field	V/cm
J _n	electron current density	A/cm ²	μ _n	electron mobility	cm ² /V-s
J _p	hole current density	A/cm ²	μ _p	hole mobility	cm ² /V-s
G _n	electron generation rate	cm ⁻³ s ⁻¹	D _n	electron diffusion coefficient	cm ² /s
G _p	hole generation rate	cm ⁻³ s ⁻¹	D _p	hole diffusion coefficient	cm ² /s
R _n	electron recombination rate	cm ⁻³ s ⁻¹	τ _n	electron life time	s
R _p	hole recombination rate	cm ⁻³ s ⁻¹	τ _p	hole life time	s

Table 5.2 - 2. Parameters and Their Meanings

Parameter	Physical Meaning	Unit
P ₀	optical power per unit surface area	W/cm ²
h	Planck's constant	J-s
ν	optical frequency	Hz
S	electrode spacing	μm
W	electrode width	μm
m	modulation index	
α	optical absorption coefficient	cm ⁻¹
ω	modulation angular frequency	Hz

$$\epsilon_0 \epsilon_s \nabla^2 \psi = -q(p - n + N_D - N_A) \quad (5.2 - 21)$$

$$-\frac{1}{q} \nabla J_n - G_n + R_n + \frac{\partial n}{\partial t} = 0 \quad (5.2 - 22)$$

$$\frac{1}{q} \nabla J_p - G_p + R_p + \frac{\partial p}{\partial t} = 0 \quad (5.2 - 23)$$

Electron and hole current densities are given by

$$J_n = q\mu_n n \nabla \psi + qD_n \nabla n \quad (5.2 - 24)$$

$$J_p = q\mu_p p \nabla \psi - qD_p \nabla p \quad (5.2 - 25)$$

The recombination rate is given by [Sze, 1981]

$$R = \frac{n \cdot p - n_i^2}{n\tau_p + p\tau_n} \quad (5.2 - 26)$$

Photogeneration rates G_n and G_p are given by

$$G_n = G_p = G(y) , \quad \text{between fingers} \quad (5.2 - 27)$$

$$= 0 , \quad \text{beneath fingers}$$

where $G(y)$ is given by

$$G(y) = \frac{P_o}{h\nu} \cdot \frac{D}{D+L} \cdot \alpha \cdot (1-r) e^{-\alpha y} (1 + m \sin \omega t) \quad (5.2 - 27a)$$

Electron and hole velocities depend on the local electric field and are given by [Sano, 1990]

$$v_n(E) = \frac{\mu_n E + v_{sn} (E / E_{th})^4}{1 + (E / E_{th})^4} \quad (5.2 - 28)$$

$$v_p(E) = \frac{\mu_p E}{1 + (\mu_p E / v_{sp})} \quad (5.2 - 29)$$

where E is the electric field in the MSM-PD. Electron and hole mobilities, μ_n and μ_p , are determined by several scattering processes. For simplicity, these mobilities are assumed to be given by [Baccarani, 1986]

$$\mu_n = \mu_{n1} + \frac{\mu_{n2}}{(1 + \Gamma / N_{rn})^{a_1}} \quad (5.2 - 30)$$

$$\mu_p = \mu_{p1} + \frac{\mu_{p2}}{(1 + \Gamma / N_{rp})^{a_2}} \quad (5.2 - 31)$$

where $\Gamma = N_D + N_A + n + p + N_T$.

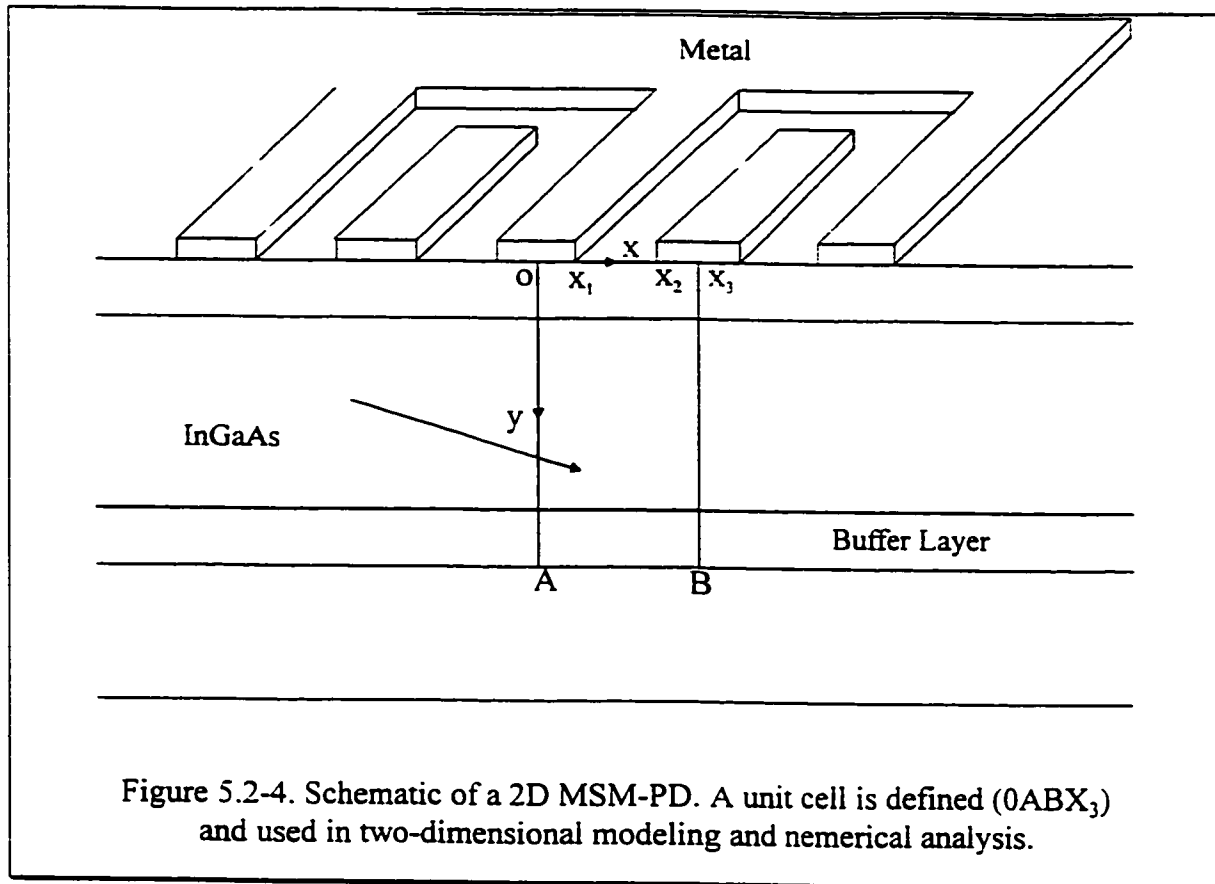
Table 5.2 - 3. Heterointerface Parameters

[Katz, 1992]

	InGaAs/InP	InGaAs/InAlAs
ΔE_g (eV)	0.60	0.72
ΔE_c (eV)	0.254	0.52
ΔE_v (eV)	0.346	0.20

If a barrier-enhancement layer is employed, the discontinuity at the InAlAs (or InP)/InGaAs interface must be considered. Some parameters of these heterojunctions are shown in Table 5.2 - 3.

Assuming the MSM-PD to be a symmetric device, one can analyze a unit cell as is shown in Figure 5.2 - 4. To solve Poisson's equation and the current-continuity equation in the analyzed region, one has to set the boundary conditions properly. Different approaches can be used to obtain an analytical description of the state of the MSM-PD



device at any given time, which includes the carrier densities at all points in the device and, hence, the electrode currents including electron conduction current, hole conduction current, and displacement current.

Sano [Sano, 1990, 1991] used a finite-difference time-domain (FDTD) technique to solve Poisson's equation. Ashour et al. [Ashour, 1995a, b] used the matrix-double-sweep (MDS) method to solve Poisson's equation, while the continuity equation was solved by the successive over relaxation (SOR) -Newton method. After obtaining the electric field distribution, the carrier distribution and therefore the electrode currents, one can deduce the responsivity and the impulse response of the MSM photodetector.

5.3 EXPERIMENTAL PROCEDURES

5.3.1 Device Fabrication

All device structures shown in Table 5.3-1 were grown by GS-MBE. First, an undoped InP buffer layer of 5000Å was grown on the SI InP substrate. The undoped InGaAs active layer, its thickness ranging from 0.5 to 2.0 μm was subsequently grown. Finally, a barrier enhancement layer with thickness of 200 - 500 Å was grown on top. The barrier layer is either InP or InP/In_{1-x}Ga_xP (x=0.15). The MBE samples investigated are listed in Table 5.3-1.

In some cases, the MBE grown samples were annealed by RTA at 600°C for 5 seconds before device fabrication. The details of the device fabrication are described below.

Table 5.3-1. MSM Samples Grown by GS-MBE

MBE Sample	Absorption Layer (μ) InGaAs	Barrier Layer InP (Å)	Metallization Scheme	Mask (#)
1	1	200	Au/Ni/Pt	1
2	1	200	Au/Ti/Pt	1
3	1	200	Au/Ti/Pt	2
4	1	300	Au/Ti/Pt	2
5	1	500	Au/Ti/Pt	2
6	2	500	Au/Ti/Pt	2
7	2	500	Au/Ni/Pt	2
8	2	400 *	Au/Ti/Pt	2

* 8 has another 100 Å of In_{1-x}Ga_xP (x=0.15) on top of InP.

I. Sample Cleaning

The MBE-grown samples were chemically cleaned sequentially by trichlorethylene, acetone and methanol at 90°C for 5 minutes each, repeated once in the above clean solutions for another 5 minutes, then rinsed in flowing de-ionized water for 5 minutes, and finally blown dry by N₂. In some cases, the sample was cleaned by an O₂ plasma for 5 to 10 minutes. The rf power was 150 watts and the chamber pressure was maintained at 2 mTorr. Then the samples underwent the regular chemical cleaning as described above.

The cleaned samples were dipped into HF:H₂O (1:10) for 10 to 20 seconds to remove the surface oxide. They then were immediately either loaded into the vacuum chamber for SiO₂ growth or were coated with spin-on-glass.

II. Dielectric Layer Growth

SiO₂, Si₃N₄, or spin-on-glass (SOG) was used as the insulation layer to isolate the contact pads and the semiconductor in device fabrication. A 1000Å layer of SiO₂ was deposited by plasma CVD (Technics Micro - PD 900 series) using SiH₄ and N₂O as gas sources. The base pressure was less than 10⁻⁴ mTorr. The SiH₄ and N₂O gas flows were 300 and 12 sccm, respectively. The total pressure was maintained at 750 mbar, and the rf power was set at 150 W. The substrate temperature was set at 300°C. At these conditions, the growth of 1000Å of SiO₂ took about 3 - 4 minutes. The thickness of SiO₂ was determined by ellipsometry (Ruldolph Research/AutoEL) or α - step (Tencor Instrument) measurement.

In case of using spin-on-glass (SOG #111, Allied-Signal), the SOG was spun on at a speed of 3000 RMP for 30 seconds to obtain a thickness of 1000Å. The samples with SOG were hardened by baking in an oven at 230°C for at least 36 hours before further processing.

III. Sample Patterning

Two different types of MSM-PDs were fabricated in our investigation. Their configurations are given in Tables 5.3-2 and 5.3-3. There are two different sizes of the active area in the first kind MSM-PDs, and both the finger width and the finger spacing are 2 μm. In the second type of MSM-PDs, the finger width and the finger spacing vary from 1 to 2.5 μm while the active areas range from 20×20 to 50×50 μm². The second type was designed such that it is compatible for high speed measurement by optic-electro sampling technique. The patterning processes are described below.

Photoresist (PR 1808, Shipley), at a thickness of about 1 μm, was put on the samples using a spinner at a speed of 5000 RMP for 30 seconds. Then they were “soft-baked” at 120°C for 90 seconds using a hot-plate. The first mask was used to open the SiO₂ window

Table 5.3-2. Configurations of Type #1 MSM-PDs

Electrode Structure	Large	Small
Finger width (μm)	2	2
Finger separation (μm)	2	2
Finger length (μm)	60	20
Active area (μm ²)	3,360	540

Table 5.3-3. Configurations of Type #2 MSM-PDs

MSM Device	Finger			Active Area	
	Width (μm)	Spacing (μm)	Length (μm)	($\mu\text{m} \times \mu\text{m}$)	(cm^2)
1.0 \times 1.0	1.0	1.0	20	20 \times 20	4.0×10^{-6}
1.0 \times 1.5	1.0	1.5	25	25 \times 25	6.25×10^{-6}
1.0 \times 2.0	1.0	2.0	30	30 \times 30	9.0×10^{-6}
1.5 \times 1.5	1.5	1.5	30	30 \times 30	9.00×10^{-6}
1.5 \times 2.0	1.5	2.0	35	35 \times 35	1.23×10^{-5}
2.0 \times 2.0	2.0	2.0	40	40 \times 40	1.6×10^{-5}
2.0 \times 2.5	2.0	2.5	50	50 \times 50	2.5×10^{-5}

for the active area. Exposure was done with an ultra-violet light source at a wavelength of 365 nm. The light intensity was set at 8.6 mW/cm^2 , and the exposure took about 4 to 6 seconds. The exposed samples were first dipped into a toluene solution for 5 to 7 minutes and immediately (kept away from water) "hard-baked" at 150°C for 90 seconds. The samples were developed using a solution consisting of Developer #351 (Shipley) and de-ionized water (1:5) at room temperature for 30 to 40 seconds. To check the quality of the developing, examination under microscopy was under-taken frequently. Then the SiO_2 or SOG in the opened area was removed by a chemical solution.

The second layer was patterned for the finger electrodes on the opened windows where SiO_2 was removed. This process is similar to the first layer except much patience was needed to align the mask and get a good pattern.

IV. Metallization

The electrode finger metals were deposited by electron beam evaporation. The evaporator has two UHV chambers (UHV Instruments Ltd.), one loading chamber (or preparation chamber) and one deposition chamber. The base pressure in both chambers was less than 1×10^{-8} Torr. Usually, the samples were loaded into the preparation chamber immediately after patterning. Subsequently, the samples were transferred to the deposition chamber for metallization. Before metals were being deposited on the patterned samples, the metal sources were degassed for a few minutes to remove the surface oxide. During the source degassing, the samples were shielded by a shutter.

Two most frequently used metallization schemes were Au/Ni/Pt and Au/Ti/Pt. First, 450-500Å of Pt was deposited, followed by 250 - 300 Å of Ni or Ti, then 1500 Å of Au. During deposition of metals, the stage (or sample holder) on which the samples were mounted was rotating to obtain uniform metal-semiconductor contacts. The parameters for Au, Ni, Ti, and Pt deposition are given in Table 5.3-4. W, WN and TiN were

Table 5.3-4. Parameters of Metallization

Metal	Filament Current (A)	Deposition Rate (Å/s)	Time	Thickness (Å)
Pt	1.53 - 1.56	2.5 - 3.0	2'30'' - 3'10''	500 Å
Ni	1.32 - 1.35	2.0 - 2.5	2'10'' - 2'30''	300 Å
Ti	1.31 - 1.33	2.0 - 2.5	2'10'' - 2'30''	300 Å
Au	1.38 - 1.41	4.0 - 5.0	5'30'' - 6'30''	1500 Å
Al	1.50 - 1.53	3.5 - 4.0	5'30'' - 6'00''	1000 Å
Ge	1.28 - 1.32	2.5 - 3.0	1'30'' - 2'00''	250 Å
W	1.56 - 1.60	3.0 - 3.5	5'30'' - 6'30''	1000 Å

deposited by rf sputtering [Pang, 1992, 1994], or by ECR-CVD [Boumerzoug, Pang et al. 1994] either on the whole sample surface or on patterned areas. W was also deposited by electron beam evaporation. In the latter case, a thin Ti layer was evaporated first on the sample to improve the sticking of W on InP.

V. Etching

The SiO_2 was removed to open the active area windows. The chemical solution used to etch SiO_2 was HF:HF buffer (1:10). This was done at room temperature. For 1000Å SiO_2 , the etching took about 35 - 40 seconds. The HF buffer solution was prepared by HF and ammonia (40% wt HF). Usually, the etchant was prepared at least 20 minutes before etching was taking place. This made the etching rate more uniform and allowed better control.

SiO_2 can also be selectively etched by reactive-ion-etching (RIE) (Technics, Micro - RIE, series 800) using photoresist (1µm) or a metal (such as Al, 2000Å) as mask. The etchant used is CF_4 , set to a flow of 20 sccm. The total pressure in the chamber was maintained at 400 mbar. The rf power was 100 W. For 1000 Å of SiO_2 , the etching time is about 10 minutes. SOG and Si_3N_4 can be etched by ways similar to those for SiO_2 .

For mesa etchdown isolation, the InP and InGaAs in the areas between contact pads and between devices were etched away. InP was etched by a chemical solution of $\text{HCl}:\text{H}_3\text{PO}_4$ (1:1) at room temperature. It took about 10 seconds to etch 200 Å of InP. The InGaAs was etched by a mixed solution of citric acid and H_2O_2 (1:8). For 1 µm of InGaAs, the etching time was about 360 seconds.

When W and TiN were used as electrode finger metals, device fabrication was completed either by etching or by lift-off. In the case of etching, W was etched by RIE using a CF₄ plasma, and TiN was etched by a chemical solution consisting of equal parts of ammonium hydroxide and 30% hydrogen peroxide at 40°C.

VI. Surface Passivation

Passivation of InGaAs MSM-PDs by sulfide solution was conducted. The preparation of the sulfide solution was described in Chapter 4. For MSM-PD passivation, we performed different procedures which are listed below:

- 1) The whole sample surface was sulfide passivated after sample cleaning;
- 2) The active areas where SiO₂ was removed were passivated;
- 3) Only the areas beneath the finger electrodes were passivated. This was done after fingers were patterned;
- 4) Device passivation was performed after lift-off.

VII. Thermal Annealing

Thermal annealing was performed using a rapid thermal annealer (RTA) (AG Associates, Heatpulse 210, or Mini-Pulse). Some MBE grown device structures were annealed at 600°C for 5 seconds before device fabrication, while some MSM photodetectors using Au based metallization schemes as electrode fingers were annealed at 300°C, 400°C, and 500°C for 10 seconds. For devices with W, WN, TiN, and WTiN as

electrode metals, the annealing temperature could be raised to 800°C for 10 to 30 seconds.

5.3.2 Characterization

I. I - V and C-V Characteristics

The I - V characterization was done with a semiconductor analyzer (HP4145B) controlled by a computer. For low temperature characterization, the sample was mounted on a thermal conducting stage cooled by a Joule-Thomson refrigerator (see description in Chapter 3). The available temperature range is 77K to 400 K. This I-V measurement can provide information about the dark current, the flat band voltage, and the breakdown voltage of MSM photodetectors. Similar to the I - V measurements, C-V characterization was done at both room temperature and at low temperatures with a capacitance-conductance analyzer (LCZ meter - HP 4277A) at a frequency of 1 MHz.

II. Photocurrent Measurements

Unlike the dark current measurement by I-V characterization, the DC photoresponse measurement was performed with light illumination of the active area of the MSM photodetectors. The experimental set-up is shown in Figure 5.3-1. The light source is a laser diode (SeaStar Optics) with specifications listed in Table 5.3-5. The calibration of the laser diode's output is given in Table 5.3-6. The laser diode has a built-in pigtail fiber through which the light can be directed to the active area of the MSM photodetectors. The

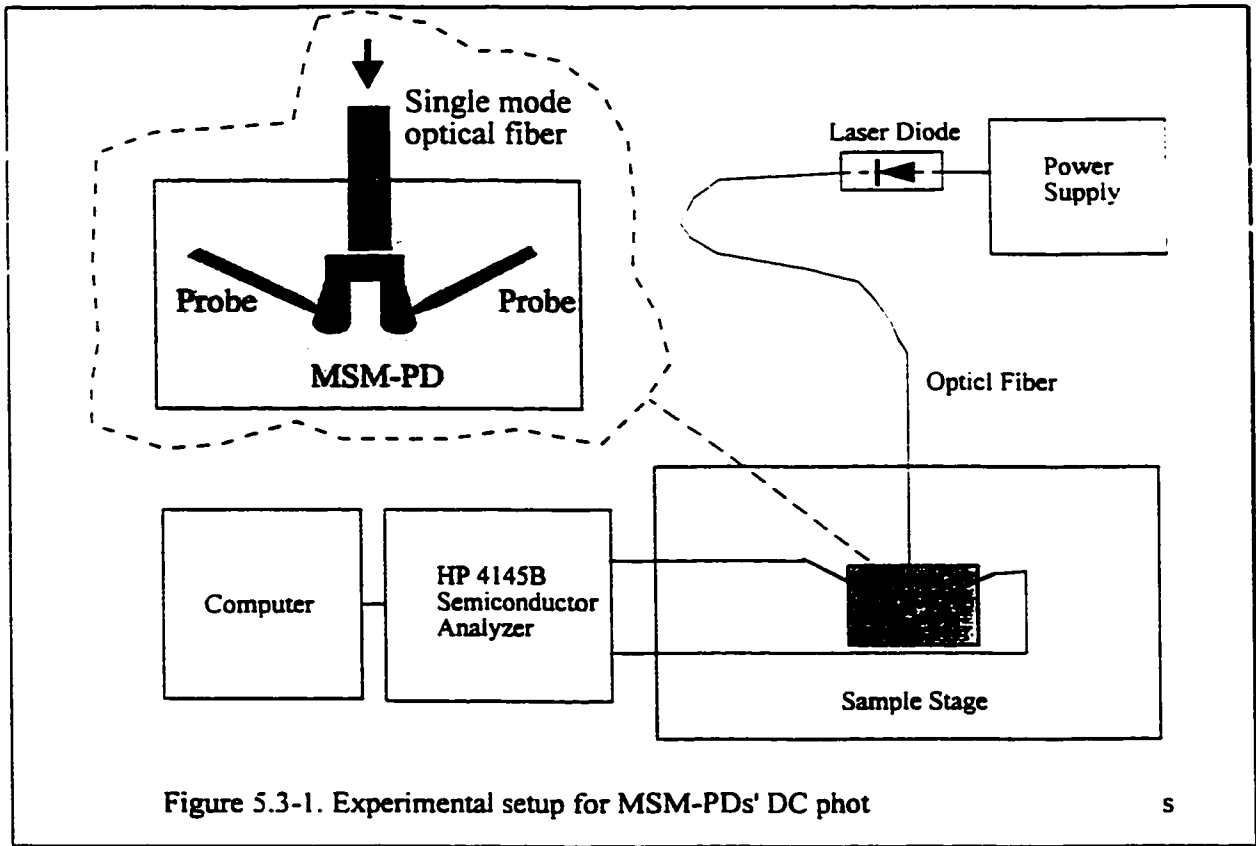


Figure 5.3-1. Experimental setup for MSM-PDs' DC phot

5

Table 5.3-5
Specification of Laser Diode

Wavelength (Å)	1310
Manufacturer	SeaStar Optics Inc.
Model	PT-450L-1310
Series No [*]	Sp4024
I_{th} (mA)	8.8
I_{max} (mA)	65.9
P_{max} (mW)	2.606 ± 0.005

Table 5.3-6
Calibration of Laser Diode
($\lambda = 1.31 \mu\text{m}$)

Current (mA)	Optical Power (± 0.005 mW)
10	0.074
15	0.321
20	0.577
25	0.825
30	1.077
35	1.315
40	1.553
45	1.792
50	2.036
55	2.290
60	2.523

core of the single mode fiber has a radius of 5 μm while the diameter of the cladding layer is 50 μm . When taking the photoresponse measurements, the fiber head must be carefully positioned to make sure that the entire light beam was incident onto the active area. This can be done by monitoring the photoresponse to be a maximum.

III. Temporal Response Measurements

The temporal response of the MSM-PDs was measured using an optic - electro sampling system (OES) as is shown in Figure 5.3-2a and b (courtesy S. Pang). The MSM-PD was biased at a given voltage. When light pulses illuminate the active area of the MSM-PDs, an electric field in the active area (between oppositely biased electrode fingers) is generated by the photogenerated carriers. This electric field can be detected by

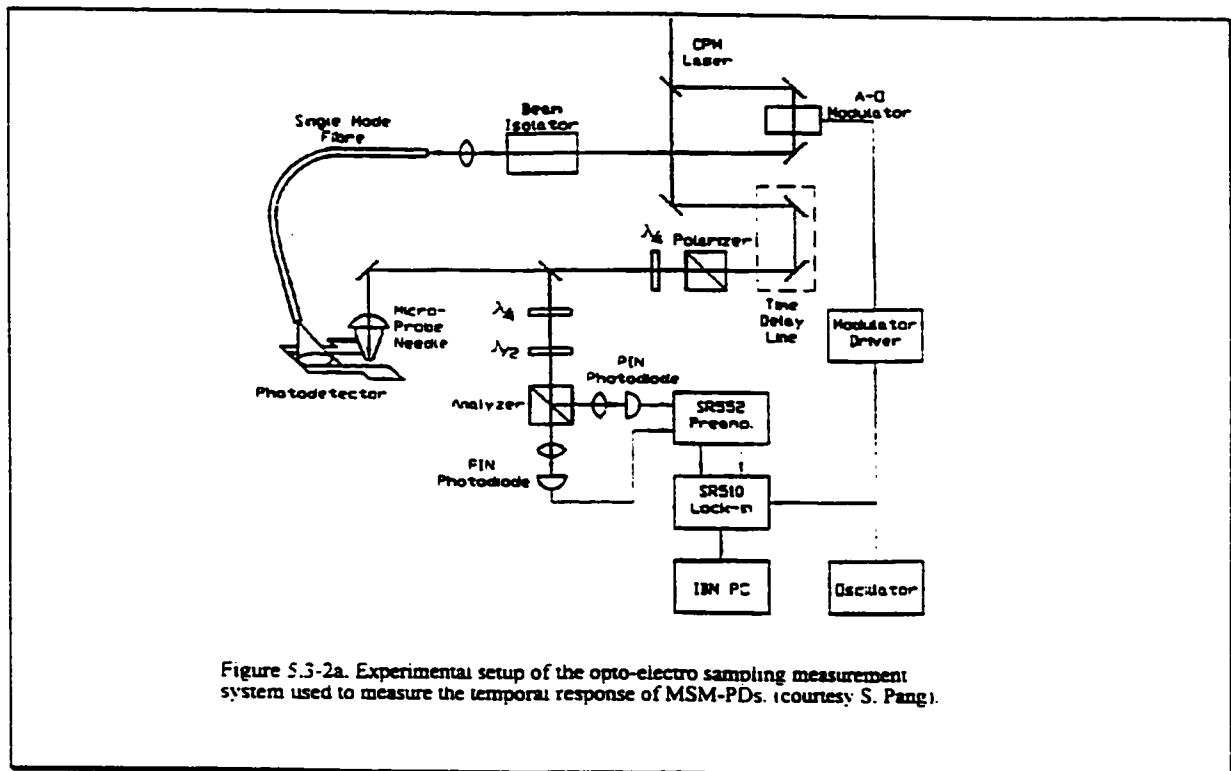
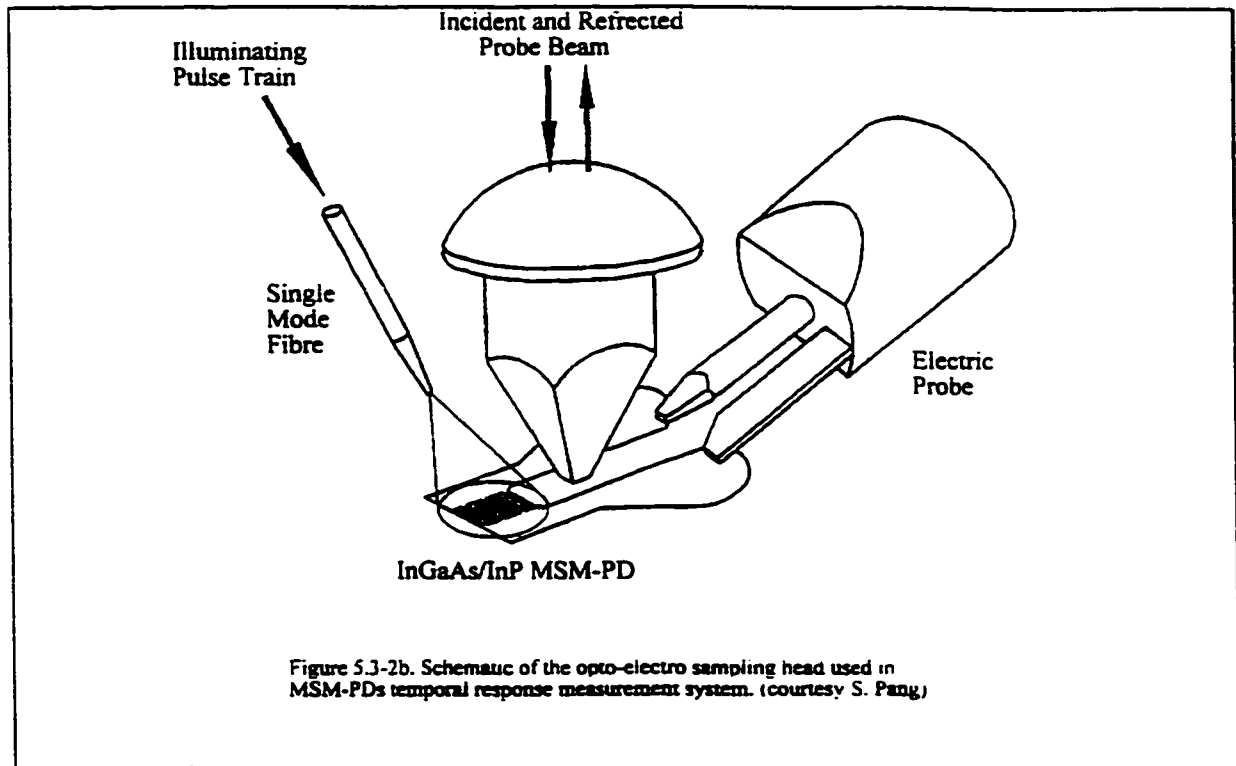


Figure 5.3-2a. Experimental setup of the opto-electro sampling measurement system used to measure the temporal response of MSM-PDs. (courtesy S. Pang).



a crystal head positioned close to the MSM-PD active area.

The system uses a CW Argon laser ($\lambda = 488 \text{ nm}$) to pump a ring-cavity dye laser with pulsed output. The pulse width from the dye laser was reduced to 100 ps by a mode-locking technique. The output laser beam was split into two beams. One was used to be the light source illuminating the active area of the MSM photodetector, while the other was used as a reference to activate the crystal head to detect the electric field in the active area generated by the pulse signal.

The temporal response obtained by OES is the intrinsic response from the MSM-PDs. A real time frequency response measurement was performed using a high-speed optical measurement system (courtesy CRC) and the 3 dB cut-off frequency (unit current gain cut-off frequency) can be obtained by performing Fourier transform of the temporal response data.

5.4 RESULTS AND DISCUSSION

5.4.1 Metallization Schemes

At the very beginning in our MSM-PD's investigation, we systematically studied the metallization schemes for the fabrication of MSM-PDs [Pang et al. 1995] as listed in Table 5.4-1. Electron-beam evaporation and rf sputtering were employed to deposit the electrode metals. Au-based metallization schemes are not stable at elevated temperatures (>400°C). The I-V characteristic of such contacts on InP becomes nonlinear or ohmic after annealing at temperatures higher than about 450°C - 500°C. Au/Ti/Pt has the highest

Table 5.4-1. Metallization Schemes of InP/InGaAs MSM-PDs

Metal	Deposition	I - V	ϕ	RTA
Au	e-Beam		0.41	>500°C . ohmic
Au/Al	e - beam		0.38	
Au/Ti	e - beam	nonlinear	/	
Au/Pt	e - beam	Schottky	0.43	
Au/Ti/Pt	e - beam	Schottky	0.47	
Au/Pt/Ti	e - beam	Schottky	0.39	
Au/Ni/Pt	e - beam	Schottky	0.44	< 400°C
Au/Pt/Ti/Pt	e - beam	Schottky	0.48	
Au/W/Pt	e - beam	Schottky	0.43	-> 450°C
Au/W/Ti	e - beam	Schottky	0.48	
W/Ti	e - beam	Schottky	0.46	-> 600°C
W	sputter	ohmic		
WN	sputter	nonlinear		-> 850°C
TiN	sputter	nonlinear		>500°C ohmic

Schottky barrier, while Au/Ni/Pt is the best contact in terms of uniformity. W, WN, and TiN were sputtered on InP hoping to obtain good metallization that is stable at high temperatures. Unfortunately, the contact is not a good Schottky contact probably due to sputtering damage of the InP surface. W can be evaporated but it does not stick very well on InP. So a thin Ti layer was evaporated on InP before W evaporation. The thermal stability of W/Ti is better than that of Au-based metallization schemes. In the following investigation, the metallization scheme is Au/Ni/Pt, due to its good contact and relatively high Schottky barrier, unless otherwise specified.

We used SiO₂, deposited by plasma CVD, as the insulating layer to isolate the electrode contact pads and the semiconductor. Unfortunately, the I-V characteristic of MSMs with SiO₂ shows ohmic behavior rather than Schottky. The possible reasons are that the semiconductor was doped by Si when the metal film was being grown at a temperature of about 300°C or that the plasma process might produce surface damage to the semiconductor (InP).

The results of InGaAs (1μm) MSM-PD with 500Å of InP as the barrier enhancement layer is given in Table 5.4-2. The MSM-PD using Au/Ni/Pt as electrode has a dark current of 700nA at 8V. This current is reduced to 300nA after annealing at 300°C for 10 seconds. MSMs with sputtered TiN as electrodes have the smallest dark current (30 nA at 6V), but the responsivity under light illumination is significantly smaller than those using Au-based contacts as electrodes.

Table 5.4-2. Results of InP/InGaAs MSM-PDs

Structure No [#]	SiO ₂ Y/N	Electrode Metals	I _D	V _s (V)	V _B (V)
748 [#]	no	Au/Ni/Pt	0.2 μA, at 2V	0.2	4.0
	yes	Au/Ni/Pt	Ohmic		
747 [#]	yes	Au/Ni/Pt	Ohmic		
760 [#]	no	Au/Ni/Pt	700nA, at 8V	0.6	10
		RTA@300°C, 10s	300nA, at 8V	0.6	10
		> 350°C, 10s	ohmic		
	no	Au/Ni/Ti	10μA, at 10V	1.2	18
	no	Au/W/Pt	15μA, at 8V	2.0	10
	no	TiN (1000Å)	30nA, at 6V	2.0	10
		RTA@350°C, 10s	12nA, at 6V		
		@400°C, 10s	18nA, at 6V		

A SEM micrograph of an InGaAs MSM-PD is shown in Figure 5.4-1a. A portion of the device, the active area, is shown in Figure 5.4-1b. The Schottky contact layer in this device is InP with a thickness of 500Å. The finger width and the spacing of the MSM-PD are 2μm and 2 μm, respectively.

In the following sections, we will discuss the experimental results of the InGaAs MSM-PDs with an absorption layer of 2 μm (InGaAs). The barrier enhancement layer is InP (500Å) or InP(400Å)/In_{1-x}Ga_xP (x = 0.15, 100Å), and a new mask (Mask #2) was used. In §5.4.2, we will discuss the capacitance and flat-band voltage of MSM-PDs.

Dark current will be addressed in §5.4.3, while §5.4.4 will deal with the photoresponse and §5.4.5 discusses the quantum efficiency. The temporal response measurements were done with assistance from S. Pang (McMaster University) and the Communication Research Center (CRC) in Ottawa. Results of the temporal response are not included in this thesis.

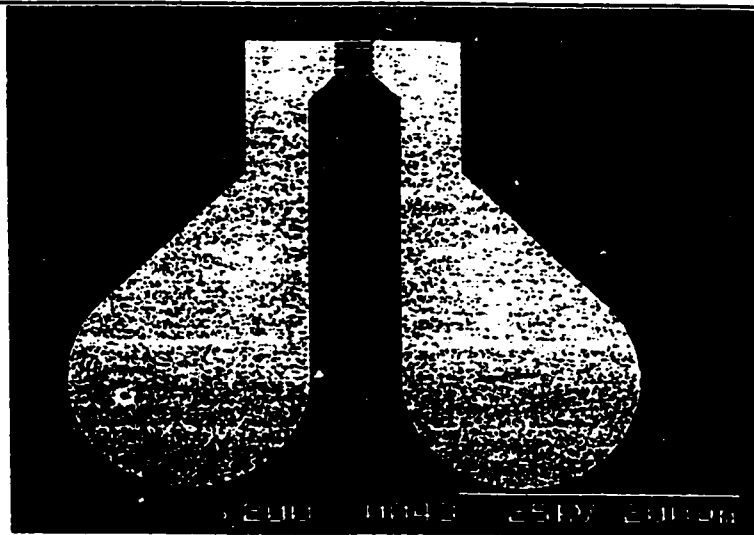


Figure 5.4-1a. SEM micrograph of a 2x2 InGaAs MSM-PD.

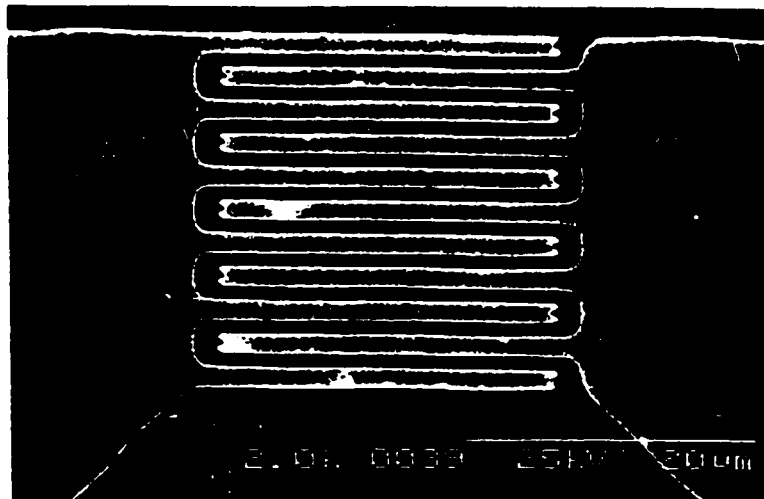


Figure 5.4-1b. SEM micrograph of the active area of a 2x2 InGaAs MSM-PD.

5.4.2. Capacitance

I. Depletion of the Device

Figure 5.4-2 shows the capacitance of an InGaAs MSM with finger width of $2\mu\text{m}$ and finger spacing of $2\mu\text{m}$ as a function of bias voltage. In this device, 500\AA InP was grown on top as the barrier enhancement layer. As is shown in the figure, the zero-bias capacitance is about 3 pF while the saturation capacitance (when the device is fully depleted) is about 0.2 pF . For our InP/InGaAs MSM-PDs, the device is fully depleted at a bias of 2 to 2.5V , corresponding to the flat band voltage. According to Sze [Sze, et al., 1971], the flat band voltage of a simplified one-dimensional MSM can be given as

$$V_{fb} = (qN_d/2\epsilon)L^2 \quad (5.4 - 1)$$

where L is the electrode spacing (actually, it is the thickness of the semiconductor in a 1D

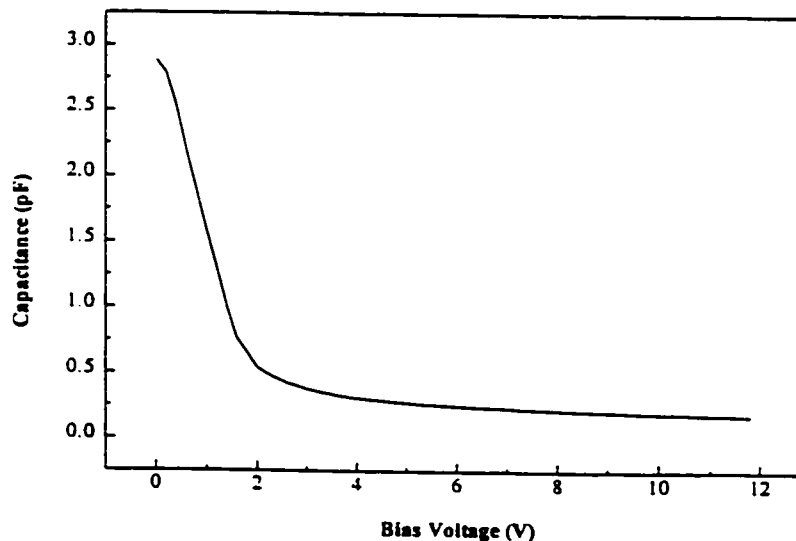


Figure 5.4-2. Capacitance of a typical InGaAs MSM-PD (2×2). The barrier layer is InP with a thickness of 500\AA .

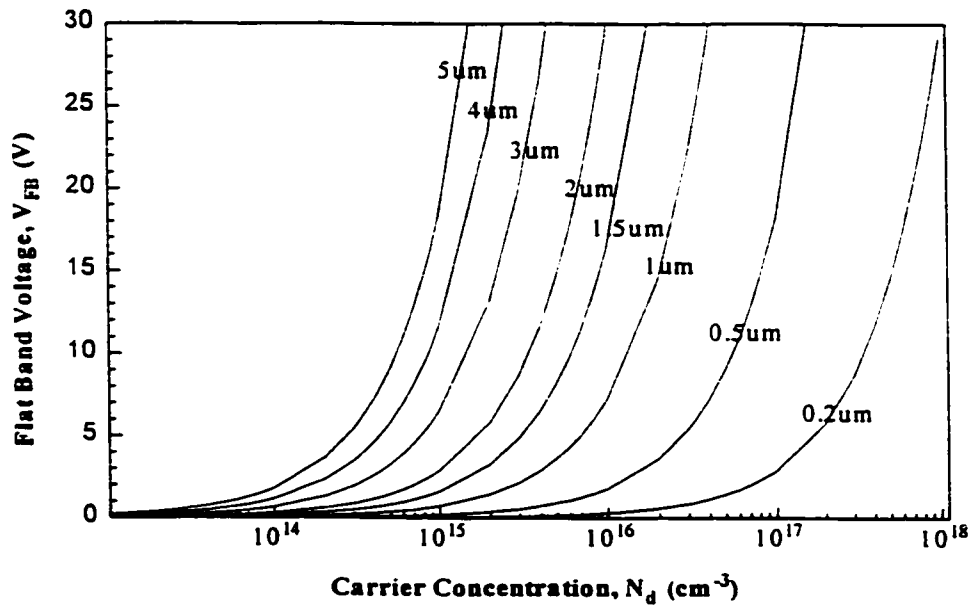


Figure 5.4-3. Calculated flat-band voltage of a one dimensional InGaAs MSM-PD as a function of carrier concentration for different thicknesses of the absorption layer.

MSM-PD) and N_d is the residual doping level. Figure 5.4-3 shows the calculated flat band voltage from eq.(1) as a function of the residual carrier concentration for different thicknesses of the InGaAs absorption layer. For $N_d = 1 \times 10^{15} \text{ cm}^{-3}$, and $L = 2 \mu\text{m}$. V_{fb} calculated from eq.(1) is about 2.5 V - i.e. very close to that observed.

According to Lim [Lim, et al., 1968] and Soole [Soole et al., 1990], for an undoped and infinitely thick semiconductor, the capacitance is given by

$$C = \frac{K(\kappa)}{K(\kappa')} \cdot \epsilon_0 (1 + \epsilon_r) \cdot \frac{S}{d} \quad (5.4-2)$$

where ϵ_r is the relative dielectric constant of the semiconductor, S is the interdigitated area, d is the finger period, and $K(\kappa)$ is the complete elliptic integral of the first kind.

$$K(\kappa) = \int_0^{\pi/2} \frac{1}{\sqrt{1 - \kappa^2 \sin^2 \phi}} d\phi \quad (5.4-3)$$

with

$$\kappa = \tan^2 \left[\frac{\pi W}{4d} \right] \quad (5.4-3)$$

where w is the finger width, and

$$\kappa' = \sqrt{1 - \kappa^2} \quad (5.4-4)$$

For a MSM-PD with active area = $50 \times 50 \mu\text{m}^2$, finger width $2 \mu\text{m}$ and finger spacing $2 \mu\text{m}$, the capacitance is about 50 fF. Table 5.4-3 shows the calculated capacitance of InGaAs MSM-PDs for different finger configurations.

Table 5.4-3. Calculated Capacitance of InGaAs MSM-PDs

MSM -PD	Active Area (μm^2)	Capacitance (fF)	Active Area (μm^2)	Capacitance (fF)
1.0×1.0	20×20	16.7	50×50	104
1.0×1.5	25×25	12.7	50×50	50.9
1.0×2.0	30×30	10.4	50×50	28.8
1.5×1.5	30×30	25.0	50×50	69.6
1.5×2.0	35×35	20.7	50×50	42.3
2.0×2.0	40×40	33.4	50×50	52.2
2.0×2.5	50×50	35.6	50×50	35.6

For our MSM-PDs, InGaAs has a residual doping concentration of $1 \times 10^{15} \text{ cm}^{-3}$, and 2 - 3 volts bias is required to deplete the device. Once the device is depleted, the capacitance is given by eq(2). The depletion of a two dimensional MSM-PD, as in our case, is different from a one-dimensional MSM-PD [Sze, et al., 1971]. The capacitance continues to deplete regions further from the surface, under the electrodes, and beneath the absorption layer, while in a one-dimensional MSM-PD, once it is depleted, the capacitance stays constant as the bias is increased.

Apparently, the saturation capacitance is dependent on the thickness of the absorption layer (including the barrier layer) as well as the geometry of the electrodes. Hieronymi [Hieronymi, et al., 1994] reported that the saturation values of the capacitance for circular InGaAs MSM-PDs (circular pattern, electrode width $0.5 \mu\text{m}$, spacing $5 \mu\text{m}$, diameter of $350 \mu\text{m}$) with InGaAs thicknesses of $0.7 \mu\text{m}$ and $1.2 \mu\text{m}$ are 0.75 and 0.8 pF, respectively. The flat-band voltages were 0.5 and 1.3 V, respectively for 0.7 and $1.2 \mu\text{m}$ InGaAs. The device capacitance per unit area was very small, 7.8 pF/mm^2 , a factor 10 - 20 smaller than those of commercial PIN photodiodes. In our case, 0.2 pF saturation capacitance of InGaAs MSM-PDs with an active area of $50 \times 50 \mu\text{m}^2$, corresponding to capacitance per unit area of 8 pF/mm^2 , was obtained.

II. Thermal Annealing

Although the saturation capacitance is determined by the thickness of the semiconductor and the electrode geometry, the zero-bias capacitance is affected by defects and traps in the semiconductor and by surface and interface states. Figure 5.4-4

shows the capacitance of MSM-PDs processed in different ways. Thermal annealing of the MBE grown wafer at 600°C for 5 seconds before fabricating the MSM devices reduced the capacitance at low biases. This is attributed to the reduction of the defect and trap density in the MBE grown structure. Further dipping the annealed sample into HF:H₂O (1:10) for 20 seconds only has a slight influence on the capacitance of the device, while mesa-etch down between the contact pads results in a significant reduction of the capacitance at low biases. This is due to the reduction in the conduction area by the mesa-etchdown isolation. It will be seen in next section that the mesa-etchdown can reduce the dark current significantly, too. In practice, either mesa-etchdown or deposition of a dielectric thin film, such as SiO₂ or Si₃N₄, are employed to isolate the contact pads. While the zero-bias capacitance and the capacitance at low biases are affected by the above processing, the saturation capacitance remains unchanged, and the voltage needed to deplete the device (V_{fb}) is almost the same.

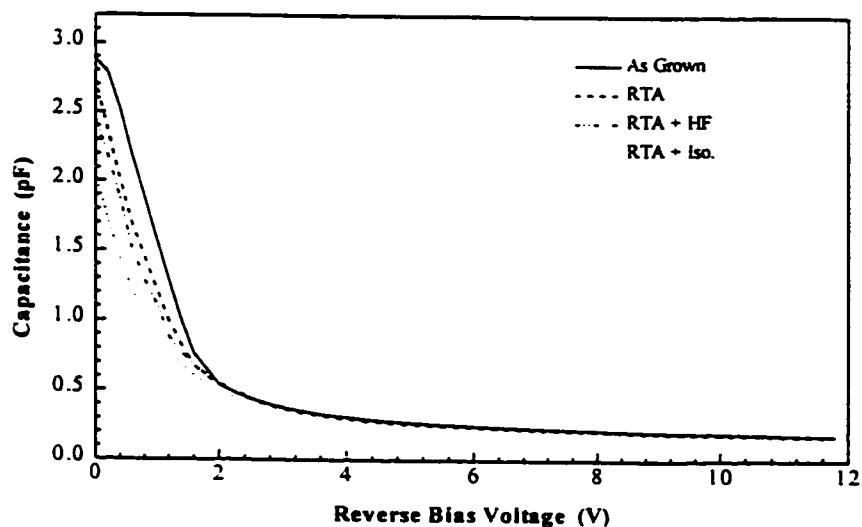


Figure 5.4-4. Capacitance of InGaAs MSM-PDs (2x2) processed in different ways.

III. Sulfide Passivation

Dipping the sample into HF can remove the native surface oxide, but it is unlikely to reduce the density of surface states of the sample. Sulfide passivation of the sample's surface can reduce the surface and interface states and the traps in the bulk semiconductor [Landheer, et al., 1994] in InP. We conducted sulfide passivation of the InP/InGaAs MSM using the method described in §5.3. Figure 5.4-5 shows the capacitance of the sulfide passivated MSM together with that of the untreated device. At low biases (below the flat band voltage), the sulfide passivated device has much lower capacitance, 0.93 pF compared to 1.98 pF for the unpassivated MSM at zero bias. The unpassivated device shows a strong dependence on bias, which indicates that there are many interface states between the contact metal and the semiconductor. Besides the reduction of the capacitance at low biases, the saturation capacitance of the passivated device is slightly

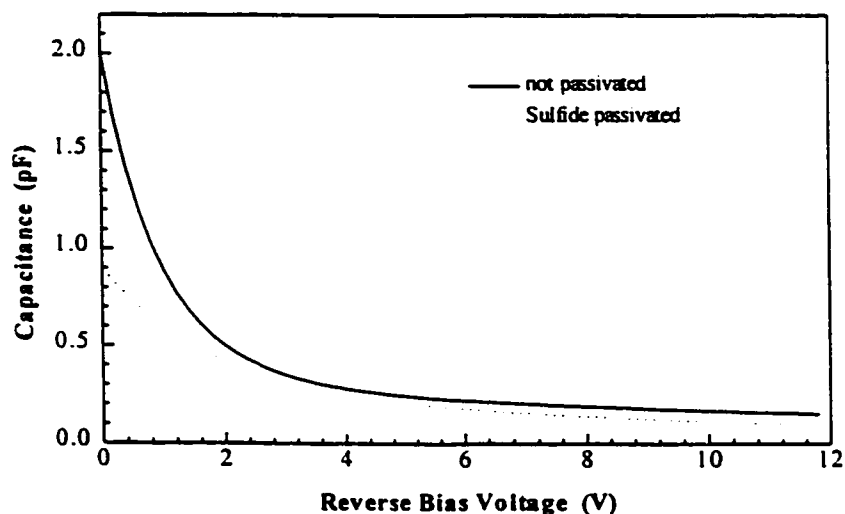


Figure 5.4-5. Capacitance of InGaAs MSM-PDs (2x2) with and without sulfur passivation

reduced from about 180 - 200 fF to 120 - 150 fF. Han [Han. et al., 1994] attributed the lower saturation capacitance in passivated devices to the existence of a thin layer of InP_xS_y between the contact metal and the semiconductor. Otherwise, the capacitance of both types of MSM should be the same in the fully depleted region. An atomic layer of sulfur on the passivated InP surface is commonly observed [Sugiyama et. al., 1995; Y. Fukuda et. al., 1994; Tao, et al., 1992; Gao et al., 1995]. It was found that $(\text{NH}_4)_2\text{S}$ treated GaAs (001) and InP (001) surfaces are completely terminated by S-Ga and S-In bonds, respectively. Auger electron spectra taken from the sulfide passivated InP do indicate the existence of sulfur atoms on the surface as is shown in Figure 5.4-6a. After sputtering the surface for 30 seconds, the sulfur signal can no longer be detected (Figure 5.4-6b). It was suggested that the In-S bonds formed on the sulfide passivated InP surface are very stable. Desorption of group V-elements, such as As and P atoms, is hindered by sulfide passivation [Sugiyama et. al., 1995], and this is responsible for the improvement of the reliability of the sulfide passivated device. It was also reported that $(\text{NH}_4)_2\text{S}_x$ significantly reduces the surface roughness of the as-received samples and these sulfide treated surfaces were also found to be free of oxide [Gao et. al., 1995].

We conducted photoluminescence (PL) measurements of passivated InP samples together with the unpassivated samples. The PL signal from the sulfide-passivated sample is stronger than that from unpassivated InP at room temperature [Figure 5.4-7]. Similar observations were made for GaAs.

Other passivation techniques were employed to improve the performance of MSM-PDs, such as the deposition of SiO_2 [P.Ambree. 1995, Lee, 1988], Si_3N_4 [Lee. et al, 1988.

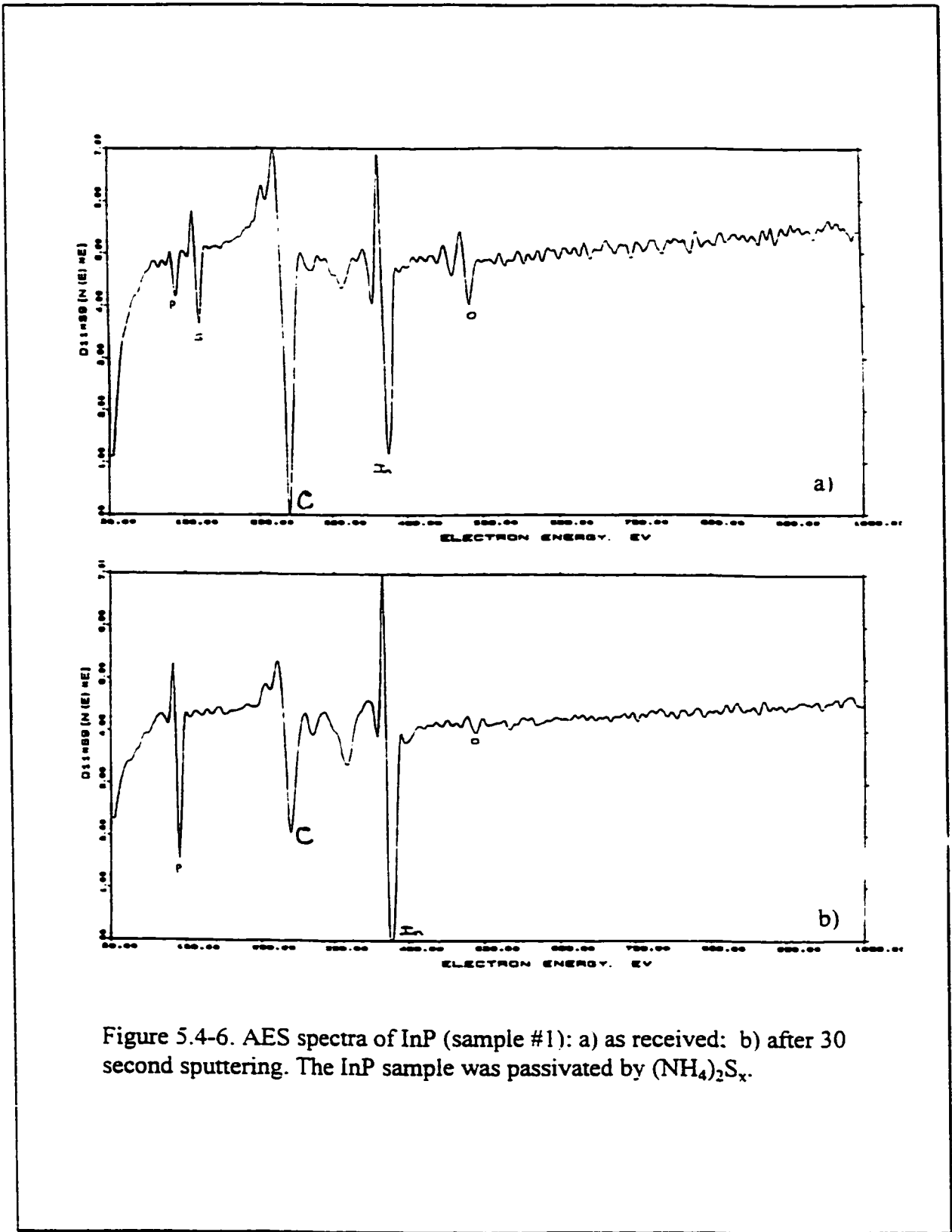
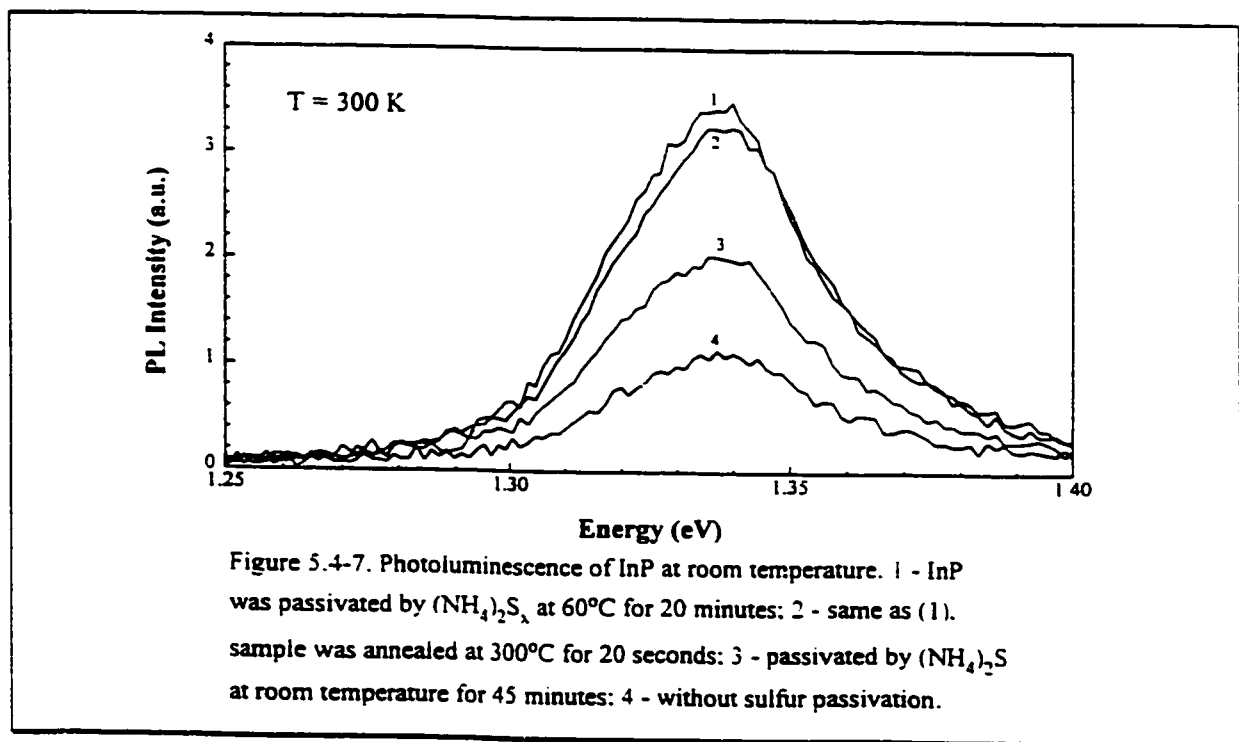


Figure 5.4-6. AES spectra of InP (sample #1): a) as received: b) after 30 second sputtering. The InP sample was passivated by $(\text{NH}_4)_2\text{S}_x$.

St. Kollakowski, 1994], Al_2O_3 [Klockenbrink, et al., 1994], and polyimide [Lee, 1988]. The results reported were somewhat controversial. Lee found that the deposition of SiO_2 can cause a buildup of As_2O_3 and/or In_2O_3 , thus increasing the amount of As, which is expected to be a source of excess leakage current, due to the mid-gap states, and the long-term failure of the device performance. On the other hand, Ambree reported that the use of SiO_2 reduced the dark current, and improved the long term stability of the device. For Si_3N_4 , Lee reported an improvement of the MSM-PD's performance, while Kollakowski observed an increase of the capacitance after Si_3N_4 passivation. Klockenbrink used Al_2O_3 to improve the thermal stability of the MSMs because the thermal expansion coefficient of Al_2O_3 is very close to that of InP and InGaAs. Although a slight increase in the dark current was observed, the saturation capacitance was found to be unchanged.



5.4.3 Dark Current

I. Flat Band Voltage

A typical I - V characteristic of an InGaAs MSM-PD (2x2) is shown in Figure 5.4-8. Figure 5.4-8a shows the dark current (without any light illumination) while Figure 5.4-8b shows the photoresponse under illumination at different power levels. The I-V curves of both the dark current and under illumination can be divided into three regions where different mechanisms dominate the carrier transport. At biases below the “knee” voltage, which corresponds to the flat band voltage obtained by a C-V measurement, the dark current is very small (negligible) but increases rapidly with increasing bias voltage because of the incomplete depletion below the flat band voltage. When the device is under light illumination, the photogenerated carriers recombine because the electric field

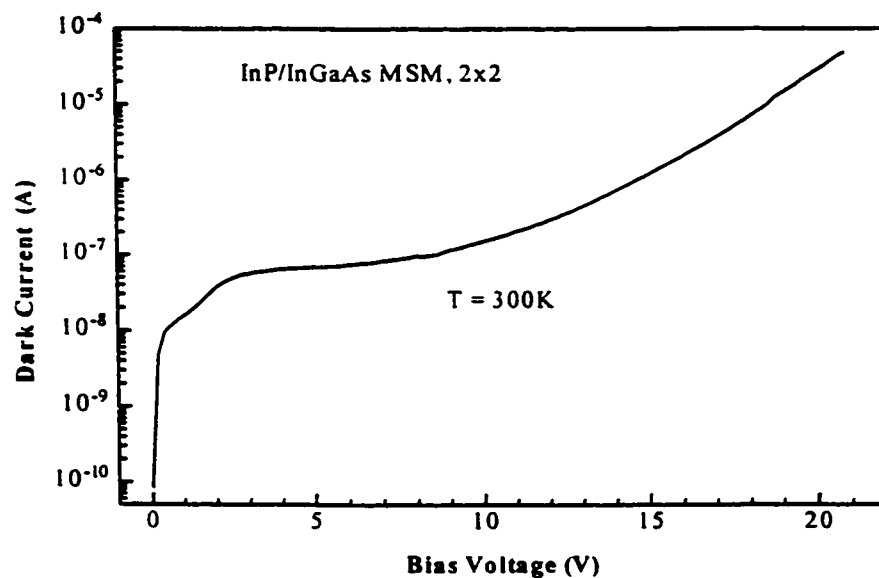


Figure 5-4-8a. Dark current of a typical InGaAs MSM-PD (2x2) as a function of bias voltage at 300K.

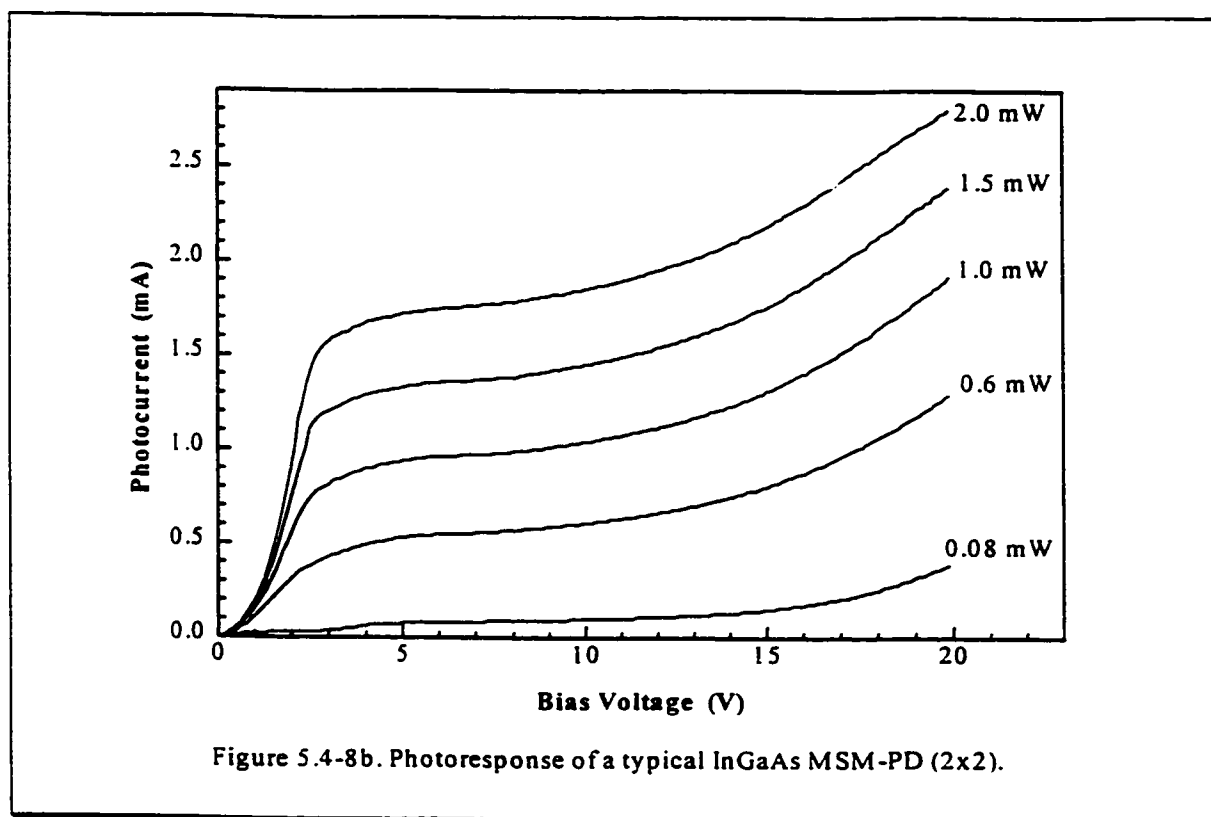


Figure 5.4-8b. Photoresponse of a typical InGaAs MSM-PD (2x2).

is not strong enough to separate them due to the low bias. The photoresponse curves also show a “knee” and its position shifts slightly to higher biases as the illumination increases - presumably a result of the increased space charge present. Just above the flat-band condition, a substantial fraction of the electron-hole pairs generated may still recombine if the separating field is not strong enough.

II. Saturation Dark Current

Above the “knee” voltage, the device is fully depleted and the saturation dark current is determined by the Schottky barrier heights for electrons and holes at the forward-biased and reverse-biased electrodes, respectively. When the device is illuminated, the photogenerated electron-hole pairs are being separated quickly by the strong electric field

due to the high-bias voltage and are being collected by the electrodes. In this region, the I-V curve is relatively flat - almost independent of bias voltage. In practice, however, a slight dependence of the saturation current on the bias is commonly observed. Many factors, such as defects and traps in the absorption layer, surface and interface states, and the charge pileup at the heterointerface in case of a wide-bandgap material being used as barrier-enhancement layer, are suggested to be responsible for this field dependence (it is also called “internal gain”). We will discuss this in more detail later.

Because of the lateral-current conduction in finger interdigitated MSM-PDs, the I-V curve is not exactly the same as that of a Schottky diode. Actually, the electrode semiconductor interface is by no means a “simple” Schottky contact. Still, thermionic emission is the dominant part of carrier transport, although field-assisted tunneling might be more significant in some cases, especially at high biases. According to the thermionic-emission model, in a one dimensional MSM-PD, the current may consist of electron flow and hole flow [Sze, 1971]

$$J = A_n^* T^2 \exp[-q(\phi_n - \Delta\phi_n)/kT] + A_p^* T^2 \exp[-q(\phi_p - \Delta\phi_p)/kT] \quad (5.4-5)$$

where A_n^* and A_p^* are the effective Richardson constants of electrons and holes, while ϕ_n and ϕ_p are the Schottky barrier height for electrons and holes, respectively. $\Delta\phi_n$ (eq.5.2-8) and $\Delta\phi_p$ (eq.5.2-15) are the barrier lowerings for electrons and holes, respectively. Table 5.4-4 is a summary of these parameters for the III/V compounds most commonly used to fabricate MSM-PDs.

Table 5.4-4. Important Parameters of Most Commonly Used III/V Compounds

	A_n^* ($\text{Acm}^{-2}\text{K}^{-2}$)	A_p^* ($\text{Acm}^{-2}\text{K}^{-2}$)	E_g (eV)	ϵ_r	ϕ_{Bn} (eV)	ϕ_{Bp} (eV)
InGaAs	5.04	49	0.75	11.09	0.2	0.6
InAlAs			1.47	10.28	0.82	0.7
InP	9.2	60	1.35	12.4	0.5	0.8
GaAs	8.86		1.42	13.1	0.8	0.6
$\text{In}_{0.49}\text{Ga}_{0.51}\text{P}$	13.2		1.92		0.92	1.2

At biases higher than the flat-band voltage, the current is governed by the thermionic emission of electrons at the reverse-biased electrode and by the hole injection at the forward biased electrode. As described by eq.(5.4-5), the saturation dark-current density varies exponentially with the electron and hole barriers. In some MSM-PDs, the saturation dark current may be dominated by the hole current, such as in an InAlAs/InGaAs MSM where the hole barrier (about 0.7eV) is lower than the electron barrier (0.82eV). For our InP/InGaAs MSM-PDs, electrons dominate the current transport in all bias regions.

The saturation dark current, as predicted in eq.(5.4-5), is affected by the barrier lowering terms, and the geometry of the electrodes because $I = S J$, where S is the electrode area (or the area of the electrode-metal contact), and J is the current density. Because of the lateral conduction in the MSM-PDs, the effective conduction area is different from the contact area. If the two contacts are not identical (geometry, area, barrier heights, electrode metals, etc.), then the I - V characteristics obtained after reversing the external applied bias are not symmetric, as is shown in Figure 5.4-9a. Figure 5.4-9b,

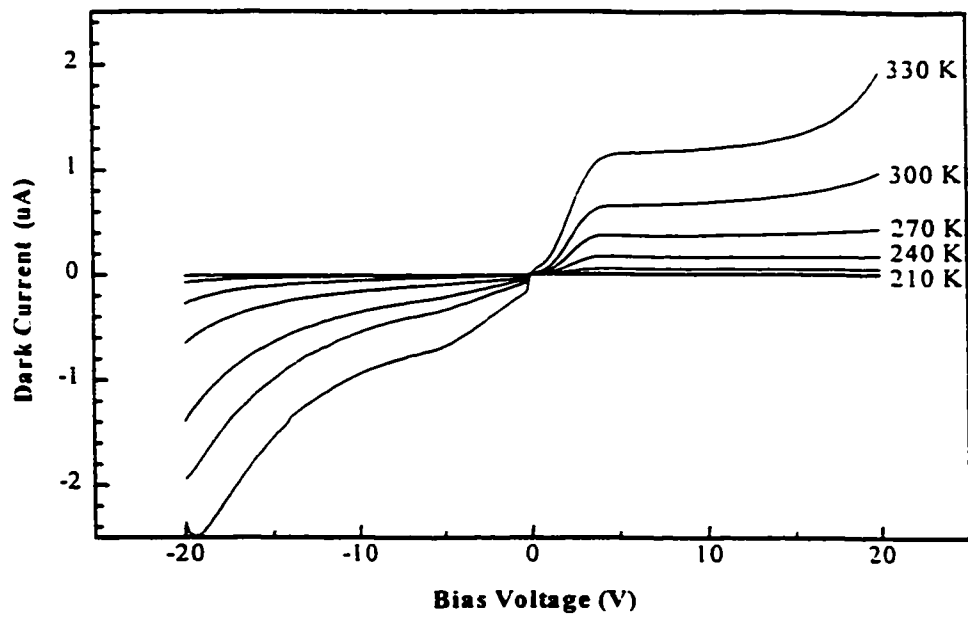


Figure 5.4-9a. Dark currents of an InGaAs MSM-PD (2x2) at temperatures from 120 to 330K.

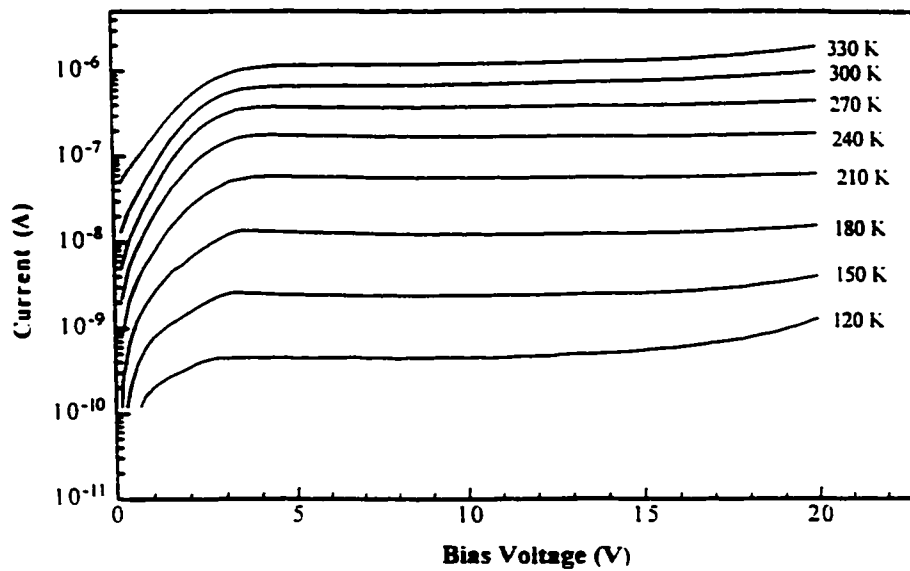
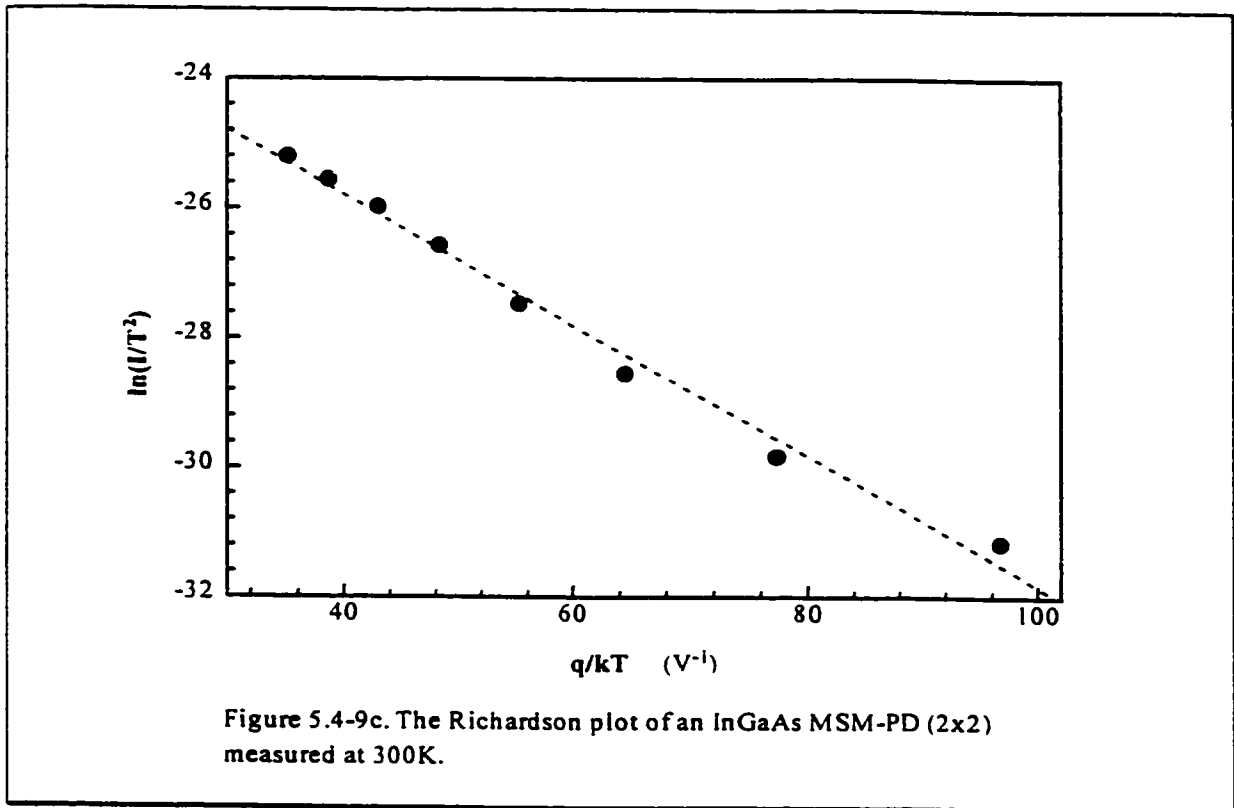


Figure 5.4-9b. Dark currents of an InGaAs MSM-PD (2x2) on a semi-log scale.

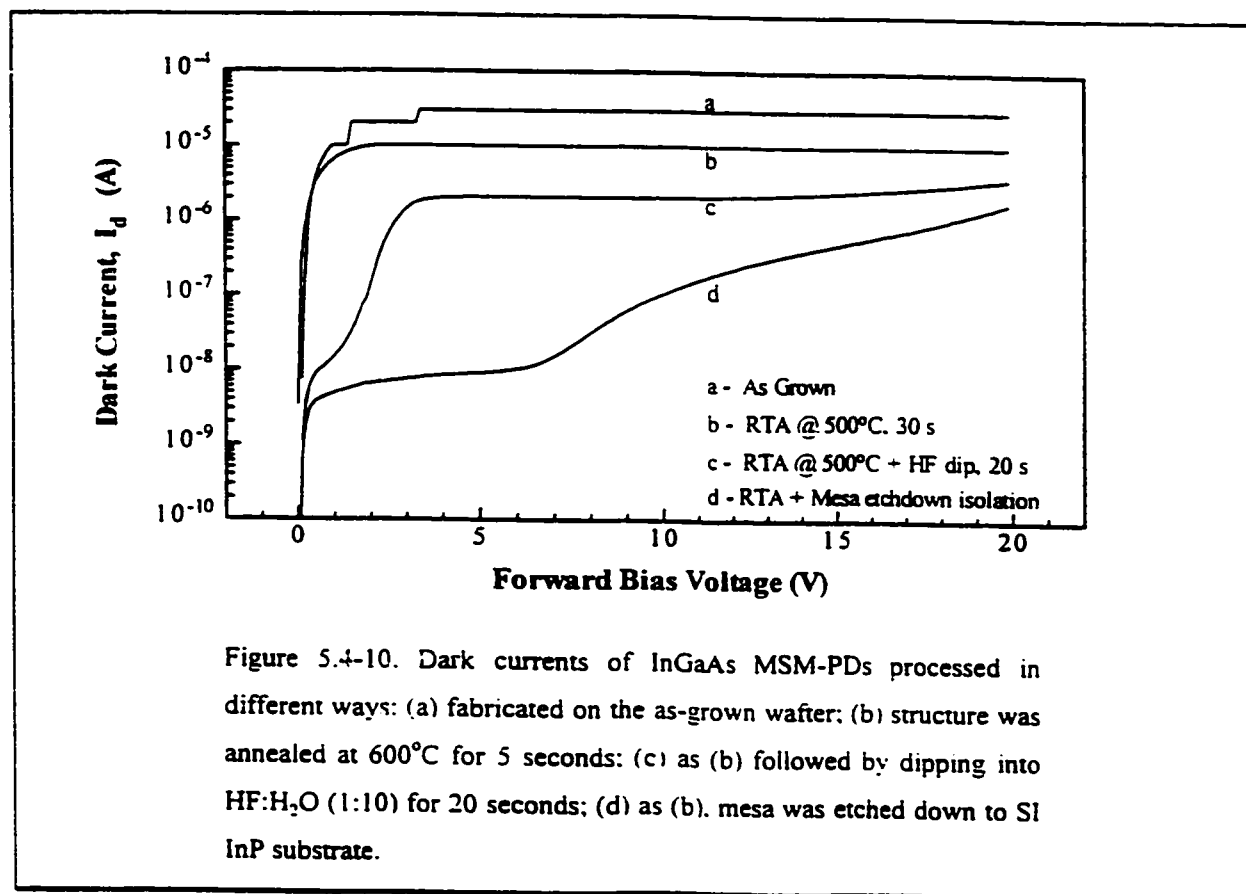


a part of Figure 5.4-9a, shows the dark current on a semi-log scale as a function of applied bias voltage at different temperatures. Figure 5.4-9c shows a Richardson plot, i.e., $\ln(I/T^2)$ as a function of inverse temperature (current measured at 10V). The fairly linear plot indicates that the carrier transport follows the thermionic emission model at this bias voltage.

In Chapter 3, we had investigated the InP/InGaAs Schottky diode which has the same MBE grown structure as the InP/InGaAs MSM-PD, except the SI InP substrate in the MSM-PD was replaced by n^+ -InP. For this Schottky diode, a barrier height of 0.48 - 0.50 eV was obtained. As is shown in Figure 5.4-9b, the saturation dark current decreases rapidly as the temperature is lowered. In temperature range between 120 - 330K, in an

InP/InGaAs MSM-PD, the carrier transport is mainly governed by thermionic emission at biases below breakdown. Based on the thermionic emission model, if the effective Richardson constant is assumed to be $A^*=9.2 \text{ Acm}^{-2}\text{K}^{-2}$, a barrier height of 0.475eV is obtained from the data in Figure 5.4-9c at $T=300\text{K}$. This is in good agreement with the values obtained in Chapter 3.

Figure 5.4-10 shows the dark currents of InP/InGaAs MSM-PDs processed by different techniques. The dark current of the MSM-PDs fabricated directly from the MBE grown structure is relatively high, about $30\mu\text{A}$ at 10V . If the MBE grown structure was annealed at 600°C for 5 seconds before device fabrication, the dark current of the fabricated MSM-PDs is reduced to $10\mu\text{A}$ at 10V . This is attributed to the reduction of



defects and traps in the MBE grown structure after thermal annealing. If, following the annealing, the structure was dipped into HF for 20 seconds, the dark current of the MSM-PDs is reduced to $2\mu\text{A}$ at 10V due to the removal of the surface oxide by HF. The dark current can be further significantly reduced by mesa etch-down to the SI InP between the electrode contact pads (Figure 5.4-10, curve *d*). This reduction in dark current is mainly due to the reduction of the conduction area between two oppositely biased electrodes. The above I-V results are consistent with the C-V data discussed in the previous section.

III. "Soft Breakdown"

There exists a "soft breakdown" in the I-V characteristics at high biases where the current increases dramatically as the bias voltage is increased. If the current is not

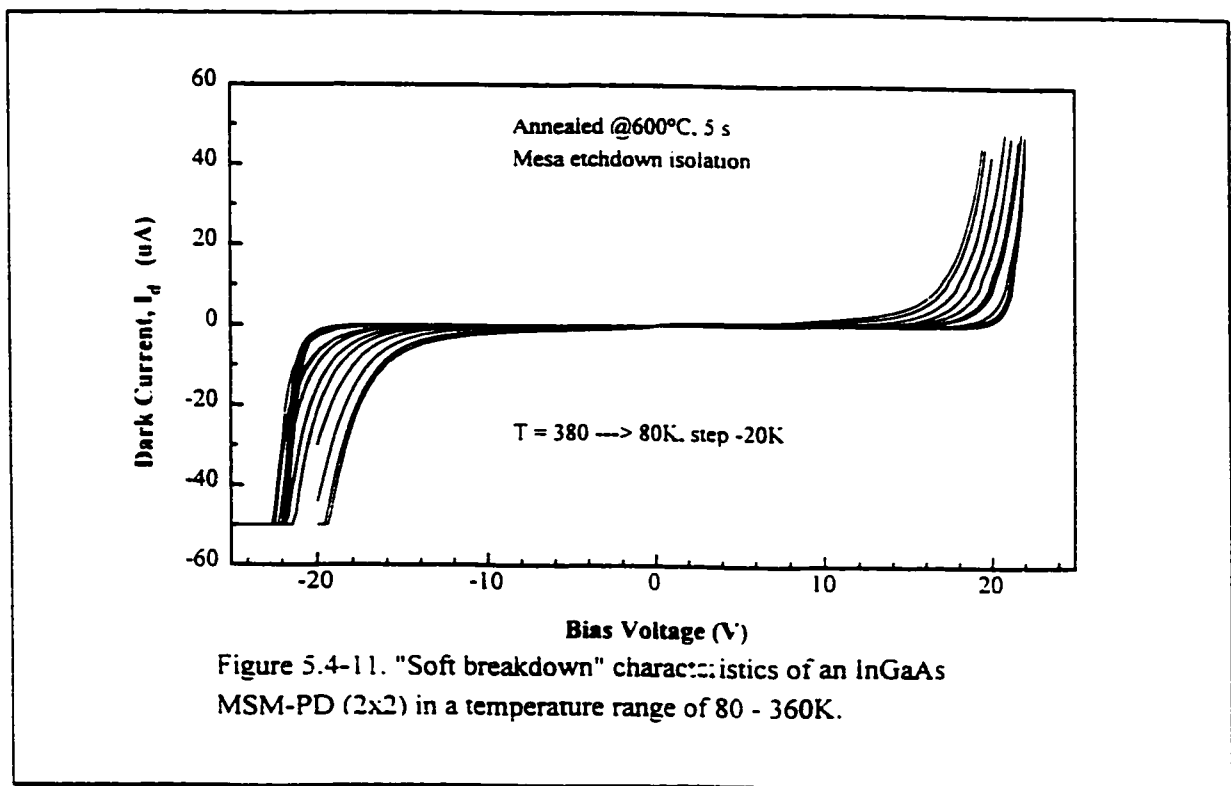


Figure 5.4-11. "Soft breakdown" characteristics of an InGaAs MSM-PD (2x2) in a temperature range of 80 - 360K.

limited, the device will eventually break down as the voltage is increased. Many groups [Soole, 1989; Griem, 1990; Harder, 1990] have argued that avalanching was responsible for this “soft breakdown”. However, our experimental results do not support the avalanche breakdown model and suggest that field-assisted tunneling could be responsible for the breakdown. Figure 5.4-11 shows the I-V characteristics at various temperatures. First, the breakdown voltage, V_B , of the InP/InGaAs MSM-PD is found to

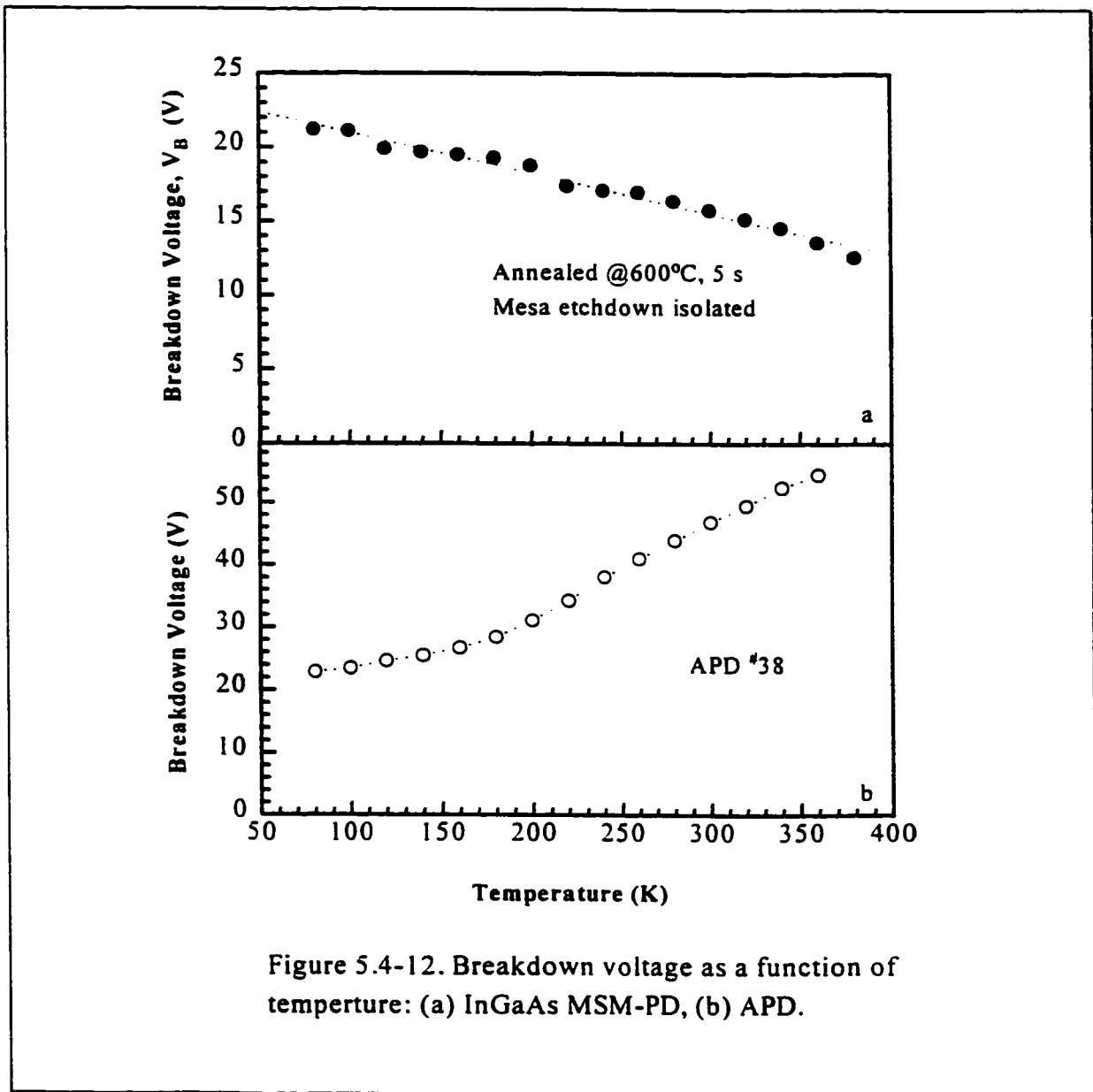


Figure 5.4-12. Breakdown voltage as a function of temperature: (a) InGaAs MSM-PD, (b) APD.

be about 15 -20 Volts. which is much smaller than that expected from avalanching. For InP (2 μm slab), the avalanche breakdown voltage is about 100-150 V while it is about 60 - 100V [Soole et al., 1989] for a 2 μm slab InGaAs. Second, the breakdown voltage, V_B , decreases when the temperature is increased (Figure 5.4-12a). If avalanching was responsible for the soft breakdown, then the breakdown voltage should increase when the temperature is increased, as is observed in avalanche photodiodes (APD) (Figure 5.4-12b) [BNR samples, 1996]. When breakdown occurs in a MSM-PD, it will be concentrated near the periphery of the electrodes. most probably at the finger tips where the electric field is likely to be the strongest.

IV. Barrier Enhancement

As mentioned in the introduction, the Schottky barrier height of InGaAs is about 0.2 eV, which is too low to make a good Schottky contact in device applications. Lattice-matched materials, such as InP and InAlAs, and lattice-mismatched materials, such as GaAs and AlGaAs, are employed to enhance the barrier height. We focus on the investigation of InP as the barrier-enhancement layer in an InGaAs MSM-PD. The

Table 5.4-5. Schottky Barrier Height of $\text{In}_{1-x}\text{Ga}_x\text{P}/\text{InP}$ Schottky Contacts

x	ϕ_b (± 0.01 eV)	n (± 0.01)	I_d (nA, 2V)
0.0	0.50	1.02	11.4
0.1	0.56	1.05	9.0
0.2	0.61	1.14	2.8
0.3	0.68	1.21	1.7

Schottky barrier height of MBE-grown InP is about 0.40 - 0.50 eV (see Chapter 3), depending on the metallization schemes, as well as the thickness of the MBE-grown InP and its doping level. To further increase the Schottky barrier height and to reduce the dark current, we investigated $\text{In}_{1-x}\text{Ga}_x\text{P}/\text{InP}$ on InGaAs as the barrier enhancement layer(s). Figure 5.4-13 shows the dark current of an InGaAs Schottky diode with 200Å $\text{In}_{1-x}\text{Ga}_x\text{P}$ ($x=0.15$) and 300 Å InP on top as the barrier layers, together with that of an InGaAs Schottky diode with only InP (500 Å) as the barrier layer. The employment of wide-band-gap InGaP reduces the dark current significantly, due to the increase in the Schottky barrier. Table 5.4-5 shows the barrier heights, Φ_B , the ideality factor, n , and the dark current, I_d , of the InP Schottky diodes with $\text{In}_{1-x}\text{Ga}_x\text{P}$ as the barrier layer (see Chapter 3, and Pang et al., 1995), where x is the fraction of Ga in the $\text{In}_{1-x}\text{Ga}_x\text{P}$.

In summary, employment of a thin barrier enhancement layer such as InP, or InAlAs,

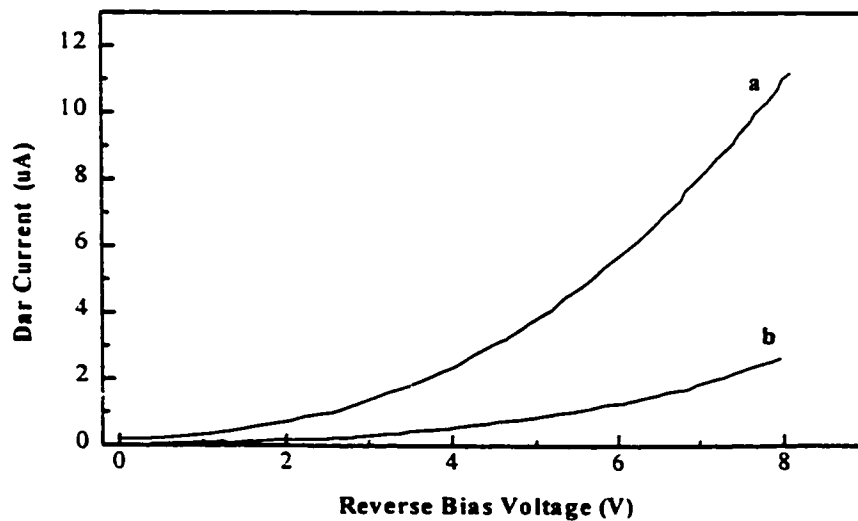


Figure 5.4-13. Dark current as a function of reverse bias voltage of InP/InGaAs (a) and $\text{In}_{0.85}\text{Ga}_{0.15}\text{P}/\text{InP}/\text{InGaAs}$ (b) Schottky diodes.

can increase the barriers for electrons and holes, and improve the carrier confinement to result in a smaller dark current.

V. Field-Assisted Tunneling

The simple Schottky barrier model provides an understanding of the low bias portion of the I-V characteristic. However, tunneling through the barrier enhancement layer (InP or InAlAs barrier) is required to explain the rapid rise of the dark current with increasing bias and the “soft-breakdown” characteristic. The tunnel current component of the leakage current rises steeply as the voltage dropped across the enhancement barrier reduces the effective barrier height(s). Then, with increasing bias, the width of the triangular barriers reduces, and eventually diminishes. The exponential dependence of the tunnel current on the barrier height and width results in a rapidly rising I-V curve. As shown in Figure 5.4-12, the soft breakdown is caused by field-assisted tunneling rather than avalanching.

VI. Surface Passivation

We systematically investigated the effect of sulfide passivation on InP/InGaAs MSM-PDs. It was found that the dark current of sulfide passivated devices was reduced by a factor of 2. The performance of the passivated MSM-PDs, such as the flat-band voltage and the breakdown voltage as well as the dark current are more consistent from device to device compared to that of unpassivated devices. Table 5.4-6a shows the dark currents of MSM photodetectors with different finger width and finger spacing, measured

Table 5.4-6a. Dark Currents of InGaAs MSM-PDs

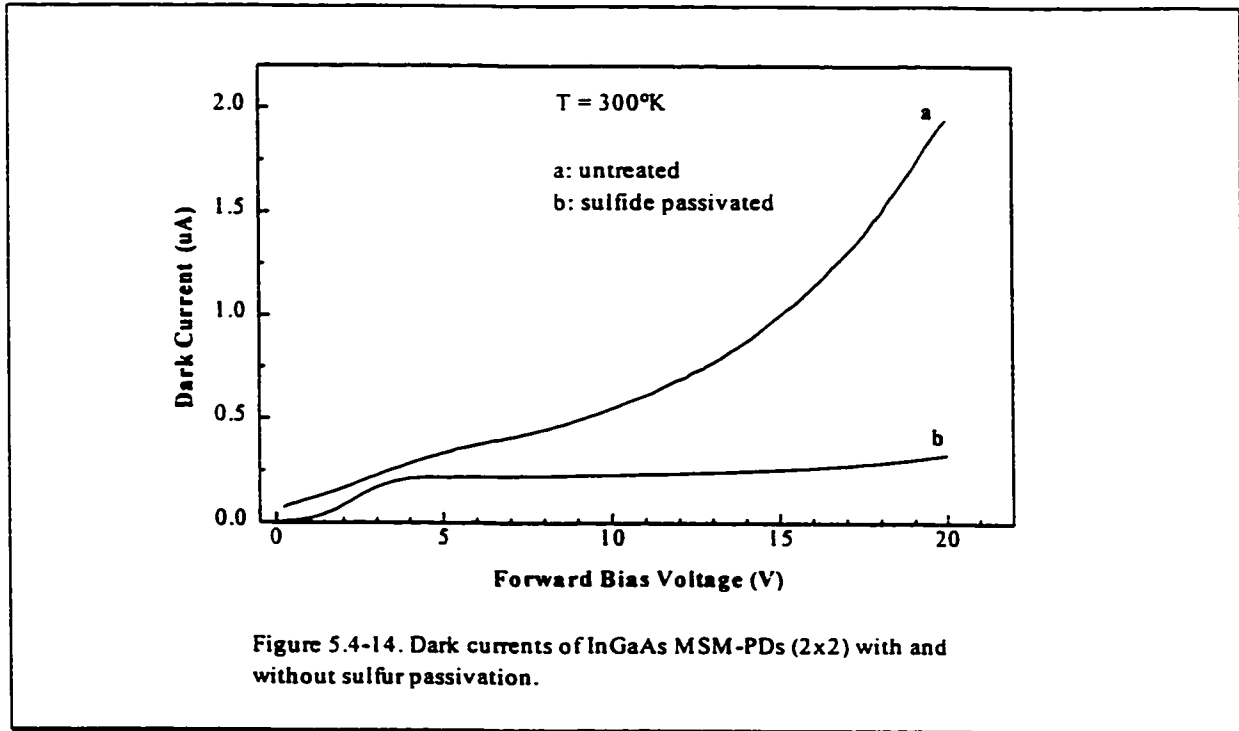
MSM-PD ($\mu\text{m}\times\mu\text{m}$)	I_d (± 5 nA)			
	T_a	T_b	T_c	T_d
1.0 \times 1.0	213	269	303	409
1.0 \times 1.5	281	249	341	426
1.0 \times 2.0	315	351	434	460
1.5 \times 1.5	353	398	397	447
1.5 \times 2.0	405	416	458	476
2.0 \times 2.0	306	354	430	480
2.0 \times 2.5	418	419	455	472

**Table 5.4-6b. Dark Currents of InGaAs MSM-PDs
(Sulfide Passivated)**

MSM-PD ($\mu\text{m}\times\mu\text{m}$)	I_d (± 5 nA)			
	T_o	T_1	T_2	T_3
1.0 \times 1.0	223	167	143	158
1.0 \times 1.5	279	170	142	198
1.0 \times 2.0	323	197	139	233
1.5 \times 1.5	418	165	141	228
1.5 \times 2.0	411	178	149	186
2.0 \times 2.0	286	185	162	201
2.0 \times 2.5	442	220	157	/

at different times (T_a , T_b , T_c , and T_d , represent 0, 2, 200 and 490 days, respectively) after fabrication, while Table 5.4-6b shows the dark currents of the MSM photodetectors passivated by a sulfide solution. T_0 was measured before sulfide passivation. T_1 , T_2 , and T_3 were measured at different times (2, 200, and 490 days, respectively) after surface passivation. All data shown in Table 5.4-6 were averaged from the results measured on 3 nominally identical devices. The reduction of the dark current in sulfide passivated InP MSM-PDs was caused by the increase in Schottky barrier height due to Fermi level depinning on the sulfur-treated surface while it is commonly suggested [Robinson, III/V Interface] that the Fermi level is pinned in InP so that the Schottky barrier height of a metal/InP (n-type) contact is about one third of the energy gap and is insensitive to the metal work function. It was reported [Han, et al.,1994] that sulfidization of the InP surface can cause Fermi-level depinning, therefore the Schottky barrier height of metals on sulfide-passivated InP can be increased when a proper metallization scheme is used. We systematically investigated the InP Schottky diodes with sulfide passivation as discussed in Chapter 4. The Schottky barrier height of sulfide-passivated diodes is increased from 0.42 to 0.44 eV for InP wafer, from 0.46 to 0.48eV for MBE grown structures. Figure 5.4-14 shows the I-V characteristics of InP/InGaAs MSM-PDs with and without passivation. At 10 V, the dark current of the passivated MSM-PDs is about 240nA while it is about 600nA for the same device without surface sulfide passivation. For the unpassivated device, a considerable increase of the dark current with bias was observed. This indicates the presence of relatively strong barrier lowering effects in the

devices. After sulfide passivation, this field dependency of the dark current is significantly reduced.



Because of the lateral conduction in MSM-PDs, the surface layer plays a more important role in the current flow than it does in other vertical conduction devices. The current flow is confined to the high electric field region near the metallization edges of the contact fingers. Obviously, the electrically activated area is much smaller than the geometric area. As discussed in Figure 5.4-9, if the two contacts are not identical, the I-V curve is not symmetric when the bias is reversed. Figure 5.4-15a shows the I-V curves of the same device represented in Figure 5.4-9 after sulfide passivation. The fact that they are more symmetric than those of Figure 5.4-9 indicates that the surface sulfide passivation reduces both the concentration of the surface states and the barrier lowering which are field dependent. A calculation of the saturation current at T=300K from Figure

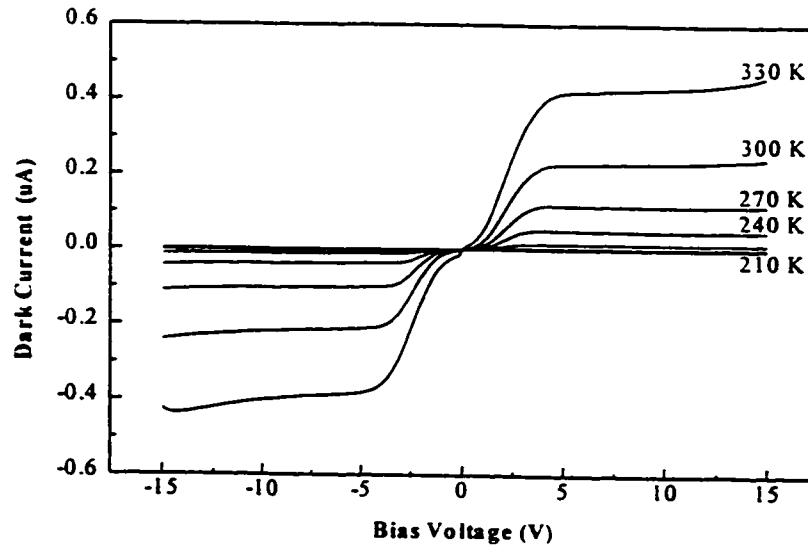


Figure 5.4-15a. Dark currents of a 2x2 InGaAs MSM-PD at temperatures from 120 to 330K. The MSM-PD was passivated by sulfide solution.

5.4-15a gives the Schottky barrier height of 0.498 eV, compared to 0.475eV from Figure 5.4-9 for the unpassivated MSM-PDs. This is in agreement with the 0.02 - 0.03 eV increase in Schottky barrier height of InP Schottky diodes after sulfide passivation, discussed in Chapter 4. Table 5.4-7 gives the calculated Schottky barrier heights from Figure 5.4-9 and Figure 5.4-15a.

Table 5.4-7. Schottky Barrier Heights of InP/InGaAs MSM-PDs

(calculated from I-V-T, Figures 5.4-9 and 15)

T (K)	SBH (eV @2V)		SBH (eV @5V)		SBH (eV @10V)	
	As is	Passivated	As is	Passivated	As is	Passivated
270	0.432	0.459	0.410	0.437	0.410	0.437
300	0.471	0.498	0.446	0.474	0.445	0.473
330	0.506	0.536	0.480	0.509	0.479	0.509

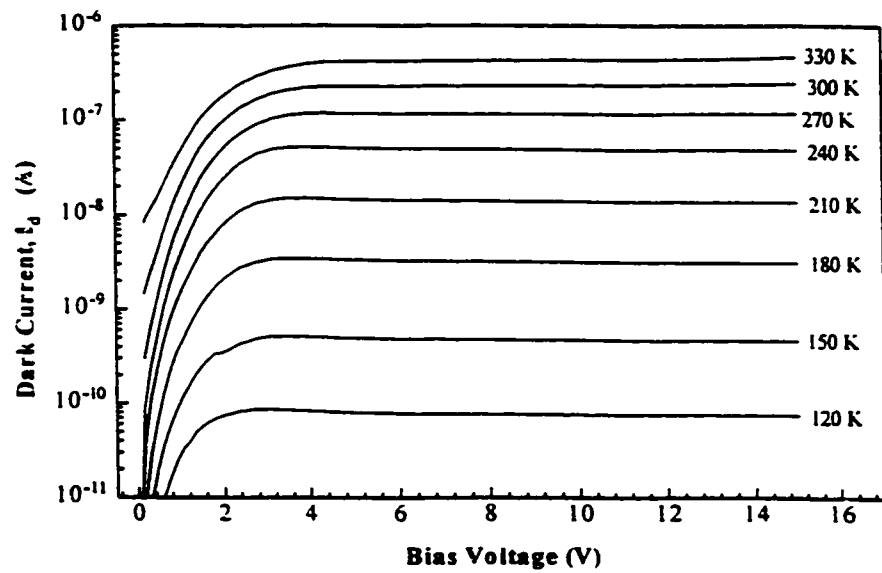


Figure 5.4-15b. Dark currents (in log scale) of an InGaAs MSM-PD (2x2) at temperatures from 120 to 330K. The MSM-PD was passivated by sulfide solution.

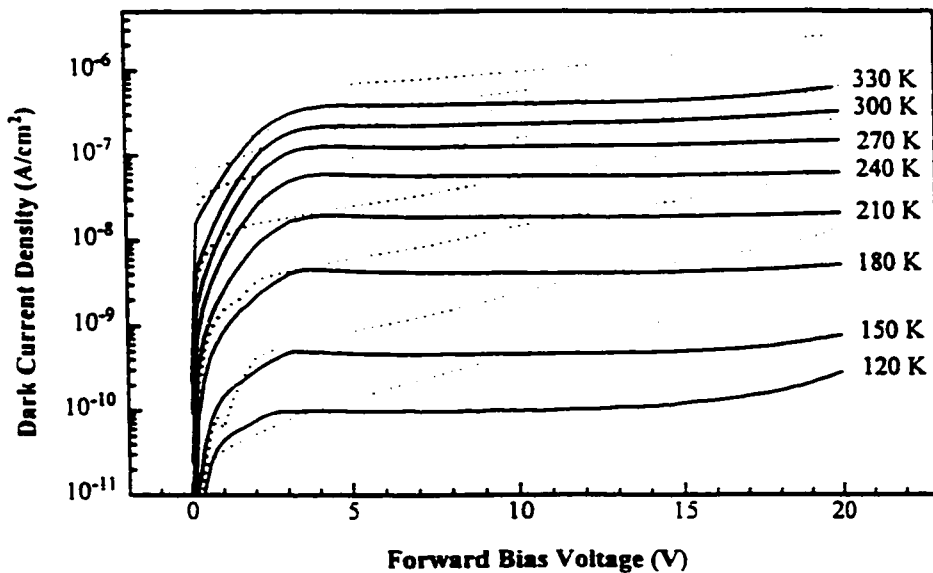


Figure 5.4-15c. Dark currents of an InGaAs MSM-PD (2x2) before and after sulfur passivation. Currents were measured at temperatures from 120 to 330K.

Figure 5.4-15b, a part of Figure 15a, shows the I - V characteristics at different temperatures (120 - 330K). Compared to Figure 5.4-9b for the unpassivated device, the I-V characteristic of the sulfide-passivated MSM-PD is flatter.

To see the improvement in the dark current after sulfur passivation, the dark currents of the MSM-PDs with and without sulfur passivation are shown together in Figure 5.4-15c.

Figure 5.4-16a shows the dark currents of sulfide passivated MSM photodetectors with different finger configurations as a function of aging time. Compared to those of the unpassivated devices shown in Figure 5.4-16b, the dark currents of passivated MSM-PDs are much more stable as the aging time increases. This improvement in stability after sulfide passivation is attributed to the reduction of surface states and the formation of In-S bonds which are very stable, as mentioned previously.

In Chapter 2, we have shown that inhomogeneities at the metal-semiconductor interface may cause the current-voltage behavior to depart from the ideal thermionic emission model. As discussed previously, the "soft breakdown" I-V characteristics of an InP/InGaAs MSM-PD are primarily caused by the field-assisted tunneling through the barrier due to the high fields near the edges of the metal semiconductor contacts. The surface sensitivity of the dark current characteristics can be qualitatively explained as follows: Electrons may tunnel into surface traps in the vicinity of the electrode edges. As a result, charges accumulate on the surface and give rise to a modification of the electric field distribution near the contact edge. The effect of these trapped charges counteracts the electric field strength in the direction along the surface produced by the externally

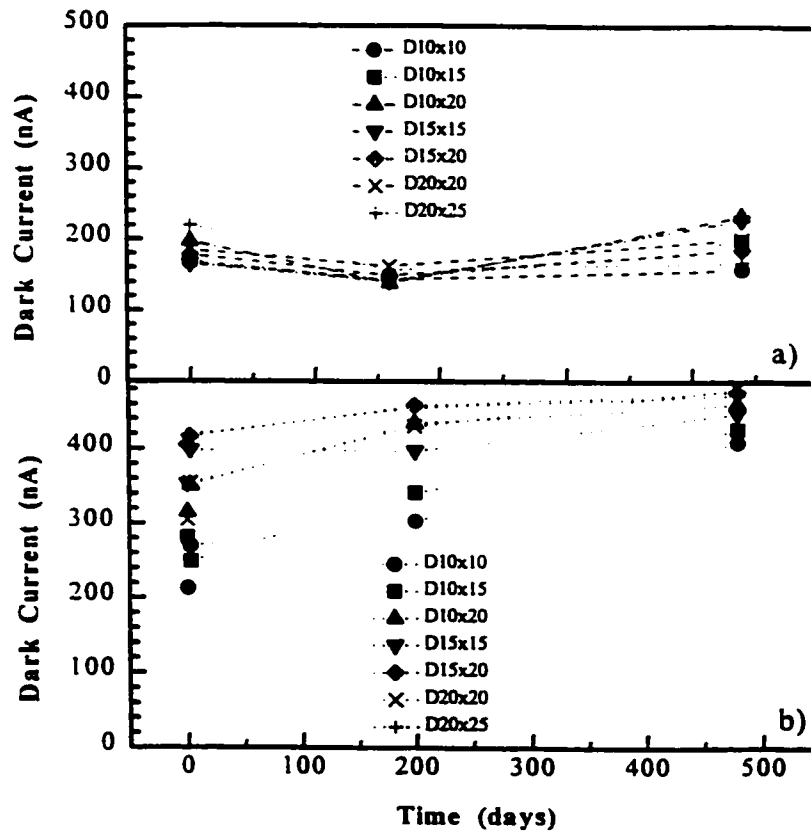


Figure 5.4-16. Dark currents of InGaAs MSM-PDs with (a) and without (b) sulfur passivation. Currents were measured after the devices had been exposed to air for some time.

applied voltage. The increasing occupation of surface traps impedes a rapid rise of the dark current and leads to the observed soft characteristics with increasing bias.

The surface passivation of InP/InGaAs MSM-PDs can reduce the surface states and minimize the field-dependent barrier lowering effects as discussed in Chapter 4, especially in areas near the electrode edges. In turn, the effective barrier height is raised and the dark current is reduced.

5.4.4 Photoresponse

I. I - V Characteristics

As is shown in Figure 5.4-8b, at low bias (below the knee voltage), the current increases rapidly because of incomplete depletion and photogenerated carriers recombine at low electric fields. Above the “flat-band” voltage, the photocurrent rises gently as the bias is increased. At high biases, “soft break down” characteristics are observed, similar to that without light illumination.

Figure 5.4-17 shows the photoresponse of InP/InGaAs MSM-PDs treated in different ways before fabrication. The I-V curves of the MSM-PDs fabricated directly from a MBE grown structure show a strong bias dependency (Figure 5.4-17a). Annealing of the MBE grown sample at 600°C for 5 seconds reduced the trap and defect density in the bulk material, and the I-V characteristic of the MSM-PD annealed before fabrication is more flat below “soft breakdown” (Figure 5.4-17b). Dipping the annealed sample into HF for 20 seconds further reduced the field dependent effect due to removal of the surface oxide (Figure 5.4-17c). The unintentional interfacial oxide barrier under the electrodes can result in carrier trapping because the oxide barrier can cause carrier injection from the electrodes. Figure 5.4-17d shows the photoresponse of the MSM-PD annealed and then mesa etchdown isolated.

The dark current characteristics of all above devices processed in different ways were discussed in §5.4-3. Under illumination, the I-V characteristics behave in similar ways except for the contribution from the photocurrents. The main differences will be discussed in the following sections.

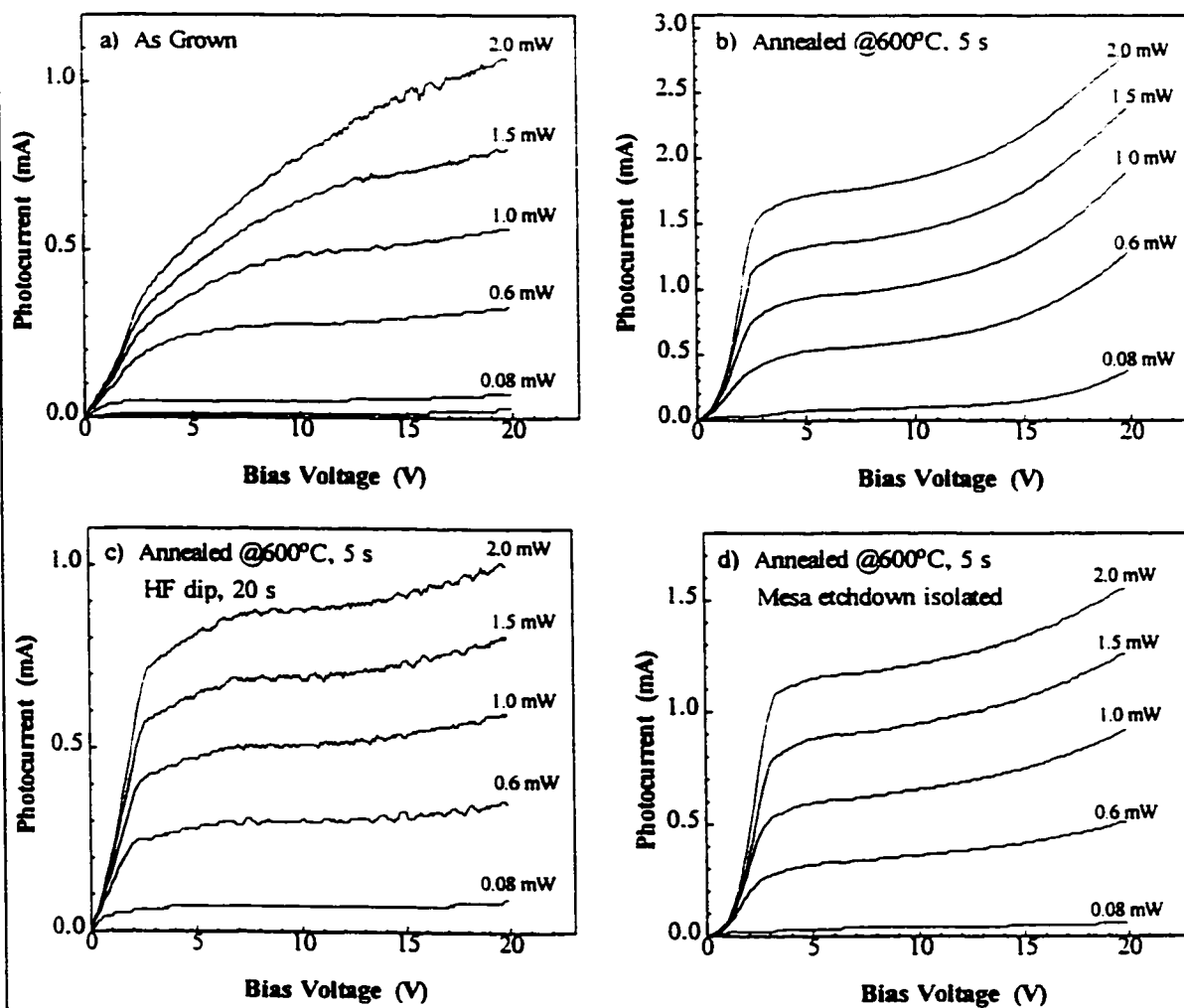


Figure 5.4-17. Photoresponses of InGaAs MSM (2x2) photodetectors fabricated by different processes. (a) fabricated on as-grown structure; (b) structure was annealed at 600°C for 5 s before fabrication; (c) as (b), followed by dipping into HF:H₂O (1:10) for 20 s. (d) as (b), mesa was etched down to SI InP substrate.

II. Internal Gain

In the current saturation region, the photocurrent is expected to be constant (independent of bias voltage). However, a slight bias dependency of the photocurrent - the photocurrent increases with the bias voltage, is observed due to internal gain.

A possible mechanism for the internal gain is field-assisted tunneling, similar to that discussed in §5.4-3 to explain the "soft breakdown" characteristic of the dark current of the InGaAs MSM-PDs. Under illumination, the photogenerated carriers may contribute to this field-dependent effect. This mechanism can be qualitatively described as follows: In the saturation current and the soft breakdown regions, the electric field in the vicinity of the negatively biased electrodes is very high, resulting in the accumulation of the photogenerated holes near the edges of the negatively biased electrodes. The accumulation of holes will increase the electric field and enhance the tunneling effect. These processes will trigger the internal gain. As a consequence, the emission rate of electrons into surface traps rises. The magnitude of the photocurrent gain produced by field-assisted tunneling and enhanced by the photogenerated carriers, is closely related to the dark current behavior. The number of injected excess carriers is much larger than that in the current saturation region. So, the field-dependence of the photocurrent under illumination is more significant than that of the dark current (without illumination). That is why the "soft breakdown" shifts to lower bias voltage, and steeper I-V curves are observed under illumination.

Figure 5.4-18 shows that the I-V curves of sulfide passivated MSM-PDs are more flat than those of unpassivated devices. This observation is agreement with those obtained from previous capacitance and dark current measurements. The improvements in the performance of MSM photodetectors after sulfide passivation are presumably closely connected to a modification of the surface electronic conditions. As discussed in Chapter 4, surface sulfide passivation results in a reduction in surface states and a minimization of field dependent effects.

Although the internal gain is primarily attributed to traps and defects on the semiconductor surface, the accumulation of (the photogenerated) holes is not necessarily caused by trapping localized at the surface. Traps and defects in the bulk semiconductor, [Harder, et al., 1990, Ito, et al. 1986], the pile-up of holes at the InP/InGaAs

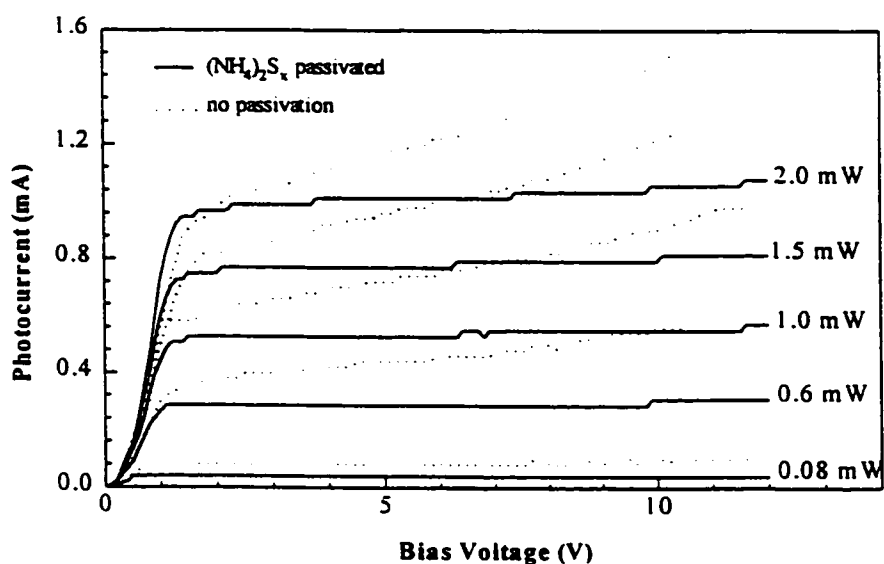


Figure 5.4-18. Photoresponses of an InGaAs MSM-PD (2x2) before and after sulfur passivation.

heterointerface and/or trapping by interface states [Soole, et al., 1990], represent further possibilities. It is also suggested that the modulation of the conduction-band edge under the anode (positively biased electrode) might be responsible [Ito, et. al., 1986] for the internal gain.

The trap density in the absorption layer can be minimized by using high-quality absorption material and by growing a buffer layer between the substrate and the active layer. It was found that using lattice-matched barrier enhancement layers can reduce the internal gain compared to using a lattice-mismatched barrier layer. It is suggested that charge pileup can be avoided by grading out the band offset at the InP (or InAlAs) /InGaAs heterointerface.

III. Responsivity

The photoresponse was found to increase linearly with the incident light intensity, up to 2 mW (maximum level available in our experiment). Power saturation effects might be expected to occur due to space charge buildup within the device. The observed decrease of the gain with increasing optical power may result from saturation of the hole traps and/or the unoccupied surface traps.

Figure 5.4-19 shows how the responsivity varies with the incident optical power for the devices in Figure 5.4-17. The responsivity increases slightly as the optical power increases from 0.5 mW to 1.0 mW, then decreases slightly in the range of 1.0 mW to 2.0 mW. Generally speaking, the responsivity is relatively flat in the range of 0.5 mW to 2.0 mW.

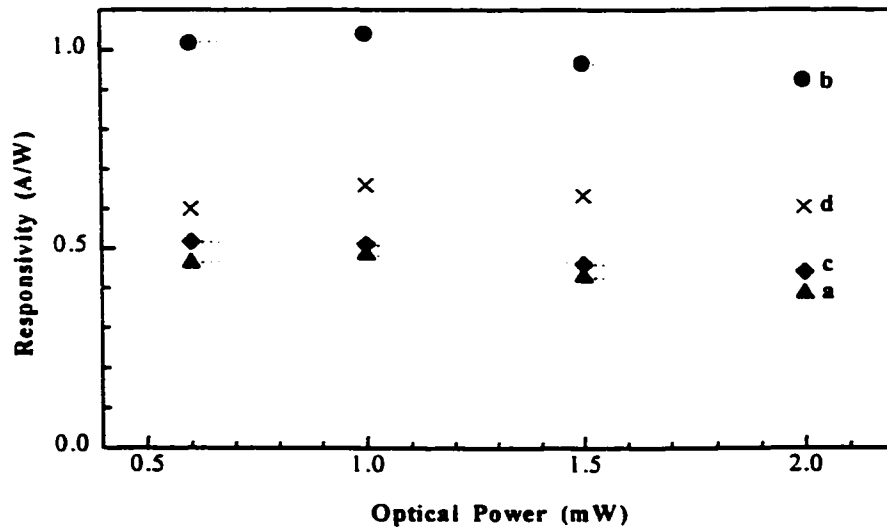


Figure 5.4-19 Responsivity of InGaAs MSM-PDs as a function of the incident power. (a) MSM-PD was fabricated on as-grown structure; (b) structure was annealed at 600°C for 5 s before fabrication; (c) same as (b), and was dipped into HF:H₂O (1:10) for 20 s. (d) same as (b), mesa was etched down to SI InP substrate.

Table 5.4-8. Dark Currents and Responsivity of InP/InGaAs MSM-PDs

	I_d ($\pm 0.1 \mu A$)	Resp. ($\pm 0.005 A/W$)		I_d ($\pm 0.1 \mu A$)	Resp. ($\pm 0.005 A/W$)
As-Grown	@ 5V	@ 10V	HF Treated	@ 5V	@ 10V
1x2 -11	180.9	0.537	2x2 -1	1.25	0.529
2x2 -11	25.1	0.301	2x2 -2	2.63	0.521
2x2 -22	25.9	0.366	2x2 -3	10.4	0.495
2x2 -33	26.8	0.378			
Annealed	I_d ($\pm 0.1 \mu A$)	Resp. ($\pm 0.005 A/W$)	As.G.+Isol.	I_d ($\pm 0.1 \mu A$)	Resp. ($\pm 0.005 A/W$)
1x2 -21	18.9	0.845	1x2 -11	0.410	0.565
1x2 -41	17.8	0.850	1x2 -41	1.001	0.672
2x2 -13	14.9	1.222	1x2 -52	0.929	0.542
2x2 -21	16.4	0.698	2x2 -12	0.207	0.606
2x1 -22	14.1	0.867	2x2 -31	0.045	0.583
2x2 -41	17.9	0.924	2x2 -53	0.010	0.594

Table 5.4-8 shows the responsivity of InP/InGaAs MSM-PDs processed by different techniques. The device fabricated directly from the as-grown MBE structure has a responsivity of 0.37 A/W, the annealed one has the highest one of 0.85 A/W, while the HF treated one has 0.52 A/W, and the mesa etchdown device has 0.57 A/W. These results are consistent with the C-V and dark current results.

5.4.5 Quantum Efficiency

The external quantum efficiency is predominantly determined by the electrode structure and the absorption layer of the MSM device. This is given by [Soole, 1991]

$$\eta = (1-r) \cdot \frac{s}{s+w} \cdot (1 - e^{-\frac{d}{L}}) \quad (5.4-6)$$

where w is the finger width, s is the interdigitated finger spacing, L is the optical penetration length at the wavelength used, d is the InGaAs absorption layer thickness, r is the reflectivity. For InGaAs, the penetration length is 0.87 μm and 1.47 μm at wavelengths of 1.3 μm and 1.55 μm , respectively [Humphreys, et al., 1985].

Figure 5.4-20 shows the calculated external quantum efficiency of MSM-PDs vs InGaAs thickness with different geometries (finger width x finger spacing) at wavelengths of 1.3 μm (Figure 5.4-20a) and 1.55 μm (Figure 5.4-20b), respectively. For the same MSM-PD structure, the external quantum efficiency at 1.3 μm is slightly higher than that at 1.55 μm due to the shorter penetration depth in the former case. For the same active area at a given wavelength, the MSM-PD with the same finger width and a larger finger spacing has a higher external quantum efficiency because of the larger effective

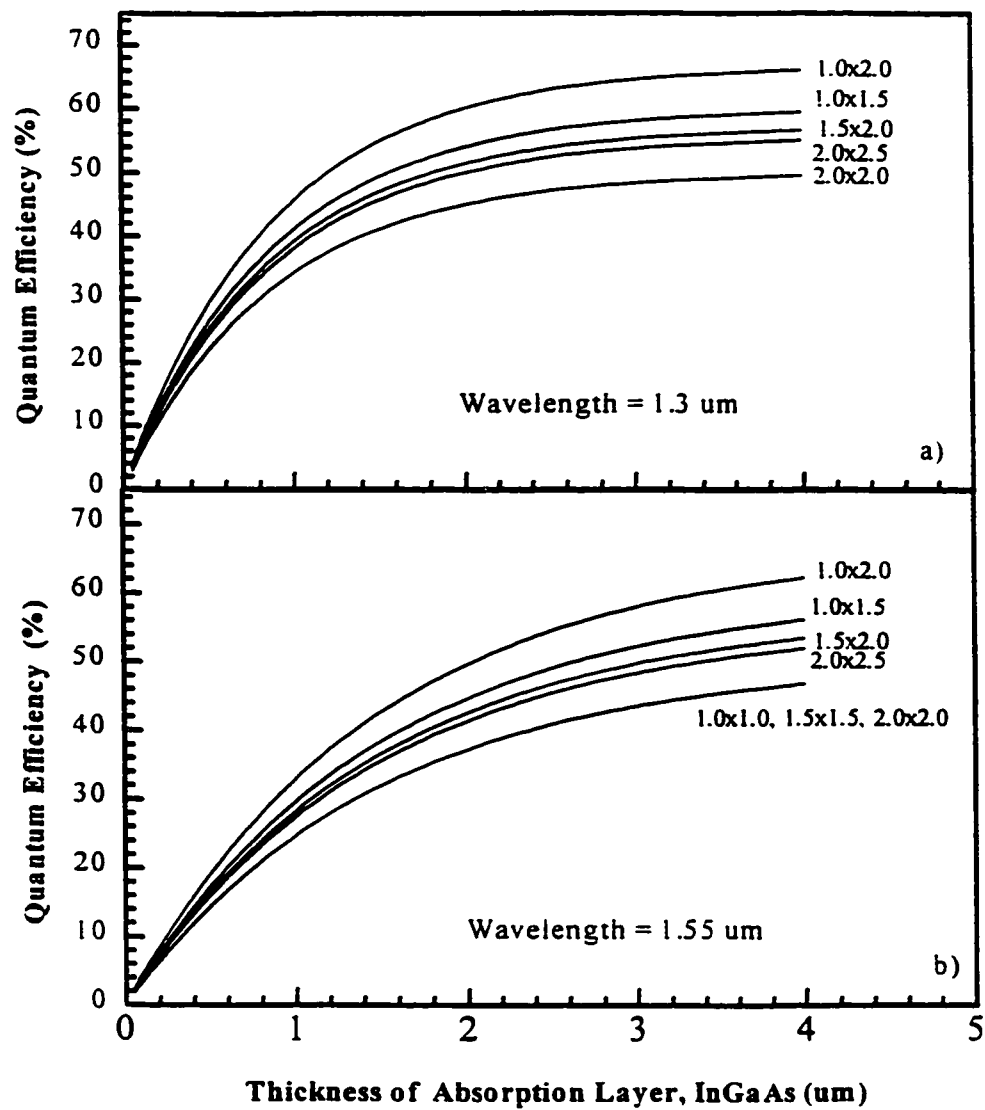


Figure 5.4-20. Calculated quantum efficiency of InGaAs MSM-PDs at wavelengths of (a) 1.3 um and (b) 1.55 um.

area to absorb the incident light. For a $2\mu\text{m}$ thickness of the InGaAs absorption layer, the external quantum efficiency ranges from 40% to 65% depending on the finger configuration as well as the wavelength.

High speed, low dark current and high external quantum efficiency are the most important parameters of an MSM-PD. Compared to p-i-n photodetectors (PIN-PD), MSM-PDs have lower external quantum efficiency because of the interdigitated finger structure. Many different techniques have been employed to achieve higher external quantum efficiency. The most commonly used and the most important ones are summarized below:

- a) *Antireflection (AR) Coating* The quantum efficiency can be increased slightly by use of an antireflection coating [Kollakowski, 1994] which reduces the reflection of the incident light. SiO_2 , Si_3N_4 and polyimide are the most frequently used antireflection coatings.
- b) *Reducing the Finger Width by e-Beam Writing* As is shown in Figure 5.4-19a and 5.4-19b, reducing the electrode finger width can increase the quantum efficiency. However, the conventional photolithographical processes limit the finger width to about $1\mu\text{m}$. Compared to optical lithography, electron beam lithography can be employed to produce submicron devices.
- c) *Semitransparent Electrodes* To effectively reduce the finger shadowing, semitransparent electrodes may be used to increase the quantum efficiency. It was reported [Yuang, 1995] that the responsivity was increased from 0.4 to 0.7

A/W at a wavelength of 1.55 μm using semitransparent Au electrodes with a thickness of 100Å.

- d) *Using a Back Reflector* A back reflector making the incident light go through the absorption layer twice can be used to increase the quantum efficiency. However, this technique may make the growth and fabrication more complicated.
- e) *Surface Grating* Surface gratings [Sheridan, 1993, Fallahi, 1993] were used to increase the quantum efficiency because a grating can change the incident light distribution pattern and make the incident light be collected more efficiently.
- f) *Back Illumination* To avoid the finger shadowing problem, back illumination was proposed [Kim, 1992, Hieronymi, 1993]. To use the back illumination, the substrate must be thinned to a few microns. The highest quantum efficiency was obtained with a responsivity of 0.96 A/W for an InGaAs/InAlAs MSM-PD using back illumination [Kim, 1992].
- g) *Using Lattice-Mismatched $\text{In}_x\text{Ga}_{1-x}\text{As}$ ($x > 0.53$)* It was reported that $\text{In}_x\text{Ga}_{1-x}\text{As}$ ($x > 0.53$) is more efficient in absorbing the incident light than InGaAs lattice-matched to InP. Therefore, the quantum efficiency can be increased. However, the employment of lattice-mismatched $\text{In}_x\text{Ga}_{1-x}\text{As}$ may cause degradation in the DC characteristics of the MSM-PDs, and degradation in speed because of traps associated with the strained absorption layer.

Chapter 6

CONCLUSION

In conclusion, a systematic investigation of Schottky contacts to InP has been carried out. The work can be divided into several parts. First, we extended the inhomogeneous barrier model proposed by Werner [1991] by introducing the ideality factor, n_1 , and the virtual barrier height, $\overline{\phi}_b(0,0)$, to analyze the current-voltage data and to explain the barrier anomalies. Second, a systematic investigation was conducted to optimize the metallization schemes for Schottky contacts to InP and related materials. The results provide us with a guideline to fabricate InP Schottky diodes and other devices to achieve the best performance. Third, barrier enhancement on InP using $\text{In}_{1-x}\text{Ga}_x\text{P}$ as the contact layer was investigated. This can further raise the Schottky barrier height of the metal-InP/InGaAs structure, and therefore improve the performance of InP/InGaAs devices, such as MSM-PDs and HEMTs. Fourth, surface control of the InP samples was investigated using sulfur passivation. This surface passivation can greatly reduce the density of the surface states and improve the performance of the InP-based devices. Finally, InP/InGaAs MSM-PDs were designed, fabricated and characterized. The performance of the InGaAs MSM-PDs is comparable to the best reported so far. The results of each part are briefly summarized below:

I. CONDUCTION MECHANISMS IN InP SCHOTTKY BARRIER

The current-voltage characteristics of the InP Schottky diodes are found to depart from the ideal behavior. The departure is more significant at low temperatures. This can not be explained by the ideal thermionic emission theory. It was found that the ideality factor, n , increases dramatically as the temperature is lowered, while the Schottky barrier height was found to be both temperature and bias dependent. The Schottky barrier height and the Richardson constant can not be extracted from the linear fitting to the Richardson plot. $\ln(J_0/T^2)$ vs. $1/T$, because of its nonlinearity.

Although the contact edge leakage current, the image-force lowering, the field-assisted tunneling through the barrier, the recombination current in the depletion region, the effects of interfacial layers, such as oxides, may cause the I-V characteristics to depart from the ideal thermionic emission behavior, careful examination shows that, for undoped InP, their contributions are not significant: the ideality factor is slightly increased up to about 1.10 in the whole experimental temperature range from 80 K to 360 K. Apparently, the above current transport mechanisms can not explain why the ideality factor increases up to about 2.0 at low temperatures (80 - 200K).

In this investigation, an inhomogeneous Schottky contact was assumed, where the built-in potential and the Schottky barrier height fluctuate around their mean value with a Gaussian distribution. Based on this inhomogeneous barrier model [Werner, 1991], a modified current-voltage relationship was developed with the introduction of n_1 and $\overline{\phi_b}(0,0)$. The behavior of the temperature-dependent ideality factor and the temperature- and-bias dependent barrier height can be well explained by this modified model. The

modified Richardson plot is a direct result of this modified model, and the so called " T_0 " effect is an approximation under certain conditions. All parameters in this model can be determined experimentally. Most importantly, the barrier height determined from this model is very consistent regardless of forward-bias measurement or reverse-bias measurement are employed.

II. METALLIZATION SCHEME FOR SCHOTTKY CONTACTS TO InP

Metallization schemes for Schottky contacts to InP were systematically investigated, which include refractory metallization schemes prepared by rf sputter deposition and Au-based metallization schemes deposited by electron-beam evaporation. Although sputtered TiN, WN, and WTiN have superior thermal stability, surface damage to the InP surface caused by sputtering, and the difficulty in controlling the film stoichiometry and the film uniformity over large areas are major drawbacks to rf sputtering for device applications. Electron beam evaporation is more easy to control and is compatible with device fabrication processes. However, the Au-based metallization schemes based on e-beam evaporation are thermally unstable at temperatures higher than 400°C. Moreover, it is difficult to deposit nitride compounds of refractory metal(s) by e-beam evaporation. For the Au-based Schottky contact schemes on n^+ (or undoped) -InP prepared by e-beam evaporation, it was found that

1. AuTiPt and AuPtTiPt have higher barrier heights in Schottky contacts to InP. AuNiPt has the best uniformity and reproducibility although it has a slightly lower barrier height.

2. Thermal annealing at temperatures from 300°C to 400°C for 20 - 30 seconds improves the performance of the InP Schottky diodes. Annealing at temperatures higher than 400°C will result in degradation of the device's performance. This is due to the inter-diffusion of Au and P at high temperatures.
3. The Schottky barrier height of AuNiPt Schottky contacts to epitaxially grown n⁻-InP is about 0.50 eV with an ideality factor of 1.04 at room temperature. The reverse breakdown voltage is about 12 V and the leakage current at -2V is about 11.4 μA for the Schottky diode with a diameter of 400 μm.

III. SCHOTTKY BARRIER HEIGHT ENHANCEMENT

Although the barrier height of the InP Schottky diode is about 0.5 eV, it is not high enough for some device applications. Barrier enhancement using In_{1-x}Ga_xP as the enhancement layer has been investigated. This makes use of the wider band gap of InGaP. The results can be summarized as follows:

1. The employment of a thin In_{1-x}Ga_xP (x = 0.1 to 0.3) layer on top of the InP results in an increase in barrier height. The zero-bias Schottky barrier height is increased from 0.50 for (x= 0) to 0.58, 0.61, and 0.67 eV for x = 0.1, 0.2 and 0.3, respectively. However, the ideality factor is also increased from 1.04 for x = 0 to 1.07, 1.12, and 1.21 for x = 0.1, 0.2 and 0.3, respectively.
2. Due to the barrier enhancement by In_{1-x}Ga_xP, the reverse leakage current is reduced from 11.4 μA for x = 0 to 9.8, 2.8, and 1.7 μA for x = 0.1, 0.2 and 0.3.

respectively. The reverse breakdown voltage is slightly increased from 12 V for InP to 15-18 V for $\text{In}_{1-x}\text{Ga}_x\text{P}/\text{InP}$ ($x = 0.1$ to 0.3).

The results of this investigation have been successfully applied in the design and fabrication of InP Schottky devices, such as MSM-PDs and HEMTs described in Chapter 5. The performance of such devices employing $\text{In}_{1-x}\text{Ga}_x\text{P}$ as barrier layer were greatly improved, in that lower dark currents (reverse leakage currents), and higher breakdown voltages were obtained.

IV. SURFACE PASSIVATION OF InP

Surface passivation of InP using sulfur solutions has been successfully conducted. The performance of such sulfur passivated InP devices is significantly improved. Results are summarized below:

The best conditions for InP surface passivation are found to be: solution of $(\text{NH}_4)_2\text{S}_x$:DI $\text{H}_2\text{O} = 1:15$, temperature = 60°C , passivation time = 20 minutes. 600 W tungsten light illumination is required for best performance.

Applications of sulfur passivation to InP and InGaAs devices, such as Schottky diodes, MIS diodes, and InP and InGaAs MSM-PDs, show that

- 1) Surface recombination velocity was reduced due to the reduction in surface state density;
- 2) Schottky barrier height was slightly increased, and therefore the dark current was reduced;
- 3) Capacitance was slightly reduced, and was found to be less frequency dependent

due to the reduction of interface states;

- 4) Performance of InP devices are more consistent from device to device after sulfur passivation;
- 5) Photoresponse was less field-dependent due to the minimization of the field-dependent effects;
- 6) Frequency response of InP/InGaAs MSM-PDs was not affected by sulfur passivation.

This investigation shows that the $(\text{NH}_4)_2\text{S}_x$ passivation of the InP surface can effectively reduce the density of the surface states and the surface recombination velocity, therefore improve the performance of the InP devices. Results on InP/InGaAs MSM photodetectors were presented in Chapter 5.

V. InP/InGaAs/InP MSM PHOTODETECTORS

InGaAs MSM-PDs using InP as the barrier enhancement layer were fabricated and characterized. The device is completely depleted at a bias of 2.5 - 3.0 V. The capacitance of a “2×2” device under full depletion is about 150 fF, which is equivalent to the RC charging time of 7.5 ps for a 50 Ω load. The carrier transit time in such a device is about 20 ps. It is obvious that the speed of the MSM-PDs is limited by the carrier transport between the electrodes rather than by the RC charging time. The dark current at 10V is about 400 nA and the breakdown voltage is about 12 - 15V. Unlike avalanche photodetectors (APD), the “soft” breakdown characteristics in the MSM-PDs is caused by the field-assisted tunneling. The breakdown voltage shows a linear decrease as the

temperature is increased while it shows an opposite tendency in the APDs. The responsivity obtained ranges from 0.4 A/W to 0.75A/W, depending on the device structure and the fabrication processes. A FWHM of 15 ps for a "2×2" device was obtained from its temporal response, very close to the value of 16.7 ps calculated from the transit time limited model. Fourier transform of the temporal response shows that the 3 dB cutoff frequency is about 20 GHz.

Annealing the MBE samples at 600°C for 5 seconds before fabrication results in a decrease in dark current and an increase in the responsivity of the fabricated devices due to the reduction of defects and the trap density in the MBE grown structures. Further dipping the annealed sample into HF for 20 seconds can reduce the dark current slightly while the responsivity is reduced. Mesa etch-down of the annealed sample can reduce the dark current significantly and reduce the device capacitance. The responsivity is reduced compared to that of the annealing-only device.

Sulfide passivation of the InP surface can improve the performance of the device. The device capacitance is reduced from 180 fF to 120 fF for a 2×2 MSM-PD, the dark current is reduced from 400 - 500 nA to 200 - 300nA at 10V. Although the responsivity is slightly reduced after sulfide passivation, the internal gain is minimized, and the I-V curve is more flat (less bias dependent). No significant change in the device speed performance of the passivated device was observed, which is in agreement with the transit time limited model. The improvement in the performance of the sulfide passivated MSM photodetectors is attributed to the reduction of the surface states, the increase of the effective Schottky barrier height, and the more stable In-S bonds at the device surface.

In the design of a MSM photodetector, a trade off of the speed and efficiency must be considered. The finger spacing is the major parameter that determines the detector's response speed although the thickness of the InGaAs absorption layer has some influence. while the efficiency of the MSM-PDs is determined by the absorption layer thickness and the finger spacing - to - finger width ratio. The active area does not have any significant influence provided that it is not large enough to make the capacitance very high, and therefore the RC charging time larger than the carrier transit time.

VI. SUMMARY

In summary, the conduction mechanisms in InP Schottky barriers were investigated. The departure of the current-voltage characteristics from ideal behavior can be well explained by the inhomogeneous barrier model. Systematic metallization schemes for Schottky contacts to InP were investigated and optimized. Barrier enhancement has been successfully achieved using an $\text{In}_{1-x}\text{Ga}_x\text{P}$ on the InP. The InGaAs MSM-PDs using an InP or an $\text{In}_{1-x}\text{Ga}_x\text{P}/\text{InP}$ as the barrier enhancement layer(s) were designed, fabricated and characterized. Their performance are compatible to the best reported so far for InGaAs MSM-PDs. Sulfur passivation of the InP surface was investigated and applied to the InP/InGaAs MSM-PDs. The performance of the sulfur passivated devices was greatly improved.

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8. J. Showell, Z. Pang, K. Song, P. Mascher, J. G. Simmons, and D. A. Thompson, "Design and Fabrication of High Performance InGaAs/InP High Electron Mobility Transistors (HEMTs)", Canadian Institute for Telecommunication Research Annual Meeting, Ottawa, Canada, August 1994.
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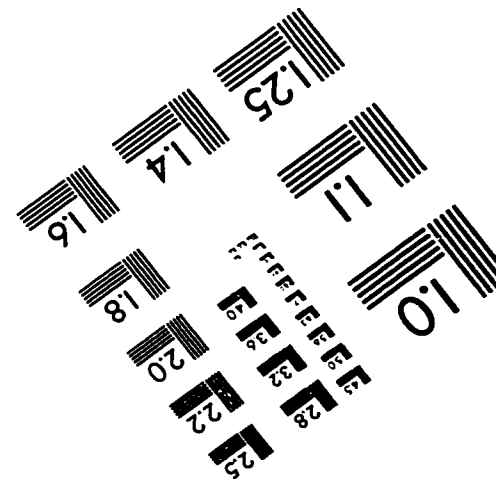
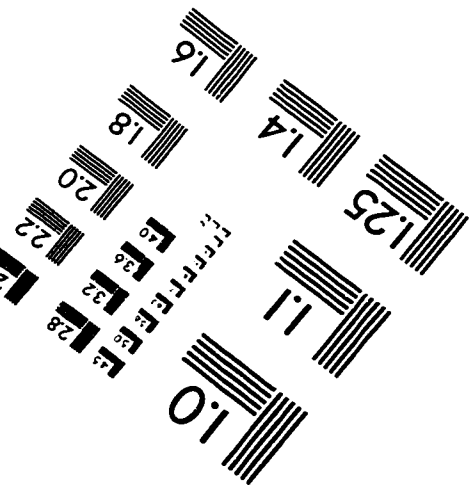
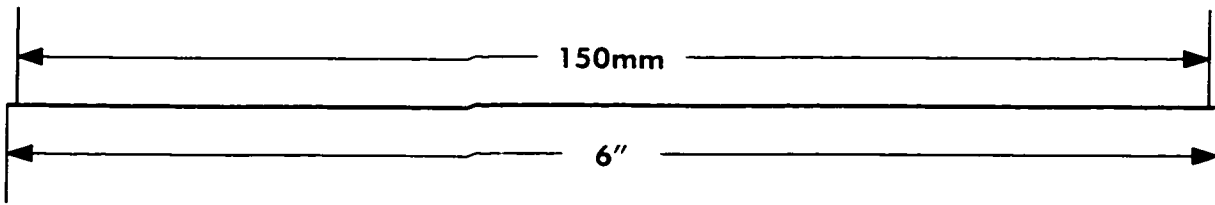
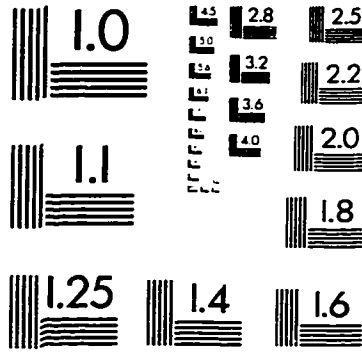
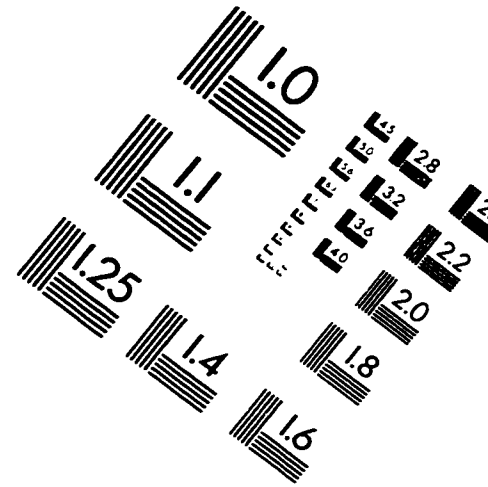
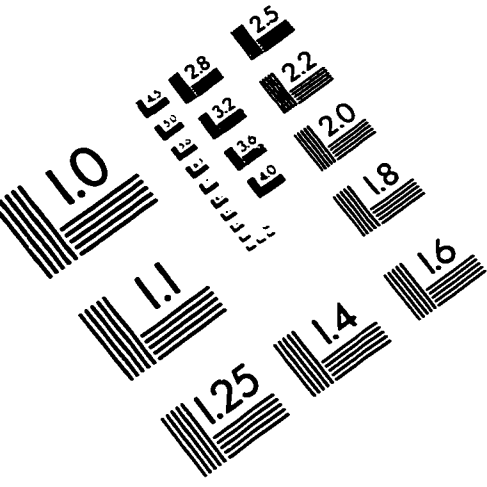
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IMAGE EVALUATION TEST TARGET (QA-3)



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