The Bistable Field Effect Transistor (BISFET):
Theory and Realization
of A Novel
Optoelectronic Switching Device

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ABSTRACT

A novel optoelectronic switching device, the bistable field effect transistor (BISFET) has been developed. The BISFET is an inversion channel heterostructure device containing a positive feedback loop transverse to the channel, between the gate and collector terminals. This leads to the existence of two distinct operating states. In one state, the feedback loop is in a high-impedance OFF state, associated with which are a large carrier population in the conduction channel and a correspondingly high drain current. In the other state, the feedback loop is in a low-impedance ON state, characterized by a small carrier population and a relatively low drain current. As the drain voltage is varied, the device undergoes abrupt changes in drain current. These transitions, referred to as switchup and switchdown, sweep out a large hysteresis loop in the drain characteristics of the BISFET, making the device strongly bistable. A mathematical model is developed to describe the operation of the device.

Implementation of the BISFET in the GaAs/AlGaAs material system is reported. A study of the electrical characteristics of the device has been carried out, using two separate device configurations. In one configuration, a separate collector terminal is used to supply feedback current in the device. In the other, known as the integral collector configuration, the source contact simultaneously serves as the collector terminal. The electrical characteristics reveal a sharp drop in gate current corresponding with that in the drain current. This confirms the feedback loop as the origin of the switching. The gate characteristics are shown to exhibit S-type negative differential resistance (NDR) associated with the

feedback loop. The transfer characteristics of the BISFET are found to contain hysteresis corresponding with that seen in the drain characteristics.

A single set of transitions is observed in the BISFET when the integral collector configuration is used. The feedback loop in this case lies between the gate and source terminals. The device has also been operated using a separate collector terminal. Two distinct sets of transitions have been observed in this mode. The previously-observed set resulting from the gate-source feedback loop (integral collector configuration) is still present. In addition to this, however, a second set of transitions is seen, which is associated with the feedback loop between the gate and the separate collector terminal.

An enhancement in drain current is reported in the BISFET at low drain voltage. This increase, seen at high gate bias, is believed to result from a geometric and electrical symmetry between the source and drain terminals at low drain voltages. The turn-off of the enhancement with increasing drain bias varies from a gradual decline at lower gate voltages to an abrupt drop at higher values.

Optical bistability in the GaAs/AlGaAs BISFET is reported. The device is found to emit light from the active region when it is in the ON state. The light output exhibits abrupt transitions and hysteresis corresponding directly with those seen in the electrical characteristics. Optical *control* of the bistability is also reported. The drain voltages at which the current transitions occur are found to change when optical excitation is applied to the device. As the optical intensity is increased, the transition voltages decrease, then saturate, then increase.

The structure and fabrication process used for the BISFET are compatible with a range of other devices, including light sources and detectors. The feasibility of constructing optoelectronic integrated circuits using the BISFET is demonstrated using a circuit consisting of an LED and a BISFET current driver.

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Dedication

To my mother - this probably means

even more to her than to me.

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2   J.J. Ojha, J.G. Simmons, R.S. Mand, and A.J. SpringThorpe, "Realization of an n-Channel GaAs/AlGaAs Bistable Field-Effect Transistor (BISFET)," *IEEE Electron Device Lett.*, vol. 14, pp. 385-387 (1993).

3   J.J. Ojha, J.G. Simmons, R.S. Mand, and A.J. SpringThorpe, "DC Electrical Characteristics of the n-Channel GaAs/AlGaAs Bistable Field Effect Transistor (BISFET)," submitted for publication, *IEEE Trans. Electron Dev.*

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CONFERENCE PRESENTATIONS

1 J.J. Ojha, J.G. Simmons, P.E. Jessop, R.S. Mand, and A.J. SpringThorpe, "Monolithic Optoelectronic Integration Using Inversion Channel Technology," Canadian Inst. for Telecomm. Research, Annual Conference, Ste.-Adele, Canada, May, 1992.

2 J.J. Ojha, A.S. Vetter, J.G. Simmons, P.E. Jessop, R.S. Mand, and A.J. SpringThorpe, "Optical Bistability in the GaAs/AlGaAs Bistable Field Effect Transistor (BISFET)," Sixth Canadian Semiconductor Technology Conference, Ottawa, Ontario, August, 1992.

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Chapter 1

INTRODUCTION

1.1 Backdrop

The development of semiconductor electronics has revolutionized modern life. It has led to the development of the computer, as well as ultrafast digital communications. The computer was originally developed as a machine to carry out large-scale numerical computation tasks - in effect, to do for mental labour what mechanical machines have done for physical labour. However, it has since evolved into a much more versatile tool, now being used for control of manufacturing systems, graphical applications, and many other industrial, commercial, and consumer uses, including the preparation of the page you are presently reading. Communication systems have likewise developed into flexible tools, allowing the transmission of not only audio signals, but text, video images, and other kinds of data around the world with the push of a few buttons.

The early uses of computing and modern communications were for research and engineering applications. As these technologies have become

cheaper, more powerful, and easier to use, they have spread rapidly into industrial and commercial uses. And now, they are generating truly mass-market products and services, which are breaking with lightning speed into the consumer marketplace.

The development of optical communications technology in the 1970's has accelerated the explosion of modern communications by making available faster and faster data transmission rates. This has led to the development of new products and services which make use of the increased transmission bandwidth that is now available, such as FAX machines, computer networks and electronic mail - the list is growing rapidly. Optical communication through glass fibers offers a number of well-known advantages over traditional electrical systems, such as vastly improved bandwidth, increased signal repeater spacing, and virtual elimination of interference, to name a few.

As communications systems and computers have evolved, they have begun to fuse into one seamless technology - "information technology." Plans are currently underway for an "information superhighway" which will combine the visual information medium of television and the switching capabilities of telephone networks, with the data handling and processing abilities of computers. The result will be a powerful, flexible new technological paradigm. It will allow services such as interactive video, direct access to financial transactions and taxation filings, as well as providing access to a vast array of information services to the average consumer. Among other things, this is expected to lead to greater efficiency in the day-to-day business of human society, requiring less manpower to carry out routine transactions, and less paper to be used in the distribution of information.

The result of all this is no less than a transformation and reorganization of

society comparable in magnitude to the agricultural and industrial revolutions. It will entail a vast reallocation of human resources, leading to a massive economic restructuring. This restructuring is already underway, and is largely responsible for the socio-economic upheaval which has characterized the 1990's to date. Is the information superhighway really coming? Most certainly. Part of the reason for the high cost of rebuilding eastern Germany after the reunification of that country is that billions of extra dollars are being spent to make provisions for the technologies of the future, rather than opting for yesterday's less expensive methods. While the rest of the world is just beginning to build the infrastructure required, Germany will have some twenty million people optically wired for the information society of the twenty-first century. France has had a nation-wide computerized public information system for years. This system, known as Minitel, has terminals in many public places, and offers over 12,000 individual information services. Canada has had its own (premature) experiment with a public information system in the 1980's in the form of the Telidon network.

The rapid evolution of information technology will continue well into the 21st century, and perhaps into the 22nd. With the development of other advanced technologies, such as virtual reality, short-haul wireless communications, neural networks, and semiconductor micro-motors, the pace of change and the power of the information tools available to us should continue to increase. As remarkable as the progress to date has been in computing and communications technology, still more remarkable is the fact that the information revolution has just begun.

1.2 Development of Technology to Date

Semiconductor electronics was effectively born with the invention of the

bipolar junction transistor (BJT) by Bardeen, Brattain, and Shockley in 1948 [1],[2]. This was followed by a number of other developments, including the realization of the junction field effect transistor (JFET) [3], the metal-semiconductor field effect transistor (MESFET) [4], and the metal-oxide-semiconductor field effect transistor (MOSFET) [5]. In 1962, semiconductor heterostructures were first implemented [6], paving the way for bandgap engineering. This permits the design of semiconductor structures having a desired energy band profile, allowing a wide range of new devices to be realized. The use of heterostructures has been applied to transistor design in the form of the heterostructure bipolar transistor (HBT) [7],[8] and the high-electron-mobility transistor (HEMT), also known as the modulation-doped field effect transistor (MODFET) [9]. The latter makes use of an inversion channel formed at a heterointerface, which contains a two-dimensional electron gas (2-DEG). This allows high-speed carrier transport between the source and drain.

The development of semiconductor technology has not been restricted to electronic devices. In 1962, the semiconductor laser was developed [10], extending the field into the realm of optical devices. Heterostructures were incorporated into the semiconductor laser in 1969 [11], opening the way for dramatic increases in efficiency of operation.

The development of optical communications, together with the fusion of computing and communications, has led to an interest in optoelectronic devices and circuits for switching, signal processing, and logic applications. Such applications have attracted particular interest because of the limitations on switching speed placed on traditional electronics by resistive and capacitive effects. Optoelectronic devices and circuits hold the potential for greater speeds, since they can sometimes be designed so that *photon* transport and decay are the

limiting processes. If optical interconnection of devices and semiconductor chips can be achieved, a significant bottleneck will have been overcome, allowing a dramatic increase in the operational bandwidth of systems. Thus, there is an impetus towards achieving optoelectronic integrated circuits (OEIC's), which would allow full use to be made of the bandwidth offered by optoelectronics.

In particular, there is an interest in bistable optoelectronic devices, as these have a variety of uses in switching and logic applications. A bistable device is one which has two distinct operating states [12]. It is characterized by hysteresis in its output characteristics, making the two operating states stable against minor variations in input. In electronics, an example of a bistable device is the thyristor, which is used as a power switching device [13]. It displays S-type negative differential resistance (NDR) in its current-voltage (I-V) characteristics. A number of bistable optoelectonic devices have been explored, such as the bistable Fabry-Perot etalon [12] and the self-electro-optic effect device (SEED) [14].

Another bistable optoelectronic device which has been developed is the double-heterostructure optoelectronic switch (DOES) [15-20]. This is an inversion channel device which combines attributes of inversion channel devices (HEMT) and bistable devices (thyristor). It exhibits electrical characteristics similar to the thyristor. However, it replaces the gate layer in the latter with a thin (≈ 50 Å), highly doped charge sheet. This charge sheet induces an inversion channel, which can be used to control the state of the device. The DOES can also be controlled by applying an optical input to it [21]. When implemented in the GaAs/AlGaAs material system, it generates an optical output roughly proportional to the current flowing in the device [22]. The DOES thus exhibits electrical and optical bistability, both of which can be controlled by either an electrical or an optical input signal. This makes it an interesting candidate for optoelectronic

integration. The DOES has also been implemented in the Si/SiGe [23],[24] and InP/InGaAsP [25] material systems.

A number of other devices have been implemented using the same inversion channel heterostructure as the DOES. The bipolar inversion channel field effect transistor (BICFET) is a bipolar transistor in which the base is replaced by the inversion channel [26]-[30]. The heterojunction field effect transistor (HFET) is a FET which uses the inversion channel for high-mobility conduction from source to drain [31]-[35], much as in the HEMT. Use of an HFET as a photodetector has been demonstrated [36]. Inversion channel lasers have also been achieved [37]-[39]. The mutual compatibility of these devices with regard to the semiconductor structure and fabrication process, together with the fact that it can be used as an optical source or detector, makes this inversion-channel technology potentially useful in implementing OEIC's [40]-[42].

1.3   Scope of This Work

In this thesis, a new inversion channel optoelectronic switching device, the bistable field effect transistor (BISFET), is developed. This device exhibits both electrical and optical bistability. The BISFET is compatible with the other inversion channel devices described above in both structure and fabrication procedure.

In Chapter 2, the theory of operation of the BISFET is presented. The BISFET incorporates a $p\delta npn$ positive feedback loop between the gate and a terminal referred to as the collector, leading to abrupt transitions and bistability in the output characteristics. In Chapter 3, the electrical characteristics of an n-

channel GaAs/AlGaAs BISFET are presented for operation in what is referred to as the integral collector mode. In this mode, the device structure is simplified by utilizing the source contact as a combined source and collector terminal. Chapter 4 deals with the electrical characteristics in the separate collector mode, in which the source and collector terminals are separated.

In Chapter 5, it is shown that the GaAs/AlGaAs BISFET produces an optical output signal, which exhibits bistability corresponding with that seen in the electrical characteristics. In Chapter 6, the device is shown to respond to an optical input signal, thus offering bistable electrical and optical outputs, both of which can be controlled by either an electrical or an optical input signal. Practical application of the BISFET is explored in Chapter 7. It is demonstrated that the GaAs/AlGaAs BISFET can be integrated with a light-emitting device (LED) on a single substrate, using a single fabrication sequence. Chapter 8 concludes with a summary of the work undertaken and proposals for further advances to the technology.

The capabilities of the BISFET make it a potentially powerful component for optoelectronic integration and logic applications. Its compatibility with a range of other electronic and optoelectronic devices means that a range of functions can be implemented on a single chip. The fact that it produces an optical output allows it to be optically cascaded with more BISFET's or other devices. Since the interconnections between devices would thus be optical, the result would be a potentially very fast OEIC capable of performing switching and logic functions.

Chapter 2

DESCRIPTION AND THEORY

OF THE BISFET

2.1 Generalized Design of the BISFET

The BISFET consists of a $p\delta npn$ (n-channel) or $n\delta pnp$ (p-channel) semiconductor structure. The present discussion will focus on the n-channel version, as this is the structure used to implement the devices used in this work. The generalized epitaxial layer structure of the BISFET is shown in Fig. 2.1. The corresponding equilibrium energy band diagram for a cross-section through the wafer is shown in Fig. 2.2. The layer structure is similar to that of the HFET [4], but with the addition of a collector to the back of the device. The first layer (at the surface of the wafer) is a p-type gate region formed from a wide-bandgap semiconductor (WBGS). It will be shown in this chapter that the gate terminal controls the charge in the inversion channel of the device via this gate layer. The gate terminal itself consists of an ohmic contact to the gate layer at the surface of the semiconductor. It is important to note that this contact must be ohmic rather than insulating, since the gate current plays a crucial role in the operation of the device.

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gate	WBGS	p
charge sheet	WBGS	n^+
active layer	NBGS	p
collector	WBGS	n
substrate	NBGS	n

Figure 2.1   Layer structure of the n-channel BISFET, showing wide- and narrow-bandgap semiconductor regions (WBGS and NBGS, respectively). The name of each layer is indicated at left, followed by the type of semiconductor and dopant type.

The next layer in the structure is a delta-doped n-type charge sheet. This is typically very thin - on the order of 50 Å. This layer is roughly comparable to the gate layer in the thyristor. The charge sheet is designed to be fully depleted of carriers under normal conditions. For present purposes, the thickness of the charge sheet may be neglected. Thus, the bending of the energy bands within the charge sheet layer may also be ignored, simplifying the energy band diagram. This is illustrated in the simplified equilibrium band diagram of Fig 2.3(a).

The charge sheet depletes a portion of the p-type semiconductor regions adjacent to it. In the process of doing so, it induces an inversion channel at the interface with the following layer, the active region of the device. The inversion channel serves much the same role as that in the HEMT - it provides a high-mobility
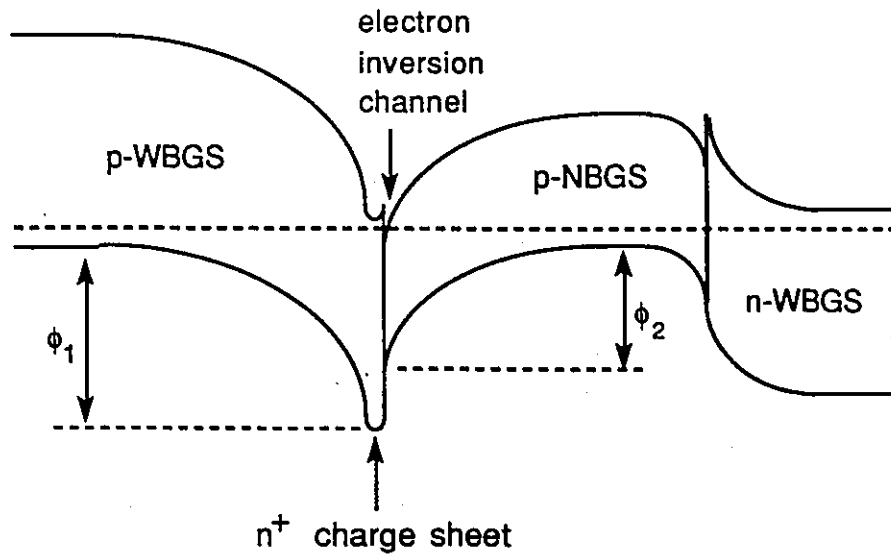
Figure 2.2   Energy band diagram of the n-channel BISFET, showing
bending of energy bands at the charge sheet. WBGS and
NBGS denote wide- and narrow-bandgap semiconductor
regions, respectively

conduction channel for carrier flow between the source and drain. This channel in

the conduction band is accompanied by a potential barrier in the valence band.

When the device is electrically biased, the barrier controls the injection of holes

from the gate into the active region, which is described below. Its height varies

with position along the channel, having a direct correspondence with the channel

potential itself.

The active region consists of a *p*-type layer of narrow-bandgap

semiconductor (NBGS). The portion of the active region immediately adjacent to

the channel is depleted by the charge sheet. The band bending associated with this

depletion region serves to bound the inversion channel on the side opposite the
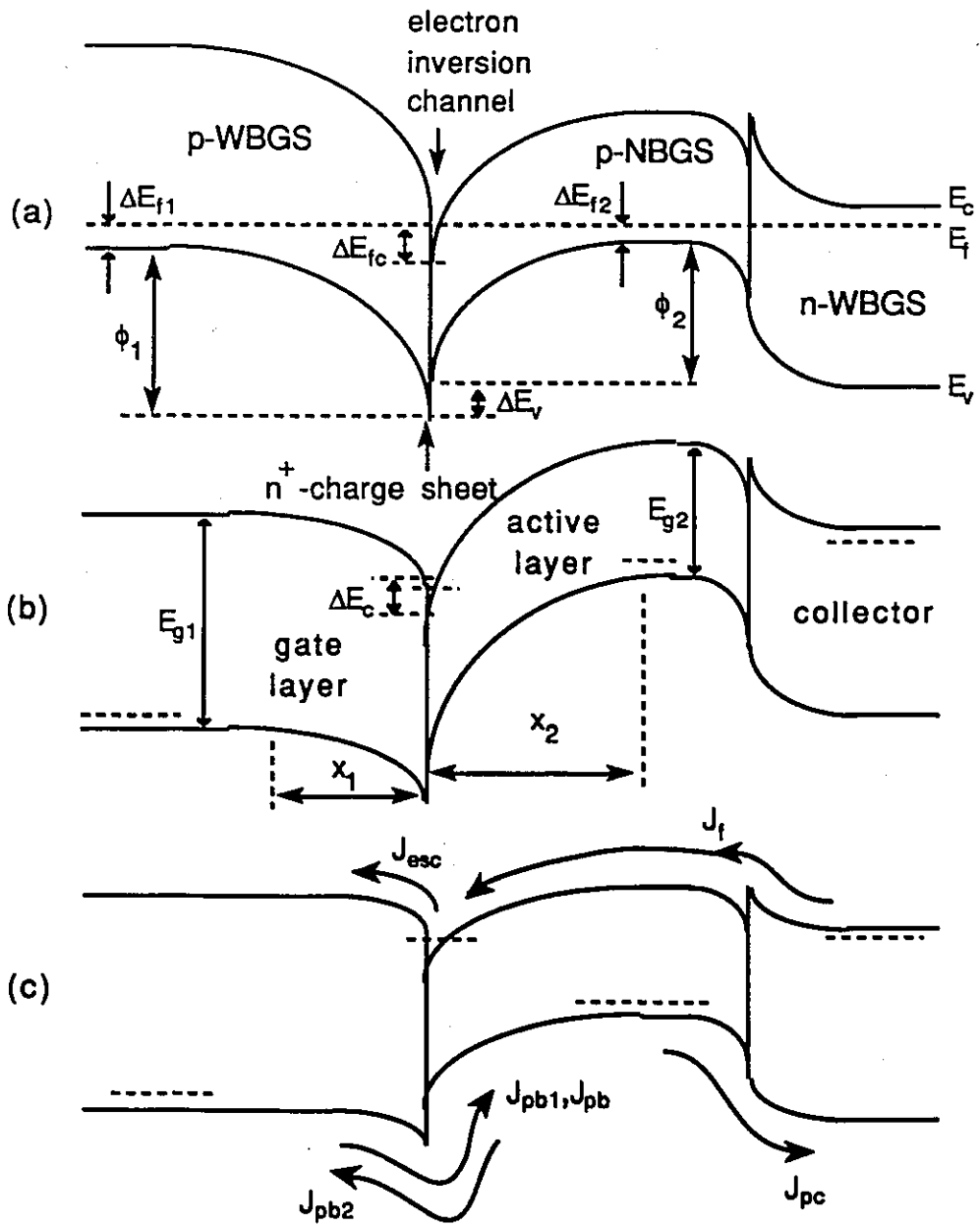
Figure 2.3   Energy band diagram through BISFET with charge sheet
            assumed to have infinitesimal thickness, so that bending
            of energy bands within region of charge sheet may be
            neglected. The band diagram is shown (a) at equilibrium,
            (b) in the OFF state, and (c) in the ON state. The
            quantities of interest in this discussion are defined in the
            diagram.

charge sheet. The hetero-offset, or discontinuity in the energy bands, between the active region on the one hand, and the charge sheet and gate layer on the other, provides additional confinement for electrons in the inversion channel. The active region plays an important role in the operation of the BISFET. Its potential changes abruptly as the device switches state. This potential serves to control the injection of feedback current from the collector or source of the device into the channel. The active layer is also the site of radiant recombination in the GaAs/AlGaAs BISFET. The final layer in the structure is the n-type WBGS collector. This layer serves two purposes. The first is to provide some measure of confinement for carriers in the active region. The second is to inject feedback current into the inversion channel via the active region.

The potential drops, ϕ_1 and ϕ_2, are defined in Fig. 2.3. These occur across the depletion regions adjacent to the charge sheet in the gate and active layers, respectively. The physical structure of the BISFET is shown in Fig. 2.4. An ohmic contact is made to the gate layer, as discussed above, to form the gate terminal of the device. Ohmic contacts are also made to the channel to serve as source and drain terminals. The latter are formed by ion implantation.

2.2 Mathematical Model: Statement of Problem

The BISFET represents a very complex modelling problem. There are two perpendicular directions of current flow in the device - one along the conduction channel and one transverse to it. The behaviour of the device stems from a strong coupling between these two mutually perpendicular current flows. Furthermore, each of these current flows undergoes abrupt changes in magnitude. Additional

Source (gnd)   gate (+)   drain (+)

p-WBGS
(gate layer)

n⁺⁺   n⁺⁺

n⁺-WBGS
(charge sheet)

feedback path
with integral
source and collector

p-NBGS
(active region)

feedback path
with separate
collector

n-WBGS Collector

collector (-)
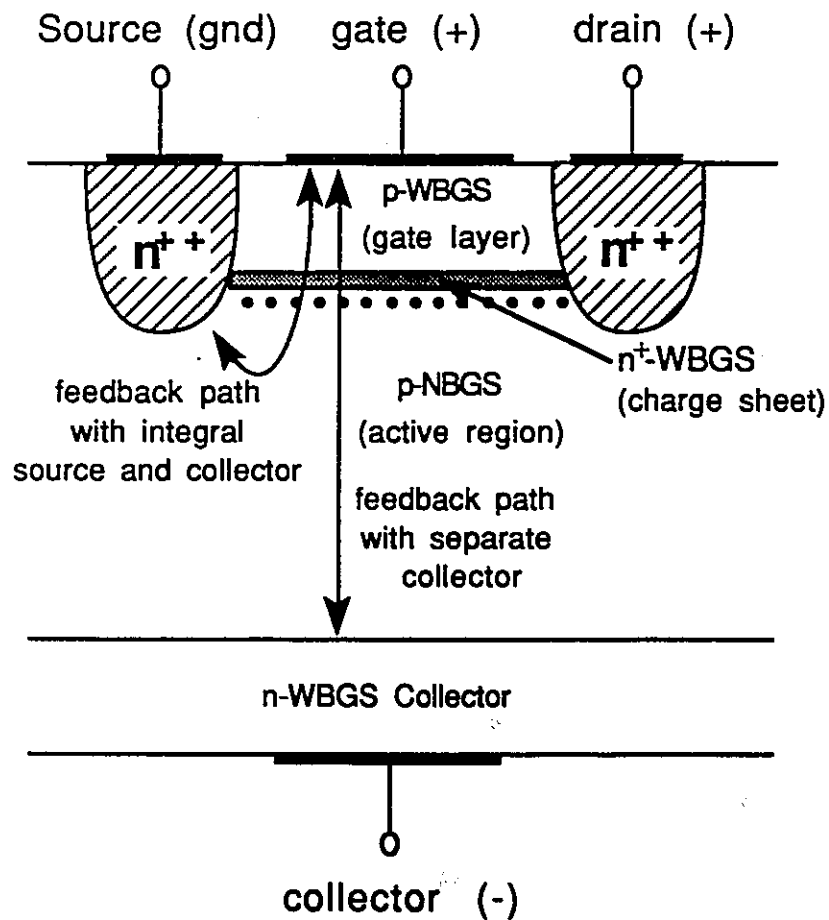
Figure 2.4   Physical structure of the BISFET, showing the various
layers and terminals, as well as the polarities of the bias
voltages applied to the latter.

complications arise because lateral potential variations play a critical role in the

switching process. Thus, an ideal model would be a fully two-dimensional one,

with current flows parallel and transverse to the channel being treated in a fully

integral fashion, rather than being artificially decoupled. However, the complexity

of the problem and the discontinuities evident in the behaviour of the device make it

far from clear that a satisfactory, truly two-dimensional model of the BISFET can be constructed and solved.

Thus, a number of simplifying assumptions are made to arrive at a model which illustrates the mechanisms influencing the operation of the device. The task is further simplified by developing the model for the simplest geometric configuration of the BISFET - that containing a separate collector, rather than an integral source-collector contact. Thus, the feedback loop is not folded back on itself, and further simplifying assumptions may be made, as outlined below. The various configurations of the BISFET are explained in more detail at a later point, and their implications for the model will become evident as the discussion proceeds.

2.3 Simplifying Assumptions

The first major assumption which is made in modelling the BISFET is that the current components parallel and transverse to the conduction channel are substantially de-coupled, and can hence be partially separated mathematically. Thus, one set of equations has been developed to describe the operation of the feedback loop, while a second has been formulated to describe the current flow along the channel. In practice, of course, the interaction of these current components is central to the operation of the device. Thus, a complete decoupling is not possible without introducing arbitrary constraints on the switching mechanism. A linkage between the two sets of equations is thus maintained via the feedback current emanating from the collector. This current appears in both sets of equations, and solution of the mathematical model developed here would require that the two sets of current equations be made mutually self-consistent with respect

to the feedback current.

Subsidiary to the above considerations, it is assumed that the active region serves to effectively separate the *p-n* junction formed by the active region and the collector from the conduction channel and associated potential barrier, with regard to lateral variation of the current. In other words, it is assumed that the active-collector junction (henceforth referred to as the *p-n* junction) is shielded by the active region from any lateral variation in current at the barrier and channel (i.e., variation along the direction of the channel). Thus, the current flow across the *p-n* junction is taken as being uniform over its cross-section. This assumption is justified if the active region is not punched through, since it then contains a non-depleted neutral region which allows the current from the barrier to the active region to establish lateral uniformity before flowing into the collector. Thus, since the active region in the device structure studied here is quite large (1 μm), it is justifiable to assume that the current flow from the active region to the collector is spatially uniform.

Similarly, it is assumed for simplicity that any feedback current injected by the collector finds its way into the conduction channel without being laterally deflected by potential variations within the device. In other words, the feedback current is injected uniformly into the channel from the collector via the active region.

With these assumptions in mind, let us now construct a model for the operation of the n-channel BISFET. The operation of the feedback loop is first described, and the equations governing its steady-state operation are developed. The effects of applying a drain bias are then discussed. Finally, the equations describing the current flow along the conduction channel are developed, and the relationship between these and the feedback equations is established.

2.4 Equilibrium Relationships

Before going on to discuss the operation of the feeedback loop and the drain characteristics of the BISFET, the equilibrium relationships describing the device must first be established. In this section, the relationships governing the electric charge, the Fermi levels, and the barrier potentials are developed with no bias applied to any of the terminals of the BISFET.

2.4.1 Charge Balance Relationships

The height of the potential barrier associated with the conduction channel is central to the behaviour of the feedback loop, and hence, the device as a whole. This height, in turn, depends on the balance of charge amongst the space charge regions surrounding the channel and the free carriers in the channel itself. Application of Poisson's equation in one dimension (transverse to the channel) dictates that the net electrical charge between the neutral portions of the gate and active layers must sum to zero. Thus,

$$Q_s + Q_1 + Q_2 + Q_{ch} = 0 \qquad (2.1)$$

where Q_s is the positive space charge associated with the fully-depleted charge sheet; Q_1 and Q_2 are the negative space charges stored in the depletion regions in the gate (also referred to as the barrier layer) and the active region, respectively; and Q_{ch} is the negative charge associated with the free carriers in the conduction channel.

Using the depletion approximation, Q_1 and Q_2 are given by

$$Q_1 = \left[2q\varepsilon_1 N_1 \phi_1\right]^{1/2}$$
$$Q_2 = \left[2q\varepsilon_2 N_2 \phi_2\right]^{1/2} \qquad (2.2)$$

where q is the magnitude of the electronic charge. ϕ_1 and ϕ_2 are the electric potentials in the gate and active regions, shown in Fig. 2.3. N_1 and N_2 are the three-dimensional doping densities in the gate and active layers, while ε_1 and ε_2 are the dielectric permittivities of the semiconductor in the two regions.

The charge in the conduction channel, Q_{ch}, is given by

$$Q_{ch} = qN_{ch} \qquad (2.3)$$

The charge sheet is assumed to be fully depleted, so the space charge, Q_s, associated with it is given by

$$Q_s = qN_s \qquad (2.4)$$

where N_s is the two-dimensional doping density in the charge sheet.

It is apparent from Eq. 2.1 that when the depletion space charges (and accompanying potentials) are large, the charge in the conduction channel is relatively small. Conversely, when the depletion charges are small, the channel charge is correspondingly large. The significance of this charge relationship becomes apparent in the discussion that follows.

2.4.2 Fermi-Level Relationships and Barrier Potentials

The charge balance relationships of Section 2.4.1 cannot be solved without determining the barrier potentials ϕ_1 and ϕ_2. Therefore, a second set of relationships governing ϕ_1 and ϕ_2 is required. These can be found by matching the Fermi levels in the gate, channel, and active region. At equilibrium, the Fermi levels in the gate and channel must align with each other, as shown in Fig. 2.3(a). Thus,

$$\Delta E_{f1} + \phi_1 = \Delta E_v + E_{g2} + \Delta E_{fc} \tag{2.5}$$

where ΔE_{f1} is the energy difference between the valence band edge and the Fermi level in the gate region. ΔE_{fc} is the difference between the conduction band edge and the Fermi level in the channel, taken as being degenerate (i.e., the Fermi level lies above the conduction band edge). ΔE_c is the energy offset between the conduction band edges in the gate and active regions. E_{g2} is the bandgap energy in the active region. The various energies and energy differences are illustrated in Fig. 2.3.

Similarly, the Fermi levels in the channel and active region are aligned at equilibrium:

$$\Delta E_{f2} + \phi_2 = \Delta E_{fc} + E_{g2} \tag{2.6}$$

where ΔE_{f2} is the energy difference between the conduction band edge and the Fermi level in the active region.

2.5   Operation of the Feedback Loop

As described above, the BISFET contains a *pδnpn* sequence between the gate and collector layers. This is readily apparent in Figs. 2.1-2.4. This sequence constitutes a positive feedback loop, the theory of which has been developed in detail elsewhere [43]. In this section, a description of the essential principles of operation of the feedback loop is presented as it relates to the BISFET. The gate is also referred to as the emitter in the context of the feedback loop.

2.5.1   Biasing of the BISFET

The polarities of the various bias voltages applied to the BISFET are indicated in Fig. 2.4. In normal operation, all voltages are applied relative to the source terminal, which is grounded. The gate terminal is supplied with a positive voltage, forward biasing the potential barrier ϕ_l and inducing a charge in the conduction channel. A negative voltage is applied to the collector, forward biasing it with respect to the active region and causing it to inject electron feedback current into the latter, as discussed below. Since we are dealing with an n-channel device, the drain terminal is positively biased, causing electrons to flow along the conduction channel into the drain contact.

In describing the operation of the feedback loop, it is assumed that *no bias is applied to the drain terminal relative to the source*, so that the electric potential is essentially constant along the conduction channel. The effects of applying a drain voltage are considered later.

2.5.2 Charge and Fermi-Level Relationships

When a bias voltage V_{gc} is applied to the feedback loop, the device is no longer in equilibrium, but in steady state. The corresponding energy band diagram through the structure is shown in Figs. 2.3(b) and (c). The charge balance relationships developed in Section 2.4.1 under equilibrium conditions continue to apply, so that Eqs. 2.1-2.4 still hold. However, the Fermi-level relationships of Section 2.4.2 must be modified. Equation 2.5 must be rewritten to reflect the fact that the Fermi levels are no longer aligned. Thus,

$$\Delta E_{f1} + \phi_2 = \Delta E_c + E_{g2} + \Delta E_{fc} + V_{gs} \tag{2.7}$$

Here, V_{gs} is the potential of the gate relative to the conduction channel.

Similarly, under bias Eq. 2.6 becomes

$$\Delta E_{f2} + \phi_2 + V_j + V_{cs} = \Delta E_{fc} + E_{g2} \tag{2.8}$$

where V_j is the bias voltage which develops across the *p-n* junction formed by the active region and the collector, given in Eq. 2.13 of Section 2.5.4, and defined as being positive for forward bias. V_{cs} is the collector voltage relative to the channel.

2.5.3 Barrier Potentials and Currents

Let us now consider the components of current flow over the potential barrier, as these determine the state of the feedback loop. The various current flows described below are illustrated in Fig. 2.3.

With no drain-source bias applied, there is a thermionically emitted hole current over the barrier from the gate. The current per unit area, J_{pb1}, is given by

$$J_{pb1} = qN_1 v_{th} e^{-\phi_1/V_t} \tag{2.9}$$

where v_{th} is the thermal velocity of the carriers in the semiconductor. V_t is the thermal voltage, given by

$$V_t = \frac{kT}{q} \tag{2.10}$$

where T is the temperature, and k is the Boltzmann constant.

There is also a component of hole flow J_{pb2} in the opposite direction, from the active region to the gate, which is given by

$$J_{pb2} = qN_2 v_{th} e^{-\phi_2/V_t} \tag{2.11}$$

The net hole current, J_{pb}, from the gate to the active region is given by

$$J_{pb} = J_{pb1} - J_{pb2} \tag{2.12}$$

At equilibrium (no bias applied to the system), J_{pb1} and J_{pb2} are equal in magnitude. Thus, $J_{pb} = 0$, that is, there is no net hole flow past the barrier. When a gate bias is applied, however, this balance is disturbed. Applying a gate voltage to the device reduces the barrier height ϕ_1, causing a rapid increase in J_{pb1}, as indicated by Eq. 2.9. A net hole current thus flows over the barrier from the gate to

the active region.   After the initial increase, J_{pb} increases approximately exponentially with the gate voltage.

2.5.4 Active Region Potential and Feedback Current

The net hole current from the gate into the active region accumulates in the latter, causing an electric potential to develop in the active region. This serves to apply a bias to the *p-n* junction, allowing a hole current J_{pc} (shown in Fig. 2.3) to flow into the collector. The *p-n* junction potential, V_j, is given by

$$V_j = V_T \, ln\left[1 + \frac{J_{pc} + J_f}{J_s} \right]$$

(2.13)

where J_s is the total (electron and hole) reverse saturation current [44]. When the feedback loop is off, both the gate and collector currents are small, resulting in a small potential in the active region (relative to the collector, or alternatively, the channel). However, when the loop is on, substantial current flows along this path, leading to a significant active-region potential. This change in potential in the active region plays a critical role in the operation of the BISFET by helping, together with the barrier potential, to regulate the current in the feedback loop. Under steady state conditions, the total hole current per unit gate width, I_{pb}, entering the active region from the gate must equal the hole flow from the active region into the collector, I_{pc}. Thus, for conditions of interest in this discussion,

$$I_{pc} = I_{pb}$$

(2.14)

I_{pc} and I_{pb} may be found by integrating the respective current densities along the conduction channel, and are given by

$$I_{pc} = \int_0^l J_{pc} dx = J_{pc} l$$

$$I_{pb} = \int_0^l J_{pb} dx = J_{pb} l$$

(2.15)

where l is the gate length of the device, i.e., the length of the channel from source to drain, and x is the distance along the channel from the source towards the drain. The bias on the p-n junction causes an electron feedback current, J_f, to flow from the collector into the active region. This current, shown in Fig. 2.3, can be approximately related to J_{pc} via the doping levels on the two sides of the junction:

$$J_f = \frac{N_3}{N_2} J_{pc}$$

(2.16)

Thus, we have obtained an expression relating the feedback current (which ultimately enters the conduction channel) to the hole current through the collector, which in turn is equal to the hole current from the gate to the active region.

2.5.5 Gate-Collector Characteristic

Having established the charge balance and barrier current relationships, let us now consider the electrical characteristic of the feedback loop from gate to collector. As before, it is assumed that no source-drain voltage is applied to the
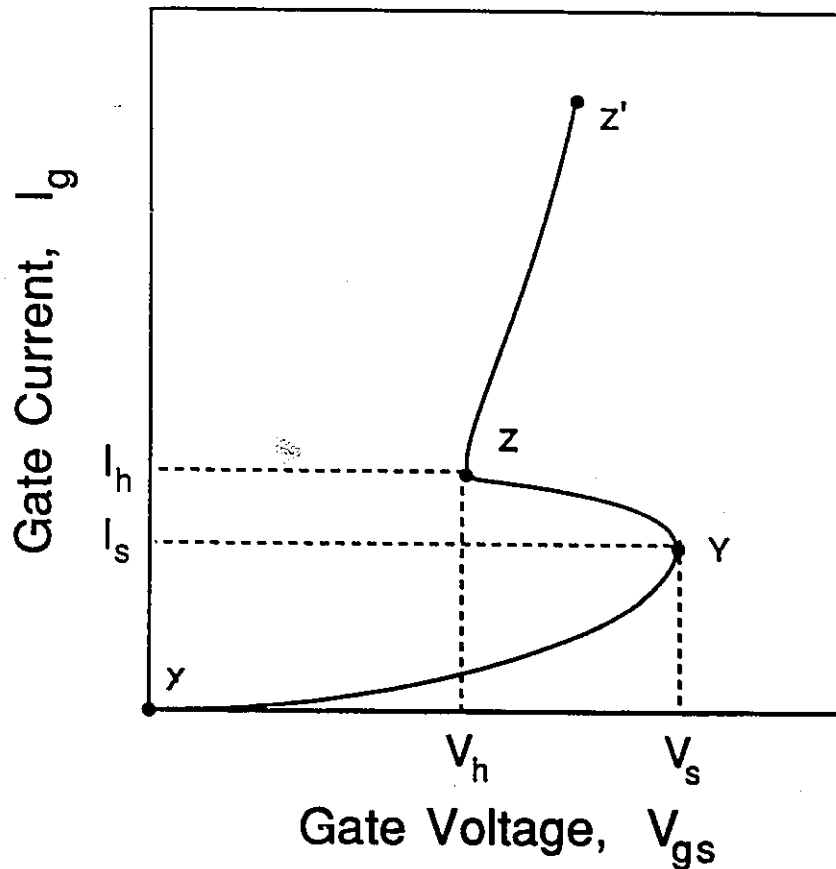
Figure 2.5   Schematic of the gate-collector characteristic of a BISFET, showing the gate current, I_g, as a function of the gate-collector voltage, V_{gc}. The switching point Y is indicated by the voltage and current V_s and I_s, while the holding point Z is indicated by V_h and I_h. The segment YZ is a region of negative differential resistance (NDR).

BISFET, so the electric potential is constant along the conduction channel. A schematic of the gate-collector characteristic, showing the gate current, I_g, as a function of the gate-collector voltage, V_{gc}, is shown in Fig. 2.5. When no gate-collector voltage is applied to the feedback loop, the equilibrium band diagram shown in Fig. 2.3(a) pertains. The current components J_{pb1} and J_{pb2}, given by

Eqs. 2.9 and 2.11 and shown in Fig. 2.3, are equal, so there is no net hole flow over the potential barrier.

As V_{gc} is increased from zero, the gate junction is progressively forward biased, and the hole flow from the gate to the active layer increases exponentially, as described in Section 2.5.3. This results in accumulation of holes in the active region, which forward-biases the *p-n* junction formed by the active region and the collector. An electron feedback current, J_f, given by Eq. 2.16, thus flows from the collector, through the active region, and into the conduction channel at the interface between the gate and active regions. This in turn tends to further forward bias the gate junction and reduce the charge sheet barrier, ϕ_1, causing an incremental hole current J_{pb}' to flow from the gate, hence completing the positive feedback loop between the gate and collector. The roundtrip differential gain of the feedback loop, G_f, is given by

$$G_f = \frac{J_{pb}'}{J_{pb}} \tag{2.17}$$

For low gate bias, ϕ_1 is still relatively large, so very little hole current is able to flow from the gate past the potential barrier associated with the charge sheet. The *p-n* junction formed by the active region and the collector layer is thus only weakly forward biased. Only a small feedback current diffuses from the collector to the active region. The feedback is non-regenerative; in other words, $G_f < 1$, and the incremental current becomes smaller with each successive trip around the loop. The feedback loop is thus in a high-impedance OFF state, characterized by very little current flow and a relatively large potential drop, ϕ_2. The corresponding portion of the gate characteristic is shown in Fig. 2.5 as segment XY. The energy band

diagram describing the OFF-state, shown in Fig. 2.3(b), now applies. The voltage applied across the loop is shared amongst the active-collector junction and the two barrier potentials, ϕ_1 and ϕ_2. The result is to forward bias the barrier in the gate, while reverse biasing that in the active region. The potential ϕ_1 is thus somewhat smaller than at equilibrium. However, ϕ_2 is substantially larger than at equilibrium. Thus, Q_1 is reduced, and Q_2 increased, compared with equilibrium. The total depletion space charge, Q_1+Q_2, is still relatively large.

As V_{gc} is increased further, the current flowing past the potential barrier continues to rise exponentially, and the differential gain of the feedback loop increases. When the switching point Y is reached, defined by the voltage V_s and current I_s, the feedback becomes regenerative, i.e., G_f exceeds unity. The depletion layer in the active region adjacent to the inversion channel begins to collapse, together with the associated potential drop ϕ_2. The voltage across the feedback loop, V_{gc}, cannot increase further without leading to an uncontrolled, discontinuous increase in I_g. For a continuous increase in current, V_{gc} must actually begin to fall once more. The device therefore enters a region of S-type negative differential resistance, shown as segment YZ in Fig. 2.5. When the holding point Z is reached, defined by the voltage V_h and current I_h, the device enters the low-impedance ON state, indicated by segment ZZ'. In this state, the current flowing in the feedback loop increases rapidly with relatively little change in the voltage V_{gc}. The energy band diagram corresponding to the ON state is shown in Fig. 2.3(c). The barrier potentials ϕ_1 and ϕ_2 are both significantly smaller than in either the equilibrium or OFF states. The space charges Q_1 and Q_2 are therefore comparatively small. The total space charge, Q_1+Q_2, is similarly reduced.

In summary, when the feedback loop is in the high-impedance OFF state,

the space charge in the active-region depletion layer is relatively large. According to Eq. 2.1, Q_{ch}, the charge in the inversion channel, must be correspondingly small. Conversely, in the low-impedance ON state, Q_1 and Q_2 are relatively small, while Q_{ch} is correspondingly large. Thus, the conductivity of the channel is distinctly higher in the ON than in the OFF state.

2.5.6 Constrained Feedback Loop

In practice, the feedback loop in the BISFET operates in a manner somewhat different from the more traditional way described above. The preceding discussion assumes that a voltage is applied across the feedback loop from the gate to the collector, with the potentials of the channel and the active region being free to find their own levels. In fact, the source of the BISFET is grounded, and the gate is biased by applying a voltage relative not to the collector, but to the source. The collector is then biased relative to the source as well, thus indirectly establishing the gate-collector voltage. The feedback loop therefore has an additional constraint placed upon it. Rather than the channel and active region potentials both being allowed to vary freely, only the latter can do so. Thus, the potentials of the gate, the collector, and the end of the channel are externally determined. The active region potential, however, is allowed to find its own level, and this will undergo substantial changes as the feedback loop switches between the ON and OFF states. In effect, one degree of freedom has been removed from the system.

The equations developed in the preceding subsections describe the constrained feedback loop in the BISFET as well as the conventional one described elsewhere. However, in the conventional feedback loop, V_{gs} and V_{cs} in Eqs. 2.7 and 2.8 are free to vary with the source potential, while in the constrained loop,

they are externally imposed. The voltage V_j, given by Eq. 2.13, is the free variable of interest. As mentioned above, it undergoes substantial changes as the loop changes state.

2.6 Effects of Drain Voltage

2.6.1 Variation of Energy Bands Parallel to Channel

Let us now consider the effects of applying a drain voltage to the BISFET. So far, the energy bands and the electrical potential in the device have been assumed to vary only in the direction perpendicular to the conduction channel, i.e., transverse to the plane of the device. They have been taken as being uniform in the plane. Applying a voltage to the drain relative to the source removes the in-plane electrical symmetry. This has a number of important consequences, which are discussed below. It is to be noted that in the n-channel device, the drain-source voltage applied is positive.

Application of a drain-source bias means that the barrier potentials ϕ_1 and ϕ_2 are no longer constant along the channel. Rather, they increase progressively from the source toward the drain. Thus, the potentials must be rewritten as functions of x, the distance along the channel from the source:

$$\phi_1 = \phi_1(x)$$
$$\phi_2 = \phi_2(x)$$

(2.18)

The potentials ϕ_1 and ϕ_2 are, of course, still governed by Eqs. 2.7 and 2.8. The
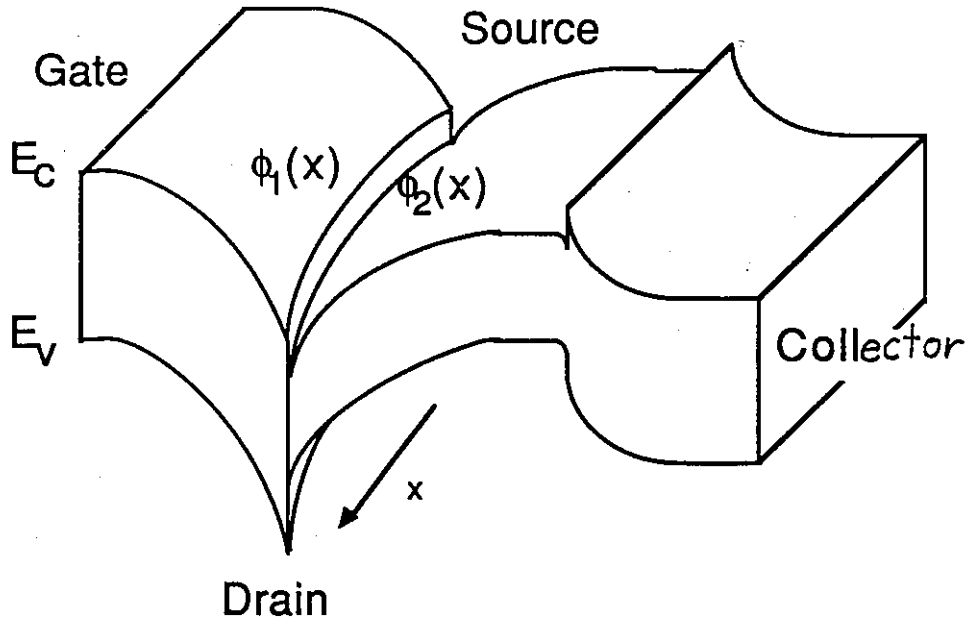
Figure 2.6   Three-dimensional energy band diagram of the n-channel
BISFET, showing the variation of the barrier potentials
along the channel from source to drain with a drain-source
voltage applied.   For illustrative purposes, the drain is
shown at the front of the diagram, while the source is at
the back. The potentials ϕ_1 and ϕ_2 are associated with the
depletion layers in the gate and active regions,
respectively.

variation of the energy bands parallel to the channel is illustrated in the three-

dimensional energy band diagram of Fig. 2.6.

The barrier current densities, J_{pb1}, J_{pb2}, and J_{pb}, given in Eqs. 2.9, 2.11,

and 2.12, now vary with position along the channel, since they are functions of ϕ_1

and ϕ_2. Each of the current density components must be integrated along the length

of the barrier from the source to the drain to determine the corresponding total

currents. The total barrier hole current per unit gate width, given in Eq. 2.15, must

then be calculated as

$$I_{pb} = \int_0^L [J_{pb1}(x) - J_{pb2}(x)]dx$$

$$= qN_1 v_{th} \int_0^L e^{-\phi_1(x)/V_t}dx - qN_2 v_{th} \int_0^L e^{-\phi_2(x)/V_t}dx$$

(2.19)

As discussed in Section 2.5.6, the feedback loop in the BISFET has certain constraints placed upon it. Rather than being free to vary, V_{gs} and V_{cs} in Eqs. 2.7 and 2.8 represent the voltages applied to the gate and collector contacts relative to the source. With lateral potential variations introduced to the device, Eqs. 2.7 and 2.8, describing the non-equilibrium Fermi-level relationships, are only valid at the source end of the device.

The variation of the energy bands in the plane of the device, described in this section, allows the state of the feedback loop, and hence the device, to be controlled by the source-drain voltage. This is the basis of operation of the BISFET.

2.6.2 Effect on Gate-Collector Characteristics

Increasing or decreasing the height of the potential barrier, ϕ_1, in the BISFET is equivalent to extracting carriers from or injecting them into the inversion channel, respectively. This has a significant effect on the gate-collector characteristic of the feedback loop, shown above in Fig. 2.5. The characteristics can be made to scale to higher or lower voltage by increasing or decreasing the height of the potential barrier, respectively. The source and drain contacts may be

used to this end. Applying a positive bias to the drain terminal relative to the source is equivalent to extracting electrons from the channel. It destroys the electrical symmetry which prevails between the source and drain terminals when $V_{ds} = 0$ by progressively increasing the size of the potential barrier towards the drain end, as shown in Fig. 2.6.

The increase in barrier height impedes the flow of holes from the gate to the active region and reduces the corresponding electron feedback current from the collector. Larger gate-collector voltages are therefore required to switch the feedback loop on; accordingly, V_s and V_h are increased. A schematic set of characteristics of the feedback loop is shown in Fig. 2.7, showing the effect of varying drain bias, V_{ds}, on the gate characteristics. The characteristics scale to the right with increasing V_{ds}, and to the left with decreasing V_{ds}.

2.6.3   Current Along Conduction Channel

Application of a drain bias to the BISFET and the resultant bending of the energy bands cause a current to flow along the conduction channel, in a manner similar to that in a normal FET. Unlike that in a normal FET, however, the channel current in the BISFET varies with position along the channel. In general, the source and drain currents are not equal in magnitude, because of the feedback current injected into the active region by the collector. This current (except for a portion which is lost to recombination, neglected in this discussion) enters the conduction channel by diffusion. As discussed earlier, it is assumed that the feedback current experiences no lateral drift component before entering the channel. Thus, it is assumed to be uniformly distributed along the channel from source to drain. In addition to the feedback current, there is a component of current leaving
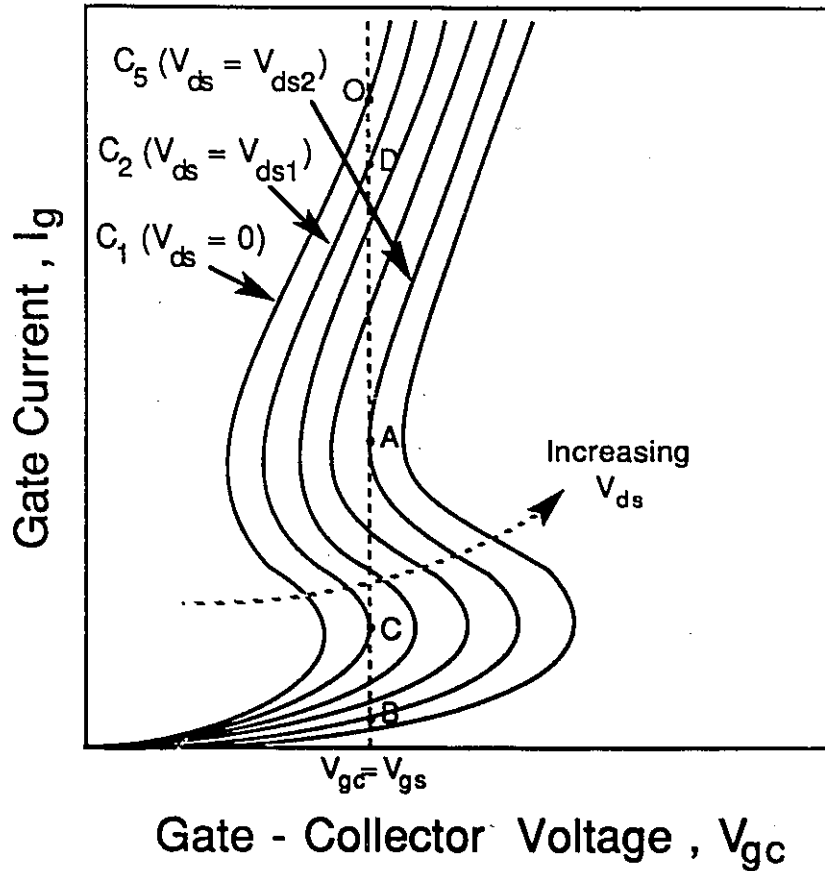
Figure 2.7   Schematic set of characteristics of the feedback loop in the
BISFET. The effect of varying V_{ds} is shown. The
characteristics scale to the right with increasing V_{ds}, and
to the left with decreasing V_{ds}.

the channel due to thermionic escape into the gate, or barrier layer. Thus, the

channel current consists of three main components, due to drift, feedback, and

thermionic escape.

The drift current at a position x along the channel is given by

$$I_{ch}(x) = \mu_n q N_{ch}(x) E(x) \tag{2.20}$$

where μ_n is the mobility of electrons in the channel and $E(x)$ is the electric field, which is a function of position. $N_{ch}(x)$ is the carrier population in the channel as a function of x. In a traditional FET, this drift equation is applied together with the current continuity equation:

$$\frac{dI_{ch}(x)}{dx} = 0 \qquad (2.21)$$

or, in integral form,

$$I_{ch} = constant \qquad (2.22)$$

However, in the BISFET, the continuity equation is modified by the feedback and thermionic current components transverse to the channel. Thus, while Eq. 2.20 holds at any position x, Eq. 2.21 must be rewritten:

$$\frac{dI_{ch}(x)}{dx} = J_{ic}(x) - J_{esc}(x) \qquad (2.23)$$

where J_{ic} is the feedback current injection density (per unit length of the channel), approximated by

$$J_{ic} = \frac{I_f}{l} = J_f \qquad (2.24)$$

$J_{esc}(x)$ is the thermionic escape current density as a function of position, shown in Fig. 2.3, and given by

$$J_{esc}(x) = qN_{ch}(x)v_{th}e^{-\left[\phi_1(x) + \Delta E_c - \Delta E_k(x)\right]/V_t} \qquad (2.25)$$

where $\Delta E_{fc}(x)$ is the energy difference between the Fermi energy and the conduction band edge in the channel as a function of x. Because of the difficulty of determining the function $\Delta E_{fc}(x)$, in attempting to solve the equations describing the operation of the BISFET, the somewhat crude approximation could be made of setting it to zero.

Now, combining Eqs. 2.20 and 2.23, we obtain

$$
\begin{aligned}
I_{ch}(x+dx) &= \mu_n q N_{ch}(x+dx)E(x+dx) \\
&= \mu_n q N_{ch}(x)E(x) + \left[J_f(x) - J_{esc}(x)\right]dx
\end{aligned} \qquad (2.26)
$$

This equation provides the relationship between the electric field at two points in the channel separated by a distance dx. Equally important, it provides a second relationship between the feedback current and the potential profile along the barrier. This is true because the barrier potential profile, $\phi_1(x)$, is related to the electric field function $E(x)$ by

$$E(x) = \frac{d\phi_1(x)}{dx} \qquad (2.27)$$

or, in integral form,

$$\phi_1(x) = \phi_1(0) + \int_0^x E(x)\, dx$$

where $\phi_I(0)$ is the height of the potential barrier at the source. Thus, together with Eqs. 2.1-2.4 and 2.7-2.12, and the feedback Eqs. 2.13-2.16, Eq. 2.26 establishes a channel potential profile that is self-consistent from the point of view of current continuity both along the conduction channel (once transverse components of current flow are accounted for) and in the feedback loop.

2.6.4 Increasing Drain Voltage

Let us now consider the effect of increasing the drain bias from zero. At low gate voltage, the feedback loop is in the OFF state, and the carrier population in the conduction channel is directly controlled by the gate voltage. A schematic of the drain characteristics is found in Fig. 2.8, showing I_d as a function of V_{ds} for fixed V_{gs}. They resemble those of a typical FET. As the drain voltage is increased from zero, the drain current first increases rapidly, then saturates.

At a sufficiently high gate voltage, say V_{gsl}, the feedback loop is in the ON state with no drain bias applied. Generalized drain characteristics for such a gate voltage are shown in Fig. 2.9 for both increasing and decreasing V_{ds}. The characteristics display abrupt transitions in output current, the origin of which is described below.

The gate-collector characteristic for zero drain bias is labelled C_I in Fig. 2.7. The vertical line is the load line corresponding to $V_{gc} = V_{gcl}$, where V_{gcl} is some fixed voltage applied to the gate. Thus, the device operates initially at the intersection of this load line with C_I, the point labelled O, which corresponds to the point O in Fig. 2.9. At this point, the feedback loop is in the ON state.

As V_{ds} is increased, the gate-collector characteristics begin to scale to higher voltage, and the operating point of the feedback loop moves down the curve to
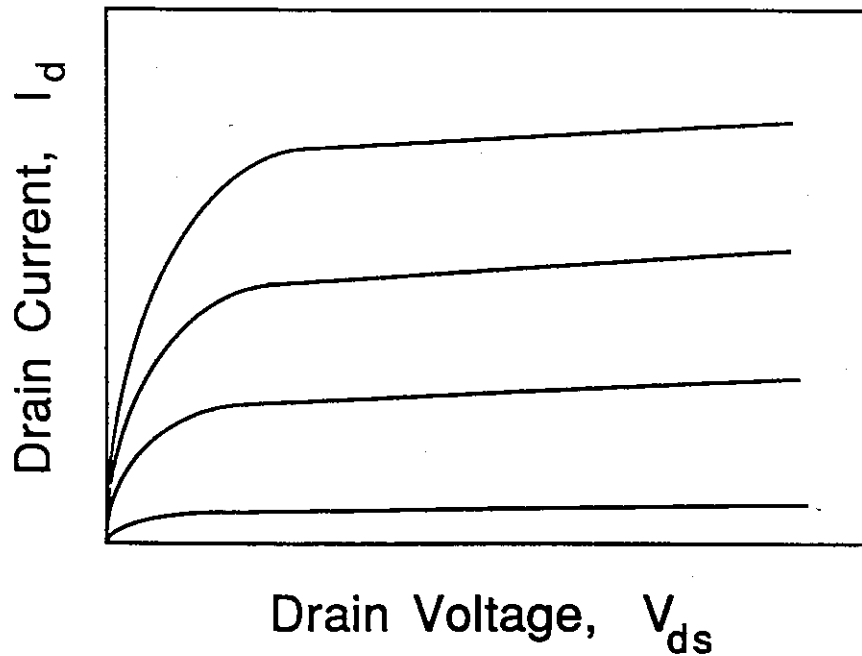
Figure 2.8   Schematic showing typical drain characteristics of a normal FET.

lower current. For instance, when the characteristic is described by curve C_2, the feedback loop operates at the point labelled D, corresponding to the point D in Fig. 2.9. The downward shift continues until the operating point reaches the point A on curve C_5, again corresponding to that in Fig. 2.9, at a drain voltage V_{ds2}, as labelled in both figures.

Note that point A coincides with the holding point of the feedback loop, labelled Z in Fig. 2.5. When the drain voltage is increased even slightly beyond V_{ds2}, the load line imposed on the feedback loop no longer intersects the characteristic in the ON state. Rather, it intersects only in the OFF state, at the point B. Thus, the operating point drops abruptly from point A to point B when
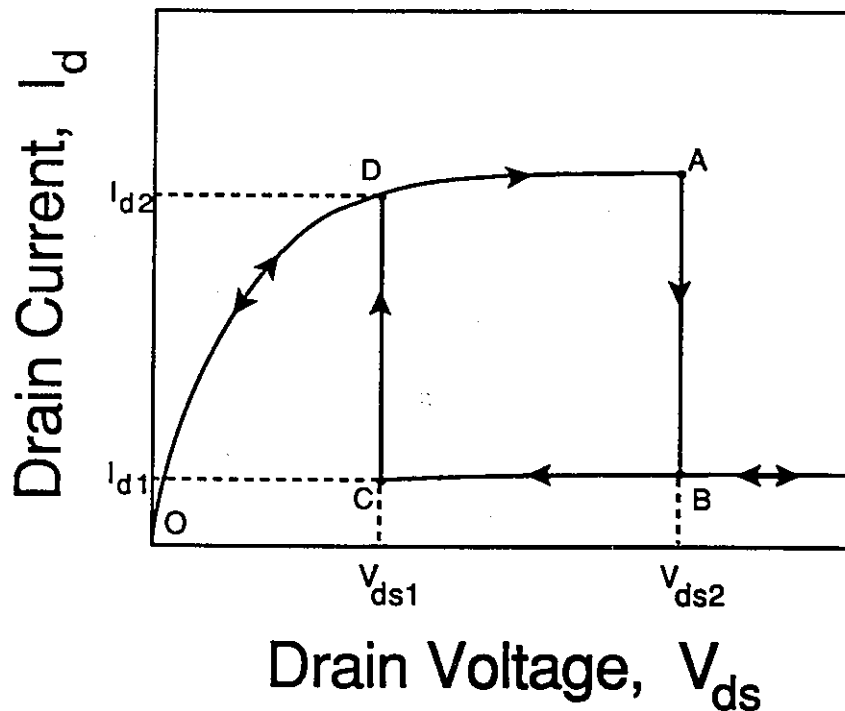
Figure 2.9   Generalized drain characteristic of the BISFET for a value
of V_{gs} high enough to activate the feedback loop. The
abrupt switchup and switchdown transitions are evident at
V_{ds1} and V_{ds2}, respectively.

$V_{ds} = V_{ds2}$, and the feedback loop turns off. However, as described in

Section 2.5.5, the OFF state is characterized by a substantially larger depletion

space charge, and correspondingly smaller charge in the conduction channel, than

found in the ON state. This results in lower channel conductance and, hence,

smaller drain current than in the ON state for a given V_{gs} and V_{ds}. Thus, the drain

current drops abruptly from a value I_{d2} to a significantly lower level, I_{d1}. This

appears as the precipitous drop indicated by segment *AB* in Fig. 2.9. This sharp

transition is referred to as switchdown. As V_{ds} is increased further beyond V_{ds2},

the feedback loop remains in the high-impedance OFF state, and the drain output remains in the low-current state.

2.6.5 Decreasing Drain Voltage

Consider now what happens when V_{ds} is decreased towards zero again. The gate characteristics begin to scale towards lower voltage once more. However, note that when curve C_5 of Fig. 2.7 is reached once more, corresponding to $V_{ds} = V_{ds2}$, the feedback loop does not return to the ON state at point A. This is because $p\delta npn$ feedback loops are inherently bistable - that is, they remain in their existing state until they are forced out of it, even if other valid operating points exist for the same set of bias conditions. As the drain voltage is reduced below V_{ds2}, the characteristics continue to scale inward, and the operating point slides along the characteristic in the OFF state towards higher I_g. When the curve C_2 is reached at a drain voltage V_{ds1}, the operating state of the feedback loop is given by point C in Fig. 2.7. Note that this corresponds to the switching point Y in Fig. 2.5. The drain output is still in a low-current state, as shown in Fig. 2.9.

As V_{ds} is reduced even slightly below V_{ds1}, the load line no longer intersects the curve in the OFF state. A single valid operating point exists at D. Thus, the feedback loop switches abruptly into the ON state. This leads to a collapse in the depletion space charge in the device, with an accompanying jump in the inversion channel charge. The result is an abrupt increase in drain current from I_{d1} to I_{d2}, referred to as switchup, and illustrated by the segment CD in Fig. 2.9. As V_{ds} is reduced further, and the gate characteristics continue to scale to lower voltage, the operating point slides further up the characteristics towards the point O.

In summary, then, the device switches on when the operating point of the

feedback loop coincides with the switching point, i.e., when V_{gs} is equal to the switching voltage, V_s. It switches off when the operating point coincides with the holding point, i.e., when V_{gs} equals the holding voltage, V_h. Obviously, these two points do not generally coincide. As the feedback loop follows the sequence of operating points *ABCD* in Fig. 2.7, the drain characteristics of the device therefore sweep out the corresponding hysteresis loop *ABCD*, shown in Fig. 2.9. The abrupt transitions and the hysteresis thus result from the properties of the feedback loop.

2.6.6   Separate and Integral Collector Configurations

It has been assumed thus far that the collector consists of a separate, distinct terminal attached to the collector layer of the BISFET. The feedback loop thus lies completely transverse to the conduction channel, extending from the gate, over the potential barrier, and through the active region to the collector. A new type of feedback loop is now proposed, however, which is folded back on itself.

It will be recalled that the gate-collector feedback loop consists of a *pδnpn* semiconductor sequence. A similar sequence lies in traversing a path from the gate, past the barrier to the active region, then into the source contact. This loop still operates transverse to the channel, beginning with the gate and passing over the potential barrier into the active region. However, from here, it doubles back on itself, terminating with the source contact rather than the collector layer. The source contact thus serves as an integral source and collector. It now performs two functions. It still provides electrons for conduction through the inversion channel. However, it also serves the additional role of the collector. Hence, holes flow from

the gate into the active region, then exit via the source. At the same time, the source provides electron feedback current which diffuses into the active region. As in the separate-collector configuration, this current enters the channel by a combination of drift and diffusion, whence some of it diffuses into the gate. The remainder flows into the drain and contributes to the drain current.

In summary, then, when a separate collector terminal is used, the feedback path in the BISFET lies between the gate and the collector layer of the structure. In contrast, when an integral source and collector contact is used, the feedback path lies between the gate and source terminals. Because it obviates the need for a separate collector, the integral source/collector configuration represents a fundamental design simplification of the BISFET. In order for this to be implemented, however, the source contact must be designed and fabricated so as to penetrate the depletion layer in the active region and form an effective *p-n* junction with the latter. The source contact must have relatively high doping, and the junction must have an adequate cross-sectional area, so that it is capable of providing the feedback current required to switch the device on.

The integral collector configuration is electrically equivalent to the separate collector case, with V_{cs} set to zero. However, it is clearly quite different geometrically, as discussed above. The cross-sectional area of the junction is, in general, different in the two cases. Additionally, the current flows are less uniform in the integral collector case. The current flowing from the collector to the active region cannot be geometrically mapped onto the channel in as clear and simple a way. Hence, the assumption that the current from the collector flows uniformly into the channel is less valid than in the separate collector case.

While the function of the collector may be built into the source contact, the

use of a separate collector terminal offers some benefits. In particular, it has so far been assumed that the collector is electrically equivalent to the source, that is, it has been set to the same potential as the latter. In practice, however, the use of a separate collector allows a finite collector-source voltage, V_{cs}, to be applied. In the n-channel device, a negative bias applied to the collector relative to the source tends to forward bias the junction formed by the collector and the active region, in addition to the forward bias provided by the gate current. This increases the feedback and tends to push the device further into the ON state than it would be with $V_{cs} = 0$. The effect of this is to cause the gate characteristics to scale to lower voltage. Applying a positive bias to the collector tends to de-bias the p-n junction, reducing the feedback and causing the gate characteristics to scale to higher voltage. Application of a collector bias also affects the threshold voltage of the device, in much the same manner as the substrate bias in a MOSFET [44]. A separate collector terminal thus offers an extra degree of freedom in controlling the operation of the BISFET.

Chapter 3

ELECTRICAL CHARACTERISTICS
OF THE BISFET

Now that a theoretical description of the operation of the BISFET has been given, the experimentally measured electrical characteristics of an actual device are presented. The semiconductor structure and physical design of the device are first described. Then, a range of characteristics are presented, including the drain characteristics, the transfer and complementary transfer characteristics, and the gate characteristics.

3.1   Heterostructure and Physical Design of the BISFET

The BISFET has been implemented using an n-channel GaAs/AlGaAs heterostructure grown by molecular beam epitaxy. The layer structure is shown in Fig. 3.1. The substrate consists of a wafer of n^+ GaAs with a doping density of 10^{18} cm^{-3}. The growth commences with a 1000 Å buffer layer of GaAs doped n-type at 5×10^{17} cm^{-3}. This serves to isolate the epitaxial layers from any dislocations in the substrate. Substrate dislocations will typically propagate

contact layer	300 Å	GaAs	10^{19} cm^{-3}	p
contact layer	200 Å	AlGaAs	10^{19} cm^{-3}	p
gate	500 Å	AlGaAs	10^{17} cm^{-3}	p
charge sheet	50 Å	AlGaAs	10^{19} cm^{-3}	n^{+}
channel layer	50 Å	GaAs		i
active layer	1 μm	GaAs	10^{17} cm^{-3}	p
collector	3000 Å	AlGaAs	3×10^{18} cm^{-3}	n
interface layer	100 Å	AlGaAs	3×10^{18} cm^{-3}	n
contact layer	2000 Å	GaAs	3×10^{18} cm^{-3}	n
buffer layer	1000 Å	GaAs	5×10^{17} cm^{-3}	n
substrate		GaAs	10^{18} cm^{-3}	n

Figure 3.1 Layer structure of the n-channel GaAs/AlGaAs BISFET. The name of the layer is indicated at left, followed by the thickness, composition, doping density, and dopant type. The composition of the AlGaAs layers is $Al_{0.3}Ga_{0.7}As$, except the interface layer, which is graded from 0 to 30% aluminum content.

through a growing epilayer, but are progressively corrected as the epilayer grows thicker.

The buffer layer is followed by a 2000 Å n-GaAs layer doped at 3×10^{18} cm^{-3}. This relatively heavily-doped layer serves to provide a good ohmic contact to the back of the device structure. A 100 Å layer of n-AlGaAs, again doped at 3×10^{18} cm^{-3}, is grown on the ohmic contact layer. The aluminum fraction in this layer is continuously graded from 0-30%. This is done to provide a continuous grading of the energy bands from the GaAs contact layer to the subsequent AlGaAs collector layer, rather than creating an energy discontinuity which might interfere with the electrical operation of the device by trapping or impeding the flow of carriers.

The collector layer itself consists of 3000 Å of Al$_{0.3}$Ga$_{0.7}$As doped n-type at 3×10^{18} cm^{-3}. Because the substrate and the buffer, contact, and interface layers are all doped n-type, the collector layer can be contacted via the back of the wafer. When the device is used in the integral source-collector mode described in Chapter 2, the collector is allowed to float electrically. It thus serves no biasing role, but it still helps to confine holes in the active region. When a separate collector terminal is desired, this layer is required to provide feedback current in the device.

The collector is followed by a 1 μm p-type GaAs active layer, doped at 10^{17} cm^{-3}. The active region plays a critical role in the switching of the BISFET. It is the site of hole accumulation resulting from the gate current. The potential in the active region changes abruptly as the feedback loop switches on and off, thus controlling the injection of feedback current into the device from the collector. The active region is terminated with a 50 Å channel layer consisting of intrinsic GaAs. This is done to provide a high-mobility layer to serve as the conduction

channel at the interface between the active region and the gate layer. The presence of dopant atoms here would reduce the carrier mobility in the channel by providing collision sites for the free carriers.

The charge sheet is formed by growing atop the channel layer a 50 Å layer of n-type $Al_{0.3}Ga_{0.7}As$ doped at 10^{19} cm^{-3}. The effective doping level in the charge sheet is very likely to be substantially lower than 10^{19} cm^{-3}. This is a result of poor electrical activation efficiency of n-type dopants at such high concentrations in GaAs [45]. The effective doping level is perhaps as low as 2-3×10^{18} cm^{-3}. The charge sheet is followed by a 500 Å p-type gate layer of $Al_{0.3}Ga_{0.7}As$ doped at 10^{17} cm^{-3}. The gate layer is sometimes referred to as the barrier layer because it is the site of most of the potential barrier to hole flow which is induced by the charge sheet. The structure is completed by growing two 10^{19} cm^{-3} p-type contact layers. The first of these consists of 200 Å of $Al_{0.3}Ga_{0.7}As$ to provide continuity of the energy bands from the contact to the gate layer. However, because of the difficulty of achieving good ohmic contact to AlGaAs, it is followed by a 300 Å layer of GaAs.

An ohmic contact is made to the gate of the BISFET by depositing metal on the top contact layer of the heterostructure. The high doping level of the top contact layer ensures that a good ohmic contact is achieved by minimizing the Schottky effect. As noted in Chapter 2, this is important because of the crucial role played by the gate current in the switching of the device. Ohmic contacts are also made to the conduction channel to serve as source and drain terminals. This is done by n-type ion implantation of Si to provide highly-doped regions, again to overcome Schottky effects, as well as to provide an n-type conduction path for electrons through the p-type gate and contact layers.

The source is designed to serve as an integral source and collector for the BISFET. The implant is thus made deep enough to ensure that the source contact penetrates the active layer depletion width, so it forms an effective junction with the active region. The gate length and width of the GaAs/AlGaAs devices reported in this work are 2 μm and 150 μm, respectively, unless otherwise indicated for a particular set of measurements.

3.2 Drain Characteristics For Low Gate Voltage

The electrical characteristics of the GaAs/AlGaAs BISFET were measured using a Hewlett-Packard 4145B semiconductor parameter analyzer. The parameter analyzer has a maximum voltage resolution of 1 mV when applying a voltage bias. The biasing scheme, indicating where the various bias voltages are applied to the device, as well as their polarities, is shown in in Fig. 3.2. Note that in this chapter, the device characteristics are reported with the collector floating, so that the device operates in the integral collector mode.

The drain characteristics of a typical GaAs BISFET, giving I_d vs. V_{ds}, are shown in Fig. 3.3 for $V_{gs} = 0.5$ V to 2.25 V in steps of 0.25 V. For $V_{gs} < 0.5$ V, the curves are found to be indistinguishable from the horizontal axis, as they lie below the threshold voltage of the device. The last two curves have values of V_{gs} clearly lying well above the holding voltage, V_h, of the feedback loop from gate to source, which is approximately 1.7 V for this structure. The characteristics display typical FET behaviour for $V_{gs} < V_h$, with the drain current rising with V_{ds} for a given gate bias, then saturating. The spacings amongst the characteristics are quite regular for low gate voltage. However, for $V_{gs} = 2$ V, which lies above

GND V_{gs} (+) V_{ds} (+)

S   G   D

n^{++} p-AlGaAs   n^{++}

p-GaAs   n$^+$-AlGaAs

n-AlGaAs   Collector

V_{cs}

(floating)
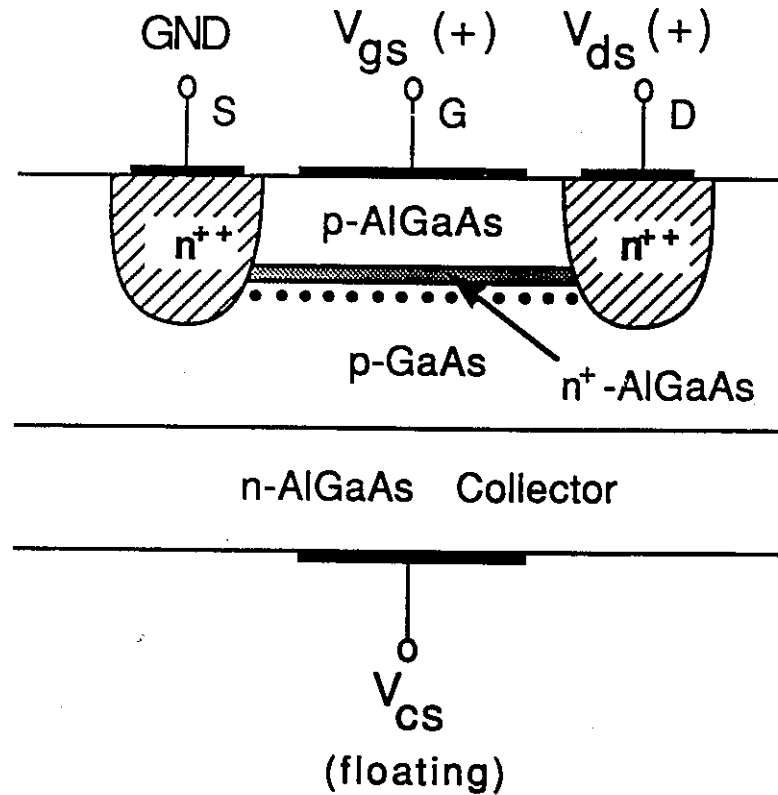
Figure 3.2   Biasing scheme for the GaAs/AlGaAs BISFET, showing
the locations and polarities of the various bias voltages.

V_h, I_d takes an unusually large jump from the values measured for the previous gate voltage. This reflects the fact that at low gate voltages ($V_{gs} < V_h$), the feedback loop is off for all values of V_{ds}. However, at sufficiently high V_{gs} ($V_{gs} \gg V_h$), the feedback loop is on for all V_{ds}. Thus, there is a conspicuous jump in drain current, resulting from the enhancement in channel charge when the feedback loop is in the ON rather than the OFF state.

It is noteworthy that the drain current becomes negative at very low drain bias when V_{gs} is high enough for the device to be in the ON state. This occurs
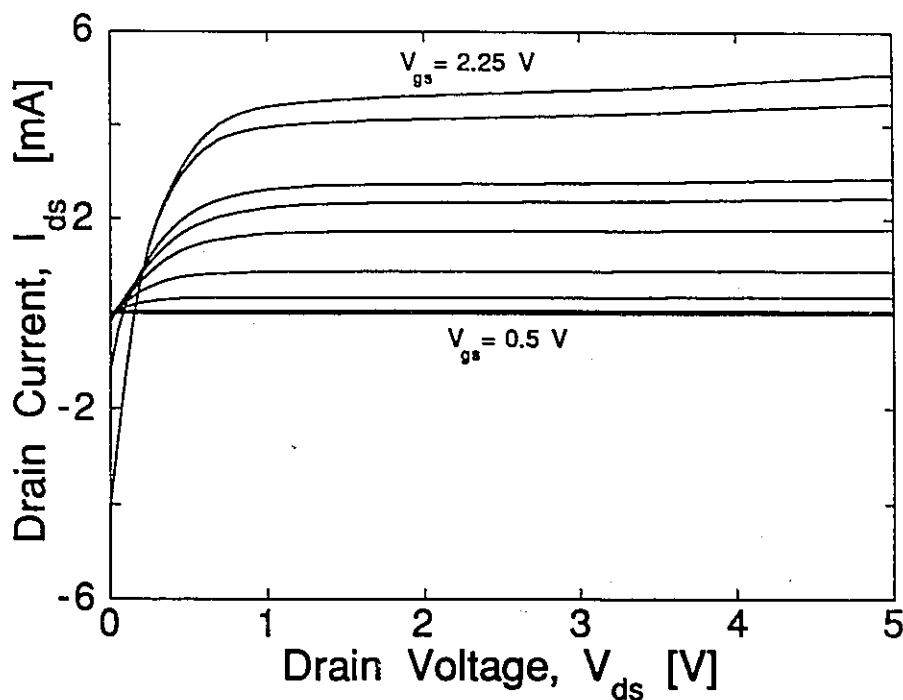
Figure 3.3   Drain characteristics of the BISFET for coarse spacings of V_{gs}. The characteristics are shown for $V_{gs} = 0.5$ V to 2.25 V in steps of 0.25 V. For $V_{gs} < 0.5$ V, the curves are found to be indistinguishable from the horizontal axis.

because the hole current from the gate into the active region of the device forward biases the junction between the drain contact and the active region when $V_{ds} = 0$. A substantial portion of this hole current thus flows into the drain, causing I_d to become negative. As V_{ds} is increased, however, the junction between the drain and the active region becomes less forward biased, and eventually, reverse biased. The hole flow into the drain is progressively cut off with increasing V_{ds}, being diverted instead to the source contact. I_d thus becomes positive.
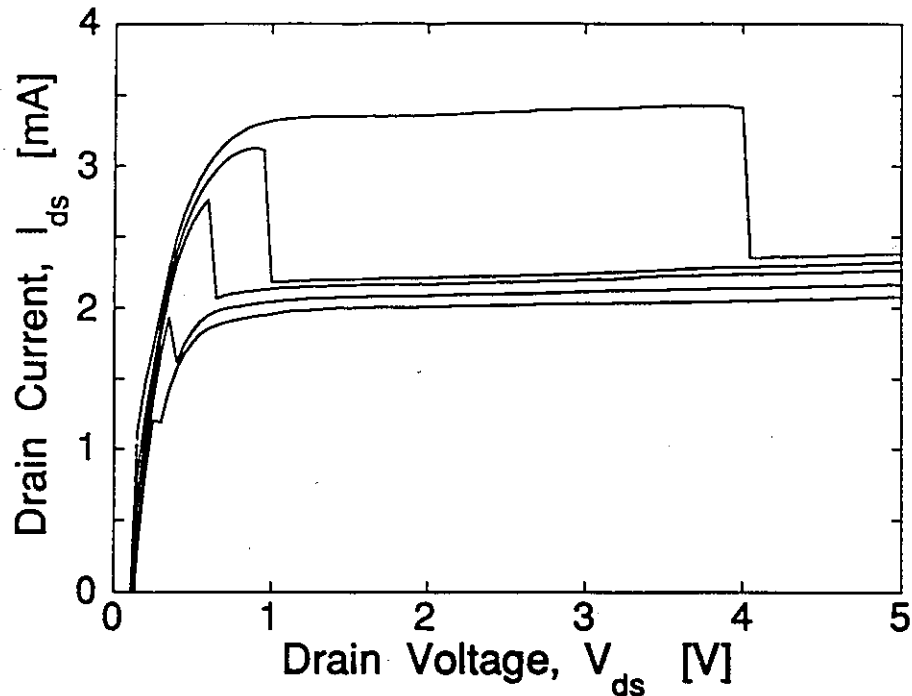
Figure 3.4   Drain characteristics of the BISFET, measured in the
forward direction for a narrow range of gate voltage
above V_h. The characteristics are given for $V_{gs} = 1.70$ V,
1.72 V, 1.74 V, 1.75 V, and 1.76 V.

3.3   Drain Characteristics For High Gate Voltage

The drain characteristics are shown in Fig. 3.4 with much finer steps in the

region of interest revealed in Fig. 3.3. The gate voltages used were 1.70 V,

1.72 V, 1.74 V, 1.75 V, and 1.76 V. These particular values were chosen to

illustrate the evolution of the transition with increasing gate bias. The range of

voltage shown is slightly above V_h for the feedback loop from gate to source.

These characteristics were obtained by sweeping in the forward direction (i.e.,

increasing V_{ds}). Initially, as the drain voltage is increased from zero for a given
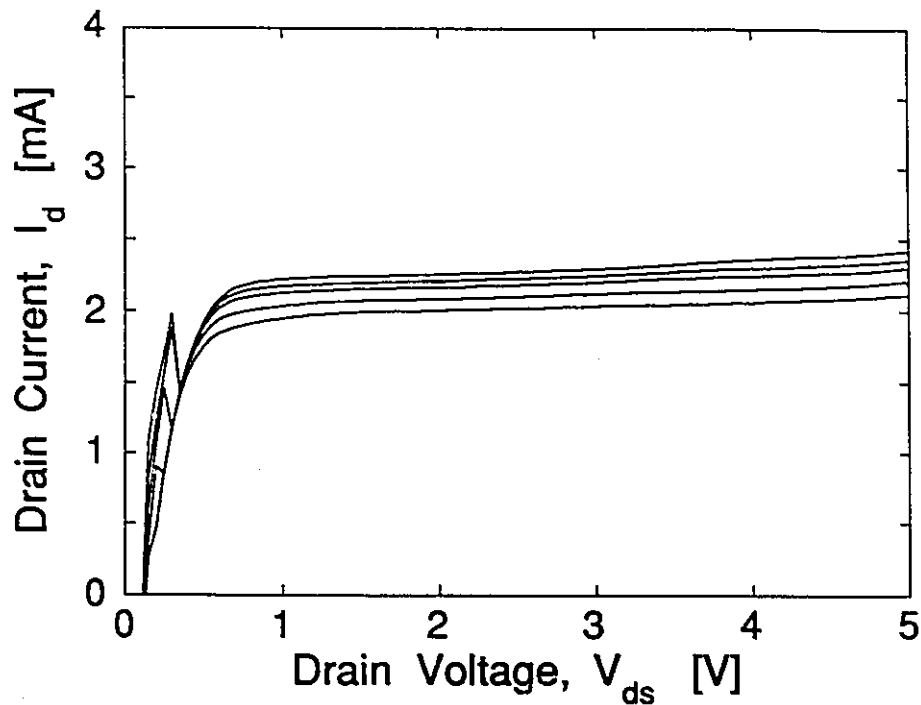
Figure 3.5   Drain characteristics for the same values of V_{gs} as in Fig. 3.4, but with V_{ds} swept in the reverse direction.

gate voltage, the device follows a normal FET curve. However, at a voltage V_{ds2}, a switchdown transition is observed as the current drops abruptly from I_{d2} to the lower value I_{d1}, as described in Chapter 2. The switching ratio for this transition is approximately 1.5. As the gate bias is increased, V_{ds2} increases.

When V_{ds} is swept in the reverse direction (i.e., decreasing drain voltage), the drain characteristics given in Fig. 3.5 are obtained. These are shown for the same gate voltages as in Fig. 3.4. This time, abrupt switchup transitions are observed from the low-current state to the high-current state, this time at a voltage V_{ds1}. The drain current jumps from the value I_{d1} to I_{d2}, both of which were defined in Chapter 2. As with V_{ds2}, V_{ds1} also increases with increasing V_{gs}.
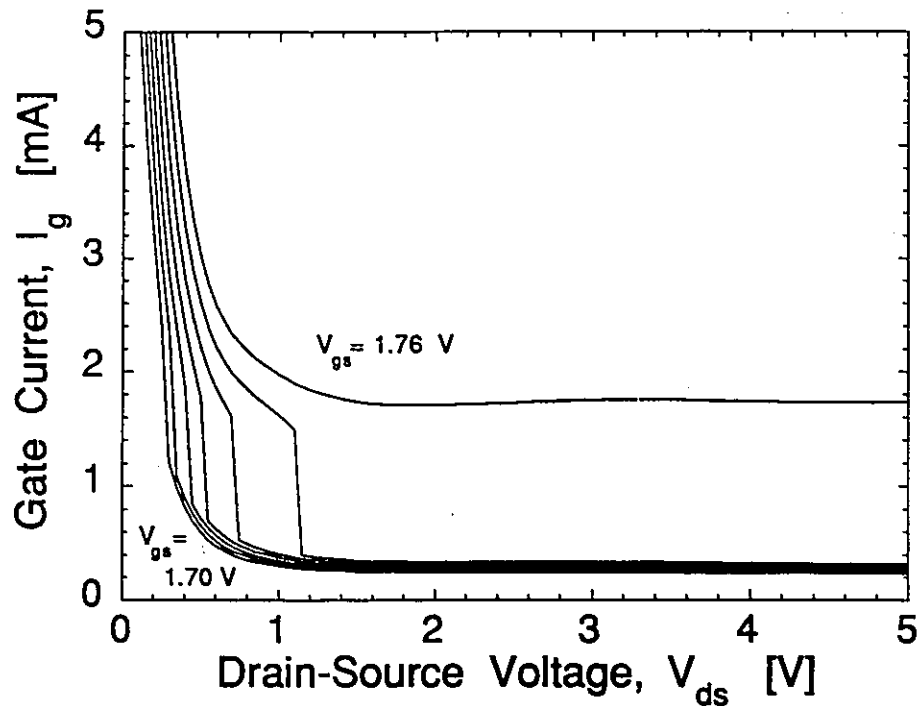
Figure 3.6 Complementary transfer characteristics of the BISFET, plotting the gate current against the drain voltage. The curves are shown for the same gate voltages as in Figs. 3.4 and 3.5.

However, V_{ds1} is substantially lower than V_{ds2} for a given gate voltage. In fact, in the reverse-swept characteristics, the transitions are compressed into the ohmic region of operation for all the gate voltages which were used.

3.4 Complementary Transfer Characteristics

Confirmation of the operation of the feedback loop can be seen in Fig. 3.6. This shows the variation of the gate current in a BISFET with V_{ds} for the same gate voltages used in Figs. 3.4 and 3.5, for increasing V_{ds}. These curves are

referred to as the complementary transfer characteristics of the device. The gate current is relatively low for gate voltages below the holding voltage, corresponding to cases where the feedback loop is off for all values of V_{ds}. As V_{gs} approaches V_h for the feedback loop, the gate current becomes quite large for low drain voltages. However, following a general decline, precipitous drops in gate current are evident as the drain bias is increased. For every gate voltage, these sudden drops are found to correspond precisely with the switchdown points in the drain characteristics, indicating the turn-off of the feedback loop.

Similar results are obtained when the reverse complementary transfer characteristics are taken, that is, with decreasing V_{ds}. In this case, abrupt increases in gate current are observed as V_{ds} is decreased, corresponding to the voltage at which switchup is observed in the reverse-swept drain characteristics. In all cases, the transitions in both the gate and drain currents are reproducible, and sharper than the instrument resolution of 1 mV.

3.5   Hysteresis in Drain And Complementary Transfer Characteristics

As mentioned above, the switchdown voltage V_{ds2} is significantly greater than V_{ds1}. This is illustrated in Fig. 3.7, which shows the drain characteristics for increasing as well as decreasing V_{ds} for a single gate voltage of 1.76 V. The fact that the device remains in the low-current state with decreasing V_{ds}, even for voltages less than the switchdown voltage, is readily observed. This is seen to result in substantial hysteresis in the drain characteristics. For the case shown, V_{ds1} and V_{ds2} are 0.3 V and 4 V, respectively, giving hysteresis of 3.7 V. This hysteresis increases with increasing V_{gs}. The forward and reverse complementary
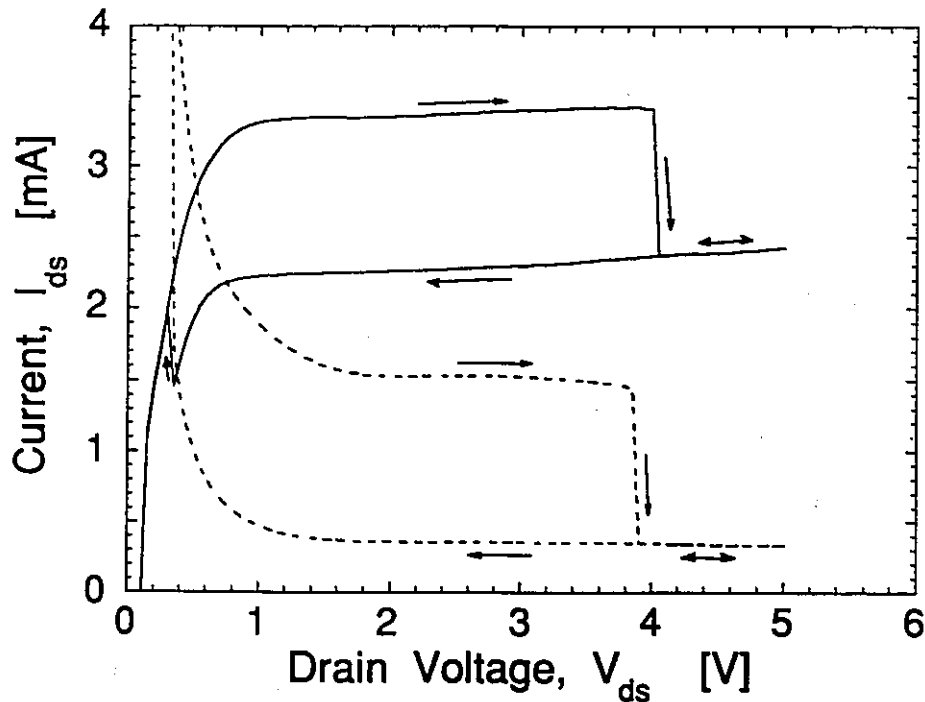
Figure 3.7   Drain (solid line) and complementary transfer (dotted line) characteristics of the BISFET in both the forward and reverse sweep directions for $V_{gs} = 1.76$ V. The characteristics illustrate the hysteretic behaviour of the device.

transfer characteristics for $V_{gs} = 1.76$ V are also superimposed in Fig. 3.7. As the transitions in gate current correspond with those in the drain current, the complementary transfer characteristics are seen to exhibit hysteresis corresponding with that in the drain characteristics.

The drain characteristics of the GaAs BISFET are qualitatively like the hypothetical ones shown in Fig. 2.9. Switchdown appears to occur for all gate voltages above the DOES holding voltage. However, the drain voltage at which it occurs escalates rapidly with increasing gate voltage. This is because the current

in the feedback loop increases with V_{gs}, so the potential barrier must be raised further and further to turn the feedback loop off. This requirement is easily met below pinchoff. However, once pinchoff is reached it becomes more difficult, since the barrier height no longer increases substantially along most of the channel. In other words, once pinchoff is reached, any further increase in V_{ds} is taken up by the pinchoff region, leaving the rest of the conduction channel and accompanying potential barrier essentially unchanged. This explains the great sensitivity of the transition voltages to gate bias in the saturation region.

3.6 Transfer Characteristics

The transfer characteristics of the BISFET were taken by sweeping the gate voltage and measuring the resulting drain current. The results are shown in Fig. 3.8 for increasing and decreasing V_{gs}, with $V_{ds} = 1$ V. In the forward sweep, little or no drain current is measured up to a voltage of approximately 0.5 V. This is therefore taken as the threshold voltage, V_{th}, of the device. A steady increase in drain current is initially seen as V_{gs} is increased beyond V_{th}. However, at a gate voltage which we shall call V_{gs2}, the drain current jumps abruptly as the feedback loop is forced into the ON state. The dramatic rise in gate current as the feedback loop turns ON prevents the gate voltage from being driven substantially beyond the turn-on point without damaging the device. However, it is possible to discern a significantly higher differential transconductance in the ON than in the OFF state. This results from the effect of the feedback current on the drain characteristics and the strong exponential dependence of this current on gate voltage in the ON state. V_{gs2} has been found to increase slightly with increasing
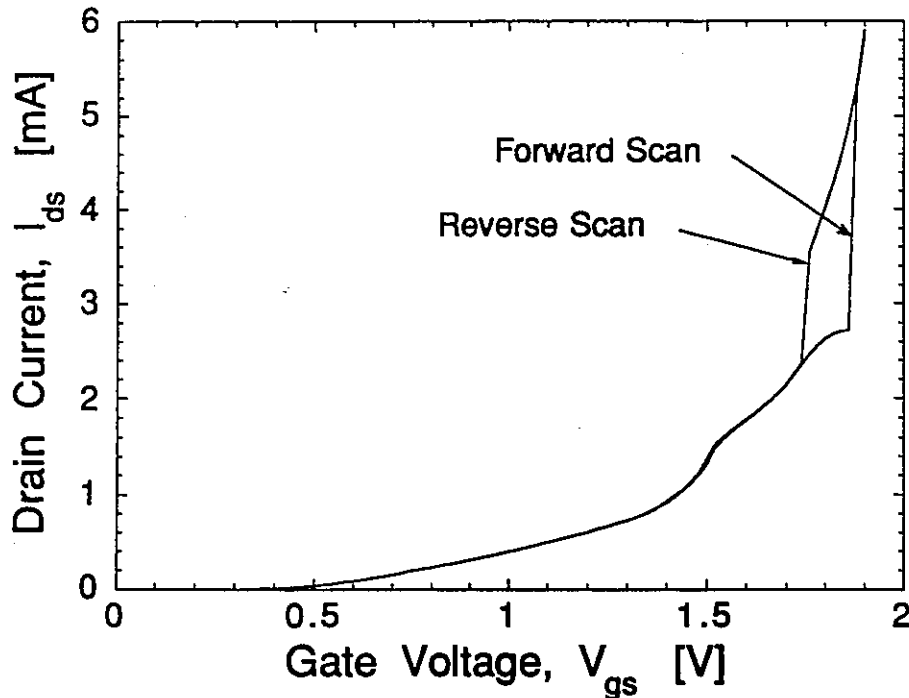
Figure 3.8   Forward- and reverse-swept transfer characteristics of
the BISFET, showing I_d as a function of V_{gs} for
$V_{ds} = 1$ V. The characteristics display abrupt transitions
and substantial hysteresis.

drain voltage. This is expected, since increasing V_{ds} raises the height of the

potential barrier at each point along the channel, tending to reduce the gate

current. Thus, a higher gate voltage is required to switch the device ON.

In the initial stages of the reverse sweep in Fig. 3.8, the device is in the

ON state. The drain current initially decreases rapidly but continuously as the

gate voltage is decreased. However, when the gate voltage reaches a value which

we shall call V_{gs1}, the feedback loop turns OFF once more, and the drain current

undergoes a corresponding abrupt drop. Again, in the OFF state, the

transconductance is substantially lower than in the ON state. It is evident that this

turn-off transition in the transfer characteristics does not occur at the same voltage as the turn-on transition. Rather, $V_{gs1} < V_{gs2}$. As in the drain characteristics, this results in the hysteresis seen in Fig. 3.8. The transition gate voltages in the case illustrated are approximately 1.75 V and 1.90 V, resulting in hysteresis of 0.15 V. The voltage V_{gs1}, like V_{gs2}, has been found to increase very slightly with increasing drain voltage.

3.7 Gate Characteristics

The gate characteristics of the BISFET were taken by measuring V_{gs} while sweeping the gate current. These are shown in Fig. 3.9, for $V_{ds} = 0$ V to 0.8 V in steps of 0.2 V, and 1 V to 5 V in steps of 1 V. The characteristics are qualitatively similar to the schematic ones shown in Fig. 2.7, with the S-type negative differential resistance apparent. Note that these are current-driven, rather than voltage-driven characteristics. The reason for this is that the S-type NDR makes I_g a multi-valued function of V_{gs}. V_{gs}, on the other hand, is a single-valued function of I_g, allowing the characteristics to be swept out by varying I_g. The characteristics contain an initial, low-impedance OFF segment. At the current I_s, however, the gate voltage drops from V_s to V_h as the feedback loop switches into the ON state. Beyond this point, the device remains in a low-impedance state, with the current increasing relatively rapidly with gate voltage. The switching and holding voltages, V_s and V_h, increase with V_{ds}, as expected according to the theory of operation presented in Chapter 2.
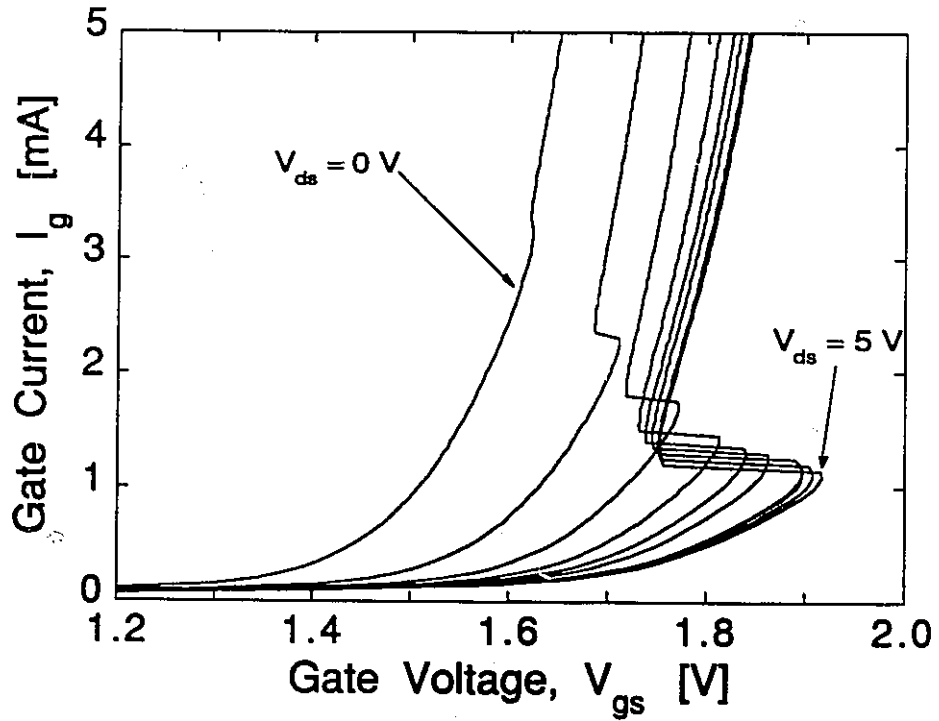
Figure 3.9   Gate characteristics of the BISFET for $V_{ds} = 0$ V to 0.8 V in steps of 0.2 V, and 1 V to 5 V in steps of 1 V.

Chapter 4

CHARACTERISTICS WITH
SEPARATE COLLECTOR TERMINAL

In Chapter 3, the DC electrical characteristics of the BISFET were presented with the substrate (and hence, the collector) electrically floating. The feedback loop lay between the gate and source terminals (integral collector mode). In this chapter, the characteristics are studied with a bias applied to the collector terminal. As the magnitude of the collector bias is increased, this is shown to introduce a second feedback loop into the device, which becomes operational at sufficiently high V_{gs}.

4.1 Effect of Low Collector Voltage

4.1.1 Drain Characteristics

The drain characteristics of the BISFET have been measured with a bias, V_{cs}, applied to the collector relative to the source. The collector layer can be contacted via the substrate, since both layers are doped n-type. A comparison

between the biased-collector and the floating-collector results is made below.

Fig. 4.1 shows the drain characteristics in the forward and reverse directions for a typical BISFET. They were taken for $V_{gs} = 1.81$ V to 1.90 V in steps of 10 mV, with the collector floating, as before. The characteristics were measured again for the same values of V_{gs} with the collector grounded, as shown in Fig. 4.2. The results are qualitatively similar in the two cases. Both sets of characteristics display the abrupt switchup and switchdown transitions. However, grounding the substrate has a dramatic quantitative effect. The OFF-state current is significantly reduced compared with the floating-substrate case, while the ON-state current is increased slightly. The result is a large increase in the switching ratio (the ratio of the ON- to the OFF-state current), from approximately 1.4 to almost 2. Grounding the collector also causes the transition voltages, V_{ds1} and V_{ds2}, to increase.

The device characteristics have also been measured with $V_{cs} < 0$, which forward biases the *p-n* junction. Due to the unavailability of a set of characteristics from a single device with the collector floating, grounded, *and* with a negative bias applied, the results with the negatively-biased collector are shown separately in Fig. 4.3 for a different device from that in Figs. 4.1 and 4.2. The characteristics are shown in both the forward and reverse sweep directions, with $V_{gs} = 1.91$ V and V_{cs} ranging from zero to -0.3 V, for a device having a gate length and width of 2 μm and 100 μm, respectively. As mentioned in Chapter 3, all of the characteristics reported are for devices having dimensions of 2 μm and 150 μm, unless otherwise indicated.

The characteristics of Fig. 4.3 show that applying a negative V_{cs} results in a continuation of the trends observed upon grounding the substrate compared with letting it float. The OFF-state current is progressively reduced from the case
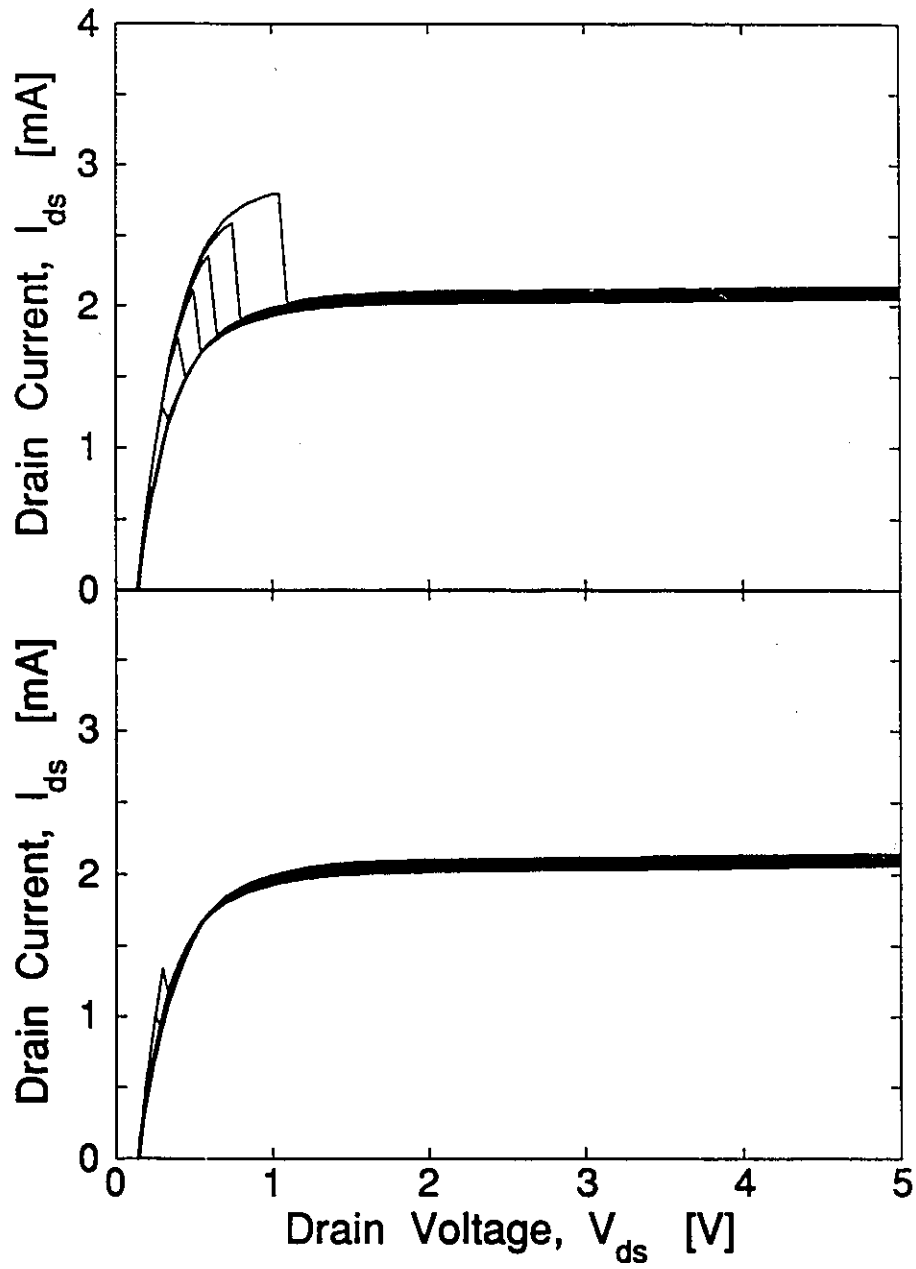
Figure 4.1   Drain characteristics of a typical BISFET in the forward (top) and reverse (bottom) sweep directions, with the substrate (collector) electrically floating. The characteristics are shown for $V_{gs} = 1.81$ V to 1.90 V in steps of 10 mV.
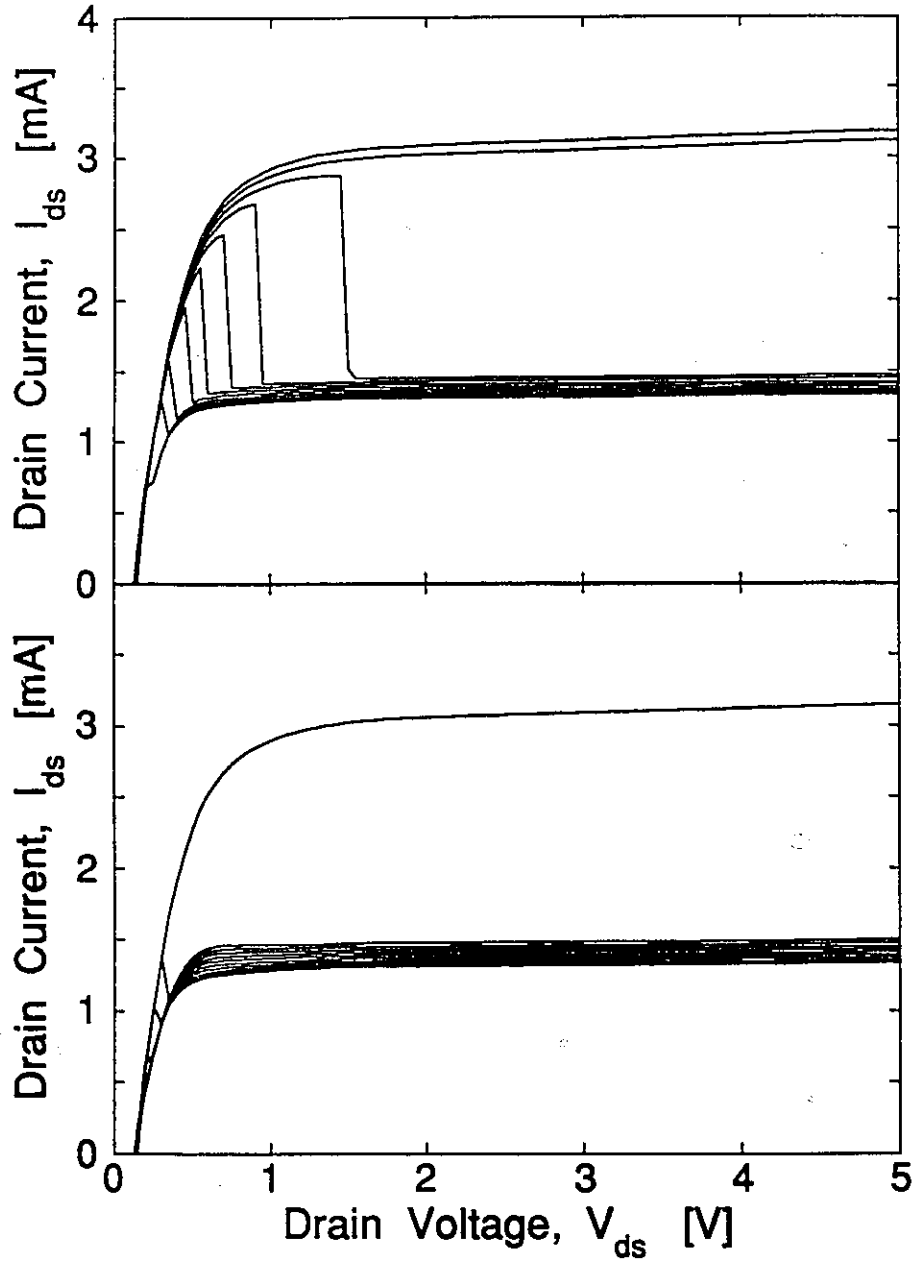
Figure 4.2   Drain characteristics of the device in Fig. 4.1 in the
forward (top) and reverse (bottom) sweep directions,
with the substrate (collector) grounded. The curves are
shown for the same values of V_{gs} as in Fig. 4.1.
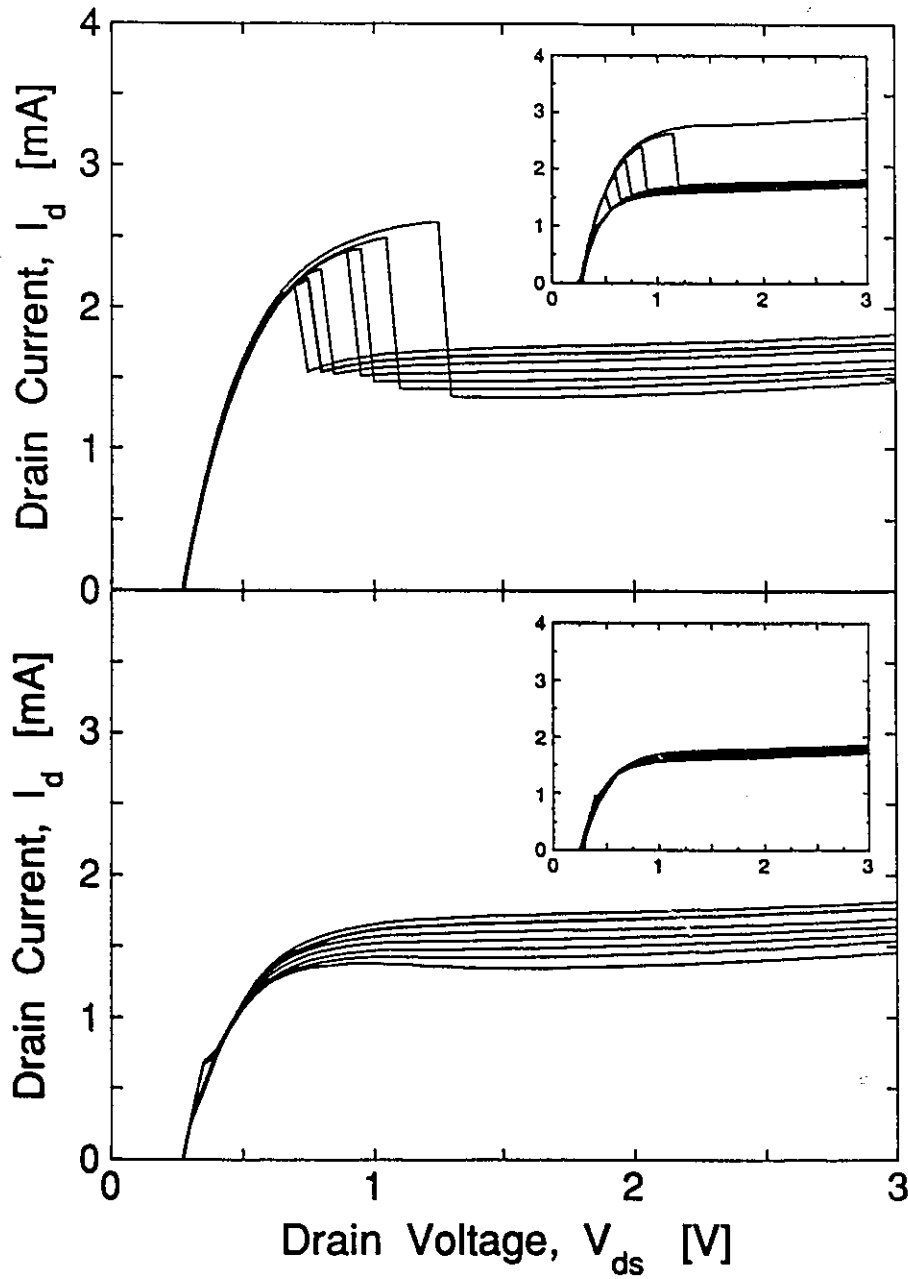
Figure 4.3   Drain characteristics of typical BISFET with V_{cs} as the parametric variable for fixed $V_{gs} = 1.91$ V, and $V_{cs} = 0$ V to -0.3 V in steps of 50 mV. Both forward- (top) and reverse-swept (bottom) characteristics are shown. Insets show forward- and reverse-swept characteristics for the same device with V_{gs} as the parametric variable for fixed $V_{cs} = 0$ V, and $V_{gs} = 1.85$ V to 1.94 V in steps of 10 mV.

where $V_{cs} = 0$, which already results in a reduced current compared with the floating-collector case. The ON-state current and the transition voltages, on the other hand, are progressively increased from their values at $V_{cs} = 0$, which are already higher than their floating-collector levels. A general explanation of the origin of these effects is proposed below.

4.1.2   OFF- State Current

As described above, grounding or applying a negative bias to the collector of the BISFET leads to a reduction in the OFF-state current. This is believed to result from an increase in the width of the depletion layer adjacent to the conduction channel in the active region. This is because the increase in depletion charge causes an equivalent reduction in the channel charge. Consider what happens when the substrate is floating. No current can pass over the active region-collector junction (or *p-n* junction) under steady state conditions, since there is nowhere for the holes injected into the collector region to escape. Thus, the collector layer must float in tandem with the active region, causing the former to develop a positive potential relative to the source to inhibit hole injection.

When a collector bias $V_{cs} \leq 0$ is applied to the device in the OFF state, the tendency is for the *p-n* junction to become forward biased, and for progressively larger and larger currents to flow across it. However, this is not possible, since the current through this junction is limited by the rate of hole injection into the active region from the gate. Thus, the active region must be pulled down to lower potential with the collector. This causes an increase in the width of the active region depletion layer adjacent to the conduction channel, and a corresponding increase in the depletion space charge, Q_2. Recalling Eq. 2.1,

$$Q_s + Q_1 + Q_2 + Q_{ch} = 0 \qquad (2.1)$$

it is apparent that this increase in Q_2 must be accompanied by a decrease in the channel charge, Q_{ch}. The result is a reduction in the OFF-state current as the collector voltage is made increasingly negative.

4.1.3 ON-State Current

When a collector bias is applied with the feedback loop in the ON state, the active region potential must, as before, be lowered along with the collector. However, in the ON state, the source-active junction is substantially forward biased. The *p-n* junction also becomes forward biased along with the source-active junction as the collector potential is pulled down, since hole current can now flow from the active region into both the source contact *and* the collector. Increasing the magnitude of the collector bias progressively increases the forward bias on the *p-n* junction, causing the collector to feed substantial additional electron current into the active region. These electrons flow into the conduction channel and contribute to I_d. They also contribute additional current to the feedback loop, tending to turn it on more forcefully. Thus, any reduction in channel charge due to expansion of the active region depletion layer is compensated by the additional collector current which is unleashed. The overall result is either very little change or an increase in the ON-state current when $V_{cs} \leq 0$, compared with when the collector is allowed to float.

The increase in collector current in the OFF state as the collector potential is pulled down is comparatively small, because the impedance of the feedback

loop is much higher in the OFF than in the ON state (recall Figs. 2.5, 2.7, and 3.9). Thus, it does not significantly compensate for the reduction in channel charge associated with the expansion of the active-region depletion layer.

In addition to affecting the ON- and OFF-state current levels in the BISFET, application of a collector bias $V_{cs} \leq 0$ also causes a significant increase in the switchup and switchdown transition voltages, as noted above in Section 4.1.1. This occurs because the *p-n* junction becomes progressively more forward biased as V_{cs} is made more negative, causing an increasing number of electrons to be injected into the active region. This, in turn, lowers the height of the potential barrier and increases the potential of the active region, making the feedback loop easier to turn on, and more difficult to turn off.

4.1.4   Comparison of the Effects of V_{cs} and V_{gs}

In order to compare the effects of varying V_{gs} and V_{cs}, the drain characteristics of the device are shown in the insets of Fig. 4.3 with V_{gs} as the parametric variable rather than V_{cs}. Increasing V_{gs} causes the transition voltage to increase. However, unlike the effect of increasing V_{cs}, the ON- and OFF-state current levels increase in tandem, so that any increase in the switching ratio is limited.

The voltage applied to the collector layer (or equivalently, to the substrate) offers a unique means of controlling the BISFET when the gate-source feedback loop is active. V_{cs} can be used to switch the state of the device via its effect on the transition voltages. In addition to this, however, it offers a means of directly controlling the switching ratio of the BISFET. Thus, the use of a separate collector offers an additional degree of freedom which can be used in controlling
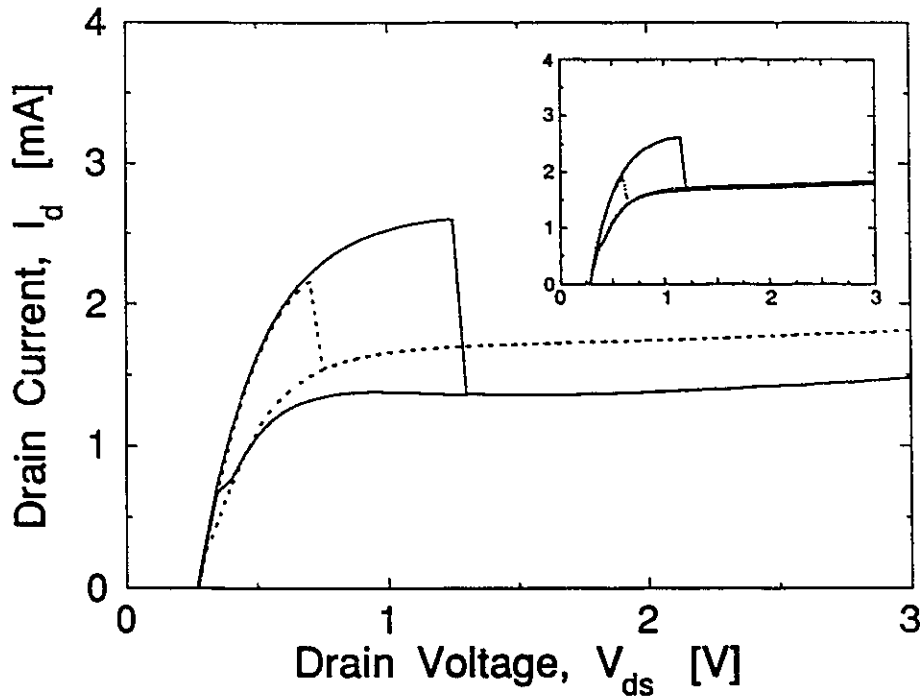
Figure 4.4   Full hysteresis loop in drain characteristics of device
shown in Fig. 4.3 for fixed $V_{gs} = 1.91$ V, with $V_{cs} = 0$ V
(dashed line) and -0.3 V (solid line).   Inset shows
hysteresis loop for fixed $V_{cs} = 0$ V, with $V_{gs} = 1.90$ V
(dashed line) and 1.93 V (solid line).

the operation of the device.

The effect of varying V_{cs} on the hysteresis in the drain characteristics of
the BISFET is illustrated in Fig. 4.4, which shows the full hysteresis loop for
$V_{gs} = 1.91$ V and $V_{cs} = 0$ V and -0.3 V.   For comparison, the hysteresis loop is
shown in the inset for two different values of V_{gs} and fixed $V_{cs} = 0$ V to illustrate
the effect of V_{gs}.   It is apparent that the hysteresis loop grows in size when either
V_{gs} or V_{cs} is increased.   However, a substantial vertical improvement results from
the change in V_{cs} compared with increasing V_{gs}.

4.2   Optimization of Design

The effect of V_{cs} on the drain characteristics offers important insight into optimization of the BISFET design. Ideally, it it desirable to make the switching ratio as large as possible, which requires making the OFF-state current as *small* as possible. The decrease in the OFF-state current achieved by negatively biasing the collector confirms that a reduction in the OFF-state channel charge is an effective means of doing this. Thus, it should be possible to increase the switching ratio by reducing the areal doping density in the charge sheet. This is illustrated in Fig. 4.5, which shows a schematic of the transfer characteristics of the BISFET. Fig. 4.5(a) shows the general case, with the traditional (analogue) threshold gate voltage, V_{th}, and the threshold for bistability (approximately equal to and denoted by the holding voltage of the feedback loop, V_h) indicated. Note that V_{th} and V_h are not, in general, equal. If the charge sheet doping is reduced sufficiently to make V_{th} equal to V_h, as shown in Fig. 4.5(b), no drain current will flow until V_{gs} is made large enough to access the bistable region of device operation. Thus, the OFF-state current should approach zero, as shown. In principle, then, it is expected that the switching ratio could be made arbitrarily large for a given V_{gs} by making the charge sheet doping density sufficiently small.

4.3   High Collector Voltage and Gate-Collector Feedback Loop

In Section 4.1, it has been shown that a voltage applied to the collector terminal influences the sizes of the transitions and the values of V_{ds} at which they
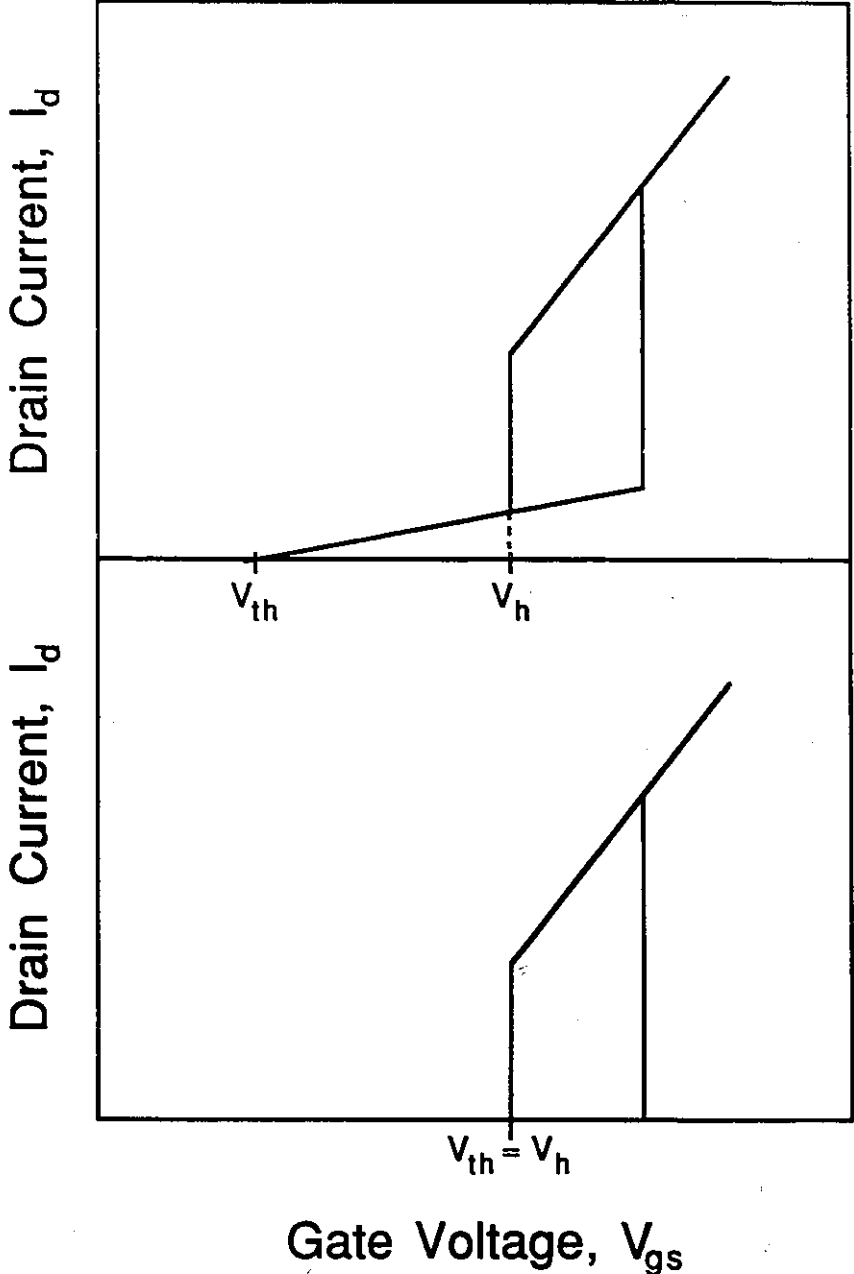
Figure 4.5   Schematic showing transfer characteristics of BISFET. Top sketch shows general transfer characteristics, with V_{th} and V_h indicated. Bottom shows case where $V_{th} = V_h$ to maximize switching ratio.
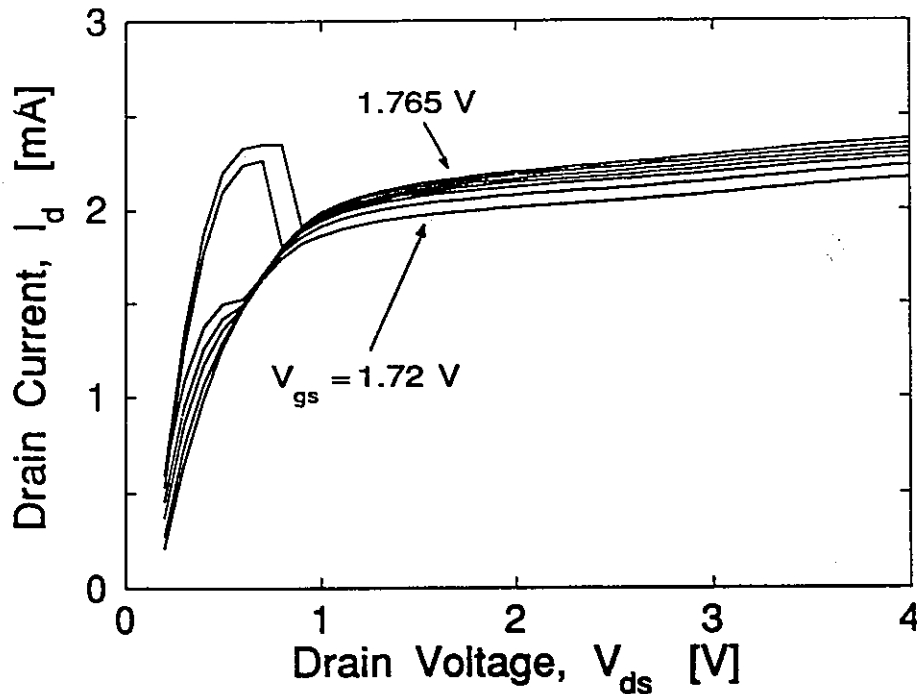
Figure 4.6   Drain characteristics of a typical device for $V_{gs} = 1.72$ V
to 1.765 V in steps of 5 mV, with $V_{cs} = 0$ V.

occur. However, the voltages applied were relatively small, ranging in magnitude up to only 0.3 V. When a larger negative voltage is applied to the collector, the effect is far more dramatic.

The drain characteristics of a typical BISFET are shown in Fig. 4.6 for $V_{gs} = 1.72$ V to 1.765 V in steps of 5 mV, with $V_{cs} = 0$ V. The sharp current transitions are evident. The characteristics are repeated in Fig. 4.7 in both the forward and reverse directions, but with $V_{cs} = -1.6$ V. The OFF-state current has decreased considerably, resulting in a relatively large switching ratio for the transitions associated with the gate-source feedback loop. This is a result of the effects described in Sections 4.1 and 4.2.
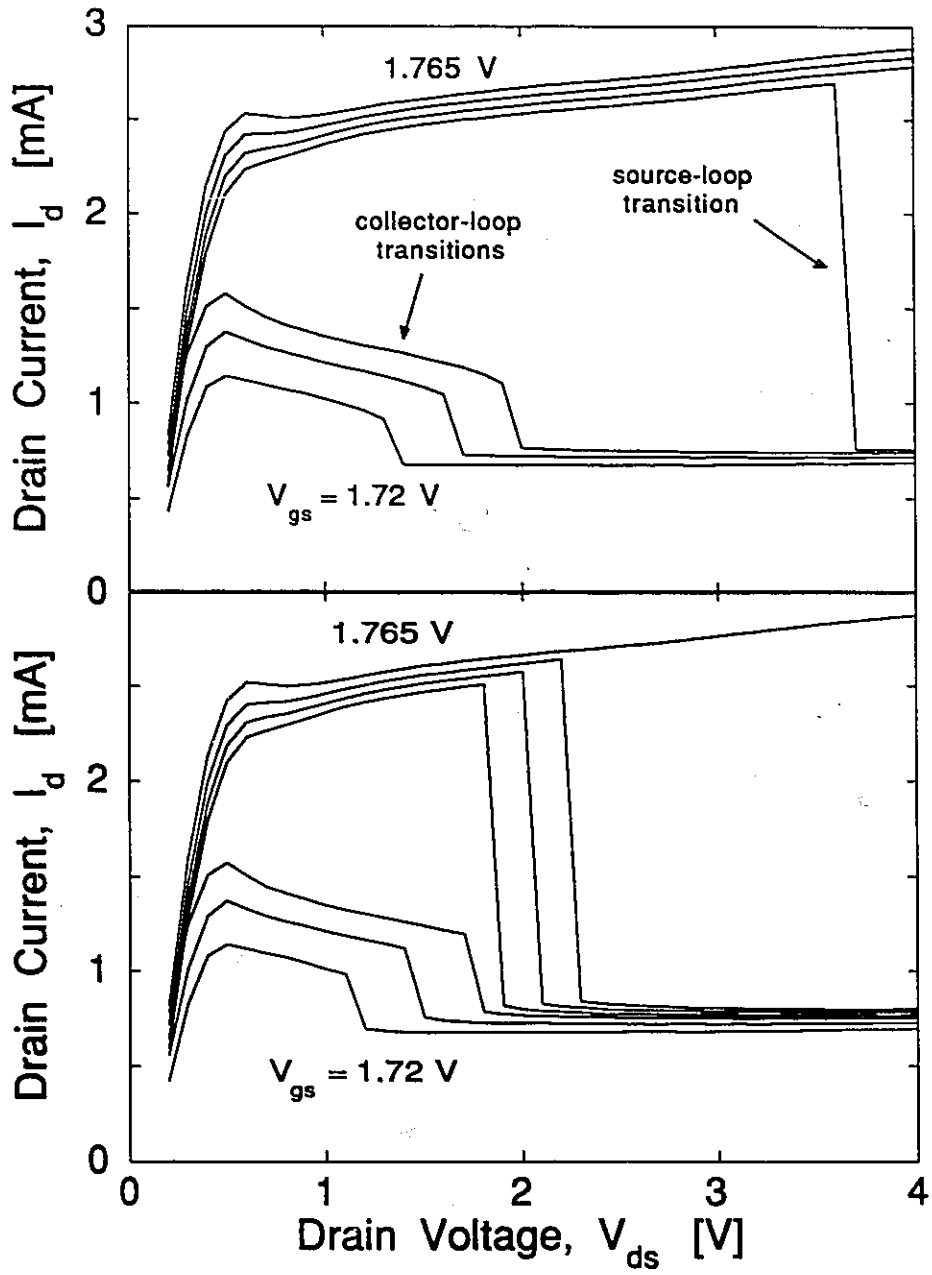
Figure 4.7   Repeat of drain characteristics in Fig. 4.6, with $V_{CS} = -1.6$ V. Characteristics are shown for both forward (top) and reverse (bottom) sweeps.

In addition to the source-loop transitions, however, a second, smaller set of transitions is visible in Fig. 4.7. The simultaneous presence of two sets of transitions indicates that a second feedback loop, lying between the gate and collector terminals, is operative within the device. Each set of transitions is thus associated with the change between the ON and OFF states of one of these loops. The possibility of this has previously been indicated in Chapter 2, where it was shown that both the gate-source and gate-collector paths in the device constitute *pδnpn* feedback loops. It was proposed that the BISFET could be implemented using either an integral-collector or a separate-collector configuration, i.e., using either the gate-source or the gate-collector feedback loop [1].

In the case described here, both loops operate simultaneously. This situation is illustrated in Fig. 4.8. The two feedback loops are intimately coupled together, in that they share the portion of the path from the gate, over the potential barrier, and into the active region. Beyond this point, the two loops diverge, so that the gate current, I_g, is split into two components: I_{gs} (to the source) and I_{gc} (to the collector terminal), such that

$$I_g = I_{gs} + I_{gc} \qquad (4.1)$$

That the smaller set of transitions in Fig. 4.7 is associated with the collector loop is evident from the evolution of the characteristics with increasingly negative V_{cs}. This is illustrated in Fig. 4.9, which shows the drain characteristics for a $V_{gs} = 1.72$ V, with a range of values of V_{cs} from -1.4 V to -1.9 V. No current transition is apparent for $V_{cs} = -1.4$ V. However, the smaller transition appears and grows progressively larger as the magnitude of V_{cs} is increased to and beyond the point where the collector loop turns on (see Section 2.5.6). Also, increasing
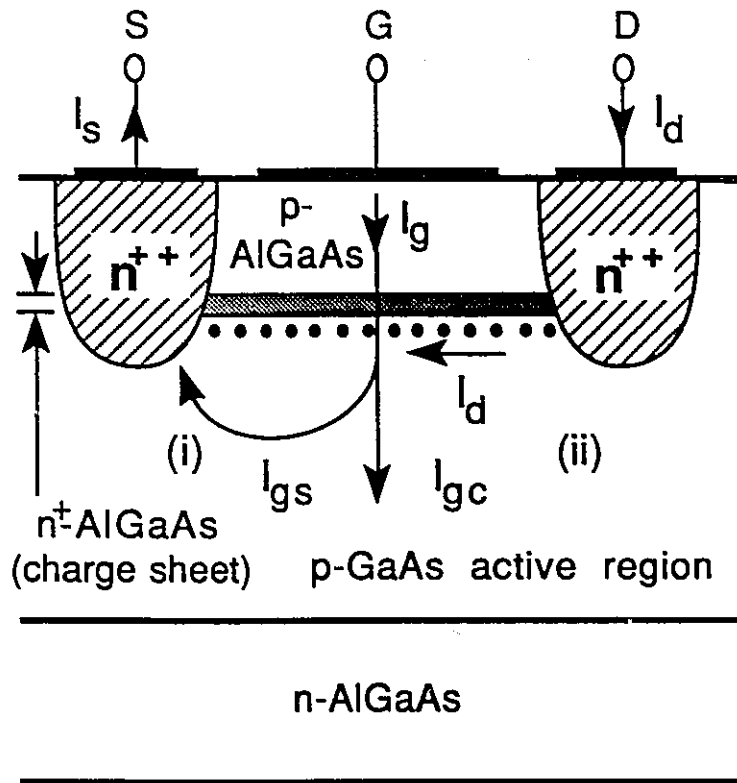
Figure 4.8   Diagram of the BISFET, showing the simultaneous existence of two feedback loops. The gate current, I_g, splits into two components in the active region. One component, I_{gs}, flows in the path from gate to source, while I_{gc} flows from the gate to the collector.

the magnitude of V_{cs} causes the collector-loop transition to shift to higher V_{ds}. This is due to the increasing feedback current which is injected by the collector, making the loop more difficult to turn off. Higher V_{ds} is thus required to switch the state of the gate-collector feedback loop.
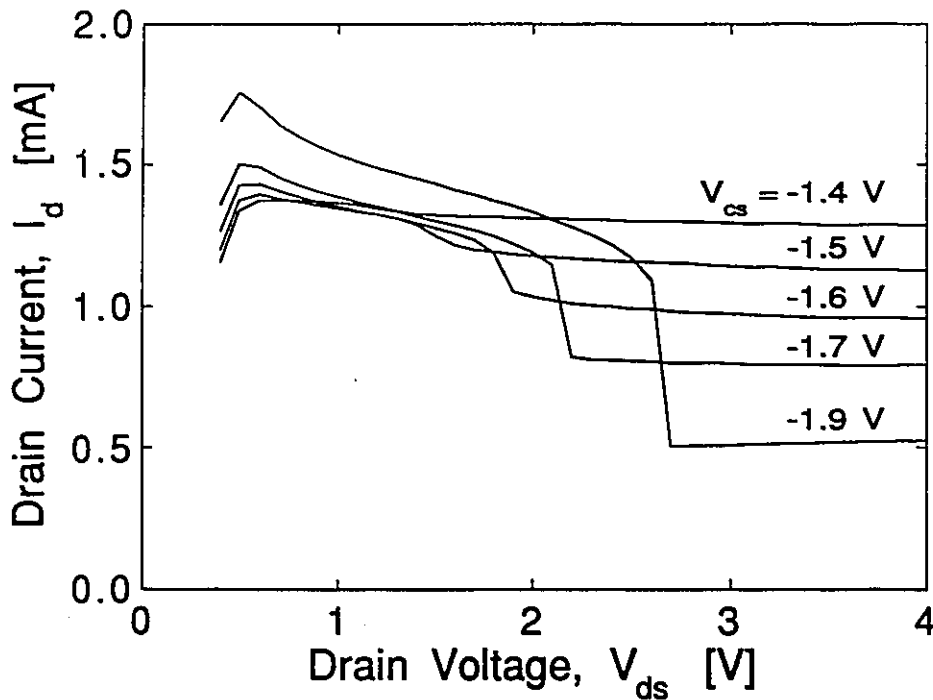
Figure 4.9   Forward-swept drain characteristics of the BISFET shown in Figs. 4.6 and 4.7, with V_{CS} as parametric variable. The characteristics are shown for fixed V_{gs} = 1.72 V, with V_{cs} = -1.4 V, -1.5 V, -1.6 V, -1.7 V, and -1.9 V. The transition illustrated here is associated with the turn-off of the gate-collector feedback loop, which operates simultaneously with the gate-source loop.

4.4   Gate-Drain Feedback Loop and Associated Transitions

4.4.1   Drain Characteristics

Two sets of current transitions in the drain characteristics are described above - one associated with the gate-source feedback loop, the other, with the gate-collector loop. In addition to these, a third distinct set of transitions has been observed. These are generally seen at higher values of V_{gs} than those at which

either the source- or collector-loop transitions appear. However, in some devices, the range of V_{gs} for the source-loop transitions overlaps with that for this third set of transitions.

Figure 4.10 shows a set of forward- and reverse-swept drain characteristics for a GaAs/AlGaAs BISFET for $V_{gs} = 1.74$ V to 1.84 V in steps of 20 mV, with $V_{cs} = 0$ V. The small transitions are those previously shown to be associated with the source loop. A set of much larger transitions is apparent at relatively low V_{ds}. The origin of these transitions is believed to lie in a third feedback loop lying between the gate and drain terminals of the device. Upon examining the curve for $V_{gs} = 1.84$ V in Fig. 4.10, we see that the ON- and OFF-state currents for the drain-loop transition are approximately 8 mA and 3.5 mA, respectively. The current levels for the source-loop transition are 3.5 mA and 3 mA. Thus, the on-off ratio, defined as the ratio of the ON- and OFF-state currents, is much larger for the drain loop (approximately 2.3) than for the source loop (1.2).

The forward and reverse sweeps of the drain characteristics are superimposed in Fig. 4.11 for $V_{gs} = 1.84$ V. Two hysteresis loops are apparent - one associated with the source loop, the other, with the drain loop.

4.4.2 Nature of the Gate-Drain Loop

With $V_{ds} = 0$ V, the source and drain terminals are, for all intents and purposes, geometrically and electrically symmetric. Thus, if feedback current can pass between gate and source, it can just as readily pass between gate and drain via the active region, resulting in a gate-drain feedback loop. As with the gate-collector loop in Section 4.3, it shares with the gate-source loop the portion of the path from the gate, past the barrier, and into the active region. From here,
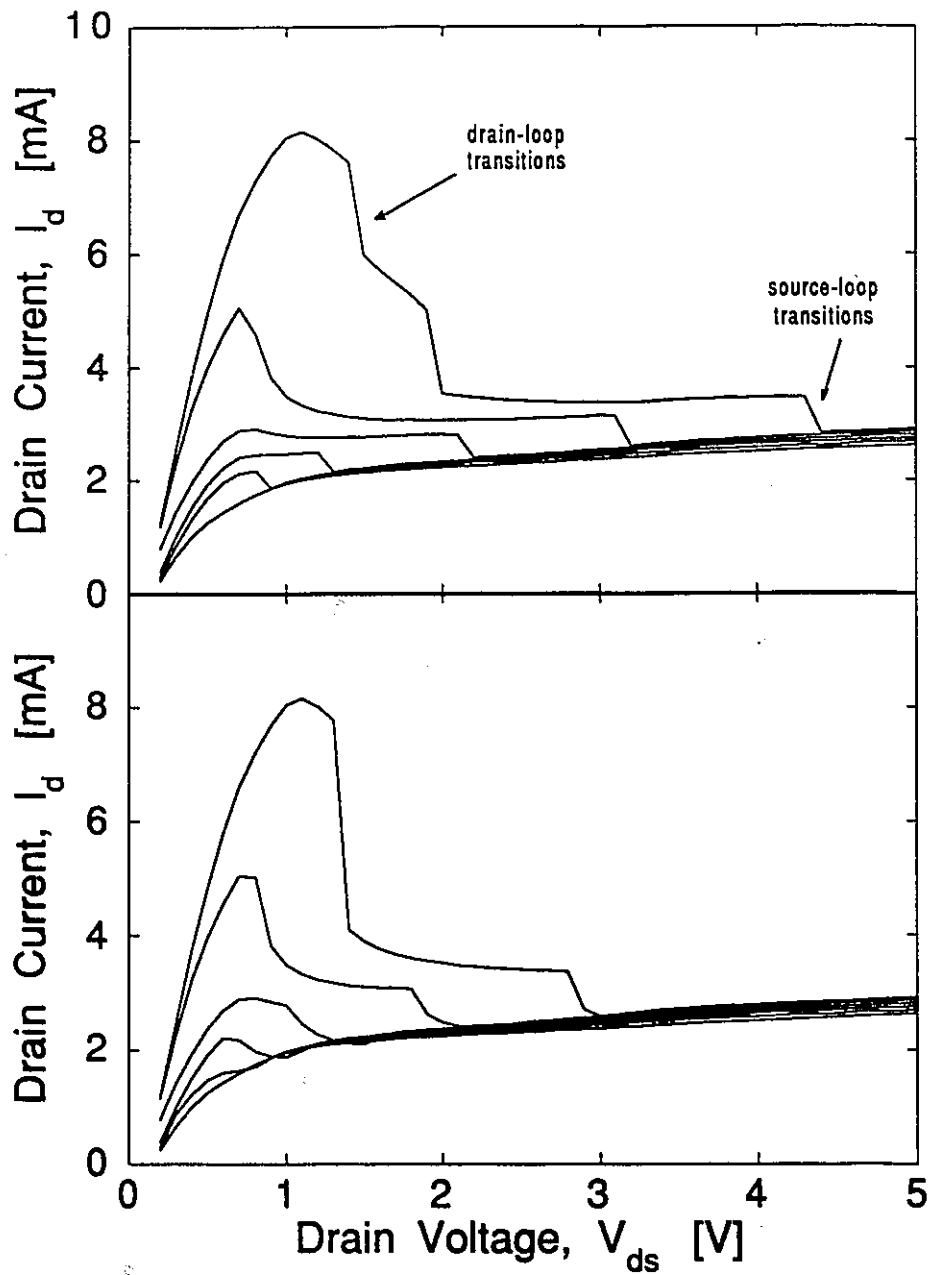
Figure 4.10 Forward- (top) and reverse-swept (bottom) drain
characteristics of a typical BISFET showing, in addition
to the small transitions associated with the gate-source
loop, a larger set of transitions whose origin is believed
to lie in a third feedback loop between the gate and
drain. The characteristics are shown for $V_{gs} = 1.74$ V to
1.84 V in steps of 20 mV, with $V_{cs} = 0$ V.
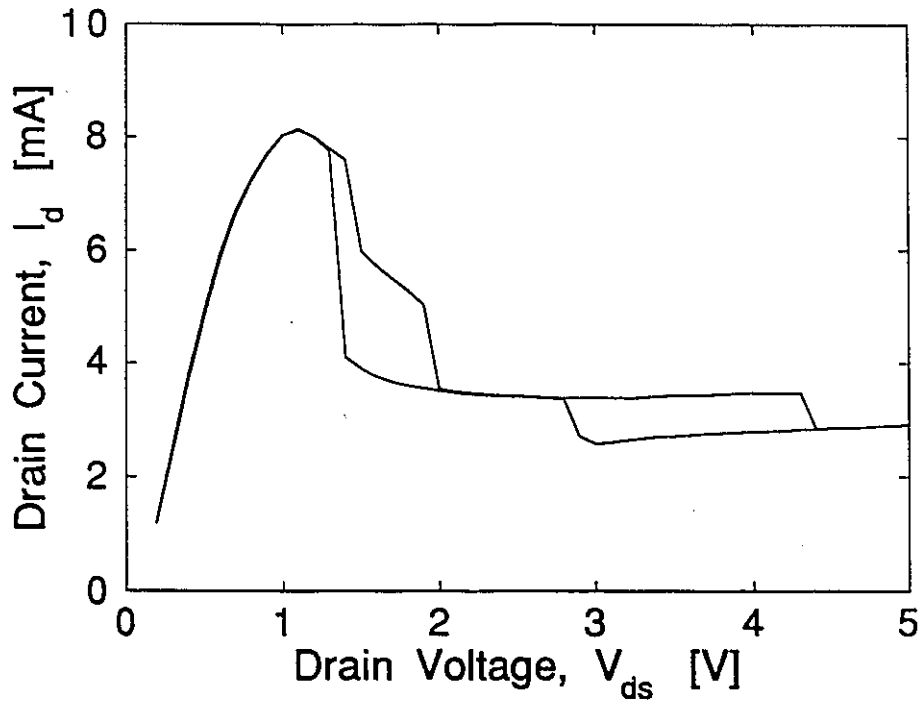
Figure 4.11 Superposition of forward and reverse sweeps of the drain
characteristics in Fig. 4.10 for $V_{gs} = 1.84$ V, showing
dual bistability. Two hysteresis loops are evident - one
associated with each of the source and drain loops.

however, the two loops diverge, with one terminating at the source contact, the

other, at the drain, as illustrated in Fig. 4.12. The gate current is thus split into

two components - I_{gs} (to the source) and I_{gd} (to the drain contact), such that

$$I_g = I_{gs} + I_{gd}$$
(4.2)

I_{gd} reduces I_d, so that

$$I_d = I_{ds} - I_{gd}$$
(4.3)
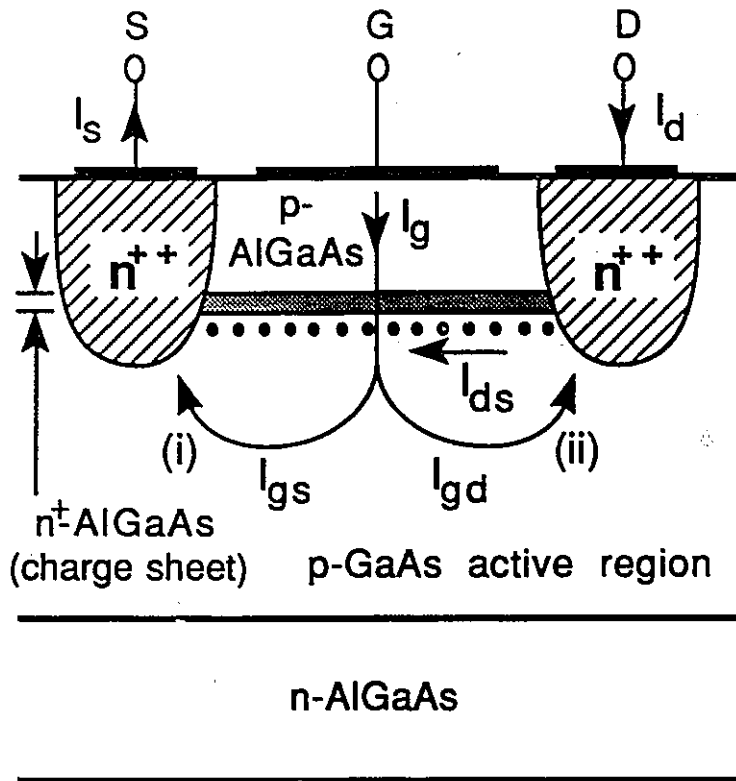
Figure 4.12 Diagram of the BISFET, showing the simultaneous operation of the gate-source and gate-drain feedback loops. The gate current, I_g, splits into two components in the active region. One component, I_{gs}, flows in the path from gate to source, while I_{gd} flows from the gate to the drain.

where I_{ds} is the component of I_d along the inversion channel. At low V_{ds} and I_{ds}, V_{gd}, and hence I_{gd}, are at their largest. Thus, large negative current flows through the drain terminal for drain voltages of 0 V or slightly higher when the feedback loop is on. This was seen in Fig. 3.3. Since this region is not of particular interest, and in order to avoid this large current flow (and, by symmetry, a correspondingly large current through the source contact), the characteristics of Figs. 4.10 and 4.11 were not swept all the way to $V_{ds} = 0$ V.

4.4.3   Origin of Transitions

The gate-drain feedback loop, like the gate-source loop, has distinct ON and OFF states. When it is in the ON state, the drain contact injects electron feedback current into the channel, both directly and via the active region. Thus, I_d is enhanced compared with the OFF state due to an increase in carrier population in the channel, as seen previously with the source loop in Section 3.3. This enhancement is in addition to that associated with the source loop.

The drain-source symmetry, of course, prevails only for $V_{ds} = 0$ V. Thus, increasing V_{ds} tends to reduce the forward bias on the drain-active region junction, until the gate-drain feedback loop eventually turns off. As seen in Fig. 4.10, this results in a dramatic drop in I_d at a relatively low V_{ds}, as the charge in the conduction channel drops. Conversely, decreasing V_{ds} eventually allows the drain-active region junction to become forward biased once more, causing the drain feedback loop to turn on again. The result is a substantial increase in I_d. At low V_{gs}, the transition associated with the drain loop occurs for even a small V_{ds}, since only a small reverse bias is required on the drain-active junction to turn the drain loop off. At the same time, this very small drain voltage does not allow the drain-current enhancement associated with the drain loop to grow very large before the loop turns off. Thus, at small V_{gs}, the transition disappears into the origin of the drain characteristics. As V_{gs} is increased, the drain loop becomes more and more difficult to turn off, so the drain-loop transition occurs at higher and higher V_{ds}. This also allows the enhancement of the drain current to grow relatively large before the drain loop turns off.

4.4.4 Switching Ratio

It was seen in Section 4.4.1 that the drain-loop transitions exhibit a much larger switching ratio (ratio between the ON- and OFF-state currents) than the source-loop transitions (approximately 2, compared with 1.4 for the source loop). The reason for this is not entirely clear, although it may be surmised that the source and drain feedback loops interact nonlinearly, so that the current enhancement is compounded dramatically when both feedback loops are on simultaneously. Ideally, when $V_{ds} = 0$ V, the drain loop is ON when the source loop is ON, and OFF when the latter is OFF. (In practice, of course, this condition may be relaxed somewhat due to differences in contact resistance at the source and drain, differences in electron injection from the two terminals, and similar effects.) However, as V_{ds} is increased above zero, larger and larger V_{gs} is required for the drain-loop transition to become visible, so that in general, the drain-loop transitions first become evident at higher V_{gs} than the source-loop ones.

It is not clear why a dramatic compounding of the ON-state current is not also seen when the collector feedback loop, described in Section 4.3, is turned on concurrently with the source loop. However, it should be borne in mind that both the geometry and electrical biasing of the gate-collector loop differ significantly from the gate-drain loop. (For instance, the spatial distribution of the feedback current injected into the channel via the active region is expected to differ substantially in the two cases.) The difference in behaviour of the two feedback loops could result from these factors.

4.4.5 Characteristics of the Drain-Loop Transitions

The drain-loop transition has been observed to have several characteristic shapes, depending on the bias conditions and the individual device used. In the first scenario, I_d drops abruptly from the ON-state level to the OFF-state level. This is similar to the behaviour resulting from the source and collector feedback loops. In the second scenario, the transition consists of two abrupt drops connected by a flat or sloping region in the characteristics. The reason for this two-stage transition is not known. In the third scenario, the transition is gradual, rather than abrupt. This suggests that the switching and holding voltages of the drain loop do not differ significantly from each other. Such a situation was illustrated in the gate characteristics of Fig. 3.9 by the curve for $V_{ds} = 0$ V.

When the difference between the switching and holding voltages vanishes, the feedback loop does not switch abruptly between distinct ON and OFF states. However, hole current still flows from the gate, over the potential barrier, and into the active region, serving to bias the latter. The result is a reduction in the width of the depletion layer, and hence the depletion space charge, in the active region adjacent to the charge sheet. This is accompanied by an increase in the channel charge, resulting in a larger I_d when I_g is large than when it is small. As V_{ds} is increased in this scenario, I_g is reduced as the height of the potential barrier is increased, reducing the bias in the active region, and thus, the channel charge and drain current. However, in the absence of an abrupt transition, this effect is a continuous one, leading to the gradual current cut-off seen in Fig. 4.10.

4.5   Simultaneous Operation of All Three Feedback Loops

4.5.1   Requisite Criteria

In the preceding sections, it has been demonstrated that three distinct, yet coupled, feedback loops operate in the BISFET. The first lies between the gate and source terminals. The second lies between the gate and the collector. Finally, the third feedback loop lies between the gate and drain. There is a distinct set of current transitions in the drain characteristics of the device associated with each of these loops.

It is to be remembered that considerable variation in the electrical characteristics has been observed amongst devices. This suggests that a multitude of subtle effects influence the behaviour of the devices, and that even slight variations in geometry, contact resistance, doping densities, and other device parameters can significantly affect such characteristics as the switching voltage, ON- and OFF-state currents, and range of gate voltage over which the transitions are observed. This complexity makes it difficult to explain the detailed differences from one device to another. However, one of the results of this variation is that the range of V_{gs} over which each feedback loop is observed to undergo transitions within the measurement range varies from device to device. Additionally, the values of V_{ds} at which the various transitions occur within this range vary considerably.

It has been found that all three of the feedback loops can be operational in the same BISFET under some bias conditions. The gate current is thus split into three separate components, as shown in Fig. 4.13 - I_{gs}, I_{gd}, and I_{gc}. Thus,
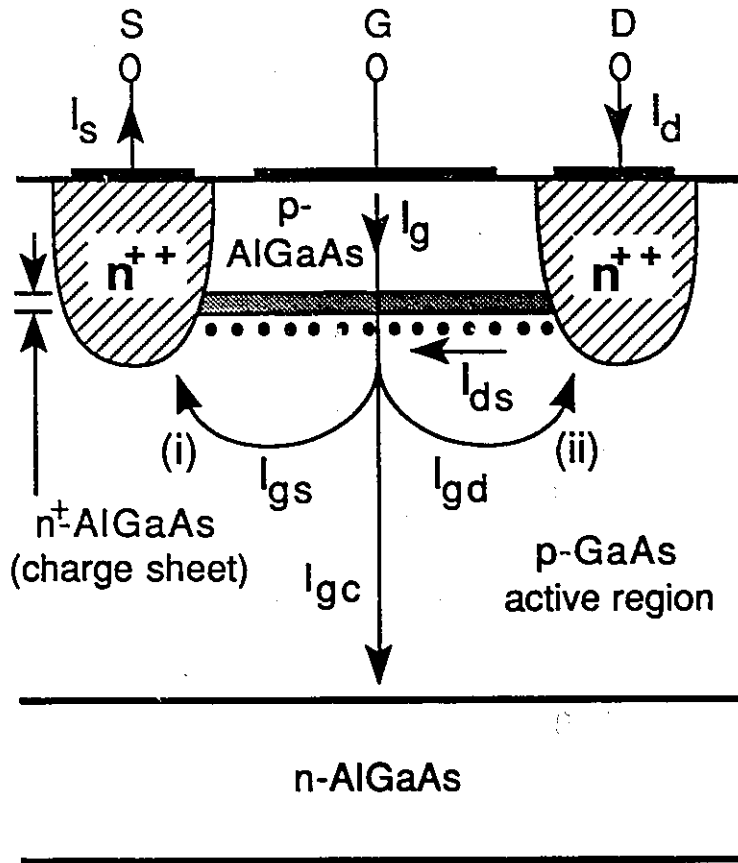
Figure 4.13 Diagram of the BISFET, showing the simultaneous operation of all three feedback loops, from the gate to the source, drain, and collector, respectively. The gate current, I_g, now splits into three components in the active region - I_{gs}, I_{gd}, and I_{gc}.

$$I_g = I_{gs} + I_{gd} + I_{gc} \qquad (4.4)$$

Since one set of transitions is sometimes masked, or absorbed, by another, it is not always possible to differentiate the various sets. However, because of the substantial variation amongst devices, the transitions associated with all three

Figure 4.14 Drain characteristics of a typical BISFET for
V_{gs} = 1.88 V to 1.93 V in steps of 5 mV, with V_{cs} = -
1.2 V. Transitions associated with all three feedback
loops are visible.

feedback loops can, in some cases, be readily distinguished in a single set of drain

characteristics for the appropriate bias conditions.

4.5.2 Drain Characteristics

A set of drain characteristics of a typical device illustrating all three sets of

transitions particularly well is shown in Fig. 4.14. The characteristics were

measured with increasing V_{ds} for V_{gs} = 1.88 V to 1.93 V in steps of 5 mV, and

V_{cs} = -1.2 V. For most of the values of V_{gs} shown, all three transitions are visible

in any single curve, providing support for the theory that the three sets of transitions actually result from three distinct feedback loops. The large transitions at low V_{ds} are clearly associated with the drain loop, as described in Section 4.4. The transitions seen in the intermediate range of drain current are associated with the source loop. This identification is made on the basis of the sensitivity of the transition voltage to V_{gs}, as well as by observing the evolution of the transitions with varying V_{cs}.

The characteristics of Fig. 4.14 are repeated with the same device for $V_{cs} = -1$ V at the top of Fig. 4.15. They provide an example of how the source-loop transitions sometimes swallow, or absorb, the collector-loop ones. The source-loop transition voltages have shifted to higher V_{ds} relative to Fig. 4.15 and overtaken the collector-loop ones. When the source loop turns off, the collector loop also does. However, the fact that all three feedback loops are still functioning is illustrated by the corresponding reverse-swept characteristics, which are shown at the bottom of Fig. 4.15. All three sets of transitions are again visible, although the source-loop ones occur very close to the drain-loop transitions.

4.5.3   Transitions in Gate and Source Currents

The drain characteristics of Fig. 4.14 demonstrate that the three coupled feedback loops in the BISFET operate simultaneously under appropriate bias conditions. The coupling between the various loops is demonstrated by an examination of the currents at the terminals other than the drain.

The drain characteristics of a typical device are shown in Fig. 4.16 for $V_{gs} = 1.73$ V to 1.82 V in steps of 10 mV, with $V_{cs} = -1.624$ V. All three sets of
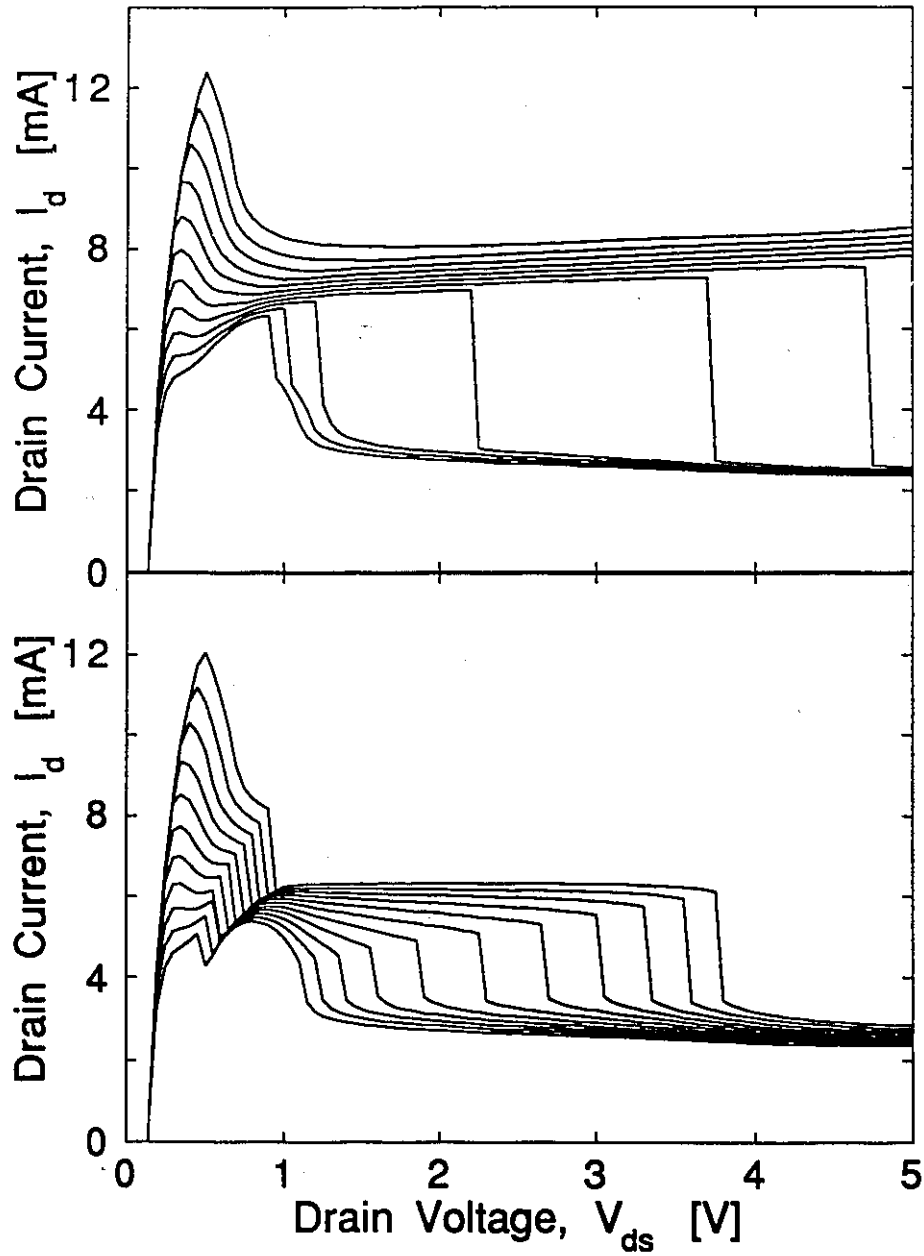
Figure   4.15 Forward-   (top)   and   reverse-swept   (bottom)
characteristics of the device in Fig. 4.14 for the same
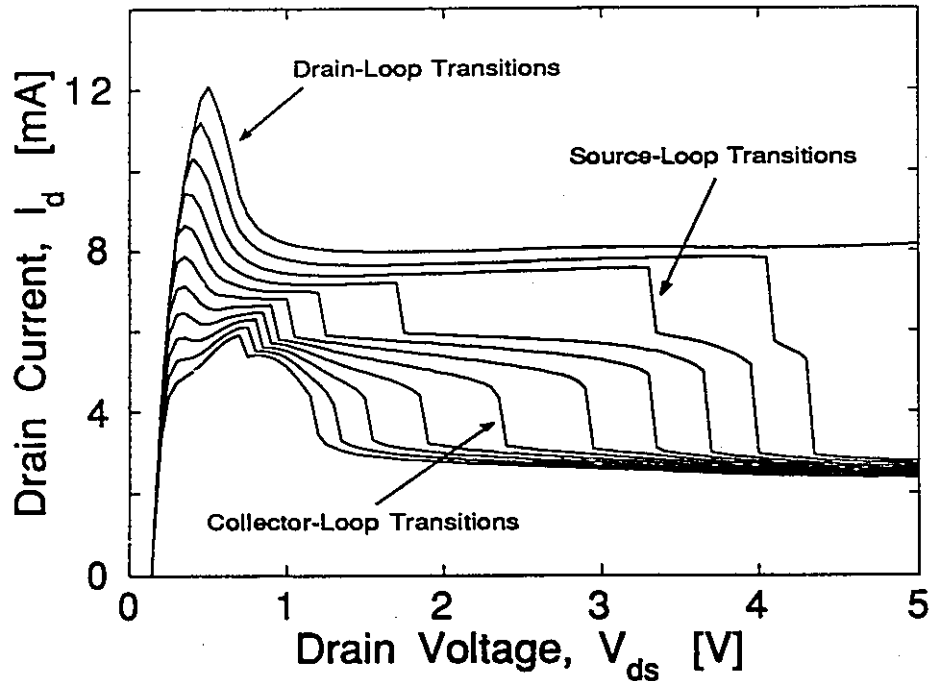values of V_{gs}, but with $V_{cs} = -1$ V.
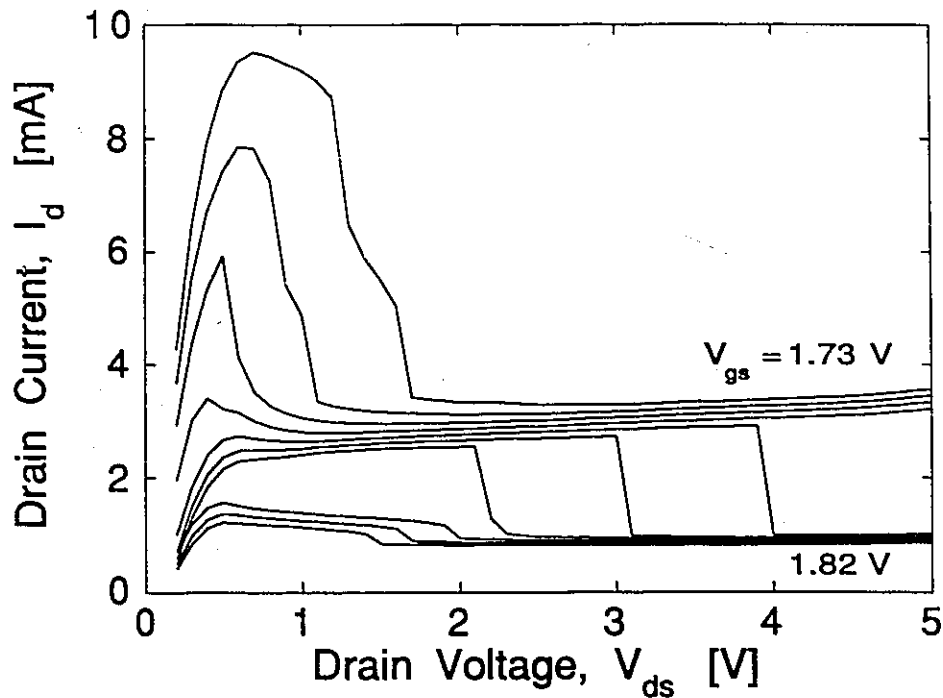
Figure 4.16 Drain characteristics of a typical BISFET for $V_{gs} = 1.73$ V to 1.82 V in steps of 10 mV, with $V_{cs} = -1.624$ V. Transitions associated with all three feedback loops are evident.

transitions are visible. The gate current is shown in Fig. 4.17 as a function of V_{ds}. The curves exhibit abrupt transitions having a direct correspondence with those in the drain characteristics. That is, for each transition in the latter, a corresponding change in current is seen in the former at the same V_{ds}. This includes the transitions associated with all three of the feedback loops. This is as expected, since Eq. 4.4 shows that the gate current is the sum of the components flowing to the source, drain, and collector terminals.

The variation of the source current, I_s, with V_{ds} is shown in Fig. 4.18. As with I_{gs}, a sharp transition is observed corresponding to each transition in the
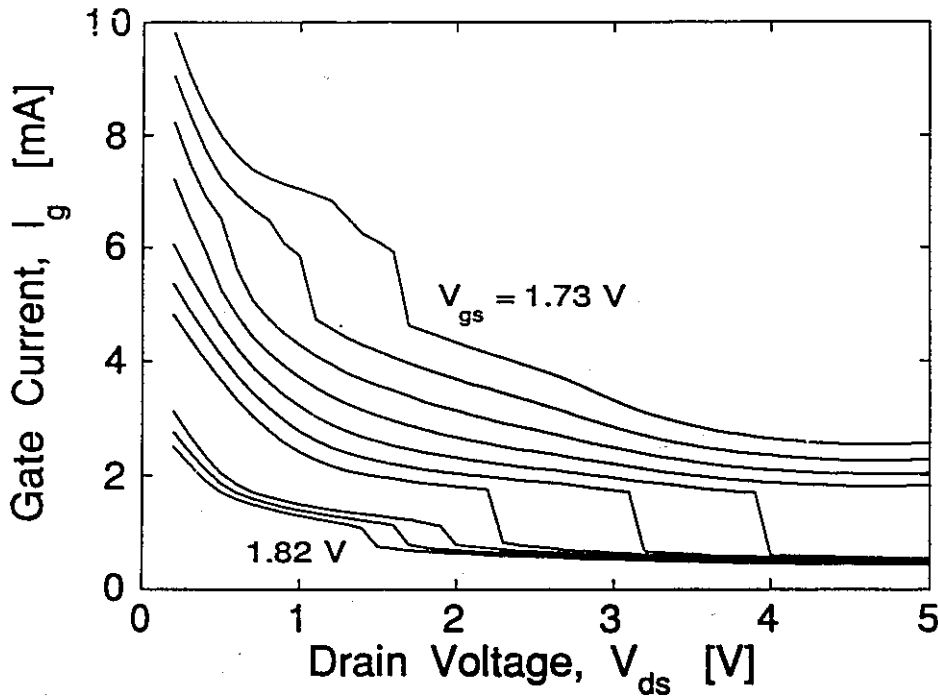
Figure 4.17   Variation of I_g with V_{ds} for the same device and bias
conditions as in Fig. 4.16.

drain characteristics. However, a comparison of Figs. 4.16 and 4.18 shows that I_s is substantially larger in magnitude than I_d. This is because the component of I_g associated with the source loop, I_{gs}, flows into the source. Although this is partially balanced by the component I_{gd} flowing into the drain, the latter is smaller for any V_{ds} greater than zero, due to the lower bias across the drain loop than across the source loop. Figs. 4.16-4.18 show that most of the difference between the source and drain currents is accounted for by I_g. As seen below, the remainder of the difference results from the collector current, I_c.
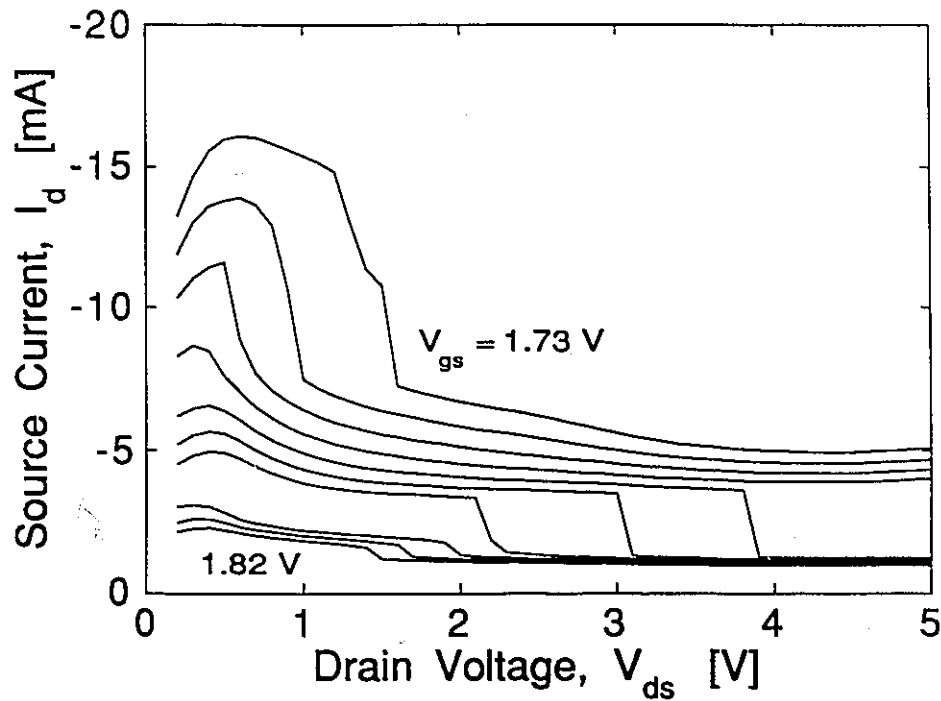
Figure 4.18   Source current as a function of V_{ds} for the same device
and bias voltages as in Figs. 4.16 and 4.17.

4.5.4   Current Transitions at Collector Terminal

Fig. 4.19 shows I_c as a function of V_{ds}. Note that the current is negative, reflecting the fact that the n-type collector supplies electrons to the active region, while sinking hole flow from the gate.   Again, the curves exhibit abrupt transitions having a direct correspondence with those in the drain characteristics. This result is particularly interesting, since only the gate-collector feedback loop terminates at the collector.   The source and drain loops do not, yet their changes of state are reflected in I_c.   This reflects the fact that the three feedback loops are coupled together.   The detailed behaviour of any one of them cannot be
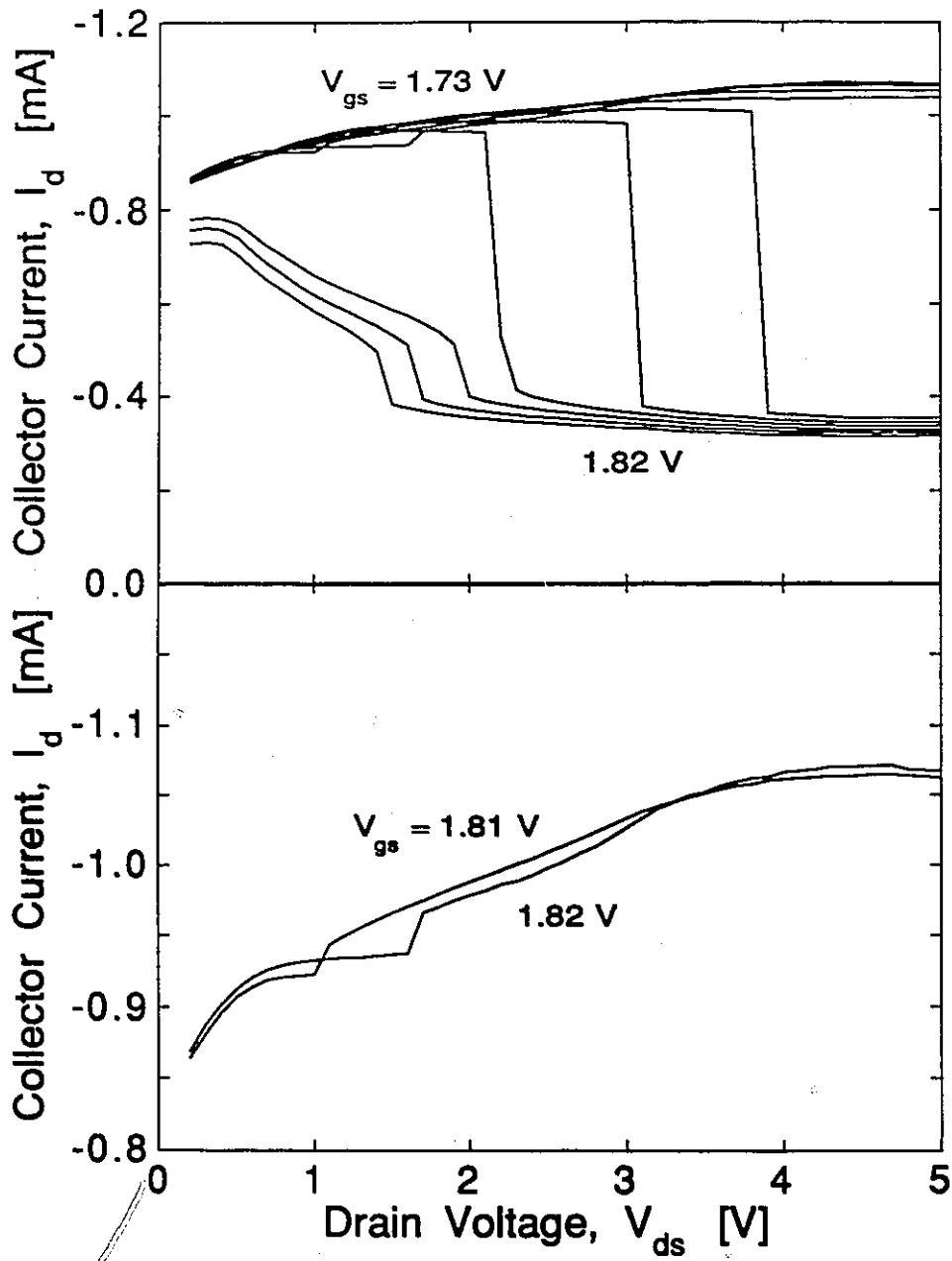
Figure 4.19   Variation of I_c with V_{ds} for the same device and bias conditions used in Figs. 4.15 to 4.18 (top). The curves for $V_{gs} = 1.81$ V and 1.82 V are plotted separately with an expanded vertical scale (bottom) to illustrate the increase in I_c as the drain loop switches off.

accurately explained without reference to the others.

It is interesting to note that I_c drops abruptly when the source and collector loops switch from the ON to the OFF state. This is expected, since the reduced current entering the active region decreases the bias across the active-collector (p-n) junction. However, when the drain loop is switched off, I_c actually increases. This effect is difficult to discern in Fig. 4.19, as a number of the curves cross each other. Thus, the two curves for $V_{gs} = 1.81$ V and 1.82 V are also plotted separately in Fig. 4.19, and the vertical scale is expanded. A possible explanation for the increase in I_c is as follows. The path from the collector, through the active region, and into the drain contact may be regarded as constituting a parasitic *npn* bipolar junction transistor (BJT). The collector forms the emitter, the active region corresponds to the base, and the drain may be regarded as the "collector" (quotation marks indicate that this term refers to the parasitic transistor, and not to the BISFET terminal of the same name) of this parasitic component.

When the drain loop is on, the active region potential is relatively large, and the drain-active, or "collector"-base, junction is forward biased. Thus, although the active-collector (or base-emitter) junction is forward biased, no electrons can flow into the "collector" from the active region. When the drain loop turns off, the base-emitter bias is reduced. However, the "collector"-base junction goes from a forward-biased state to a reverse-biased one. Thus, the parasitic transistor begins conducting current. This increase in current, which must be supplied by the collector of the BISFET, more than compensates for any reduction in I_c flowing to the gate terminal via the active region.

Chapter 5

OPTICAL BISTABILITY IN THE BISFET

5.1 Optical Emission from the BISFET

GaAs/AlGaAs inversion channel structures produce optical emission when driven with an electrical current. This property has been used to implement light-emitting devices (LED's) and lasers [18],[37]-[39]. Not surprisingly, it has been found that the BISFET also emits light under certain conditions. The light output from the device has been found to be closely correlated with the gate current flowing through it. Specifically, optical output is only produced when gate current is flowing in the device. This is because the light is emitted by radiative recombination of carriers in the active region, as shown in Fig. 5.1. For this to occur, both electrons and holes must be supplied. When the feedback loop is in the OFF state, little or no current enters the active region. However, when it is in the ON state, holes (in an n-channel device) are injected over the potential barrier from the gate. Electrons are injected into the active region from the collector (or the source in the integral-collector configuration). The electron and hole currents

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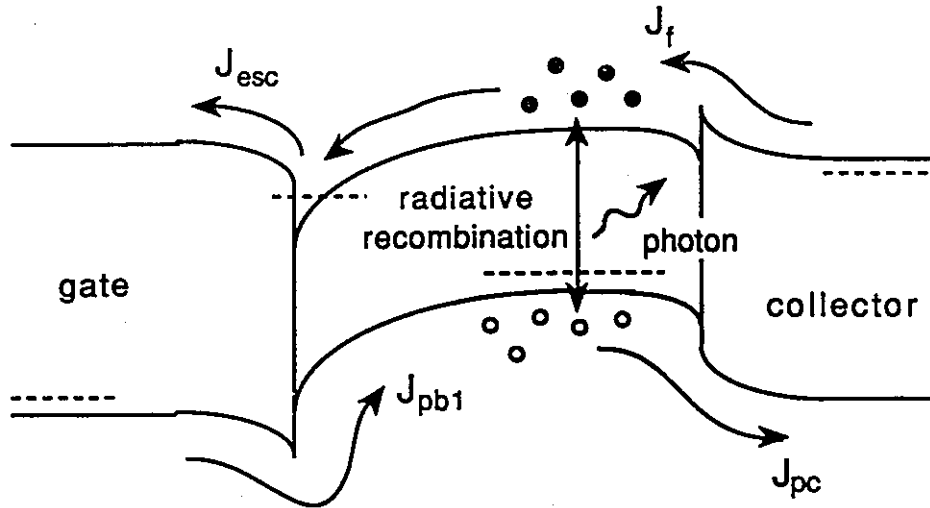
Figure 5.1   Energy band diagram of the GaAs/AlGaAs BISFET in the ON state, showing injection of electrons and holes into the active region from the gate and collector, respectively. Some of these carriers undergo radiative recombination in the active region, resulting in light emission.

in the feedback loop vary in tandem, of course. Thus, the BISFET emits light when it is in the ON state, but not in the OFF state.

5.2   Optical Output Characteristics

5.2.1   Optical Drain Characteristics

The optical output characteristics were measured using the apparatus shown in Fig. 5.2. The optical output from the device was monitored by mechanically chopping the emitted light and focusing it on a silicon *p-i-n* photodetector. The electrical signal from the detector was supplied to a Stanford

SR-500 lock-in amplifier. The output from the lock-in was then sent to the voltage monitor on the HP 4145B parameter analyzer.

Figure 5.3(a) shows the complementary transfer characteristics of the device, defined in Chapter 4. Fig. 5.3(b) shows the variation of the light output as a function of V_{ds} for a forward sweep. The latter are referred to as the optical drain characteristics. Both sets of characteristics are given for gate voltages ranging from 1.70 V to 1.76 V in increments of 10 mV. The integral-collector
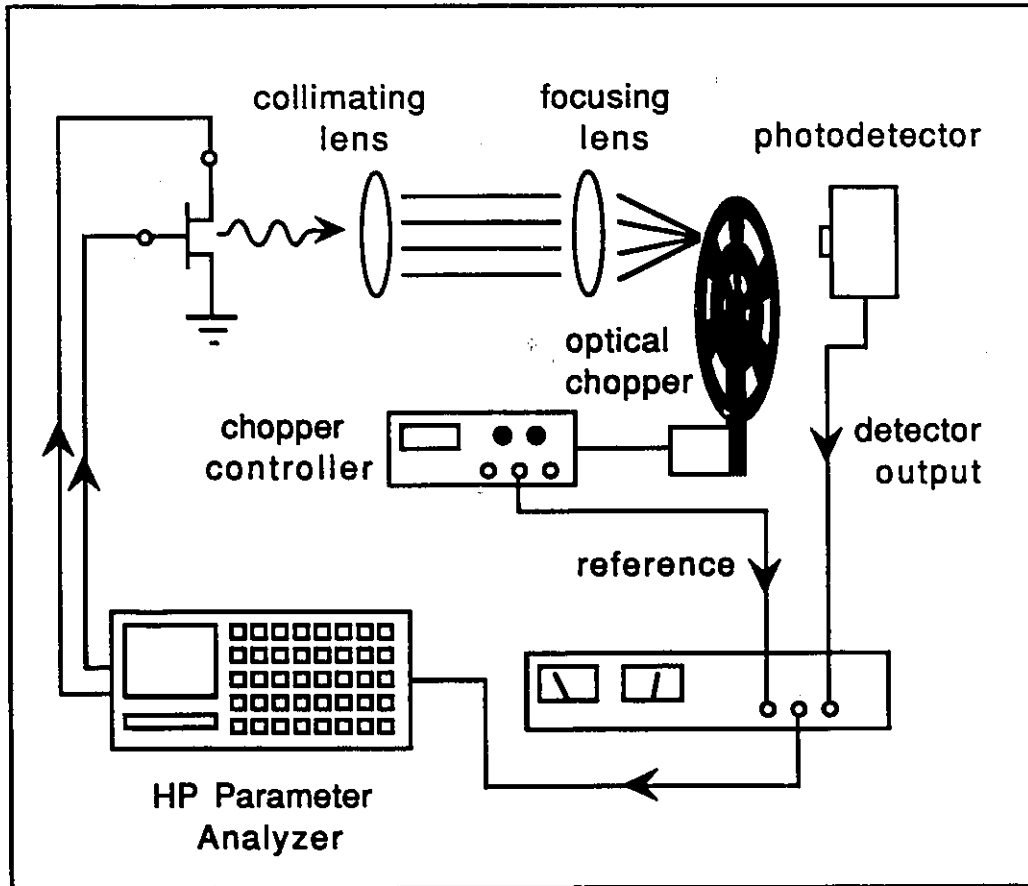
Figure 5.2   Schematic diagram of experimental apparatus used to measure optical output characteristics of the BISFET.
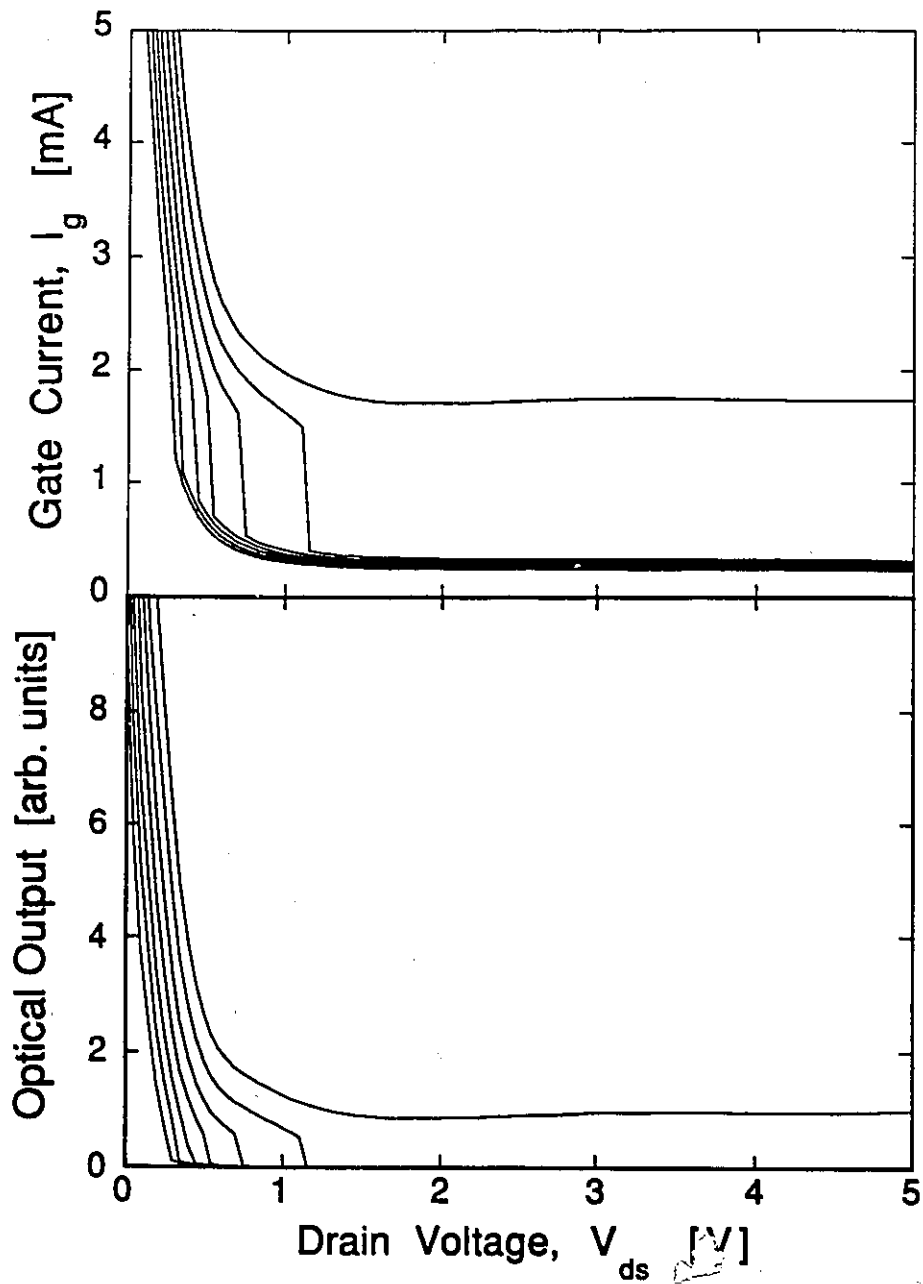
Figure 5.3 (a) Complementary transfer characteristics of the BISFET, showing gate current as a function of drain voltage, and (b) optical drain characteristics of the BISFET, showing optical output from the device as a function of drain voltage. Both sets of characteristics are shown for $V_{gs} = 1.70$ V to 1.76 V in steps of 10 mV. The optical output transitions correspond to those seen in the electrical characteristics characteristics.

configuration was used for these measurements, so that the source supplies the feedback current. The light emission from the BISFET is seen to be relatively high at low V_{ds}, when the feedback loop is on. In this state, substantial gate current flows in the device, so that holes are injected past the potential barrier into the active region. These recombine radiatively with electrons which are injected into the active region via the forward-biased *p-n* junction formed by the latter and the source contact. However, as V_{ds} is increased, the gate current is reduced as the potential barrier rises, in the manner described in Section 2.5.2. The light output thus falls off rapidly with increasing V_{ds}. At sufficiently high drain bias, the feedback loop turns off as the small-signal gain falls below unity, and the gate current drops abruptly. When this occurs, there is a corresponding drop in optical emission. In the OFF state, the light output is zero within the limits of the measurement noise. This transition, referred to as optical switchdown, is found to correspond under all bias conditions with the switchdown seen in the drain and complementary transfer characteristics, as evidenced by Fig. 5.3. From Fig. 5.3(b), it is seen that the optical transition voltage increases rapidly with V_{gs}. Again, this is consistent with the electrical results.

A reverse sweep of the optical drain characteristics is given in Fig. 5.4 for the same bias conditions as in Fig. 5.3. The optical emission is essentially zero in the OFF state for all gate voltages shown. However, when the feedback loop returns to the ON state, the light output undergoes an abrupt increase. This transition, referred to as optical switchup, again corresponds exactly with the electrical switchup in the drain characteristics and the sharp increase in gate current as the feedback loop turns on, seen in Section 3.5. It is noted that the transitions move to lower V_{ds} compared with the forward sweep for the same V_{gs}. The switchup transitions are also less sensitive to gate bias than the optical
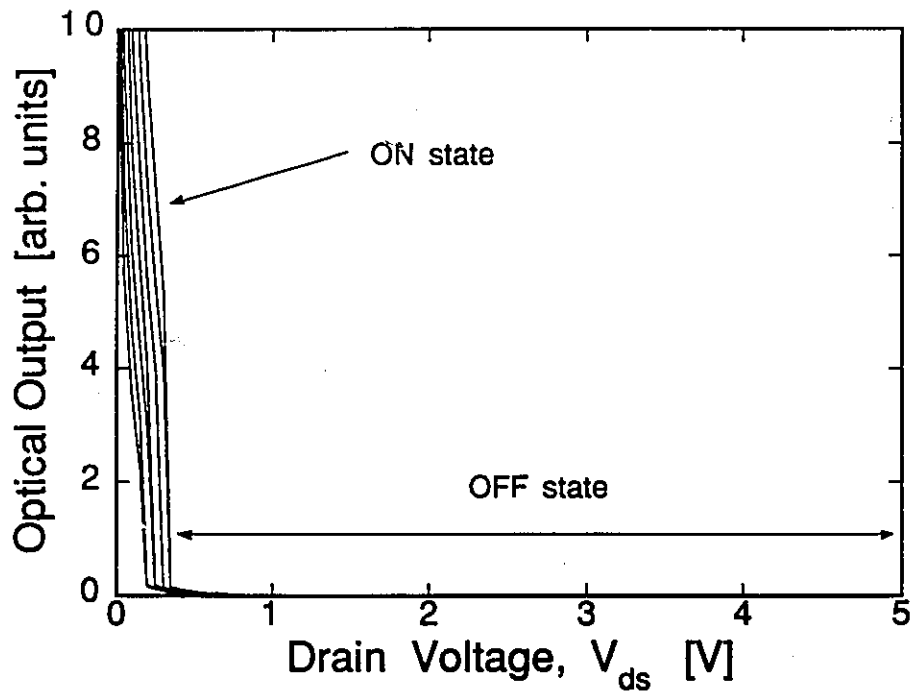
Figure 5.4 Reverse sweep of optical drain characteristics corresponding to Fig. 5.3.

switchdown. This is consistent with the electrical characteristics, in which the transition is far more sensitive to V_{gs} in the saturation than in the ohmic regime.

The forward and reverse sweeps of the optical drain characteristics for a single gate voltage of 1.75 V are superimposed in Fig. 5.5, clearly showing hysteresis in the optical output. The slope associated with the transitions is a result of the expansion of the horizontal scale. The transition has actually been observed to be abrupt to within the 1 mV resolution of the instrumentation used, as were the transitions in the drain and gate currents. The switchup transition in Fig. 5.5 occurs at approximately 0.3 V, compared with the switchdown voltage of about 1.2 V for the same V_{gs}. This gives an optical hysteresis of about 0.9 V.
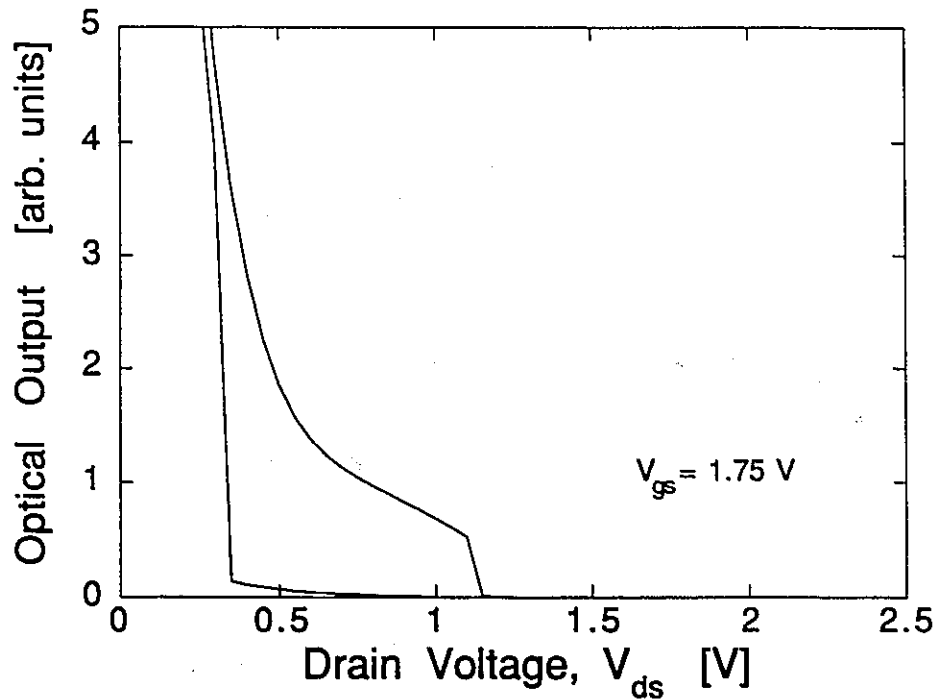
Figure 5.5 Forward and reverse optical drain characteristics for
$V_{gs} = 1.75$ V, showing hysteresis.

However, referring to Figs. 5.3 and 5.4, we see that for $V_{gs} = 1.76$ V, the switchdown transition has moved beyond the measurement range, so the hysteresis is in excess of 4 V.

A lower bound of 20 dB may be placed on the optical switching ratio between the ON and OFF states, γ. The actual value of γ is difficult to determine accurately, as the OFF-state output level is essentially zero, within the noise limit and offset error of the instrumentation. Thus, γ is probably much higher than the figure quoted above.

5.2.2   Differential Characteristics

The differential optical drain characteristics of the BISFET were computed from the absolute output characteristics shown in Fig. 5.3. The results are plotted in Fig. 5.6 for both the forward and reverse sweep directions, with $V_{gs} = 1.75$ V. The vertical axis gives dL/dV_{ds}, where L is the optical output. The abrupt transitions in optical output observed in the optical drain characteristics appear as essentially delta functions in the differential characteristics. The delta functions appear to have substantial width; however, this is simply due to the finite spacing between data points and the expansion of the horizontal scale. The peak heights are also under-represented due to the data-point spacing.
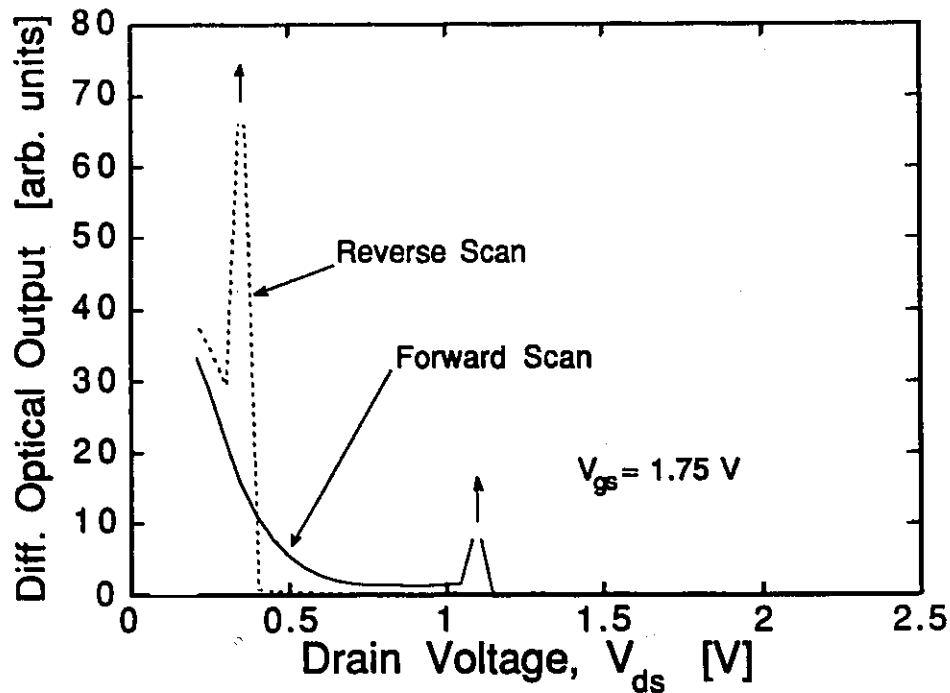
Figure 5.6 Differential optical drain characteristics, showing
differential optical output vs. drain voltage for both the
forward and reverse sweep directions.
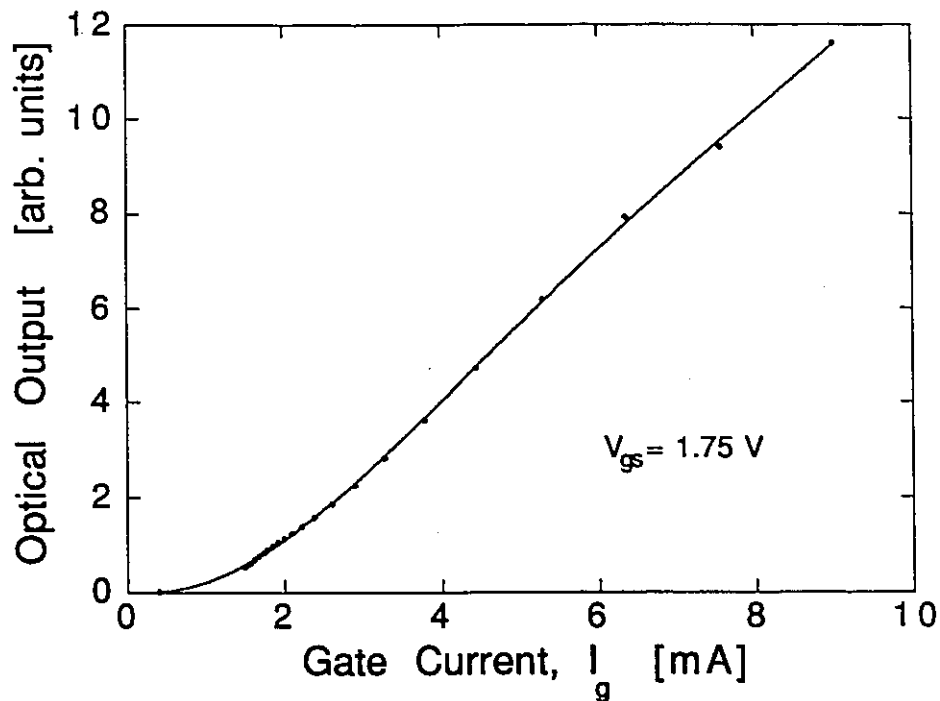
Figure 5.7   Optical output from the BISFET as a function of gate current. The relationship is approximately linear, like that expected for a typical light-emitting diode (LED).

The strong correlation between the light output and the gate current flowing in the device is illustrated in Fig. 5.7. This shows the variation of L with I_g, also known as the light-current characteristic. The curve is approximately linear, with a slight upward curvature at low current. This is roughly what would be expected for a light-emitting diode with I_g as the drive current.

5.3   Carrier Flows and Optimization of Optical Output

The fact that the OFF-state light output drops to zero yields some interesting information about the carrier flows within the device. Note that the

gate current in the OFF state, as given by the complementary transfer characteristics of Fig. 5.3(a), does not drop to zero, but rather, saturates at a value of approximately 0.3 mA for $V_{gs} = 1.75$ V. However, the near-zero optical emission indicates that either one or both of the following conditions hold in the OFF state:

(1)   Very few holes are emitted over the barrier from the gate to the active region.

(2)   Very few electrons diffuse into the active region from the source contact and the portion of the channel immediately adjacent to it.

This suggests that the OFF-state gate current is due to other carrier transport mechanisms. Two possibilities are proposed to explain this.

If Condition 1 applies, then two possible mechanisms are proposed. The first of these is thermionic emission of electrons into the gate from the inversion channel, particularly from the portion near the source, as this is where the channel potential is most shallow. The second component which can contribute to the gate current is leakage from the gate directly into the source contact, since the latter penetrates the gate layer, forming a physically small but potentially effective *p-n* junction. Under conditions of interest, this junction is forward biased, possibly allowing some leakage current to flow.

If Condition 2 holds, it indicates that electron flow from the source enters the channel directly in the OFF state, since the source-active region junction is not significantly forward biased. However, in the ON state, with this junction under

substantial forward bias, a significant portion of the electron flow from the source must diffuse over the junction into the active region. From there, most of it flows into the channel via drift and diffusion. However, a portion of it recombines with the holes injected by the gate to emit optical radiation.

The optical efficiency of the BISFET structure studied here is observed to be relatively low, due to the poor carrier confinement in the neutral region of the active layer. Electrons that diffuse into the active region experience no confining potential keeping them from diffusing and drifting back into the inversion channel. Better electron confinement could be achieved by making the material between the intrinsic channel layer and the neutral region of the active layer of AlGaAs rather than GaAs. However, this would also reduce the efficiency of both the feedback from the source and the optical emission. This problem could be remedied by resorting to a separate-collector design for the BISFET, mentioned above. Alternatively, instead of placing an AlGaAs barrier between the channel and the active region, a confinement region or quantum well of InGaAs or some other small-bandgap material could be placed in the latter. This would confine carriers without preventing electrons from diffusing from the source to the active region. Thus, the optical efficiency would be improved. However, the feedback efficiency would still be reduced, since the electrons would be less likely to drift or diffuse into the channel. Another way of looking at this is that carriers undergoing recombination are essentially stolen from the feedback current.
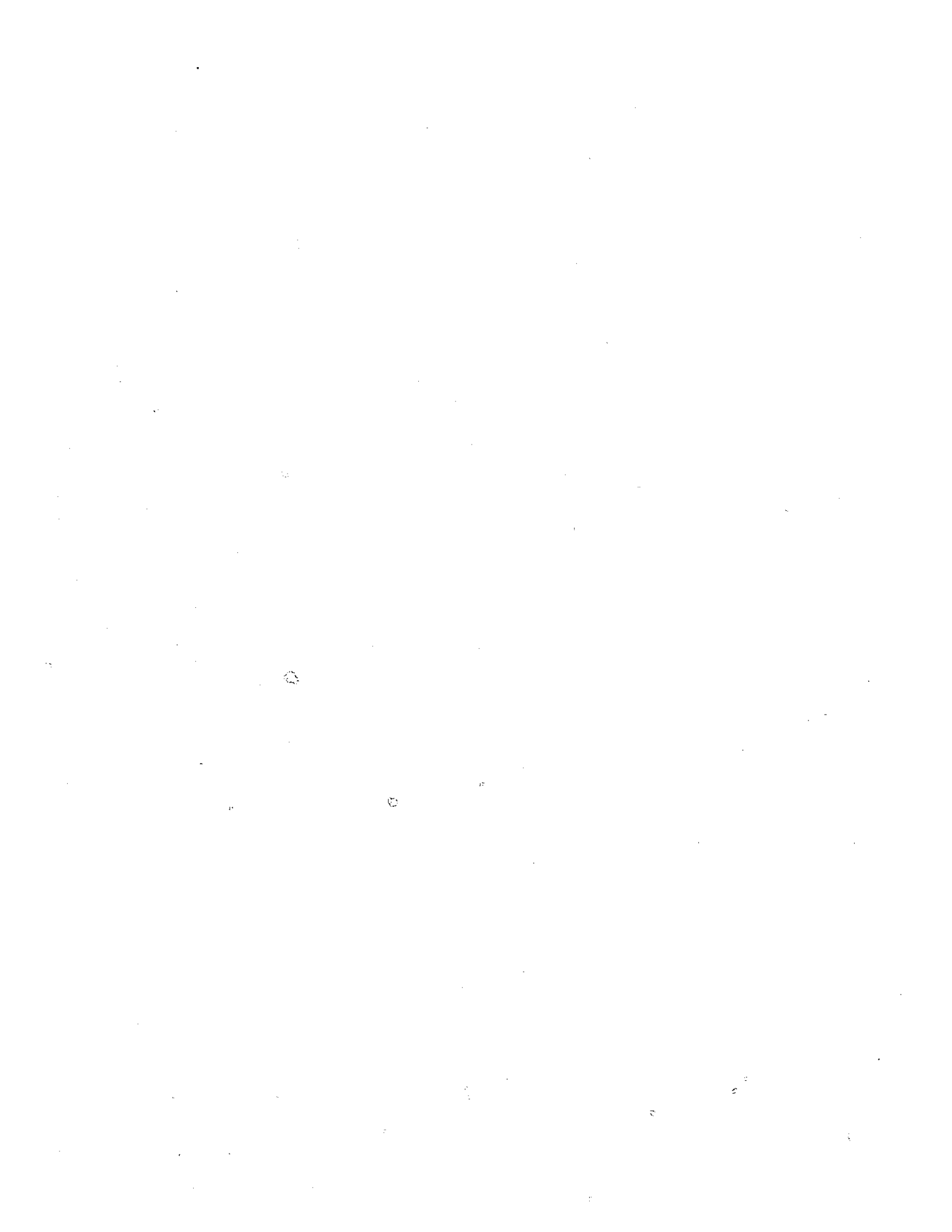
Chapter 6

OPTICAL CONTROL OF THE BISFET

In this chapter, the effects of optical excitation on the electrical characteristics of the BISFET are presented. In particular, it is shown that the electrical characteristics of the BISFET can be controlled using an optical input applied to the device. The drain voltage at which the electrical transitions in the device occur is found to vary with incident optical intensity.

6.1 Illumination of the BISFET

Optical excitation of the BISFET was achieved by focusing on it the output of a helium-neon laser having a wavelength of 6328 Å. The nominal beam power was 5 mW. The incident light generates electron-hole pairs in the device, with the electrons drifting into the conduction channel. The holes drift into the active region, as shown in Fig. 6.1, serving to forward bias the p-n junction formed by the source and the active region. As described in Chapter 2, this junction provides the feedback current. This, in turn, causes additional electron injection into the channel.

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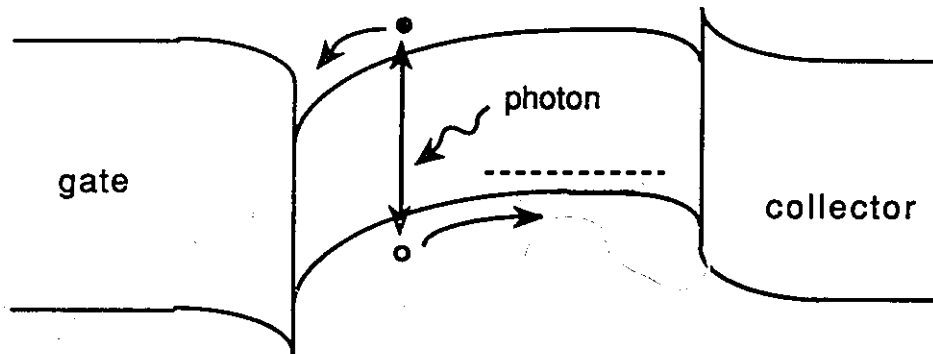
Figure 6.1   Band diagram of the BISFET, showing generation of electron-hole pair by incident photon. The electron drifts into the conduction channel, while the hole enters the active region.

A variable attenuator was placed in the beam and used to vary the light intensity incident on the device. Because of the difficulty of determining the optical coupling efficiency, a measure of the total optical power coupled into the device was obtained by taking the reverse-biased gate characteristics under the illumination conditions of interest. These give the photocurrent collected from the device in reverse bias, which is expected to be roughly proportional to the optical injection current under forward bias. The nominal absorbed optical power was calculated on this basis. Thus, while it may be taken as a measure of the level of excitation, it does not necessarily correspond to the absolute power level.

6.2 Effect on Drain Characteristics

The forward- and reverse-swept drain characteristics of a typical BISFET were measured as in Chapter 3. They are shown in Fig. 6.2 for $V_{gs} = 1.70$ V,

Figure 6.2   Drain characteristics for gate voltages of 1.70 V, 1.72 V, 1.74 V, 1.75 V, 1.754 V, and 1.756 V.   The characteristics are given for the forward (top) and reverse (bottom) sweep directions, with no illumination applied to the device.

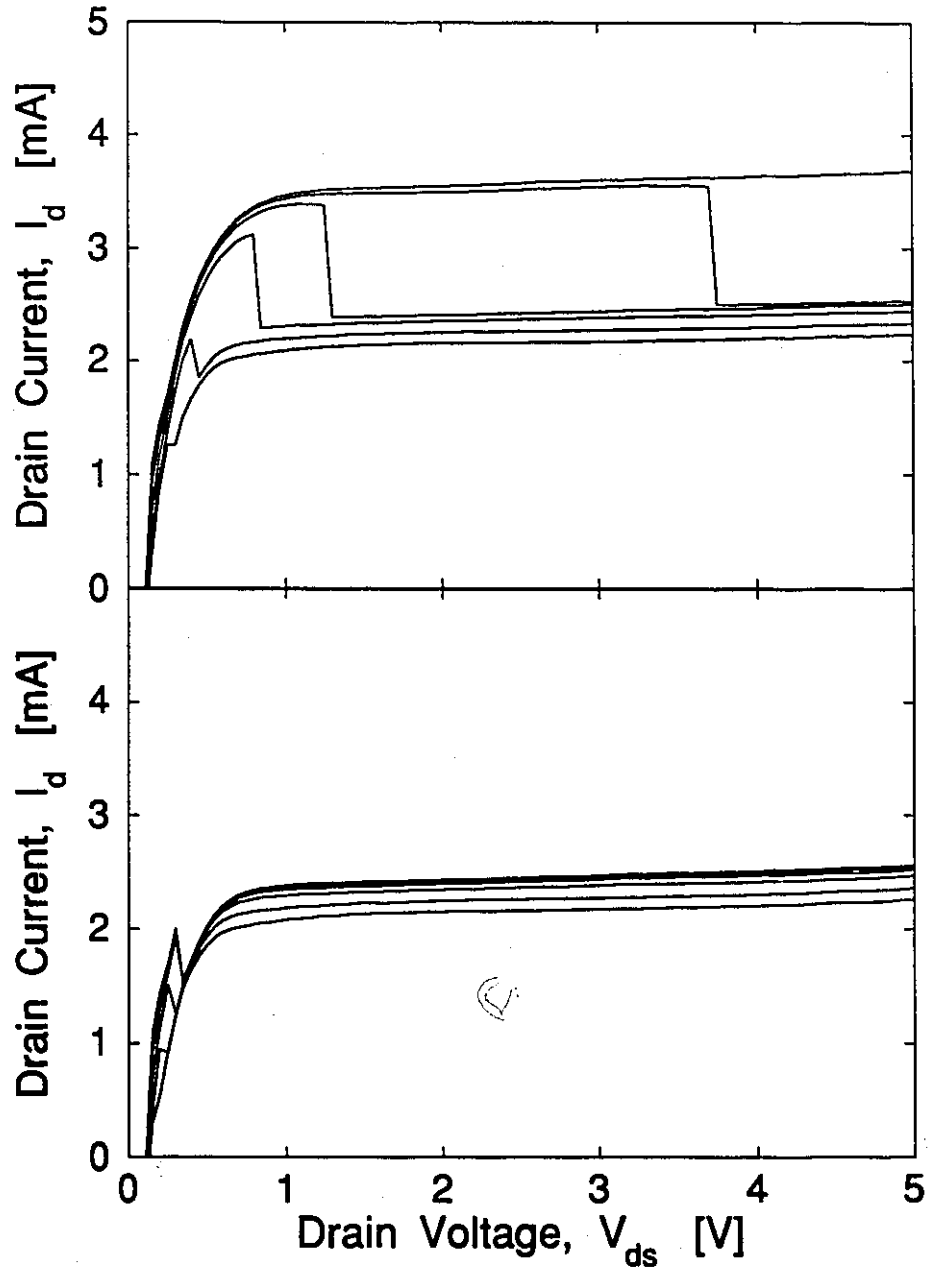1.72 V, 1.74 V, 1.75 V, 1.754 V, and 1.756 V, and display abrupt transitions similar to those shown earlier. The characteristics were monitored for various levels of incident optical intensity. Fig. 6.3 shows the forward- and reverse-swept characteristics for the same gate voltages as in Fig. 6.2, with a relatively low absorbed light level of 12 μW, calculated as described above. The location of the switchdown transitions (forward-swept characteristics) is very sensitive to light intensity. Comparison of Fig. 6.3 with Fig. 6.2 reveals that V_{ds2} has decreased compared with the no-light case. The switchup transition does not appear to be significantly affected by illumination.

The drain characteristics are repeated once more in Fig. 6.4, this time for a much higher light level of 50 μW. *Now, the switchdown transition voltages begin to increase, beyond even the no-light values.* Again, the switchup transition does not appear to be affected. In both the low- and high-illumination cases, the current levels in both the ON and OFF states are higher than when no light is present. The increase is greater for high than for low illumination.

6.3 Origins of Behaviour

An explanation of the behaviour of the BISFET under illumination is proposed in terms of the optical injection of carriers into the conduction channel. Normally, the current conservation condition, given by Eq. 2.21, holds along the channel of a FET:

$$\frac{dI_{ch}(x)}{dx} = 0 \qquad\qquad (2.21)$$

Figure 6.3   Drain characteristics for the same gate voltages as in Fig 6.2, with optical injection level of 12 μW. As before, the characteristics are given for the forward (top) and reverse (bottom) sweep directions.
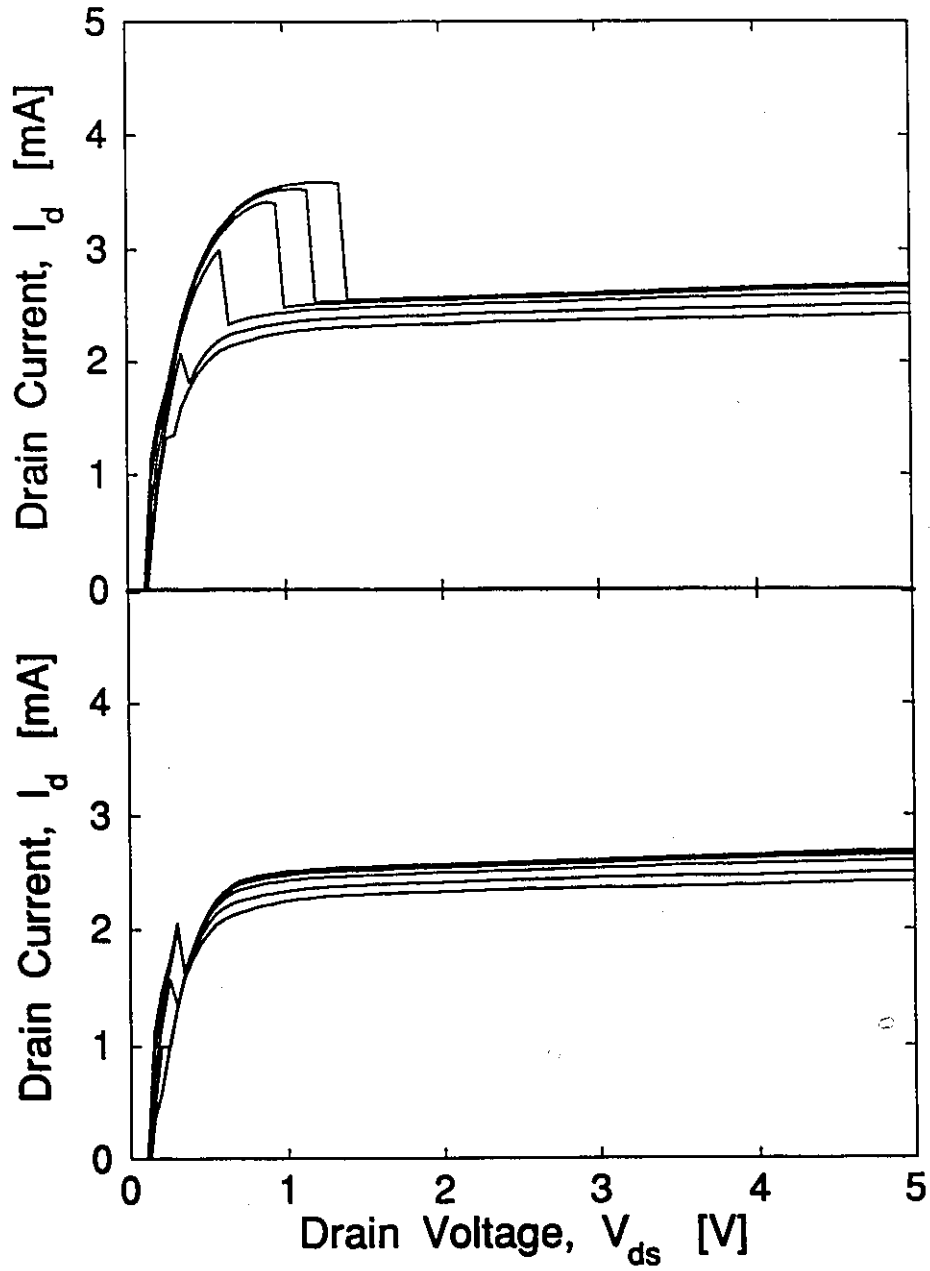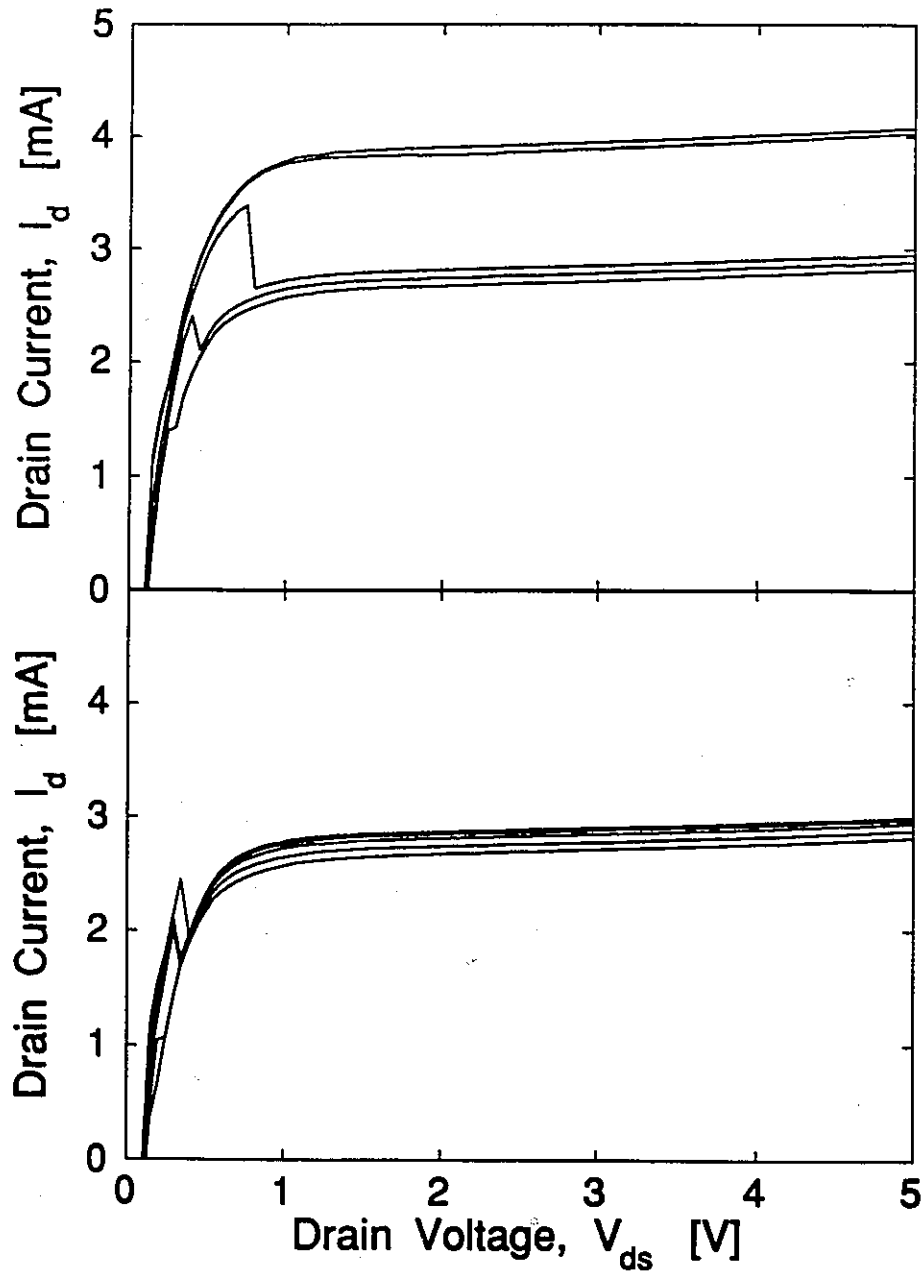
Figure 6.4   Drain characteristics for the same gate voltages as in Figs 6.2 and 6.3, with optical injection level of 50 μW. Again, the characteristics are given for the forward (top) and reverse (bottom) sweep directions.

Transverse injection of current into the channel, however, leads to non-conservation of the current along the conduction channel (*total* current, of course, must always be conserved). Equation 2.21 is thus rewritten as Eq. 2.23 in Chapter 2 to take account of the feedback current. With optical injection of carriers included, however, the expression becomes

$$\frac{dI_{ch}}{dx} = J_f - J_{esc} + J_{opt} \tag{6.1}$$

or, in integral form,

$$I_{ch}(x+dx) = \mu_p q N_{ch}(x+dx) E(x+dx)$$
$$= I_{ch}(x) + J_f dx - J_{esc} dx + J_{opt} dx \tag{6.2}$$

The first term in Eq. 6.2 is simply the current at the previous point in the channel. However, $I_{ch}(x+dx)$ is modified by the optical injection current, $J_{opt} dx$, together with the feedback current and the thermionic escape current. Note that these three current components represent carrier flows transverse to the channel.

Inclusion of the transverse current components and the resulting non-conservation of current along the channel (again, *total* current is conserved) can have a significant effect on the potential distribution along the channel [46]. The current continuity equation, together with Poisson's equation and the boundary conditions, normally leads to the existence of very high electric field in the pinch-off region of the conduction channel, with relatively low fields along the remainder of the channel. This effect is enhanced by the feedback, which tends to lower the potential barrier, increasing the curvature. However, injection of carriers into the pinched-off region by optical excitation can lead to a substantial redistribution of

potential, reducing the field there and increasing it elsewhere. Since V_{ds} is fixed, this tends to raise the barrier along the entire length of the channel except at the source and drain contacts, which are pinned at 0 V and V_{ds}, respectively. In other words, the curvature of the potential distribution is reduced. Note that the device is operated in the integral collector configuration, so the feedback current is injected very nonuniformly, as shown in Fig. 6.5. Most of it finds its way into the end of the channel closest to the source, with relatively small amounts being injected near the drain. However, the optical excitation is relatively uniform, and therefore injects carriers into regions of the channel where the feedback current does not necessarily reach, inducing the effect described.

A schematic of the channel potential as a function of position from source to drain is found in Fig. 6.6. The channel potential, $V_{ch}(x)$, is given by

$$V_{ch}(x) = \phi_1(x) - \phi_1(0) \qquad (6.2)$$

The potential variation is shown in Fig. 6.6 for both low and high levels of optical injection, as well as without illumination. The average barrier height with low illumination intensity is higher than it is without illumination for a given V_{gs} and V_{ds}, for the reasons outlined above. This tends to reduce the electron flow over the barrier from the gate to the active region. This, in turn, reduces the bias on the *p-n* junction formed by the active region and the source contact. The result is reduced feedback current from the source contact, which makes it easier to turn the feedback loop off, and harder to turn it on again. Thus, the switchup and switchdown voltages, V_{ds1} and V_{ds2}, are reduced for low levels of optical injection compared with the no-light case, as seen in Figs. 6.2 and 6.3.

As the level of optical injection is increased, the additional contribution to
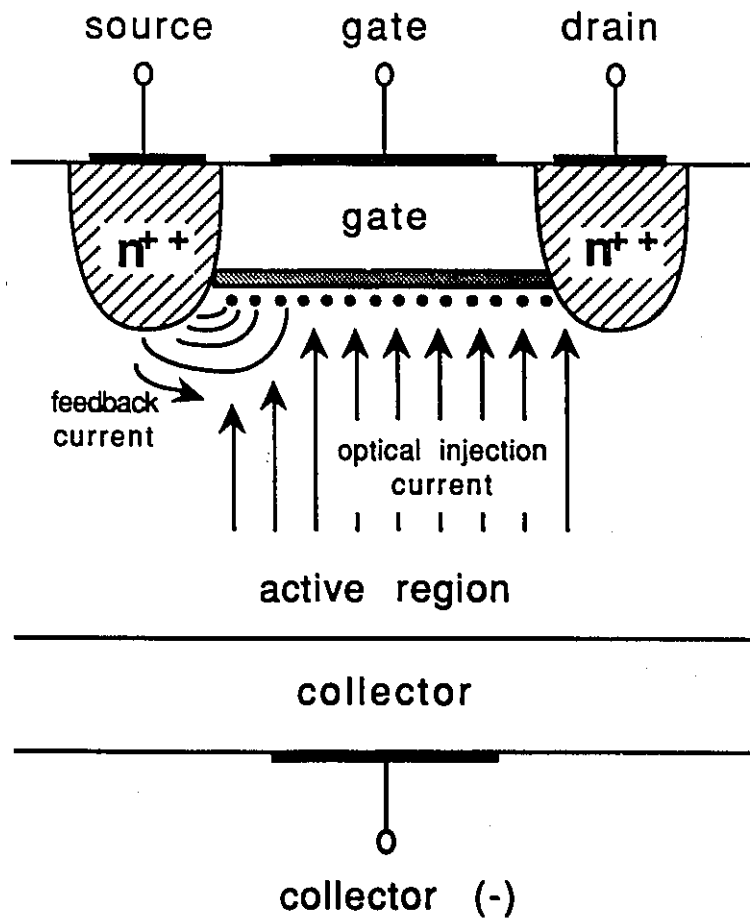
Diagram of the BISFET, showing injection of feedback
current and optical injection current. Note that the former
is injected only near the source end of the channel, while
the optical injection is distributed more uniformly.

the current flow within the feedback loop turns it on further. This tends to reduce

the potential barrier at any given point along the channel, increasing the curvature of

the potential profile, as illustrated in Fig. 6.6. More electrons are thus able to flow

over the barrier from the gate, which in turn increases the feedback current from the

source. The feedback loop thus becomes easier to turn on, and more difficult to
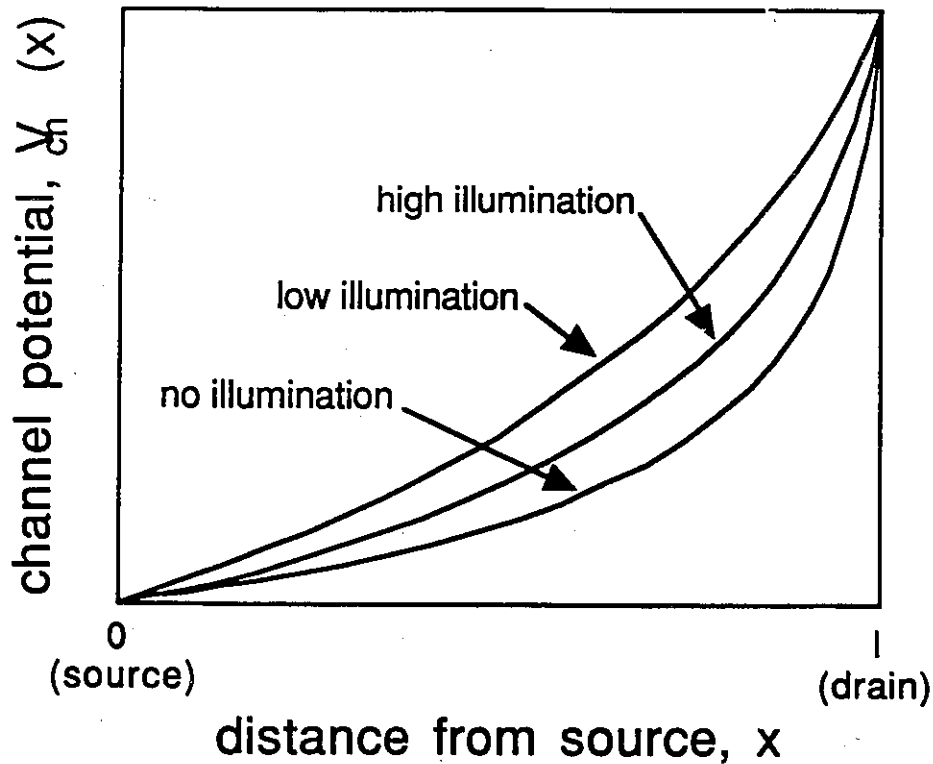
Figure 6.6   Schematic graph of channel potential as a function of distance from source for high, low, and zero illumination levels.

turn off. This effect may be considered equivalent to increasing the gate bias. It competes with the reduction in curvature resulting from non-conservation of channel current in the pinched-off region (again, *total* current is conserved). At some level of illumination, the effect of the increased feedback overtakes that of the non-conservation. The barrier height begins to drop everywhere along the channel except at the source and drain, leading to an increase in electric field in the pinched-off region and a reduction in field elsewhere. The result is increased curvature of the potential profile, as shown in Fig. 6.6. This leads to an increase in the drain

voltages, V_{ds1} and V_{ds2}, at which the loop turns on and off, as seen experimentally.

6.4 Effect on Gate Characteristics

The changes in V_{ds1} and V_{ds2} under illumination are consistent with what is observed in the gate characteristics of the BISFET. As in Chapter 3, these characteristics were taken by sweeping I_g as the independent variable, as the characteristics exhibit S-type negative differential resistance. The results are given in Fig. 6.7 for $V_{ds} = 2$ V, with L = 0, 12 μW, and 50 μW. It can be seen that

Figure 6.7   Gate characteristics of BISFET for $V_{ds} = 2$ V, with
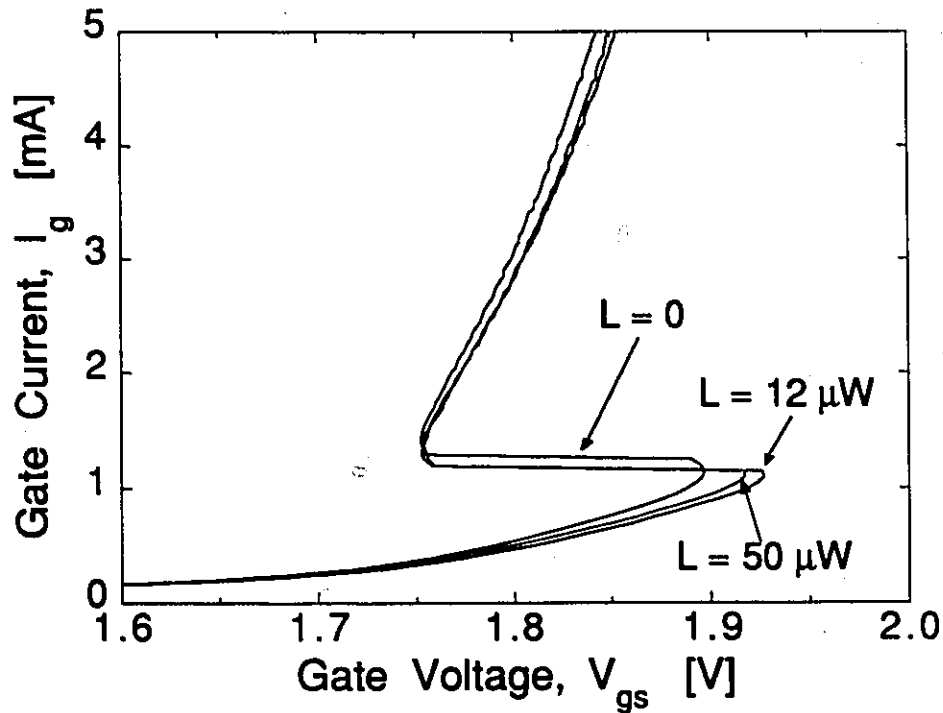optical injection levels of 0 μW, 12 μW, and 50 μW.

at very low intensity, the switching and holding voltages, V_s and V_h, of the gate characteristics both increase as the curve shifts to higher gate voltage. This is consistent with a decrease in feedback current and resultant reduction in curvature of the channel potential profile, illustrated in Fig. 6.6. At the same time, it helps in understanding the reduction in V_{ds1} and V_{ds2} directly.

When the feedback loop is in the OFF state for a given V_{gs} and V_{ds}, the difference between V_{gs} and V_s is a measure of the reduction in V_{ds} required to turn the loop on. In other words, the greater the difference V_s-V_{gs}, the more the drain potential must be lowered to allow enough holes to flow from the gate into the active region to turn the device on. Similarly, when the feedback loop is in the ON state, the difference between V_{gs} and V_h is a measure of the increase in V_{ds} required to switch the loop back into the OFF state [1],[3]. Thus, the greater the difference V_{gs}-V_h, the more the drain voltage must be increased to reduce the hole flow past the potential barrier enough to turn the feedback loop off. Therefore, an increase in V_s and V_h necessarily leads to a decrease in V_{ds1} and V_{ds2}. Thus, the increase in both V_s and V_h under low optical injection, seen in Fig. 6.7, accounts for the decrease in V_{ds1} and V_{ds2} under these conditions. Conversely, a reduction in V_s and V_h results in an increase in the transition drain voltages. Again, the changes in the gate and drain characteristics under high illumination conditions are mutually consistent. High optical injection causes V_s and V_h to decrease as the curve shifts to the left, explaining the increase in V_{ds1} and V_{ds2} at higher intensities.

6.5 Intensity Dependence of Transition Voltages

In order to determine the details of the intensity dependence of the drain

characteristics, the transition voltage V_{ds2} has been determined as a function of nominal optical power. The results are plotted in Fig. 6.8 for $V_{gs} = 1.753$ V, 1.755 V, and 1.756 V. The sharp drop in the transition voltage at low illumination levels is readily apparent. V_{ds2} reaches a minimum value of 1.1-1.4 V (depending on V_{gs}), giving a maximum negative shift, ΔV_{ds2}, in excess of 3 V. Very little change in V_{ds2} is observed as the excitation level is increased from 5 μW to 25 μW. The minimum value of V_{ds2} which is reached corresponds to where the transition enters the ohmic region of the characteristics. The transitions shift to higher drain voltage for larger optical intensities.

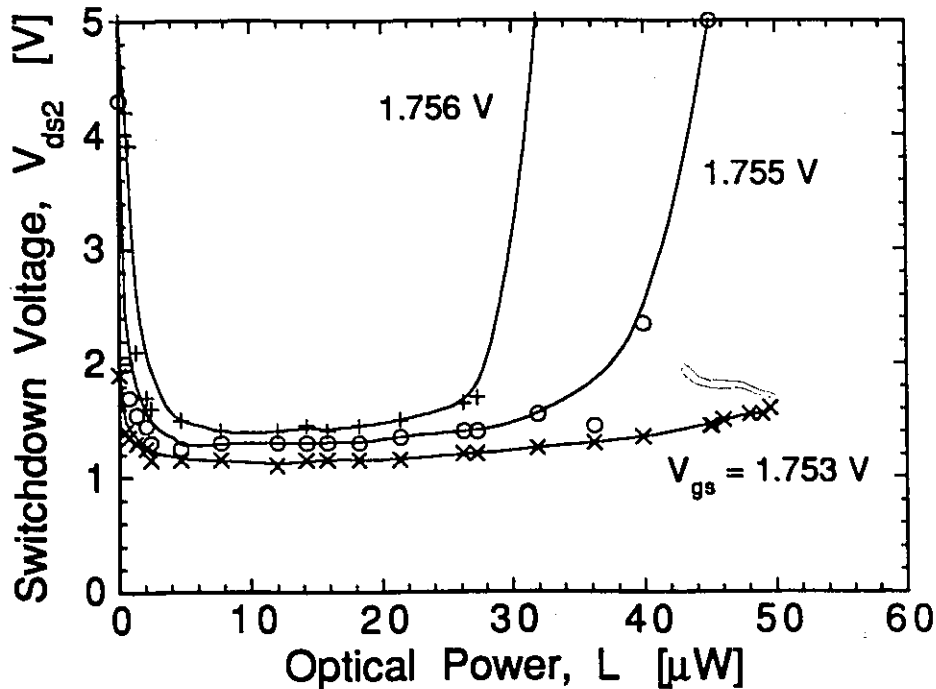The relative insensitivity of the transition voltage to illumination level in the

Figure 6.8   Variation of switchdown voltage, V_{ds2}, with injected optical power for $V_{gs} = 1.753$ V, 1.755 V, and 1.756 V.

ohmic regime suggests that the optical injection current, I_{opt}, in Equation 6.1 has a significant effect only when a high-field, low-carrier-density pinched-off region exists. Thus, in the ohmic regime, where there is no pinchoff region, the potential profile $\phi_1(x)$ is not substantially affected by optical injection of carriers. However, in the saturation regime, even a relatively modest change in optical injection (and hence in the potential distribution along the channel), can cause a relatively large change in V_{ds1} (or V_{ds2}). In fact, this tremendous sensitivity is a remarkable feature of the device. A change of as little as 3 µW results in a shift in voltage of as much as 3 V. This translates into a sensitivity of 1000 V/mW. This large sensitivity in the saturation region occurs because the pinchoff region absorbs any change in drain voltage in this region of operation. Thus, the potential barrier height along most of the channel is not significantly affected by changes in V_{ds}. Large changes in drain bias must therefore be made to counteract even relatively small changes in current injected into the channel.

For the behaviour described above to occur, the transitions must take place in the saturation region. However, catastrophically high gate voltages were necessary to increase V_{ds1} to the saturation regime. Hence, it was not feasible to obtain a plot like that in Fig. 6.8 for V_{ds1}.

Fig. 6.9 shows the full hysteresis loop in the drain characteristics at a gate voltage of 1.754 V, with light intensities of 0 µW, 12 µW, and 50 µW. The size of the hysteresis loop clearly decreases with low-level optical excitation. If we define the hysteresis voltage, V_{hys}, as

$$V_{hys} = V_{ds2} - V_{ds1} \qquad (6.3)$$

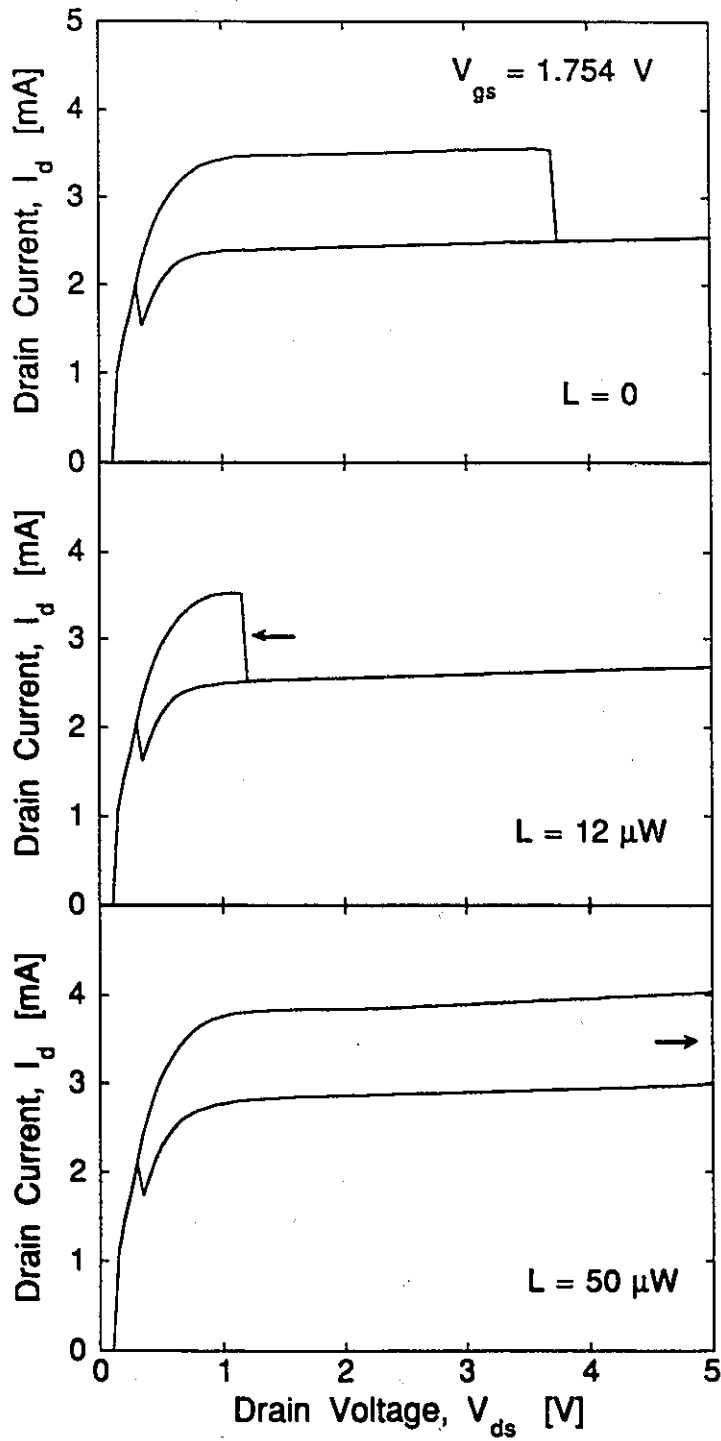Fig. 6.9 reveals that V_{hys} decreases from 3.5 V with no illumination to a minimum

Figure 6.9 Hysteresis loop in drain characteristics for optical injection power of $0\,\mu W$, $12\,\mu W$, and $50\,\mu W$.

of 1 V in the low-injection case. Under high excitation, V_{hys} increases relative to the no-light case, with V_{ds2} increasing beyond the measurement range used.

Chapter 7

OPTOELECTRONIC INTEGRATION

OF A BISFET AND LED

7.1 Device Structure and Circuit Configuration

As discussed earlier, there is currently great interest in optoelectronic integrated circuits (OEIC's) for communications and other applications. The semiconductor structure used for the BISFET is compatible with a range of other electronic and optical devices, including optical sources and detectors [40],[41], making it suitable for monolithic OEIC's. An n-channel GaAs/AlGaAs BISFET has been integrated with a light-emitting device (LED) to demonstrate the feasibility of constructing digital OEIC's using this technology.

When the BISFET's used in this thesis were processed, LED's were fabricated simultaneously on the same substrate, using the same fabrication process. The result was a wafer containing both types of devices side-by-side. This is shown schematically in Fig. 7.1(a) to illustrate the shared layer structure. The LED was made by etching a 50 μm square mesa and making ohmic contacts to the gate and collector layers. The BISFET used in the integrated circuit had a
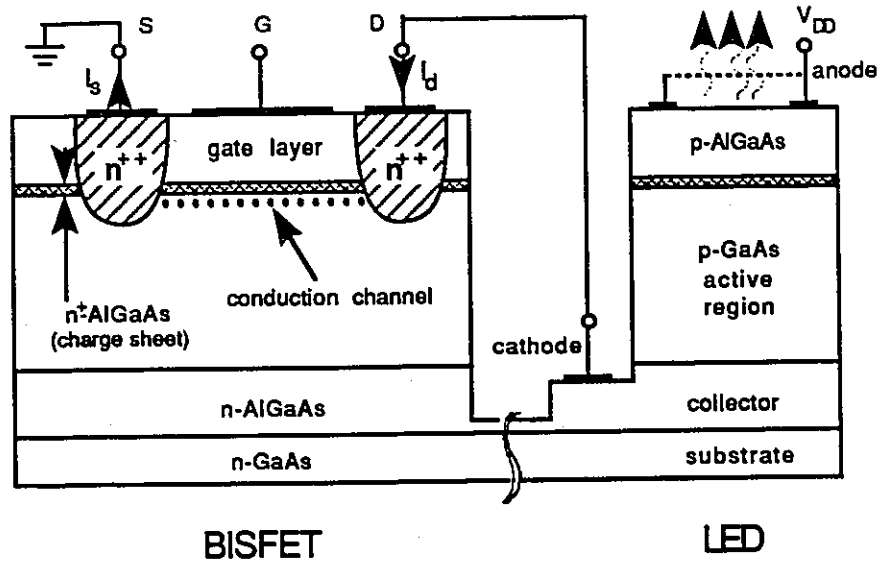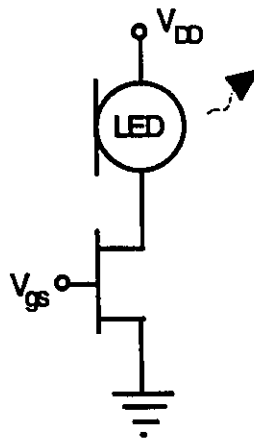
Figure 7.1 *(a)* Integrated structure of GaAs/AlGaAs BISFET and LED, showing physical structure and common semiconductor layer sequence. *(b)* Schematic of circuit configuration corresponding to *(a)*.

gate length and width of 2 μm and 150 μm, respectively.

The circuit configuration used in this work is shown in Fig. 7.1(b). The BISFET was used as a current-driver for the LED. Thus, the LED acts as the load for the BISFET. Since the devices were made on an *n*-type substrate, they were separated by cleaving the wafer so as to achieve electrical isolation between them. In a practical circuit, the devices would be fabricated on a semi-insulating substrate, and an isolation etch would be performed between them down to the level of the substrate. This would provide electrical isolation without the need to cleave the wafer. The drain of the BISFET was connected to the cathode of the LED by wirebonding. Again, in a practical circuit, deposited metal connections would be used to achieve a fully integrated circuit, with all intra-chip connections being formed during the fabrication process.

A positive bias $V_{DD} = 5$ V was applied to the anode of the LED, and the source of the BISFET was grounded. Thus, when the circuit is driven by applying a positive voltage to the gate of the BISFET, a current flows through the LED, causing it to emit light.

7.2   LED and BISFET Characteristics

Before bonding and testing the circuit, the characteristics of the individual devices were measured. The anode-to-cathode current-voltage (I-V) characteristic of the LED is shown in Fig. 7.2. The path from anode to cathode coincides with the gate-collector feedback loop in the structure. As seen in Fig. 7.1, the anode corresponds to the gate of the BISFET; the charge sheet and active region are common to both; and the cathode corresponds to the collector layer. Thus, the
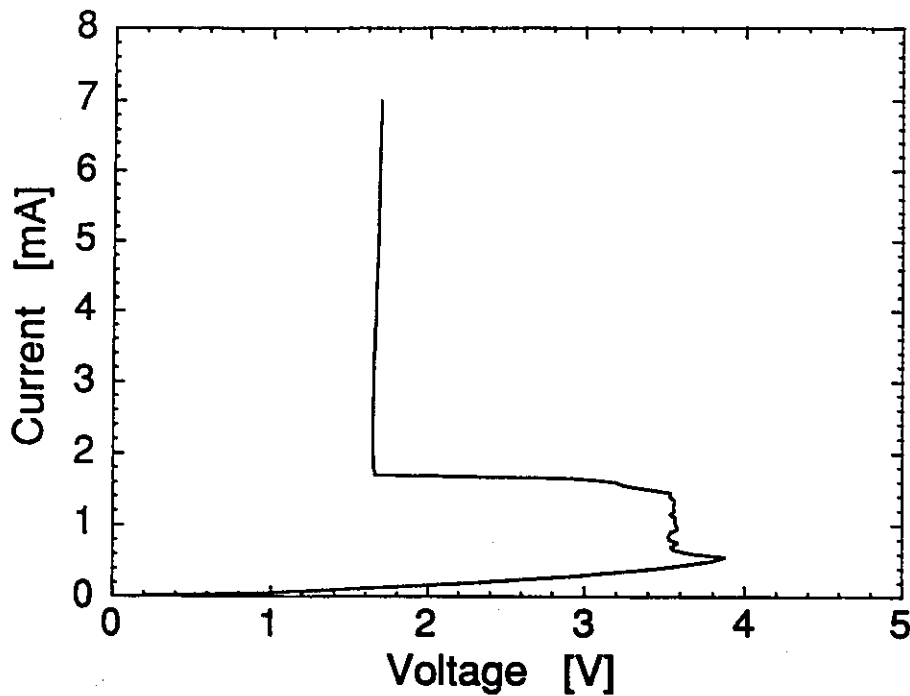
Figure 7.2   Anode-to-cathode current-voltage (I-V) characteristic of the LED, showing high- and low-impedance states connected by a region of S-type negative differential resistance (NDR).

LED displays S-type negative differential resistance (NDR), like that seen in the gate characteristics of the BISFET, over a range of current. This results from the feedback loop between the anode and cathode terminals.

The LED emits light from the active region in a manner similar to that observed in the BISFET in Chapter 5. The double heterostructure formed by the GaAs and AlGaAs regions provides confinement for the electrons and holes injected into the active region from the anode and cathode. These carriers can undergo radiative recombination, causing the device to emit light. The optical output was measured with the same experimental apparatus used to study the BISFET emission (see Fig. 5.2). The typical light-current (L-I) curve is given in

Fig. 7.3. It resembles that for a typical LED, except that it contains a region of enhanced output at low current. This is a result of oscillations associated with the NDR [47].

The forward and reverse drain characteristics of the BISFET, measured using the HP 4145B semiconductor parameter analyzer, are shown in Figs. 7.4 and 7.5. In addition to the usual source-loop transitions of Chapter 3, some structure is visible at low V_{ds}, which is associated with the source-drain symmetry discussed in Chapter 4. Hysteresis is apparent in the characteristics.

7.3   Integrated Circuit Characteristics

The BISFET was used as a current-driver for the LED, producing optical
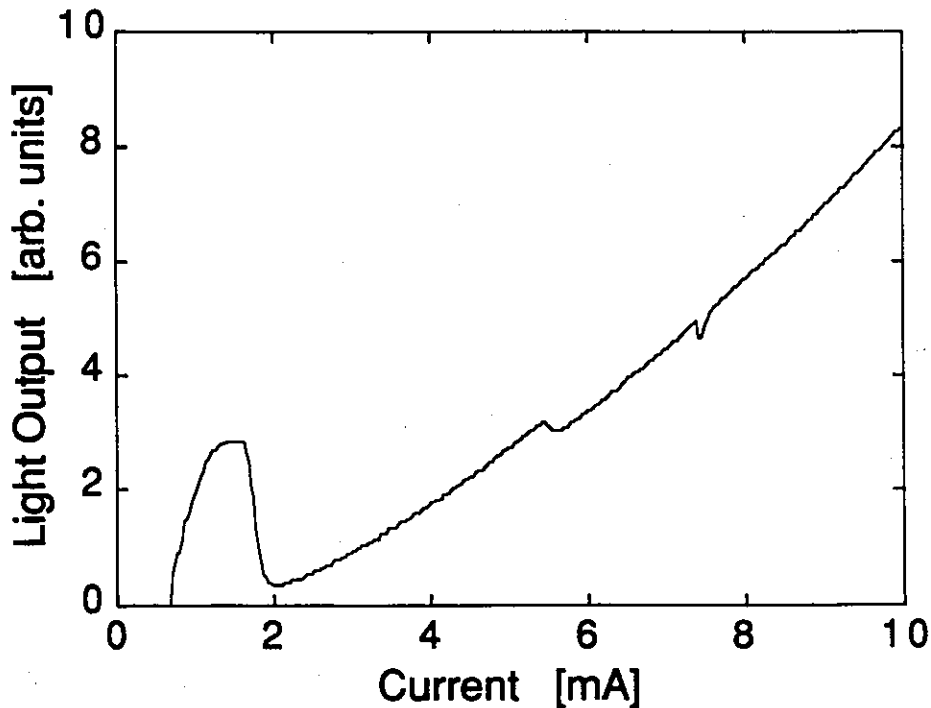
Figure 7.3   Typical light-current (*L-I*) curve for LED. The region of enhanced output at low current is a result of oscillations associated with the NDR
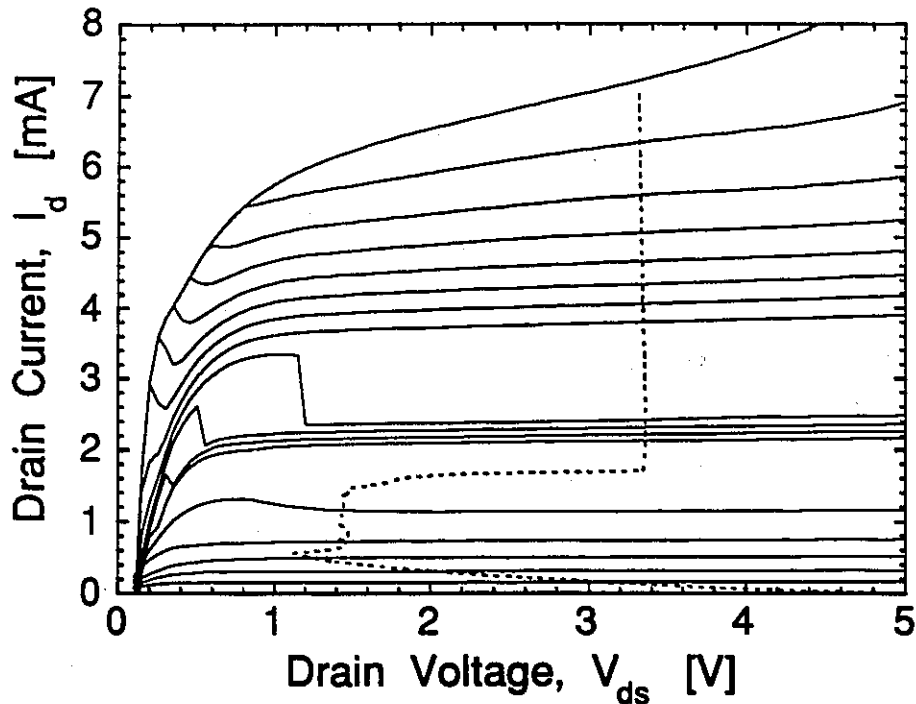
Figure 7.4   Drain characteristics of the BISFET used to implement
the integrated circuit, for increasing V_{ds}, with
Vgs = 0.5 V to 1.7 V in steps of 0.2 V, and 1.72 V to
1.90 V in steps of 20 mV. The load curve representing
the LED characteristic is superimposed (dotted line).

emission from the latter. The load curve associated with the LED (defined by its

anode-cathode characteristic) is given by the expression

$$V = V_{DD} - V_{LED}(I) \tag{7.1}$$

where $V_{LED}(I)$ is the voltage across the LED for a given current. The load curve is

superimposed on the BISFET characteristics in Figs. 7.4 and 7.5. The BISFET

curves have nearly zero slope at the intersections with the load curve. Thus, the

BISFET does indeed serve as a nearly ideal current drive for the LED.
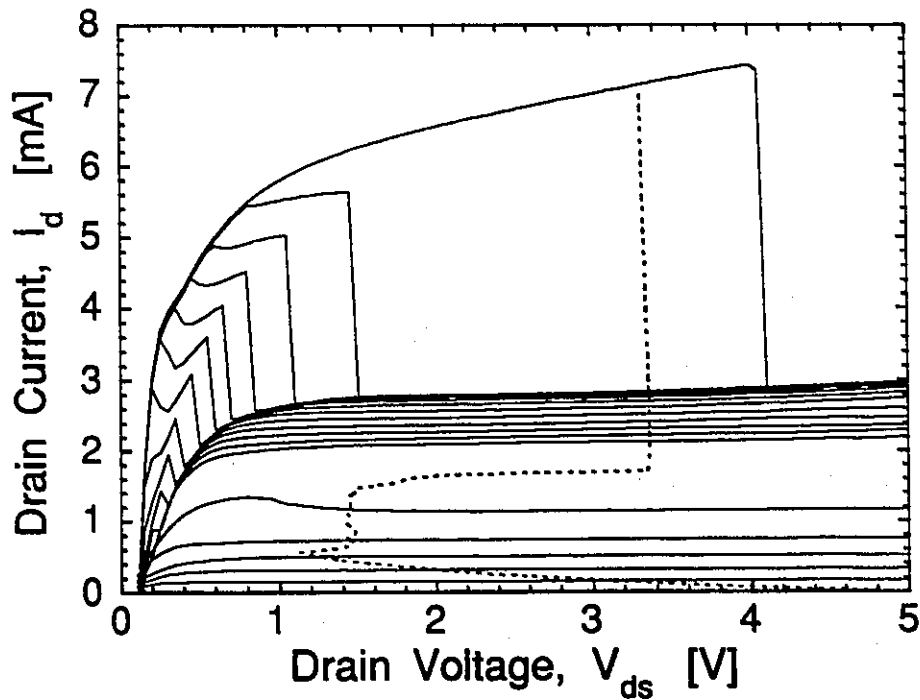
Figure 7.5   Drain characteristics of the BISFET used to implement the integrated circuit for the same gate voltages as in Fig. 7.4, this time for decreasing V_{ds}. The load curve representing the LED characteristic is once again superimposed (dotted line).

The current flowing in the circuit and the optical output from the LED were both measured as a function of V_{gs}. The former measurement yields the transfer characteristics of the circuit, while the latter gives what are referred to as the optical transfer characteristics. These characteristics were measured in both the forward and reverse sweep directions, with the results given in Figs. 7.6 and 7.7. In the forward sweep in Fig. 7.7, the device initially exhibits a gradual increase in optical output, up to $V_{gs} \approx 1.9$ V. The optical output increases abruptly at $V_{gs} \approx 1.9$ V as the BISFET turns on. This transition from the OFF to the ON state corresponds to the reverse sweep in the drain characteristics. (The

Figure 7.6   Transfer characteristics of the integrated circuit, showing current in the circuit vs. gate voltage. The characteristics are shown in both the forward and reverse sweep directions.

BISFET may be switched on by increasing V_{gs} or decreasing V_{ds}.) The circuit thus enters a state of high absolute and differential optical output relative to the OFF state. In the region from $V_{gs} = 1.2$ V to 1.4 V, there is an enhancement of the output associated with the LED oscillations mentioned in Section 7.2.

In the reverse sweep, as V_{gs} is decreased from the ON state, the optical output decreases rapidly but continuously until $V_{gs} \approx 1.75$ V, at which point it drops abruptly back to the OFF state and rejoins the forward-swept characteristic. Note that the turn-on and turn-off voltages differ by about 150 mV, leading to substantial hysteresis. This results from the hysteresis in the electrical

characteristics of the BISFET, illustrated by the dramatic difference in the forward- and reverse-swept curves of Figs. 7.4 and 7.5. The NDR in the LED characteristics plays no role in the switching, since the BISFET serves as an essentially ideal current drive. In fact, the NDR is purely incidental, resulting from the use of a compatible layer structure for the two devices. It is not essential to the circuit.

It is apparent that the BISFET can be readily integrated with an LED to implement monolithic OEIC's. The optical output from the structure used here is relatively inefficient because of the large thickness of the GaAs region - the
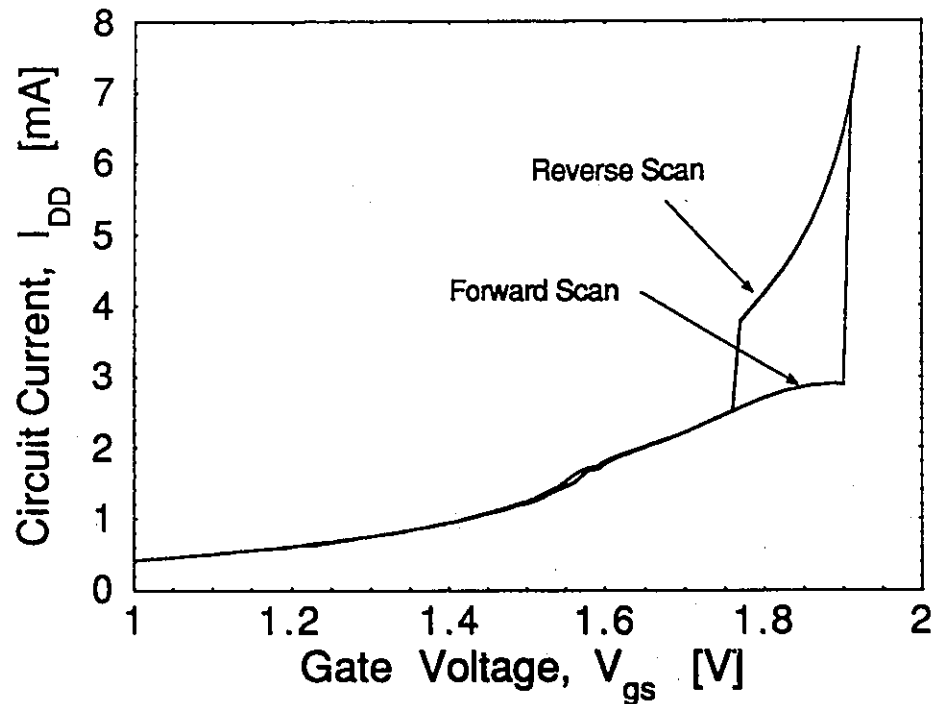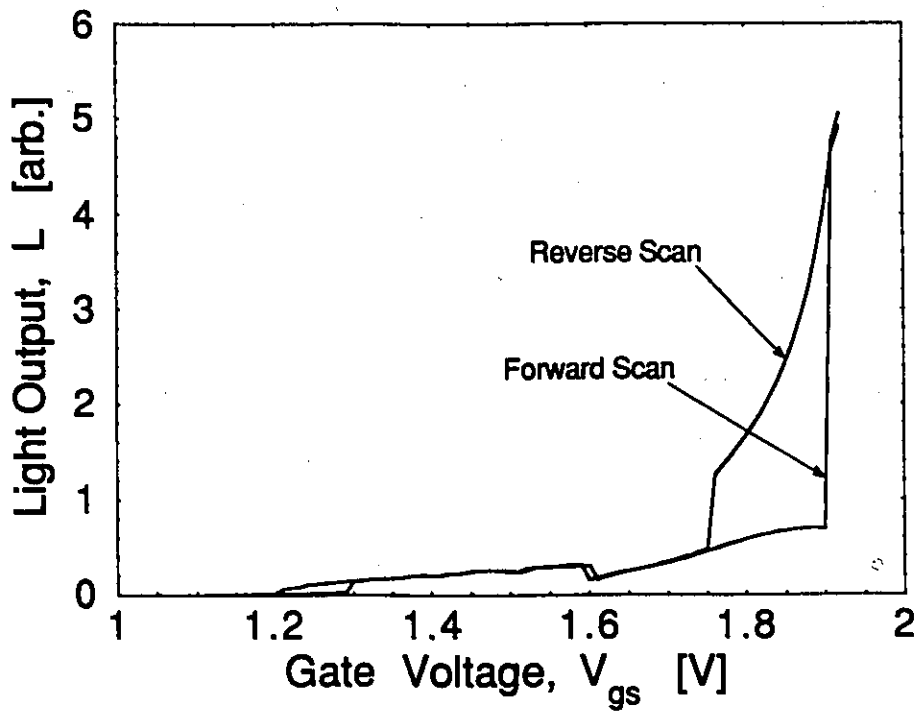

Figure 7.7   Optical transfer characteristics of the integrated circuit, showing LED light output vs. gate voltage. The characteristics are shown for both forward and reverse sweeps. The enhanced output at low gate voltage is due to the LED oscillations mentioned in Section 7.2.

electrons and holes tend to move to opposite ends of this region, thus separating them rather than increasing their proximity. However, optimization of the heterostructure to provide better confinement of carriers in a narrower portion of the active region should improve the efficiency considerably. This could be achieved as described in Section 5.3. Such a structure would also allow implementation and integration of a semiconductor laser and a BISFET, further increasing the usefulness of the device.

Chapter 8

CONCLUSION

In this work, the BISFET has been developed as a novel optoelectronic switching device. A model for the operation of the device has been set forth, and the BISFET has been implemented in the GaAs/AlGaAs material system.

The BISFET has been shown to have two distinct output current states, and to undergo abrupt transitions between these states with varying drain bias. These transitions exhibit substantial hysteresis. It has been shown that multiple coupled feedback loops may be operational in the device simultaneously. Specifically, it has been shown that feedback loops may exist between the gate and the source, drain, and collector terminals. Current transitions associated with each of these feedback loops have been observed in the drain characteristics. It has proven possible to observe transitions associated with all three loops in a single set of drain characteristics under appropriate bias conditions. This leads to multiple bistability, raising interesting prospects for multi-level switching and logic.

In addition, the GaAs/AlGaAs BISFET has been found to produce an

optical output, which undergoes transitions and exhibits hysteresis corresponding with those seen in the electrical characteristics.

It has been shown that both the electrical and optical output states of the BISFET can be controlled electrically by the gate voltage applied to it. Alternatively, the state may be controlled by exposing the device to an optical input signal. Thus, in summary, the device produces bistable electrical and optical outputs, both of which may be controlled by either an electrical or an optical input signal. This would allow the BISFET output to be cascaded with subsequent devices, either electrically or optically. These properties make the BISFET a remarkably versatile switching device for optoelectronic applications.

Although not reported here, the BISFET has also been implemented in the Si/SiGe material system, confirming the principles of operation of the device.

Aside from its practical applications potential, the BISFET opens an interesting realm of device physics by fusing the properties of field-effect and bipolar devices into a hybrid form of operation. Carrier transport within the conduction channel has a field-effect, or unipolar, component controlled directly by the gate. At the same time, however, bipolar carrier transport in the feedback loop transverse to the channel plays an important role in determining the drain current in the device. The unipolar and bipolar current components do not simply coexist within the BISFET. Rather, they are intimately interlinked, so that the state of the device cannot be determined with reference to only one of the components. The task of arriving at a mathematical model which adequately and accurately reflects this coupling between the two transverse currents is not a trivial one.

The insight gained into hybrid bipolar and field-effect transport from the BISFET should lead to further progress in other areas of device physics, such as

thyristor design and the development of other switching components for both logic and power applications.

The usefulness of the BISFET is augmented by the demonstration of its suitability for monolithic optoelectronic integration. As part of this work, a BISFET has been fabricated in the GaAs/AlGaAs system on the same substrate as an LED, with a compatible fabrication process. The devices have been successfully operated as an integrated emitter and current-driver circuit. In principle, this should make possible very compact circuits integrating logic functions with optical signal detection and generation capabilities.

Further study is required to determine the criteria for optimizing the performance of the BISFET. For instance, it has been determined in this work that the switching ratio between the currents in the ON and OFF states could be improved by designing the analog threshold voltage of the device to be roughly equal to the threshold for bistability. This could be achieved by reducing the amount of dopant in the charge sheet. The effect of the size of the hetero-offsets on the device behaviour also remains to be determined.

Another key issue in the design of the BISFET is whether the gain (the ratio of the current in the conduction channel to that in the feedback loop) can be increased. This would be desirable in applications where the drain current is the output variable of interest. In such cases, the current in the feedback loop would function primarily as a control current. In other applications, it may be desirable to increase the feedback current relative to the drain current. For instance, when the optical output from the device is the signal of interest, the drain may be regarded as the control terminal. In this case, the greater the current in the feedback loop, the greater the optical emission from the device.

It is clear that the BISFET represents an interesting new device

development, in terms of both potential applications and new insights into the physics of carrier transport within semiconductor devices. A great deal of work remains to be done, however, before the design criteria and the detailed physics at play within the device are fully understood. It is hoped that this work will stimulate further research in this interesting area.

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