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Si-Based Optoelectronics: Monolithic Integration for WDM

by

Matthew R.T. Pearson, B.Sc.

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in Partial Fulfillment of the Requirements
for the Degree
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Si-Based Optoelectronics: Monolithic Integration for WDM

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Abstract

This thesis details the development of enabling technologies required for inexpensive, monolithic integration of Si-based wavelength division multiplexing (WDM) components and photodetectors. The work involves the design and fabrication of arrayed waveguide grating demultiplexers in silicon-on-insulator (SOI), the development of advanced SiGe photodetectors capable of photodetection at 1.55 μm wavelengths, and the development of a low cost fabrication technique that enables the high volume production of Si-based photonic components.

Arrayed waveguide grating (AWG) demultiplexers were designed and fabricated in SOI. The fabrication of AWGs in SOI has been reported in the literature, however there are a number of design issues specific to the SOI material system that can have a large effect on device performance and design, and have not been theoretically examined in earlier work. The SOI AWGs presented in this thesis are the smallest devices of this type reported, and they exhibit performance acceptable for commercial applications.

The SiGe photodetectors reported in the literature exhibit extremely low responsivities at wavelengths near 1.55 μm. We present the first use of three dimensional growth modes to enhance the photoresponse of SiGe at 1.55 μm wavelengths. Metal-semiconductor-metal (MSM) photodetectors were fabricated using this undulating quantum well structure, and demonstrate the highest responsivities yet reported for

a SiGe-based photodetector at 1.55 μm. These detectors were monolithically integrated with low-loss SOI waveguides, enabling integration with nearly any Si-based passive WDM component.

The pursuit of inexpensive Si-based photonic components also requires the development of new manufacturing techniques that are more suitable for high volume production. This thesis presents the development of a low cost fabrication technique based on the local oxidation of silicon (LOCOS), a standard processing technique used for Si integrated circuits. This process is developed for both SiGe and SOI waveguides, but is shown to be commercially suitable only for SOI waveguide devices. The technique allows nearly any Si microelectronics fabrication facility to begin manufacturing optical components with minimal change in processing equipment or techniques. These enabling technologies provide the critical elements for inexpensive, monolithic integration in a Si-based system.

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Contents

1 Introduction 1

1.1 Wavelength Division Multiplexing 3

1.2 Silicon Photonics 4

1.3 Optoelectronic Integration 5

1.4 Structure of this Thesis 7

2 Optical Waveguides 8

2.1 Introduction 8

2.2 Modeling Techniques 12

2.2.1 The Effective Index Method 12

2.2.2 The Beam Propagation Method 14

2.3 SiGe Optical Waveguides and Detectors 15

2.4 SOI Optical Waveguides 23

3 LOCOS Optical Waveguides 27

3.1 The Local Oxidation of Silicon 27

3.2 SiGe LOCOS Waveguides 29

3.2.1 Temperature Effects 30

3.2.2 Strain-Compensating Mask Layer 32

3.3 SOI LOCOS Waveguides 33

4 Passive WDM Components 35

4.1 1.3/1.55 μm Duplexer 35

4.2 Arrayed Waveguide Grating Demultiplexer 39

4.2.1 Principles of Operation 39

4.2.2 Design Issues Specific to SOI 47

5 SiGe Coherent Wave Photodetectors 55

5.1 Coherent Wave Quantum Wells 56

5.2 MSM Waveguide Photodetectors 60

6 Experimental Results 63

6.1 LOCOS Optical Waveguides 64

6.1.1 SiGe LOCOS Waveguides 64

6.1.2 SOI LOCOS Waveguides 72

6.2 Passive WDM Components 74

6.2.1 1.3/1.55 μm Duplexers 74

6.2.2 Arrayed Waveguide Grating Demultiplexers 76

6.3 SiGe Coherent Wave Photodetectors 90

7 Conclusion 100

7.1 Recommendations for Future Research 101

A List of Publications 104

B Glossary of Abbreviations 106

C Photolithography Masks 107

References 114

List of Figures

1.1 Schematic of a 4-channel WDM optical network 3

1.2 FTTH transceiver based on Si optical bench technology and hybrid integration. Commercially available from Bookham Technology Inc. From [1]. 6

2.1 The basic geometry of a planar optical waveguide. Optical confinement requires $n_f > n_c$ and $n_f > n_s$ 10

2.2 Top view and cross section of a rib waveguide used with the effective index method. 13

2.3 SiGe optical waveguides 16

2.4 Equilibrium and metastable critical thicknesses for SiGe epilayers. The equilibrium critical thickness of Matthews and co-workers is denoted by the solid line. The theoretical curves for metastable critical thickness are based on theory derived in [2], and are calculated for relaxation temperatures of 750, 550, and 500°C, as noted on the figure. Adapted from [2]. 20

2.5 X-ray rocking curve for an as-grown SiGe heterostructure with germanium concentration of 2.7%. 21

2.6 X-ray rocking curve for a SiGe heterostructure with Ge concentration of 2.7% after a 3.9 h anneal at 900°C. 23

2.7 The SIMOX process for fabricating SOI wafers. Epitaxial growth of Si typically follows this substrate preparation. 24
2.8 Schematic of a rib waveguide in SOI. 26
2.9 Plots of theoretical curves for the single-mode limit determined by Soref [3], and by using the EIM [4]. The circles and crosses correspond to experimental observations of multimode and single-mode waveguides, respectively. From [4]. 26

3.1 The LOCOS process. The masking layers, and the structure after several hours in an oxidizing furnace. 28
3.2 Illustration of the effects of processing at different temperatures. . . . 31

4.1 1.3/1.55 μm duplexer layout and BPM simulations. Note that light is input the top left waveguide in both cases. 38
4.2 Layout of an arrayed waveguide grating demultiplexer. Adapted from [5] 40
4.3 Geometry of the Rowland mounting. Adapted from [5] 42
4.4 90-degree device geometry used for some of the devices in this work. . 46
4.5 TE/TM birefringence calculated for waveguides fabricated in 1.5 μm thick SOI using an etch depth of 0.75 μm. The solid curves are provided as a guide to the eye only. The waveguide structures used for the calculations are shown on the right. 49
4.6 Bending losses in SOI. 51
4.7 Power coupled to slab waveguide modes from a single-mode input waveguide in SOI. 53

5.1 Elastic distortion of vertical lattice planes in a coherent wave QW. Adapted from [6] 57

5.2 Illustration of the effects of quantum confinement on the absorption edge of flat $Si_{1-x}Ge_x$ QWs, and the benefit derived from coherent wave growth. Based on results published in [7] and [8]. 58

5.3 Conditions necessary for coherent wave growth of $Si_{1-x}Ge_x$. The solid line represents the Matthews-Blakeslee critical thickness. The dashed line represents the theory governing surface wave formation presented in [9]. Coherent wave growth is expected in the hatched region. Adapted from [10]. 59

5.4 SOI waveguide photodetector structure. 61

5.5 Cross-sectional view of the SOI waveguide photodetector structure. The device layers are not drawn to scale. 61

6.1 X-ray rocking curves of a $Si_{.97}Ge_{.03}$ sample after an oxide growth of 0.6 μm. (a) Processed at 900°C for 3.9 hours, (b) processed at 1050°C for 1.0 hours. The as-grown curve is shown in (c). 67

6.2 X-ray rocking curves of a $Si_{.97}Ge_{.03}$ sample. (a) As grown, (b) with a strain-compensating mask layer deposited on the surface, and (c) after removal of the masking layer. The strain in the SiGe layer is reduced by the masking layers. 68

6.3 X-ray rocking curves of a $Si_{.97}Ge_{.03}$ sample oxidized at 1050°C for one hour. (a) Without any masking layer deposited. (b) With a SiO_2/Si_3N_4 masking layer of 30 nm SiO_2 and 180 nm Si_3N_4. The as-grown curve is shown in (c). 70

6.4 LOCOS optical waveguides in SiGe. (a) The structure after several hours in an oxidizing furnace, showing the masking layer and the field oxide. (b) The structure after removal of the SiO_2/Si_3N_4 mask and the thermal oxide. 71
6.5 SEM image of a LOCOS waveguide fabricated in SOI. The sample was oxidized at 1100°C for 12 h with a SiO_2/Si_3N_4 mask. 73
6.6 Infrared camera traces of 1.3/1.55 μm demultiplexer output using TM polarized light. This device was fabricated using LOCOS processing. The channel wavelengths (in μm) are indicated in bold. 75
6.7 SEM images of an AWG demultiplexer fabricated in SOI. (a) Device layout. (b) Close-up of the splitter/array interface. 78
6.8 Measured output spectrum for an SOI AWG. This is a first generation device in 2.1 μm SOI with rib width of 1.7 μm, chemically etched to a depth of 1.1 μm. The light is TM polarized. 79
6.9 Measured polarization dispersion in first generation SOI AWG demultiplexers fabricated in 1.5 μm SOI. The experimental uncertainty in these measurements is $\pm$0.1 nm. The solid curves are provided as a guide to the eye only. 80
6.10 Measured polarization dispersion in the center channel of a first generation SOI AWG demultiplexer fabricated in 1.5 μm SOI. 81
6.11 Measured output spectrum for an SOI AWG fabricated using the LOCOS process. This is a first generation device in 2.1 μm SOI with rib width of 1.7 μm, and rib height of 1.0 μm. The light is TM polarized. 83
6.12 Sidewall of a waveguide rib, (a) as removed from the RIE. (b) After thermal oxide growth and removal of the oxide. 84

6.13 Mask layout for second generation AWGs. 85
6.14 Measured output spectrum for a normal passband AWG. This is a second generation device in 4.2 μm SOI with rib width of 5 μm and etch depth of 2 μm. 86
6.15 Measured output spectrum for a wide passband AWG. This is a second generation device in 4.2 μm SOI with rib width of 4 μm and etch depth of 2 μm. 87
6.16 Measured polarization dispersion in the center channel of a second generation SOI AWG demultiplexer fabricated in 4.2 μm SOI. 88
6.17 Measured temperature sensitivity of an AWG fabricated in 4.2 μm SOI. 89
6.18 TEM image of a $Si_{.50}Ge_{.50}$ coherent wave superlattice grown for this work. 91
6.19 Photoluminescence spectrum for a UHV-CVD grown $Si_{.50}Ge_{.50}$ superlattice. 92
6.20 Photocurrent spectrum for a UHV-CVD grown $Si_{.50}Ge_{.50}$ superlattice. 94
6.21 Photocurrent spectrum for a UHV-CVD grown $Si_{.50}Ge_{.50}$ superlattice. The solid line is a fit of the equation $\alpha(E) \approx (E - E_g)^3$ to the data. . 95
6.22 Dark current vs. bias for the photodetectors. 96
6.23 The dependence of photocurrent on bias for different illumination levels at 1310 nm wavelength. The light intensities indicated on the figure are intensities out of the fiber. Insert: The I-V at 16 μW plotted in semi-log scale. 97
6.24 The dependence of photocurrent on light intensity for (a) 1310 nm wavelength, and (b) 1520 nm wavelength. 98

C.1 Mask layout for second generation AWGs fabricated in SOI. 108

C.2 Mask layout for second generation SOI AWGs monolithically integrated with SiGe photodetectors. This mask will be used in future research but is based on all the technologies and device structures developed in this work. 109
C.3 Close up view of AWGs fabricated in SOI, monolithically integrated with SiGe photodetectors. Optical input at left, electrical output contacts at bottom. 110
C.4 Close up view of MSM detector structure at the output of the AWG. 111
C.5 First generation AWG demultiplexer. 112
C.6 Second generation AWG demultiplexer. 113

List of Tables

6.1 Wafer structures for samples used in this work, as determined using x-ray rocking curves and SEM. 64

Chapter 1

Introduction

The telecommunications industry relies on two distinctly different semiconductor technologies. Optical components that are used in fiber optic systems are fabricated using III-V semiconductors. However, switching and the processing of electrical signals are carried out using advanced VLSI circuitry, and this is the exclusive domain of silicon. Optoelectronic integrated circuits that integrate optical components and electrical circuitry on a single chip are therefore a very ambitious goal. The potential cost reductions associated with integration make this a very attractive concept, but neither silicon nor III-V substrates can be the optimal choice for both electronics and optics. One approach to solving this problem is the use of silicon-based systems for optoelectronics, such as SiGe and silicon-on-insulator (SOI).

Monolithic integration requires passive optical components and active photodetectors to be integrated onto a common substrate. The passive optical components of interest to this work are primarily dense wavelength division demultiplexers. In recent years the demand for dense wavelength division multiplexing (DWDM) components has escalated to unprecedented heights, and DWDM is unquestionably the largest area of photonic research today. In its simplest form, DWDM refers to the technique of transmitting several discrete communication channels over a single opti-

cal fiber, where each channel is represented by a slightly different wavelength. At the receiver end these multiple channels must be separated (using a demultiplexer) and detected individually. This thesis work includes, in part, the design and fabrication of DWDM demultiplexers based on SOI waveguides.

The optical outputs from a DWDM demultiplexer are typically coupled to separate receiver modules where they are converted to electrical signals. By monolithically integrating detectors onto the same chip as the demultiplexer, the component cost is significantly reduced, optical losses are minimized, and system complexity is also minimized. Infrared photodetectors can be made using SiGe with high Ge contents, and this material can be monolithically integrated with Si or SOI. However, the absorption in these detectors is generally limited to wavelengths under 1.4 μm, making them unsuitable for telecommunications applications, which typically operate near 1.55 μm. In an effort to overcome this problem our research group was the first to develop photodetectors based on undulating quantum well growth of SiGe. This technique pushes the absorption edge of the material out to wavelengths beyond what is attainable with standard quantum well growth, making it more suitable for photodetection at 1.55 μm. This work will also be presented in the thesis.

Monolithic integration alone, even in inexpensive Si-based material, may not reduce component cost to desired levels. The recent demand for inexpensive DWDM components has also necessitated the development of new fabrication and assembly techniques that allow for mass production. In order to take advantage of well-established silicon processing techniques, our group was the first to develop a method for fabricating optical waveguides in siiicon using standard VLSI processing. This processing is used in the fabrication of nearly all Si integrated circuits. This means that nearly any silicon electronics fabrication facility could begin producing photonic

components with virtually no change in equipment or process. This fabrication technique will also be presented in the thesis.

These three enabling technologies provide the critical elements for inexpensive, monolithic integration in a Si-based system.

1.1 Wavelength Division Multiplexing

Wavelength division multiplexing allows the channel count of an optical network to be vastly increased without the need to lay more fiber optic cable. By encoding different channels on different wavelengths, all channels can be transmitted down a single fiber and then separated again at the receiver end, as illustrated in Fig. 1.1. WDM has revolutionized optical network architecture and supplied the bandwidth necessary to support the growing demand for broadband internet access.

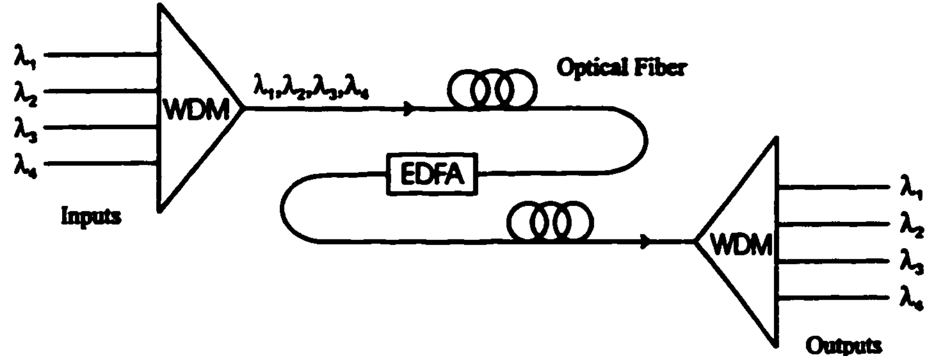


Figure 1.1: Schematic of a 4-channel WDM optical network

As telecommunication networks evolve to incorporate fiber optics in nearly all major links, there is a significant bottleneck at what is generally termed "the last mile." Fiber-to-the-curb is becoming a practical reality, but the final "mile" between a local switching station and each house is still limited to twisted copper wire, due mainly to the high cost of modern photonic components. One solution to

this bottleneck is the incorporation of fiber-to-the-home (FTTH) transceivers, which transport all the phone, television, and internet signals over a single optical fiber. These transceivers are capable of transmitting signals at $\lambda = 1.55$ μm while simultaneously receiving signals at $\lambda = 1.3$ μm.

The introduction of the erbium-doped fiber amplifier (EDFA) resulted in a concentration of research activity towards the 1.55 μm communications band, where erbium acts as an effective amplifier for optical signals. Although 1.3 μm systems are still in service, new systems operate exclusively in the 1.55 μm window. This may change in the future, with the recent introduction of new Raman amplifiers and "all-wave fiber", which allow the efficient transmission of nearly all wavelengths between 1.3 μm and 1.6 μm, however current systems are limited to the 1.55 μm bands.

Modern WDM networks have therefore evolved from coarse WDM systems based on 1.3/1.55 μm duplexing, to dense WDM (DWDM). DWDM systems rely on very small channel spacings to transmit as many discrete signals as possible within the erbium-doped fiber amplification window. State-of-the-art commercial DWDM systems have channel spacings as low as 50 GHz (0.4 nm). Demultiplexing these tightly spaced channels requires advanced photonic components such as arrayed waveguide grating demultiplexers (AWGs).

1.2 Silicon Photonics

Advanced photonic components are typically fabricated in III-V semiconductors, which allow for band gap engineering and precise control over refractive indices. However, III-V semiconductors are very costly to manufacture and require processing that is often difficult to adapt to mass production.

The dominance of inexpensive silicon devices for electronic circuits has led to

the pursuit of silicon-based photonic components. Early work relied on the doping of Si layers to create optical waveguides [11]. Modern Si photonic components often use doped silica layers on Si substrates to perform the same function [12], and offer a close match to optical fiber modes in terms of refractive index and mode size. However, these devices are typically quite large because of the low refractive index contrast, minimizing wafer real-estate benefits. The subject of this thesis work is the use of SiGe and silicon-on-insulator structures to perform these optical functions.

SiGe offers a variable band gap, necessary for creating photodetectors in the material, however it will be shown in this thesis that it is not well suited for optical waveguides. SOI has a lot of potential for this application, but does not offer a variable band gap. This thesis concentrates on merging these two technologies in order to take advantage of the benefits of each. Optical waveguides will be fabricated in SOI, and epitaxial layers of SiGe will be grown on this material in order to integrate a new type of SiGe photodetector.

1.3 Optoelectronic Integration

One of the benefits of III-V semiconductors is the possibility for integrating optical waveguides, lasers and photodetectors, and electronics all onto the same wafer. Although lasers cannot be fabricated in Si because of the indirect band gap, it is desirable to be able to integrate the other components onto a common substrate.

Some recent successes for this technology in Si have included the use of SiGe for both waveguide and photodetector structures [13]. Low Ge content SiGe is used for waveguides, and MQWs of high Ge content are used for detector layers. This technology suffers from the fact that the strained-layer SiGe waveguides are quite birefringent, and the detector response spectra is not well suited for operation at

wavelengths in the 1.55 μm band.

Si -based optoelectronic components are commercially available from a limited number of suppliers, however they rely on hybrid integration, as shown in Fig. 1.2. In this case, III-V laser and detector chips are positioned into small pits etched in the chip, while the Si acts as an "optical bench". This hybrid layout is costly to manufacture because of the alignment involved in assembly. Monolithic integration eliminates this problem.

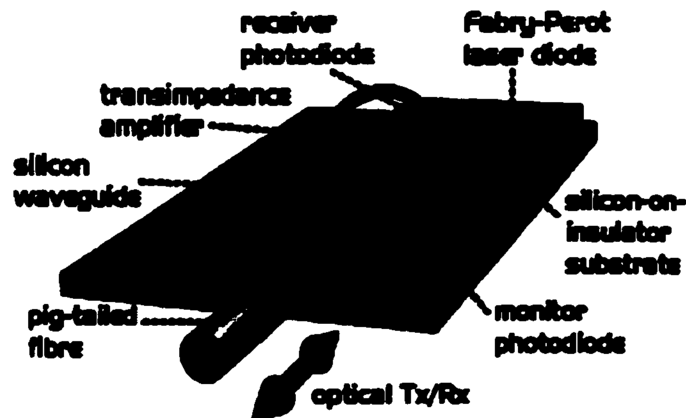


Figure 1.2: FTTH transceiver based on Si optical bench technology and hybrid integration. Commercially available from Bookham Technology Inc. From [1].

This research concentrates on developing the technologies required to monolithically integrate a DWDM demultiplexer in SOI with SiGe photodetectors. This type of integration would allow for an input from one optical fiber, carrying a number of different wavelengths, to be demultiplexed and converted to a series of electrical outputs. Because the technology is completely compatible with Si electronics processing, there is further potential for integrating electrical amplifier circuitry onto the same chip. This, to our knowledge, represents the highest level of monolithic integration ever reported in a Si -based system.

1.4 Structure of this Thesis

Chapter 1 of this thesis has presented a brief background on various topics that are of interest to this work, including WDM networks, Si-based photonics, and optoelectronic integration.

Chapter 2 introduces optical waveguides and various modeling techniques used in this research. This is followed by a more detailed discussion of SiGe and SOI waveguides, both of which have properties that are unique to each system.

Chapter 3 presents the local oxidation of silicon (LOCOS). This process is developed from a standard fabrication technique for Si integrated circuits, to a novel method of fabricating optical waveguides in SiGe and SOI.

Chapter 4 discusses the passive WDM components of interest to this work, which include both coarse WDM duplexers and DWDM demultiplexers based on arrayed waveguide gratings (AWGs). The theory governing AWG operation is discussed in detail and modeling results which are unique to SOI AWGs are presented.

Chapter 5 presents a brief theoretical treatment of MSM photodetectors, and a detailed discussion of coherent wave quantum well growth of SiGe. This growth technique is utilized for the fabrication of SiGe photodetectors suitable for operation at $\lambda = 1.55\ \mu m$.

Chapter 6 presents the experimental results derived from this research. These include LOCOS devices, AWGs, advanced SiGe photodetectors, and the monolithic integration of these technologies.

The final chapter summarizes the results and conclusions from this research, and suggestions for future work are also presented. The appendices include a list of publications resulting from this work, a glossary of abbreviations, and figures that show the photolithography masks produced for this work.

Chapter 2

Optical Waveguides

This chapter begins with a brief review of the waveguide theory important to this work. Modeling techniques used for integrated optic applications are reviewed, including the effective index method and the beam propagation method. The final part of this chapter analyzes SiGe and SOI waveguides in detail, as both of these material systems have characteristics that are unique from other systems.

2.1 Introduction

Optical waveguides connect various parts of an optical circuit, just as metallic strips connect various electrical components on an integrated circuit. However, optical waves travel in the waveguide in distinct optical modes, with a spatial distribution of optical energy that is confined to the area near the waveguide core. This waveguide is produced by varying the refractive index of the material such that the core has a higher index than the cladding layers on either side. A brief review of the physics of wave propagation in materials is given here, and a more detailed derivation can be found in [14].

The behaviour of electromagnetic waves in matter can be determined by a set

of partial differential equations called Maxwell's equations,

$$\nabla \times \boldsymbol{E} = -\frac{d\boldsymbol{B}}{dt} \tag{2.1}$$

$$\nabla \times \boldsymbol{H} = \boldsymbol{J} + \frac{d\boldsymbol{D}}{dt} \tag{2.2}$$

$$\nabla \cdot \boldsymbol{D} = \rho \tag{2.3}$$

$$\nabla \cdot \boldsymbol{B} = 0 \tag{2.4}$$

where the above quantities are defined as follows:

$\boldsymbol{E}$ the electric field intensity, in V/m;

$\boldsymbol{D}$ the electric displacement vector, in Coul/m^2;

$\boldsymbol{H}$ the magnetic field intensity, in A/m;

$\boldsymbol{B}$ the magnetic displacement vector, in Wb/m^2;

$\boldsymbol{J}$ the electric current density, in A/m^2;

ρ the electric charge density, in Coul/m^3.

These equations are usually combined with the following constitutive relations,

$$\boldsymbol{D} = \epsilon \boldsymbol{E} \tag{2.5}$$

$$\boldsymbol{B} = \mu \boldsymbol{H} \tag{2.6}$$

where ϵ and μ are the dielectric constant and magnetic permeability of the medium respectively, and we have assumed a linear, isotropic medium.

Taking the curl of both sides of Eq. (2.1), combining with Eqs. (2.2),(2.5), and (2.6), and using the vector triple product $\nabla \times \nabla \times \boldsymbol{E} = \nabla(\nabla \cdot \boldsymbol{E}) - \nabla^2 \boldsymbol{E}$, we arrive at the wave equation for the electric field,

$$\nabla^2 \boldsymbol{E} = \epsilon\mu \frac{\partial^2}{\partial t^2} \boldsymbol{E} \tag{2.7}$$

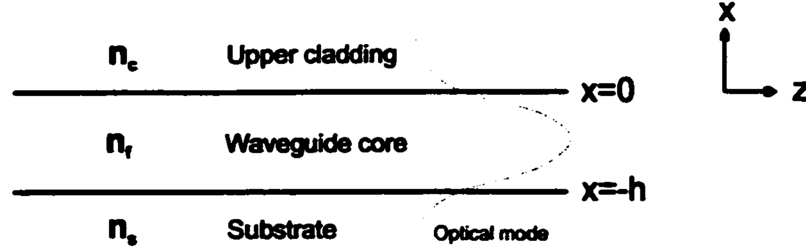


Figure 2.1: The basic geometry of a planar optical waveguide. Optical confinement requires $n_f > n_c$ and $n_f > n_s$

where we assume $J = 0$ and $\rho = 0$ for simplicity. This expression is often reduced to the Helmholtz equation,

$$\nabla^2 \boldsymbol{E} + \omega^2 \mu\epsilon \boldsymbol{E} = 0 \tag{2.8}$$

A similar equation can also be found for the magnetic field,

$$\nabla^2 \boldsymbol{H} + \omega^2 \mu\epsilon \boldsymbol{H} = 0 \tag{2.9}$$

The solutions of Maxwell's equations in an infinite planar waveguide, such as that shown in Fig. 2.1, can therefore be found for either transverse electric (TE) or transverse magnetic (TM) polarized waves by solving Eqs. (2.8) and (2.9). In this case we will examine only the TE modes since both solutions are similar. TE waves propagating in the z direction of the slab waveguide have no x or z electric component, and the solution of Eq. (2.8) is of the form,

$$E_y(x, z, t) = E_y(x)\, e^{i(\beta z - \omega t)} \tag{2.10}$$

where $\omega = 2\pi f$, where f is the frequency of the light, and β is the propagation constant of the waveguide mode. A consequence of Eq. (2.10) is that the velocity component in the z direction can be expressed as $v_z = \omega/\beta$, which determines the effective index N of the medium, $N = \beta/k_o$, where $k_o = 2\pi/\lambda_o = \omega\sqrt{\mu_o \epsilon_o}$. The

boundary conditions for a TE polarized electric field require the continuity of both the electric field and its derivative at a dielectric interface. The obtain a physically meaningful solution the electric field of a confined TE waveguide mode must have the following form:

$$E_y = \begin{cases} A e^{-\gamma_c x} & x > 0 \\ A \cos(\kappa_f x) - \frac{\gamma_c}{\kappa_f} \sin(\kappa_f x) & 0 \geq x \geq -h \\ A \left(\cos(\kappa_f h) + \frac{\gamma_c}{\kappa_f} \sin(\kappa_f h)\right) e^{\gamma_s (x+h)} & x < -h \end{cases} \tag{2.11}$$

This simply requires that the field decay exponentially outside the waveguide core and have a sinusoidal shape inside. The electric field has been made continuous at the dielectric interfaces. Substituting the expressions from Eq. (2.11) into Eq. (2.10), and the result into Eq. (2.8), we obtain the following conditions,

$$\gamma_c^2 = \beta^2 - n_c^2 k^2 \tag{2.12}$$

$$\kappa_f^2 = n_f^2 k^2 - \beta^2 \tag{2.13}$$

$$\gamma_s^2 = \beta^2 - n_s^2 k^2 \tag{2.14}$$

It can be seen from the above equations that the propagation constant β is the vital parameter describing the waveguide mode, since all of the above variables depend on β. To obtain a complete solution for the planar waveguide it is necessary to apply the final boundary condition, which states that $\partial E_y / \partial x$ is continuous at the dielectric boundaries. This leads to the condition,

$$\kappa_f h = m\pi + \tan^{-1}\left(\frac{\gamma_c}{\kappa_f}\right) + \tan^{-1}\left(\frac{\gamma_s}{\kappa_f}\right) \tag{2.15}$$

where $m = 0, 1, 2, \ldots$. The above four equations can be combined to solve for β either numerically or graphically. This results in the propagation constants β_m, where each value of m results in an optically guided mode. Solving for the propagation constant β of each guided mode can become very difficult when considering a more complicated,

n-layer dielectric waveguide structure. An example of the numerical methods required to solve such a problem can be found in [15].

This analysis is further complicated by the fact that we are often concerned not with planar waveguides, but with rib waveguides where the light is confined in two directions. In most applications these waveguide geometries are too complicated to examine exactly, and simplifications are required to determine the propagation constants of the guided modes. A number of different modeling techniques have been developed to solve for guided optical modes and simulate propagation through rib waveguides.

2.2 Modeling Techniques

There are a number of different techniques that can be used for modeling integrated optic devices. This thesis uses primarily the effective index method (EIM) and the beam propagation method (BPM). The EIM is typically used for calculating the propagation constants of waveguide modes, whereas BPM is used to simulate the transmission of light through a photonic device.

2.2.1 The Effective Index Method

The effective index method (EIM) is a very useful approximation method for solving the guided eigenmodes of optical waveguides, and was originally introduced by Knox and Toulios [14].

A waveguide structure such as that illustrated in Fig. 2.2 can be separated into three distinct regions, as shown. In order to calculate the propagation constant β of the waveguide mode, the effective indices in the vertical direction are first calculated for each of the regions N_l and N_f. These values are then used as the refractive indices

in the horizontal direction for calculating β for the waveguide mode.

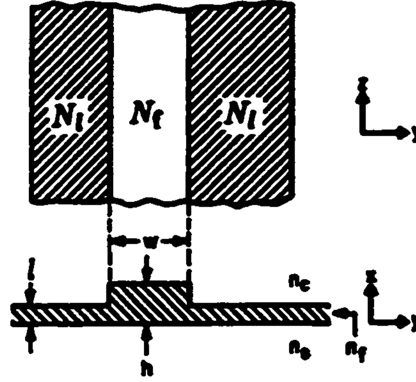


Figure 2.2: Top view and cross section of a rib waveguide used with the effective index method.

The EIM begins by calculating the normalized frequency V for both the rib and slab areas, where V is defined by,

$$V = kt\sqrt{n_f^2 - n_s^2} \tag{2.16}$$

where $k = 2\pi/\lambda$, and t is the thickness h or l of each region respectively. The normalized guide index b is defined as,

$$b = \frac{N^2 - n_s^2}{n_f^2 - n_s^2} \tag{2.17}$$

where N is the effective index of the slab waveguide mode. The asymmetry factor a is defined as,

$$a = \frac{n_s^2 - n_c^2}{n_f^2 - n_s^2} \tag{2.18}$$

With these normalized units the eigenvalue equation for the TE modes, found in Eq. (2.15), is then,

$$V\sqrt{1-b} = m\pi + \tan^{-1}\sqrt{\frac{b}{1-b}} + \tan^{-1}\sqrt{\frac{b+a}{1-b}} \tag{2.19}$$

where $m = 0, 1, 2, \ldots$ This is used to solve for the effective indices N_f and N_l. Once the effective index in each region is determined the problem is turned on its side and these values are used to solve for the effective index of the rib waveguide. This is accomplished as above, using the effective indices N_f and N_l along with the waveguide width w. This results in the propagation constant for the waveguide mode since $\beta = kN$.

This procedure is typically simplified using computer algorithms such as those found in [15], making the EIM a very simple and powerful tool for modeling optical waveguide modes.

2.2.2 The Beam Propagation Method

The EIM can be a useful tool for the modeling of optical waveguides, however in some cases a more powerful simulation technique is required. The EIM is useful for calculating the guided eigenmodes of straight waveguides, but does not simulate the evolution of the electric field as light travels through a device.

The beam propagation method (BPM) is a step-by-step method of modeling the transmission of light through almost any medium. It is based on the Helmholtz equation derived in section 2.1, and consists basically of propagating an input light beam over a small distance through homogeneous space and then correcting for the refractive index distribution seen by the beam during this step. This algorithm is equivalent to treating the waveguide as a periodic system of lenses, and can be examined in more detail in [16].

The main advantage of BPM is that it can treat multimode structures as easily as single-mode structures. It is particularly useful where coupling between radiated fields and guided modes is significant, compared to other methods which

typically neglect the effect of the radiated field [17]. BPM also allows the choice of any initial input excitation, and can easily treat a structure whose refractive index varies along the propagation direction.

A major limitation of BPM is that beams reflected opposite the direction of propagation are ignored. Traditional BPM algorithms are also restricted to small refractive index contrasts, although this limitation has been overcome in some advanced algorithms [18]. BPM is well suited for this thesis work since it can model SiGe devices and certain detector properties, however special considerations are generally required for simulating SOI devices because of the large index contrast between SiO_2 and Si. Three-dimensional SOI structures must be reduced to two-dimensional structures using the EIM before accurate BPM modeling can be performed.

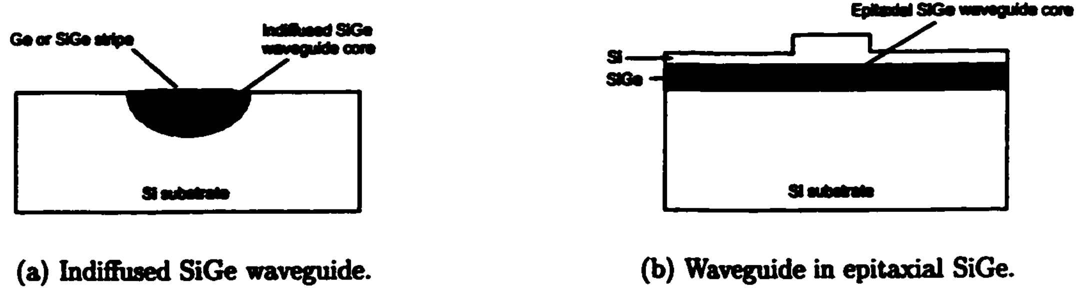
Waveguide modeling for this work was done using two BPM programs. Early modeling was performed using code provided by Dr. D. Yevick from the University of Waterloo. The AWG simulations were performed using a commercial BPM package from Optiwave Inc.

2.3 SiGe Optical Waveguides and Detectors

In recent years there has been an increasing interest in SiGe heterojunction bipolar transistor (HBT) technology. The use of a SiGe layer in the base of an HBT can increase the speed of these transistors and lower the power consumption relative to a typical Si bipolar junction transistor (BJT). The large commitment to SiGe HBT technology has led to the investigation of also using SiGe for integrated optic devices.

Germanium can be used to increase the refractive index of silicon, creating the index difference necessary to support optical waveguiding. Ge can be diffused into Si to create this waveguide core [19], or the SiGe layer can be grown epitaxially

on a Si substrate, as shown in Fig. 2.3. This thesis deals exclusively with epitaxial layers of Si/SiGe, which can be fabricated by either MBE or CVD growth. Since the bandgap of $Si_{1-x}Ge_x$ shifts to longer wavelengths with increasing Ge content, x is limited to $x \leq 0.2$ in order to avoid absorption at $\lambda = 1.3$ μm.



(a) Indiffused SiGe waveguide.

(b) Waveguide in epitaxial SiGe.

Figure 2.3: SiGe optical waveguides

Pure Si at wavelengths near 1.3 μm and 1.55 μm has a refractive index of $n_{\mathrm{Si}} \approx 3.5$, whereas pure Ge has a refractive index of $n_{\mathrm{Ge}} \approx 4.3$. The assumption of a linear relationship between the Ge content and the refractive index of a SiGe layer is approximately valid for indiffused waveguides. For strained layers, resulting from epitaxial growth on Si substrates, a relationship between the Ge content x and the refractive index of the SiGe layer was found experimentally in the early stages of this research project [20],

$$n_{\mathrm{TE}} = n_{\mathrm{Si}} + (0.34 \pm 0.05)\,x \tag{2.20}$$

$$n_{\mathrm{TM}} = n_{\mathrm{Si}} + (0.55 \pm 0.05)\,x \tag{2.21}$$

The strain in the epitaxial layers results in a large birefringence, represented by the different effective indices for TE and TM polarizations. This strain results from the 4.2% lattice mismatch between Si and Ge. SiGe has a larger lattice parameter than Si, and therefore epitaxial layers of SiGe on a Si substrate will be strained, with the

magnitude of the strain dependent on the Ge concentration. This strain is compressive in the plane of growth and tensile perpendicular to the plane of growth. This results in a large birefringence since the strain contributions to refractive index for TE and TM polarizations have opposite sign.

This strain limits the maximum Ge content and thickness that can be grown before the structure relaxes through dislocation formation. This thickness is termed the critical thickness h_c. If the epilayer thickness is below h_c then the SiGe lattice contracts elastically to accommodate the mismatch, resulting in a compressively strained layer with no defects . However if the thickness exceeds t_c then threading dislocations form at the Si/SiGe interface. At this point the strain is partially relaxed through dislocations and the remaining strain is accommodated by elastic deformation of the crystal lattice, meaning that even after dislocation formation the structure is still partially strained. The transition from a stable strained layer to a partially relaxed layer happens quite abruptly as the film thickness exceeds h_c [21].

The critical thickness is a function of Ge content and can be calculated for a structure such as that shown in Fig. 2.3(b). If the relaxation process goes to completion an energy minimum is attained [21]. Further relaxation by dislocation formation is unlikely, since although plastic relaxation reduces elastic strain energy, the dislocation self-energy increases the overall energy of the multilayer as the dislocation density increases. Alloys that are coherently strained to fit the Si substrate have a strain ϵ given by,

$$\epsilon = \frac{(a_{Ge} - a_{Si})}{a_{Si}} x \tag{2.22}$$

where a_{Si} and a_{Ge} are the lattice constants for unstrained Si and Ge, respectively, x is the Ge content, and the substrate is assumed to be unstrained. For SiGe $\epsilon = 0.042\,x$.

The energy per unit area associated with elastic strain in a film is [22]

$$E_{\text{strain}} = 2\mu \frac{(1+\nu)}{(1-\nu)} \epsilon^2 h \tag{2.23}$$

where μ is the shear modulus, ν is Poisson's ratio, and h is the distance from the free surface. The energy per unit length of an isolated dislocation segment can be written as [21],

$$E_{\text{disl}} = \frac{\mu b^2 (1 - \nu \cos^2\theta)}{4\pi(1-\nu)} \ln\left(\frac{4h}{b}\right) \tag{2.24}$$

where b is the Burgers vector, and θ is the angle between the dislocation line and its Burgers vector.

Partial relaxation of the strain is accomplished by introducing pairs of orthogonal misfit dislocations with a spacing of $b\cos\lambda/\epsilon$ [21], where λ is the angle between the Burgers vector and the direction in the film plane normal to the dislocation line. The energy per unit area of a partially relaxed heterostructure is therefore

$$E_{\text{f}} = \frac{2\epsilon\, E_{\text{disl}}}{b\cos\lambda} + E_{\text{strain}} \tag{2.25}$$

The minimum energy for a partially relaxed heterostructure is found when $dE_{\text{f}}/d\epsilon = 0$ and the strain energy reduction just balances the increase in dislocation energy. This defines the onset of dislocation formation. It can be used to provide an expression for the critical thickness of the strained layer,

$$h_c = \frac{b\,(1 - \nu\cos^2\theta)}{8\pi\,(1+\nu)\,\epsilon\cos\lambda} \ln\left(\frac{4h_c}{b}\right) \tag{2.26}$$

This equation is similar to that originally proposed by Matthews and Blakeslee in [23], [22]. Values applicable to the Si/SiGe system are $\nu = 0.28$, $\cos\theta = \cos\lambda = 0.5$, appropriate for 60° glide dislocations, and $b \approx 0.4$ nm is the Burgers vector for dislocations of the $a/2\langle 110\rangle$ type. Since $\epsilon = 0.042\,x$ for $Si_{1-x}Ge_x$,

$$h_c = \frac{5.5}{x} \ln(10 h_c) \tag{2.27}$$

which represents the equilibrium critical thickness for an uncapped single strained layer of $Si_{1-x}Ge_x$. The critical thickness can vary slightly for buried strained layers and strained-layer superlattices [21].

The "equilibrium" critical thickness refers to the epilayer thickness for which no dislocation formation will occur regardless of processing temperature (up to the material melting point). If we restrict ourselves to lower temperatures then it is possible to define a "metastable" critical thickness. In this case the epilayer will remain pseudomorphic until the relaxation temperature is exceeded, at which point dislocation formation begins. Some of these critical thicknesses are illustrated in Fig. 2.4.

As shown in Fig. 2.4, the metastable h_c for low Ge contents can often be orders of magnitude larger than the equilibrium h_c. This is important since nearly all SiGe layers suitable for optical waveguiding conform to a certain metastable h_c, but exceed the equilibrium h_c. This issue will be dealt with in more detail when discussing the Local Oxidation of Silicon.

The strain in a crystal and the degree of relaxation, among other properties, are often measured by x-ray diffraction techniques. The physical principles governing this technique can be found in a number of sources [24], [25], and will not be reviewed here. However, the interpretation of x-ray rocking curves will be briefly reviewed, because this is important to the characterization of the SiGe structures used in this work.

A typical x-ray rocking curve for a strained SiGe layer is shown in Fig. 2.5. The vertical axis represents the countrate, or intensity, of the x-rays reflected off the crystal lattice. The horizontal axis represents the angle, in arcseconds, of the rocking sample, and is in effect a measure of the lattice constant of the sample in the growth

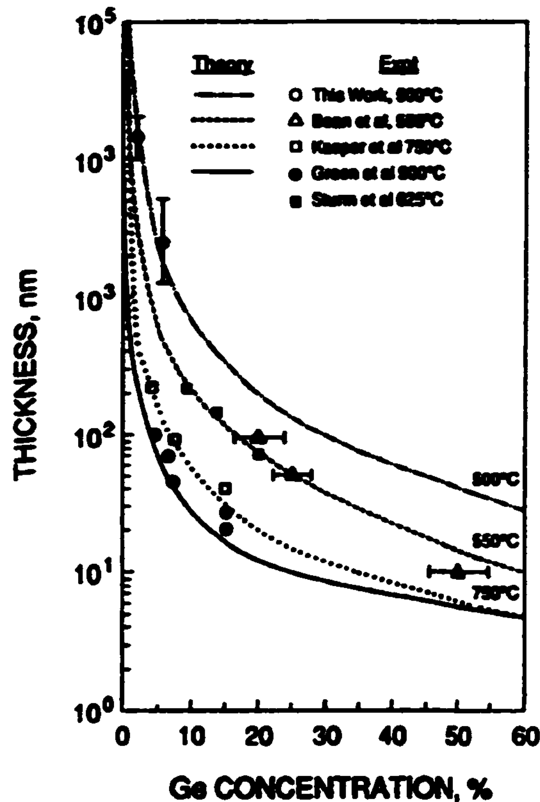


Figure 2.4: Equilibrium and metastable critical thicknesses for SiGe epilayers. The equilibrium critical thickness of Matthews and co-workers is denoted by the solid line. The theoretical curves for metastable critical thickness are based on theory derived in [2], and are calculated for relaxation temperatures of 750, 550, and 500°C, as noted on the figure. Adapted from [2].

direction. The large peak at the right of the figure is the substrate peak, and results from the high count of x-rays reflected off the crystal lattice of the Si substrate. Ideally, this large peak should have a single maximum, but two maxima can be seen in the peak. This results from the reference crystal used in the x-ray system, which in this case is InP rather than Si. The x-ray diffraction system available at McMaster is typically used for the characterization of InP and is therefore equipped with an InP crystal. When used for characterizing Si/SiGe this results in slightly lower angular

resolution, but is quite sufficient for the analysis performed in this work. The impact is further minimized by the fact that in this work we are more concerned with the relative change in the width and location of diffraction peaks, rather than the absolute measurement of their half-width.

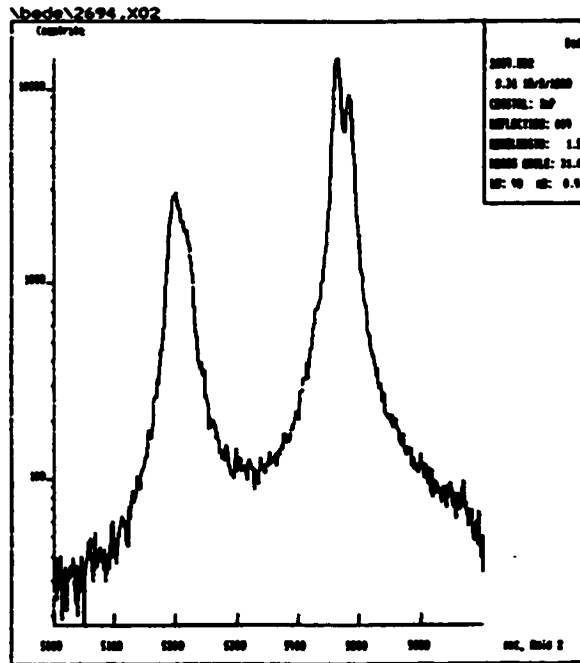


Figure 2.5: X-ray rocking curve for an as-grown SiGe heterostructure with germanium concentration of 2.7%.

The peak at the left of Fig. 2.5 results from the strained SiGe layer. The SiGe layer is compressively strained to match the Si lattice constant, which forces the lattice to expand in the vertical direction. This larger lattice constant is seen as a peak in the x-ray rocking curve. The sharp peak, with half-width comparable to that of the substrate peak, indicates that the layer is fully strained and pseudomorphic. The angular splitting between the substrate peak and the SiGe peak can be calibrated to represent the strain in the layer. In this case the splitting is 262 arcsec, which corresponds to a strain of approximately 0.11%. Note that the numbers on the x-

axis are arbitrary and that only the relative numbers are important to measure the splitting of the peaks. These x-axis values will in fact vary with how the sample is orientated in the system, and x-ray rocking curves are sometimes normalized so that the substrate peak corresponds to 0 arcsec.

Fig. 2.6 shows the x-ray rocking curve for the same sample after a 3.9 h anneal at 900°C. The broadening of the SiGe peak is indicative of misfit dislocation formation within the SiGe layer. In [26], the dislocation density ρ in the SiGe epilayer is estimated from the peak broadening $\Delta\theta$ using the expression,

$$\rho = \frac{(\Delta\theta)^2}{18\, b^2} \tag{2.28}$$

where b is the Burger's vector of the dislocation. This peak broadening is typically accompanied by a slight shift in the location of the peak, in the direction of the substrate peak, which indicates that the strain in the layer has partially relaxed.

Critical thickness considerations impose some very restrictive design criteria for SiGe optical waveguides, because when the structure relaxes through dislocations the optical losses in the material increase and the wafer can become unsuitable for electronic devices. SiGe is suitable for making photodetectors when the Ge content is increased to over 50%, as will be discussed in Chap. 5. However, the potential for SiGe optical waveguides is very limited by the strain, and they are therefore not used extensively in this thesis, although some early devices based on SiGe waveguides will be presented. In order to overcome the limitations of SiGe optical waveguides we have concentrated on silicon-on-insulator wafers.

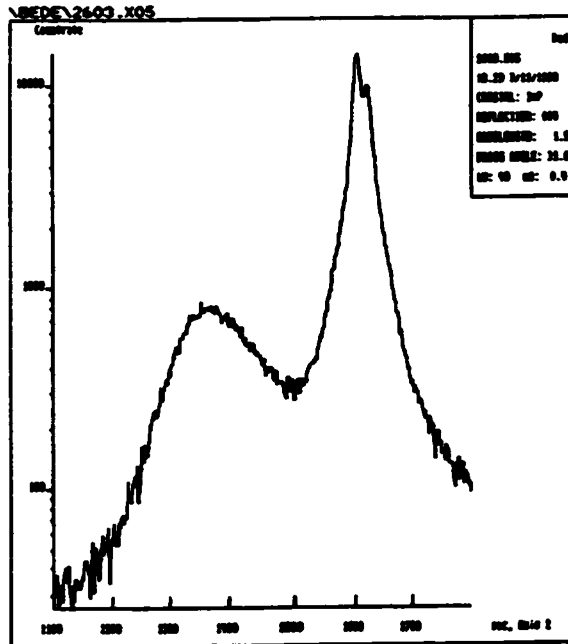


Figure 2.6: X-ray rocking curve for a SiGe heterostructure with Ge concentration of 2.7% after a 3.9 h anneal at 900°C.

2.4 SOI Optical Waveguides

Silicon-on-insulator technology offers tremendous potential for cost-effective photonic components. Interest in SOI has grown rapidly in recent years since, like SiGe, the structure allows for the fabrication of electrical devices that operate at higher speeds and lower power levels than traditional Si devices. SOI is completely compatible with well-established Si processing technology, such as the LOCOS process which will be discussed in Chap. 3.

SOI substrates can be fabricated using a variety of techniques, such as Separation by Implantation of Oxygen (SIMOX-SOI) [27], Smart-Cut [28], and Bond-and-Etchback (BESOI) [29]. This research utilized SIMOX SOI purchased from IBIS Technology Inc.

The SIMOX process is illustrated in Fig. 2.7. It begins with a common ⟨100⟩ Si substrate, which is then implanted with oxygen at high doses, typically $\geq 10^{18}\text{cm}^{-2}$ at 200 keV. A high temperature anneal at 1300°C for 6 h follows, which forms a buried SiO_2 layer in the Si wafer, and helps to eliminate the damage caused by the implantation. This results in a crystalline layer of silicon, typically about 200 nm thick, above a buried SiO_2 layer typically about 400 nm thick. This top Si layer is too thin for most optical applications, and therefore an additional layer of epitaxial Si is grown on this layer to whatever total thickness is desired. The result is a single-crystal layer of Si isolated from the Si substrate by a buried layer of SiO_2. Since the refractive index of Si is approximately 3.5 and that of SiO_2 is about 1.46, the SOI layer forms an optical waveguide layer.

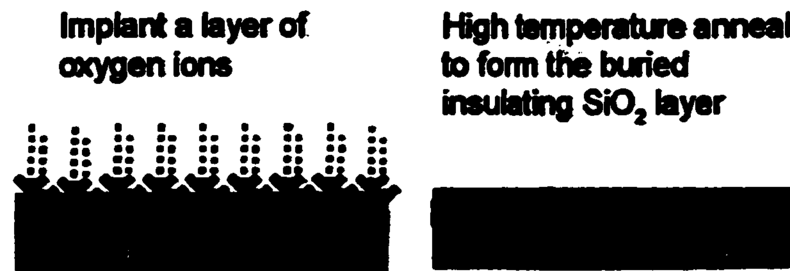


Figure 2.7: The SIMOX process for fabricating SOI wafers. Epitaxial growth of Si typically follows this substrate preparation.

SOI waveguides are unlike most other photonic systems in that the thick layers, in conjunction with high refractive index steps in the vertical direction, make any single-mode operation seem questionable. However, it has been shown that for certain rib dimensions a single-mode ridge waveguide exists even if the corresponding slab waveguide is multimode [3].

This behaviour can be understood by considering a rib waveguide of well defined height and width. If the width and height are chosen so that all high order

modes in the rib have propagation constants lower than that of the fundamental mode of the slab waveguide regions on either side of the rib, these modes are filtered out by leaking away. Only the fundamental mode in the rib survives, since only its propagation constant is higher than that of the fundamental mode of the slab waveguide regions. Therefore, even if a higher-order mode is launched by off-axis excitation, the light will evolve to the fundamental mode as it propagates, resulting in a single-mode waveguide. This evolution into the fundamental mode generally occurs over a distance of less than 2000 μm [4].

Mathematical treatments of this behaviour can be found in [3] and [4]. In [3], the condition for single-mode propagation is determined by taking into account cutoff values from numerical solutions of the waveguide V parameter. In [4], this treatment is extended to a modified version of the effective index method (EIM), which eliminates the curve-fitting approximations used in [3]. The results are design conditions that dictate the rib width/height ratio necessary for single-mode operation. Referring to Fig. 2.8, single-mode operation requires

$$\frac{w}{H} \leq c + \frac{r}{\sqrt{1-r^2}} \tag{2.29}$$

where $r = h/H$, and $c = 0.3$ in [3] and $c = 0$ in [4]. The condition in Eq. (2.29) is only valid for $r > 0.5$, since at lower values of r the effective index of the fundamental slab mode becomes lower than the effective index of any higher-order vertical modes in the central rib region.

The condition in Eq. (2.29) has been compared to a large array of SOI waveguide structures in order to confirm its validity [4]. This data is shown in Fig. 2.9, and is a very convenient reference for designing single-mode SOI waveguides.

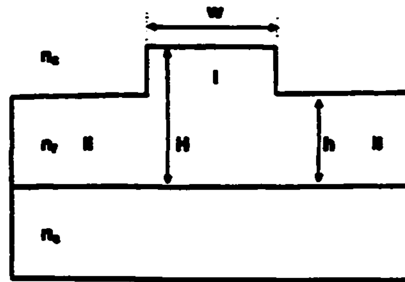


Figure 2.8: Schematic of a rib waveguide in SOI.

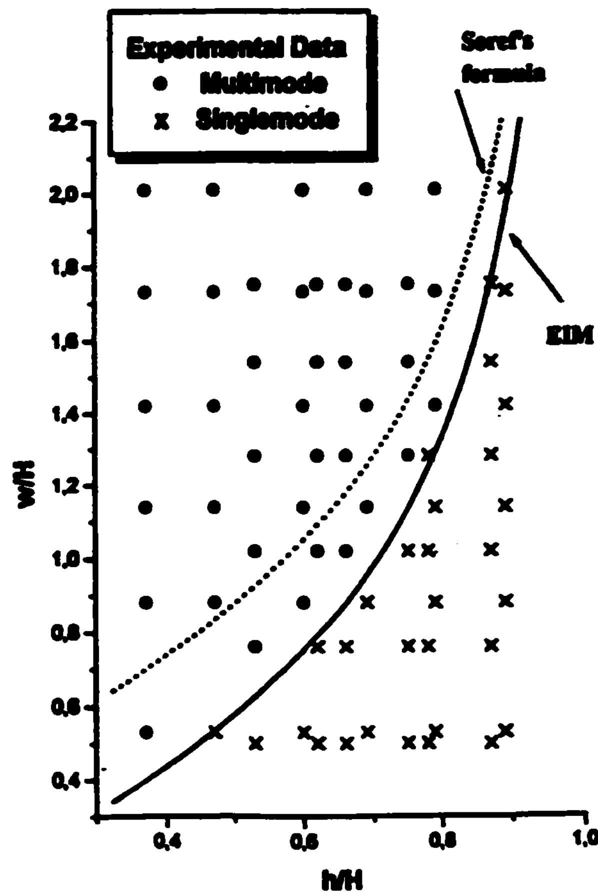


Figure 2.9: Plots of theoretical curves for the single-mode limit determined by Soref [3], and by using the EIM [4]. The circles and crosses correspond to experimental observations of multimode and single-mode waveguides, respectively. From [4].

Chapter 3

LOCOS Optical Waveguides

3.1 The Local Oxidation of Silicon

The pursuit of viable silicon-based optoelectronics is motivated in part by the potential for fabricating optical components using standard, well established, VLSI processing. This would allow for the very inexpensive, mass production of optical components at facilities that are currently limited to producing only electronic devices. Furthermore, a fabrication process that is suitable for both optics and electronics would significantly advance the pursuit of monolithic optoelectronic integration, essential for FTTH components and high-speed computing.

The use of standard Si electronics processing for the fabrication of optical waveguides presents a number of challenges. The structure of an optical waveguide is similar to that of a transistor well, which is a raised area of Si on which individual transistors are fabricated. The depression between transistor wells is filled with SiO_2 to electrically isolate the adjoining transistors. However, the physical size of these transistor wells can be significantly different than the dimensions of a typical rib waveguide. Furthermore, electronics are typically fabricated on Si substrates, but optical waveguides require a change in refractive index, necessitating a slightly different material system, such as Si/SiGe . This introduces a number of difficulties.

One of the essential steps in VLSI processing is the Local Oxidation of Silicon (LOCOS). This process is very common and is used in the production of virtually all Si integrated circuits. A Si_3N_4 masking layer of roughly 200 nm is deposited by chemical vapor deposition (CVD). Because of the thermal expansion mismatch to silicon, a thin (~30 nm) layer of SiO_2 is usually grown before this for strain compensation, as illustrated in Fig. 3.1. This structure is then placed in an oxidizing furnace at a temperature between 800 and 1200°C, with a wet-oxygen atmosphere, for times of 30 minutes to several hours. The silicon in the unmasked regions is oxidized, consuming silicon to create SiO_2. At the edges of the SiO_2/Si_3N_4 layer, the thermal oxide encroaches under the mask, resulting in the "bird's beak" structure that is characteristic of the LOCOS process.

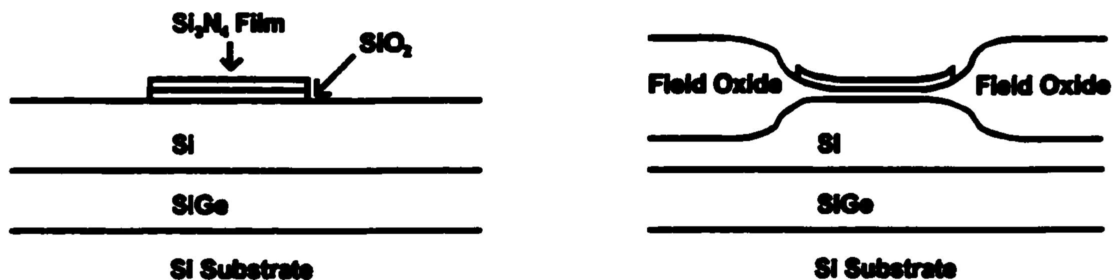


Figure 3.1: The LOCOS process. The masking layers, and the structure after several hours in an oxidizing furnace.

This research has been aimed at using the LOCOS process to define an optical waveguide in a Si-based system. Although the illustration in Fig. 3.1 resembles a rib waveguide, the feature height that is typically used for electronics applications is on the order of 100 nm, which is far too small to provide adequate optical confinement in a rib or strip-loaded waveguide, which is often an order of magnitude larger. The use of the LOCOS process for optical waveguide fabrication has never been reported

in the literature prior to this author's initial presentation of the technique [30], and offers the potential for true high-volume production of photonic components.

3.2 SiGe LOCOS Waveguides

The idea of using the LOCOS process to fabricate optical waveguides in SiGe was first conceived by S.J. Kovacic and J.J. Ojha at Nortel Networks Ltd. [31], collaborators on this project. The development of the process beyond theoretical concepts was performed entirely at McMaster, and the process was further adapted for use in SOI, where it was found to be a commercially viable technology [32]. The original idea for SiGe LOCOS waveguides was found to be of limited practical use because of the crystal damage induced during high temperature processing. However, the developments presented in this thesis help to minimize this damage and make the process more suitable for the fabrication of photonic components.

Electronic devices in SiGe typically use SiGe layers below the critical thickness so that dislocations are not induced during high-temperature IC processing. However, any single SiGe layer that is sufficiently thick to provide good optical confinement is inevitably above this critical thickness and will relax at these high temperatures.

The relaxation of SiGe layers at high temperatures can significantly affect the optical loss in the material, and the wafer can become unsuitable for electronic devices. The aim of this work is to fabricate optical waveguides in SiGe using standard high-temperature silicon IC processing techniques, while maintaining the induced dislocation density at a level acceptable for optical waveguiding. As a result of this work, a number of processing and design conditions have been developed to minimize the induced dislocation density to levels acceptable for optical waveguiding, including the use of temperature effects and mask layer design.

3.2.1 Temperature Effects

Typical SiGe optical waveguide layers are invariably above even a metastable critical thickness for temperatures exceeding about 800°C. Processing at relatively low temperatures, close to this metastable limit, was initially thought to be a means of minimizing the induced misfit dislocation density. Two factors make this incorrect for SiGe waveguide layers.

First, it has been shown in a number of articles that for temperatures above 800°C the interdiffusion of Ge in Si can become significant [21], [2]. Although a relatively small effect in fully strained layers below the critical thickness, the diffusion becomes significant when dislocations are introduced. Misfit dislocations facilitate the diffusion of Ge into neighboring Si layers. This yields a competing mechanism for interfacial strain relaxation, reducing the amount of relaxation due to dislocation formation. At higher processing temperatures this diffusion is enhanced, making it more likely for layers to relax through interdiffusion than by dislocation formation. Since the diffusion length is quite small compared to a typical waveguiding layer the effect on the optical mode is minimal, but the effect on dislocation formation can be significant. Ge in Si at 1200°C has a diffusion coefficient of about 10^{-2} $\mu m^2/h$ [33], suggesting that under typical LOCOS processing conditions of 1050°C for 3 h, the Ge will diffuse a distance of around 100 nm. This helps maintain the Ge near the waveguide core and should not have a major effect cn the waveguiding properties of a SiGe layer 1000 nm thick, typical for optical waveguiding, although it could potentially affect the performance of some photonic devices.

Second, it was shown in [34] that the onset of dislocation formation is quite abrupt, and very rapid to evolve to a more stable state where further temperature cycling has little effect. However, it is important to note that dislocation formation

continues in this state, albeit at a much reduced rate. This fact can potentially be used to help minimize dislocation formation by increasing the oxidation temperature, which minimizes the time required for oxidation. Minimizing the time in the furnace minimizes any further dislocation formation that occurs during thermal oxide growth. Although in [34] no further relaxation was observed after an additional 30 min of annealing, the oxidation times required for processing at 800°C can often be over twenty hours longer than those required for 1050°C. These significantly longer times can potentially lead to a high number of subsequent dislocations. For a given time, the dislocation density induced by processing at 900°C will not exceed that corresponding to 1100°C. But for a given oxide thickness, it is possible for the dislocation density induced by processing at 900°C to slightly exceed that corresponding to 1100°C. This effect is illustrated in Fig. 3.2. Although the benefit from this effect is expected to be very small, coupled with the interdiffusion discussed above and the mask layers discussed below, we expect to reduce the dislocation density by more than an order of magnitude.

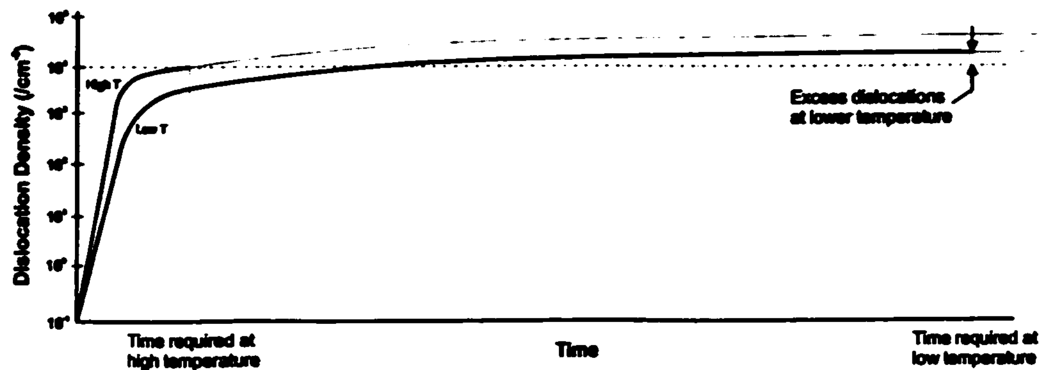


Figure 3.2: Illustration of the effects of processing at different temperatures.

The dislocations induced during LOCOS processing can be reduced by choosing appropriate temperatures as discussed above, however they cannot be completely

eliminated. Therefore a second means of optimizing the LOCOS process would also be advantageous. The use of strain-compensating mask layers are one possibility.

3.2.2 Strain-Compensating Mask Layer

The LOCOS process typically involves depositing a masking layer of Si_3N_4, which acts as a barrier for the oxidation process. However, due to the large strain that can be imposed by the different thermal expansion coefficients of Si and Si_3N_4, a thin layer of SiO_2 is generally deposited first. A modification of this mask layer design was investigated as a means of improving the LOCOS process for SiGe.

The main problem encountered during LOCOS processing of SiGe is that the inherent strain in the SiGe layer causes the structure to relax through dislocation formation at high temperatures. We have investigated the use of the strain in the SiO_2/Si_3N_4 masking layer to help compensate the strain of the SiGe layer. By modifying the thicknesses and deposition temperatures of the SiO_2/Si_3N_4 masking layers, the resulting strain can be tailored so that it opposes the strain inherent to the SiGe layer. This helps reduce the strain in the SiGe layer during oxidation, and can thereby reduce the induced dislocation formation at high temperatures.

It is generally desirable to have an opposing strain in the mask layer that is larger than the strain of the SiGe layer. The reason for this is that the strain field from the mask layer must extend through the top Si cladding in order to affect the SiGe layer. Although the strain field will generally extend several microns [35], far enough to overlap the SiGe layer, the magnitude of the field decreases with distance.

Unfortunately, the thermal properties of the SiO_2/Si_3N_4 films deposited for this work were very dependent on deposition conditions, and it was therefore difficult to model the mask layer parameters that resulted in the best strain compensation.

Furthermore, this strain compensation is dependent on thermal expansion coefficients, and ideally is optimized for the best strain compensation at the oxidation temperature, which is typically above 1000°C. Since measurements of the resulting strain are impossible at these temperatures, the effects can only be inferred from experimental evidence deriving from the resulting rocking x-ray curves and optical properties of the samples after oxidation.

The temperature considerations discussed above help to minimize the dislocation formation during LOCOS processing, but do not eliminate it. Likewise, the strain of the masking layers can only be used to help lower the strain in the SiGe layer during oxidation, not completely eliminate it. This means that although the damage to the wafer can be minimized, the optical properties will be affected and the constraints on waveguide design can be very restrictive. In order to take full advantage of the LOCOS process for making commercial photonic components at low cost, a different material system must be investigated. The use of silicon-on-insulator as a substrate for LOCOS optical waveguides was investigated for this work, and was found to be vastly superior to SiGe.

3.3 SOI LOCOS Waveguides

The use of SOI for LOCOS optical waveguides eliminates virtually all of the problems inherent to the SiGe material system. The SOI material system has only very recently matured to a commercial technology, and in fact was not widely available even at the start of this research project. However, today it is a rapidly emerging technology that appears very promising for both optics and electronics. Most of our current research efforts have shifted from SiGe to SOI.

The temperature considerations and strain-compensating mask layers developed for the SiGe system are not necessary in SOI. SOI has no strained epitaxial layer and therefore does not dislocate at high temperatures. The optical loss in the material is therefore unaffected by the LOCOS process. The material itself has no inherent birefringence, so is very well suited for photonic devices. Furthermore, the maximum ridge heights achievable are no longer limited by the material considerations, but only by the self-limiting nature of the LOCOS process.

With SOI it is not necessary to use the mask layer for strain compensation, and therefore other mask materials can replace the SiO_2/Si_3N_4. Metal can easily be evaporated onto the surface and patterned as a mask to oxidation. A number of metals have melting points above 1300°C and are suitable for this application, including nickel, titanium, and chromium. The LOCOS technique could be a completely thermal process if a thick thermal oxide could be grown and patterned, and act as a mask inhibiting oxidation of the underlying silicon. All of these techniques were investigated and are discussed in Chap. 6.

LOCOS optical waveguides in SOI can in theory exhibit lower loss than conventionally-etched waveguides in the same material. Since the telecommunications wavelengths are far from the Si absorption edge, the majority of the optical loss for etched SOI waveguides is due to the sidewall roughness that results from typical reactive ion etches or chemical etches. The LOCOS process, by its very nature, smooths these sidewalls as the waveguide is created.

Chapter 4

Passive WDM Components

This work concentrated mainly on optical components intended for WDM/DWDM networks. The rapid expansion of optical communications networks demands inexpensive optical components for these applications. The first WDM components fabricated for this work were 1.3/1.55 μm duplexers in SiGe, intended for FTTH applications. The shift to SOI and the pursuit of DWDM components led to the design and fabrication of arrayed waveguide grating (AWG) demultiplexers, the main focus of this work. Coupled with the SiGe photodetector technology also developed in this thesis, these represent the necessary components for a monolithically integrated receiver chip suitable for low cost DWDM.

4.1 1.3/1.55 μm Duplexer

The early stages of this research project were focused on measuring the material properties of SiGe optical waveguides, including the refractive index and birefringence [20]. This work was followed by some preliminary development of the LOCOS process in SiGe [30]. In order to validate the materials characterization that was done in this work, a very simple photonic device was designed for demultiplexing 1.3 and 1.55 μm wavelengths. This device is completely passive, and therefore the operation

depends entirely on the material parameters of the device.

A simple directional coupler was chosen for modeling and fabrication. This device was optimized for the demultiplexing of 1.3/1.55 μm wavelength inputs by specially tailoring the coupling section of the device. This type of duplexer is suitable for Fiber-to-the-Home (FTTH) transceivers, in which 1.3 μm and 1.55 μm signals are received and transmitted simultaneously. A simple and inexpensive demultiplexer is required for this device. This duplexer design was not intended to be original, and has already been reported in the literature [36]. It was intended to be a demonstration of the validity of our materials research and LOCOS development. At the time of this work there were no such devices designed in SiGe, and more importantly, this would be the first report of any SiGe photonic device fabricated using the LOCOS process.

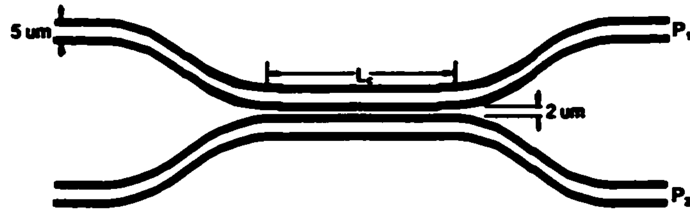
The duplexer is based on a directional coupler, and is illustrated in Fig. 4.1(a). The modeling of these devices was done using two-dimensional BPM. Light is input the upper waveguide, which is single-mode. In the coupling section, a second identical guide is brought close enough that the waveguide modes overlap. Due to these coupled modes, power is transferred from one guide to the next.

The coupling length L_c is defined as the length in the coupling section that is required for complete transfer of power from one guide to the other. Power oscillates between the coupler modes with a coupling length given by $L_c = \pi/2\kappa$, where the coupling coefficient κ is a measure of the overlap integral between the coupled modes [37]. The length L_c can be tailored by varying the etch depth, rib width, or waveguide spacing. It is also dependent on wavelength, and therefore the device can be used as a demultiplexer if designed so that,

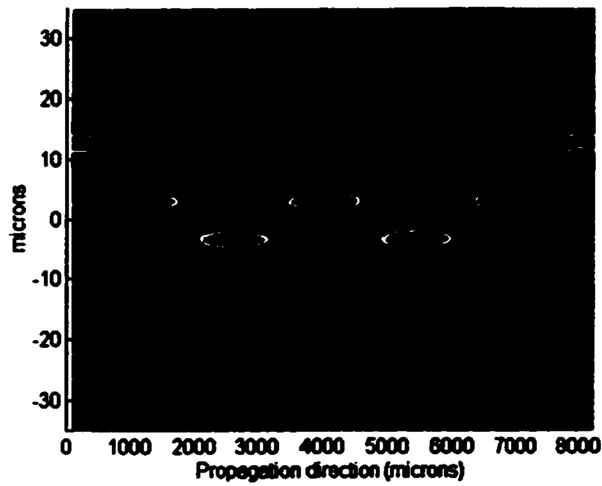
$$mL_{c(1.3\mu m)} = (m + 1/2)L_{c(1.55\mu m)} \tag{4.1}$$

where m is an integer.

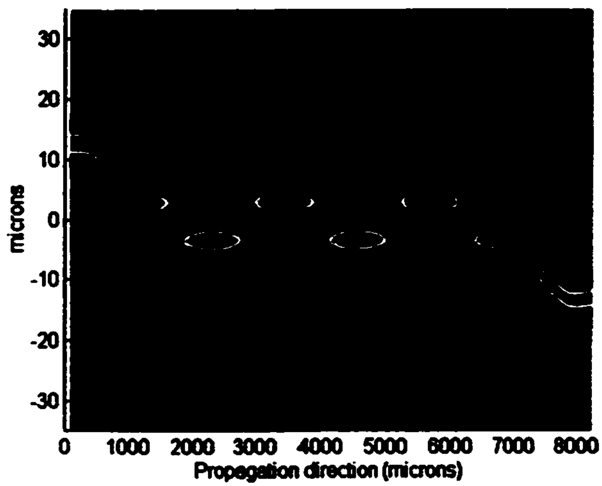
An example of the device operation is shown in Figs. 4.1(b) and 4.1(c). These figures show the BPM simulations of the duplexer for 1.3 and 1.55 μm wavelengths. The length and separation of the waveguides in the coupling section were varied in order to satisfy Eq. (4.1). The devices operate only for one polarization due to the large birefringence in the SiGe waveguides, which creates a different coupling length for TE and TM polarized light. This is a major issue for photonic devices, and eventually led to our adoption of SOI as a photonic system.



(a) Device layout.



(b) 1.3 μm wavelength TE light.



(c) 1.55 μm wavelength TE light.

Figure 4.1: 1.3/1.55 μm duplexer layout and BPM simulations. Note that light is input the top left waveguide in both cases.

4.2 Arrayed Waveguide Grating Demultiplexer

This section presents the operating principles of arrayed waveguide grating demultiplexers, and some design issues specific to SOI. These devices represent a main focus of this work, and will therefore be discussed in detail.

Many principles have been proposed and reported for realization of DWDM demultiplexers. Most commercially available components are based on dielectric filters, but as channel counts increase these devices become restrictively expensive to fabricate. Arrayed waveguide grating demultiplexers (AWGs) are one possible solution. AWG demultiplexers, also referred to as phased array demultiplexers, are realized in conventional waveguide technology and do not require the vertical etching or difficult fabrication steps often needed for other demultiplexer designs.

AWGs were proposed in 1988 by Smit [38], and have advanced over the past decade to incorporate higher channel counts [39] and polarization insensitivity [40]. Devices reported to date have typically been fabricated in either InP or silica-based systems. The use of SOI to fabricate these components offers the potential for low cost, small device size, polarization insensitivity, compatibility with standard Si electronics, and LOCOS processing.

4.2.1 Principles of Operation

The theory governing AWG operation will be discussed here, however more information can be found in [5], [41]. The layout of an AWG is shown in Fig. 4.2. The device consists of an input waveguide and a series of output waveguides coupled to a waveguide array through slab waveguide regions. Light is input from the left, and consists of a number of channels centered around 1550 nm. As the light enters the free propagation region (FPR), it is no longer laterally confined and becomes

divergent through this slab waveguide section, sometimes referred to as the splitter. On arriving at the input aperture the beam is coupled into the array waveguides. The radius of the input aperture is chosen so that the waveguides in the array will all be excited with the same phase. The length of the array waveguides is chosen such that the optical path length difference between adjacent waveguides equals an integer multiple of the centre channel wavelength. For this wavelength, the fields in each waveguide arrive at the output aperture with equal phase, apart from integer multiples of 2π, and the field distribution at the input aperture will be reproduced at the output aperture. This now corresponds to a convergent beam, and an image of the beam at the object plane will be formed at the centre of the image plane. This focused beam is coupled into an output waveguide at the image plane, and the light exits to the right.

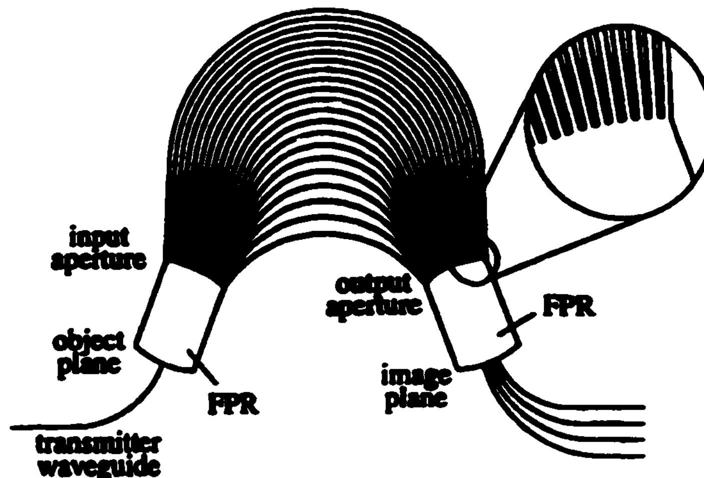


Figure 4.2: Layout of an arrayed waveguide grating demultiplexer. Adapted from [5]

For other wavelengths, the input into the array waveguides happens identically to that of the centre channel. The separation of the different wavelength

channels begins in the array. Since each wavelength has a slightly different propagation constant, each wavelength will experience a slightly different phase shift while traveling through the array. The linearly increasing length of the array waveguides causes the phase change, induced by a change in the wavelength, to vary linearly along the output aperture. The resulting beam will be "steered" to a different point along the image plane.[1] The phase front will tilt with varying wavelength, thus sweeping the focal spot across different output waveguides. By placing receiver waveguides at proper positions along the image plane, spatial separation of the different wavelength channels can be obtained.

Rowland Mountings

The planar waveguide sections of an AWG are often referred to as the splitter and combiner. In the splitter the input beam diverges to fill all of the array waveguides, and in the combiner the beam from the output aperture gets focused onto the image plane. If the splitter and combiner are not designed properly, then the output beam will not be properly focused on the output waveguides. This can contribute to crosstalk and device loss, since the beam could overlap other output waveguides, and not all of the power will be coupled into the intended waveguide.

The splitter and combiner are typical examples of Rowland mountings [41]. Fig. 4.3 illustrates the Rowland mounting and how it relates to the splitter and combiner. In its simplest form, the Rowland mounting condition states that the focal line of the mounting follows a circle with radius $R_r = R_a/2$, where R_a is the distance from center of the image plane to the array waveguides, as shown in Fig. 4.3. This focal line forms the image plane for the AWG, and the receiver waveguides should be

[1]This effect is similar to that used in a phased array antenna, where small phase shifts are induced between the transmitters in order to steer the beam in different directions. Further detail can be found in [42].

positioned on this line.

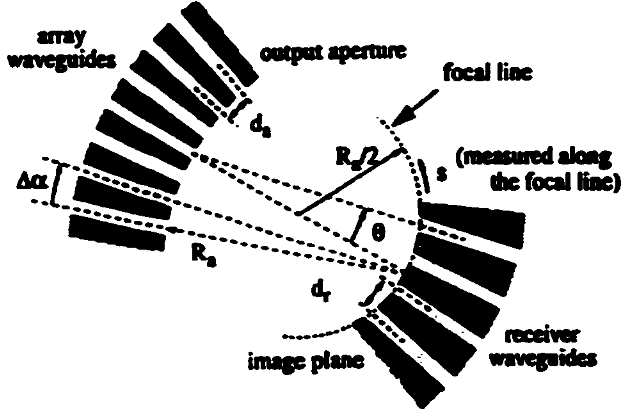


Figure 4.3: Geometry of the Rowland mounting. Adapted from [5]

Phased Array

The centre channel of the AWG is determined by the length difference ΔL between adjacent array waveguides,

$$\Delta L = \frac{m\lambda_c}{N} \tag{4.2}$$

where m is the order of the phased array, λ_c is the central wavelength in vacuo, and N is the effective index of the waveguide mode.

To determine the angular position at which different wavelengths will be focused onto the image plane, we need to determine the dispersion angle θ resulting from a phase difference $\Delta\Phi$ between adjacent waveguides. Referring to Fig. 4.3,

$$\theta = \sin^{-1}\left(\frac{\Delta\Phi - 2\pi m}{\beta_s d_a}\right) \tag{4.3}$$

where $\Delta\Phi = \beta_a \Delta L$, β_a and β_s are the propagation constants of the array waveguide mode and the slab mode in the splitter/combiner, respectively, and d_a is the center to

center spacing of the array waveguides [5]. The dispersion D of the array is defined as the lateral displacement of the focal spot along the image plane per unit frequency. Assuming small angles for θ, it follows from (4.3) that [5],

$$D = \frac{ds}{df} = R_a \cdot \frac{d\theta}{df} = \frac{1}{f_c} \cdot \frac{\tilde{N}_g}{N_{\mathrm{FPR}}} \cdot \frac{R_a \Delta L}{d_a} \tag{4.4}$$

where $f_c = c/\lambda_c$ is the center frequency, N_{FPR} is the slab mode index in the FPR, and $\tilde{N}_g$ is the group index of the waveguide mode.

It can be seen from (4.3) that the response of the phased array is periodic. After each change of 2π in $\Delta\Phi$ the field will be imaged at the same position. The period in the frequency domain is called the free spectral range (FSR). Since the value of $\Delta\Phi$ is dependent on wavelength, this means that different wavelengths will be imaged to the same output waveguide. For example, if 1550 nm light is incident on the centre output waveguide, and the FSR is 15 nm, then 1565 nm light will also be focused to this same output waveguide. In order to avoid this unwanted effect, it is necessary to design the AWG to have a FSR larger than the range of wavelengths to be demultiplexed. The FSR can be calculated as the frequency shift Δf_{FSR} for which the phase shift $\Delta\Phi$ equals 2π. Recall that

$$\Delta\Phi = \beta_a \Delta L$$

and that β_a, the propagation constant of the array waveguide mode, is defined as

$$\beta_a = \frac{2\pi f}{c} N$$

The group index $\tilde{N}$ of the array waveguide mode is,

$$\tilde{N} = N + f\frac{dN}{df}$$

The FSR requires that

$$\frac{2\pi\Delta f_{\mathrm{FSR}}}{c}\tilde{N}\Delta L = 2\pi \tag{4.5}$$

and from this we find

$$\Delta f_{\text{FSR}} = \frac{c}{\bar{N}\Delta L} \tag{4.6}$$

which represents the FSR in units of frequency.

Polarization Dispersion

It is typically desirable to fabricate photonic devices that are insensitive to polarization, since the light coupled from an optical fiber will be randomly polarized. The most simple way of achieving this condition in an AWG is by designing the array waveguides to be polarization independent. If the waveguides are birefringent, i.e. have different propagation constants, then the two polarizations will be focused to different positions on the image plane, potentially coupling the light into different output waveguides.

This polarization sensitivity can be quantified by monitoring one output waveguide while controlling the wavelength and polarization of the light at the input. The polarization dispersion resulting from a certain birefringence can be quantified by considering that two different wavelengths in vacuo will be coupled into the same receiver waveguide if the wavelengths λ_{TE} and λ_{TM} of the waveguide mode are equal [5]. Again, it is useful to work with units of frequency, since the wavelength depends on refractive index. The wavelengths can be described by their frequencies, f and $(f - \Delta f_{\text{pol}})$. Then,

$$\lambda_{\text{TM}}(f) = \lambda_{\text{TE}}(f - \Delta f_{\text{pol}}) \tag{4.7}$$

where $\lambda_{\text{TM}} = \frac{c}{f \cdot N_{\text{TM}}}$ and $\lambda_{\text{TE}} = \frac{c}{f \cdot N_{\text{TE}}}$, where $N_{\text{TM/TE}}$ are the effective refractive indices of the TM and TE waveguide modes, respectively. Therefore,

$$\frac{c}{f \cdot N_{\text{TM}}(f)} = \frac{c}{(f - \Delta f_{\text{pol}}) \cdot N_{\text{TE}}(f - \Delta f_{\text{pol}})} \tag{4.8}$$

where N_{TE} and N_{TM} are the effective indices for both polarizations, and are a function of the frequency of incident light. By solving Δf_{pol} from (4.8),

$$\Delta f_{\text{pol}} \approx f \cdot \frac{(N_{\text{TE}} - N_{\text{TM}})}{N_{\text{TE}}} \tag{4.9}$$

in which the approximation is due to the removal of the material dispersion effects on the effective indices, which are generally very small over the bandwidth of interest in an AWG.

The polarization dispersion from (4.9) is often expressed in terms of vacuum wavelength as $\Delta\lambda_{\text{pol}}$. For InGaAsP/InP DH waveguide structures $\Delta\lambda_{\text{pol}}$ is typically on the order of 4 to 5 nm [5]. This can be very problematic since it is typically greater than the channel spacing and therefore significantly affects the crosstalk. For SOI and silica-based devices the polarization dispersion is much smaller, and sometimes eliminated.

In many material systems it is very difficult to design waveguides with no birefringence. A number of techniques have been developed to compensate for the polarization dispersion in AWGs in these materials [43], [40], [44], but each suffers from complications in fabrication or limited performance. The most attractive solution is to use a material with no material birefringence and controllable waveguide birefringence. SOI is well suited for this application since it has no inherent birefringence, and the waveguide birefringence can be easily controlled by tailoring the waveguide geometry. This will be discussed further in section 4.2.2.

Crosstalk

The crosstalk in an AWG can be attributed to a number of different mechanisms. The four major sources of crosstalk will be discussed here. A more detailed discussion including the effects of multiple active inputs can be found in [45].

The most simple source of crosstalk is light that is unintentionally coupled into the slab waveguide sections between waveguides, and subsequently propagates to the device outputs. In traditional AWG designs this problem is compounded since the output waveguides are directly opposite the input waveguide, as illustrated in Fig. 4.2. In an effort to eliminate this effect, some of the AWGs for this work were designed and fabricated in a 90-degree geometry, as illustrated in Fig. 4.4. This design is similar to that used by Jalali in [46]. This design can help reduce the crosstalk due to background radiation, however it does not completely eliminate it. Some of this crosstalk is due to light that is properly coupled to the waveguides at the input, but scattered out of the waveguide mode during propagation through the device, due to bend losses or scattering at rough sidewalls [5].

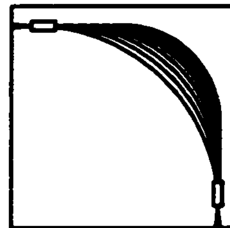


Figure 4.4: 90-degree device geometry used for some of the devices in this work.

Coupling between different output waveguides can also contribute to channel crosstalk. This coupling is due to an overlap of the exponential tails of the adjacent waveguide modes, and can be minimized by designing the AWG so that the output waveguides are adequately separated at the image plane, and quickly separated thereafter. A detailed analysis of directional coupling can be found in [37].

Another source of crosstalk is mode conversion in the array waveguides. If the array waveguides are not strictly single mode, a first-order mode can be excited and can propagate coherently through the array [5]. Since the fundamental mode and

first-order mode have different propagation constants, the images formed by these fields will occur at different locations on the image plane, and the "ghost image" may couple to an undesired receiver, thereby contributing to the channel crosstalk.

Finally, a significant amount of the device crosstalk can be due to imperfections in the fabrication process. The propagation constants of the array waveguide modes can be altered by local variations in film thickness or waveguide width, which can lead to considerable errors in the phase transfer and can thereby increase the crosstalk level. It has also been shown that the standard stepping pattern used for e-beam writing of masks, a common problem encountered when patterning curved waveguides, can contribute to this source of crosstalk [47]. It has been shown by a number of authors [48], [49] that improved crosstalk is feasible by correcting this phase error. However, because of the increased complexity in fabrication involved with this correction it is rarely used in practical devices.

Although the crosstalk in an AWG demultiplexer can be reduced by appropriate design and fabrication, the values reported for practical devices are relatively consistent, and often limited by the fabrication process. Typical values are on the order of -20 dB for InP-based devices, and better than -25 dB for silica-based devices [5]. There have not been many reports of SOI-based AWG performance in the literature, but the reports in [46] indicate performance similar to InP-based devices.

4.2.2 Design Issues Specific to SOI

In addition to the design criteria discussed above, there are a number of issues specific to SOI that need to be considered. A limited number of SOI AWGs have been reported in the literature, but there is currently a lack of theoretical discussion relating directly to these SOI devices. Because of the very large index contrast between the Si

layer and the oxide cladding, SOI waveguides present some unique challenges as well as opportunities. In this section we concentrate on the material and optical design issues pertaining to the development of practical polarization insensitive SOI AWG demultiplexers.

Waveguides fabricated in SOI will in general be multimode, and will also have an intrinsic polarization birefringence which depends on the silicon overlayer thickness. It has been shown that the polarization birefringence can be removed by an appropriate choice of the SOI ridge waveguide width to height ratio [50]. Similarly, by carefully choosing the ridge width and height, it is possible to design a ridge waveguide supporting only a single mode, which was discussed in section 2.4. The waveguides used in an AWG must be single-mode and the device must be free of birefringence. Meeting these two requirements is the fundamental challenge in designing AWG devices on SOI . Although requirements for zero birefringence and single mode operation can be met using appropriate ridge design, they cannot always be satisfied simultaneously. A ridge that supports only a single mode is not necessarily birefringence free, and a ridge that is birefringence free may support higher order modes. Furthermore, the combiner/splitter sections of an AWG demultiplexer are essentially slab waveguides and it is not possible to use ridge height and width to control waveguide properties.

Waveguide Birefringence

Waveguides were modeled using a finite-difference mode solver with semi-vectorial capability, commercially available from Apollo Photonics. Although it is relatively simple to design waveguides with zero birefringence in thick SOI layers, some of this work focused on using an SOI thickness of 1.5 μm in order to reduce device size. At these dimensions the etch depth and width must be more carefully

controlled. It was found that once a waveguide width is chosen, it is generally possible to calculate an etch depth that results in zero waveguide birefringence, and vice versa, for a waveguide with vertical sidewalls (e.g. fabricated using a reactive ion etch). This is not true for chemically-etched waveguides with sloped sidewalls. This is illustrated in Fig. 4.5, which shows the effective index difference between the TE and TM modes in an SOI ridge waveguide, for an etch depth of 0.75 μm. The waveguide birefringence is larger for a wet-etched waveguide, and not as sensitive to etch depth or ridge width. For the wet-etch, the ridge width refers to the width at the top of the waveguide, and the anisotropic etch results in a sidewall angle approximately 55° from horizontal.

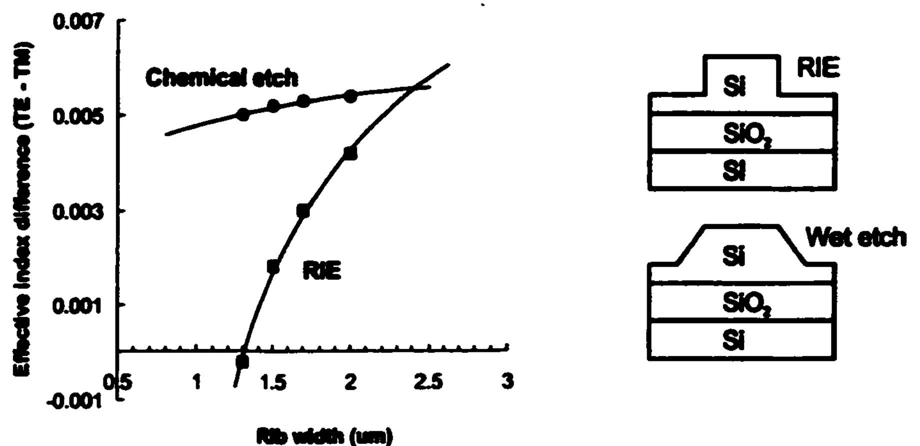


Figure 4.5: TE/TM birefringence calculated for waveguides fabricated in 1.5 μm thick SOI using an etch depth of 0.75 μm. The solid curves are provided as a guide to the eye only. The waveguide structures used for the calculations are shown on the right.

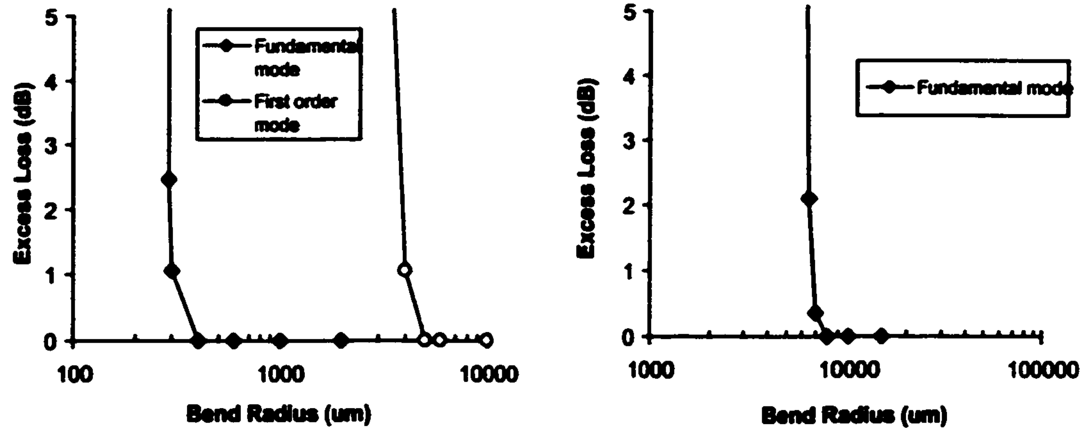
Although the waveguide dimensions shown in Fig. 4.5 predict zero waveguide birefringence they do not assure single-mode operation, which is also necessary for effective demultiplexing using an AWG. In fact, many SOI waveguides with zero birefringence are inherently multi-mode. This issue will be addressed further when discussing bend losses.

Bend Losses

The design of an AWG demultiplexer requires careful attention to waveguide bending losses. Some of this work has focused on designing AWG devices which are significantly smaller than those reported in the literature. In order to decrease device size it is necessary to design waveguides with low loss through bends of small radii of curvature. By decreasing the thickness of the SOI layer, waveguides can be designed with very small radii of curvature, at the expense of coupling losses with optical fibers. The SOI used for photonics is typically 4 to 5 μm thick, but by reducing this thickness to 1.5 μm, the minimum acceptable bend radius can be reduced by more than an order of magnitude. Fig. 4.6 illustrates the bending losses calculated for 1.5 μm and 4 μm SOI. These bending losses were calculated using an optical waveguide mode solver from Apollo Photonics. The waveguide dimensions for this plot were chosen so that the waveguides would each support two horizontal modes and one vertical mode.

The calculated bending loss versus radius of curvature demonstrated a sharp threshold. Above a certain radius of curvature effectively no loss was observed, but for tighter bends the loss increased very rapidly, effectively to extinction. It is evident from Fig. 4.6 that the use of thinner SOI significantly reduces the minimum acceptable bend radius, from 8000 μm in 4 μm SOI, to 400 μm in 1.5 μm SOI.

Also illustrated in Fig. 4.6, the threshold for bending loss is dependent on the waveguide mode. Higher-order horizontal modes leak away at larger radii of curvature, and this fact was used in our AWG design. By designing waveguides with zero birefringence we minimize the polarization sensitivity of our AWG, but typically create multi-mode guides, limiting the performance of the device. However by choosing an appropriate bend radius for the waveguides we can effectively filter out the higher order modes, leaving only the fundamental mode at the output splitter.



(a) 1.5 μm SOI, etch depth = 0.7 μm.

(b) 4.0 μm SOI, etch depth = 1.4 μm.

Figure 4.6: Bending losses in SOI.

For the waveguides represented in Fig. 4.6(a), this radius would be around 1000 μm. This modeling therefore predicts that the array waveguides *can* be made multi-mode if necessary to achieve zero birefringence.

The modeling presented thus far provides the design criteria for SOI waveguides that are birefringence free and support only a single mode at the output splitter. The birefringence from the slab waveguide section of the output combiner has a minimal effect on device crosstalk [51]. However, in addition to being birefringent, this slab waveguide will also support a high number of modes in the vertical direction. This occurs because the ridge width-to-height ratio used for obtaining single-mode waveguides in SOI is not respected in this slab waveguide section. This effect is specific to SOI and is not encountered in III-V or silica-based systems. The effect on device performance could be quite significant, however the issue has not been theoretically analyzed in the literature. An analysis of this effect is presented in the following section.

Multi-Mode Combiner and Splitter

In 1.5 μm thick SOI, the slab waveguide sections used for the combiner and splitter will support six vertical modes. Light from the single-mode input waveguide that is coupled into the slab region will in general excite all of these modes, to varying degrees. This higher mode excitation will contribute to crosstalk at the output of the AWG since each mode has a slightly different propagation constant. Modeling was performed to estimate the effects of this modal coupling on SOI AWG performance. Single-mode SOI waveguides rely on propagation in order to evolve to a single mode. The effective index method cannot be directly applied to SOI waveguides because of this fact, and because of the very large refractive index contrast between silicon and air or SiO_2. For the modeling presented here, two-dimensional mode shapes were calculated using a finite-difference optical waveguide mode solver from Apollo Photonics. An overlap integral was used to calculate the coupling from the waveguide fundamental vertical mode, to the slab waveguide modes in the combiner. This finite-difference calculation is necessary since the EIM would result in identical vertical mode shapes for the waveguide and slab sections, which is not correct since the SOI etch depth displaces the position of maximum amplitude of the waveguide mode. It was found that coupling to the fundamental vertical mode of the slab waveguide is more than two orders of magnitude higher than the coupling to higher order vertical modes. These modeling results are shown in Fig. 4.7 for an SOI thickness of 1.5 μm and a rib width of 3.0 μm.

The power coupled to all six supported vertical modes of the slab waveguide is shown in Fig. 4.7. The power coupled to the fundamental slab waveguide mode does in fact vary, since for a given ridge height the sum of the power in all modes must equal unity. However this variation is less than 1% and is therefore not visible

in Fig. 4.7. The power coupled to different modes varies with the ridge height since as the etch depth changes so does the vertical position of the maximum amplitude of the waveguide mode. This affects the coupling to higher-order slab modes since they have maxima at differing vertical locations.

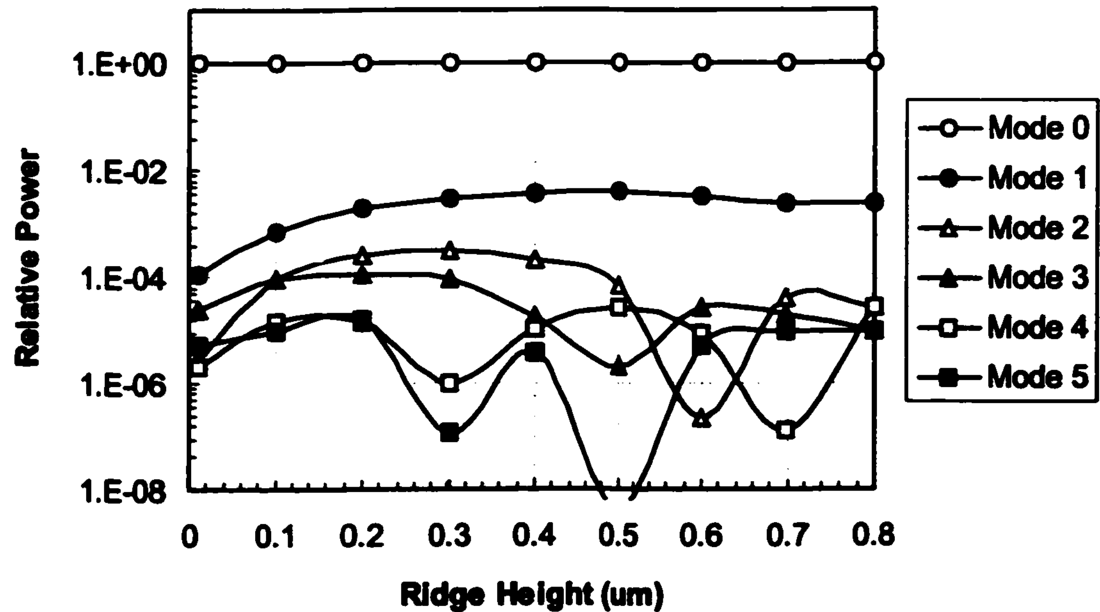


Figure 4.7: Power coupled to slab waveguide modes from a single-mode input waveguide in SOI.

Because of reversibility, the same calculations can be used to estimate coupling from the fundamental slab waveguide mode to the fundamental array waveguide mode at the input aperture. Coupling between ridge and slab waveguide modes takes place four times throughout the length of the AWG: twice for the input star coupler and twice for the output star coupler. Since the conversion efficiency is greater than 99%, the overall contribution to insertion loss is negligible. Note that it is not correct to assume that this will result in a four-fold increase in modal extinction, since, for example, the coupling of the second-order mode of the slab to the second-order mode

of the waveguide is also nearly 100%.

Mode conversion is an important factor in the performance of AWG devices in SOI. To our knowledge, calculations of the effect of mode conversion have not yet been reported in the literature, despite the fabrication of several SOI AWGs. The results shown in Fig. 4.7 show that the higher order mode excitation will have a minimal impact on AWG insertion loss and crosstalk, since the power coupled to higher order modes amounts to less than 1% of the total power. These modeling results are considered to be quite important to the literature since they constitute a theoretical limit on the crosstalk performance of SOI AWGs.

Chapter 5

SiGe Coherent Wave Photodetectors

Conventional photodiodes with high responsivity at 1.3 μm and 1.55 μm are made with III-V materials such as InGaAsP. Although these diodes provide high detection efficiency, incorporating them with mature Si technology is difficult and expensive.

The optical absorption edge of Si-based detectors can be extended further into the infrared by the use of epitaxial SiGe alloys. The absorption edge of Si limits its use as a photodetector to wavelengths shorter than 1100 nm. Pure Ge is in fact a good photodetector for wavelengths out to almost 1800 nm. Previous work has been reported on using planar epitaxial SiGe multiple quantum wells (MQWs) on Si substrates [13], [52], or Ge layers grown on relaxed Ge buffer layers [53]. These approaches demonstrate encouraging results for operation at 1.3 μm, but showed limited success in obtaining good responsivity at 1.55 μm. The main difficulty in the MQW approach is that the high lattice mismatch limits the maximum Ge concentration and SiGe layer thickness. The combination of large quantum confinement and low Ge concentration make it difficult to grow wells with an optical absorption edge suitable for detecting signals at 1.55 μm. Although pure Ge provides a suitable

absorption edge, full incorporation with Si technology may prove very challenging.

In practice, Ge concentrations well over $x = 0.5$ are required to obtain a significant photoresponse in $Si_{1-x}Ge_x$ at $\lambda = 1550$ nm, and the corresponding critical thicknesses are on the order of 10 nm or less [2]. The increasing role of quantum confinement in such thin layers tends to push the absorption edge to shorter wavelengths, thus counteracting the effect of increasing Ge concentration. This fundamentally limits the absorption edge attainable in strained QWs to wavelengths below 1.5 μm, requiring a new type of SiGe photodetector.

5.1 Coherent Wave Quantum Wells

A strained epilayer will usually relax by forming dislocations, but given suitable growth parameters SiGe epilayers can also lower strain energy by forming non-planar structures with periodic thickness variations (coherent waves), or isolated islands on a thin wetting layer (Stranski-Krastanov growth). The latter growth mode is often observed in compressively strained InGaAs alloys on GaAs, and can be used to create self-assembled quantum dot arrays. Coherent wave growth has often been considered a problem in the growth of very thin InGaAsP layers because of the non-planar structure, and because the larger elements tend to migrate to the ripple maxima where the lattice is allowed to expand. We have focused on using the unique properties of the three-dimensional growth modes in a beneficial way, to develop strained superlattices with lower energy gap than could otherwise be achieved, allowing photodetection in SiGe at $\lambda = 1.55$ μm.

The formation of the coherent wave structure is a natural strain relief mechanism. Fig. 5.1 illustrates a compressively strained SiGe layer on a Si substrate. The undulating surface allows the lattice planes in the mounds to dilate by lateral expan-

sion, which allows partial elastic strain relief within the mound. A consequence of the relaxation is that there is a complementary additional compression of the lattice planes at the thickness minima, however this compression is very localized so that the volume of material subjected to additional stress is much less than the volume experiencing partial stress relief [6].

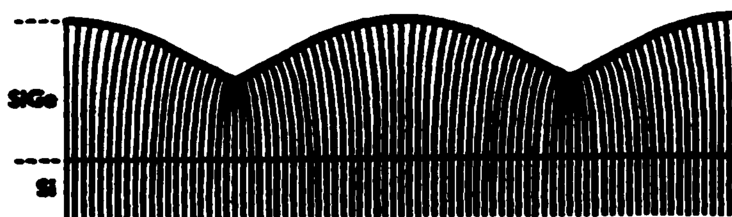


Figure 5.1: Elastic distortion of vertical lattice planes in a coherent wave QW. Adapted from [6]

This structure benefits photodetector response in a number of ways. During the formation of these coherent wave QWs, it is believed that Ge tends to migrate towards the thickness maxima due to its larger unit-cell size and the stress gradients that promote mass transport away from the thickness minima [54]. This migration increases the local Ge concentration in the mounds, helping to push the absorption edge to longer wavelengths. Furthermore, the undulating structure reduces the quantum confinement at the peaks because of the larger thickness. This again lowers the energy gap and pushes the optical absorption edge to longer wavelengths. Finally, the coherent wave growth lowers the strain energy in the material, and it is therefore possible to deposit more Ge. The results of this coherent wave growth are illustrated in Fig. 5.2, which shows the absorption edge versus Ge concentration when the SiGe film is grown to the critical thickness. The flat quantum well response is limited by the quantum confinement at high Ge concentrations, which begins to counteract the effect of more Ge. Coherent wave growth reduces the quantum confinement in the

mounds, and therefore produces QWs with significantly lower band gaps compared to planar QWs with the same nominal composition. This effect has been theoretically calculated and plotted in [7] and [8], and Fig. 5.2 illustrates the results of these calculations.

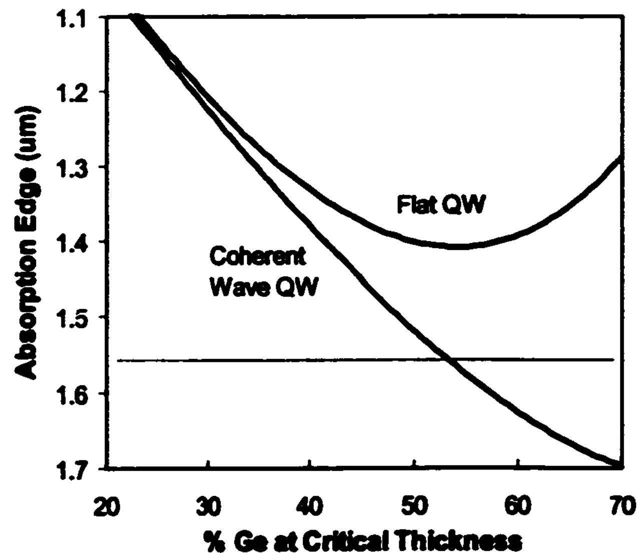


Figure 5.2: Illustration of the effects of quantum confinement on the absorption edge of flat $Si_{1-x}Ge_x$ QWs, and the benefit derived from coherent wave growth. Based on results published in [7] and [8].

Coherent wave growth will occur naturally for certain epilayer thicknesses and Ge contents, and no modification of the growth conditions are necessary. Predictions for surface wave generation can be found in [9], [55], and [6], and are based on growth kinetics and energetics. At low epilayer thicknesses, coherent wave growth offers a competing mechanism for strain relaxation in place of misfit dislocations, and the formation of the coherent wave structure is a mechanism through which the strain energy and surface energy are minimized. A flat layer might be expected to represent the minimum surface energy condition, since when a surface wave is created the area

of the surface increases. The larger the ripple, the larger the surface area and energy. Therefore this factor inhibits surface wave generation until the free-energy reduction in the system by stress relief outweighs the free-energy increase due to surface-area increase.

The conditions required for coherent wave growth have been experimentally verified and compared to theory in [10]. The results are presented in Fig. 5.3, and show the thickness/composition ranges that result in coherent wave growth. The photodetectors designed for this work are based on a superlattice with nominal Ge content of 50%, and nominal well thickness of 5 nm.

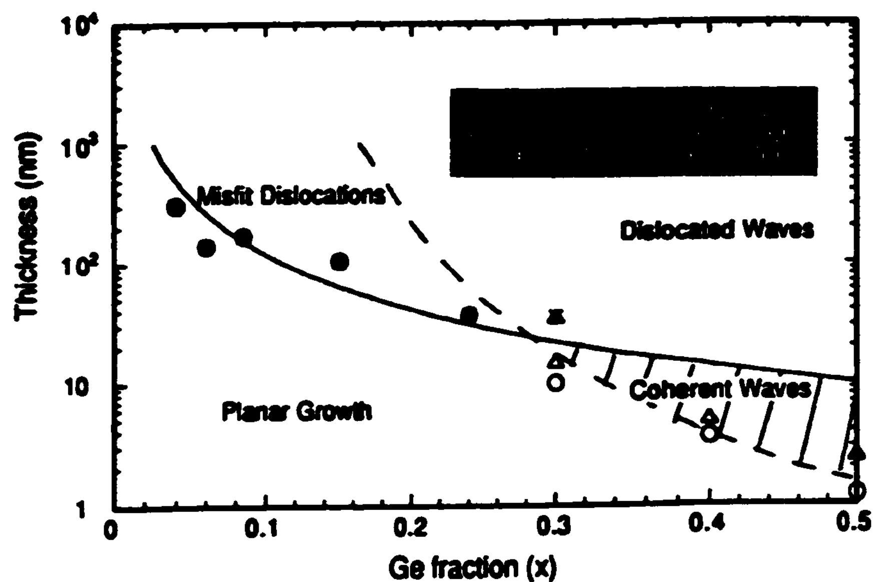


Figure 5.3: Conditions necessary for coherent wave growth of $Si_{1-x}Ge_x$. The solid line represents the Matthews-Blakeslee critical thickness. The dashed line represents the theory governing surface wave formation presented in [9]. Coherent wave growth is expected in the hatched region. Adapted from [10].

The materials research concerning coherent wave growth of SiGe has been reported in the literature, and is generally focused on improving the performance of

SiGe electronic devices. The use of coherent wave growth for the fabrication of SiGe photodetectors has not yet been reported by other authors. In this work, we exploit the coherent wave growth mode to fabricate SiGe waveguide photodetectors with a band gap suitable for operation at 1.3 and 1.55 μm on SOI substrates.

5.2 MSM Waveguide Photodetectors

Although the absorption edge of a SiGe quantum well can be extended to telecommunications wavelengths, the lowest lying transitions are still indirect. As a result, the carrier generation efficiency remains low relative to direct gap materials. Surface-illuminated detectors are not suitable because the total active layer thickness is limited by the critical thickness of the SiGe. To improve overall sensitivity it is necessary to fabricate detectors in a waveguide geometry to provide a long optical path over which most of the light can be absorbed. SOI offers a substrate suitable for the growth of SiGe, and can therefore be used for the monolithic integration of waveguides, photodetectors, and microelectronics.

The photodetectors designed for this work are based on a Si/SiGe superlattice grown on an SOI substrate, as illustrated in Fig. 5.4. The SOI structure provides the optical confinement for the input light, and the MSM detector length is tailored to absorb the incoming light. This thesis will demonstrate the monolithic integration of this waveguide/detector structure. Replacing the straight input waveguide with an output waveguide from an AWG would not affect the device performance and would be a simple extension of the technology.

The light coupled from the input fiber to the SOI waveguide travels to the detector region with very low loss. The Si/SiGe superlattice has a higher refractive index than the SOI waveguide due to the high Ge content of the detector structure.

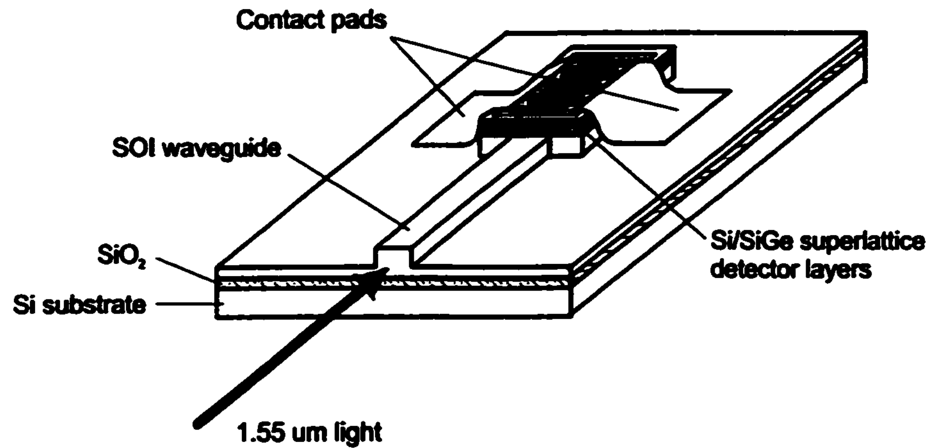


Figure 5.4: SOI waveguide photodetector structure.

Therefore, the light passing beneath the detector layer is coupled up into the SiGe and is absorbed down the length of the detection region. This is illustrated in Fig. 5.5, which also shows how Si electronic amplifier circuitry could be integrated onto the same chip.

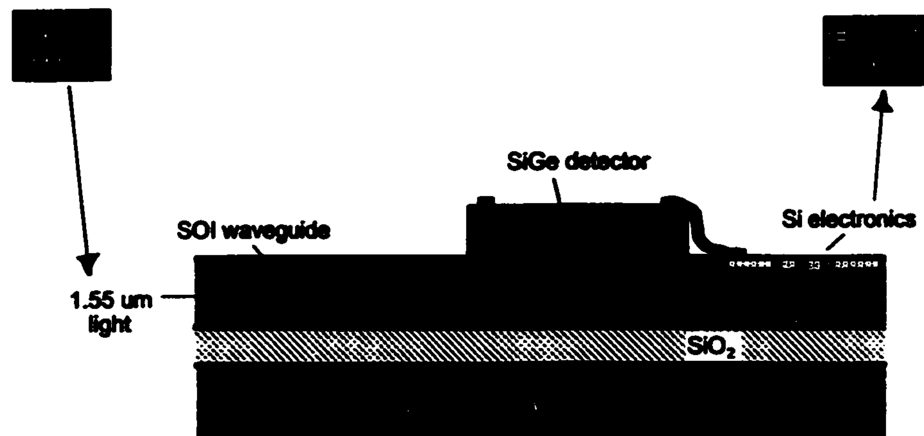


Figure 5.5: Cross-sectional view of the SOI waveguide photodetector structure. The device layers are not drawn to scale.

The monolithic integration of Si-based waveguides and photodetectors represents a significant step towards inexpensive optical components. The use of three-

dimensional growth morphologies for the fabrication of SiGe photodetectors with response at 1.55 μm wavelengths has not been reported in the literature by any other authors to date. This technique could overcome the limitations inherent to traditional SiGe MQW detectors.

Chapter 6

Experimental Results

This chapter presents the experimental results for all aspects of this work. This includes LOCOS results for both SiGe and SOI, the experimental performance of 1.3/1.55 μm duplexers in SiGe, AWG demultiplexers in SOI , and advanced SiGe photodetectors. The monolithic integration of SOI waveguides and SiGe photodetectors will also be discussed.

6.1 LOCOS Optical Waveguides

The use of the optimization techniques discussed in Chap. 3 was found to help minimize the dislocations induced during LOCOS processing of SiGe waveguides. It will be shown that the LOCOS processing of SiGe waveguides is often not possible without the techniques discussed in Chap. 3, and duplexer devices were successfully fabricated using this technique. However the commercial viability of the SiGe LOCOS process is questionable due to the minimum dislocation densities achievable, which are only marginally acceptable for electronic device integration. The LOCOS process for fabricating waveguides in SOI was very successful, and presents significant opportunities for commercial application.

6.1.1 SiGe LOCOS Waveguides

The SiGe wafers used in this study were purchased from Lawrence Semiconductor Research Laboratory Inc., and from the National Research Council of Canada, and in both cases were grown by UHV-CVD. The specifications of each wafer are shown in Table 6.1.

Table 6.1: Wafer structures for samples used in this work, as determined using x-ray rocking curves and SEM.

Wafer no.	Si cladding layer thickness (μm)	SiGe layer thickness (μm)	SiGe layer Ge content (%)
1	0.85	0.85	1.8
2	0.85	0.85	2.7
3	1.5	0.75	6.0
4	0.6	0.75	6.0

The SiO_2/Si_3N_4 masking layers were deposited at McMaster through collabo-

ration with S. Wallace and Dr. P. Mascher. The films were deposited by ECR-PECVD in a mixed plasma of argon, silane and nitrogen/oxygen. Depositions were performed at 2.3 mTorr and 120°C using 400 W of microwave power. Typical depositions began with an SiO_2 layer of 30 nm. Prior to the Si_3N_4 layer deposition, the chamber was cleaned using a high power argon plasma to remove oxygen from the chamber. Residual oxygen was determined to contaminate subsequent layers by incorporation into the Si_3N_4. This significantly reduced the effectiveness of the nitride layer as a mask to oxidation. Following the argon purge a Si_3N_4 layer was deposited to a typical thickness of 200 nm.

Waveguide channels were patterned in the Si_3N_4 using standard photolithography in a cleanroom environment. The masking layers were etched to the silicon cap using a CF_4/O_2 plasma etch. Oxidation was performed in a laboratory furnace using a wet oxygen environment, and samples were inserted and removed while the furnace was at the desired processing temperature. Samples were typically about 1 cm^2 in size, and depending on experiment were either unmasked, fully coated with the masking layer, or patterned with optical waveguides as detailed above. After removal from the oxidizing furnace the masking layers were removed using a chemical etch, and the samples were thinned and cleaved if required for optical waveguiding.

It was found that dislocation density was indeed minimized by increasing the oxidation temperature and thereby decreasing the oxidation time. Fig. 6.1 compares the x-ray rocking curves for SiGe samples that were oxidized to obtain a SiO_2 layer of 0.6 μm thickness, but using different temperatures and times. This shows that both samples partially relaxed through dislocations, but those processed at 1050°C survived with a lower dislocation density than those processed at 900°C (indicated by the extent of the peak broadening). We found that a high quality Si_3N_4 mask

layer is essential for these long processing times. The x-ray rocking curves were obtained using a Bede QC-1 system. The dislocation density was calculated based on the spreading of the SiGe x-ray diffraction peak, and verified using a Normarski microscope after a strain-selective Schimmel etch [34]. The dislocation density in wafers processed at 1050°C was roughly an order of magnitude lower than in wafers processed at 900°C, approximately 10^5 cm^{-2} versus 10^6 cm^{-2}. The broadening $\Delta\theta$ of the SiGe peak half-widths were measured to be 114 arcsec and 29 arcsec for the samples processed at 900°C and 1050°C , respectively. The uncertainty in the half-width values is estimated at ±3 arcsec. The dislocation density can be calculated by converting to radians and using Eq. (2.28). This dislocation density is still quite high, but can be further reduced by the compensating mask layer design.

It was found that the use of the stress in the masking layer to compensate the stress in the SiGe layer during processing can in fact have a very significant effect on the material properties. X-ray rocking curve analysis was performed in order to experimentally verify the viability of reducing the SiGe stress by using compensating mask layers. Examples of these data are shown in Fig. 6.2. In this case, a $Si_{.97}Ge_{.03}$ wafer is measured in its as-grown state, followed by a measurement with a compensating masking layer applied, and finally after removal of the masking layer. No oxidation is performed in this experiment. It is intended only to show that the mask layer does indeed have an effect on the stress in the underlying SiGe layer, and that the deformation is elastic. The data illustrated in Fig. 6.2 show that the stress in the SiGe layer is reduced by the SiO_2/Si_3N_4 film, and that it is fully returned to normal after the removal of this masking layer.

In order to verify that the stress compensating effect can be used to improve LOCOS processing of SiGe wafers, two samples from the same $Si_{.97}Ge_{.03}$ wafer were

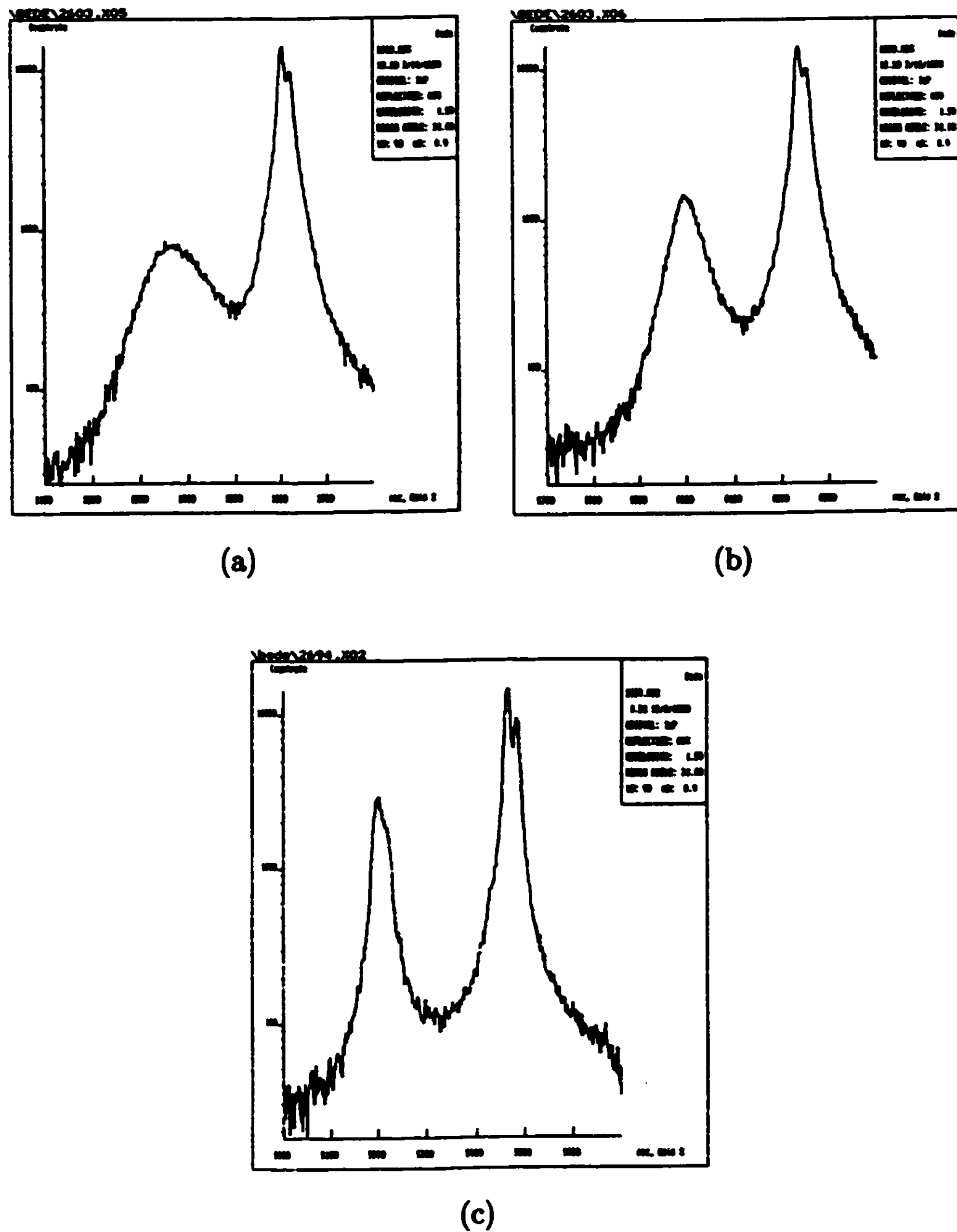
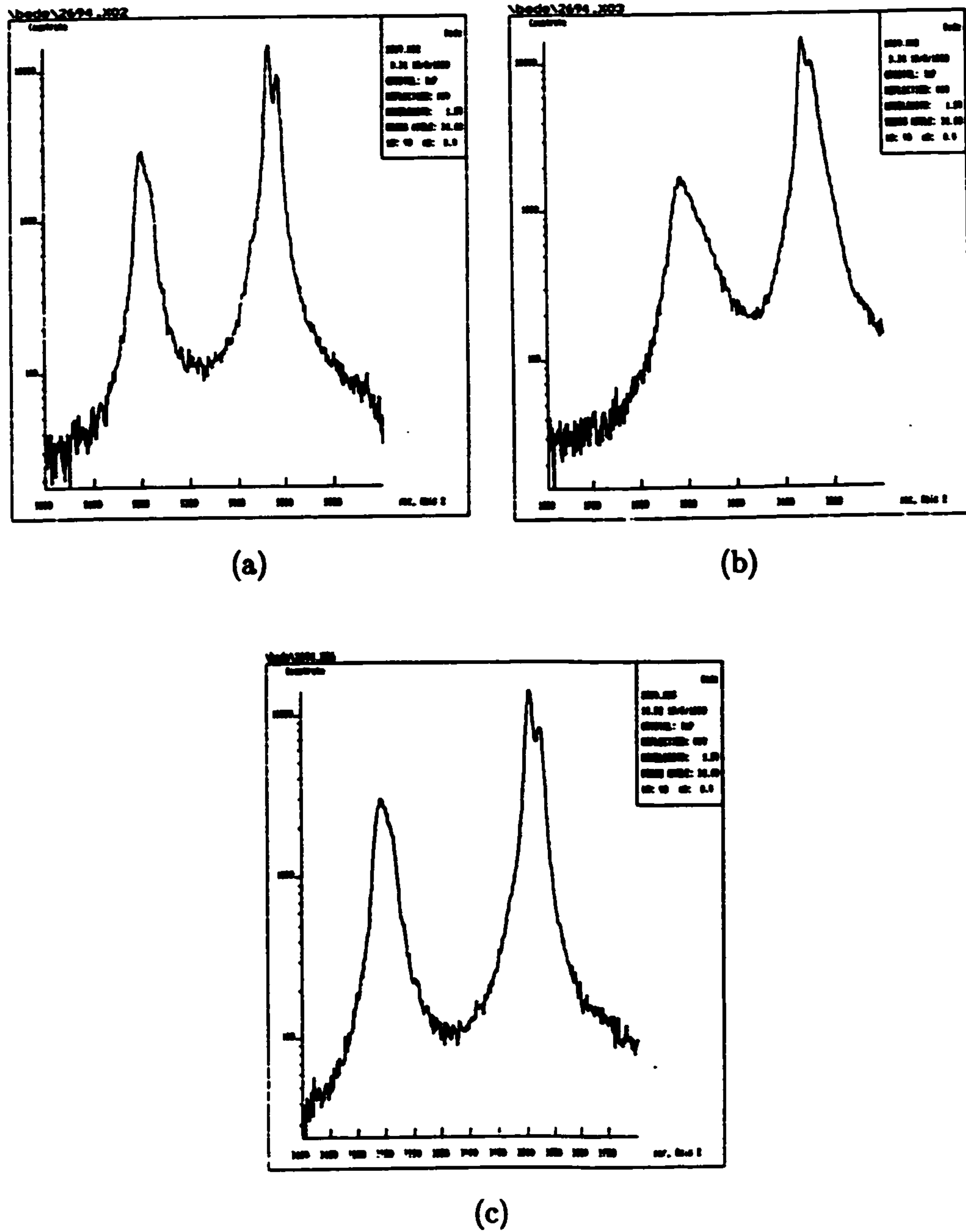


Figure 6.1: X-ray rocking curves of a $Si_{.97}Ge_{.03}$ sample after an oxide growth of 0.6 μm. (a) Processed at 900°C for 3.9 hours, (b) processed at 1050°C for 1.0 hours. The as-grown curve is shown in (c).



(a) (b)

(c)

Figure 6.2: X-ray rocking curves of a $Si_{.97}Ge_{.03}$ sample. (a) As grown, (b) with a strain-compensating mask layer deposited on the surface, and (c) after removal of the masking layer. The strain in the SiGe layer is reduced by the masking layers.

oxidized, one with no masking layer deposited, and the other with a SiO_2/Si_3N_4 layer of 30 nm SiO_2 and 180 nm Si_3N_4. After oxidation at 1050°C for one hour, the samples were removed from the furnace, the mask layer and thermal oxide were removed, and rocking x-ray measurements were performed. This data is illustrated in Fig. 6.3.

As shown in Fig. 6.3, the unmasked sample relaxed more than the masked sample during oxidation. Since much of this relaxation is due to dislocation formation, the use of a strain compensating mask can be used to help minimize the optical losses due to dislocations in SiGe LOCOS waveguides. The broadening of the SiGe peak half-widths were measured to be 44 arcsec and 109 arcsec for the samples with and without a masking layer, respectively. This corresponds to roughly an order of magnitude difference in the induced dislocation density.

It should be noted that when fabricating ridge waveguides this strain compensating mask is removed everywhere except where we intend to create the waveguides. This means that the unmasked areas between waveguides will not benefit from this technique. However, the light is confined in the area under the ridge and only a small percentage appears in the evanescent wave traveling in the unmasked area, so the technique is effective at minimizing the optical losses introduced during LOCOS processing.

We were successful in processing optical waveguides with rib heights of more than 0.5 μm, larger than previously possible, and large enough to provide good optical confinement when close to the waveguide core. Our samples from wafer no. 4 originally had a cladding thickness of 0.6 μm, leaving 0.1 μm of Si above the SiGe layer in the unmasked areas after oxidation. Fig. 6.4 shows SEM photos of a SiGe waveguide fabricated using this LOCOS processing. The "bird's beak" structure typical of the process is clearly visible. We believe this was the first reported success of utilizing

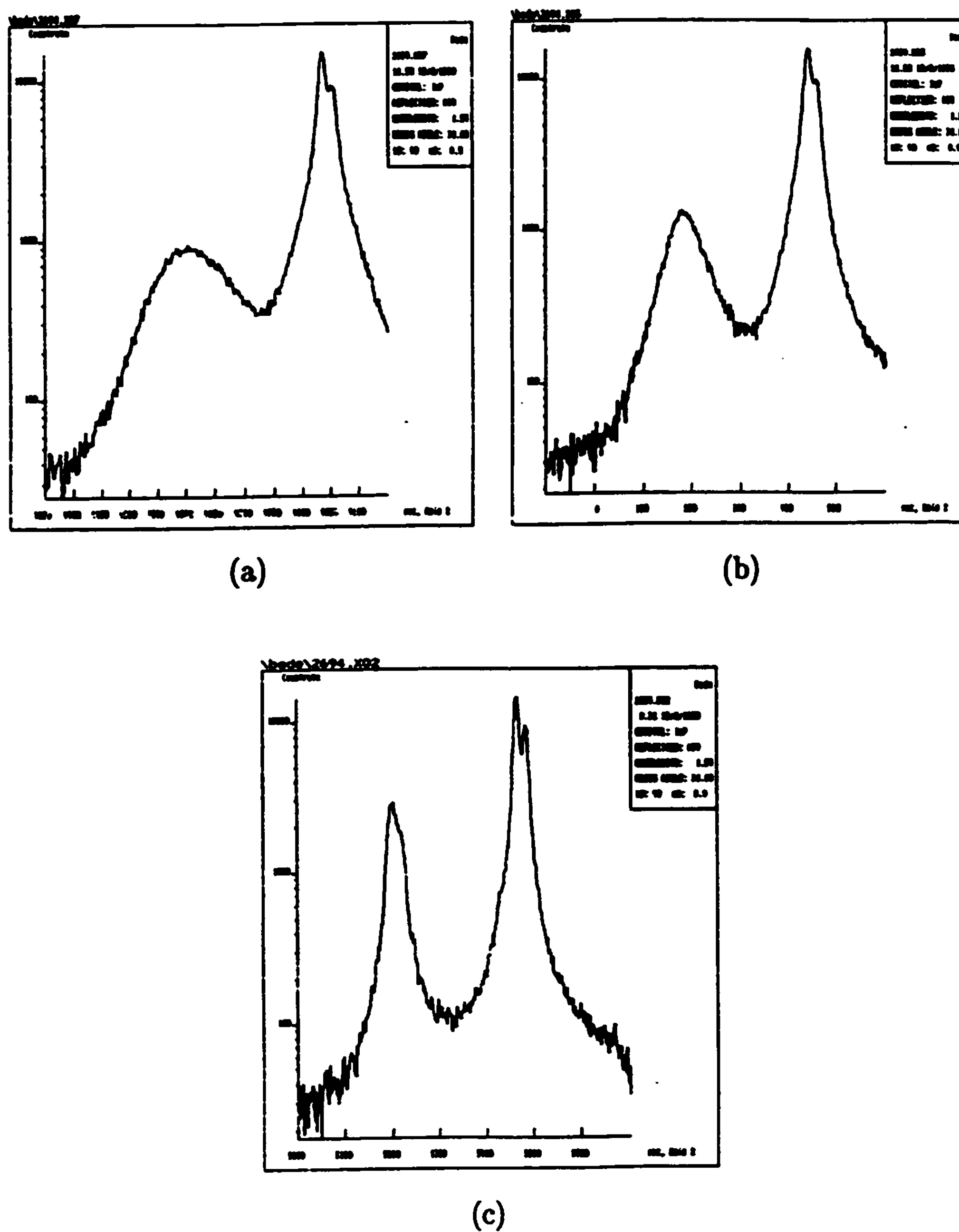


Figure 6.3: X-ray rocking curves of a $Si_{.97}Ge_{.03}$ sample oxidized at 1050°C for one hour. (a) Without any masking layer deposited. (b) With a SiO_2/Si_3N_4 masking layer of 30 nm SiO_2 and 180 nm Si_3N_4. The as-grown curve is shown in (c).

VLSI-compatible processes for making SiGe optical waveguides.

(a) (b)

Figure 6.4: LOCOS optical waveguides in SiGe. (a) The structure after several hours in an oxidizing furnace, showing the masking layer and the field oxide. (b) The structure after removal of the SiO_2/Si_3N_4 mask and the thermal oxide.

Optical loss measurements were performed using a Fabry-Perot technique [56] with a tunable diode laser centered around 1550 nm. Cleaved optical fibers were used for input coupling to the optical waveguides, and the light exiting the output facet was focused onto a calibrated Ge detector. The LOCOS waveguides processed at 1050°C with a strain compensating mask were measured to have a loss of 4.5 ± 0.5 dB/cm. Similar waveguides processed using a chemical etch exhibit loss of roughly 3.5 ± 0.5 dB/cm.

Waveguides processed without the techniques described above had higher losses that were often unsuitable for photonic devices and electronics. For example, these values were approximately 7 dB/cm in wafer no. 3 processed at 800°C. This emphasizes the fact that without utilizing the processing conditions prescribed by this work, functional devices with acceptable optical losses could not have been fabricated using LOCOS processing.

The SiGe LOCOS waveguide results presented here were the first reported success for this processing technology, and represent a step towards inexpensive optoelectronic components. However, in spite of our modest successes in reducing dislocation density, the SiGe material system is still not well suited to high temperature processing. The very minimum dislocation density achievable in SiGe LOCOS waveguides was found to be 10^4-10^5 cm^{-2}, which is acceptable for some optical applications but significantly limits the potential for on-chip electronics. In contrast, the silicon-on-insulator material system is ideally suited for this type of high temperature processing, and presents enormous potential for this area of optoelectronics.

6.1.2 SOI LOCOS Waveguides

Our work with the SiGe material system eventually led to our adoption of SOI. With SOI we were able to demonstrate the potential for the LOCOS process without the limitations imposed by SiGe. This SOI LOCOS work has prompted McMaster to seek a patent on the process in light of its potential for commercial applications [32].

The elimination of a strained epilayer means that the SOI wafer can withstand extended periods of time at high temperatures. The maximum achievable rib height is limited only by the self-limiting LOCOS process, which results in feature heights approaching 2 μm. This is in contrast to our results in SiGe where the dislocation formation restricted rib heights to less than 0.6 μm. Fig. 6.5 shows a LOCOS waveguide fabricated with a rib height of 1.2 μm, which provides good optical confinement in 2.1 μm thick SOI. The thermal oxide has been removed from the surface of this sample.

A number of different mask layers were investigated as replacements for the

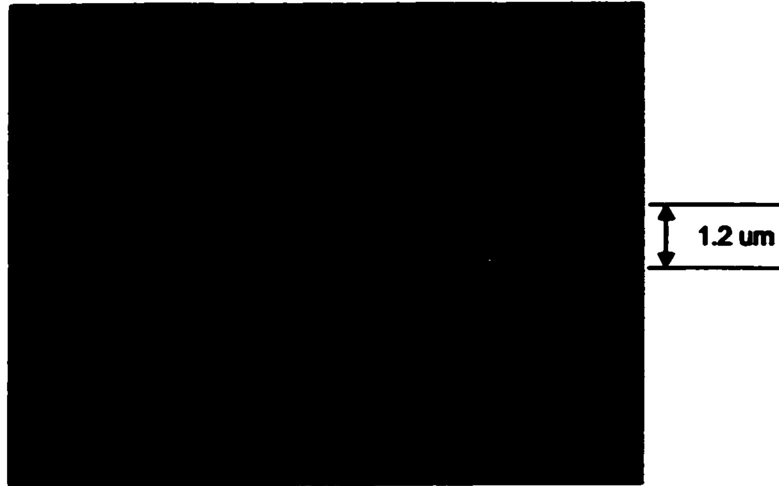


Figure 6.5: SEM image of a LOCOS waveguide fabricated in SOI. The sample was oxidized at 1100°C for 12 h with a SiO_2/Si_3N_4 mask.

SiO_2/Si_3N_4 mask, which requires a CVD deposition, but none performed as well as the SiO_2/Si_3N_4. A number of different metals were deposited and patterned, but none was successful. Aluminum, nickel, and chromium all failed because of the large stress during temperature cycling, and peeled away from the sample at high temperatures. Titanium was the only metal to survive the high temperatures intact, but the metal was rapidly oxidized to form titanium oxide which was ineffective at blocking the oxidation of the underlying silicon. A thick thermal oxide of about 2 μm was grown and patterned, and this successfully slowed the oxidation rate in the masked areas. This solution suffers from the fact that the oxide only slows further oxidation and does not inhibit it like Si_3N_4. This exaggerates the bird's beak effect and results in very shallow sloped sidewalls, which did not provide good lateral confinement for a waveguide mode.

LOCOS processing was used to fabricate both 1.3/1.55 μm duplexers and AWGs. The experimental results for these devices will be discussed further in the following section.

6.2 Passive WDM Components

Passive devices were fabricated using both conventional etches and LOCOS processing. The experimental results will be discussed here, with emphasis on the arrayed waveguide grating demultiplexers.

6.2.1 1.3/1.55 μm Duplexers

These devices were fabricated in SiGe in order to demonstrate our early development of the LOCOS process, and to determine the limitations inherent to SiGe optical waveguides. By taking advantage of the results discussed above, integrated optic duplexers were fabricated in $Si_{.94}Ge_{.06}$ using LOCOS processing. The samples were prepared as discussed in section 6.1. Annealing was performed in a wet oxygen environment for 3.1 hours at 1050°C, resulting in a rib height of 0.55 μm.

It was found that the partial relaxation of the SiGe layer does indeed have an effect on device performance. This relaxation modifies the original refractive index of the waveguide layers, and must be considered when designing photonic devices for LOCOS processing. Since the strain-induced birefringence is significantly reduced after LOCOS processing, polarization insensitive devices may be possible but the post-processing refractive index must be used during device design. This work was intended primarily to demonstrate the LOCOS waveguide technology, and did not concentrate on maximizing this device performance.

Duplexers were fabricated and were successfully used to demultiplex 1.3 and 1.55 μm wavelengths. Wavelength isolation was measured by using an infrared camera to obtain an intensity trace across the output facet, an example of which is shown in Fig. 6.6. The isolation in these preliminary devices was measured to be roughly 10 dB and 8 dB in the 1.3 and 1.55 μm channels respectively. This performance is

not acceptable for most telecom applications, however similar devices were fabricated using chemical etching and exhibited isolation of -19 dB and -15 dB, showing that the change in refractive index due to LOCOS processing can be significant. This device was not intended to exhibit commercial performance, and was deemed sufficient as a preliminary demonstration of the LOCOS technology.

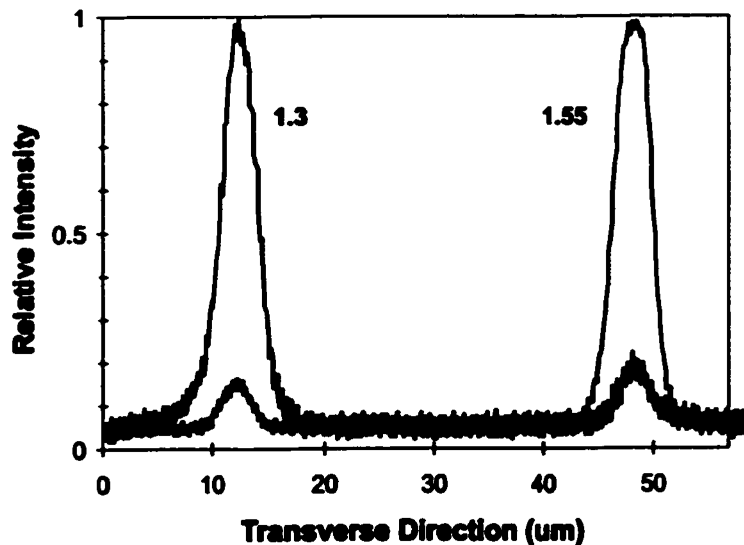


Figure 6.6: Infrared camera traces of 1.3/1.55 μm demultiplexer output using TM polarized light. This device was fabricated using LOCOS processing. The channel wavelengths (in μm) are indicated in bold.

This performance is currently limited primarily by the device design, and not the LOCOS process itself. We expect that the performance can be significantly improved in future devices by incorporating a more complex design based on the modified refractive index values, and with the addition of electrodes to fine tune the wavelength selectivity through plasma dispersion.

6.2.2 Arrayed Waveguide Grating Demultiplexers

A number of AWGs were fabricated for this work in order to characterize the device and material properties. Two different masks were designed, three different SOI thicknesses were investigated, and three different processing techniques were utilized.

First Generation Devices

The first AWGs fabricated for this work were designed for thin SOI of 1.5 and 2.0 μm thickness, since one focus of this design was a significant reduction in device size relative to earlier reported results. The devices in [50] are 2.7×2.7 cm, and those shown in [57] are over 5 cm in length. With the use of the modeling results discussed in Chap. 4 we were able to reduce this device size to roughly 5×5 mm, albeit at the expense of higher insertion loss.

The device shown in Fig. 6.7 and other similar devices were fabricated with a nominal center wavelength of 1550 nm. Each device had an array consisting of 100 waveguides with a length increment between adjacent waveguides of 22.7 μm, which by Eq. (4.2) corresponds to a grating order of 50. The fabricated devices were made with 8 channels. The output channel waveguides were separated by 8.8 μm at the combiner focus, to give a 200 GHz (1.6 nm) channel spacing. This was calculated using Eq. (4.4), with R_a=1500 μm and d_a=4 μm. BPM simulations indicated that the demultiplexer design would work equally well as a 16 channel, 100 GHz spacing device simply by halving the output waveguide separation. The mask had devices with ridge widths of 2.0, 1.7, 1.5, and 1.3 μm, and a combiner focal length of 1500 μm. At the start and end of the waveguide array section the waveguide spacing was 4 μm. At the splitter/array junction the array waveguide width was tapered out to 3 μm

to maximize optical coupling from the splitter to the array waveguides. Overall chip size for these devices was approximately 5×5 mm.

Devices were fabricated using a reactive ion etch with a CF_4/O_2 mixture. A second set of devices was fabricated using a chemical etch in potassium-hydroxide at 70°C. Chemical etching was found to be of limited use because of the high degree of undercutting encountered around waveguide bends. The devices were thinned and cleaved to produce input and output facets. Coupling was performed using a polarization-maintaining tapered fiber at the input and output waveguides. A Photonetics tunable diode laser was used for the input light source, and the intensity at the output was measured using a calibrated Ge detector.

A number of problems were encountered with our first generation devices, including high optical losses and birefringence. A certain amount of sidewall roughness is unavoidable when using RIE. In our devices this roughness was of the order of 40 nm in size. As has been reported in previous work [58], this sidewall roughness can cause very high losses in small cross section SOI waveguides due to the high refractive index contrast. This was compounded by the difficulty in coupling light into the small waveguide. The device loss, not including waveguide loss, is due mainly to light scattered at the splitter/array interface and diffraction into higher orders. This was measured to be 4.5 ± 1 dB in both the RIE and wet-etched samples, measured relative to a single test waveguide of identical input waveguide dimensions, bend radius, and device length, which was included in the mask layout. However the total insertion loss, including fiber coupling and on-chip loss, was between 15 and 20 dB, which is not acceptable for a commercial device. Commercially available AWGs typically have an insertion loss of around 6 to 7 dB.

All output spectra shown in this thesis are plotted with the maximum through-

put corresponding to 0 dB, which helps to clearly demonstrate the crosstalk level. An insertion loss for the device is provided in the text. This presentation is typical, although some authors prefer to calibrate the spectra to include insertion loss by shifting the spectrum down from 0 dB. The output spectrum for a chemically-etched device is shown in Fig. 6.8. These demultiplexers exhibited non-adjacent channel crosstalk of -20 dB, but the adjacent channel crosstalk was typically -15 dB, limiting device performance. The exact channel response was not consistent across the outputs, and was very dependent on the fabrication quality of each output. The channel spacing was measured to be 200 GHz (1.6 nm), as designed, and the free spectral range was measured to be 29 nm. The RIE samples exhibited similar performance.

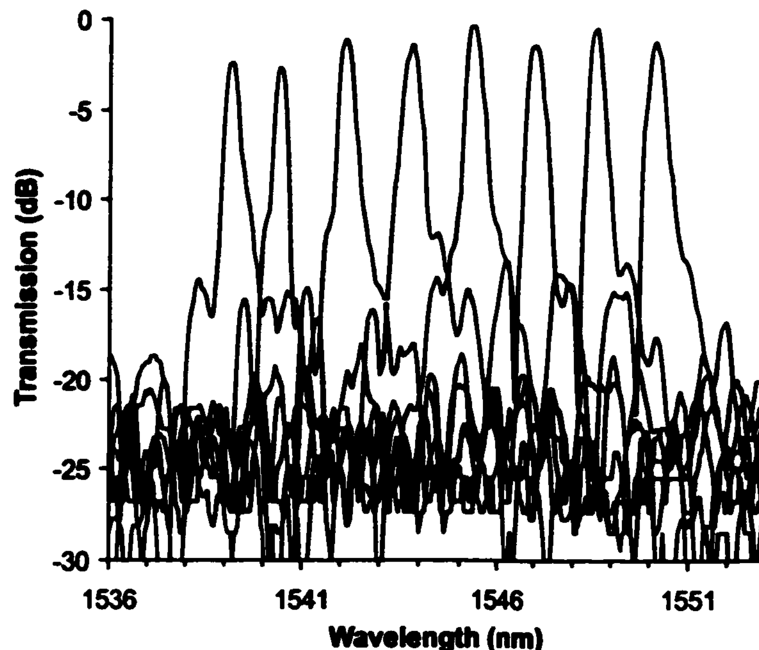


Figure 6.8: Measured output spectrum for an SOI AWG. This is a first generation device in 2.1 μm SOI with rib width of 1.7 μm, chemically etched to a depth of 1.1 μm. The light is TM polarized.

The polarization dispersion in the AWG devices was measured for both the

RIE and wet-etched samples. As predicted in section 4.2.2, the polarization dispersion varied more dramatically with ridge width in the RIE devices than in the wet-etched samples. These results are shown in Fig. 6.9 for devices with a 0.75 μm etch depth.

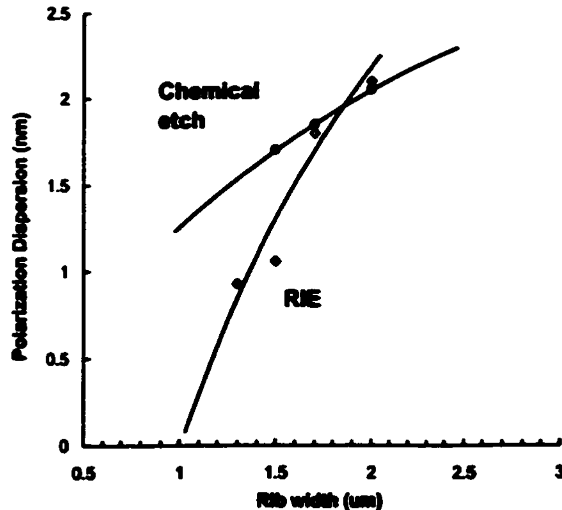


Figure 6.9: Measured polarization dispersion in first generation SOI AWG demultiplexers fabricated in 1.5 μm SOI. The experimental uncertainty in these measurements is ± 0.1 nm. The solid curves are provided as a guide to the eye only.

The results shown in Fig. 6.9 are qualitatively similar to the calculated waveguide birefringence shown in Fig. 4.5. However, in the experimental results the polarization dispersion was never found to be zero, even for ridge widths of 1.3 μm, which is where modeling predicted zero waveguide birefringence for the RIE devices. This is attributed to the very high sensitivity of the waveguide characteristics, for a small cross section SOI waveguide, to the waveguide dimensions. With this sensitivity it is difficult to achieve the necessary tolerances with the fabrication facilities available. However, the trends shown in Fig. 6.9 qualitatively support our earlier modeling.

The polarization dispersion in one channel of a first generation AWG is shown in Fig. 6.10, and will be compared with the second generation devices below. The measured dispersion is 1.8 nm. In light of the fact that the AWG is designed for a

1.6 nm channel spacing, it is easy to see that the polarization dispersion can have a significant impact on the device crosstalk. Since light exiting a fiber is typically randomly polarized, this makes the device very unsuitable for commercial application. The second generation devices do not suffer from this dispersion.

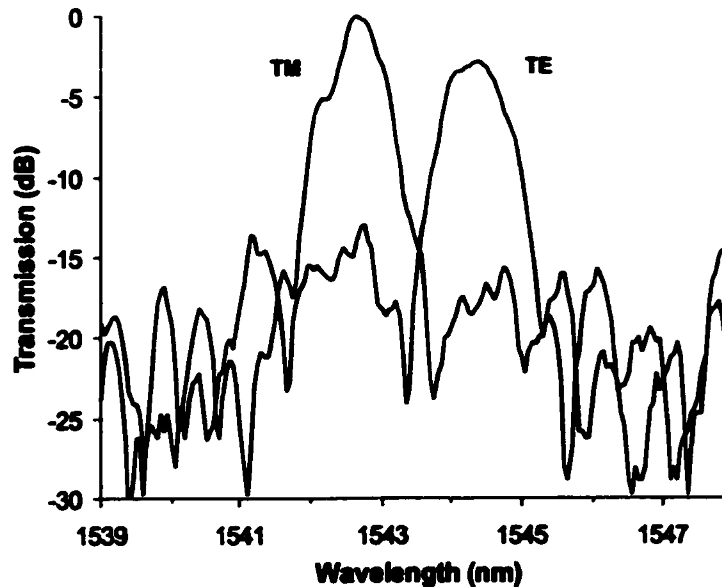


Figure 6.10: Measured polarization dispersion in the center channel of a first generation SOI AWG demultiplexer fabricated in 1.5 μm SOI.

The SOI LOCOS process was used to fabricate AWGs in 2.1 μm SOI. The same device mask was used for all the first generation devices. The LOCOS processing was done using a SiO_2/Si_3N_4 mask layer, and the samples were oxidized for 14 h at 1050°C, resulting in a rib height of approximately 1.0 μm. It was found that the SiO_2/Si_3N_4 layers were sometimes not suitable for processing at 1200°C, since the stress in the films is so dependent on deposition conditions and at times the SiO_2/Si_3N_4 mask was found to lift off during processing at 1200°C.

The output spectrum for a LOCOS device is shown in Fig. 6.11, and exhibits

crosstalk values of -13 to -15 dB. The higher crosstalk compared to conventially etched devices is likely due to the sidewalls of the LOCOS waveguides. Although the angle of the sidewalls are similar to chemically etched sidewalls, it was found that the rounded shape of the LOCOS waveguides results in slightly less confinement around waveguide bends. Light that is lost in these bends will couple to the slab waveguide regions and propagate to the output side of the device, thereby increasing the crosstalk. This conclusion is supported by the output spectrum of the LOCOS device which shows a crosstalk "floor" at approximately -15 dB. This can be compared to the chemically etched device output spectrum shown in Fig. 6.8 which exhibits a crosstalk floor at approximately -20 dB. LOCOS waveguides with greater optical confinement can be fabricated by increasing the rib height, however this can result in multi-mode waveguides. Therefore LOCOS devices should ideally be designed with slightly larger bend radii than conventionally etched devices.

The SOI LOCOS process was found to be suitable for commercial applications, although a more thorough characterization of the waveguide properties is required. The results from the LOCOS AWG shown above suggest that with appropriate design, the LOCOS process can produce devices with performance comparable to RIE and chemically etched devices. This device demonstrates the potential of the SOI LOCOS process for fabricating complex photonic components at low cost, using standard Si processing techniques that are common to almost all microelectronics fabs.

The first generation devices were successful at demultiplexing and were more than five times smaller than previously reported devices, but the high insertion losses and polarization dispersion made the devices unsuitable for commercial application or the monolithic integration proposed in this thesis. The second generation devices were designed to overcome these problems.

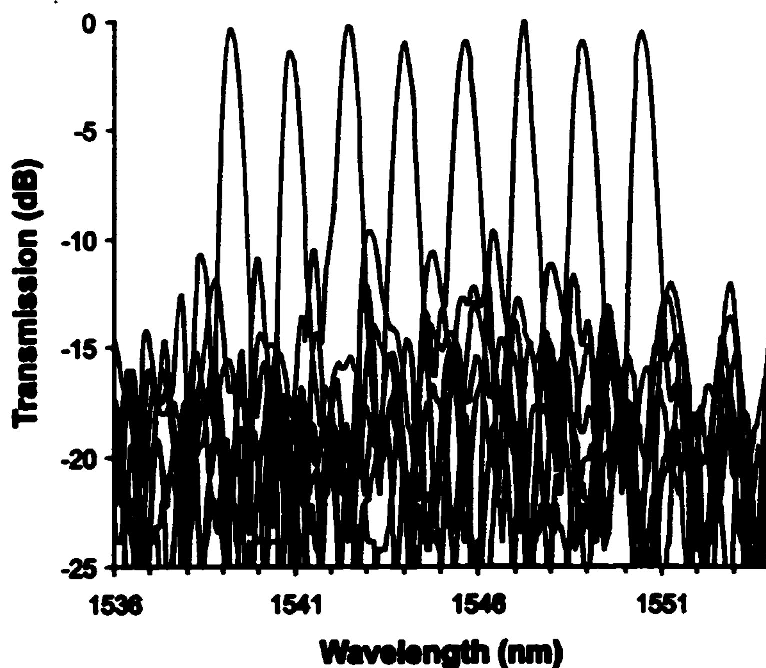


Figure 6.11: Measured output spectrum for an SOI AWG fabricated using the LOCOS process. This is a first generation device in 2.1 μm SOI with rib width of 1.7 μm, and rib height of 1.0 μm. The light is TM polarized.

Second Generation Devices

Our second set of AWGs was designed for SOI of 4 to 5 μm thickness. This greatly increases the coupling from an optical fiber and makes the devices much less sensitive to fabrication parameters. The polarization sensitivity is also much easier to control in thicker SOI . Although the devices are required to be larger than our first generation devices, a right-angle geometry helped minimize the device area and still resulted in devices smaller than those reported in the literature.

The devices were fabricated with the same RIE etch as our earlier devices, but the process was greatly improved by taking advantage of silicon's native oxide. The two main problems with this etch are the surface roughness and the undercut shape of the waveguide, shown in Fig. 6.12(a). For the new devices the sidewalls

were smoothed after the etch by growing a thermal oxide of 0.4 μm on the samples. This oxide consumes the surface silicon as it grows and is therefore very effective at smoothing these sidewalls. Due to the shape of the undercut waveguide, the oxidation also removed the flared top and resulted in a more typical rib shape, necessary for accurate modeling of the structure. This is shown in Fig. 6.12(b).

Figure 6.12: Sidewall of a waveguide rib, (a) as removed from the RIE. (b) After thermal oxide growth and removal of the oxide.

In Fig. 6.12(b) the oxide has been removed from the surface to better show the waveguide shape. However for device fabrication this thermal oxide was left on the samples and served as a protective upper cladding. The use of this thermal process is possible in SOI because of its potential for high temperature processing, and serves to smooth the sidewalls, alter the waveguide shape, and grow a high quality cladding layer.

Fig. 6.13 shows the device layout for the second generation devices. A 90-degree geometry was chosen to reduce device area and channel crosstalk. Two sets of devices were designed with identical layouts, one with a normal channel response and one with a wide passband. This type of AWG attempts to flatten the top of the

passband and widen it so that the laser sources do not need to be precisely tailored to a very narrow channel passband. This wide passband was obtained by increasing the rib width at the image plane of the device so that light from a broader range of wavelengths is coupled to each output waveguide. The top of the passband was flattened by reducing the mode width at the object plane by eliminating the input taper, and by increasing the number of array waveguides. This results in a smaller focal spot at the image plane, which helps flatten the passband by making the focal spot smaller than the width of the output waveguides.

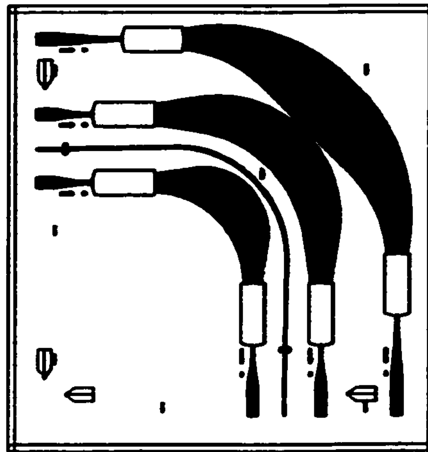


Figure 6.13: Mask layout for second generation AWGs.

The output spectra for the AWGs were found to be much cleaner than the first generation devices, and were very consistent across different channels and samples. The spectrum for a normal passband device is shown in Fig. 6.14. The crosstalk in these devices was better than -20 dB at the center of each channel. For these devices it is not necessary to distinguish between adjacent and non-adjacent channel crosstalk. The channel spacing was measured to be 200 GHz, as designed. The insertion loss for

our second generation devices was roughly 8 to 10 dB, depending on waveguide bend radius in the array. This is a significant improvement over the 15 to 20 dB loss for the earlier devices. This improvement is due to better fiber coupling with the thicker SOI, and smoother rib sidewalls. We attribute much of the loss in the second-generation devices to diffraction into higher order modes, evident from the power detected at the free spectral range of the devices.

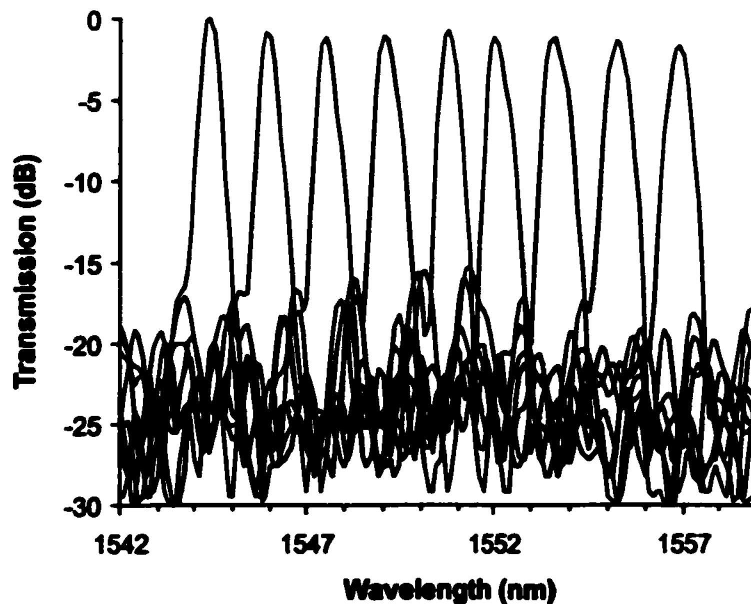


Figure 6.14: Measured output spectrum for a normal passband AWG. This is a second generation device in 4.2 μm SOI with rib width of 5 μm and etch depth of 2 μm.

The output spectrum for a wide passband AWG is shown in Fig. 6.15. The passband for the channels of this device are twice as wide as those in the normal device. This is actually too wide for the device, since the adjacent channel responses overlap significantly in some areas. Ideally, the response of a wide passband device has a flat top with very steep sidewalls, although in practice this is very difficult to realize. The crosstalk for these devices is -18 dB, ignoring the effects from the overlapping

adjacent channel responses. This can be remedied in future designs by modifying the waveguide taper width and mode shape at the image plane. The insertion loss for these devices is the same as for the normal passband devices.

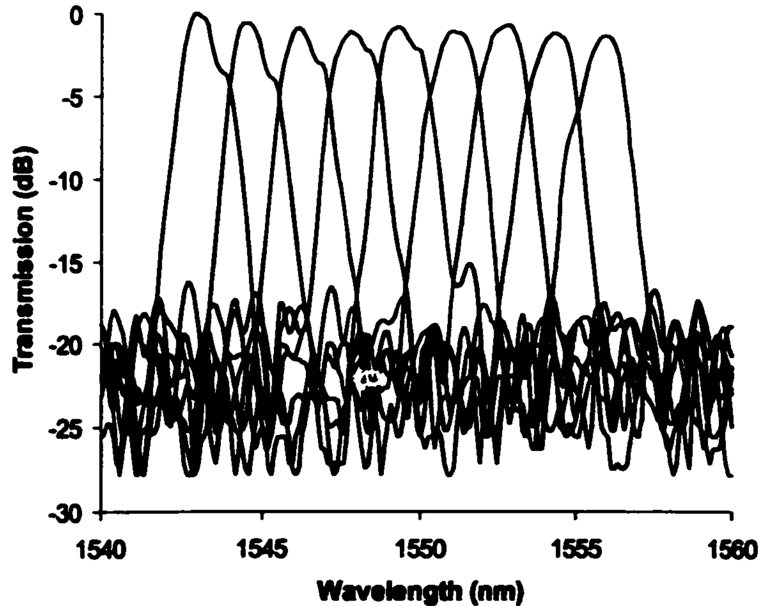


Figure 6.15: Measured output spectrum for a wide passband AWG. This is a second generation device in 4.2 μm SOI with rib width of 4 μm and etch depth of 2 μm.

The first generation devices were severely limited by polarization dispersion, limiting their use to only one controlled input polarization. This problem was virtually eliminated in the new devices since the waveguide birefringence is much easier to control in the thicker SOI, and is less sensitive to the fabrication parameters. The polarization dispersion for the center channel of a second generation device is shown in Fig. 6.16. This can be compared to that shown in Fig. 6.10. The new devices exhibit a polarization dispersion of less than 0.1 nm, which is the limit of our experimental uncertainty. Furthermore, the transmitted intensity at each polarization is also identical, within the limits of our experimental uncertainty. This means that

the device can be used with virtually identical performance in each polarization, and the input polarization does not need to be controlled. This makes the device very suitable for both commercial applications and monolithic integration.

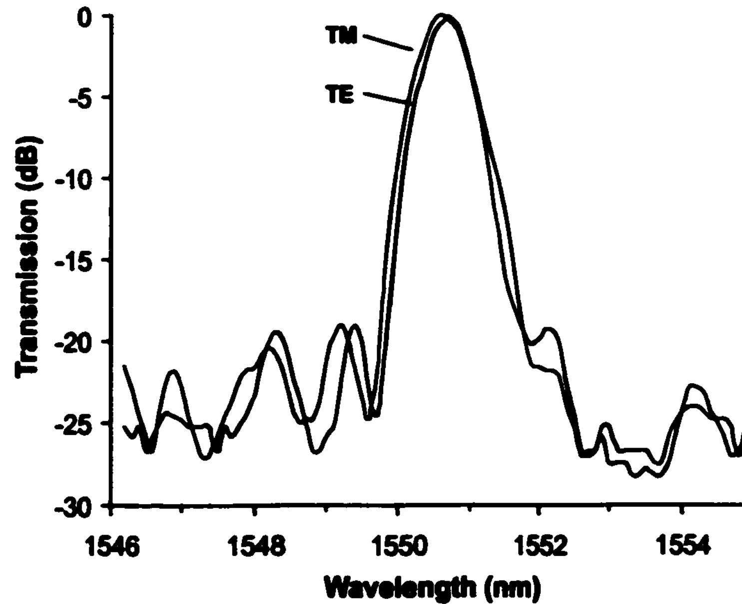


Figure 6.16: Measured polarization dispersion in the center channel of a second generation SOI AWG demultiplexer fabricated in 4.2 μm SOI.

The temperature sensitivity of the AWGs was measured by mounting the devices on a thermoelectric cooler. As the temperature of the device was varied, the laser wavelength was tuned for the maximum power at the center output waveguide. These results are shown in Fig. 6.17. The center wavelength of the AWG was found to vary by only 0.09 ± 0.006 nm/°C, which corresponds to 18.5°C for a shift of a full channel spacing. These temperature requirements could be easily accommodated in a commercial device.

The results for our second generation of AWGs were considered quite sufficient for monolithic integration with SiGe photodetectors. The following section outlines

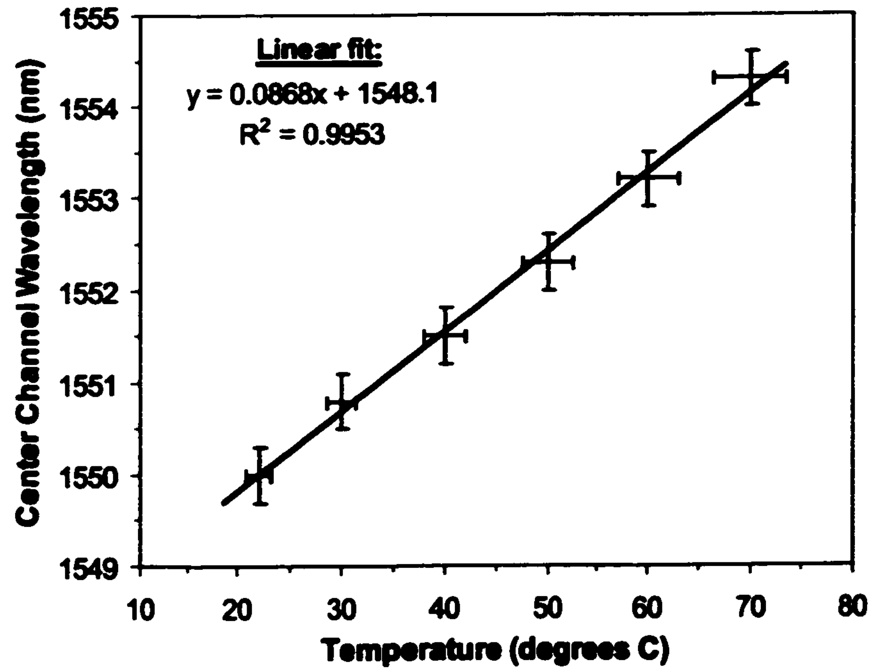


Figure 6.17: Measured temperature sensitivity of an AWG fabricated in 4.2 μm SOI.

the experimental results for our SiGe coherent wave photodetectors.

6.3 SiGe Coherent Wave Photodetectors

SOI wafers were used as the substrates for the coherent wave SiGe growth. The initial experiments were performed on SOI with a top silicon thickness of 1.8 μm. The results presented here are for samples grown at 525°C by ultra-high vacuum CVD (UHV-CVD), although structures were also grown using MBE and exhibited similar characteristics. Further information on these MBE-structures can be found in [59]. A 15 nm thick silicon buffer layer was grown, followed by a ten period superlattice with nominal $Si_{.50}Ge_{.50}$ wells of 5 nm thickness, and Si barriers 12 nm thick. The top Si cap was grown to a thickness of 25 nm. The superlattice structure departed from the nominal values since the growth parameters were deliberately selected to enhance non-planar growth.

Waveguides were formed by RIE in a Cl_2/O_2 mixture to a depth of 1.5 μm. The rib width was 5 μm in the straight waveguide section, and 65 μm in the collection section. This results in multimode waveguides, but this was of no consequence to these experiments and facilitated fiber coupling. A layer of oxide was deposited by PECVD for electrical isolation, and a window of 27 μm $\times$ 260 μm was opened for electrical contact. Schottky contacts to the Si cap layer were formed with an electron-beam evaporated Al layer, and were annealed at 420°C for 20 sec. The distance between the contact pads was 19 μm , and the length of the electrodes was 240 μm . Some devices were patterned with 2 μm interdigitated fingers to form a typical MSM detector structure, and some were left with only the large contact pads.

Transmission electron microscopy (TEM) and atomic force microscopy (AFM) were used to verify the surface wave formation. TEM images showed that the SiGe layers had thickness modulations as large as 10 nm. The Si barrier layers were not thick enough to fully planarize the growth surface, and this favored vertical ordering

and self-organization of the undulations into relatively uniform size and distribution. The wavelength of the coherent wave was roughly 100 nm. Fig. 6.18 shows a TEM image of such a growth.

Figure 6.18: TEM image of a $Si_{.50}Ge_{.50}$ coherent wave superlattice grown for this work.

Both photoluminescence (PL) and photocurrent (PC) spectroscopy were used to obtain information on the position of the band gap, and the variation of optical absorption with wavelength. PL spectra were collected at a temperature of 5 K using a Fourier transform infrared spectrometer with InSb detector. An Ar^+-ion laser operating at a wavelength of 514 nm was used as the excitation source, with a power density of 100 mW/cm^2 at the sample. Fig. 6.19 shows the PL spectrum for a UHV-CVD grown superlattice structure. No defect related PL emission lines are seen in the spectrum, confirming that these superlattices are strained and defect free. These emissions were visible in the PL spectra for structures with larger well thicknesses. Two main peaks are seen in the PL spectrum, corresponding to the direct no-phonon (NP) transition, and the transverse optical phonon (TO) assisted

transition, respectively. The energies/wavelengths of these peaks are directly related to the band gap of the material, its strain, and the shift due to the quantum well confinement. The wavelength of the NP peak near 1.55 μm corresponds to a band gap energy of 0.787 eV, which converts to 0.747 eV at room temperature. This band gap is approximately 0.05 eV lower than would be expected for a uniform planar quantum well with the same nominal growth parameters [8]. The lower band gap can only be explained by a combination of reduced quantum confinement and an enhanced Ge concentration at the wave peaks.

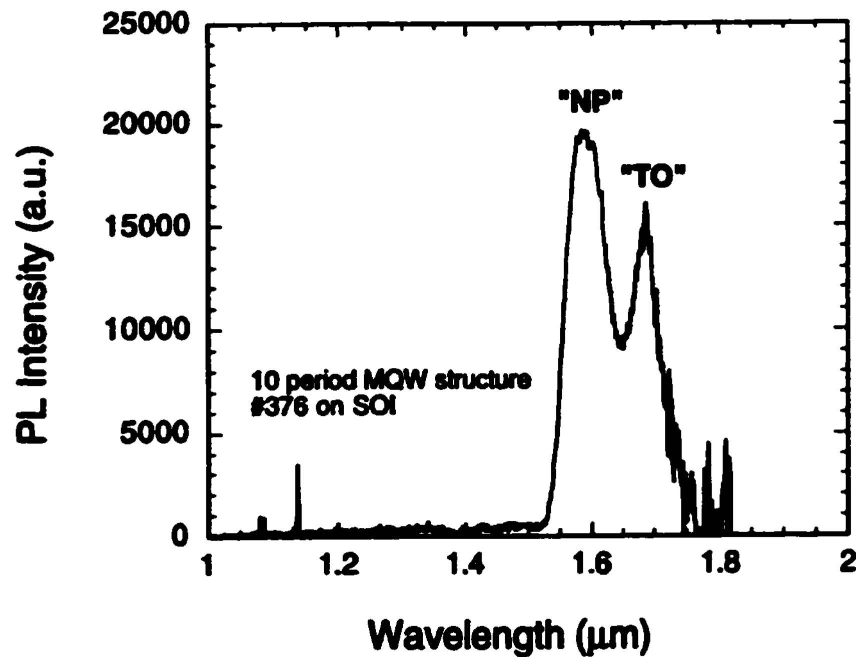


Figure 6.19: Photoluminescence spectrum for a UHV-CVD grown $Si_{.50}Ge_{.50}$ superlattice.

Photocurrent spectroscopy is the most relevant measurement for the assessment of these heterostructures for application in photodetectors. PC spectroscopy provides information on the room temperature optical absorption edge, and the variation of optical absorption with wavelength. Photocurrent spectra were obtained

between wavelengths of 1100 nm and 1700 nm. A fiber-coupled monochromator was used at short wavelengths, and to improve the signal to noise ratio and the available power, a Cr:YAG laser (λ =1380 nm to λ =1510 nm) and an external cavity semiconductor laser (λ =1490 nm to λ =1620 nm) were used for the specified wavelength ranges. In all cases the light was modulated. The sample electrodes were biased at 2 V and the photocurrent was collected using a transimpedance amplifier followed by a lock-in amplifier. For all light sources, the optical signal was passed through a Si filter before being coupled to an optical fiber. This ensures that all the residual short wavelength light from the monochromator is removed, and that the response of the SiGe photodetectors is due entirely to the Si/SiGe superlattice. Since all light within the Si absorption band is removed before the detector, the generated photocurrent at the samples can only be due to a shift of the absorption band due to the SiGe. The photocurrent spectrum for a UHV-CVD grown $Si_{.50}Ge_{.50}$ superlattice detector is shown in Fig. 6.20.

Unlike PL which provides an unambiguous determination of the electronic band gap minimum, determining this quantity from PC measurements requires a fit to experimental data. In the case of simple parabolic bands, the energy dependence of the optical absorption α should have a simple polynomial form, $\alpha(E) \approx (E - E_g)^y$, where E_g is the band gap energy, and the value of y is dependent on the structure [60]. In our samples the structure is complicated by the local variations in both quantum well thickness and Ge concentration, so that the band gap varies from point to point. If it is assumed that the local absorption edges are uniformly distributed in energy range within 0.2 eV of the lowest absorption edge E_g, it can be shown [61] that the photocurrent should vary as above with $y = 3$. This dependence has been successfully used to fit experimental photocurrent spectra of SiGe quantum

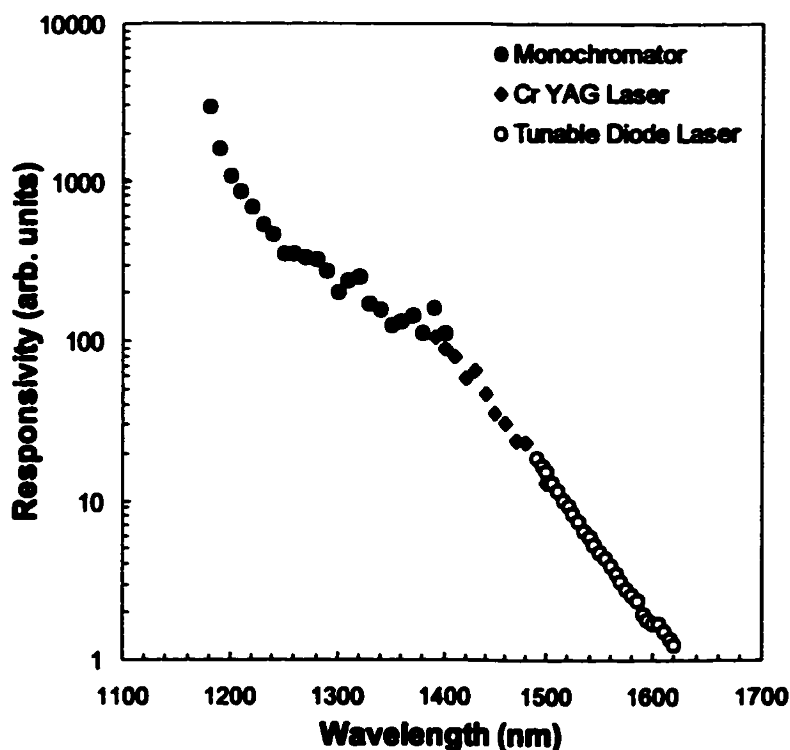


Figure 6.20: Photocurrent spectrum for a UHV-CVD grown $Si_{.50}Ge_{.50}$ superlattice.

wells [61], and was used here to estimate the band gap energy determined using PC spectroscopy. The PC spectrum for a UHV-CVD superlattice is shown in Fig. 6.21, where the wavelength data from Fig. 6.20 has been converted to photon energy. The rapid rise of responsivity with photon energy can be approximated by a cubic polynomial, $(E - E_g)^3$, with a best fit energy gap of E_g=0.745 eV.

The measured dark current for an MSM detector with Al contact pads is shown in Fig. 6.22. The dark current behavior is typical for a Schottky MSM detector, saturating at high bias voltage. The dark current for this device is quite high at $\leq$ 100 nA/μm^2, and may be due to the relatively rough surface of the Si cap layer which is only 25 nm thick, not thick enough to planarize the SiGe undulation. This roughness may result in a high density of surface states, which are known to cause

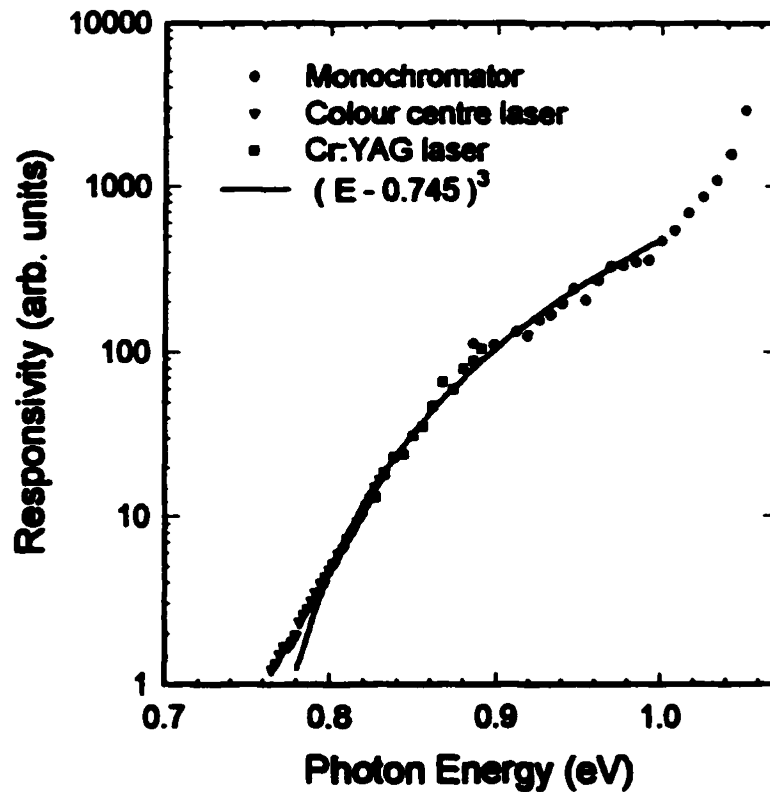


Figure 6.21: Photocurrent spectrum for a UHV-CVD grown $Si_{.50}Ge_{.50}$ superlattice. The solid line is a fit of the equation $\alpha(E) \approx (E - E_g)^3$ to the data.

large leakage currents and low frequency gain in III-V MSM photodetectors [62], [63]. A second wafer with a much thicker 300 nm Si cap over an identical superlattice exhibited a dark current of $\leq$ 10 nA/μm^2.

The photocurrent of the detectors as a function of bias voltage is shown in Fig. 6.23 for different illumination power at λ=1310 nm. At low bias the photocurrent increases linearly with voltage as the electric field gets stronger and sweeps more photo-generated carriers towards the electrodes. As bias increases further, all photo-generated carriers are collected and the photocurrent saturates. This behaviour is

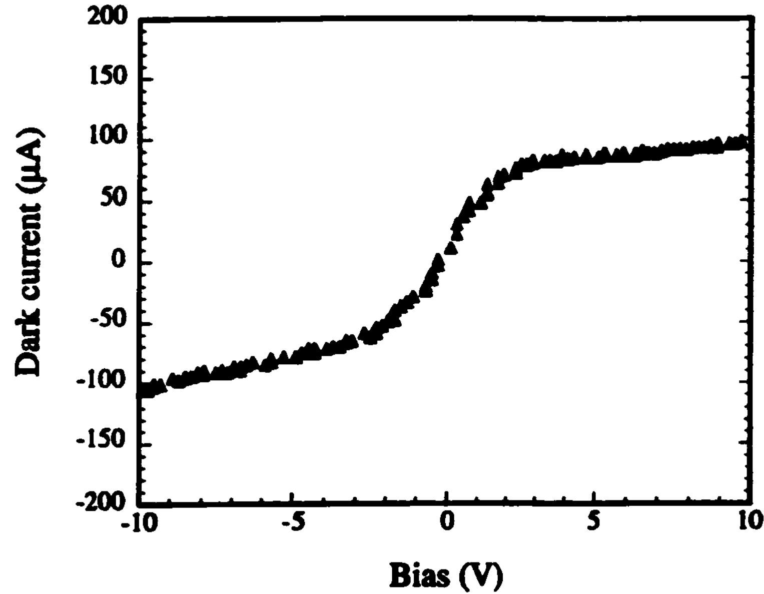


Figure 6.22: Dark current vs. bias for the photodetectors.

typical for an MSM photodetector, and can be simulated with the Hecht formula [64],

$$J_{ph} = q\Phi\alpha L(\mathrm{E})\left(1 - e^{-d/L(\mathrm{E})}\right) \tag{6.1}$$

where Φ is the photon flux, α is the optical absorption coefficient, d is the distance between electrodes, and $L(\mathrm{E}) = \mu\tau E$ is the drift length, where μ and τ are the carrier mobility and lifetime, respectively. The insert of Fig. 6.23 shows a fit of this formula to the experimental data for one illumination level. For different illumination levels the curves can be fit by simply multiplying J_{ph} by a constant. However, this constant is not directly proportional to the light intensity, suggesting that the absorption coefficient of these SiGe detectors is dependent on the light intensity.

The dependence of the photocurrent on illumination levels for different bias is plotted in Fig. 6.24 for both 1310 nm and 1520 nm wavelengths. The intensity shown is the light intensity out of the fiber. The increase of photocurrent saturates with

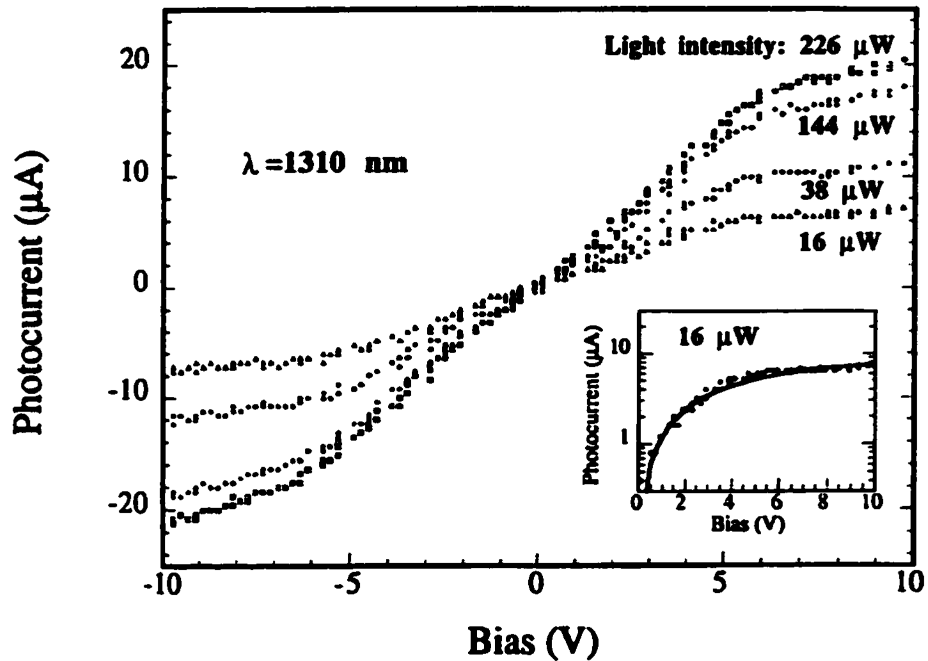


Figure 6.23: The dependence of photocurrent on bias for different illumination levels at 1310 nm wavelength. The light intensities indicated on the figure are intensities out of the fiber. Insert: The I-V at 16 μW plotted in semi-log scale.

light intensity, at different rates for the two different wavelengths. The data shown in Fig. 6.24 approximates a relationship of $I_p \approx P^n$, where I_p is the photocurrent, P is the optical power, and $n \approx 0.4$ for 1310 nm and $n \approx 0.7$ for 1520 nm. This leads to a responsivity for these detectors that varies with optical power.

The responsivity of the detectors is higher at lower illumination levels. The coupling between the tapered fiber and waveguide was estimated to be roughly 20% and could reach a maximum of 30%, as measured relative to a straight waveguide with no detector region. Within the ranges measured, the highest responsivities were approximately 1.6 A/W at 1310 nm wavelength, and 0.12 A/W at 1520 nm wavelength, based on a fiber-to-waveguide coupling of 30% to give a conservative value for the responsivities. These high responsivities suggest some photoconductive

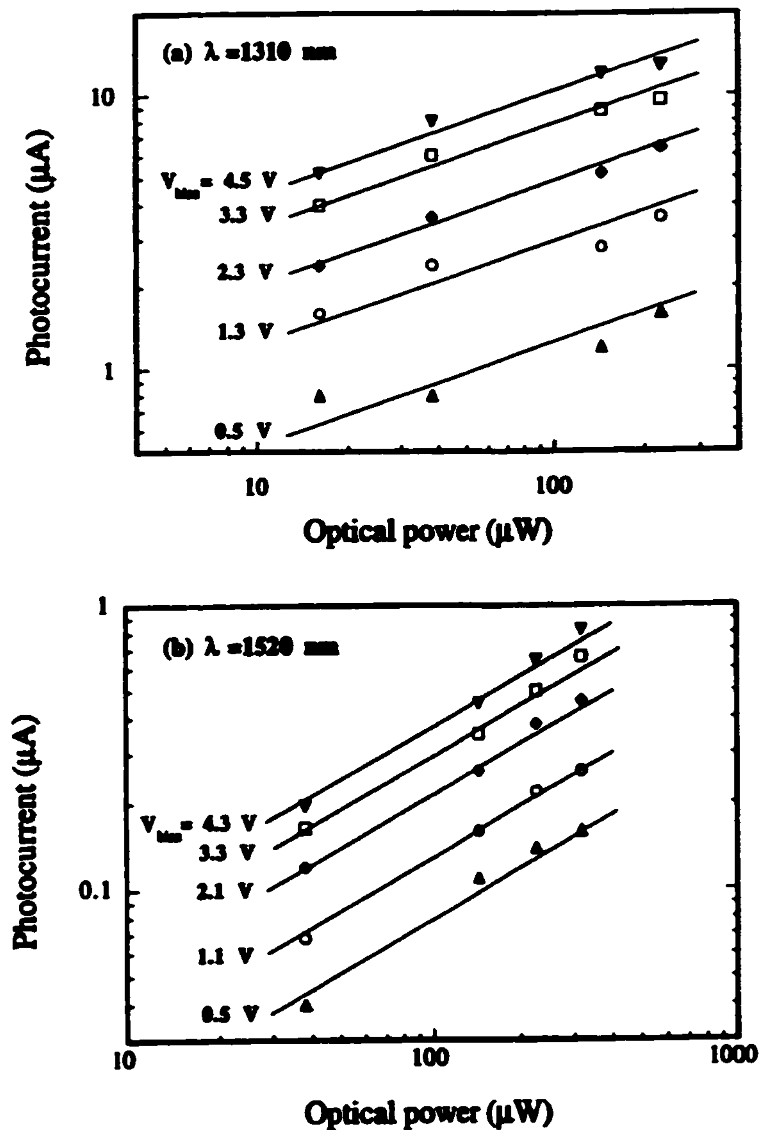


Figure 6.24: The dependence of photocurrent on light intensity for (a) 1310 nm wavelength, and (b) 1520 nm wavelength.

gain. This is likely due to the large dark currents which are sometimes accompanied by low frequency gain [63]. The large difference in mobilities for the electrons and holes in the Si/SiGe MQWs may also contribute to this phenomenon.

The responsivity for the detectors is quoted rather than the internal quantum

efficiency, since a large leakage current is sometimes accompanied by low frequency gain, as discussed above. Therefore, direct determination of the internal quantum efficiency is unreliable until there is a better understanding of the electrical properties of the coherent wave MSM photodetectors. The origin of the sub-linear dependence of the photocurrent on light intensity is also not clear at this point. These results are indicative of the complexity of these undulating SiGe superlattice structures, whose electrical and optical properties have not previously been reported.

This work represents the first reported use of three-dimensional growth morphology to fabricate SiGe photodetectors for use at 1.55 μm wavelengths. The results suggest that taking advantage of these three-dimensional structures can provide a new route to practical Si-based photodetectors in the near infrared. The proof of this concept was in the fabrication of an SOI waveguide monolithically integrated with a SiGe coherent wave photodetector. The measured internal responsivity of 0.12 A/W at a wavelength of 1520 nm, to the best of our knowledge, is the highest reported in any SiGe or Ge system to date.

Chapter 7

Conclusion

This thesis has developed all of the required technologies for the monolithic integration of DWDM devices and photodetectors in a Si-based system. Advanced SiGe photodetectors have been monolithically integrated with SOI waveguides, and demonstrate photoresponse at wavelengths suitable for DWDM receiver applications.

A low-cost fabrication technique has been developed that allows standard silicon IC technology to be used for the processing of photonic components in SiGe and SOI. This was the first reported use of this technology for the fabrication of Si-based photonics. The potential commercial applications for use in SiGe are limited by the dislocations induced during high temperature processing. Although a number of developments were presented in this thesis to minimize the dislocation density, the minimum values achievable are still only marginally acceptable for optical components and the process needs to be developed further before it is commercially viable. The LOCOS process was also adapted to SOI substrates and was shown to be very successful in this material system. The material quality is not affected by the LOCOS process, and low-loss waveguides can be manufactured with rib heights approaching 2 μm. A patent application has been filed for this technology due to the potential for commercial, high-volume processing of photonic components.

Arrayed waveguide grating demultiplexers have been designed and fabricated in silicon-on-insulator. Design issues specific to the SOI material system have been investigated and reported in the literature. It was shown that coupling to high order modes in the splitter and combiner section of the AWG should have a minimal effect on device performance, although it can be the limiting factor in the crosstalk performance of the device. AWGs fabricated in 4.2 μm thick SOI demonstrated crosstalk of -20 dB across eight channels. The measured polarization dispersion was less than the 0.1 nm experimental uncertainty of the measurements, and the temperature sensitivity was 0.09 nm/°C. This performance is suitable for a commercial device and monolithic integration with Si-based photodetectors.

This work resulted in the first demonstration of SiGe coherent wave quantum well photodetectors. Three-dimensional growth modes were used to enhance the photoresponse at λ=1.55 μm, and resulted in the highest responsivities yet reported for any Si-based photodetector. Furthermore, these detector structures were monolithically integrated with SOI waveguides. This demonstrates their potential for monolithic integration with nearly any passive WDM component.

7.1 Recommendations for Future Research

Monolithic integration of Si-based waveguides and photodetectors using conventional processing has been presented in this thesis. The benefits to fabrication and assembly costs that result from this can be significant, but would be further enhanced by the use of LOCOS processing for fabrication. This thesis has demonstrated the use of the LOCOS process for fabricating passive WDM components, but whether the SiGe coherent wave QW photodetector structure will survive LOCOS processing temperatures without dislocating remains to be investigated. It is unclear how the

strain relief from the three-dimensional growth mode will affect the stability of the SiGe layers at high temperatures. A detailed analysis of the effects on material quality and photodetector response would be a research project unto itself, and is beyond the scope of this thesis. A better understanding of the internal behaviour of the SiGe photodetectors is also required in order to eliminate the photoconductive gain and examine the high frequency operation of the MSM devices.

The SOI LOCOS process would benefit from a new suitable mask layer, eliminating the need for CVD deposition of SiO_2/Si_3N_4. Likely candidates are metal layers such as those examined in this thesis, but at lower thickness. Thinner layers of metal may not be as highly stressed, and could possibly survive the LOCOS temperatures without peeling away from the sample, and yet remain thick enough to act as a barrier to oxidation.

This thesis has concentrated on passive WDM components, however it is also possible to use current injection to actively control SOI waveguide devices. Potential applications include optical switches, add/drop multiplexers, and variable optical attenuators. SOI is also suitable for on-chip integration of electronics, such as amplifier circuitry and control circuits. The technologies presented in this thesis permit the monolithic integration of SOI AWGs with SiGe photodetectors. Integrating amplifier circuitry onto the same chip would result in one of the highest levels of integration ever reported in a Si-based system. This could lead to true "systems-on-a-chip", a long-standing goal of Si-based optoelectronics.

The devices and technologies presented in this thesis are intended to be proofs of concepts, and as such are not necessarily intended to be comparable to commercial products. However, a number of advancements in the state of the art for Si-based optoelectronics have been presented here, and can hopefully lead to more inexpensive

photonic devices that help narrow the gap between telecom fiber optics and the individual subscriber.

Appendix A

List of Publications

A number of publications and conference presentations have resulted from this research, as well as a patent application. The following list includes those publications to which this author has contributed.

Papers

M.R.T. Pearson, P.E. Jessop, D.M. Bruce, J. Ojha, "SiGe-based dual-wavelength demultiplexers and polarization splitters", *Proc. of SPIE*, vol. 3630, Jan. 1999.

D.-X. Xu, S. Janz, H. Lafontaine, M.R.T. Pearson, "Photodetectors for 1.3 μm and 1.55 μm wavelengths using SiGe undulating MQWs on SOI substrates", *Proc. of SPIE*, vol. 3630, Jan. 1999.

M.R.T. Pearson, A. Bezinger, A. Delâge, J.W. Fraser, S. Janz, P.E. Jessop, D.-X. Xu, "Arrayed waveguide grating demultiplexers in silicon-on-insulator", *Proc. of SPIE*, vol. 3953, Jan. 2000.

S. Janz, J.-M. Baribeau, D.J. Lockwood, J.P. McCaffrey, S. Moisa, N.L. Rowell, D.-X. Xu, H. Lafontaine, M.R.T. Pearson, "Si/SiGe photodetectors using three dimensional growth modes to enhance photoresponse at λ=1550 nm", *J. Vac. Sci. Technol. A*, vol. 18, no. 2, pp. 588-592, Mar/Apr. 2000.

M.R.T. Pearson, P.E. Jessop, D.M. Bruce, S. Wallace, P. Mascher, J. Ojha, "Fabrication of SiGe optical waveguides using VLSI processing techniques", submitted to *J. Lightwave Technol.*, Jan. 2000.

Conference Presentations

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Appendix B

Glossary of Abbreviations

AWG	Arrayed Waveguide Grating
BPM	Beam Propagation Method
CVD	Chemical Vapor Deposition
DWDM	Dense Wavelength Division Multiplexing
EIM	Effective Index Method
FTTH	Fibre-to-the-Home
IC	Integrated Circuit
LOCOS	Local Oxidation of Silicon
MBE	Molecular Beam Epitaxy
MQW	Multiple Quantum Well
MSM	Metal Semiconductor Metal photodetector
PHASAR	Phased Array demultiplexer
QW	Quantum Well
UHV-CVD	Ultra-High Vacuum Chemical Vapor Deposition
VLSI	Very Large Scale Integration
WDM	Wavelength Division Multiplexing

Appendix C

Photolithography Masks

Two of the four masks designed for this work are shown on the following pages. The duplexer devices have a very high aspect ratio and therefore appear more or less as straight lines, so that mask is not shown here. The first generation AWG mask is property of the National Research Council and is not shown here, however some of the devices were modified to improve performance and are included on the second generation AWG mask. With the exception of this first AWG mask, all the masks for this work were designed by the author. The masks were designed in AutoCAD and IC-Editor, and were written by e-beam at Nortel Networks Ltd.. Photographs are also included which show the size of the fabricated devices.

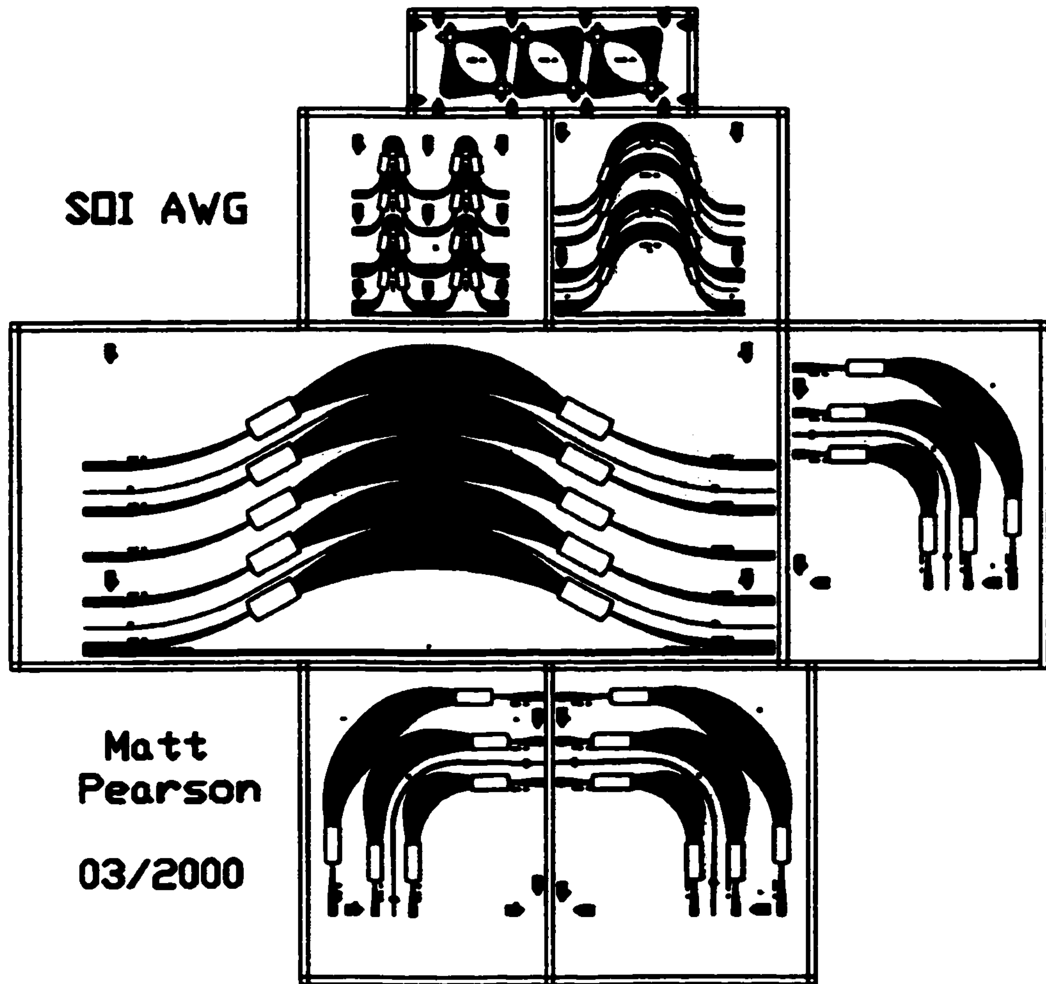

Figure C.1: Mask layout for second generation AWGs fabricated in SOI.

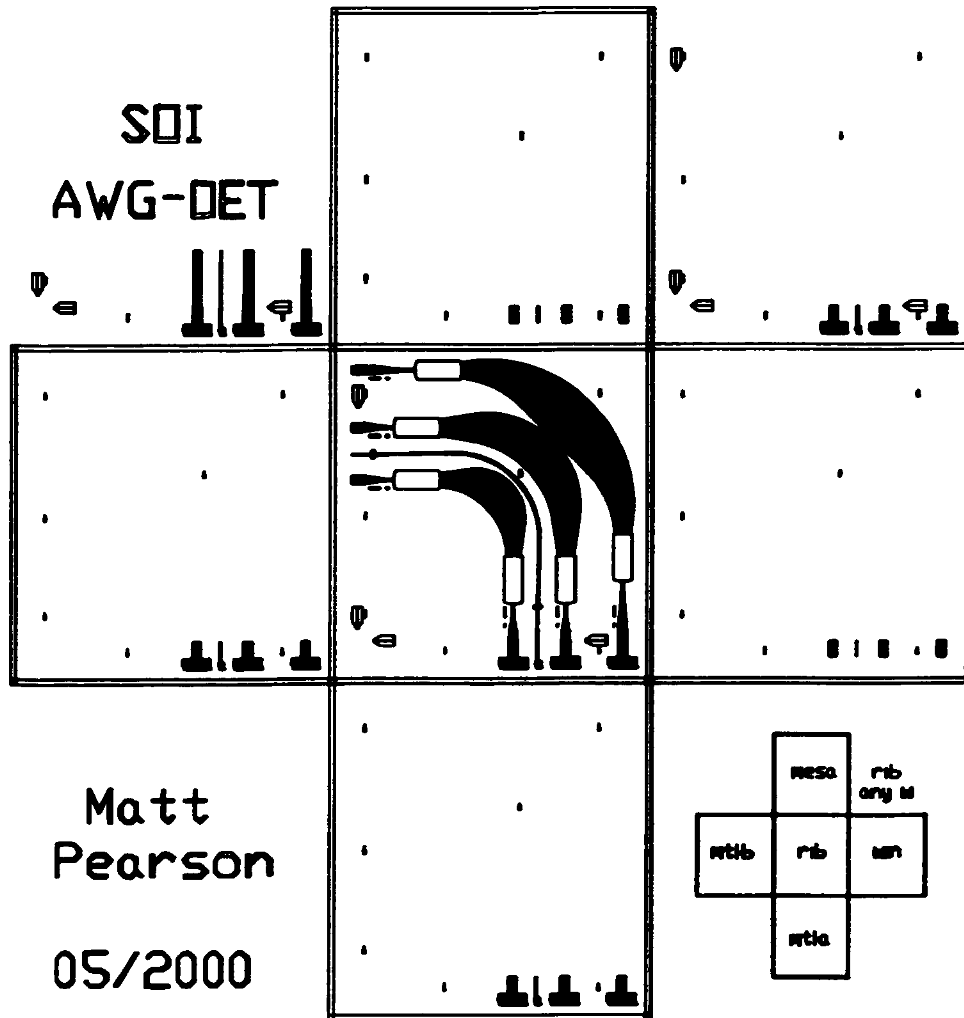

Figure C.2: Mask layout for second generation SOI AWGs monolithically integrated with SiGe photodetectors. This mask will be used in future research but is based on all the technologies and device structures developed in this work.

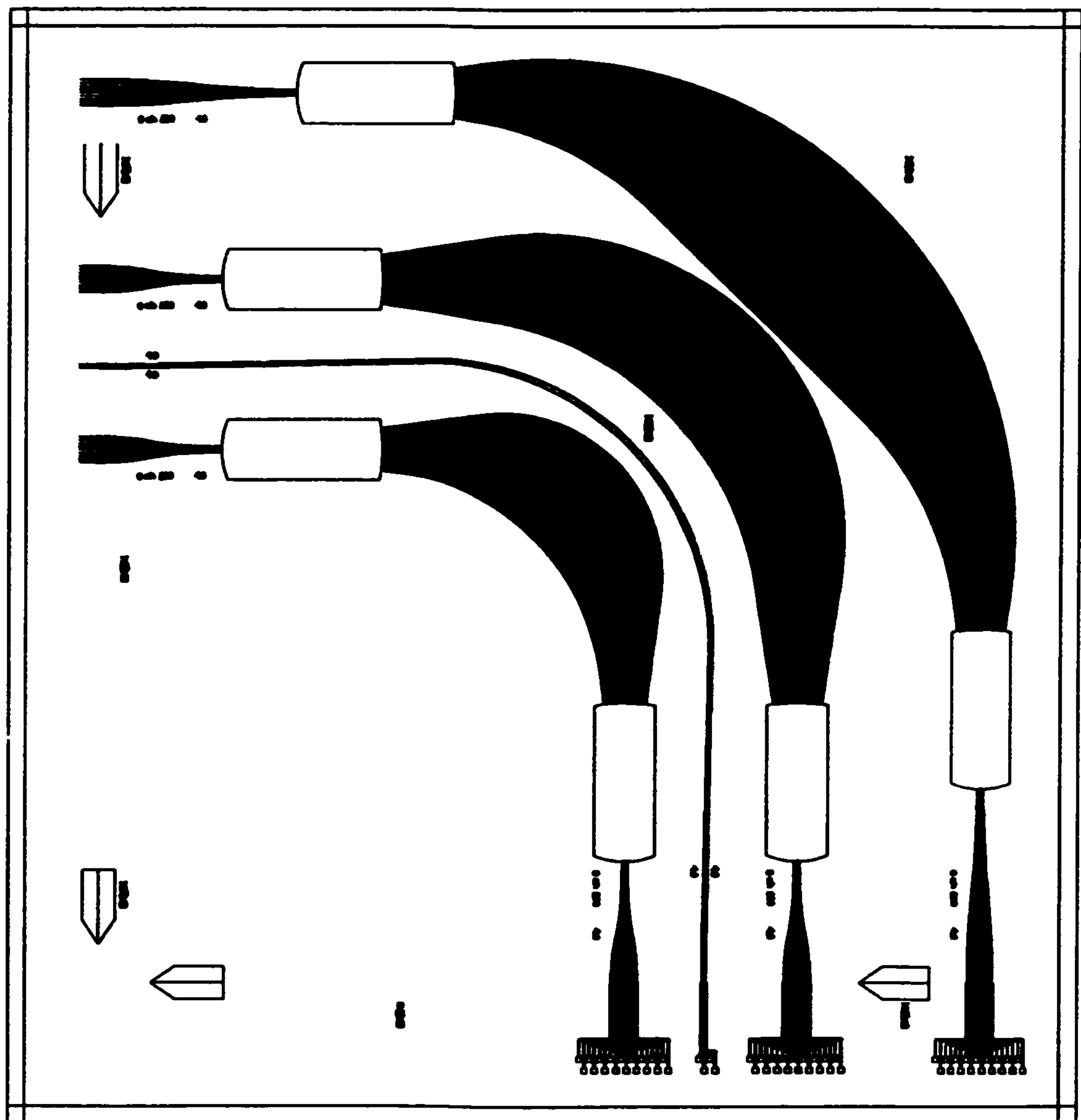

Figure C.3: Close up view of AWGs fabricated in SOI, monolithically integrated with SiGe photodetectors. Optical input at left, electrical output contacts at bottom.

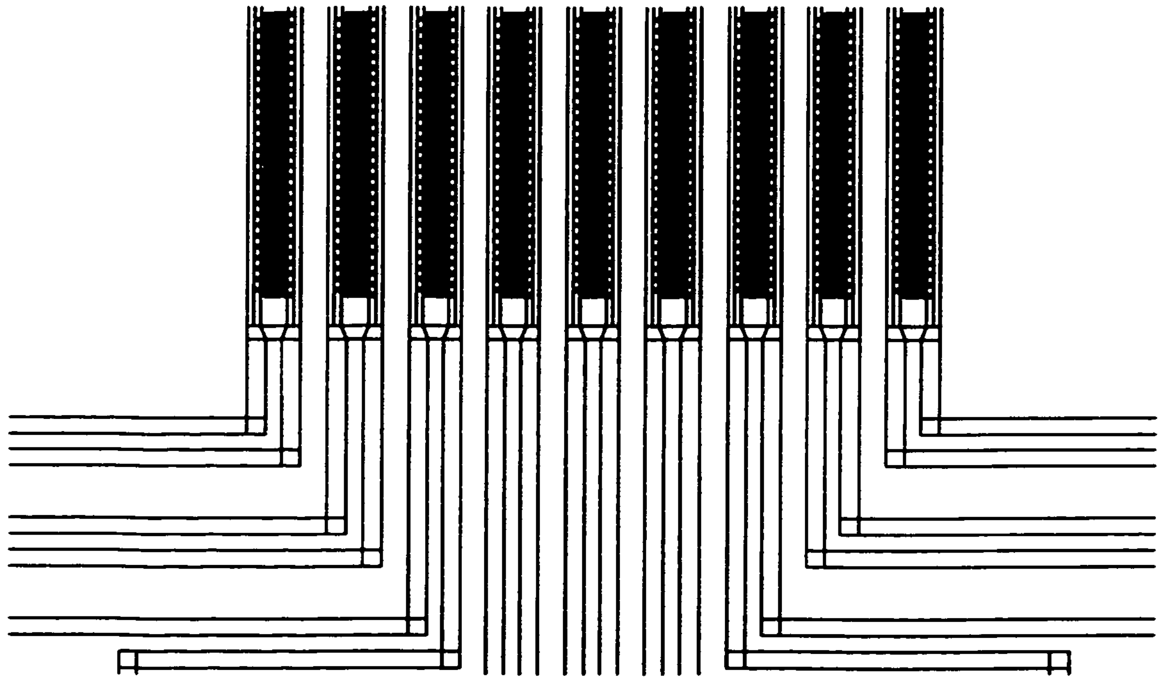

Figure C.4: Close up view of MSM detector structure at the output of the AWG.

Figure C.5: First generation AWG demultiplexer.

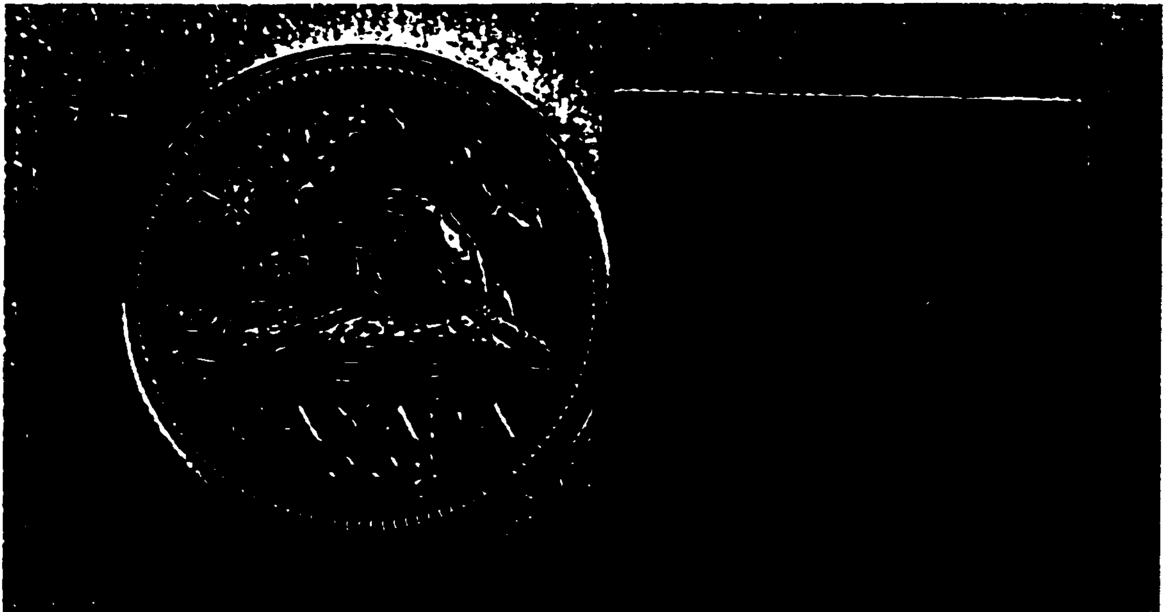

Figure C.6: Second generation AWG demultiplexer.

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