HIGH SPEED INTERDIGITAL MSM PHOTODIODES

By

RICHARD JOHN SEYMOUR, B.Sc., M.Eng.

A Thesis

Submitted to the School of Graduate Studies

in Partial Fulfillment of the Requirements

for the degree

Doctor of Philosophy

McMaster University

September 1989

HIGH SPEED INTERDIGITAL MSM PHOTODIODES

DOCTOR OF PHILOSOPHY (1989) McMASTER UNIVERSITY

(Physics) Hamilton, Ontario

TITLE: HIGH SPEED INTERDIGITAL MSM PHOTODIODES

AUTHOR: Richard John Seymour, B.Sc. (University of Waterloo)

M.Eng. (McMaster University)

SUPERVISOR: Dr. B.K. Garside

NUMBER OF PAGES: x, 143

ABSTRACT

A fast, simple photodetector which is compatible with optical integration techniques can be produced using a design consisting of an interdigital metal – semiconductor – metal (MSM) photodiode. The general operation of these devices is discussed with emphasis placed on basic device characteristics such as IV, CV, and steady state and pulsed light response. Ideas and models are presented to allow predictions of generic device performance as well as design and optimization of specific devices. These theoretical aspects are validated through comparison with experimental results.

ACKNOWLEDGEMENTS

The author would like to thank Dr. B.K. Garside for his supervision of this work and for the assistance he provided throughout. Thanks also to Dr. Timusk, Dr. Jessop, and Dr. Thompson for their assistance in completing this thesis. Special thanks to Ann Levy for her invaluable contributions and to my parents for their continuing support. Finally, thanks to all the people whose contributions were perhaps less tangible but not necessarily less valuable.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

INTRODUCTION

The development of high speed photodetectors has been driven by a variety of concurrent developments in other areas. Much of the early work can be attributed to needs which developed as a result of progress in short pulse lasers. With the introduction of room temperature diode lasers, and low loss glass fibers, optical communications became the principal driving force in the development of both fast diode lasers and fast, sensitive optical detectors. As these systems progressed both in speed and complexity, it became clear that in order to optimize performance, it would be necessary to integrate the optical and electrical components in the form of opto–electronic integrated circuits (OEICs).

OEICs incorporate optical, opto–electronic, and electronic devices on the same semiconductor substrate. The reduction in the parasitic reactances, which are a consequence of the interfacing of discrete devices, facilitate a major improvement in both speed and noise performance. The monolithic integration of many elements on a single chip also reduces the total number of components required for a complete system, producing a simpler, cheaper assembly procedure, and a more compact, reliable system (Wada 1986a).

One of the challenges of OEICs is the integration of optical devices, usually with vertical structure, and planar electronic devices such as FETs. The simplest solution involves the development of optoelectronic planar structures.

Fast, sensitive photodetectors have many uses beyond OEICs. There is a large demand for discrete devices of this type in optical communications. Other uses include monitoring short pulse lasers and other high speed optical components and phenomena.

Presented in this thesis is the study of a fast photodetector design consisting of a metal–semiconductor–metal (MSM) interdigital photodiode. The structure is of interest because it is fast, simple, easily integrated, and has a small capacitance. The purpose of this study is to understand the device well enough to allow straight forward modeling of its characteristics. Predictions and optimization of the device performance can then be made.

The MSM interdigital photodiode consists of two sets of interdigital metal fingers on the surface of a semiconductor. With the proper choice of metal and semiconductor, a pair of back–to–back Schottky barriers are formed. When a bias voltage is applied across the device, one set of digits is reverse biased creating a region of electric field between the digits. The extent of this region is a function of the applied voltage and the semiconductor parameters. It is this electric field region which separates and collects the photocarriers generated in this region. The other set of digits is forward biased and, to a simple first approximation, behaves as an ohmic contact.

Much of the appeal of these devices lies in having both contacts on the top surface. This allows the use of semiconductor–on–insulator (SOI) materials, which have several advantages. The depletion capacitance of the device is greatly reduced by limiting the semiconductor to a thin film thereby reducing the total capacitance to the structure capacitance of the digits. This inherently small capacitance is an important consideration in the response time of the device when connected to an external circuit. In addition, the use of a planar structure on a low carrier concentration ($< 10^{15}\,cm^{-3}$) SOI material without the use of pn junction technology makes these devices compatible with MESFET technology (Wada 1986). As a result these devices are directly compatible with optoelectronic integration

techniques.

An added advantage of having both contacts on the top surface is the creation of an electric field parallel to, and at the semiconductor surface. As a result the photocarriers generated at the surface are collected, giving these devices enhanced sensitivity in wavelength regions where the absorption coefficient is large (generally greater than 10^4 cm^{-1}).

Initial work on interdigital devices was done in the early 1980's. For example Sugeta et. al. (1980) put interdigital photodiodes in striplines on semi–insulating and epi–layer GaAs. They demonstrated a frequency response up to their measurement limit of 1.5 GHz. Slayman (1981) and Figueroa (1981) put a simple interdigital structure on semi–insulating GaAs, and a more complicated interdigital structure on epi–layer GaAs. They found a pulse response of 90 psec, and a flat frequency response to 2.5 GHz. Seymour et. al. (1984) presented a preliminary investigation of an interdigital device on silicon – on – sapphire (SOS) for use as a fast ultraviolet detector. Roth et. al. (1985) made a small area device which exhibited a bandwidth of 18 GHz and a quantum efficiency of 25%. These authors have demonstrated that interdigital structures can make fast, sensitive photodetectors, but they limited themselves to doing a few simple measurements on the devices.

Since 1986 interest in interdigital devices has increased as the desire for planar structures for OEIC has increased. Different designs have been studied. For instance, Jackson (1986a) has examined an interdigital p–i–n structure with a measured frequency response of 8 GHz. Wojtczuk (1987) has done comparative studies of interdigital n–p–n, n–p–metal, and photoconductor devices giving FWHM response times of 53 psec, 72 psec and 450 psec respectively. Further work

has been done on MSM interdigital devices with Schumacher (1988) reporting a response time of 55 psec and a quantum efficiency of 44 percent, and Zeghbroeck (1988) reporting an impulse response less than 5 psec and a bandwidth of 105 GHz. Preliminary investigations of the operation of these devices using GaAs were performed by Boudebous (1985) who considered capacitance, Ito (1986) who studied capacitance and dark current, and Jackson (1986b) who studied dark current. Seymour (1986, 1988) presented measured and modeled results of interdigital photodiodes on SOS, and a discussion of factors affecting the response time of interdigital photodiodes, including a model of the capacitance.

The bulk of this work contained very little modeling or analysis beyond the immediate device under test. With the increased demand for photodetectors for OEIC applications, there is a definite need to know what these structures are capable of, and to be able to design and optimize these devices to meet specific operation parameters. This thesis presents a series of models designed to meet many of these needs. The models cover a range of complexities, and have been tested through comparison with each other, and with experiment. With these tools, general and specific predictions of structure characteristics can be made.

The layout of information in the text is as follows: Chapter 1 introduces the various numerical finite differences models used and gives some basic results of these models. Chapter 2 discusses the experimental devices used, the material properties, and some of the basic DC measurements made. The measurement and modeling of capacitance is discussed in chapter 3 and chapter 4 compares the experimental and theoretical pulsed response of sample interdigital devices on silicon and GaAs substrates. The final chapter, chapter 5, will be devoted to several sample applications of the work presented.

CHAPTER 1: DEVICE MODELING

Most semiconductor photodetectors operate on similar basic principles. These principles may be summarized as follows. Incident light interacts with the semiconductor to produce electron – hole pairs. The electron – hole pairs act as current carriers and are transported through the semiconductor. Finally, they interact with the external circuitry to produce an output signal. The exact form of these processes is dependent on the type of photodetector.

The detector discussed in this thesis belongs to the group of photodetectors known as photodiodes. Photodiodes have a depleted semiconductor region with a large electric field that separates and transports photogenerated electron – hole pairs across the depletion region. They operate in the wavelength region where absorbed photons excite electron – hole pairs through energy level excitation (usually band to band). Since the diode absorbs only photons whose energy exceeds the bandgap energy, it exhibits a long wavelength cutoff beyond which no photons are detected. Electron – hole pairs which are created in the depletion region are separated by the electric field and drift in opposite directions through the depletion region resulting in net current flow. Electron – hole pairs created outside the depletion region will diffuse until they recombine and are lost, or reach the depletion region and contribute to the net current. A review of different types of photodiodes and their operation can be found in Sze (1981).

To aid in the study of interdigital photodiodes, a numerical model was developed. Numerical modeling is a powerful instrument for the analysis and design of semiconductor devices. Early semiconductor device modeling was done analytically by dividing the device into regions, and applying various simplifying

assumptions to each region. As semiconductor technology developed, the devices became more complex and the need for in–depth theoretical analysis grew. Previously neglected effects became important and it was desirable to solve the basic semiconductor equations with a minimum number of simplifying assumptions. In general this required a form of numerical solution.

The first practical application of a numerical solution was given by Gummel (1964) and developed further by DeMari (1968a,b). From these beginnings, driven by complementary growth in the semiconductor industry and the development of high speed computers, numerical modeling has become a necessary part of the understanding, design, and optimization of semiconductor devices. Accurate simulation of device operation for a variety of device parameters eliminates much of the trial and error in device processing. A good review of key papers in the development of this field is given in chapter 1 of Selberherr (1984).

The starting point of a numerical model is a reasonable mathematical model. Semiconductor device modeling is generally based on the following differential equations, usually referred to as the basic semiconductor equations.

Poisson's equation:

$$\text{div grad } \psi = \frac{q}{\epsilon} (n - p - C) \tag{1.1}$$

Continuity equations:

$$\text{div } \vec{J}_n - q \frac{\partial n}{\partial t} = q R \tag{1.2}$$

$$\text{div } \vec{J}_p + q \frac{\partial p}{\partial t} = - q R \tag{1.3}$$

Current equations:

(1.4) $$\vec{J}_n = q\, n\, \mu_n \vec{E} + q\, D_n \,\mathrm{grad}\, n$$

(1.5) $$\vec{J}_p = q\, p\, \mu_p \vec{E} - q\, D_p \,\mathrm{grad}\, p$$

Total current:

(1.6) $$\vec{J}_t = \vec{J}_n + \vec{J}_p + \frac{\partial}{\partial t}(\epsilon \vec{E})$$

where ψ is the electrostatic potential

$\vec{E}$ is the electric field vector

q is the elementary charge (= 1.602×10^{-19} Coulombs)

ϵ is the absolute permittivity

n, p are the electron and hole concentrations

C is the net fixed ionic charge

$\vec{J}_n$, $\vec{J}_p$, $\vec{J}_t$ are the electron, hole, and total current densities

R is the net carrier recombination/generation rate

μ_n, μ_p are the electron and hole mobilities

D_n, D_p are the electron and hole diffusion coefficients

t is the time

Although often treated as exact, there are various assumptions inherent in the derivations of these equations. A review of their development as well as a brief discussion of the assumptions made can be found in chapter 2 of Selberherr (1984).

For the applications to be outlined here, as well as in general, the assumptions are reasonable.

The typical layout of an interdigital detector is shown in figure 1.1. Various simplifying assumptions have been made to streamline the model. The device has been assumed to be two dimensional as illustrated in the lower part of figure 1.1. This is justified as long as the digit's length is much greater than the digit width, allowing the effect of the end of the digits to be ignored. The extent of the model is further reduced by considering only one unit cell. This greatly reduces the amount of computation and computer storage required and simplifies the boundary conditions at the edges. The symmetry of the device about this unit cell justifies this simplification.

For the computer model to be described here, the solution of these equations was broken into three major sections, each represented by an individual program. Each section represents a natural step in the process of achieving a complete solution as well as being a solution to a useful simplified problem. A general discussion of these three sections and their uses follows. A more complete discussion of the programs as well as the numerical implementation of the various physical parameters can be found in appendix A1.

The first section consists of a program to solve the potential distribution over the unit cell. The general model represented by equations 1.1 through 1.6 is simplified by assuming zero current flow. Zero current flow is a reasonable approximation for a reverse biased Schottky barrier, and is dependent on the current being small enough that the carrier distribution in the device is not significantly perturbed. This approximation ignores the effects of generation and recombination and allows the majority carrier density to be approximated using

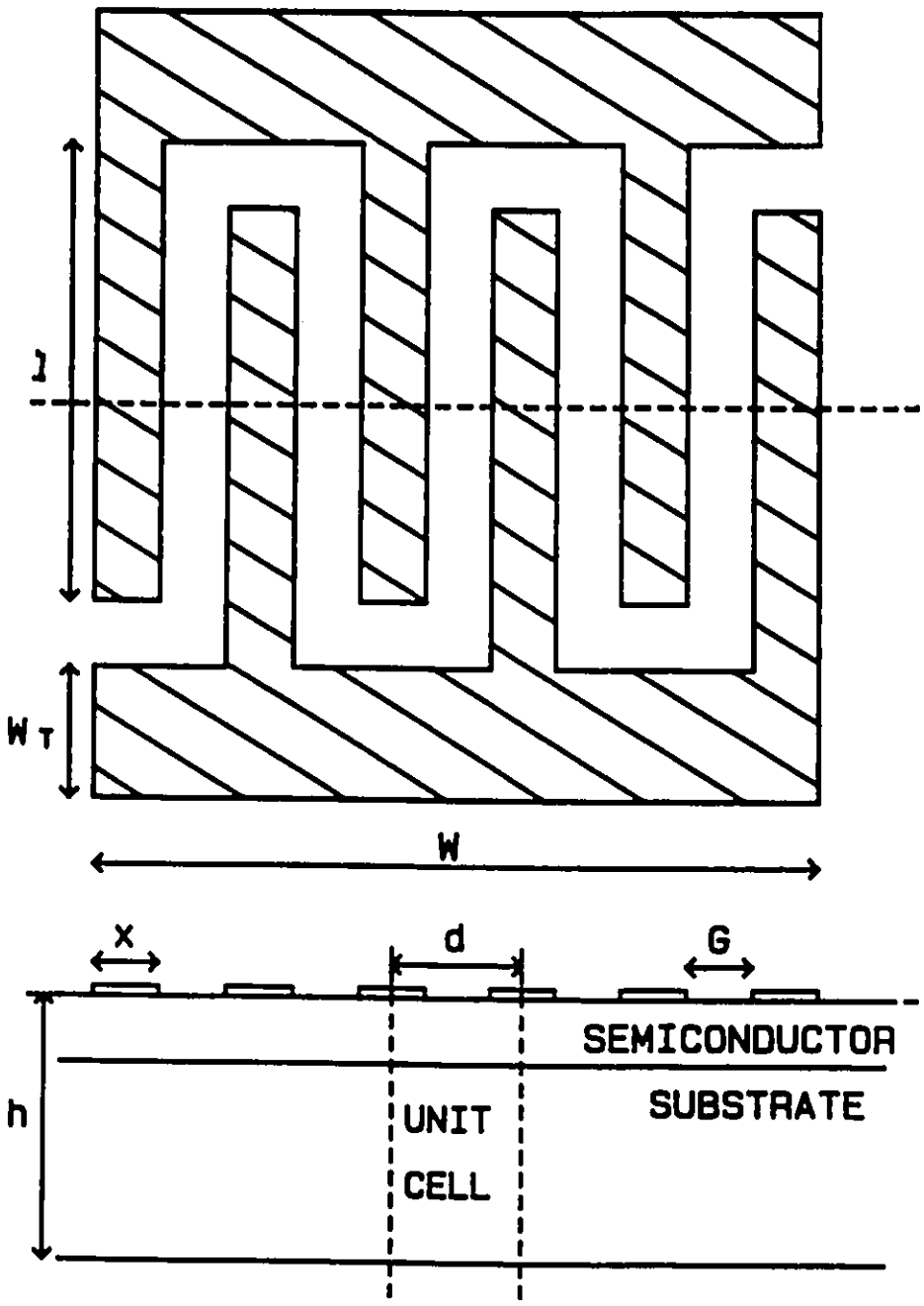


Figure 1.1 Typical layout of an interdigital diode.

Boltzmann's equation.

(1.7) $$n = n_0 \exp (q\psi / kT)$$

where n_0 is the thermal equilibrium carrier density

q is the elementary charge

k is Boltzmann's constant, and

T is the absolute temperature.

These simplifying assumptions uncouple Poisson's equation from the continuity equations and produce a single differential equation to be solved, thereby permitting the implementation of a fast and simple program to solve the potential distribution.

The potential distribution solution has several uses. These include qualitative and quantitative analysis of the electric field distribution, an important parameter in photodetector operation. Also, the spatial charge distribution can be calculated using Gauss's law. By finding the change in charge distribution due to a small change in voltage, the capacitance is simply calculated.

The potential distribution combined with the majority carrier distribution calculated using Boltzmann's equation also acts as the initial guess for the complete steady state solution calculated by the steady state routine. The steady state routine uses all of the basic semiconductor equations to solve for the potential distribution and the electron and hole concentrations (n and p respectively) in a self consistent manner. The steady state solution allows for the effects of current flow as well as generation and recombination and is obtained by setting the time derivatives in the continuity equations to zero.

The validity of the approximations used in the potential routine can be

tested by comparing its solutions with the solutions obtained from the more exact steady state routine. A sample comparison in figure 1.2 shows equipotential plots obtained from both routines. A qualitative comparison of these two plots shows no apparent differences. A quantitative comparison of the two solutions yields a maximum voltage difference of less than one part in 5×10^{-6} of the applied voltage and a maximum electric field difference of less than one part in 3×10^{-4}. This agreement is very good.

The average electron densities as a function of position as calculated by the steady state routine, and by the potential routine using Boltzmann's equation are compared in figure 1.3. Agreement is good in the low field region, but poor in the high field region due to thermal generation of carriers in the depleted semiconductor. Thermal generation is neglected in the potential solving routine, but the effect is small in absolute terms. The largest change on the grid is less than 0.00025 of the doping density.

The examples shown in figures 1.2 and 1.3 illustrated only one particular case, but are representative of all cases tested. The results of these comparisons attest to the validity of the approximations used in the potential routine and illustrate the accuracy of the resulting potential calculation when applied to interdigital Schottky diode structures.

The steady state program is principally used to calculate the initial conditions for the time dependent calculation. Unlike the potential routine which provided an initial guess for the steady state solution, the output of the steady state routine is the $t = 0$ starting point for the time dependent calculation. Thus, the convergence criterion should be as good as, or better than that desired in the time dependent routine. The steady state routine is also used to model the D.C. spatial

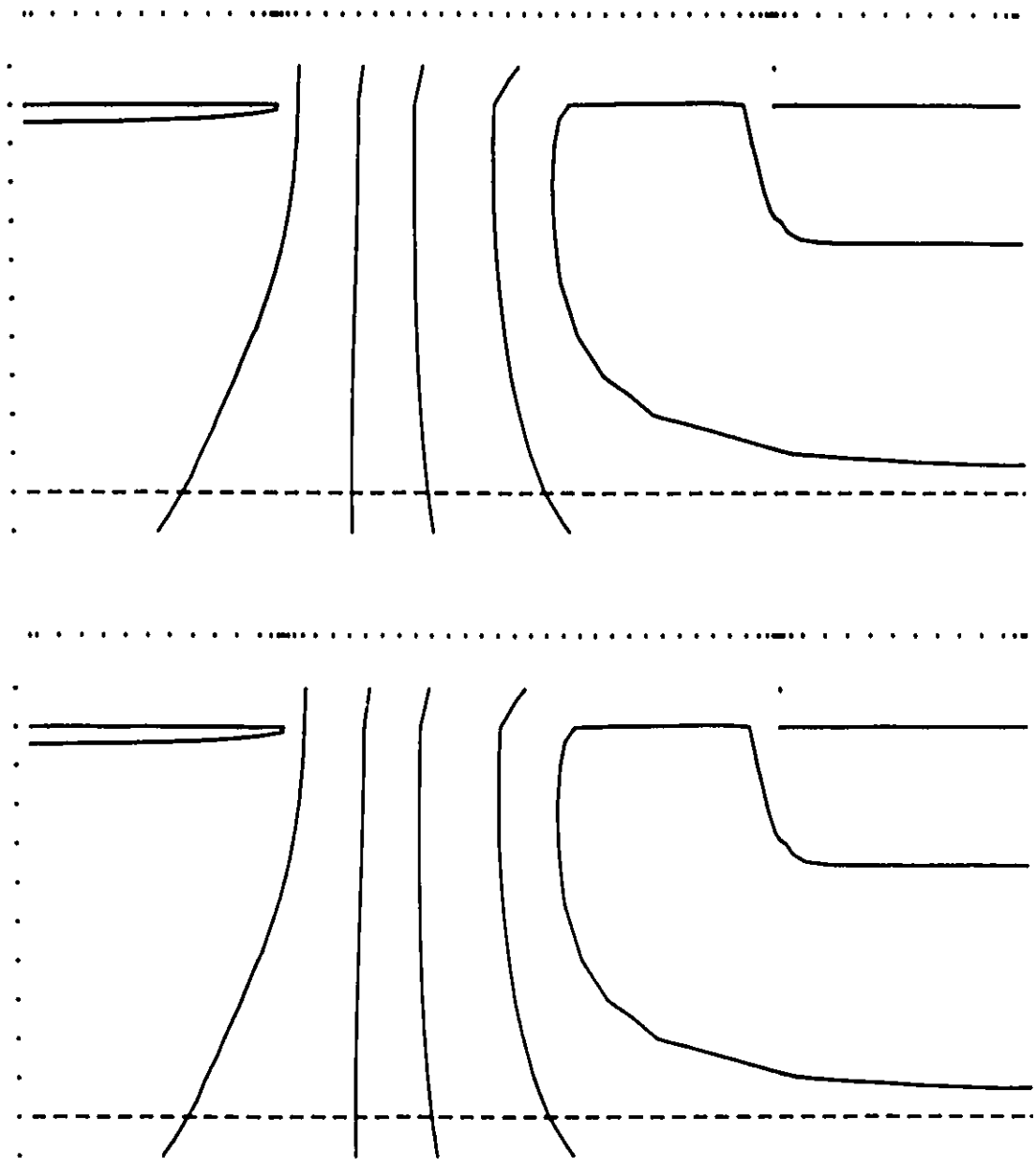


Figure 1.2 Comparison of equipotential plots obtained using the potential routine (top) and the steady state routine (bottom).

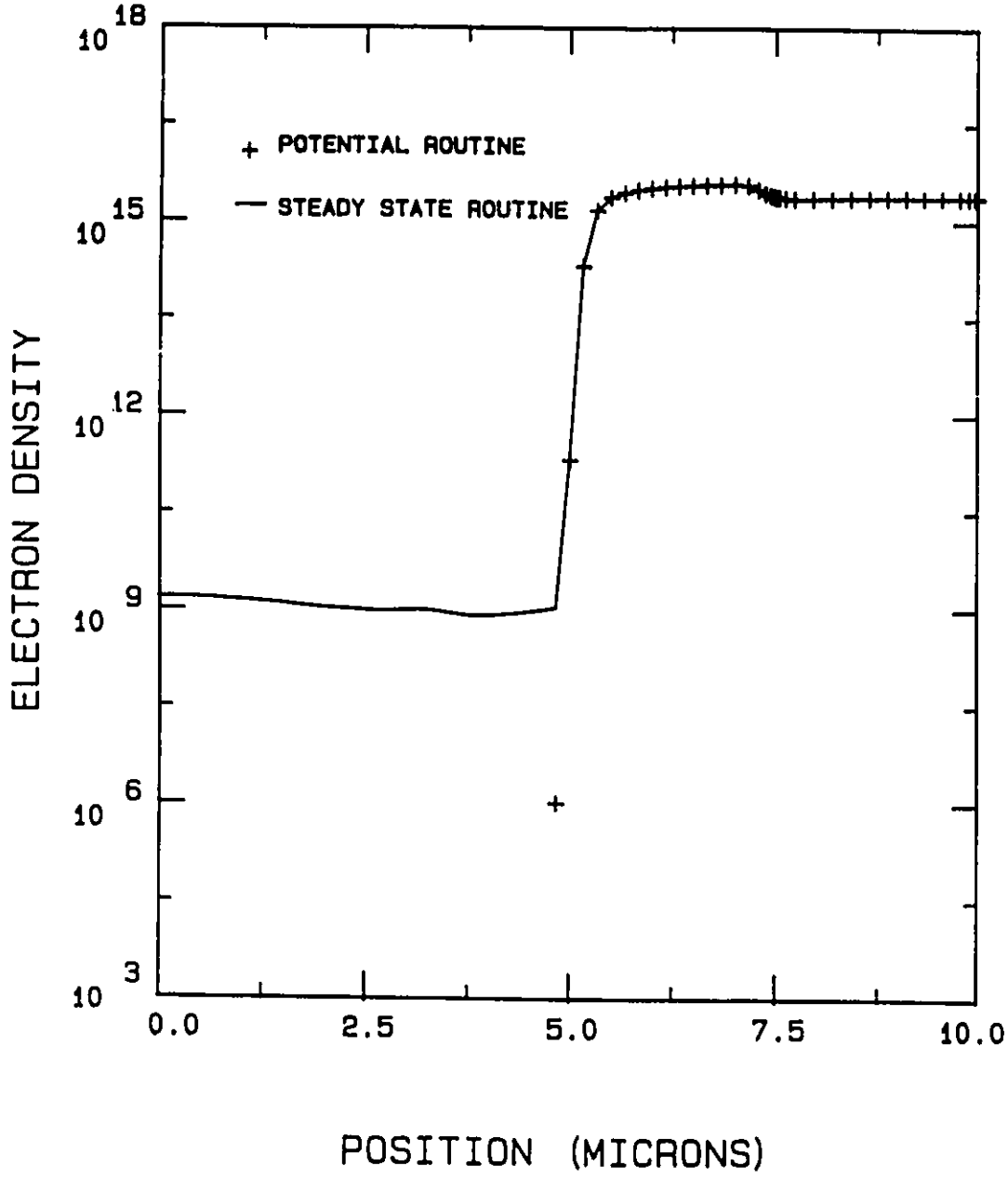


Figure 1.3 Comparison of the average electron density calculated using Boltzmann's equation and the steady state routine.

response of silicon – on – sapphire devices. This calculation involved solving the photocurrent for a Gaussian shaped spot of light incident on the semiconductor as a function of the incident spot position.

The final section of the model is a complete time dependent calculation. This program solves equations 1.1 through 1.6 as a function of time. Generally the output is current as a function of time for a user specified temporal optical generation rate.

This numerical model has two principal uses. The first involves the study of device operation. It is possible to obtain parameter values from the model which are difficult or impossible to measure directly. Understanding of how the device operates can be simplified in this way. The second use involves predicting the device performance. The ultimate aim in producing a semiconductor device is to meet a set of design criteria. Use of this model will allow the performance to be optimized before the manufacturing stage.

CHAPTER 2: STEADY STATE CHARACTERISTICS

Interdigital diodes were manufactured on three sample materials; Semi–insulating GaAs, epi–layer GaAs, and silicon – on – sapphire (SOS). These materials represent a variety of the options available for interdigital device design. To allow effective device modeling, basic knowledge of the appropriate semiconductor parameters is required. A brief description of the materials used is followed by a discussion of some of the steady state characteristics of interdigital photodiodes. Both modeling and experimental results are presented.

GaAs and related alloy materials such as InGaAs and AlGaAs are favoured material for use in opto – electronic integrated circuits. Semi–insulating GaAs has the advantage of being simple, readily available, and relatively inexpensive. Wafers were purchased from Cominco Inc.. They were nominally undoped, with a sheet resistance of $5x10^8$ ohm/□ and a mobility of $6x10^3$ cm^2/volt–sec.

Epitaxial GaAs on GaAs can be obtained with almost any specified doping profile. This gives the designer a great degree of freedom in specifying material properties, but the increased complexity generally results in significant increase in cost. A standard $n/n^-/i$ VPE wafer was purchased from Sumitomo Electric as an example of an epi–layer GaAs substrate. The nominal properties were as follows. The top layer was 0.58 μm thick and was S doped n–type to $1.8x10^{17}$ cm^{-3}. The middle layer was 3 to 4 microns thick, undoped and was n–type with a doping density less than 10^{14} cm^{-3}. The substrate was a 409 μm thick semi–insulating CrO doped wafer with a resistivity greater than 10^7 ohm–cm. This material was prepared for use by etching off the top layer using a timed (approximately 4

minutes) 1% Br:CH_3OH etch resulting in a thin low doped n^- layer on a semi–insulating substrate.

Silicon – on – sapphire (SOS) is a commercially available semiconductor – on – insulator material. SOS has been extensively discussed in the literature, and uses silicon processing techniques which are well understood. SOS wafers were purchased from Union Carbide. The silicon was nominally a 1 μm thick n–type film with a resistivity between 12 ohm–cm and 50 ohm–cm and a carrier concentration between 10^{15} cm^{-3} and $3x10^{14}$ cm^{-3}.

Thickness of the silicon film was experimentally determined using a Taly Surf 4 mechanical step profiler as well as optical interference measurements. The results were 0.96 ± .10 μm and 1.0 ± .1 μm respectively. 1.0 μm was used as the thickness in all calculations.

Electrical characteristics of the silicon film in SOS can not easily be determined due to poorly defined material properties, particularly close to the silicon – sapphire interface. Properties such as electron density and mobilities are known to be functions of distance from the silicon – sapphire interface, and are influenced by the significant concentration of deep impurity and trap states which exist near the interface. Although various authors have presented methods of measuring these parameters, their methods are beyond the scope of this thesis (see for example Dumin 1970, Hsu 1978, Chen 1981, Grivitskas 1984).

Lack of information about the distribution of charge in the SOS film makes exact modeling difficult. However, it is possible to obtain good results using reasonable approximations. One of the principal factors which limit the response time of a photodiode is the transit time of photogenerated carriers across the depletion region of the semiconductor. The depletion region is defined as that

region where the electric field is large enough to remove or deplete the free charge carriers. Transit time is limited by the width of the depletion region and the magnitude of the electric field in the depletion region. By using an appropriate average doping density in the silicon film, a good approximation of the depletion width and electric field distribution can be obtained. This permits a meaningful time dependent calculation to be made.

Use of an average doping density allows the effects of trap states on depletion width to be neglected, but the interaction of the trap states with the charge carriers is also neglected. This is justified for SOS by the exponential decrease in mobility at the silicon – sapphire interface where the majority of the traps are located (Hsu 1978). The very small mobility and poor material quality in the region containing the bulk of the traps means the contribution of carriers in this region to the fast time response is negligible.

As a first step in obtaining average values for film characteristics, Hall effect measurements were made on the SOS film. Cullen (1978) points out that Hall effect results on SOS must be interpreted with care due to the influence of charges trapped at the silicon – sapphire and silicon – silicon dioxide interfaces which can deplete the silicon of charge carriers. This effect is most pronounced in thin (< 1 μm), low carrier concentration ($< 10^{16}$ cm^{-3}) silicon which is precisely the region of interest for detector fabrication. As a result, only general conclusions will be drawn from the Hall effect results.

The temperature dependence of the average electron density measured by the Hall effect is shown in figure 2.1. At room temperature the average electron density was measured as $(5 \pm 1)\text{x}10^{14}$ cm^{-3} and the mobility was measured as 400 ± 10 cm/V–sec. The strong dependence of electron density on temperature near

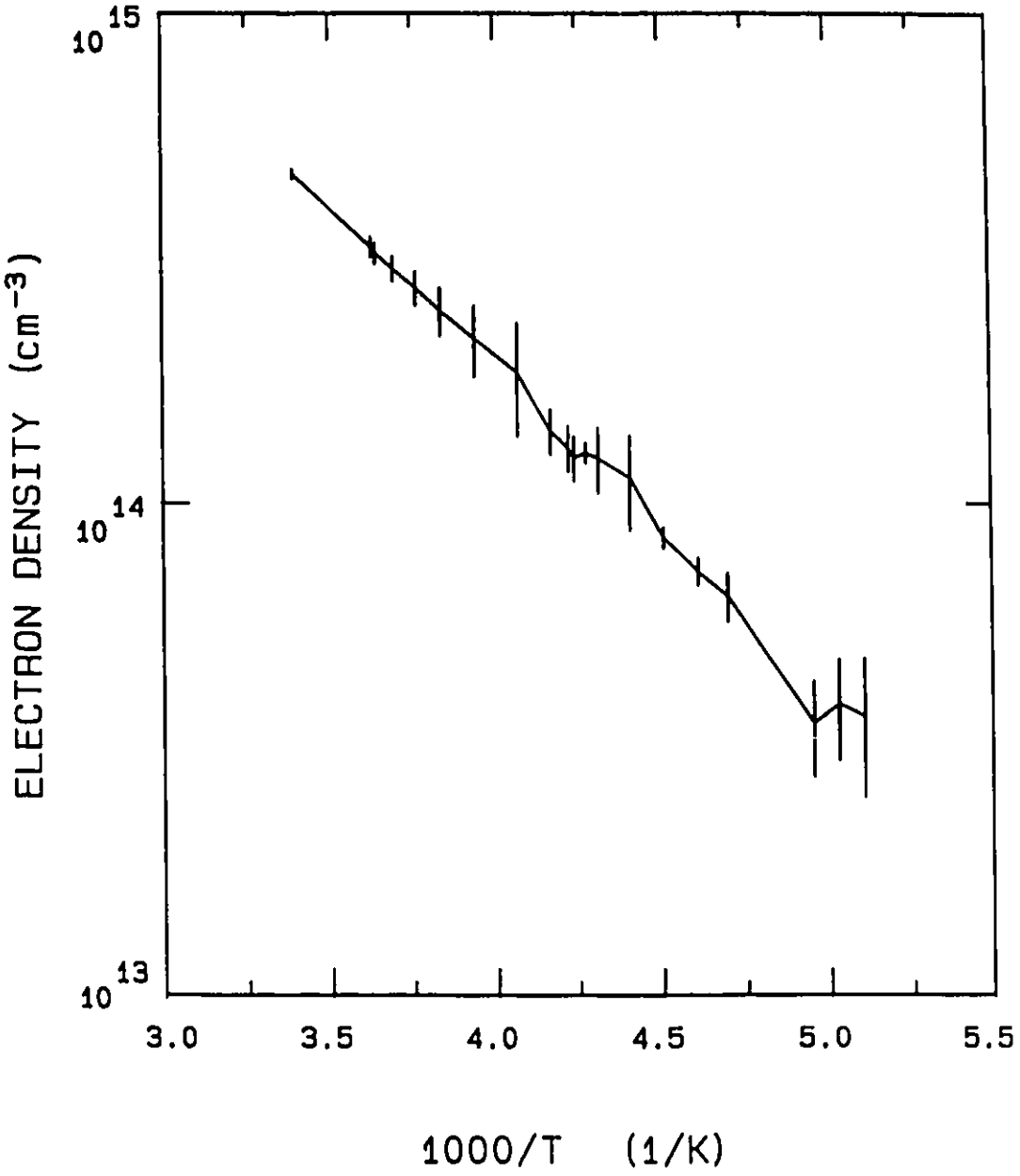


Figure 2.1 Temperature dependence of average electron density in SOS films measured using the Hall effect.

room temperature supports the existence of deep impurity levels and trap states in the silicon film. Thus the relatively small average carrier concentration measured indicates only that the average doping density is small enough ($< 10^{16}$ cm^{-3}) that the carrier concentration will be affected by the trapped charge.

Since the primary objective of finding an average doping density is to obtain a good approximation of the depletion width, an experiment to measure the depletion width of interdigital photodiodes was devised. (Details on the processing techniques used to manufacture interdigital photodiodes can be found in appendix A2.) This experiment involved scanning a small spot of light between the digits and measuring the photoresponse as a function of position. If the collection efficiency of photogenerated electron – hole pairs in the depletion region is sufficiently larger than the collection efficiency of photogenerated electron – hole pairs in the undepleted region, then the depletion region can be delineated by this measurement.

To validate the scanning experiment as a method of measuring depletion width in SOS interdigital photodiodes, the photoresponse as a function of position was simulated using the steady state routine. Figure 2.2 shows the predicted spatial dependence of the photocurrent for two values of carrier lifetime. The longer carrier lifetime, $\tau = 10^{-6}$ sec, is consistent with values found in high quality crystalline silicon and results in a significant photocurrent from the undepleted region due to carrier diffusion. The short carrier lifetime, $\tau = 4x10^{-10}$ sec, will be shown to be a good approximation of the value expected in these SOS films. A good approximation of the average depletion width, (3.9 μm for this example), is given by the full width at half maximum (FWHM) of the curve for the short lifetime carriers. The FWHM measurement is an approximate deconvolution of a rectangular window representing the depletion region from a scanned Gaussian light spot. (The actual

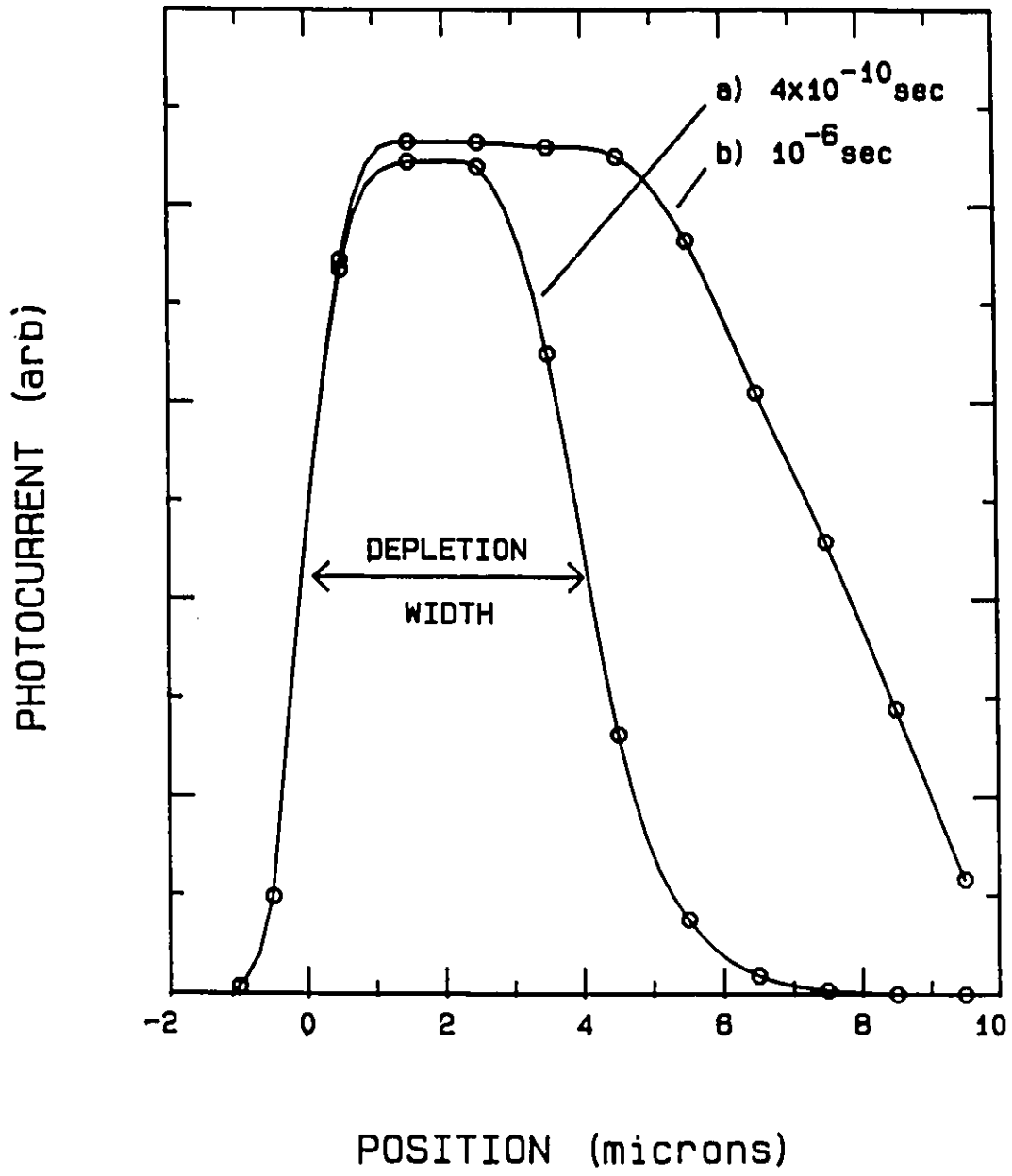


Figure 2.2 Predicted spatial dependence of photocurrent for a carrier lifetime of (a) $4x10^{-10}$ sec (b) 10^{-6} sec, (spot size 1.0 microns, reverse bias digit edge located at 0).

depletion region is assumed to start when the electron density has fallen to e^{-1} of its equilibrium value. This represents a convenient measure since the electron density decreases by several orders of magnitude in a very short distance beyond this point.)

To justify the short carrier lifetime used in these calculations, the photoresponse of the depleted and undepleted regions of an interdigital photodiode was measured. The output of a fast laser diode (FWHM = 70 psec) was focused near the reverse biased digit (on the depletion region) and then near the forward biased digit (on the undepleted region) when the device was approximately half depleted. The observed response for these two cases is shown in figure 2.3. The response in the depleted region is very fast as expected. In the undepleted region, the response is relatively slow and much smaller (signal averaging was used, and the vertical scale multiplied by approximately two orders of magnitude) as anticipated for diffusion dominated photoresponse (the initial fast signal arises through a small fraction of the light pulse which directly illuminates the depletion region). Measuring the decay time of this pulse yields a carrier lifetime of 400 ± 50 psec, which is consistent with the value of average carrier lifetime of 410 psec measured by Grivitskas (1984) for a 1 μm thick SOS film.

The experiment to measure the depletion width in SOS was performed as follows. A tightly focused laser beam (having a beam diameter of 1 to 2 microns) was incident on the device which is mechanically scanned across the beam. To measure the distance travelled accurately and to eliminate any nonlinear effects in the drive system, an interferometer was used. The system is illustrated in figure 2.4. The diode under study was mounted directly on the moving mirror mount of a Michelson interferometer, with the surface parallel to the direction of movement and the digits perpendicular to the direction of movement. (The angle of the device was

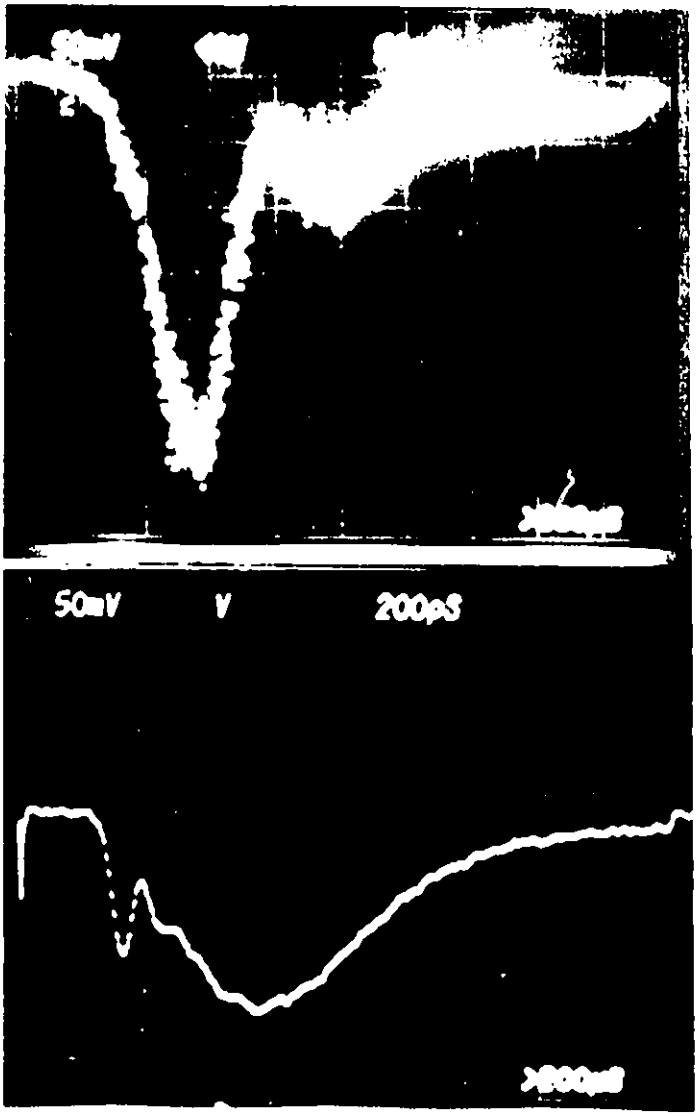


Figure 2.3 Pulse response of the (top) depleted region, and (bottom) undepleted region of an interdigital detector on SOS.

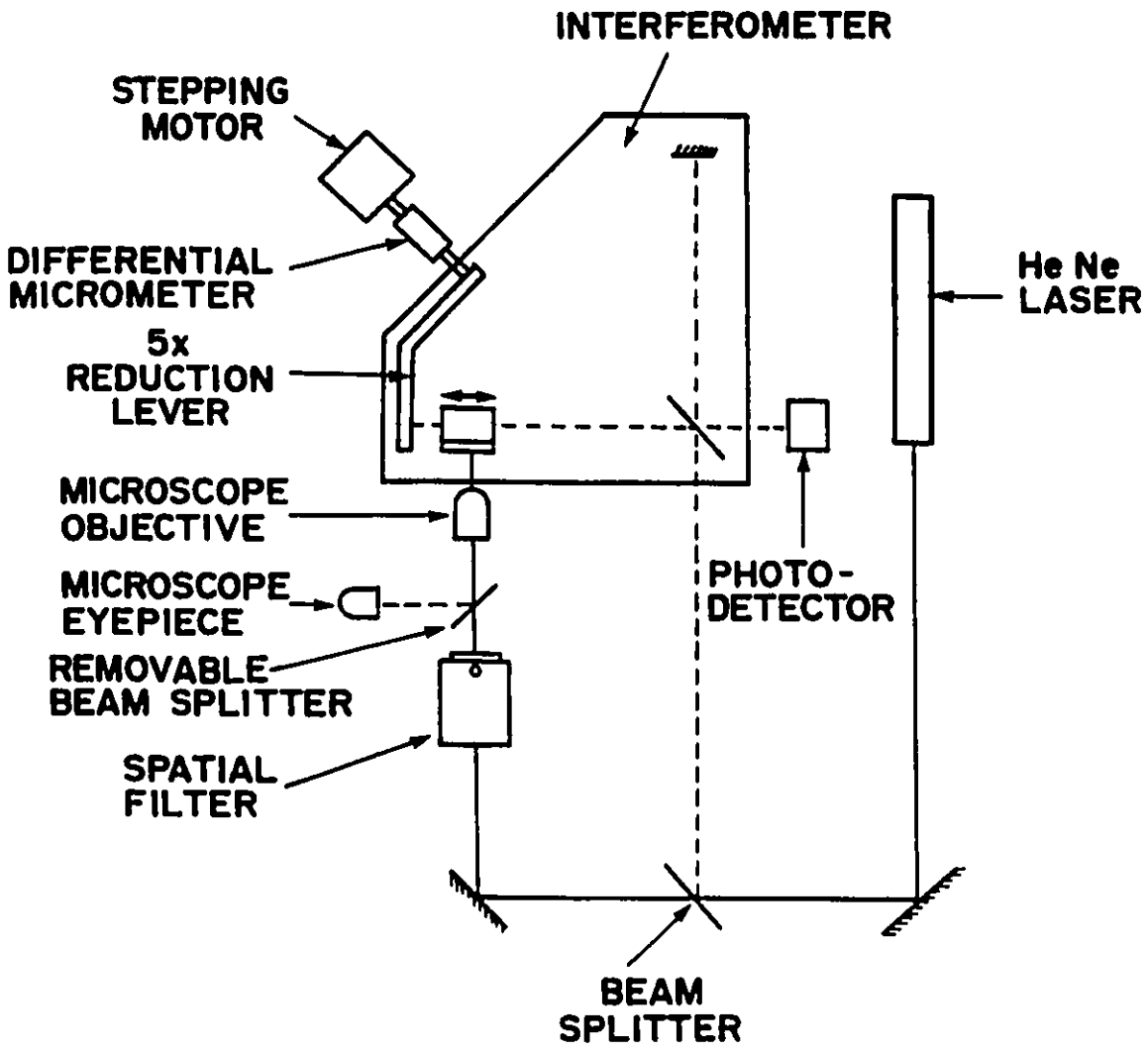


Figure 2.4 Experimental setup used to measure photocurrent as a function of position.

set by reflecting the laser beam from the diode surface and aligning the interference pattern from the digits). The mirror and the diode were driven through a 5 times reduction lever by a differential micrometer (50 μm/rev) which was rotated by a stepping motor. The distance travelled by the mirror, and thus the diode, is accurately measured by recording the fringes at the output of the interferometer using an auxiliary photodetector. Each fringe is indicated by a valley on the recorded output and represents a distance traveled of one half wavelength of the light incident on the interferometer. In this experiment a He–Ne laser with a wavelength of 632.8 nm was used.

The scanning beam was passed through a spatial filter – beam expander to improve the spatial coherence, and then through a microscope objective to be focused down to a very small spot on the diode. A removable beam splitter was placed in the beam to reflect light scattered back through the objective to a microscope eye piece to allow visual alignment. (The beam was attenuated for safety during this procedure.) During scanning, the photocurrent of the device being measured and the output from the interferometer were recorded on a dual trace chart recorder. Samples of the output of this experiment are shown in figures 2.5 and 2.6. Distances on the scans are measured by counting the number of peaks (or valleys) on the interferometer output and interpolating as required.

Figures 2.5 and 2.6 represent sample scans of interdigital device on SOS and bulk single crystal silicon respectively. The shape of these curves can be compared with the modeled results of figure 2.2. The scan on bulk silicon shows characteristics which are consistent with those shown by the long lifetime material, as expected. The scan on SOS shows the same rapid decrease in photocurrent at the depletion edge as demonstrated by the short lifetime calculation. As a result, it is

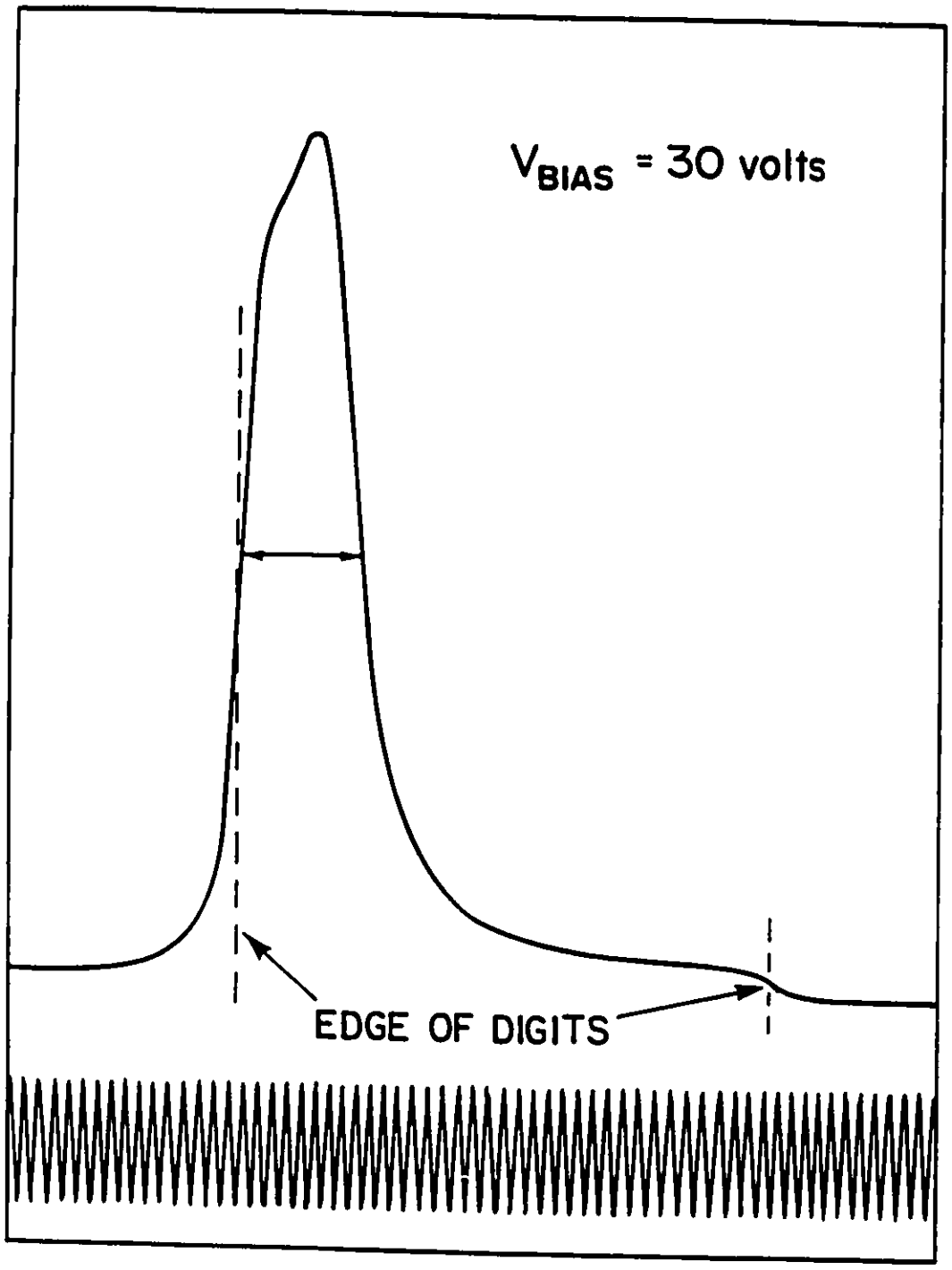


Figure 2.5 Sample scan between two digits on SOS.

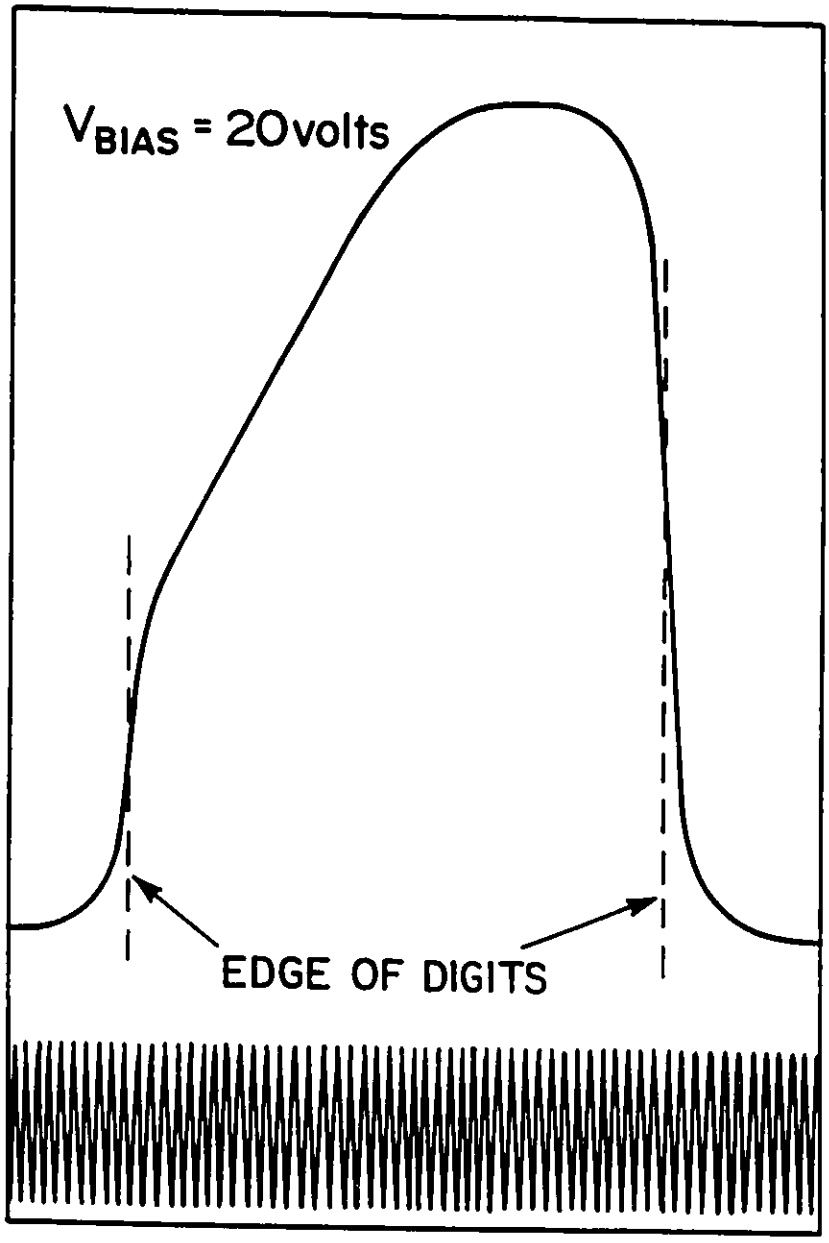


Figure 2.6 Sample scan between two digits on bulk single crystal silicon.

reasonable to expect that a good approximation of the average depletion width of SOS interdigital photodiodes can be obtained by measuring the FWHM of the scanning curve.

Values of depletion width as a function of bias voltage obtained from this experimental setup are shown in figure 2.7. Also shown are results obtained using the potential solving model with a doping density of $N_d = 5x10^{15}$ cm^{-3}. The agreement between experimental and theoretical results is good. Figure 2.7 depicts the results of measurements on a single device. Measurements on other devices yielded similar results, but the doping density used to obtain the best theoretical fit varied from sample to sample due to variations in material properties across the substrate. The average doping density from these measurements was $(5 \pm 2) \times 10^{15}$ cm^{-3}. This value of doping density is consistent with the Hall effect data presented earlier and was used in all time dependent calculations on SOS.

D.C. photoresponse measurements as a function of wavelength give an indication of the wavelength range over which a devices can be expected to operate. Figures 2.8 and 2.9 show typical measurements of the responsivity of interdigital photodiodes on semi – insulating and epi – layer GaAs, and SOS devices respectively. These results can be understood approximately using the following simple model. The responsivity is the ratio of the photocurrent to the incident optical power, and is given by

$$R = \frac{\eta \ \lambda}{1.24} \text{ amps/watt} \tag{2.1}$$

where η is the quantum efficiency, and

λ is the wavelength in μm.

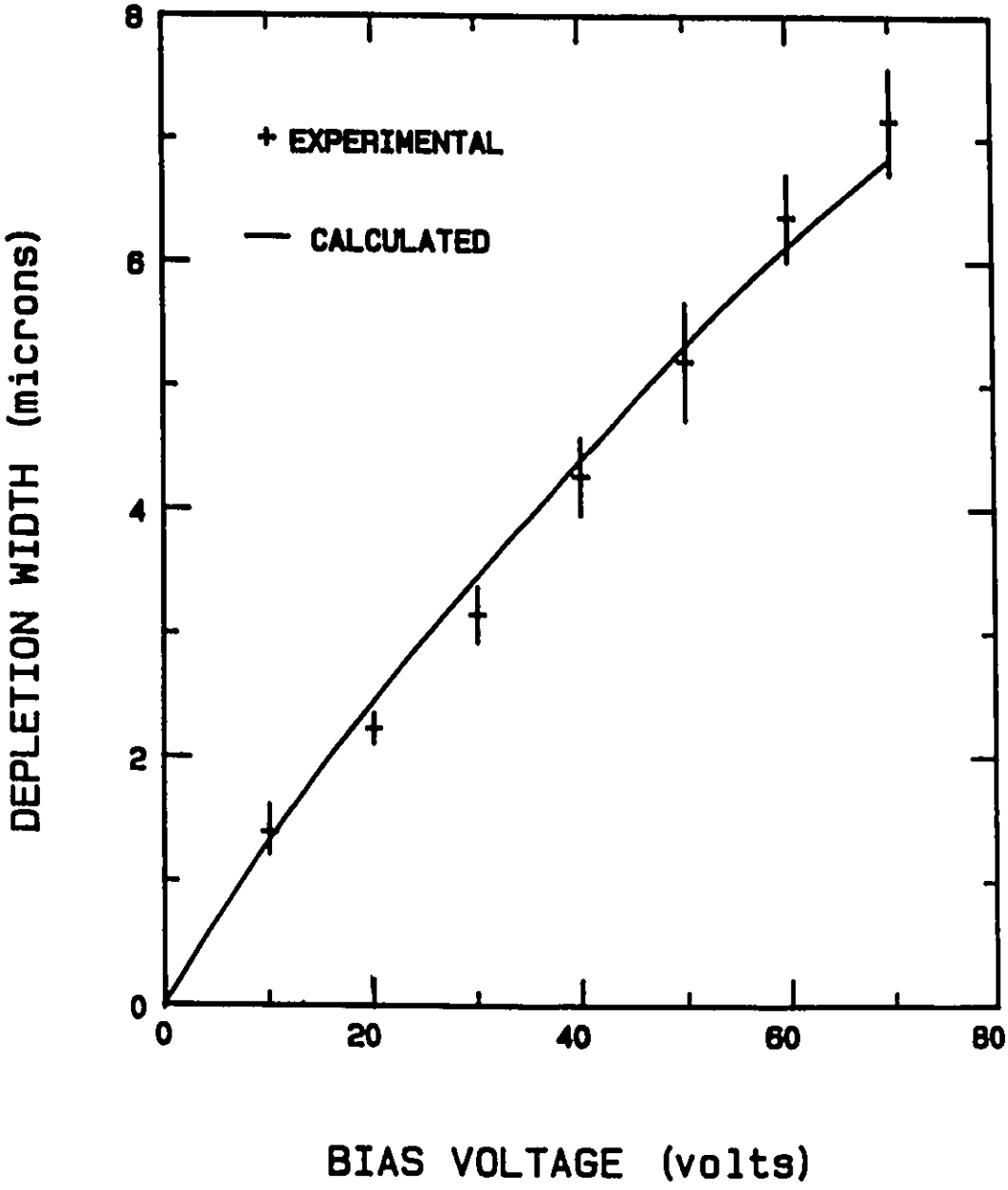


Figure 2.7 Variation of the average depletion width as a function of bias voltage.

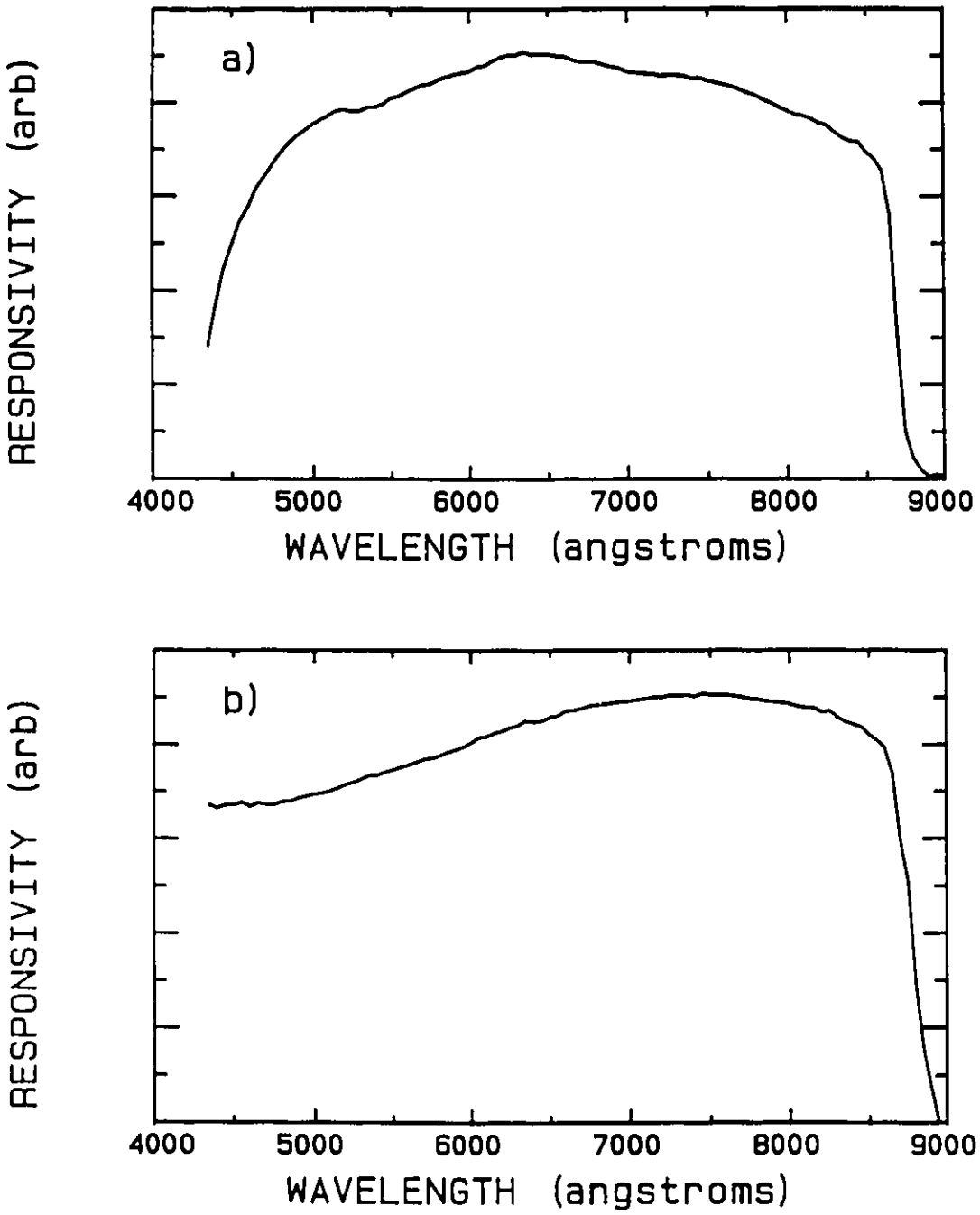


Figure 2.8 Normalized responsivity for interdigital diodes on (a) semi – insulating GaAs, (b) epi – layer GaAs.

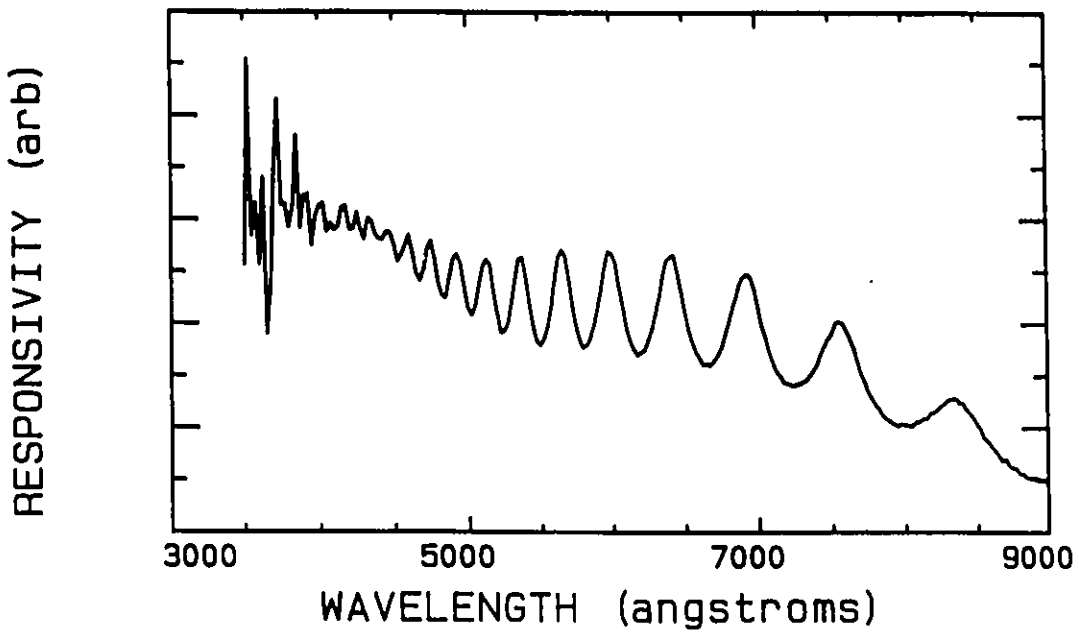


Figure 2.9 Normalized responsivity for interdigital diodes on SOS.

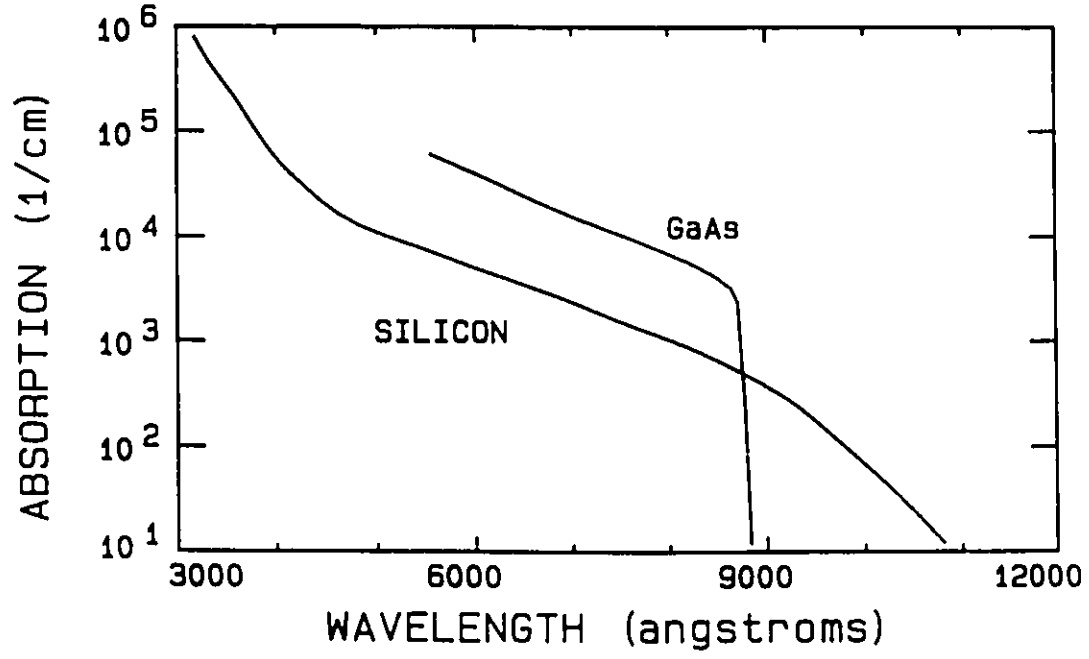


Figure 2.10 Absorption coefficients of GaAs and silicon.

The quantum efficiency is the ratio of collected charge carriers to the number of incident photons. It depends on the fraction of the light entering the semiconductor which is absorbed and can be expressed as

$$\eta \propto (1 - \exp(-\alpha t)) \tag{2.2}$$

where α is the absorption coefficient, and
t is the thickness of the absorbing region.

The absorption coefficients for GaAs and silicon are presented in figure 2.10.

Devices manufactured on semi – insulating and epi – layer GaAs show similar response characteristics. For wavelengths where the photon energy is greater than the semiconductor band energy (band edge) the absorption coefficient is very small, so that almost no light is absorbed and the responsivity is effectively zero. At the band edge, the absorption coefficient increases quickly producing a corresponding increase in responsivity. Below the band edge, the absorption coefficient is large enough that the majority of the light entering the semiconductor is absorbed within a micron of the top surface, well within the active region of the photodetector. As a result the responsivity shows only slow variation. Below 5000 Å the semi – insulating GaAs response falls off quickly unlike the epi – layer GaAs. This is probably due to increased surface recombination as a greater portion of the light is absorbed close to the surface with increasing absorption. Increased surface recombination is consistent with a roughness of the semi – insulating GaAs surface which developed during processing. It is interesting to note that the responsivity

curve for semi – insulating GaAs is similar to the equivalent curve for a junction diode on GaAs. The responsivity of a junction diode shows a similar short wavelength fall off due to the absorption of the majority of the input light in the thin top layer of the junction and recombining before it is collected (Garside 1982).

The responsivity of the SOS device illustrated in figure 2.9 shows Fabry–Perot fringes due to multiple reflections of the light through the thin silicon film. These fringes disappear at about 4500 Å where the absorption coefficient is large enough to absorb approximately 95 % of the incident light on the first pass through the silicon. The noise in the signal below this wavelength is due to small probe light source intensity below 4500 Å. A steady increase in average responsivity as wavelength decreases is shown in figure 2.9. This is due to an increased percentage of the input light being absorbed in the thin silicon film as the absorption coefficient increases.

The measurement of steady state responsivity of interdigital photodiodes as a function of wavelength shows that the relative responsivity can be understood using simple absorption considerations. These results also show that, in general, the responsivity of interdigital photodiodes remains good in regions of very large absorption such as the near UV where junction photodiodes generally show a sharp reduction in responsivity.

For the semi – insulating GaAs the thickness of the absorbing layer is equal to the thickness of the substrate, unlike the other two materials used in this thesis where the absorbing layer is limited to a thin semiconductor region. Using equation 2.2, the majority of the light is absorbed in a region approximately 1 μm thick for most wavelengths of interest. Thus, to make best use of computer resources, semi – insulating GaAs was modeled as a layer of semiconducting GaAs

about 1 μm thick on an insulating substrate of GaAs.

Absolute responsivity measurements were made on the GaAs devices at a wavelength of 6328 Å. Figure 2.11 shows a responsivity versus bias voltage curve of an epi–layer interdigital device. All GaAs devices yielded similar curves, but the absolute values varied significantly from device to device. Typical values at 10 volts were on the order of 0.51 amps/watt, which represents an external quantum efficiency of 100 %. A simple calculation including losses of 50% due to blockage of incident light by the metal digits, and a further 30% due to reflection of incident light from the GaAs surface results in an internal quantum efficiency much larger than 100% indicating the existence of a low frequency internal gain mechanism. This is further suggested by the continuous increase and slight upward curve of the responsivity at larger voltages in figure 2.11. Wada (1986) and others (Ito 1986, Schumacher 1988) have obtained similar results. Various suggestions have been made to account for this internal gain, but no specific mechanism has been established thus far. The variation in absolute responsivity from device to device suggests that the gain mechanism may in some way be associated with the Schottky barrier and the interface between the metal and the semiconductor since this is very sensitive to processing.

The measurement of absolute responsivity in SOS interdigital devices is complicated by the presence of Fabry – Perot fringes. Additionally, results fluctuate greatly between otherwise similar devices. Generally the results indicate peak quantum efficiencies at lower wavelengths between 10 % and 20 %. These numbers are not large enough to demonstrate the existence of a gain mechanism, but the lack of reproducibility of results between devices suggest a mechanism similar to that in GaAs may exist.

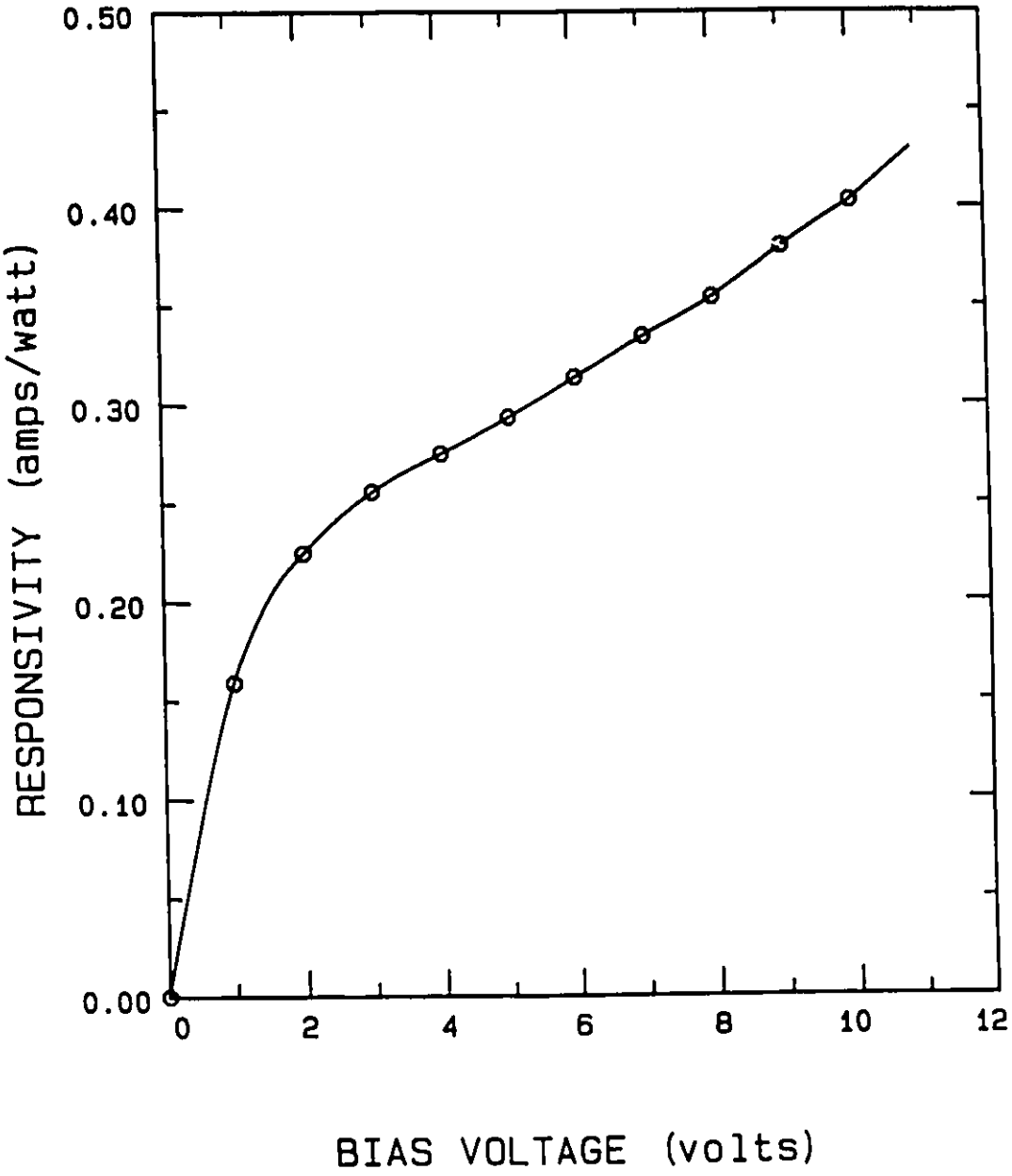


Figure 2.11 Responsivity as a function of bias voltage for an epi – layer interdigital detector.

Figure 2.12 shows a measured I–V curve of an interdigital diode. The back – to – back Schottky diode nature of the device is clearly illustrated by the overall symmetry of the curve. Note the slight asymmetry in the curves for positive and negative bias voltage arising from a different set of digits dominating the current process in each case.

The theory of current transport in one dimensional metal – semiconductor – metal (MSM) structures has been studied by Sze et. al. (1971). They have broken the operation into three distinct phases, as illustrated in figure 2.13, and presented the current equations for each phase using thermionic emission theory for Schottky barriers. Sze's notation for a symmetric MSM structure on n–type material is illustrated in figure 2.14 ($\phi_{n1} = \phi_{n2} = \phi_n$ and $V_{d1} = V_{d2} = V_d$).

In the first phase of operation the depletion regions of the two Schottky barriers are not in contact. In general the current is dominated by the emission of electrons over the reverse biased barrier. If the hole current is neglected, the current in this phase is given as;

$$J = J_{ns} \exp(\beta\, \delta\phi_{n1}) \left(1 - \exp(-\beta\, V_1) \right) \tag{2.3}$$

where $J_{ns} = A_n^* T^2 \exp(-\beta\, \phi_{n1})$ is the electron saturation current density,

A_n^* is the effective Richardson constant for electrons,

$\delta\phi_{n1}$ is the barrier lowering due to image force effect,

$\beta = q / kT$,

T is the absolute temperature and

V_1 is the applied voltage drop across the reverse bias barrier.

As the applied voltage is increased, the depletion regions of the two

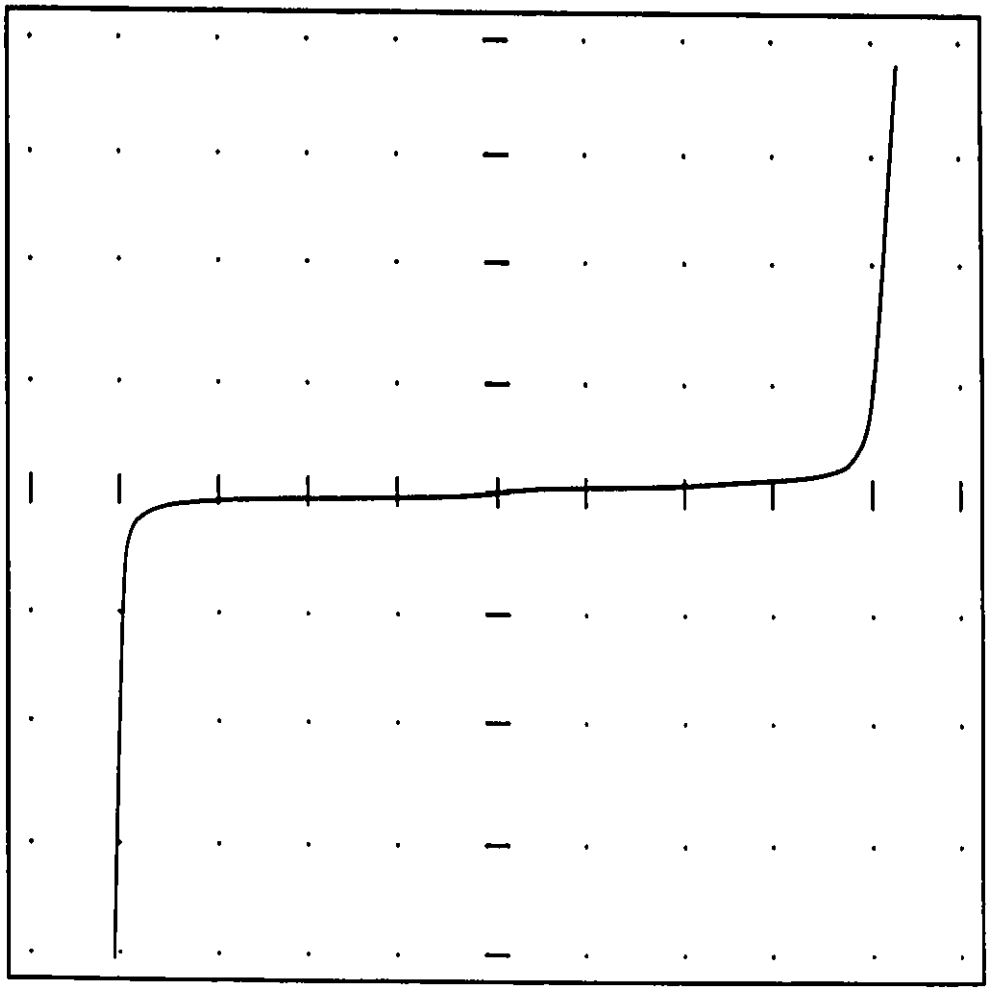


Figure 2.12 Typical I–V characteristic of an interdigital detector (vertical scale 10 μA/div, horizontal scale 30 V/div).

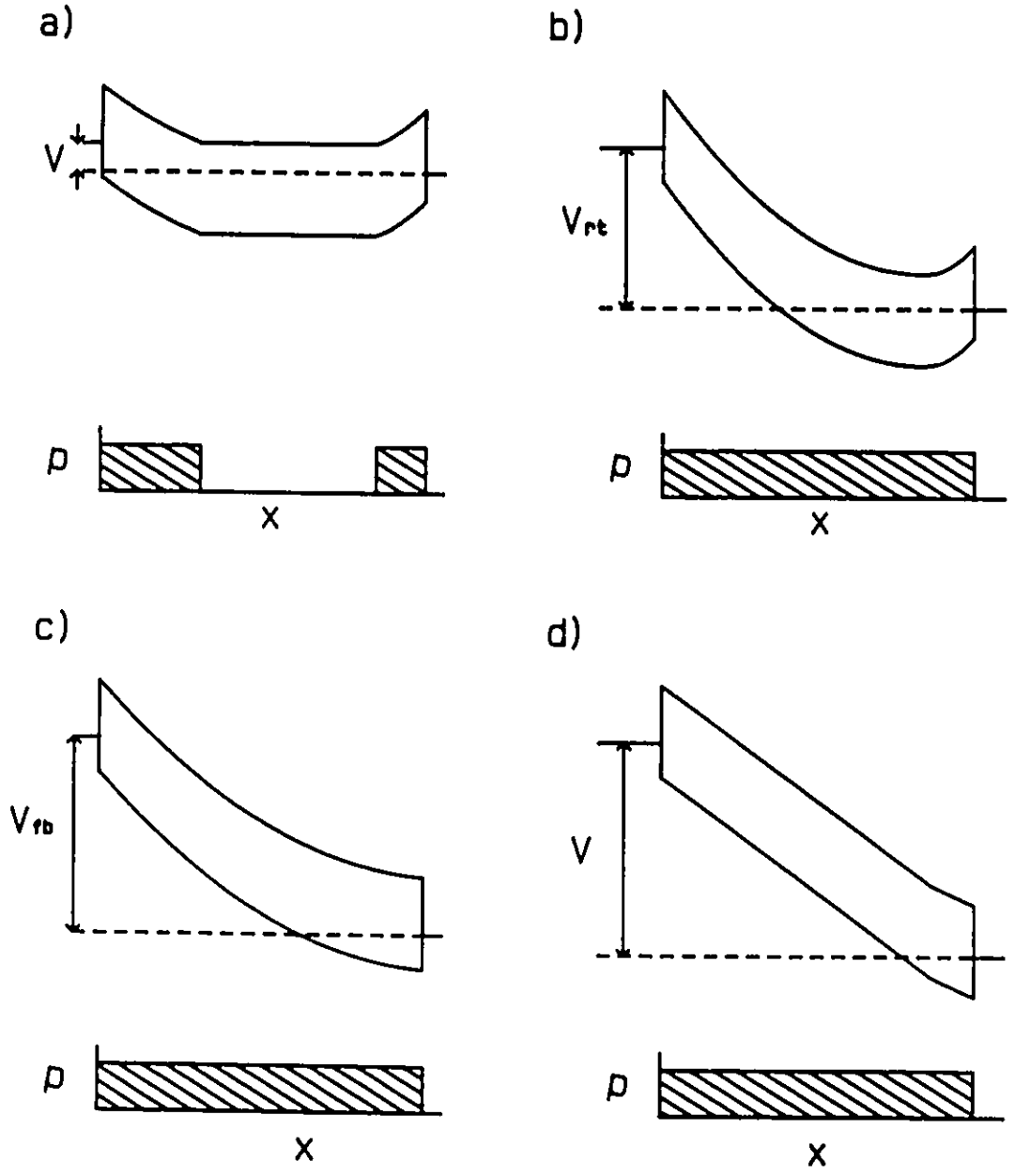


Figure 2.13 Operation phases of a one dimensional MSM device, (a) $V < V_{rt}$, depletion regions not in contact, (b) $V = V_{rt}$, depletion regions just in contact, (c) $V = V_{fb}$, the electric field at the forward bias digit equals zero. (d) $V > V_{fb}$.

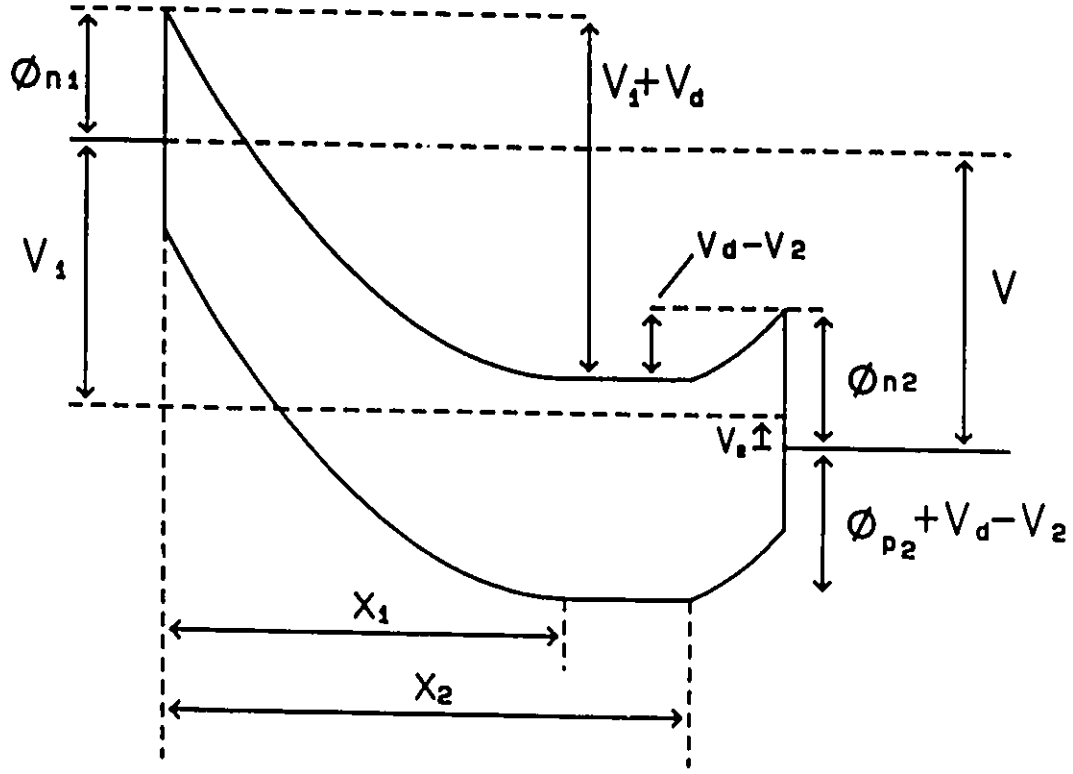


Figure 2.14 Notation used to describe a symmetric one dimensional MSM structure, ($\phi_{n1} = \phi_{n2} = \phi_n$, $V_{d1} = V_{d2} = V_d$).

Schottky barriers will come into contact. This is referred to as the reach – through voltage, and is given by;

$$(2.4) \qquad V_{rt} = \frac{q\, N_d\, L^2}{2\, \epsilon_s} - L\sqrt{\frac{2\, q\, N_d}{\epsilon_s}\,(\, V_d - V_2\,)}$$

where V_{rt} is the reach through voltage, and

L is the thickness of the semiconductor.

In the second phase of operation, increasing the applied voltage beyond V_{rt} results in the lowering of the minority carrier barrier at the forward biased contact by the field from the reverse biased contact. This causes the minority carrier current to increase rapidly as a function of increasing applied voltage.

The third phase of operation begins when the applied voltage is large enough to cause the electric field at the forward bias barrier to go to zero. This is referred to as the flat band voltage, V_{fb} where

$$(2.5) \qquad V_{fb} = \frac{q\, N_d\, L^2}{2\, \epsilon_s}$$

For bias voltages greater than the flat band voltage the electron and hole currents are given by their saturation values, with corrections for image force barrier lowering, until the avalanche breakdown field is reached. This current is given by

$$(2.6) \qquad J = J_{ns} \exp(\beta\, \delta\phi_{n1}) + J_{ps} \exp(\beta\, \delta\phi_{p2})$$

where $J_{ps} = A_p^{*}\, T^2 \exp(-\beta\, \phi_{p2})$ is the hole saturation current

The preceding discussion applies to a one dimensional device, but interdigital diodes are two dimensional devices. The nonuniformity of the electric field distribution along the digits result in nonuniform electron and hole barriers and thus nonuniform current distribution. To study this effect requires a two dimensional model. There are two fundamental models used to describe current transport in Schottky barrier contacts. The first is based on drift and diffusion in the semiconductor and uses fixed boundary conditions at the contacts. Thermionic emission theory was developed to correct some obvious problems with drift – diffusion theory. Both these models have their limitations and in fact the actual solution is generally a compromise as evidenced by the number of hybrid models in existence (Henisch 1984). Henisch also points out that these models have both been successful because in general only the coarse predictions of a model can be experimentally tested, and most models have these in common.

The steady state routine discussed in chapter 1 is a two dimensional numerical implementation of the drift – diffusion model. This model can be compared with the one dimensional thermionic emission based analytical analysis of Sze and used to study the current voltage characteristics of an interdigital device. The validity of this comparison is illustrated by comparing the results of the analytical model with a one dimensional numerical model (Levy, 1987). An example is shown in figure 2.15. Although the two models calculate different absolute values of current for any given voltage, the results are qualitatively the same. The three phases of operation discussed by Sze are clearly demonstrated by the numerical model, although the transition between phases is not as sharp. The sharp transitions in Sze's model are probably due to the approximation of an abrupt depletion edge inherent in his equations.

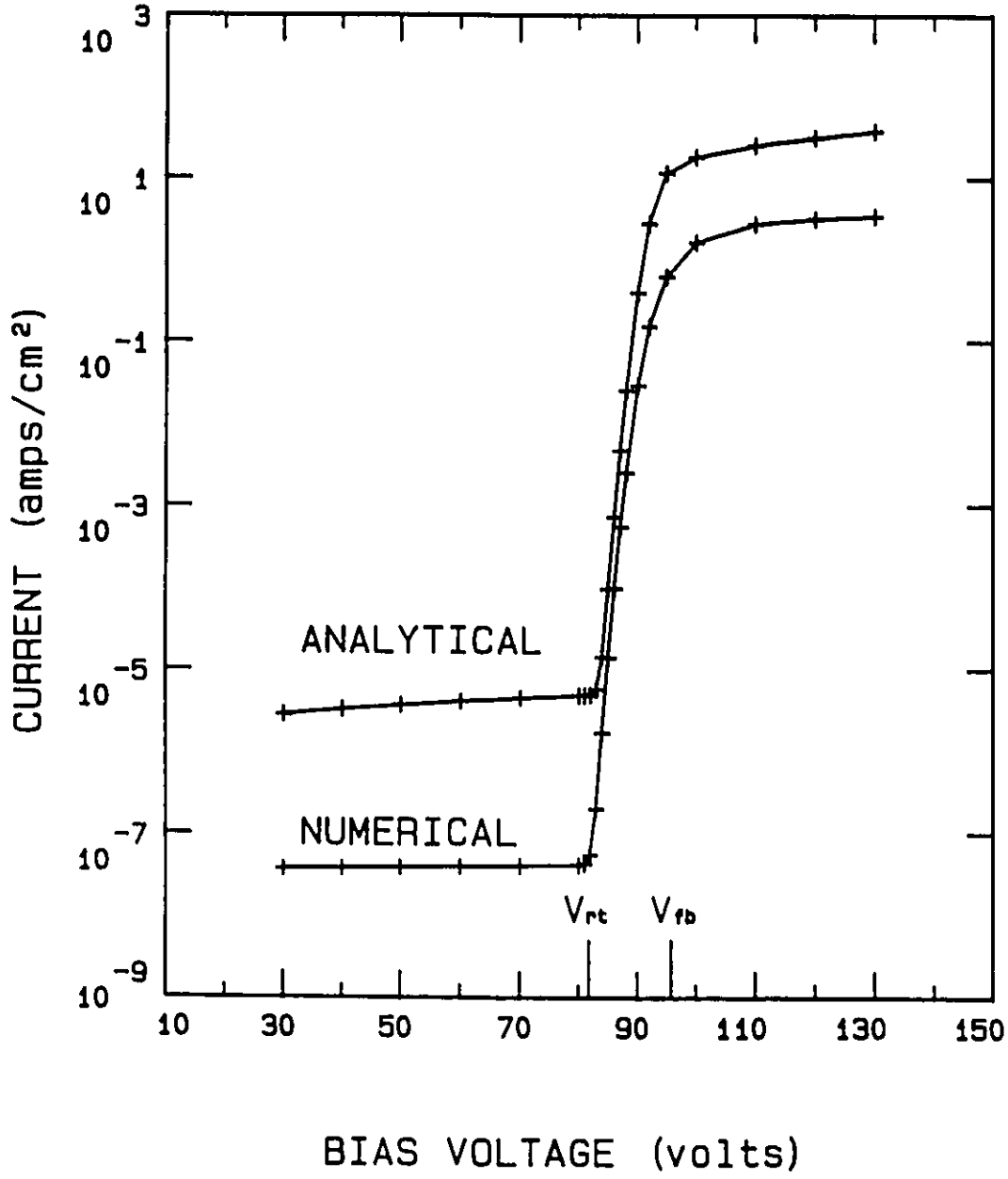


Figure 2.15 Comparison of the current calculated by the one dimensional analytical model and the one dimensional numerical model for a silicon MSM device (L = 5 μm, $N_d = 5x10^{15}$ cm^{-3}, $\phi_n = 0.8$ V).

The I–V characteristic of an equivalent interdigital device calculated using the 2–D steady state routine is shown in figure 2.16. Comparison of figure 2.16 with figure 2.15 illustrates the qualitative similarity of the results with two notable differences. Due to the two dimensional nature of the interdigital device, the transition region between V_{rt} and V_{fb} occurs at a different bias voltage. This is further illustrated in figure 2.17 which compares V_{fb} for a one dimensional silicon MSM device with a two dimensional SOS interdigital device. The values for the interdigital device were calculated iteratively using the potential solving routine. Unlike the one dimensional device curves, the interdigital device curves are not unique, but are functions of the silicon thickness and the ratio of digit width to digit separation.

The second notable difference involves the saturation of the current for $V > V_{fb}$. The interdigital device saturates very slowly due to the continued changing of the nonuniform hole barrier height across the width of the forward bias digit as the bias voltage increases.

Current in interdigital devices can thus be divided into the same three regions of operation Sze has used to describe one dimensional MSM devices. The behavior of the current in each of the three regions is qualitatively similar for both types of device. As a result, Sze's analytical expressions can be used to make general observations, but locating the bias voltages over which these regions exist in an interdigital device requires the use of a two dimensional model.

Practical interdigital devices can be divided into two groups. Those which operate at $V < V_{rt}$, and those which operate at $V > V_{rt}$. For devices operating with $V < V_{rt}$, the maximum current is given approximately by the electron saturation current of the reverse biased digit. Examination of the saturation

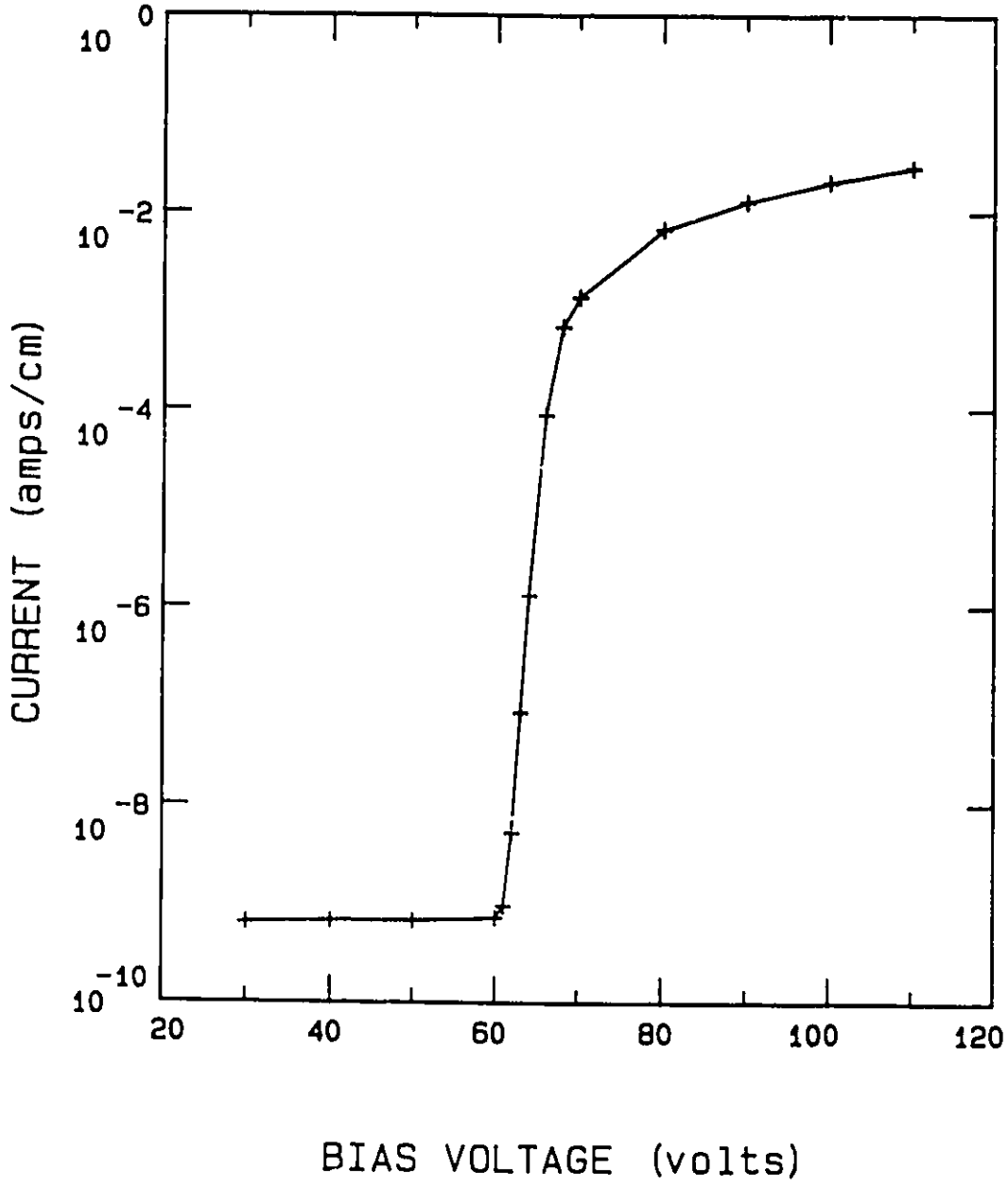


Figure 2.16 Current calculated using the two dimensional model for an interdigital MSM device on SOS (t = 1 μm, x = 5 μm, G = 5 μm, $N_d = 5 \times 10^{15}$ cm^{-3}, $\phi_n = 0.8$ V).

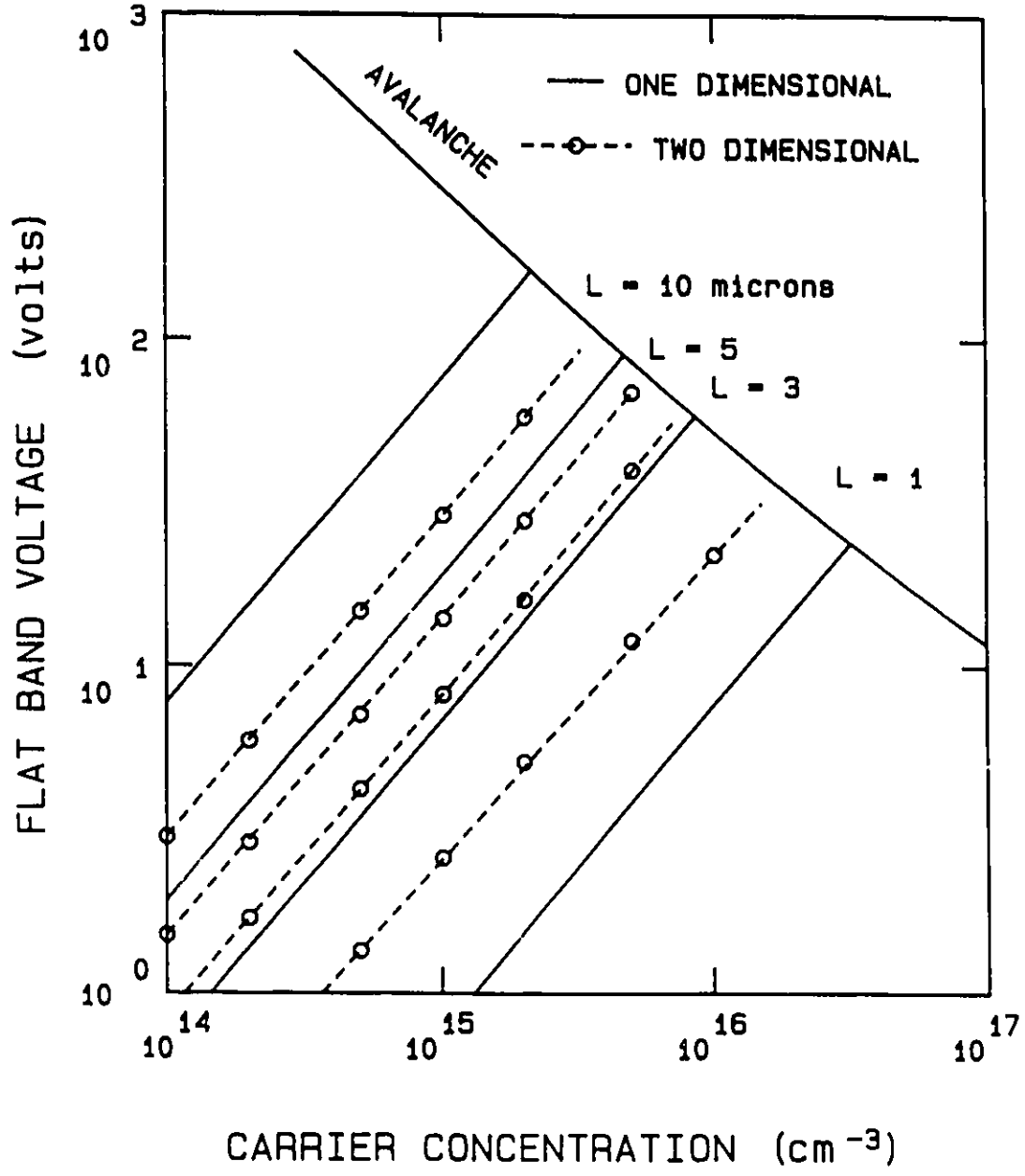


Figure 2.17 Comparison of V_{fb} calculated for a one dimensional silicon MSM device and a two dimensional SOS interdigital device for different contact separations. The limitation of avalanche breakdown is shown for the one dimensional case.

current in equation 2.3 shows the exponential dependence of the electron barrier height to be the dominant factor. Thus the dark current in such a device can be theoretically minimized with a large electron barrier height, ϕ_{n1}, as in any standard Schottky barrier device.

For interdigital diodes operating with $V > V_{rt}$, the limiting case of $V > V_{fb}$ can be considered. Equation 2.6 shows that in this region of operation the current is dominated by the larger of the electron saturation current from the reverse bias barrier or the hole saturation current from the forward bias barrier. To obtain a minimum theoretical dark current requires that both the reverse biased electron barrier, ϕ_{n1}, and the forward biased hole barrier, ϕ_{p2}, be maximized. One way of doing this is to use different metals for the forward and reverse biased barriers. This is a straight forward solution in principle, but finding metals with a large hole barrier may present a problem. It also increases the complexity of the manufacturing process.

If the same metal is used for both barriers, the best solution is a compromise between the electron and hole barrier heights. Assuming that

$$E_g = \phi_n + \phi_p \tag{2.7}$$

then to a first approximation, the best solution is given by

$$\phi_n = \phi_p = \frac{1}{2} E_g \,. \tag{2.8}$$

This was shown experimentally for GaAs by Ito (1986). He measured the dark current of an interdigital device as a function of electron barrier height using different metals as Schottky contacts. The resulting curve plotted on a semi–log scale had a V shape with a minimum close to 0.71 eV, the center of the band gap for GaAs. This is consistent with equations 2.4 and 2.5.

Ito obtained a dark current on the order of nanoamps using a barrier

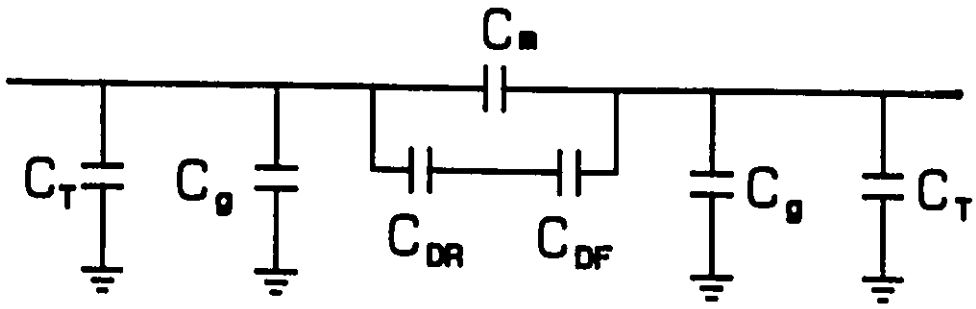
metal of WSi_x, ($x = 0.64$), with $\phi_n \cong 0.75$ eV. He claims that this result is better, or as good as an AlGaAs/GaAs pin photodiode, and thus, that interdigital devices can be made on GaAs with dark current comparable to conventional photodetectors. Extending this idea to materials with smaller band gaps will result in larger dark currents. As an example, the theoretical minimum dark current in silicon is several orders of magnitude larger than in GaAs. In materials with band gaps suitable for detectors operating at 1.3 μm or 1.5 μm the theoretical minimum dark currents would be orders of magnitude greater than silicon. For this reason it may not be possible to obtain low enough dark currents in small band gap materials if the device is operated with the bias voltage greater than the reach through voltage.

CHAPTER 3: CAPACITANCE

The capacitance of a photodiode is of interest as one of the factors limiting its response time. The capacitance of the device coupled with the internal and external load resistances creates an RC low pass filter which limits the maximum bandwidth of the device. Since R is fixed for most high speed applications (generally 50 ohms in this work), the capacitance is the parameter of interest. As a result, the ability to calculate capacitance quickly and easily is necessary to allow design and optimization of device parameters to meet specific design objectives.

The capacitance of an interdigital photodiode can be broken up into constituent components and modeled using a finite differences method. The results of such a model are compared with experiment, which leads to a simplifying assumption. This allows the use of two simple, fast models for quick evaluation of capacitance. A comparison of the models with each other, and with experiment is done, and the range of applicability of the various models discussed.

A simplified equivalent circuit of the capacitance is shown in figure 3.1 . Of principle interest is the capacitance due to the digits. It is the digits which give these devices their properties, and it will be the digit parameters which are adjusted to give a required design performance. The values of interest in figure 3.1 are the interactions of the digits with each other, C_m, with the semiconductor, C_{dr} and C_{df}, and with the ground plane, C_g. The capacitance of the pads to ground has been included in this circuit, but because they are not an active part of the photodiode, and will depend very much on the type of interconnection being used, they will be referred to only in passing. Note that it is assumed that there is no interaction between the two pads.



C_m Interdigital gap capacitance

C_{DR} Depletion capacitance of reverse biased digits

C_{DF} Depletion capacitance of forward biased digits

C_g Digit capacitance to ground

C_T Terminal capacitance to ground

Figure 3.1 Equivalent circuit for the capacitance of an interdigital diode.

As discussed in chapter 2, the numerical solution of Poisson's equation can be used as a tool to determine capacitance. A change in charge (δQ) resulting from a change in voltage (δV) can be found by calculating two potential distributions, one for each voltage. The resulting δQ and δV are used to calculate the capacitance. Numerically this necessitates taking the difference of two similar numbers and requires some care. For example, if δV is too small, the resulting change in charge will also be very small, resulting in a large error in its calculation. If δV is too large, the nonlinearity in the capacitance will produce an error. Through trial and error it was found that δV's in the range of 0.1 percent to 1.0 percent of the initial voltage gave reasonable results.

Another consideration in reducing the error is the number of terms used in the calculation of the boundary potential using Green's formula (see appendix 1). In order to keep the net charge in the numerical system as close to zero as possible, thereby minimizing the error in the total charge, it was found that the larger the number of terms the better. Thus, while only a small number of terms were necessary to get an accurate potential distribution (generally six terms were used) a greater number of terms were required to get good accuracy in the charge calculation.

The procedure for calculation of capacitance was as follows. The built in voltage on the digits was calculated using the appropriate parameters. The applied voltage was added to the reverse biased digit, and the potential distribution solved. The charge on each digit was then calculated using Gauss's law, and the charge in the semiconductor summed. Then new potential distributions were solved with a small δV applied to each of the reverse biased digit and the forward biased digit. Once again, in each case the charge values were calculated. Using these values the

various capacitances could be evaluated. As an example, the capacitance between the digits was calculated by using the change in charge on the forward biased digit when δV was applied to the reverse biased digit. Where possible, capacitances were calculated two ways, and the results compared to ensure that the error was maintained at an acceptable level. An example of this is to calculate the capacitance between the digits by using the change in charge on the reverse biased digit when the voltage was changed on the forward biased digit, and comparing it with the value obtained as described above.

Using this numerical model, the components of the capacitance due to the digits were calculated for an interdigital diode on SOS. Shown in figure 3.2 are the normalized depletion capacitance, C_d, interdigital gap capacitance, C_m, and the total interdigital capacitance as a function of bias voltage. Also shown for reference is the interdigital structure capacitance. This is the capacitance which would result if the semiconductor were replaced by an equivalent insulator and represents a minimum value for the total interdigital capacitance.

The deviation of the total interdigital capacitance from the structure capacitance as a function of voltage is illustrated in figure 3.2. As the bias voltage is increased the difference between the total interdigital capacitance and the structure capacitance decreases until the two values become equal. At this point the semiconductor is totally depleted ($C_d = 0$) and the situation is equivalent to that found in semi – insulating GaAs. Of greater interest for the operation of SOS devices is the capacitance at the reach through voltage, a practical operating voltage. For this example, the reach through voltage is approximately 85 volts. Although there is still significant depletion capacitance, the difference between the total interdigital capacitance and the structure capacitance is less than 5 percent.

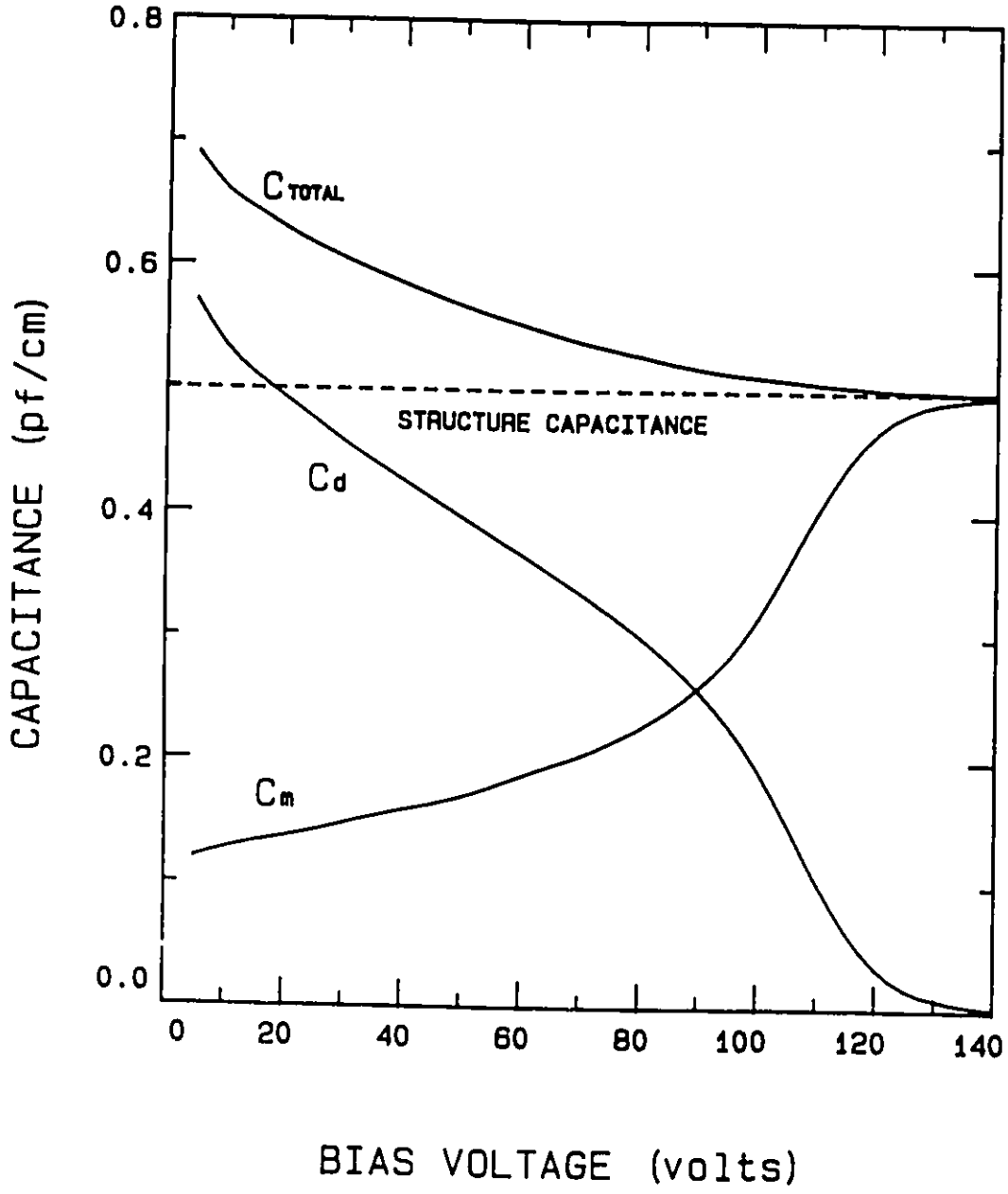


Figure 3.2 Capacitance due to digits as a function of voltage for an interdigital diode on SOS.

Even at bias voltages as low as 60 volts the difference is only 10 percent making the structure capacitance a good approximation of the total interdigital capacitance for devices which are operating near their reach through voltage.

This is further illustrated by the experimental CV curve reproduced in figure 3.3. These data were acquired using an HP 4280A 1MHz capacitance meter, as were all the capacitance data obtained in this chapter. Figure 3.3 shows the total capacitance (including bonding pads) of an interdigital device on SOS. Its parameters are approximately equivalent to those used to calculate the values found in figure 3.2. Although reach through voltage is never attained (due to high leakage currents causing errors in the capacitance measurement), this clearly shows that there is only a small variation of total capacitance at larger bias voltages.

Thus it has been shown that when an interdigital photodetector is near full depletion, the capacitance of the interlocked digits is dominant. Since this is the practical mode of operation for these devices, it is the structure capacitance which is of principal interest in the design of these devices. The finite differences model which can be employed to determine the structure capacitance is functionally exact, but requires a great deal of execution time. Therefore, two other models which are useful for structure capacitance calculations will be discussed. These models allow quick and simple evaluation of the structure capacitance.

When a device structure which is equivalent to these interdigital photodiodes is placed on a dielectric substrate, it forms an interdigital capacitor of a type frequently used in microstrip integrated circuits. The properties of these devices have been studied by several authors (Gaudreault 1985, Alley 1970, and She 1986). Many of their results draw on earlier work which was done to study the interaction between coupled microstrip lines. In one paper, Smith (1971) has

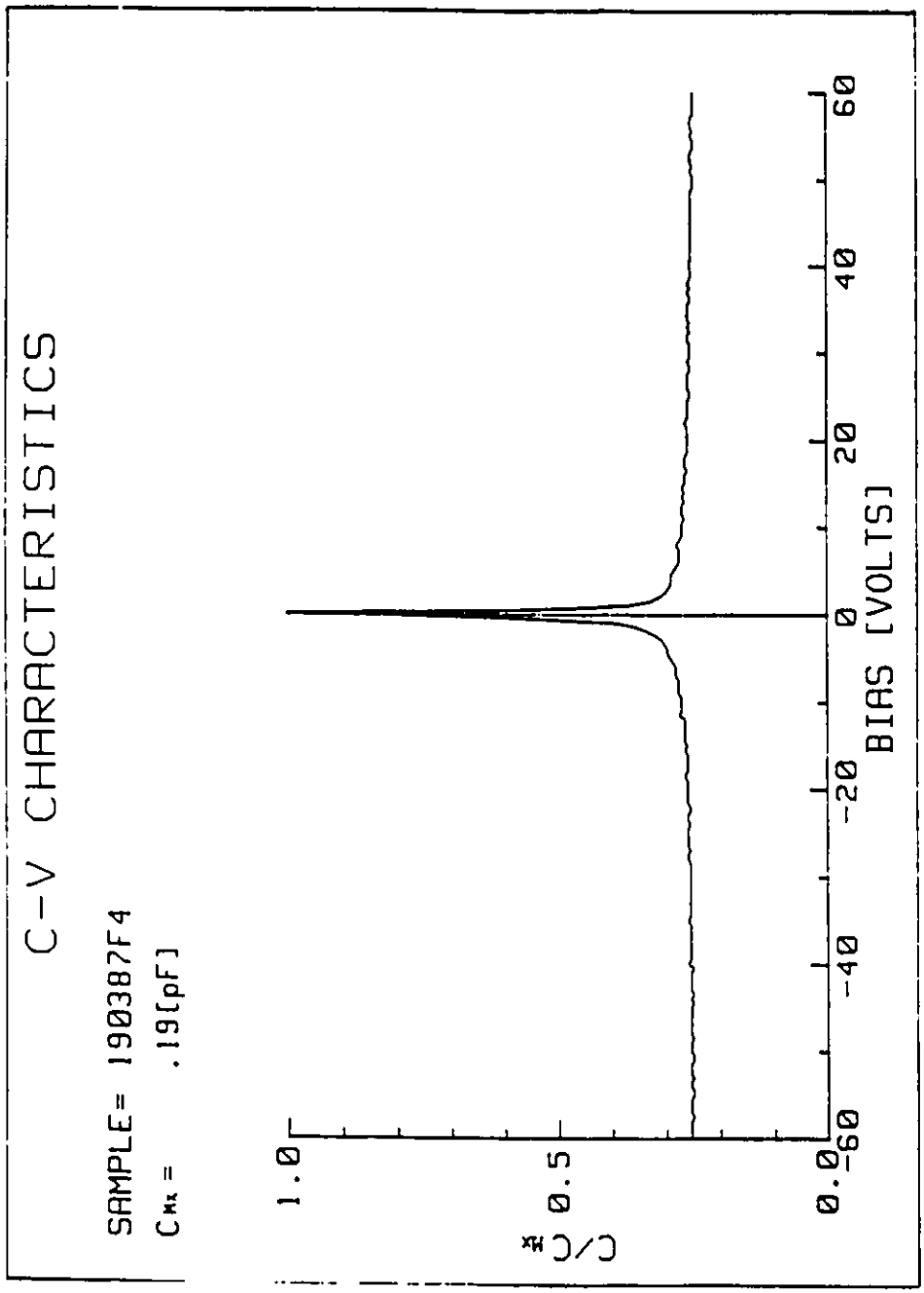


Figure 3.3 Sample of the measured capacitance of a 6 digit diode on SOS (digit width and separation of 10 μm).

presented an algorithm in the form of a fortran program for the rapid calculation of the even and odd mode fringing capacitances for coupled lines, assuming a periodic array of lines. The even mode corresponds to the case where the voltage on all the digits is the same, and the odd mode has the voltages on all the digits equal in magnitude, but alternating in sign. Smith's algorithm is based on capacitance formulas derived from variational series based on conformal transformations. These series are easily evaluated after conversion to finite forms.

The geometry which Smith used is shown in figure 3.4, where ϵ_1 and ϵ_3 are fixed as the relative dielectric constant of air, and ϵ_2 is the relative dielectric constant of the substrate, and is variable. By setting G_1 to zero and G_2 to a very large number this model can be used to calculate the capacitance between a periodic array of digits, as in an interdigital capacitor, on a single dielectric substrate.

Smith's equation 12, (based on work by Yamashita (1968)), is

$$(3.1)\quad \Psi_m = \frac{\{1+\epsilon_2 \tanh(mg_1)\coth(md_1)\}\quad \rho_m}{m\{\coth(mg_2)(1+\epsilon_2\tanh(mg_1)\coth(md_1)) + \\ +\epsilon_2(\epsilon_2\tanh(mg_1)+\coth(md_1))\}}$$

where ρ_m are fourier series coefficients for the charge density, and the remaining variables are defined in figure 3.4.

However, Yamashita treated a more general case which left the dielectric constants of all three layers as variables and obtained the equation;

$$(3.2)\quad \Psi_m = \frac{\{\epsilon_1\coth(mg_1)+\epsilon_2\coth(md_1)\}\quad \rho_m}{m\{\epsilon_1\coth(mg_1)(\epsilon_3\coth(mg_2)+\epsilon_2\coth(md_1)) \\ +\epsilon_2(\epsilon_2+\epsilon_3\coth(mg_2)\coth(md_1))\}}$$

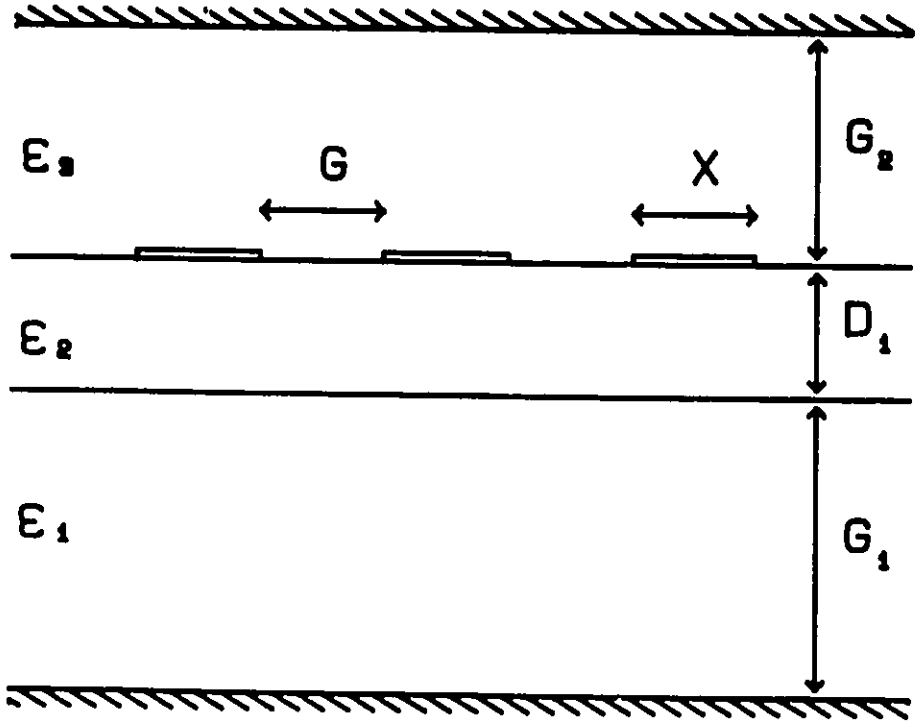


Figure 3.4 Geometry used by Smith for calculating the even and odd mode fringing capacitances of coupled lines.

where the variables have been changed to match Smith's notation. It can be easily shown that if ϵ_1 and ϵ_3 are set to 1.0 then equation 3.1 will result.

Using equation 3.2 in place of equation 3.1, and following the analysis of Smith, his results were generalized to include a two layer substrate. These changes were implemented in a fortran program using Smith's algorithm. The program calculates the even and odd mode fringing capacitances, which he has designated C_{fe} and C_{fo} respectively. Using this notation, the capacitance of the gap between two sets of digits is

$$C_m = (N - 1)\, l\, (C_{fo} - C_{fe}), \tag{3.3}$$

and the capacitance of a single set of digits to ground is

$$C_g = (\frac{N}{2} (2\, C_p) + 2 (N - 1)\, C_{fe} + 2\, C_f)\, l \tag{3.4}$$

where N is the number of digits,

$2\, C_p = \dfrac{\epsilon_0\ x}{G_2} + \dfrac{\epsilon_0\ x}{(G_1 / \epsilon_0 + D_1 / \epsilon_0)}$ is the total parallel plate capacitance between a single digit and the two ground planes,

x is the digit width,

C_f is the asymptotic value of fringing capacitance for a large gap, representing the effect of the end digit, and

l is the length of the digit.

Notice that only C_g is corrected for the effect of the end digits.

A direct approach to the calculation of the capacitance of interdigital capacitors on a homogeneous substrate was taken by She and Chow (1986) who have presented a series of simple analytical expressions. What follows is a brief discussion of their analysis, and the relevant equations which they obtain. Their starting point is the calculation of the distributed capacitances of N microstrip digits for both the even and odd mode. For the even mode, they have shown that when the finger width, x, is comparable in size with the finger separation, d, and both are much smaller than the substrate thickness, h, then the array of digits can be considered to be a wide ribbon of width W, without any gap between the digits, where W is simply the width of the array of digits. For this case the characteristic impedance is simply that of a microstrip line, which is given as

$$(3.5) \qquad Z_w = \begin{cases} \dfrac{60}{\sqrt{\epsilon^e_{eff}}} \ln\left(\dfrac{8}{W}\dfrac{h}{} + \dfrac{W}{4}\dfrac{}{h}\right) & \text{for } \dfrac{W}{h} \leq 1 \\ \dfrac{120\,\pi}{\sqrt{\epsilon^e_{eff}}}\left[\dfrac{W}{h} + 1.393 + 0.667 \ln\left(\dfrac{W}{h} + 1.444\right)\right]^{-1} & \text{for } \dfrac{W}{h} \geq 1 \end{cases}$$

where ϵ^e_{eff} is the effective dielectric constant for the even mode,

$$(3.6) \qquad \epsilon^e_{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2}\left(1 + 10\,\frac{h}{W}\right)^{-\frac{1}{2}}$$

where ϵ_r is the relative dielectric [illegible] of the substrate.

The average distributed capacita[illegible] digit for the N digit array is then

(3.7) $$C_e = \frac{1}{N} \frac{\sqrt{\epsilon^e_{eff}}}{Z_w c}$$

where $c = 3 \times 10^8$ m/sec is the velocity of light in free space.

For the odd mode, the digits are assumed to be in a homogeneous dielectric medium. This assumption is justified by the large field cancellation due to the alternating positive and negative charge which results in the "distant" ground plane having a very small effect on the field of the digits. In this case the effective dielectric constant for the odd mode is

(3.8) $$\epsilon^o_{eff} = \frac{\epsilon_r + 1}{2}.$$

The distributed capacitance per digit for an infinite number of digits in a homogeneous space is given as

(3.9) $$C^\infty_0 = \frac{2 \pi \epsilon^o_{eff} \epsilon_0}{\ln(\frac{8 d}{\pi x})}.$$

For the more general case of a finite number of digits, N, in the array, the digits at the ends of the array experience edge effects which tend to decrease the odd mode capacitance in these digits. Thus the average capacitance per finger is given as

(3.10) $$C_0 = C^\infty_0 \left(1 - \frac{A}{N} \right)$$

where A is a correction constant, for which an approximate expression was given as

$$A = \frac{25.5 + 15.5 \ln\left(\frac{d}{x}\right)}{37.3 + 48.7 \ln\left(\frac{d}{x}\right) + 12.6 \left(\ln\left(\frac{d}{x}\right)\right)^2} \tag{3.11}$$

The above expressions for even and odd mode capacitances are used to calculate the mutual capacitance per meter between two digits, and the capacitance per meter of each finger to ground using

$$C_1 = \frac{1}{2}\left(C_0 - C_e\right) \tag{3.12}$$

$$C_2 = C_e \tag{3.13}$$

where C_1 and C_2 are defined in figure 3.5 . For an array of N digits there are N/2 unit cells of two digits each. Thus for digits of length l, the total capacitances are given by

$$C_m = \frac{N}{2} C_1 l \tag{3.14}$$

$$C_g = \frac{N}{2} C_2 l \tag{3.15}$$

where C_m and C_g are defined above.

She and Chow point out that a terminal pad can be approximated as a single microstrip line. The capacitance of a terminal pad can thus be calculated using the dimensions of the terminal pad in equations 3.5, 3.6, and 3.7 with N = 1. This approximation can also be implemented using Smith's model using

$$C_t = \left(2C_p + 4C_f\right) l_t \tag{3.16}$$

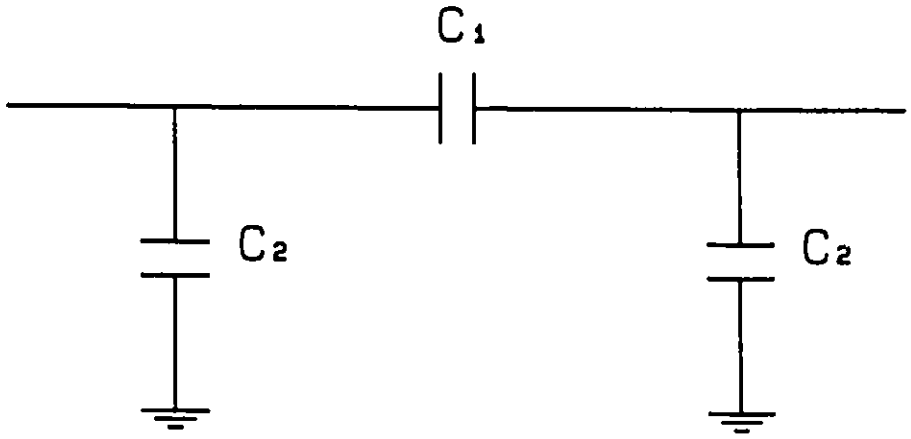


Figure 3.5 Definition of capacitances C_1 and C_2 calculated in equations 3.12 and 3.13.

where $2C_p$ and C_f are calculated using the width of the terminal pad, W_t, and l_t is the length of the terminal pad.

To summarize, three models for the calculation of interdigital capacitance values have been introduced. For simplicity they will be referred to as follows: the finite differences model will be referred to as the numerical model, Smith's modified algorithm will be referred to as Smith's model, and She and Chow's analytical expressions collectively will be referred to as the analytical model. These three models are based on different solution methods, and have very little in common. The numerical model is a functionally exact solution for an infinite number of digits. Any errors result from the numerical implementation of the solution, and can be controlled with reasonable care. The major drawback of this approach is the amount of computer time required for a solution. Smith's model uses a variational series analysis to obtain a solution which can be evaluated quickly and easily on a computer. The analytical model obtains simple approximate analytical expressions by using various simplifying approximations. The resulting formula are easily used and provide a basis for simple general analysis.

Depicted in figure 3.6 are values of C_m. the intergap capacitance, as a function of digit width for various digit separations. The values were calculated for a 10 digit device on a 500 micron thick sapphire substrate using all three models. They have been normalized by assuming digits of unit length and dividing by the number of gaps, $(N-1)$.

The agreement between Smith's model and the numerical model is very good, having a difference of less than one percent at all points. It is convenient to compare either of these two models with the analytical model in two regions. The first region has a digit separation greater than the digit width ($\frac{G}{x} \geq 1$, $\frac{d}{x} \geq 2$), and

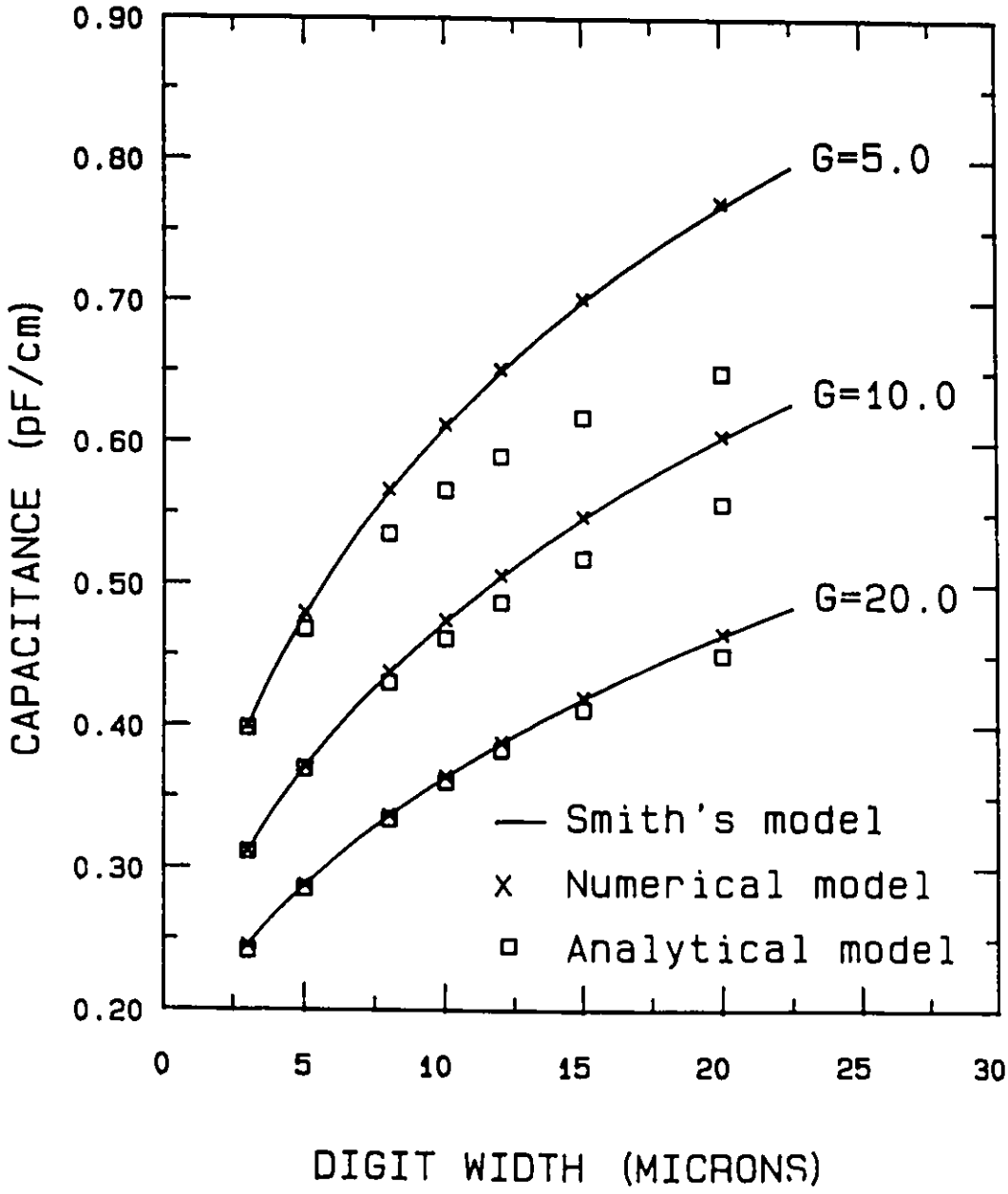


Figure 3.6 Calculated values of C_m comparing the analytical model, the numerical model, and Smith's model for a 10 digit device on a 500 μm thick sapphire substrate.

the second region has a digit separation less than the digit width ($\frac{G}{x} < 1$, $\frac{d}{x} < 2$). This is a practical distinction to make since most photodetectors are in the first category to maximize the exposed semiconductor. The agreement between the analytical model and the other two in the first region is generally good to within five percent. In the second region, the analytical model begins to deviate significantly from the other two as the digit width increases, although the results are still reasonable, with less than ten percent error, for values of $\frac{G}{x}$ down to 0.5. Figure 3.6 represents a specific case, but the results are representative of those over a wide range of parameters.

Figure 3.7 compares the values of C_m calculated using Smith's model and the numerical model for a 10 digit diode on a substrate consisting of 1 micron of insulating silicon on 500 microns of sapphire. Once again the agreement is generally better than one percent for a large range of device parameters.

A comparison of the values of C_g, the digit capacitance to ground, is shown in figure 3.8 for a 1000 digit diode on a 500 micron thick sapphire substrate. The capacitance values have been normalized to one digit by assuming digits of unit length and dividing by half the number of digits, $\frac{N}{2}$. Good agreement is found among all three models, with very little dependence on digit separation or digit width. Figure 3.9 illustrates that this is only true for devices with a very large number of digits. These curves were calculated assuming a 10 micron digit width and a 10 micron digit separation with a 500 micron thick sapphire substrate but are representative of the general relationship.

Although the difference in calculated values of C_g is as large as 30 percent for small N, the effect on the total capacitance will generally be small, as illustrated in figure 3.10 . With the exception of small h, C_m is much larger than C_g,

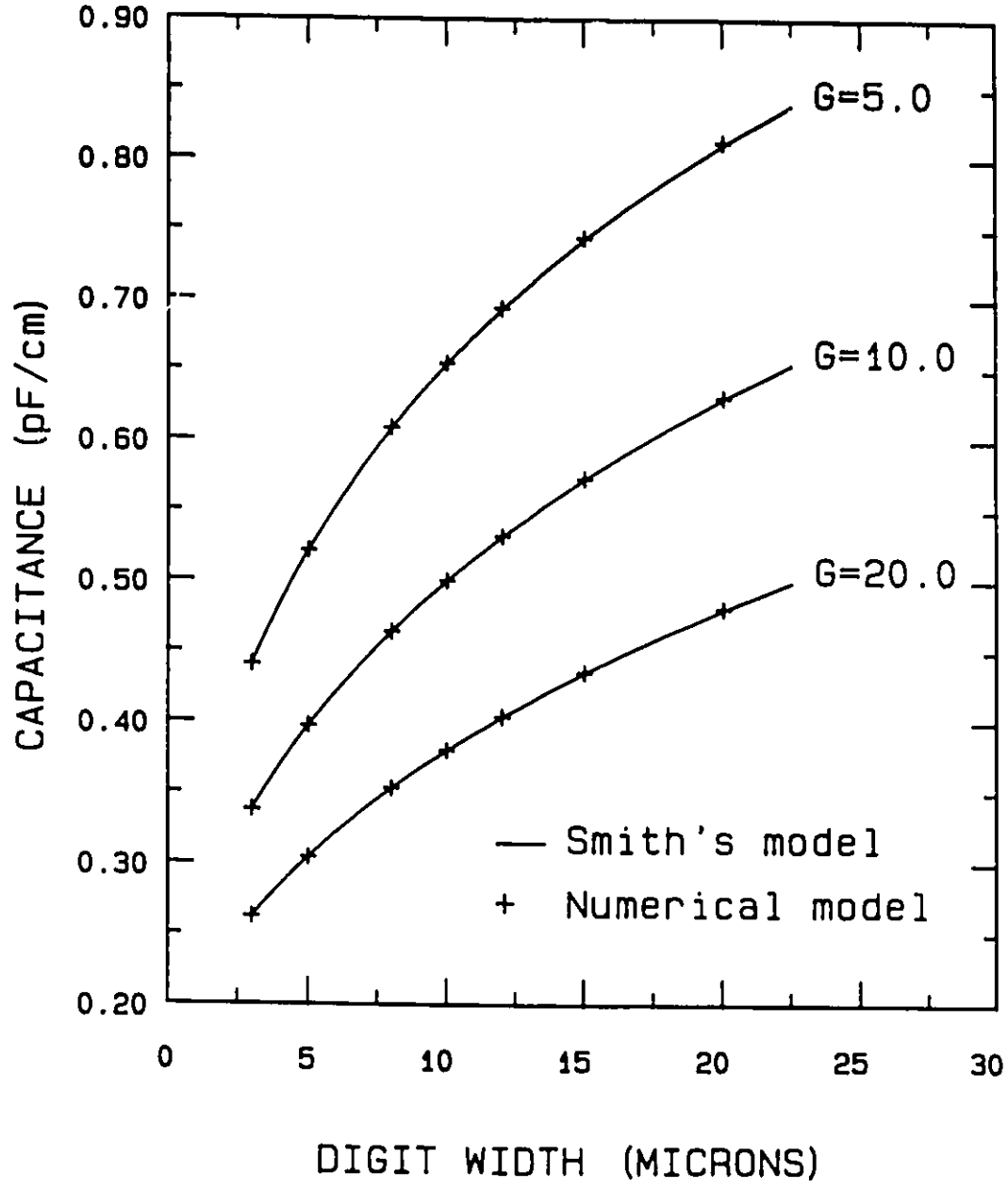


Figure 3.7 Calculated values of C_m comparing Smith's model and the numerical model for a 10 digit device on an SOS substrate of 1 μm thick insulating silicon on 500 μm thick sapphire.

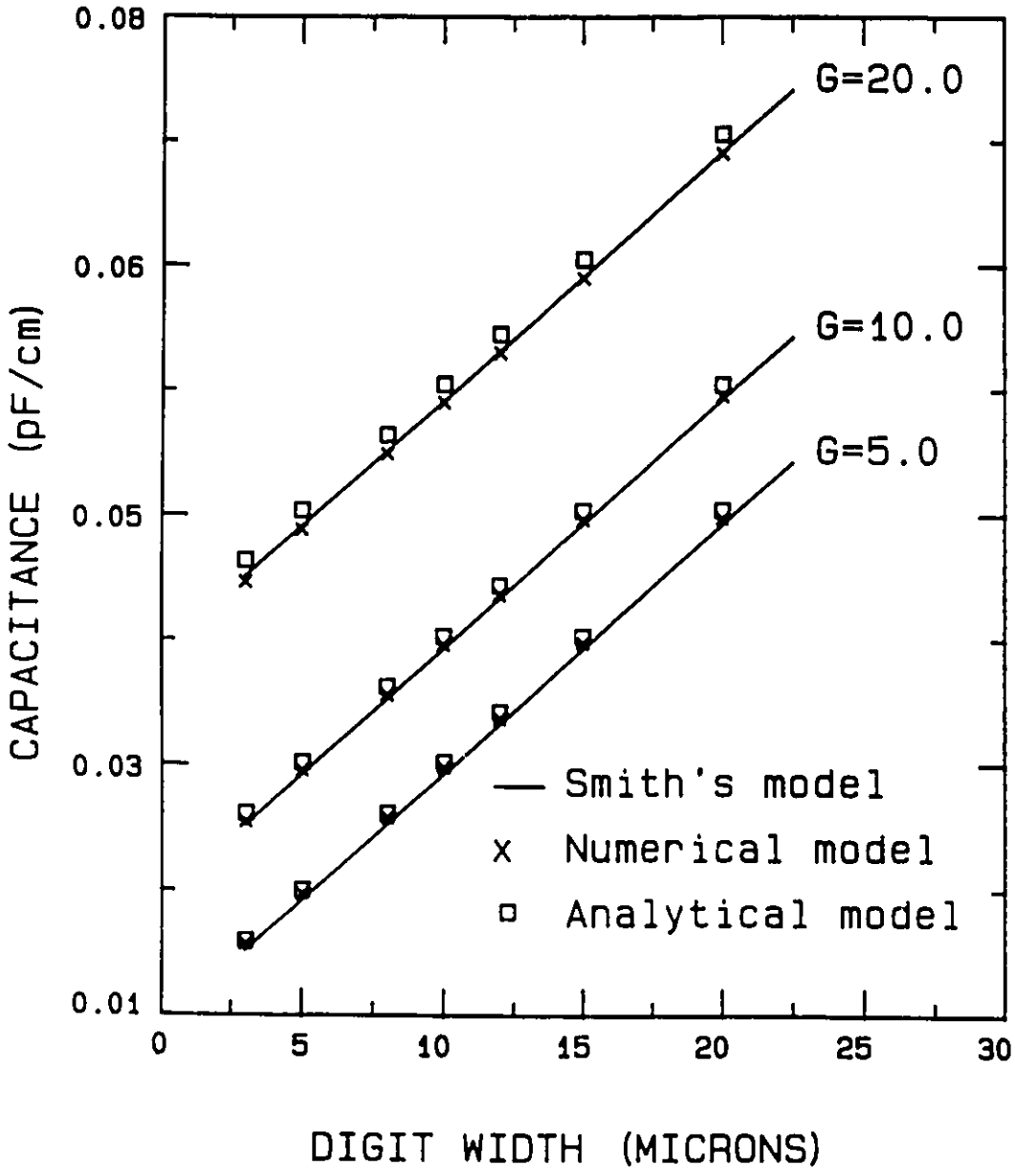


Figure 3.8 Calculated values of C_g comparing the analytical model, the numerical model, and Smith's model for a 1000 digit device on a 500 μm thick sapphire substrate.

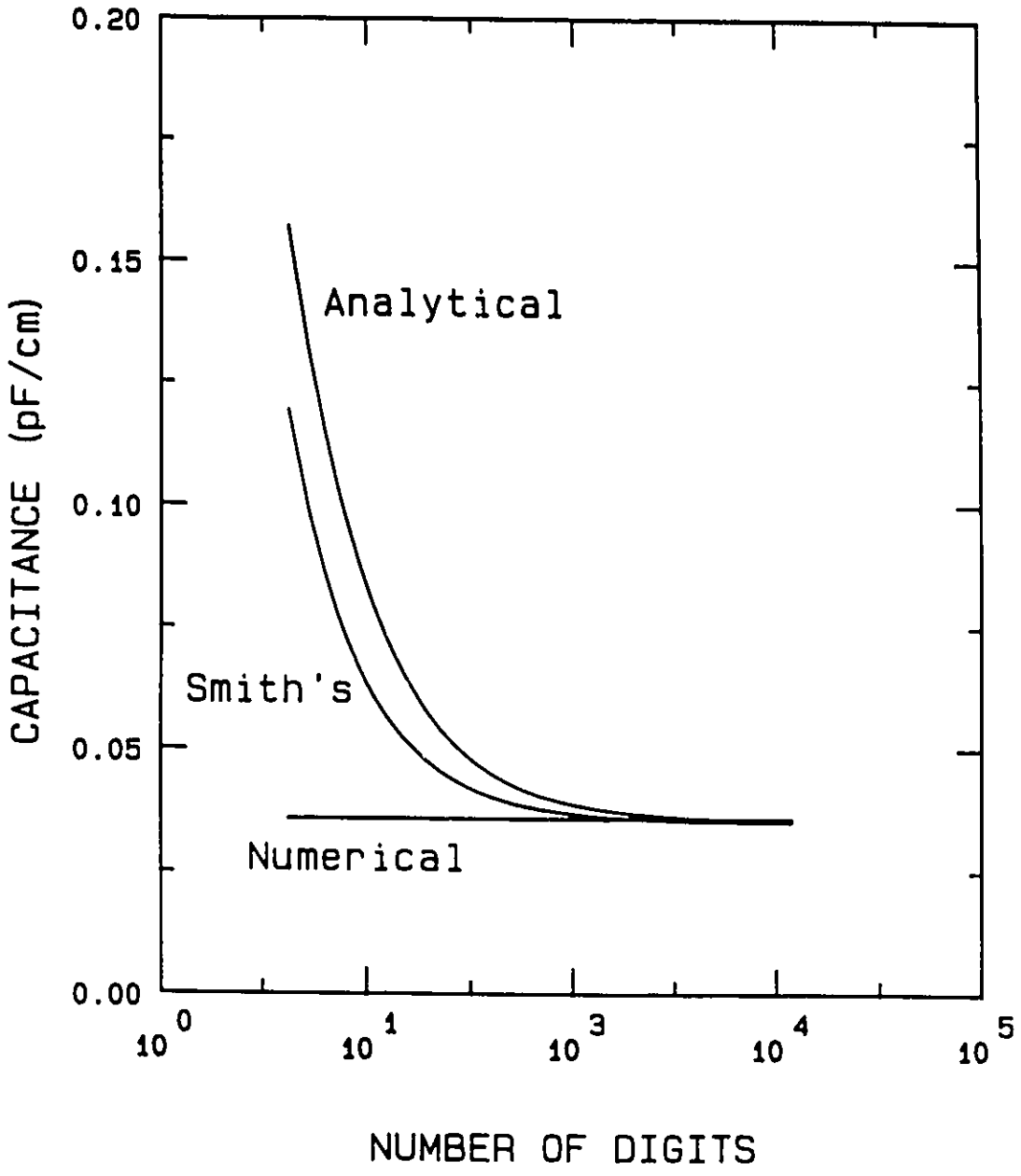


Figure 3.9 Normalized values of C_g as a function of the number of digits, assuming a digit width and digit separation of 10 μm on a 500 μm thick sapphire substrate. Results of the analytical model, the numerical model, and Smith's model are shown.

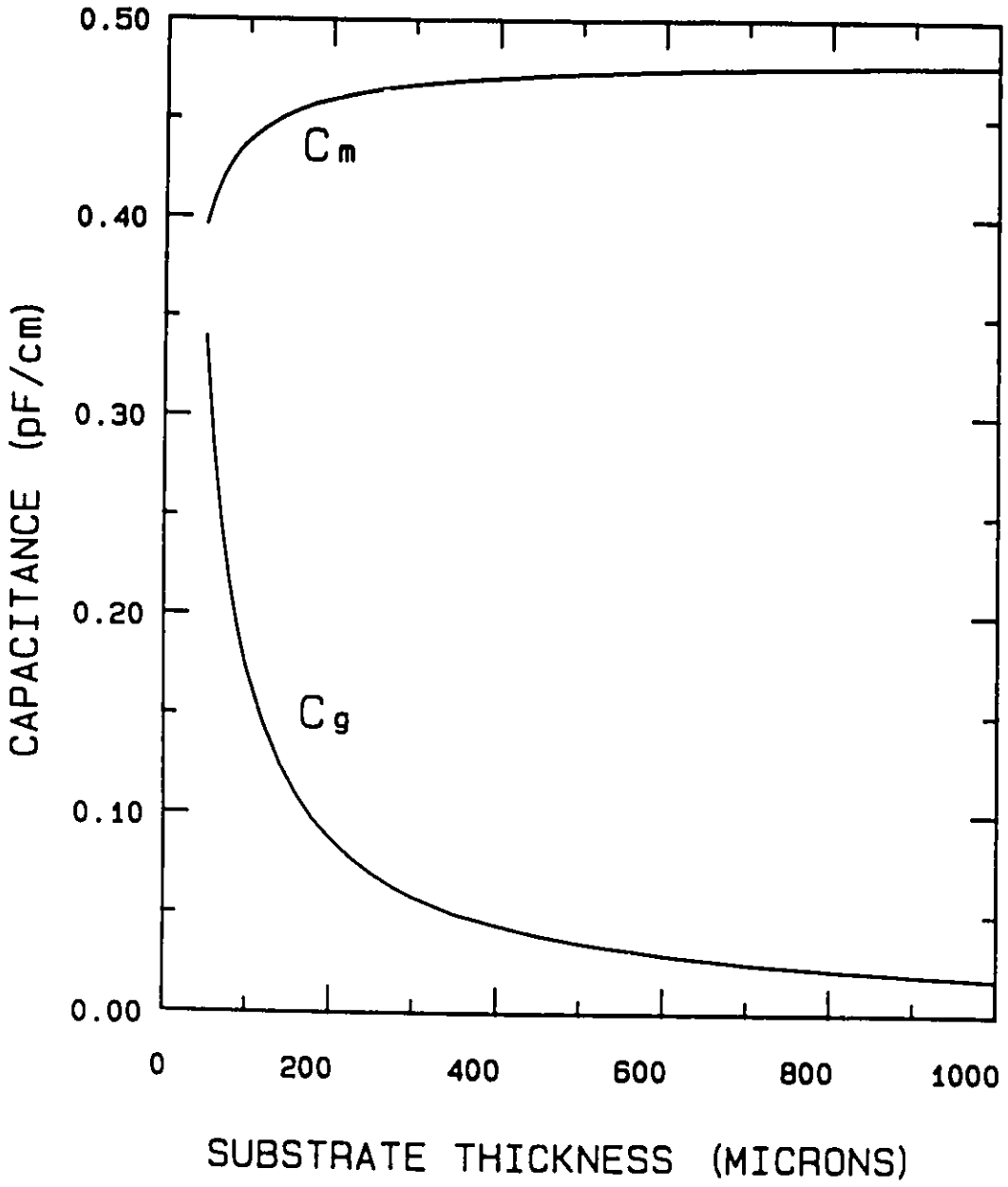


Figure 3.10 Variation of C_m and C_g as a function of substrate thickness.

minimizing the effect on the total capacitance of any error in the calculation of C_g.

The dependence of C_g on N is the result of edge effects. The numerical model does not correct for edge effects as indicated by its lack of dependence on N. Both Smith's model and the analytical model account for edge effects, but in different manners. Smith's model calculates the fringing capacitance due to an isolated digit, whereas the analytical model uses a single line with width equal to the width of the device. It is felt that in general the analytical model slightly overestimates the fringing capacitance by completely neglecting the effect of gaps, and Smith's model underestimates the fringing capacitance by ignoring the effect of the other digits. Unfortunately it was not possible to determine which gave a better estimate.

The above discussion shows that the effect of the edge digits on C_g can be significant. A review of the models shows that only the analytical model corrects for the effect of the edge digits on C_m. Therefore, this model can be used as an indicator of the error which may be incurred by ignoring this effect. Figure 3.11 shows values of C_m for a 10 micron digit separation on sapphire substrate. This clearly illustrates that the effect of the edge digit is very small unless the substrate is very thick.

Important aspects of these two models can now be reviewed and their range of applications summarized. Smith's model is generally in good agreement with the exact numerical model in regions of the latter's applicability. While Smith's model also requires a computer, the actual computational effort is very small. The flexibility of this model allows performance of capacitance calculations for two layer substrates, and a broad range of device parameters. C_m is not corrected for edge effects, but these effects have been shown to be small except when

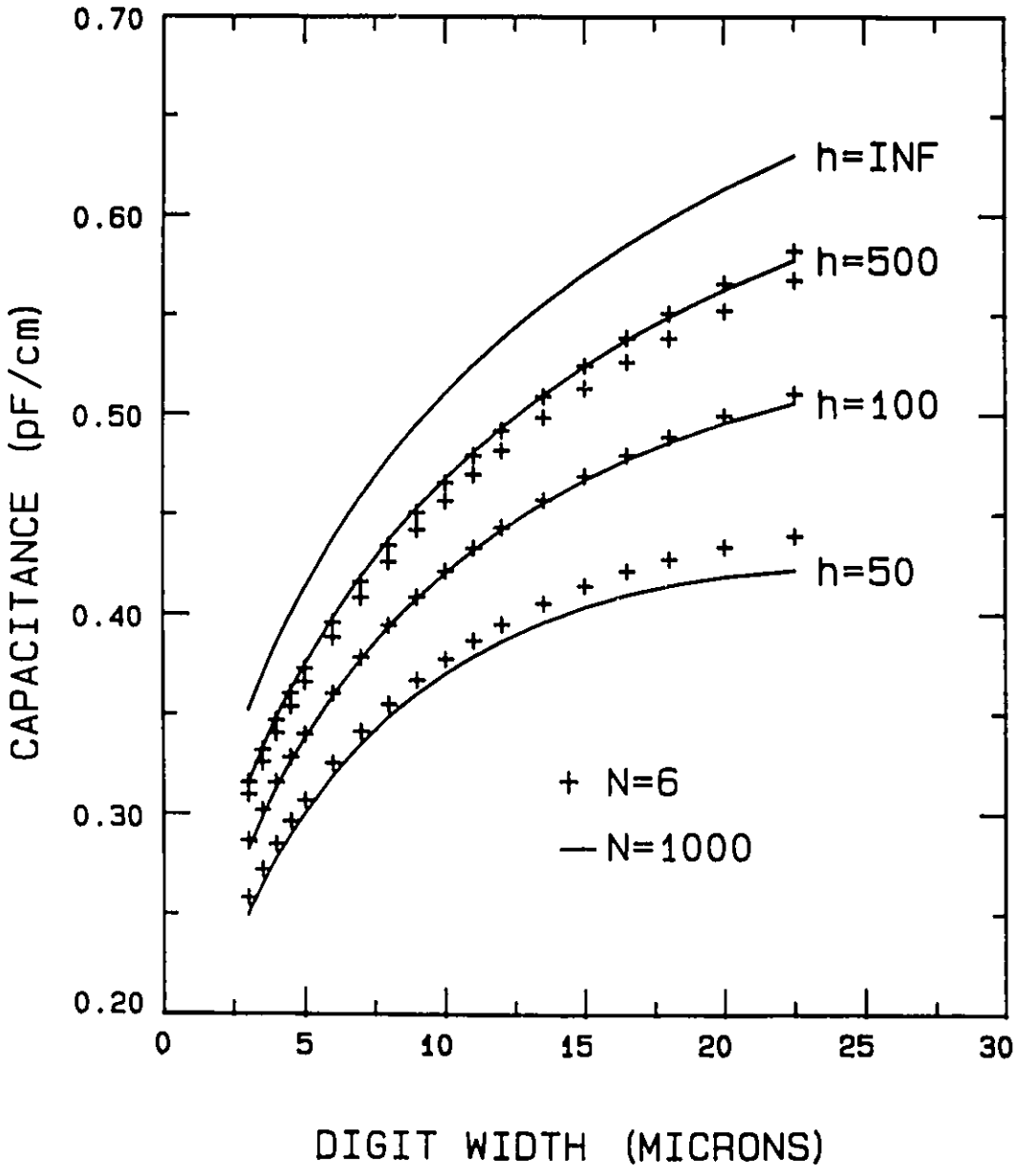


Figure 3.11 Comparison of normalized values of C_m calculated for a device with 6 digits and a device with 1000 digits using several substrate thicknesses (h). A digit separation of 10 μm and a sapphire substrate were assumed

h is very large. The speed of calculatio and the flexibility of Smith's model make it a practical method for specific calculations.

The analytical model is in reasonable agreement with the more exact numerical model in the region of most practical interest where $\frac{G}{x} \geq 1$. It can only deal with a single layer substrate, and the effect of the approximations which were required to obtain its simplified form are apparent in the region where $\frac{G}{x} < 1$. Its principal advantage rests with its analytical form. Use of these expressions enables immediate observations and conclusions in any general analysis.

As a further test of the models, a limited comparison with experiment was performed using the device structures described in table 3.1. Three different substrates were used. Two of these, sapphire and semi–insulating GaAs, are dielectric substrates. As expected the capacitance of structures on these substrates showed no voltage dependence. The other substrate was epilayer GaAs, with a nominal 3μm thick epitaxial layer doped $< 10^{14}$ cm^{-3} on a semi–insulating substrate. Structures on this substrate showed a very small voltage dependence indicating nearly complete depletion at zero bias voltage.

All of these devices were measured in two configurations, one with the ground plane floating relative to both terminals, C_b, and the other with the ground plane shorted to one of the terminals, C_a. The resulting capacitances are given by

$$C_a = C_m + C_g + C_t \tag{3.17}$$

$$C_b = C_m + \frac{1}{2}(C_g + C_t). \tag{3.18}$$

It follows that the gap capacitance can be calculated as

DIODE #	DIGIT WIDTH x (μm)	DIGIT SEP. G (μm)	NUMBER OF DIGITS	DIGIT LENGTH l (μm)	TERMINAL WIDTH W_t (μm)
1	10.	10.	16	300.	100.
2	10.	15.	14	300.	100.
3	10.	20.	12	300.	100.
4	10.	10.	6	100.	100.

Table 3.1 The dimensions of the experimental devices fabricated.

(3.19) $$C_g = 2C_b - C_a$$

The measured results are listed in table 3.2 The values calculated using Smith's model are shown in table 3.3. The differences between calculated and measured values for C_a and C_b are greater than the standard deviation in almost all cases. The measured values are generally larger than the calculated values, probably due to stray capacitances involving the bonding wire. Stray capacitance would also account for the much larger differences associated with smaller capacitances of diode #4.

The calculation of C_m from the experimental data allows a partial canceling out of errors due to stray capacitance. A comparison of experimental and theoretical values show the majority are within the standard deviation of the experimental values. The large devices with the correspondingly large capacitances generally agree to better than 10 percent. The small devices still show a large relative difference, indicative of the larger error in their measurement.

This illustrates the agreement between calculated and experimental values of the intergap capacitance, C_m. As previously indicated, the ability to calculate C_m is important because it is the dominant capacitance under the designers control. In view of the error associated with taking differences it is not possible to draw specific conclusions about the calculation of C_g and C_t; it is clear, however, that the model gives reasonable approximations of their value.

DIODE #	$C_a = C_m+C_g+C_t$ (pF)	$C_b = C_m+\frac{1}{2}(C_g+C_t)$ (pF)	$C_m = 2C_b - C_a$ (pF)
		SAPPHIRE	
1	0.289 ± .016	0.244 ± .014	0.199 ± .020
2	0.228 ± .012	0.180 ± .014	0.133 ± .011
3	0.198 ± .003	0.153 ± .006	0.107 ± .004
4	0.076 ± .005	0.047 ± .004	0.018 ± .007
		SEMI – INSULATING GaAs	
1	0.362 ± .009	0.316 ± .008	0.270 ± .008
2	0.284 ± .004	0.233 ± .005	0.182 ± .008
3	0.231 ± .003	0.183 ± .004	0.135 ± .005
4	0.082 ± .003	0.052 ± .001	0.022 ± .004
		EPI – LAYER GaAs	
1	0.378 ± .009	0.325 ± .010	0.273 ± .011
2	0.291 ± .006	0.238 ± .006	0.186 ± .009
3	0.230 ± .013	0.198 ± .014	0.158 ± .018
4	0.073 ± .011	0.056 ± .001	0.039 ± .010

Table 3.2 Measured capacitance values for interdigital capacitors on sapphire (h = 440 μm), semi – insulating GaAs (h = 500 μm), and Epi – layer GaAs (h = 410 μm).

DIODE #	$C_m+C_g+C_t$ (pF)	$C_m+\frac{1}{2}(C_g+C_t)$ (pF)	C_m (pF)
		SAPPHIRE	
1	0.251	0.228	0.205
2	0.198	0.174	0.149
3	0.161	0.136	0.111
4	0.035	0.028	0.021
		SEMI – INSULATING GaAs	
1	0.323	0.295	0.266
2	0.255	0.225	0.194
3	0.206	0.175	0.145
4	0.045	0.036	0.028
		EPI – LAYER GaAs	
1	0.327	0.296	0.265
2	0.259	0.226	0.193
3	0.210	0.177	0.144
4	0.046	0.037	0.027

Table 3.3 Values of capacitance calculated using Smith's model for the devices shown in table 3.2, (sapphire $\epsilon_r = 9.9$ and GaAs $\epsilon_r = 13.1$).

CHAPTER 4: PULSE RESPONSE CHARACTERISTICS

A time dependent model to calculate the temporal response of an interdigital detector to a given incident light pulse was discussed in chapter 2. In all practical applications the detector will be part of an external circuit, so the actual output of the detector will be the combination of the device response with the external circuitry response. In this chapter, the factors affecting the actual output of the detector system used will be discussed. These factors will be used to calculate the response of the detector system and the results will be compared with experimental values. A brief comparison of the two dimensional model with a computationally faster and simpler one dimensional model will also be included.

The time response of experimental devices was obtained by mounting the devices in a suitable mount and displaying the response to an approximately known input light pulse on a sampling scope. Figure 4.1 shows a simplified equivalent circuit of the total system, the output of which is the observed response. The time response of this system can be broken into four main factors.

The inherent response of the device is given in simple terms by the average time it takes the carriers to travel from the point of creation (by the absorption of an incident photon) to the point of collection. This is generally referred to as the transit time. The inherent response as a function of time can be obtained using the time dependent model with an impulse light input. The response of the device to an arbitrary light pulse input is represented by the interaction of the light pulse with the inherent device response. This is calculated using the time dependent model and is represented by the current source in the equivalent circuit.

A low pass filter is formed by the resistance and capacitance combination

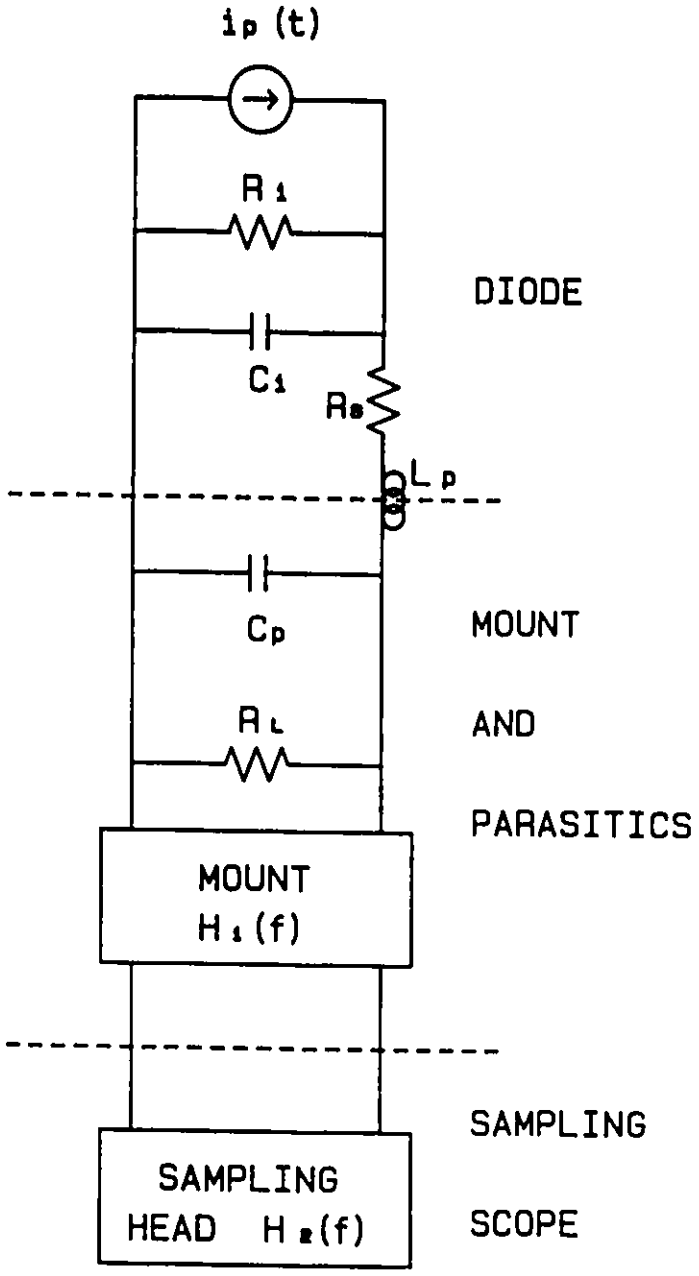


Figure 4.1 Simplified equivalent circuit of the photodiode time response measurement system.

of the detector and the external circuitry and can further limit the system response time. Referring to the equivalent circuit, generally the device is designed to have R_i very large and R_s very small so the contribution of the device to the total load resistance is small compared to the external load resistance and is assumed negligible. This will generally be true of the interdigital devices discussed here. For most applications the load resistance is fixed, usually at 50 ohms for high speed applications. In the system used here, the mount had a load resistor of 50 ohms, which when combined with the 50 ohm input impedance of the coaxial mount and system gave a net load resistance of 25 ohms.

Total capacitance is the sum of the diode capacitance, C_i, (see chapter 3) and any parasitic capacitance, C_p, which exists in the system. Every attempt is made to minimize the parasitic capacitances so the device capacitance will be the dominant effect in a well mounted diode. The capacitance of the system will be assumed to be that of the device in these calculations. Included in the equivalent circuit is a parasitic inductance. Again, every attempt is made to minimize the inductance due to mounting, but it will be shown that in these devices the inductance can be significant. As a result this is more properly modeled as an RLC circuit.

The inherent, or transit time response of the diode combined with the RC response of the diode capacitance and external load resistor represent the fundamental limits for the device response. Other limits to the device response are generally application specific. This includes the mount which has its own inherent frequency response as indicated by the transfer function $H_1(f)$ in figure 4.1. In these measurements the mount was made of an SMA stub connector with the load resistor and biasing system attached directly using chip components. The diodes were

mounted using bonded wires and silver paint, with the length of bond wires minimized by using gold ribbon as part of the mount. SMA connectors are rated to operate at frequencies up to 18 GHz and it is assumed that these mounts are not a limiting factor in this system.

A Tektronix 7409 oscilloscope was used to display and measure the output pulses. This scope was equipped with a Tektronix S-4 sampling head which has a nominal rise time of 25 psec. Experience has shown that the response of this sampling head to an impulse has a full width at half maximum (FWHM) of about 30 psec. This is consistent with the observation of Bowers (1987). The temporal response of the sampling head is assumed to be Gaussian in nature with a FWHM of 30 psec (although this is inconsistent with a step function response rise time of 25 psec indicating that this is an approximation at best) and is represented by the transfer function $H_2(f)$. The sampling head limits the frequency response of the system nominally to 14 GHz.

The observed output response is a convolution of all these factors. Modeling the output response requires that the impulse response of each of the sections discussed above be calculated and convolved together with the diode response. The diode response is calculated for the given incident light pulse using the numerical model. The impulse response of the RC (or RLC) circuit can be found in most basic electrical circuits books (see for example, Scott 1965). The effect of the mount has been assumed to be negligible and the sampling head impulse response has been assumed to be a 30 psec FWHM Gaussian. A fast Fourier transform (fft) routine was used to do the convolution (the inverse Fourier transform of a product of Fourier transforms is the convolution of the original function, Arfkin 1970).

Experimental data on mounted devices were obtained using two different lasers. One was a PLS10 Ultra High Speed Diode Laser with a nominal pulse width of 70 psec (FWHM) at a wavelength of 820 nm. This pulse width is slower than, or on the order of the response time of the devices being tested. The other was a pulsed dye laser with a nominal pulse width of 4 psec at a wavelength of 600 nm. 4 psec is much faster than the response time of any of the devices being tested, and for the purposes of discussion can be considered an impulse excitation. The output response of the device under test was displayed on the sampling scope, and the FWHM and rise time were measured using an SE10 Signal Enhancer from Opto – Electronics Inc. These two numbers are generally used to characterize pulse response time. Also measured was the period of any ringing which was present. This was characterized by the period between the primary response peak, and the first ringing peak. This number was designated τ_d and was measured visually from the scope display.

Experimental devices are defined in table 4.1 and include devices manufactured on SOS and semi – insulating GaAs. Devices on epi – layer GaAs were also tested using the 70 psec laser, but the results duplicated the results of devices on semi – insulating GaAs and were not included. Table 4.2 lists the measured and modeled results for the devices in table 4.1. A sample of the measured and modeled responses are shown in figure 4.2. The capacitance and inductance values are the ones used in the model. Capacitance values were those measured in chapter 3 and the parasitic capacitance was assumed to be negligible. The parasitic inductance was unknown and could not be ignored, so inductance was used as a fitting parameter. This was accomplished by choosing the inductance, to the nearest 0.5 nH, which gave the best fit to the three parameters measured.

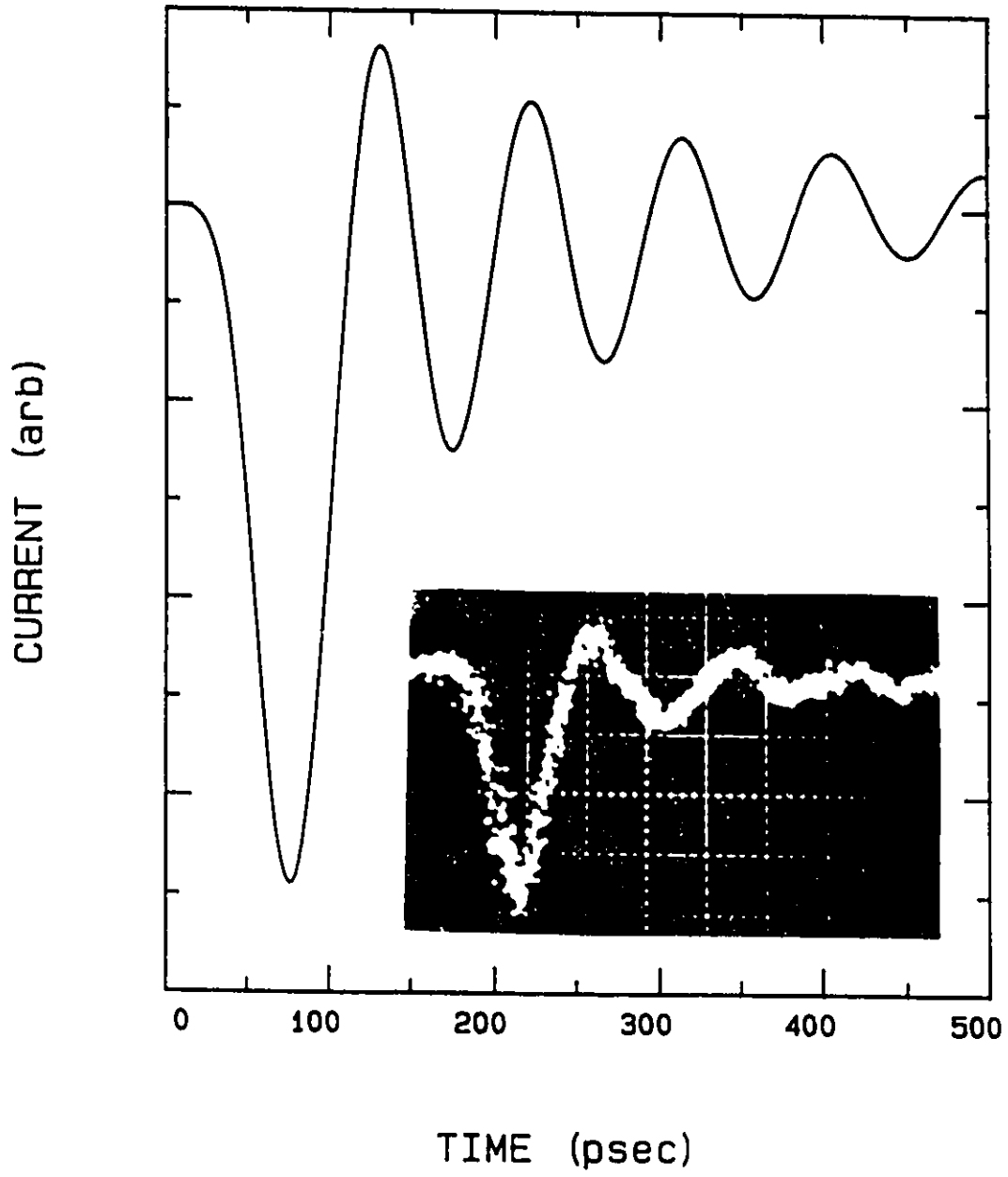


Figure 4.2 The measured (inset photo) and modeled photoresponse of device 4 to a 4 psec incident light pulse. (Time Scale 50 psec/div.)

DEVICE #	MATERIAL*	DIGIT WIDTH (μm)	DIGIT SEPARATION (μm)	NUMBER OF DIGITS
1	GaAs	10	20	12
2	GaAs	10	15	14
3	GaAs	10	10	16
4	GaAs	10	10	6
5	GaAs	5	5	6
6	SOS	10	10	6
7	SOS	5	5	6

*(GaAs, semi – insulating; SOS, $N_d = 5 \times 10^{15}$ cm^{-3})

Table 4.1 Experimental devices used in response time measurements.

	4 psec INPUT		70 psec INPUT	
	MEASURED	MODELED	MEASURED	MODELED
Device 1	V = 15 volts	C = 0.23 pf	L= 2.5 nH	
Rise	37	45	68	67
FWHM	66	69	92	87
τ_d	160	161	160	167
Device 2	V = 20 volts	C = 0.28 pf	L = 2.0 nH	
Rise	–	–	72	68
FWHM	–	–	92	92
τ_d	–	–	170	169
Device 3	V = 15 volts	C = 0.36 pf	L = 2.5 nH	
Rise	–	–	72	71
FWHM	–	–	98	94
τ_d	–	–	190	198
Device 4	V = 15 volts	C = 0.085 pf	L = 2.5 nH	
Rise	24	33	59	59
FWHM	43	48	78	80
τ_d	110	98	110	101
Device 5	V = 10 volts	C = 0.05 pf	L = 3.0 nH	
Rise	27	29	55	55
FWHM	36	38	72	73
τ_d	90	81	–	–
Device 6	V = 50 volts*	C = 0.075 pf	L = 3.0 nH	
Rise	26	32	59	57
FWHM	37	44	66	73
τ_d	110	99	120	107
Device 7	V = 50 volts	C = 0.045 pf	L = 3.5 nH	
Rise	26	28	55	55
FWHM	37	38	68	71
τ_d	–	–	–	–

*Approximately half depleted.

Table 4.2 Measured and modeled response time results for devices listed in table 4.1.

Comparing the sample measured and modeled responses in figure 4.2, the primary pulses are similar, but the modeled oscillations are significantly larger than the measured results and do not attenuate as quickly. This was generally true for all the devices, with the difference larger for results obtained using the 4 psec laser than the 70 psec laser. Additionally, the oscillations in the measured results do not appear to be purely sinusoidal as the modeled results suggest. This was true in varying degrees for all the measurements made.

Comparing the measured and modeled results in table 4.2, there is good agreement between most numbers, generally to within 10 %. The good agreement between theory and experiment for these sample devices indicates the ability of the two dimensional model to approximate the diode response to a given input pulse. (These devices, and fast photodiodes in general, are usually operated at high fields, making the saturation velocity a dominant factor in determining transit time response. The saturation velocity in most semiconductors is limited by optical phonon scattering which is relatively independent of material and processing properties (Garside 1982), making the time response relatively insensitive to errors in these quantities.)

The values of inductance found for these devices and shown in table 4.2 are larger than might be expected from just the bonding wires and mount. This suggests that there is a contribution to the total inductance from the device itself. This is a reasonable suggestion since the digits themselves will act as inductors. It is also probable that at the high frequencies involved in these measurements (on the order of 10 GHz) the RLC model used is simplistic. This is suggested by the differences in the ringing oscillations found between the measured and modeled results. Although the model discussed above is a good approximation, frequency

dependent effects such as microstrip line dispersion, and conductor and dielectric losses may have an effect on the device response. Other possible shortfalls of the model include the mount response which was assumed to have no effect, and the Gaussian approximation of the sampling head response.

Each run of the two dimensional model used in table 4.2 took at least 5 days, and in some cases considerably longer, to run on a 8 MHz IBM XT compatible. Although this time can be substantially reduced using more powerful computers, a considerable amount of computing power is required. Another possible solution is the use of a simpler model. Tables 4.3 and 4.4 show results obtained using the two dimensional model and equivalent runs using a one dimensional model (Levy, 1987). The one dimensional calculations were done in a slightly different manner on the two materials. Since the GaAs devices were depleted all the way through, the parameters used in the one and two dimensional calculations were the same. SOS devices were only partially depleted, so in order to make the calculations equivalent, the voltage in the one dimensional calculation was adjusted to obtain a depletion length which was equivalent to that obtained from the two dimensional calculation.

Figure 4.3 shows typical examples of one and two dimensional response calculations. The curves are physically similar, with the exception of the tails. A larger tail is predicted by the two dimensional model, possible due to the greater distance some slow charge carriers must travel in the two dimensional device. The ability to predict the basic response shape is important for calculations involving autocorrelation. Autocorrelation measurements involve convolving a pulse with itself, and the size and shape of the output pulse is dependent on the shape of the input pulse.

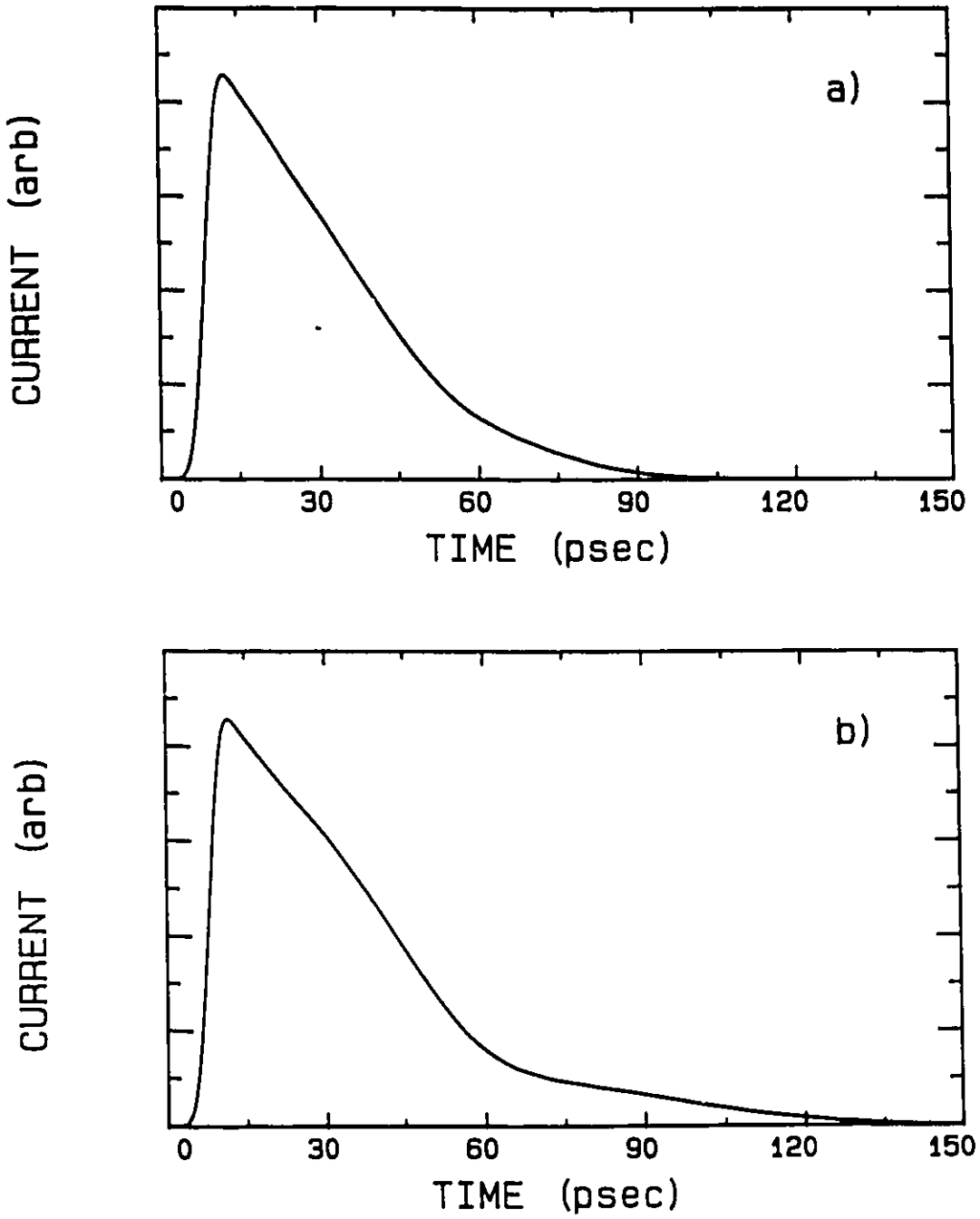


Figure 4.3 Response calculations using (a) the one dimensional model, and (b) the two dimensional model, for an interdigital device (G = x = 5 μm) on semi – insulating GaAs. A 4 psec input light pulse was used.

DIGIT G, x (μm)	APPLIED VOLTAGE (volts)	4 psec RISE 2D	RISE 1D	FWHM 2D	FWHM 1D
		GaAs (semi – insulating)			
5, 5	10.0	4.10	4.16	33.9	29.4
10, 10	15.0	4.17	4.24	58.1	54.4
15, 10	20.0	4.20	4.28	79.3	76.0
20, 10	15.0	4.27	4.27	72.2	67.6
20, 10	25.0	4.21	4.31	96.3	97.4
		SOS ($N_d = 5 \times 10^{15}$ cm^{-3})			
5, 5	10.0	6.10	4.79	18.7	13.1
5, 5	30.0	5.86	4.45	25.6	19.8
5, 5	50.0	4.95	4.25	33.5	25.4
10, 10	50.0	7.40	4.91	41.3	29.7
10, 10	120.0	4.85	4.26	68.6	50.3

Table 4.3 Comparison of results from a two dimensional model and a one dimensional model calculating the response to a 4 psec input light pulse of several different interdigital photodiodes.

DIGIT G, x (μm)	APPLIED VOLTAGE (volts)	70 psec RISE 2D	RISE 1D	FWHM 2D	FWHM 1D
		GaAs (semi – insulating)			
5, 5	10.0	55.1	54.4	83.5	79.8
10, 10	15.0	59.1	58.8	83.5	79.8
15, 10	20.0	61.9	61.6	113.	117.
20, 10	15.0	60.7	60.6	103.	108.
20, 10	25.0	63.8	63.5	129.	136.
		SOS ($N_d = 5 \times 10^{15}$ cm^{-3})			
5, 5	10.0	53.2	51.8	80.3	75.1
5, 5	50.0	54.9	53.2	82.1	76.0
10, 10	50.0	56.3	54.0	88.9	78.5
10, 10	120.0	60.3	58.0	104.	91.3

Table 4.4 Comparison of results from a two dimensional model and a one dimensional model calculating the response to a 70 psec input light pulse of several different interdigital photodiodes.

Tables 4.3 and 4.4 allow a specific comparison of the FWHM and rise time calculated by the one and two dimensional models. Table 4.4 shows results for a Gaussian input pulse with a FWHM of 70 psec. In general, when the input pulse is longer than, or on the order of, the device response time, the input pulse length will be the dominant factor in determining the output pulse length. This is true of the results shown in table 4.4, and the relatively good agreement between the models for the examples shown follows from this. Thus, if the input pulse is the dominant factor in determining the output response, a lesser degree of accuracy in the model can be tolerated.

Table 4.3 shows results for a gaussian input pulse with a 4 psec FWHM. For each device listed, the output response is dominated by the device response. This gives a true comparison of the response time calculated by the one and two dimensional models. For the SOS device calculations shown the agreement is poor, on the order of 30%. Agreement is much better for the GaAs device calculations, generally better than 10%. These results suggest that the one dimensional model can be used in place of the two dimensional model in many instances, depending on the degree of accuracy required.

Fundamentally, the ability to use the one dimensional model in place of the two dimensional model is dependent on the degree to which the two dimensional effects in the interdigital diode can be neglected. A simple example of this can be illustrated using the impulse response calculations for GaAs devices in table 4.5. For these examples, 90% of the incident light was absorbed in the first 0.5 μm of semiconductor. Using 0.5 μm as the effective semiconductor thickness, the data in table 4.5 show that as the ratio of digit separation to effective semiconductor thickness decreases, the relative difference between the FWHM calculated by the

DIGIT G x (μm)	APPLIED VOLTAGE (volts)	τ_t (psec)	FWHM 2D	FWHM 1D	PERCENT DIFFERENCE 2D, 1D
		GaAs (semi – insulating)			
1, 1	3.0	5	7.72	5.78	25%
2, 2	5.0	10	14.0	11.1	21%
5, 5	10.0	25	33.9	29.4	13%
10, 10	15.0	50	58.1	54.4	6.2%
15, 10	20.0	75	79.3	76.0	4.2%
20, 10	15.0	100	72.2	67.6	6.4%
20, 10	25.0	100	96.3	97.4	1.1%
		SOS ($N_d = 5 \times 10^{15}$ cm^{-3})			
5, 5	10.0	6.4	18.7	13.1	30%
5, 5	30.0	15	25.6	19.8	23%
5, 5	50.0	21	33.5	25.4	24%
10, 10	50.0	24	41.3	29.7	28%
10, 10	120.0	48	68.6	50.3	26%

Table 4.5 Difference between the FWHM calculated by the two dimensional model and the one dimensional model for several different interdigital photodiodes assuming an approximate impulse response. Also shown is a commonly used approximation for transit time defined in equation 4.1.

one and two dimensional models increases. Thus as effective thickness, the dimension ignored by the one dimensional model, becomes comparable to the digit separation, the error in the one dimensional model increases. Additionally, the pulse shapes predicted by the one and two dimensional model shows increasing difference for the 1 μm device suggesting that in the extreme, the one dimensional model is unreliable.

For the SOS devices shown in table 4.5, the agreement between the one and two dimensional models is uniformly poor. This indicates a more significant two dimensional nature in these devices. The existence of a discontinuity in dielectric constant and a layer of doped semiconductor all make contributions which are ignored by the one dimensional model.

This discussion has demonstrated that the one dimensional model can give a reasonable approximation for the time response of an interdigital photodiode in many instances. The range of applicability of the one dimensional model is dependent on the application, but for initial calculations where computational speed is often more important than accuracy, the one dimensional model presents a practical compromise.

In many cases all that is required for the time response of a device is a value for the impulse FWHM or transit time. A commonly used approximation for this value is given by

(4.1) $$\tau_t = \frac{1}{2}\frac{d}{v_s}$$ (Garside 1982)

where d is the length of the high field region in the photodiode, and
v_s is the carrier saturation velocity (approximately 10^7 cm/sec in most cases).

Use of equation 4.1 is dependent on the electric field being large enough (approximately 10^4 volts/cm for silicon and GaAs) that the majority of photogenerated carriers travel at the saturation velocity. Values calculated using equation 4.1 are presented in table 4.5 for comparison with values calculated by the one and two dimensional models. An example of improper use of equation 4.1 is the GaAs device with a 20 μm digit separation and a 15 volt bias shown in table 4.5. In this example equation 4.1 gives a very poor approximation of the transit time because the average field in the device (approximately 7500 volts/cm) is too small. The agreement between the results obtained using equation 4.1 and the one dimensional model are otherwise good, due to the one dimensional nature of equation 4.1. Thus the applicability of this equation to interdigital photodiodes is similar to that of the one dimensional model, provided the conditions for use are met.

CHAPTER 5: SAMPLE APPLICATIONS

In the preceding chapters, various models have been presented which can be used to predict general interdigital photodiode performance as well as to design and optimize specific devices. This chapter describes two examples of how these models might be applied. The capacitance of an interdigital device is compared with a standard device, and an example of the design of an interdigital device for insertion in a microstrip line is discussed.

It is interesting and instructive to compare the capacitance of an interdigital photodiode with that of an equivalent p–i–n photodiode. P–i–n photodiodes are one of the most common types of photodetector in use and represent an appropriate standard for comparison. The comparison will include only the active areas of these detectors, since bonding pad area is specific to the implementation and can in fact be eliminated by using a microstrip line.

An analytical model which calculates the capacitance of interdigital diodes was introduced in chapter 3. The principal advantage of this model is its analytical form. By applying several simplifying assumptions, it is possible to reduce this model to a single analytical expression which can be directly compared with a similarly simplified expression for p–i–n photodiodes.

Consider an interdigital device which is completely (or nearly) depleted between the digits. If it is assumed that the ground plane capacitance is much smaller than the interdigital gap capacitance (which can be arranged by having h, the substrate thickness, much greater than W, the width of the device), and corrections for edge effects are ignored (which corresponds to a device having many digits), the capacitance is given approximately by equations 3.8, 3.9, 3.12 and 3.14.

Substituting and simplifying these equations yields

$$C_g = \frac{W\ l\ \pi\ \epsilon_0\ (\epsilon_r+1)}{4\,d\quad \ln\left[\frac{8\,d}{\pi\,x}\right]} \tag{5.1}$$

where $N \cong W/d$ was used to approximate the number of digits (valid for large N).

For the purposes of comparison, a p–i–n photodiode can be approximated as a parallel plate capacitor with the intrinsic region acting as the dielectric between heavily doped p and n layers. This capacitance is given by

$$C_{\shortparallel} = \frac{\epsilon_r\ \epsilon_0\ \ A}{L} \tag{5.2}$$

where A is the area of the device, and

L is the thickness of the intrinsic region.

A comparison of equations 5.1 and 5.2 shows they have a similar general form. The capacitance varies directly as the area and inversely as the primary structure parameter (d and L respectively).

If the areas of the two devices are assumed to be equal ($W\ l = \Lambda$), the ratio of the capacitances is given by

$$\frac{C_g}{C_{\shortparallel}} = \frac{(\epsilon_r + 1)}{\epsilon_r}\ \frac{\pi}{4\,d}\ \frac{L}{\ln\left[\frac{8\ \ d}{\pi\ \ x}\right]} \tag{5.3}$$

Equation 5.3 is further simplified by assuming that the carrier transit times must be equal in each device as a requirement of being equivalent devices. To a first

approximation this requires that the thickness of the intrinsic region in the p–i–n device, L, must be equal to the digit separation, G. The resulting ratio is

$$\frac{C_g}{C_{\parallel}} = \frac{(\epsilon_r + 1)}{\epsilon_r} \frac{\pi}{4} \frac{(1 - \frac{x}{d})}{\ln\left[\frac{8}{\pi}\frac{d}{x}\right]} \tag{5.4}$$

where the substitution d = G + x has been used.

For the common case of $\frac{d}{x} = 2$, and assuming $\epsilon_r >> 1$, equation 5.4 reduces to 0.24 or approximately one quarter. Thus for this particular case a standard p–i–n photodiode has a capacitance which is four times larger than an equivalent interdigital device with a digit width equal to its digit separation.

As a specific example of the comparison, the capacitance of a 20 digit interdigital device has been calculated using Smith's model. The active area of the device was assumed to be square (W = *l*) and the digit width was set equal to the digit separation ($\frac{d}{x} = 2$). Figure 5.1 illustrates the results of these calculations as a function of digit separation for several different substrate thicknesses. Also shown is the capacitance of an equivalent p–i–n photodiode as previously defined. Comparing the capacitances of the interdigital device on a thick substrate with that of the p–i–n device gives a ratio of 0.26. This is in good agreement with the value of 0.24 found previously. For the interdigital device on a very thin substrate the agreement is poor due to the large ground plane capacitance, but as long as the digit separation is much less than the substrate thickness, the ratio of 0.25:1 is a good approximation.

As another example of the application of these tools, the design of an

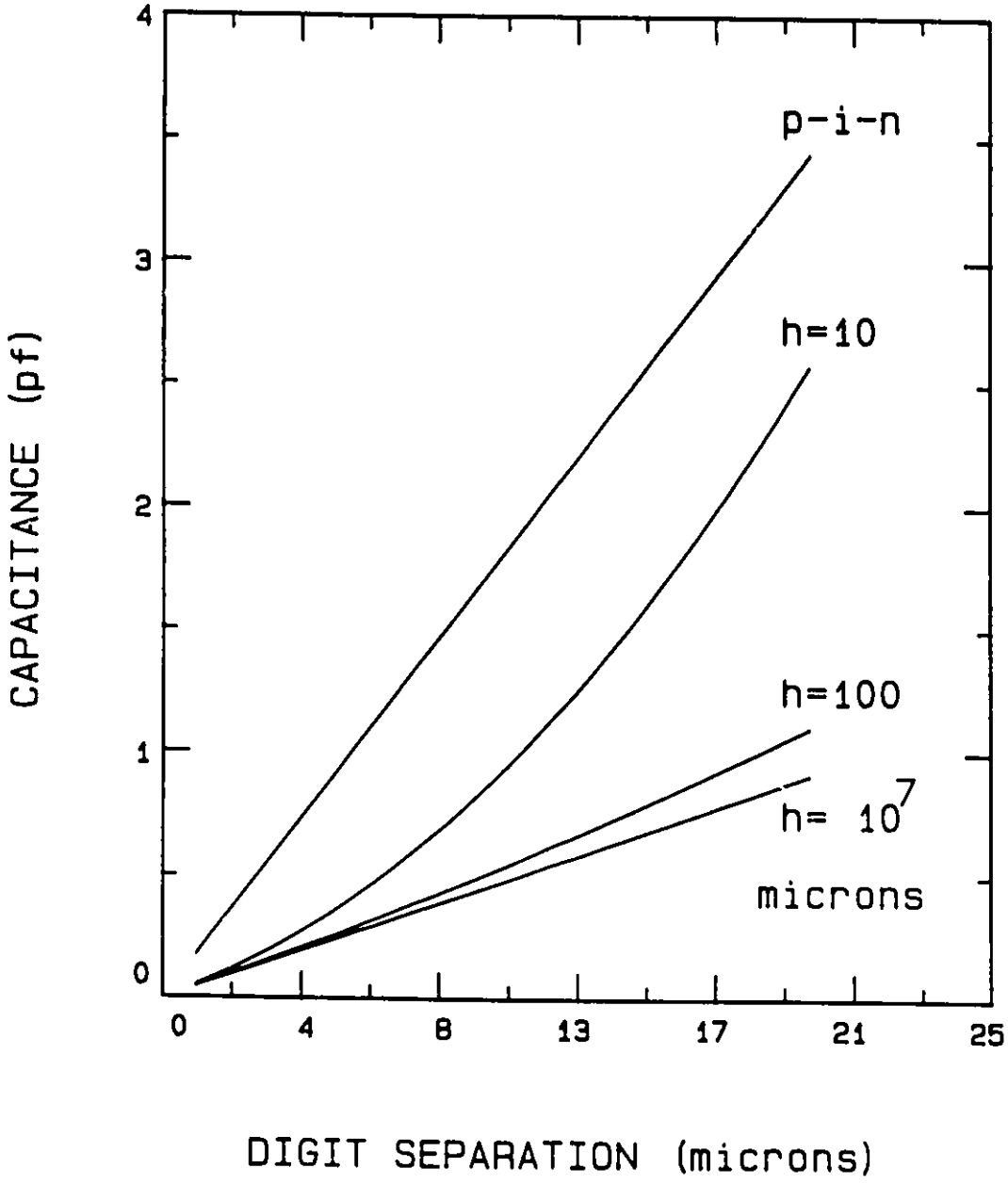


Figure 5.1 Capacitance of a 20 digit interdigital diode on semi – insulating GaAs for several substrate thicknesses (h). Capacitance of a p–i–n diode is included for comparison.

interdigital photodiode built into a microstrip line will be discussed. The basic design parameters will be as follows. The impedance of the microstrip line will be 50 ohms to match the standard coaxial cable used in these applications, and semi – insulating GaAs will be the substrate material ($\epsilon_r = 13.1$). To keep the design simple, the detector width will be the same as the width of the microstrip line, the detector will be square ($W = l$) and the digit width will be equal to the digit separation ($\frac{d}{x} = 2$).

The width of the microstrip line can be calculated using a simple relation given by Gupta (1979).

(5.5) $$\frac{2}{W}\frac{h}{} = \frac{1}{4}\exp(h') - \frac{1}{2}\exp(-h') \qquad W < h$$

where $$h' = \sqrt{\frac{(\epsilon_r + 1)}{2}}\,\frac{Z_{om}}{60} + \frac{\epsilon_r - 1}{\epsilon_r + 1}\left[0.226 + \frac{0.120}{\epsilon_r}\right]$$

Z_{om} is the characteristic impedance of the microstrip line

h is the thickness of the substrate

W is the width of the microstrip line

ϵ_r is the relative dielectric constant of the substrate.

Using the given parameters this reduces to

(5.6) $$W = 0.702\ h.$$

The width of the microstrip line, and thus the width of the device are fixed by the thickness of the substrate.

As stated in chapter 4, the temporal response of a photodetector is limited

by two fundamental factors, the RC time constant and the transit time. A very simple analysis shows that the RC time constant varies approximately inversely as the digit separation, and the transit time varies approximately directly as the digit separation. The result is a trade off between these two factors. To optimize the design it will be necessary to calculate the response time as a function of digit separation. In chapter 4, the response time was calculated by modeling the transit time response using a numerical model, and then numerically convolving this with the RC response. This is unnecessarily complicated and time consuming for a first design step. Instead a simplified model will be used.

If it is assumed that the transit time response to an impulse input takes the form of a right triangle (this is approximately true for devices operating at high fields as illustrated by figure 4.3), then this can be convolved with the RC response using Laplace transforms. The resulting convolved device response is given by

$$(5.7) \qquad i(t) = \alpha\left(1 + \frac{\alpha}{2\tau}\right)\left(1 - \exp\left[\frac{-t}{\alpha}\right]\right) - \frac{\alpha}{2\tau}t \qquad (t \le 2\tau)$$

$$= -\alpha \exp\left[\frac{-t}{\alpha}\right]\left(1 + \frac{\alpha}{2\tau}\left(1 - \exp\left[\frac{2\tau}{\alpha}\right]\right)\right) \qquad (t \ge 2\tau)$$

where τ is the FWHM of the right triangle giving the transit time, and

$\alpha = RC$.

The peak current value is found by setting the first derivative to zero for $t \le 2\tau$ (where the peak will always occur) and solving.

$$(5.8) \qquad i_{max} = \alpha\left(1 + \frac{\alpha}{2\tau}\ln\left[\frac{\alpha/2\tau}{1 + \alpha/2\tau}\right]\right)$$

Using equations 5.7 and 5.8, the FWHM of the response can be found by solving $i(t) = \frac{1}{2} i_{max}$ for t. In general this can not be done analytically, but can be done simply using numerical methods such as bisection, Newton's method, or the secant rule (Shampine 1973).

The results of solving for the FWHM as a function of α and τ is summarized as a general curve in figure 5–2 which plots $FWHM/\alpha$ as a function of $2\tau/\alpha$. A least squares fit on this data yields the equation

$$\text{FWHM} = \alpha\left(-0.00489\left[\frac{2\tau}{\alpha}\right]^2 + 0.652\left[\frac{2\tau}{\alpha}\right] + 0.711\right) \qquad (5.9)$$

$$0.1 < \frac{2\tau}{\alpha} < 20.$$

which is accurate to better than 2 % over the range indicated.

Equation 5.9 can be used along with Smiths model for the capacitance to calculate the response time as a function of digit separation. (Note that She's model could be used if an analytical calculation is required.) As a first step, a good approximation of the transit time in high field is given by $\tau = \frac{1}{2}\frac{G}{v_s}$, where v_s is the carrier saturation velocity (assumed to be 10^7 cm/sec). Examples of these calculations are shown in figure 5–3 which plots response time versus digit separation for several substrate thicknesses. These curves illustrate that due to the trade off between minimizing the RC time constant and the transit time, for each substrate thickness there is an optimum digit separation to obtain the minimum response time. If the curves in figure 5.3 are plotted with FWHM/h versus G/h, a single 'universal' curve results. Thus, in the range tested (100 μm $\leq$ h $\leq$ 1000 μm) a single minimum value can be used to represent the optimum digit separation to

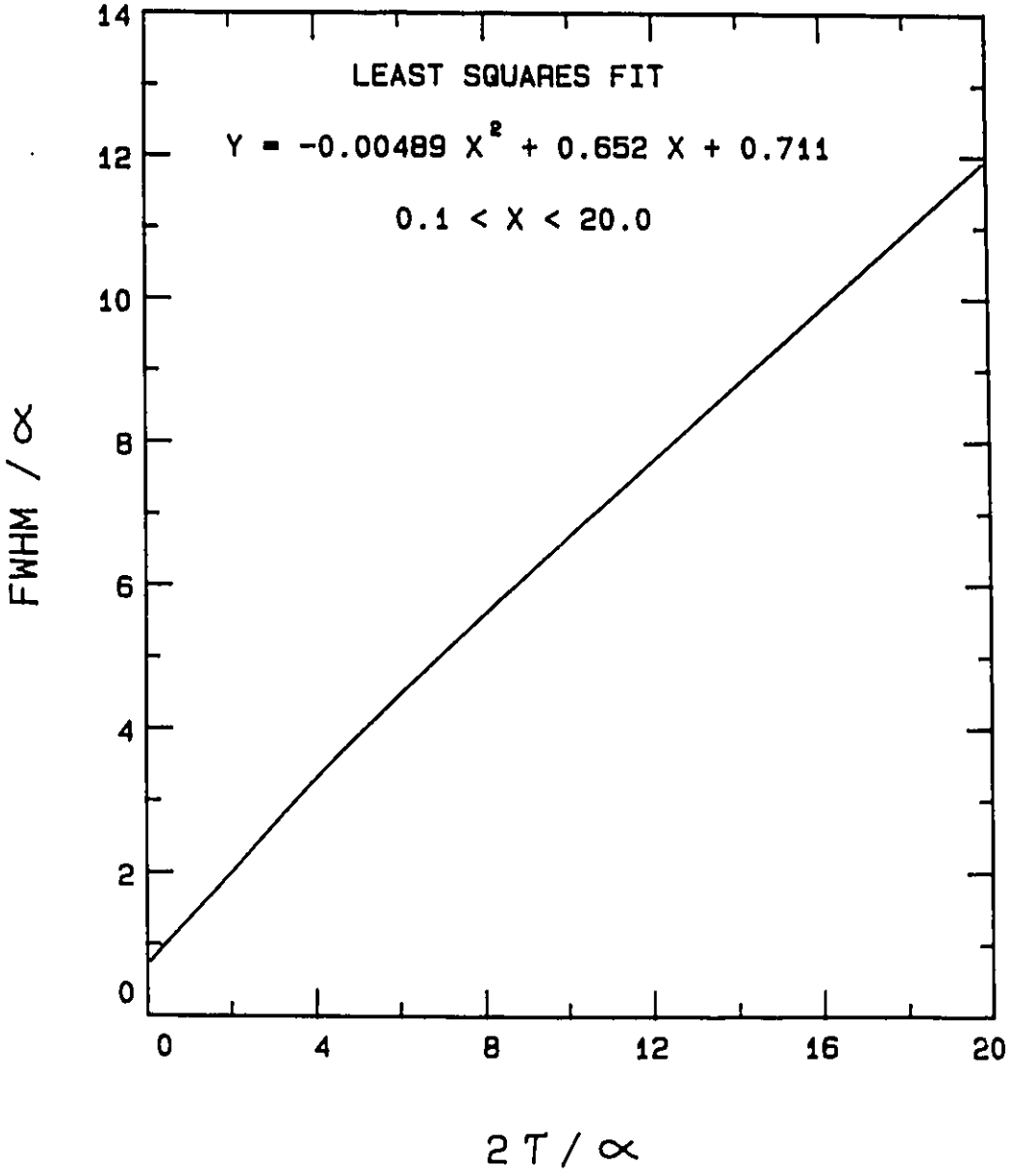


Figure 5.2 A general curve for calculation of the FWHM of the convolution of a right triangle (τ = FWHM) with a series RC circuit response (α = RC).

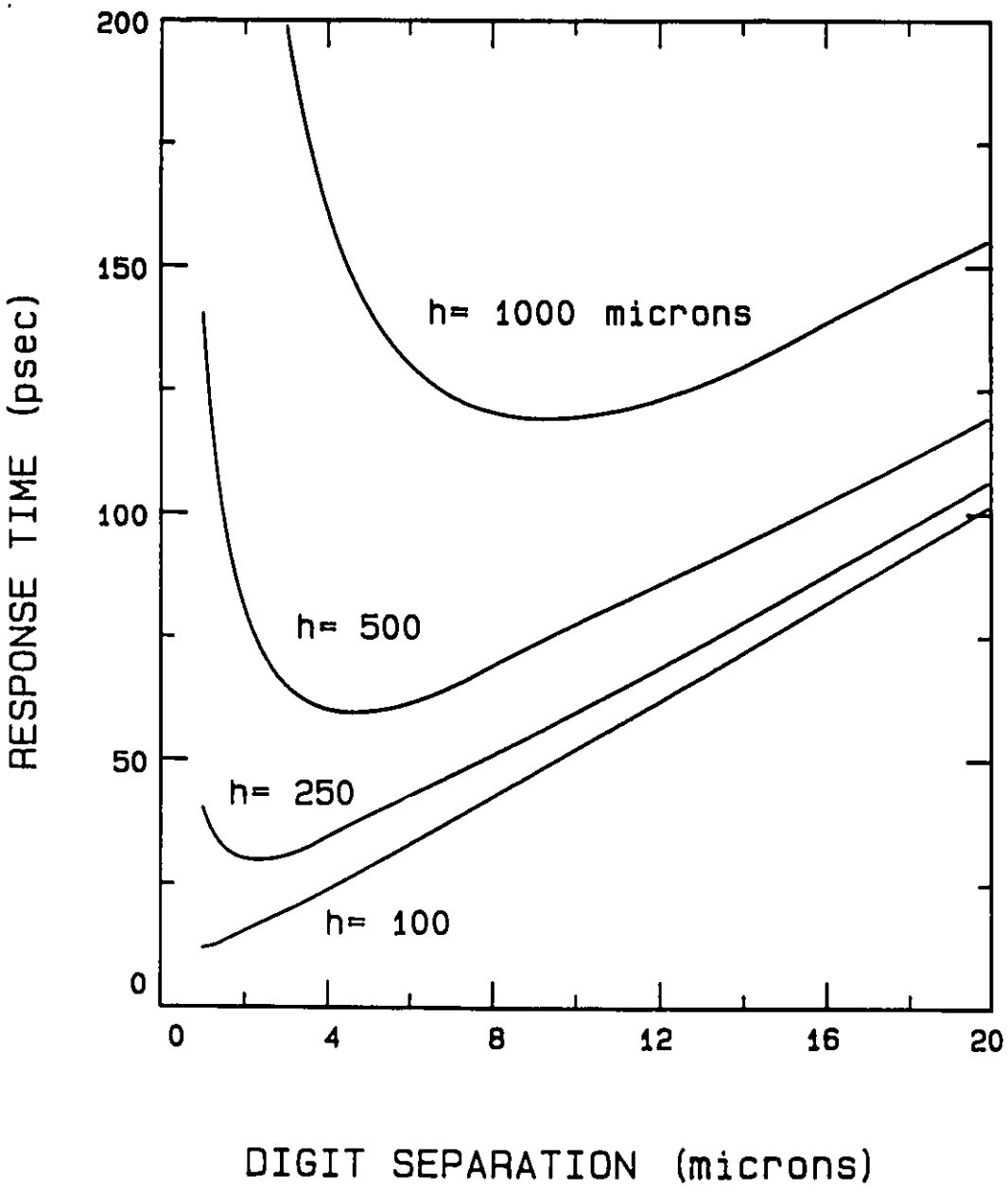


Figure 5.3 Response time versus digit separation for an interdigital diode in a 50 ohm microstrip line. Curves for several substrate thicknesses (h) are shown.

obtain a minimum response time for arbitrary h. The resulting expressions for this example are given by equations 5.10 and 5.11.

(5.10) $$G = 0.009333\ h$$

(5.11) $$FWHM = 0.1193\ h$$

where h is in μm, and

FWHM is in psec.

These results allow very general design and analysis of interdigital devices in a microstrip line. As a specific example of an application, consider the possible design of a device with a required response time of 50 psec. To begin, a 10 percent safety margin will be built in by designing for a 45 psec response. Using equation 5.11, the substrate thickness is calculated to be 377 μm, which is rounded to 375 μm. The microstrip line width is 263 μm by equation 5.3, and the digit separation is 3.50 μm by equation 5.10. These parameters can now be used in conjunction with the one dimensional model and the convolution routine to calculate the form of the response. The resulting curve is shown in figure 5.4 and has a rise time of 14.9 psec and a FWHM of 46.3 psec. Further analysis could be done using the two dimensional model or by experimental techniques to lead to a final design, but the results given here represent the necessary first steps in designing and understanding the device.

Although the design of an interdigital photodiode in a microstrip line on GaAs is a very specific example, the methodology used is generally applicable. Another example of a problem which could be solved in a similar manner would be finding the minimum response time, given the device area and substrate thickness,

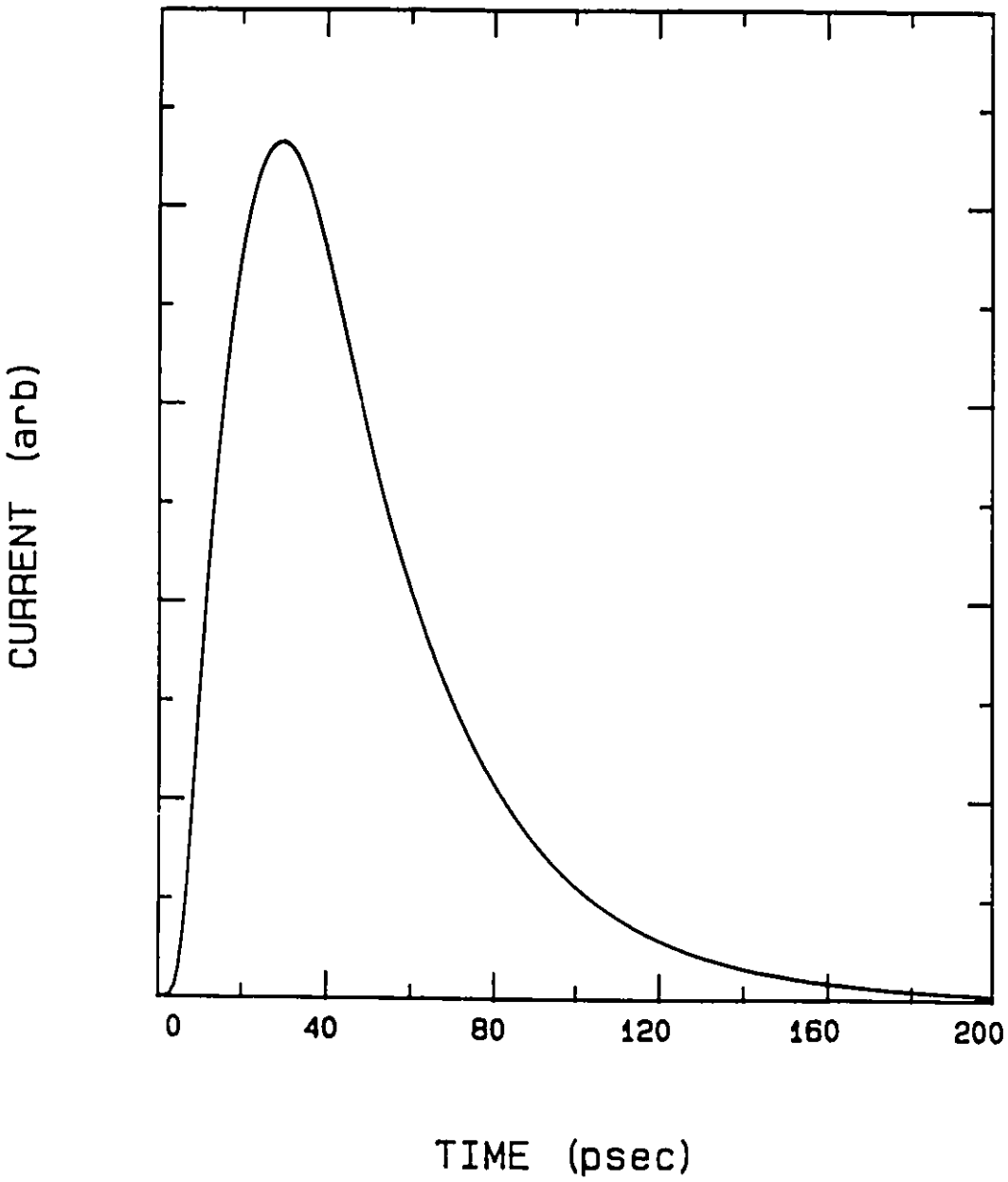


Figure 5.4 Impulse response of a 38 digit interdigital photodiode in a 50 ohm microstrip line. The device is on a 375 μm thick semi – insulating GaAs substrate and biased at 20 volts.

using epi – layer InGaAs; some preliminary analysis of this problem is discussed by Seymour (1988). These techniques can be used to solve a range of problems involving minimizing the response time, given specific design constraints, and this represents only one example of the possible applications of the models developed in this thesis.

SUMMARY

A fast, simple photodetector design consisting of an interdigital metal – semiconductor – metal (MSM) photodiode has been discussed. Initial work by other authors on these devices was limited to demonstrating their feasibility as fast sensitive detectors. This thesis has presented a variety of models and analysis which allow predictions of general device characteristics as well as the design and optimization of specific devices.

A two dimensional finite differences model based on Poisson's equation, and the continuity and current equations for semiconductors, was developed to allow numerical analysis of interdigital photodiodes. This two dimensional model was the basis of much of the theoretical analysis presented.

Experimental interdigital MSM photodiodes were fabricated on three sample materials; Semi – insulating GaAs, epi – layer GaAs, and silicon – on – sapphire (SOS). These materials represented a variety of the options available when choosing a material for interdigital photodiodes.

A discussion of the steady state characteristics placed the emphasis on photoresponse, current – voltage (IV), and capacitance – voltage (CV) characteristics. The photoresponse was measured as a function of wavelength and was discussed as a function of photon absorption. These results showed that interdigital photodiodes can operate in wavelength regions where the absorption coefficient is very large and most standard junction diodes exhibit a large reduction in photoresponse. Measurement of the absolute responsivity confirmed the existence of a gain mechanism at high bias voltages as reported by other authors.

A theoretical analysis of the IV characteristics of interdigital MSM diodes

was based on Sze's analytical model for one dimensional MSM diodes and the two dimensional numerical model for interdigital MSM diodes. The result was a system which allows general qualitative analysis of the IV characteristics of interdigital MSM diodes.

Particular emphasis was placed on the calculation of capacitance due to its importance as a factor in determining the measurable time response of a given device. Using the two dimensional numerical model, it was demonstrated that the total capacitance of an interdigital diode operating at a voltage equal to (or greater than) its reach – through voltage is approximated by the interdigital structure capacitance. Three models for the calculation of the structure capacitance were discussed. The two dimensional numerical model is functionally exact, but requires substantial computer resources. The modified version of a model due to Smith also requires a computer to run, but is fast and in good agreement with the numerical model. She's analytical model is useful for general analysis but gives reasonable numbers only when the digit separation is larger than the digit width. All three models were compared with experiment and shown to be in generally good agreement.

The pulse response of interdigital photodiodes was measured and compared with theoretical results. The measurement system used a sampling scope to displaying the response of the photodiode to an approximately known light pulse (70 psec FWHM diode laser or 4 psec FWHM dye laser). The factors affecting the observed time response were discussed. They were the device response, RLC circuit response, and sampling head response. The theoretical response was obtained by convolving the device response calculated using the two dimensional numerical model with the RLC circuit response and the sampling head response.

The parasitic inductance in the RLC circuit was unknown and was used as a fitting parameter. There was good agreement between the theoretical and experimental results.

As an alternative to the computationally slow two dimensional numerical model, the time dependent response was also calculated using a faster one dimensional model. It was demonstrated that in many instances the one dimensional model is a reasonable alternative to the two dimensional model. This is dependent on the error which can be tolerated and on the extent of the two dimensional nature of the interdigital device being modeled.

Two specific examples of the application of the tools developed in this thesis were presented. It was demonstrated that an interdigital diode could be designed to have approximately one quarter of the capacitance of an equivalent p–i–n diode. This illustrated one advantage of these devices. A sample design of an interdigital photodiode to be built into a 50 ohm microstrip line was also presented. The design was optimized for minimum response time. These two examples illustrate the capabilities of the models and analysis presented in this thesis to make general predictions of interdigital photodiode performance, as well as to design and optimize devices with specific operating parameters.

Appendix 1: NUMERICAL MODEL

The numerical methods used in this work are based on equations 1.1 through 1.6. These equations are known as the basic semiconductor equations and are reepeated here.

Poisson's equation:

$$\text{(A1.1)} \qquad \text{div grad } \psi = \frac{q}{\epsilon}\left(n - p - C \right)$$

Continuity equations:

$$\text{(A1.2)} \qquad \text{div } \vec{J}_n - q\frac{\partial n}{\partial t} = qR$$

$$\text{(A1.3)} \qquad \text{div } \vec{J}_p + q\frac{\partial p}{\partial t} = -qR$$

Current equations:

$$\text{(A1.4)} \qquad \vec{J}_n = qn\mu_n\vec{E} + q\,D_n\text{grad } n$$

$$\text{(A1.5)} \qquad \vec{J}_p = qp\mu_p\vec{E} - q\,D_p\text{grad } p$$

Total current:

$$\text{(A1.6)} \qquad \vec{J}_t = \vec{J}_n + \vec{J}_p + \frac{\partial}{\partial t}(\epsilon\vec{E})$$

where ψ is the electrostatic potential

$\vec{E}$ is the electric field vector

q is the elementary charge (= 1.602 x 10^{-19} Coulombs)

ϵ is the absolute permittivity

n, p are the electron and hole concentrations

C is the net fixed ionic charge

$\vec{J}_n$, $\vec{J}_p$, $\vec{J}_t$ are the electron, hole, and total current densities

t is the time

R is the net carrier recombination/generation

μ_n, μ_p are the electron and hole mobilities

D_n, D_p are the electron and hole diffusion coefficients

A1.1 Potential Routine

The potential solving routine calculates the potential distribution using only Poisson's equation. This program is also responsible for defining the structure of the device to be modeled as well as the discretized mesh used in this and the following routines. Figure A1.1 shows a general form of the structure modeled. Dashed lines represent the boundaries of the model domain.

The domain contains a rectangular mesh of points on which a solution of the semiconductor differential equations is sought using the finite differences method. The mesh is set by the programmer during initial setup of the program and varied

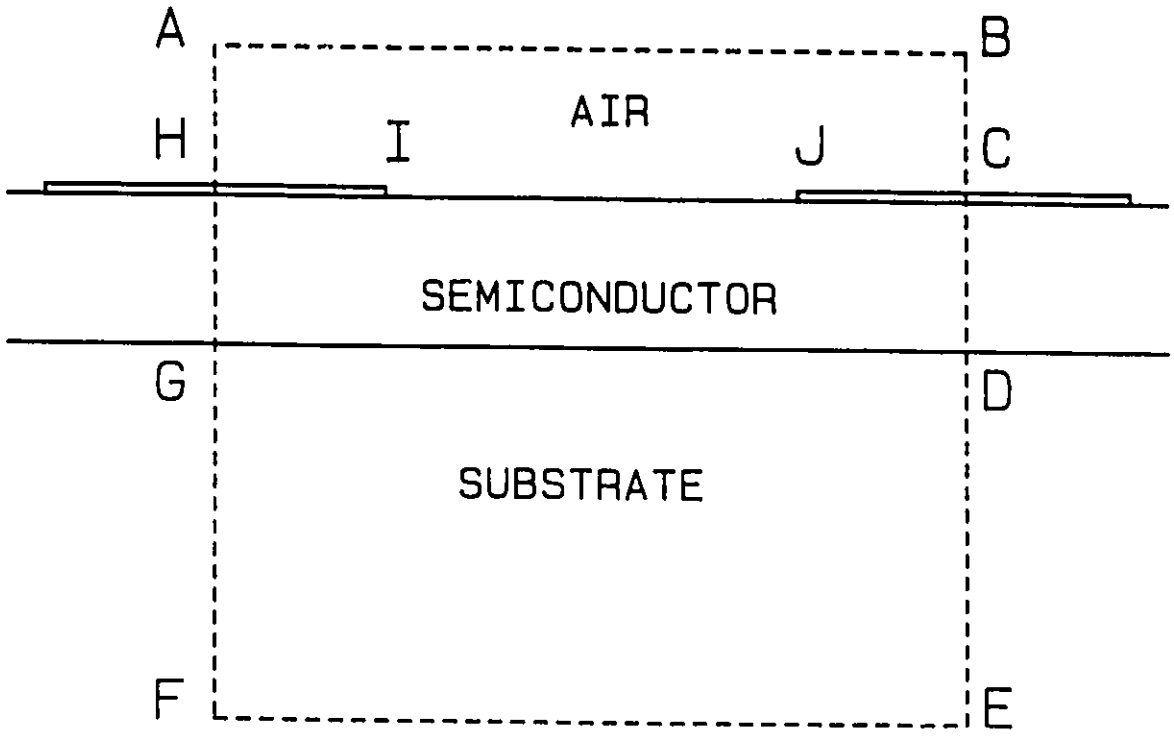


Figure A1.1 General form of the structure modeled with the boundaries of the model domain indicated by the dashed lines.

to suit the application. Best results were obtained using the following guidelines. Extra vertical grid lines were added close to boundaries AF and BE where Neumann boundary conditions are used. Extra vertical grid lines were also added at the edge of the digits to minimize local truncation error due to the singularity represented by this point (Laux, 1981.) By redistributing the existing grid points in these areas the transition in grid spacing was done smoothly.

All other regions of the domain used a uniform grid with constant though not necessarily equal, vertical and horizontal grid spacings. Some attempts were made to optimize the grid spacing in regions of rapidly varying potential or carrier concentration, but the results were inconclusive. In general, the results obtained using the quasi – uniform grid were as good or better, and had the added advantage of simplicity.

Solution of Poisson's equation in isolation from the other basic semiconductor equations requires several simplifying assumptions. For any doping concentration large enough to significantly perturb the potential distribution, the majority carrier density will be much greater than the minority carrier density. Thus only the ionized doping density and the majority carrier density need to be considered in calculating the total charge. Calculation of the majority carrier density is based on two assumptions. It is assumed that there is no current flow in the device and no generation or recombination. Although this is a simplification, the current flow in a reverse biased diode in thermal equilibrium is generally much smaller than the current which would be required to significantly perturb the majority carrier distribution. It is also assumed that Boltzmann statistics apply to the carrier densities. This is a valid approximation of Fermi – Dirac statistics as

long as the material is not degenerately doped. These conditions combine to yield the Boltzmann relation for the majority carrier density which, assuming n – type material is

(A1.7) $$n=n_o \exp (q\psi / kT)$$

where n_o is the thermal equilibrium carrier density and is set equal to the net doping density

q is the elementary charge

k is Boltzmann's constant

T is the absolute temperature.

The total charge density can be written as

(A1.8) $$\rho = - qN_d [1 - \exp (q\psi / kT)]$$

where N_d is the net doping density. In this application ψ must be negative to obtain the required reverse biased contact. Thus the form of the differential equation to be solved is

(A1.9) $$\text{div grad } \psi = \frac{- qN_d}{\epsilon} [1 - \exp (q\psi / kT)]$$

This expression contains nonlinear functions and was linearized using a Taylor series expansion with the higher order terms neglected.

(A1.10) $$\psi = \psi_o + \Delta\psi$$

$$\text{(A1.11)} \qquad \text{div grad } \psi + \frac{qN_d}{\epsilon}\left[1 - \exp\left[\frac{q\psi_o}{kT}\right]\left[1 + \frac{q}{kT}(\psi - \psi_o)\right]\right] = 0$$

Equation A1.11 is solved in an iterative fashion by calculating a new ψ using ψ_o from the previous iteration.

Discretization of equation A1.11 into a form suitable for finite differences solution was done using the box method as discussed by Bank et. al. (1983) with the appropriate difference approximation for the first derivatives. For example,

$$\text{(A1.12)} \qquad \left.\frac{\partial \psi}{\partial x}\right|_{i+\frac{1}{2},j} = \frac{\psi_{i+1,j} - \psi_{i,j}}{h_i}$$

(A1.13)

$$\frac{\dfrac{\psi_{i+1,j} - \psi_{i,j}}{h_i} - \dfrac{\psi_{i,j} - \psi_{i-1,j}}{h_{i-1}}}{\frac{1}{2}(h_{i-1} + h_i)} + \frac{\dfrac{\psi_{i,j+1} - \psi_{i,j}}{k_j} + \dfrac{\psi_{i,j} - \psi_{i,j-1}}{k_{j-1}}}{\frac{1}{2}(k_{j-1} + k_j)}$$

$$- \frac{qN_d}{\epsilon_s}\frac{q}{kT}\exp\left[\frac{q}{kT}\psi^o_{i,j}\right]$$

$$= \frac{qN_d}{\epsilon}\left[1 - \exp\left[\frac{q}{kT}\psi^o_{i,j}\right]\left[1 - \frac{q}{kT}\psi^o_{i,j}\right]\right]$$

where the indexing scheme is illustrated in figure A1.2. The form of this equation used in insulator materials is obtained by setting N_d to zero.

Equation A1.13 is solved over the closed domain bounded by the rectangle ABEF shown in figure A1.1 The following boundary conditions are used over this domain. Along lines AF and BE Neumann boundary conditions are used to reflect

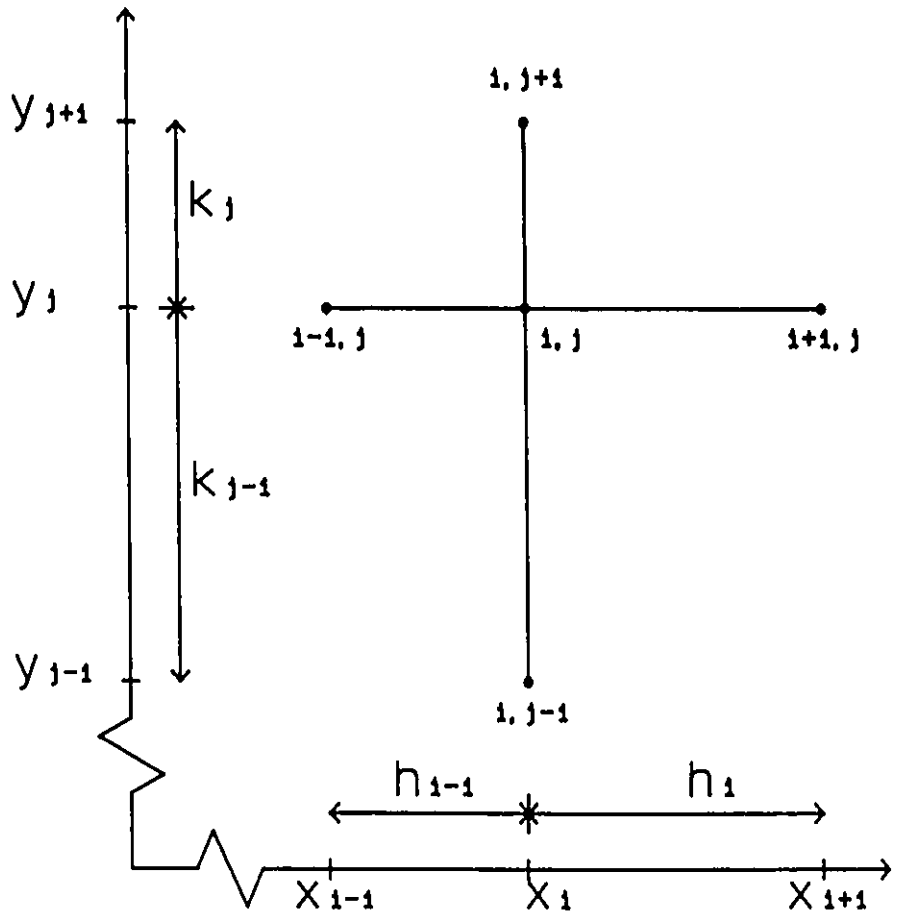


Figure A1.2 The indexing scheme used to discretize the semiconductor equations.

the symmetry of the device about these lines. Neumann boundary conditions can be stated generally as

(A1.14) $$\frac{\partial}{\partial \vec{n}} = 0$$

where $\vec{n}$ is the normal vector. Implementation of these boundary conditions is illustrated by

(A1.15) $$\psi (0^-, y) = \psi (0^+, y)$$

Lines HI and JC represent reverse and the forward biased digits respectively. At points on these lines the potential is fixed and Dirichlet boundary conditions are used, as represented by ;

(A1.16) $$\psi (x, y) = \psi_0$$

AB represents a line in air above the device. For an infinite thickness of air the potential along this line is related to the potential along the grid line just below it by Green's formula (Wasserstrom 1970):

(A1.17) $$\psi(x,y+\Delta y) = \frac{\Delta y}{\pi} \int_{-\infty}^{\infty} \frac{dx' \, \psi(x',y)}{(x-x')^2 + (\Delta y)^2} .$$

The discretized form of this equation is

(A1.18)

$$V_{i,j} = \sum_{b=-p}^{p} \sum_{m=1}^{imax} V_{m,j-1} \left\{ \tan^{-1} \left[\frac{2bx_{imax} - x_i + \left(x_m + \frac{1}{2} h_m \right)}{k_{j-1}} \right] \right.$$

$$- \tan^{-1} \left[\frac{2bx_{imax} - x_i + \left(x_m - \frac{1}{2} h_{m-1} \right)}{k_{j-1}} \right]$$

$$+ \tan^{-1} \left[\frac{2bx_{imax} - x_i - \left(x_m - \frac{1}{2} h_{m-1} \right)}{k_{j-1}} \right]$$

$$\left. - \tan^{-1} \left[\frac{2bx_{imax} - x_i - \left(x_m + \frac{1}{2} h_m \right)}{k_{j-1}} \right] \right\}$$

where $x_m = x_1 + \sum_{i=2}^{m} h_i$, $x_1 = 0$.

The limits of this summation, p and –p, represent the extension of this expression over multiple unit cells.

EF represents a line equivalent to AB in the substrate material. If the substrate is of finite thickness, then line EF represents a ground plane with a fixed potential. If the substrate is of infinite thickness, or if the effects of the ground plane can be neglected, then Green's function is used to calculate the potential along this line.

Lines IJ and GD represent interface boundaries between materials with different dielectric constants. At these interfaces the following conditions must be true (Lorrain 1970): the potential must be continuous across the interface; the tangential component of the electric field must be continuous across the interface; and the normal component of the electric displacement must be continuous across the interface if there is no surface charge. These conditions result in a modified

form of equation A1.13 for use along the interfaces.

(A1.19)

$$\frac{\frac{\psi_{i+1,j}-\psi_{i,j}}{h_i}-\frac{\psi_{i,j}-\psi_{i+1,j}}{h_{i-1}}}{\frac{1}{2}(h_{i-1}+h_i)}+\frac{\frac{\epsilon_1(\psi_{i,j+1}-\psi_{i,j})}{k_j}-\frac{\epsilon_2(\psi_{i,j}-\psi_{i,j-1})}{k_{j-1}}}{\frac{1}{2}(\epsilon_2 k_{j-1}+\epsilon_1 k_j)}$$

$$-k_{j-1}\,q\,N_d\,\frac{q}{kT}\exp\left[\frac{q}{kT}\psi^{\varrho}_{i,j}\right]\psi^{\varrho}_{i,j}$$

$$=-k_{j-1}\,q\left\{Q_{int}+N_d\left[1-\exp\left[\frac{q}{kT}\psi^{\varrho}_{i,j}\right]\left[1+\frac{q}{kT}\psi^{\varrho}_{i,j}\right]\right]\right\}$$

where it is assumed the top layer is an insulator,

ϵ_1, ϵ_2 are the dielectric constants of the insulator and semiconductor respectively, and

Q_{int} is the interface charge, if any.

Combining equations A1.18 and A1.19 with the boundary conditions over the entire grid results in a large system of algebraic equations. This system of equations is solved iteratively using Successive Line Overrelaxation (SLOR). Horizontal lines are used and the resulting tridiagonal matricies are solved with a special form of Gaussian elimination (see for example Kurata, 1968). Convergence of the solution is tested by finding the largest change in potential for a complete iteration, $\delta\psi^{max}_{i,j}$. If $\delta\psi^{max}_{i,j}$ is less than a prescribed limit, the solution is considered complete.

A1.2 Steady State Routine

The steady state condition is satisfied when the time derivatives in equations A1.2 and A1.3 are zero, yielding the steaady state continuity equations.

(A1.20) $$\text{div}\,\vec{J}_n = qR$$

(A1.21) $$\text{div}\,\vec{J}_p = -qR$$

The steady state routine simultaneously solves the steady state continuity equation as well as Poisson's equation and the current equations in a self consistent manner.

It is necessary to start by defining models for the various physical parameters. One of the more important quantities with regard to photodetectors is the field dependence of the carrier mobility. Mobility is dependent on carrier type and material. It was modeled using the following empirical formulas from the literature, with minor modifications. For silicon (Reisler, 1973):

(A1.22) $$\mu_n = \frac{2\,\mu_{no}}{1 + \sqrt{1 + \left[\frac{2\mu_{no}|\vec{E}|}{v_{sat}}\right]^2}}$$

(A1.23) $$\mu_p = \frac{2\mu_{po}}{1 + \sqrt{1 + \left[\frac{2\mu_{po}|\vec{E}|}{v_{sat}}\right]^2}}$$

For GaAs (Gammel, 1980)

(A1.24)
$$\mu_n = \frac{2.55\ \mu_{no} + \dfrac{|E|^3}{(3600)^4} \cdot v_{sat}}{2.55 + \left[\dfrac{|E|}{3600}\right]^4}$$

(A1.25)
$$\mu_p = \frac{\mu_{po}}{\sqrt{1 + \left[\dfrac{\mu_{po}|E|}{v_{sat}}\right]^2}}$$

where μ_{no} and μ_{po} are the respective low field mobilities,

$|\vec{E}|$ is the magnitude of the electric field and

v_{sat} is the saturation velocity ($\approx 10^7$ cm/sec for GaAs and Silicon).

It is customary to replace the diffusion coefficients, D_n and D_p, using the Einstein relationships:

(A1.26)
$$D_n = \frac{kT}{q}\mu_n$$

(A1.27)
$$D_p = \frac{kT}{q}\mu_p$$

These relationships are consistent with the current relations used and are valid for nondegenerate semiconductors.

Generation and Recombination have been broken up into four processes. The first process is the generation of carriers due to optical excitation. This generation rate is an input parameter which is modulated through the depth by an absorption coefficient according to the standard absorption formula

(A1.28) $$G(x) = G_o \exp(-\alpha x)$$

where G_o is the input generation rate

α is the absorption coefficient, and

x is the depth.

If $\alpha = 0$ then the generation rate is uniform through the depth. It is also possible to choose a uniform horizontal generation rate, or a Gaussian shaped spot of arbitrary width and location.

The standard fundamental generation/recombination process is generally modeled using a Shockley – Read – Hall (SRH) recombination model. The form used here is

(A1.29) $$R^{srh} = \frac{pn - n_i^2}{\tau (n + p + 2n_i)}$$

where n_i is the intrinsic carrier concentration and

τ is the carrier lifetime.

Equation A1.29 assumes single energy level traps located at the centre of the energy band with equal hole and electron capture cross sections.

The second generation/recombination mechanism considered was Auger recombination. The general form given by Selberherr (1984) is

(A1.30) $$R^{au} = (C_n^{au} n + C_p^{au} p) (np - n_i^2)$$

where $C_n^{au} = 2.8 \times 10^{-31}$ cm^6/sec and

$C_p^{au} = 9.9 \times 10^{-32}$ cm^6/sec are the Auger coefficients for bulk silicon.

Order of magnitude comparison of R^{au} with R^{srh} for bulk silicon shows that the Auger term is negligible until the excess carrier concentration is on the order of 10^{18} cm^{-3}. This is generally not the case, so this term is included only in cases of very large optical generation.

The final recombination process considered is surface recombination. It is generally considered to have a form which is equivalent to the Shockley – Read – Hall expression. However it is customary to use surface recombination velocities in place of carrier lifetimes, although this is just a matter of interpretation. The form of surface recombination used here is

(A1.31) $$R_{surf} = \frac{np - n_i^2}{\frac{1}{s} (n + p + 2n_i)} \delta(\vec{x} - \vec{x}_{surf})$$

where s is the surface recombination velocity and

$\delta(\vec{x})$ is the Dirac delta function.

The domain over which the basic semiconductor equations are to be solved is defined by the potential routine in step one and is illustrated in figure A1.1. For Poisson's equation the boundary conditions on the edge of the domain are identical to those used in step one. Along lines AF and BE Neumann boundary conditions hold, and along lines AB and EF Green's formula is used. More details can be found in the discussion of the potential routine above.

For the current and continuity equations, regions ABCH and GDEF have been defined as insulators. As such these regions can have no free carriers and the current equations are identically zero, Thus the current and continuity equations need only be solved over the subdomain HCDG bounding the semiconductor region.

Symmetry can again be invoked to allow the use of Neumann boundary conditions along the lines HG and CD. Mathematically this is expressed as

(A1.32) $$\frac{\partial n}{\partial \vec{n}} = 0 \quad \text{and} \quad \frac{\partial p}{\partial \vec{n}} = 0$$

where $\vec{n}$ is the unit normal vector.

On the digits which are represented by lines HI and JC Dirichlet boundary conditions are used. The exact values depend on the type of contact represented by the particular digit. For Schottky barrier contacts, the values given by Yoshii (1982) were used.

(A1.33) $$n = n_o \exp\left[\frac{q}{kT}\psi_s\right]$$

(A1.34) $$p = n_i^2 / n$$

where n_o is the thermal equilibrium carrier density and

ψ_s is the built in voltage due to the Schottky barrier.

For Ohmic contacts the common assumption of thermal equilibrium is used to obtain

(A1.35) $$n = n_o$$

(A1.36) $$p = n_i^2 / n_o = p_o$$

The interface between the semiconductor and the insulator are represented by lines IJ and GD. No current can flow through this interface, so the only current component through the interface is due to surface recombination. This is represented by

(A1.37) $$\vec{J} \cdot \vec{n} = - qR_{surf}$$

where $\vec{n}$ is the normal vector.

For the purposes of improved numerical stability, it is common practice to scale the dependent variables to have maximum values of order one. Scaling was accomplished using the method of DeMari (1968) with modifications suggested by Selberherr (1984). Table A1.1 lists the values used.

Scaling the variables also affects the semiconductor equations, producing the following scaled equations.

(A1.38) $$\lambda^2 \text{ div grad } \psi - (n - p - C) = 0$$

where $$\lambda^2 = \frac{\psi_o \epsilon}{x_o^2 q C_o}$$

This equation has been multiplied by $\frac{\epsilon}{q C_o}$.

Quantity	Symbol	Value
x,y	x_o	max $\|x\|$
ψ	ψ_o	max $\|\psi\|$
n,p,C	C_o	max $\|N_d(\vec{x})\|$
D_n,D_p	D_o	max $\left\| \frac{kT}{q} \mu_o \right\|$
μ_n,μ_p		D_o / ψ_o
R		$D_o C_o / x_o^2$
t		x_o^2 / D_o

Table A1.1 Values of scaling factors

(A1.39) $$\vec{J}_n = \mu_n \, n \, \text{grad} \, \psi - D_n \, \text{grad} \, n$$

(A1.40) $$\vec{J}_p = \mu_p \, p \, \text{grad} \, \psi - D_p \, \text{grad} \, p$$

where $\vec{E} = -\,\text{grad}\,\psi$ has been substituted

These equations have been multiplied by $\frac{x_o}{-\,q\;D_o\;C_o}$.

(A1.41) $$\text{div}\,(-\vec{J}_n) - R = \frac{\partial n}{\partial t} = 0$$

(A1.42) $$\text{div}\,(\vec{J}_p) - R = \frac{\partial p}{\partial t} = 0$$

These equations have been multiplied by $\frac{x_o^{\,2}}{D_o\;C_o}$.

Discretization of these equations begins with the current equations. Numerical instabilities result with the standard difference approximation when the voltage difference between adjacent mesh points exceeds $\frac{2kT}{q}$. This is unnecessarily restrictive, so an alternative method is used. Scharfetter and Gummel (1969) showed that a more general stability could be achieved by using an integral form of the current equations, as follows.

(A1.43)

$$J_n\big|_{i+\frac{1}{2},j} = \frac{\mu_n\big|_{i+\frac{1}{2},j}}{h_i}\left[B(\psi_{i,j} - \psi_{i+1,j}\,,\,U_t)n_{i,j} + B(\psi_{i,j} - \psi_{i+1,j}\,,\,-U_t)n_{i+1,j}\right]$$

(A1.44)

$$J_p\big|_{i+\frac{1}{2},j} = \frac{\mu_p\big|_{i+\frac{1}{2},j}}{h_i}\left[B(\psi_{i,j} - \psi_{i+1,j}\,,\,-U_t)p_{i,j} + B(\psi_{i,j} - \psi_{i+1,j}\,,\,U_t)p_{i+1,j}\right]$$

$$B(x, U_t) = \frac{x}{1 - \exp\left[\frac{x}{U_t}\right]} \tag{A1.45}$$

where $U_t = \frac{kT}{q}$ is the thermal voltage.

Before discussing the final discretized form of Poisson's equation and the continuity equations, it is useful to discuss their solution. As a result of the nonlinear form of the discretized continuity equations, a multistep process known as Newton's method is used. Using the formalization of Selberherr (1984), the continuity equations for electrons and holes are represented by F_1 and F_2 respectively and Poisson's equation by F_3. The complete nonlinear system is then,

$$F(n,p,\psi) = \begin{bmatrix} F_1(n,p,\psi) \\ F_2(n,p,\psi) \\ F_3(n,p,\psi) \end{bmatrix} \tag{A1.46}$$

A correction vector for the k^{th} Newton step is defined as

$$\begin{bmatrix} \delta n^k \\ \delta p^k \\ \delta \psi^k \end{bmatrix} = \begin{bmatrix} n^{k+1} - n^k \\ p^{k+1} - p^k \\ \psi^{k+1} - \psi^k \end{bmatrix} \tag{A1.47}$$

Newton's method at the k^{th} step is defined as the solution of

$$\begin{bmatrix} \frac{\partial F_1}{\partial n} & \frac{\partial F_1}{\partial p} & \frac{\partial F_1}{\partial \psi} \\ \frac{\partial F_2}{\partial n} & \frac{\partial F_2}{\partial p} & \frac{\partial F_2}{\partial \psi} \\ \frac{\partial F_3}{\partial n} & \frac{\partial F_3}{\partial p} & \frac{\partial F_3}{\partial \psi} \end{bmatrix}^k \begin{bmatrix} \delta n^k \\ \delta p^k \\ \delta \psi^k \end{bmatrix} = - \begin{bmatrix} F_1(n^k,p^k,\psi^k) \\ F\,(n^k,p^k,\psi^k) \\ F\,(n^k,p^k,\psi^k) \end{bmatrix} \tag{A1.48}$$

This is solved iteratively utilizing, for the m^{th} iteration;

(A1.49)

$$\begin{bmatrix} \frac{\partial F_1}{\partial n} & 0 & 0 \\ \frac{\partial F_2}{\partial n} & \frac{\partial F_2}{\partial p} & 0 \\ \frac{\partial F_3}{\partial n} & \frac{\partial F_3}{\partial p} & \frac{\partial F_3}{\partial \psi} \end{bmatrix}^k \begin{bmatrix} \delta n^k \\ \delta p^k \\ \delta \psi^k \end{bmatrix}^{m+1} = - \begin{bmatrix} F_1(n^k, p^k, \psi^k) \\ F\,(n\ , p\ , \psi^k) \\ F\,(n\ , p\ , \psi^k) \end{bmatrix} - \begin{bmatrix} 0 & \frac{\partial F_1}{\partial p} & \frac{\partial F_1}{\partial \psi} \\ 0 & 0 & \frac{\partial F_2}{\partial \psi} \\ 0 & 0 & 0 \end{bmatrix}^k \begin{bmatrix} \delta n^k \\ \delta p^k \\ \delta \psi^k \end{bmatrix}^m$$

Equation A1.49 represents three decoupled equations to be solved. The discretized form of these equations can be obtained by applying the box method to equations A1.38, A1.41 and A1.42 and using the discretized form of the current equations given by A1.43 and A1.44. The resulting equations are linearized by making the substitution represented by equation A1.47, using a Taylor expansion and neglecting higher order terms. Thus the final form of the equations used in this program are:

(A1.50)

$$\frac{\lambda^2\,(h_{i-1} + h_i)}{2k_{j-1}}\,\psi_{i,j-1} + \frac{\lambda^2\,(k_{j-1} + k_j)}{2h_{i-1}}\,\psi_{i-1,j}$$

$$- \lambda^2 \left[\frac{h_{i-1} + h_i}{2k_{j-1}} + \frac{k_{j-1} + k_j}{2h_{i-1}} + \frac{k_{j-1} + k_j}{2h_i} + \frac{h_{i-1} + h_i}{2k_j} \right] \psi_{i,j}$$

$$+ \frac{\lambda^2\,(k_{j-1} + k_j)}{2h_i}\,\psi_{i+1,j} + \frac{\lambda^2\,(h_{i-1} + h_i)}{2k_j}\,\psi_{i,j+1}$$

$$-\frac{(h_{i-1}+h_i)}{2}\frac{(k_{j-1}+k_j)}{2}(n_{i,j}-p_{i,j}-C_{i,j})=0$$

(A1.51)

$$-\mu_n|_{i,j-\frac{1}{2}}B(\psi_{i,j-1}-\psi_{i,j},U_t)\frac{2}{k_{j-1}(k_{j-1}+k_j)}(n_{i,j-1}+\delta n_{i,j-1})$$

$$-\mu_n|_{i-\frac{1}{2},j}B(\psi_{i-1,j}-\psi_{i,j},U_t)\frac{2}{h_{i-1}(h_{i-1}+h_i)}(n_{i-1,j}+\delta n_{i-1,j})$$

$$+\Big[-\mu_n|_{i,j-\frac{1}{2}}B(\psi_{i,j-1}-\psi_{i,j},-U_t)\frac{2}{k_{j-1}(k_{j-1}+k_j)}$$

$$-\mu_n|_{i-\frac{1}{2},j}B(\psi_{i-1,j}-\psi_{i,j},-U_t)\frac{2}{h_{i-1}(h_{i-1}+h_i)}$$

$$+\mu_n|_{i+\frac{1}{2},j}B(\psi_{i,j}-\psi_{i+1,j},U_t)\frac{2}{h_i(h_{i-1}+h_i)}$$

$$+\mu_n|_{i,j+\frac{1}{2}}B(\psi_{i,j}-\psi_{i,j+1},U_t)\frac{2}{k_j(k_{j-1}+k_j)}\Big](n_{i,j}+\delta n_{i,j})+\frac{\partial R_{i,j}}{\partial n_{i,j}}\delta n_{i,j}$$

$$+\mu_n|_{i+\frac{1}{2},j}B(\psi_{i,j}-\psi_{i+1,j},U_t)\frac{2}{h_i(h_{i-1}+h_i)}(n_{i+1,j}+\delta n_{i+1,j})$$

$$+\mu_n|_{i,j+\frac{1}{2}}B(\psi_{i,j}-\psi_{i,j+1},U_t)\frac{2}{k_j(k_{j-1}+k_j)}(n_{i,j+1}+\delta n_{i,j+1})$$

$$-\frac{2\,DN_{i+\frac{1}{2},j}(\delta\psi_{i+1,j}-\delta\psi_{i,j})}{h_i(h_{i-1}+h_i)}-\frac{2\,DN_{i-\frac{1}{2},j}(\delta\psi_{i-1,j}-\delta\psi_{i,j})}{h_{i-1}(h_{i-1}+h_i)}$$

$$-\frac{2\,DN_{i,j+\frac{1}{2}}(\delta\psi_{i,j+}-\delta\psi_{i,j})}{k_j(k_{j-1}+k_j)}-\frac{2\,DN_{i,j-\frac{1}{2}}\delta\psi_{i,j-1}-\delta\psi_{i,j})}{k_{j-1}(k_{j-1}+k_j)}$$

$$-\frac{\partial R_{i,j}}{\partial p_{i,j}}\delta p_{i,j}-R_{i,j}=0$$

(A1.52)

$$
\begin{aligned}
&- \mu_p|_{i,j-\frac{1}{2}}\, B(\psi_{i,j-1} - \psi_{i,j}, -U_t)\, \frac{2}{k_{j-1}\,(k_{j-1} + k_j)}\,(p_{i,j-1} + \delta p_{i,j-1}) \\
&- \mu_p|_{i-\frac{1}{2},j}\, B(\psi_{i-1,j} - \psi_{i,j}, -U_t)\, \frac{2}{h_{i-1}\,(h_{i-1} + h_i)}\,(p_{i-1,j} + \delta p_{i-1,j}) \\
&+ \Bigg[-\mu_p|_{i,j-\frac{1}{2}}\, B(\psi_{i,j-1} - \psi_{i,j}, U_t)\, \frac{2}{k_{j-1}\,(k_{j-1} + k_j)} \\
&- \mu_p|_{i-\frac{1}{2},j}\, B(\psi_{i-1,j} - \psi_{i,j}, U_t)\, \frac{2}{h_{i-1}\,(h_{i-1} + h_i)} \\
&= \mu_p|_{i+\frac{1}{2},j}\, B(\psi_{i,j} - \psi_{i+1,j}, -U_t)\, \frac{2}{h_i\,(h_{i-1} + h_i)} \\
&+ \mu_p|_{i,j+\frac{1}{2}}\, B(\psi_{i,j} - \psi_{i,j+1}, -U_t)\, \frac{2}{k_j\,(k_{j-1} + k_j)} \Bigg]\,(p_{i,j} + \delta p_{i,j}) + \frac{\partial R_{i,j}}{\partial p_{i,j}}\,\delta p_{i,j} \\
&+ \mu_p|_{i+\frac{1}{2},j}\, B(\psi_{i,j} - \psi_{i+1,j}, U_t)\, \frac{2}{h_i\,(h_{i-1} + h_i)}\,(p_{i+1,j} + \delta p_{i+1,j}) \\
&+ \mu_p|_{i,j+\frac{1}{2}}\, B(\psi_{i,j} - \psi_{i,j+1}, U_t)\, \frac{2}{k_j\,(k_{j-1} + k_j)}\,(p_{i,j+1} + \delta p_{i,j+1}) \\
&- \frac{2\ DP_{i+\frac{1}{2},j}\ (\delta\psi_{i+1,j} - \delta\psi_{i,j})}{h_i\,(h_{i-1} + h_i)} - \frac{2\ DP_{i-\frac{1}{2},j}\ (\delta\psi_{i+1,j} - \delta\psi_{i,j})}{h_{i-1}\,(h_{i-1} + h_i)} \\
&- \frac{2\ DP_{i,j+\frac{1}{2}}\ (\delta\psi_{i,j+1} - \delta\psi_{i,j})}{k_j\,(k_{j-1} + k_j)} - \frac{2\ DP_{i,j-\frac{1}{2}}\ (\delta\psi_{i,j-1} - \delta\psi_{i,j})}{k_{j-1}\,(k_{j-1} + k_j)} \\
&- \frac{\partial R_{i,j}}{\partial n_{i,j}}\,\delta n_{i,j} + R_{i,j} = 0
\end{aligned}
$$

(A1.53)

$$DN_{i+\frac{1}{2},j} = \frac{\mu_{n|i+\frac{1}{2},j}}{h_i}\left[\frac{(1+(Z-1)\exp Z)}{(1-\exp Z)^2}n_{i,j} + \frac{(1-(1+Z)\exp(-Z))}{(\exp(-Z)-1)^2}n_{i+1,j}\right]$$

(A1.54)

$$DP_{i+\frac{1}{2},j} = \frac{\mu_{p|i+\frac{1}{2},j}}{h_i}\left[\frac{(1-(1+Z)\exp(-Z))}{(\exp(-Z)-1)^2}p_{i,j} + \frac{(1+(Z-1)\exp Z)}{(1-\exp Z)^2}p_{i+1,j}\right]$$

where $Z = \dfrac{\psi_{i,j} - \psi_{i+1,j}}{U_t}$

$$R_{i,j} = R^{srh}_{i,j} + R^{au}_{i,j} - G_{i,j}$$

(A1.55)

$$\frac{\partial R_{i,j}}{\partial n_{i,j}} = -\frac{(p_{i,j} - \tau R^{srh}_{i,j})}{\tau(n_{i,j} + p_{i,j} + 2n_i^2)} - C_n(2n_{i,j}p_{i,j} - n_i^2) - C_p p_{i,j}^2$$

(A1.56)

$$\frac{\partial R_{i,j}}{\partial p_{i,j}} = \frac{(n_{i,j} - \tau R^{srh}_{i,j})}{\tau(n_{i,j} + p_{i,j} + 2n_i^2)} + C_p(2n_{i,j}p_{i,j} - n_i^2) + C_n n_{i,j}^2$$

Numerical implementation of these equations requires care in the evaluation of equation A1.45. To prevent a divide by zero error in evaluating this function near zero, it is necessary to use a series expansion form of the expression in this region. This problem as well as possible overflow are avoided using the following implementation.

(A1.57)

$$
B(x,U_t) = \begin{cases}
= x & (x / U_t) \le -x_1 \\
= \dfrac{x}{1 - \exp(x / U_t)} & -x_1 < \dfrac{x}{U_t} < -x_2 \\
= \dfrac{-U_t}{1 + \dfrac{x}{2U_t} + \dfrac{1}{4!}\left[\dfrac{x}{U_t}\right]^2 + \dfrac{1}{4!}\left[\dfrac{x}{U_t}\right]^3 + \cdots + \dfrac{1}{8!}\left[\dfrac{x}{U_t}\right]^7} & x > \left|\dfrac{x}{U_t}\right| \\
= \dfrac{x}{1 - \exp(x / U_t)} & x_2 \le \dfrac{x}{U_t} \le x_1 \\
= -x \exp(-x / U_t) & x_1 \le (x / U_t)
\end{cases}
$$

where the values of x_1 and x_2 depend on the computer and compiler used. The number of terms in the series expansion is also dependent on the implementation. These values were chosen to achieve a smooth transition between regions. In this application, eight series terms were required to allow a large enough value of x_2 to eliminate oscillations in the calculated value of the exponential for small x.

Solutions of the discretized equations A1.50 – A1.52 were found using two methods. Equation A1.50 was solved using SLOR as described for the potential routine. Equations A1.51 and A1.52 were solved using an iterative pentadiagonal matrix solving routine described by Stone (1968). Convergence was tested by

comparing the largest change of each of the three dependent variables for a complete Newton iteration with their respective preset error values.

A1.3 Time Dependent Routine

The time dependent routine solves the basic semiconductor equations as they are listed in equations A1.1 through A1.6. The major difference between this routine and the steady state solving routine discussed above is the inclusion of the time derivatives in the continuity equations. For this reason, only the implementation of the time derivatives will be discussed here. For other information, the reader is referred back to section A1.2 of this appendix.

Assuming scaled variables, the time derivatives are approximated using the standard difference formula (using n for example).

$$\frac{\partial n}{\partial t} = \frac{n_{i,j} - n_{i,j}^{0}}{\Delta t} \qquad \text{(A1.58)}$$

where Δt is the interval between time steps

$n_{i,j}$ is the electron density at this time step

$n_{i,j}^{0}$ is the electron density at the previous time step

Estimation of the derivatives at the midpoint of the time step interval is achieved using the method of Crank – Nicholson (see for example Kurata, 1982). This can be summarized as:

$$(A1.59) \qquad \frac{n_{i,j} - n^{o}_{i,j}}{\Delta t} = \frac{1}{2}\left[\text{div}\,(-J_n) - R \right]_{i,j} + \frac{1}{2}\left[\text{div}\,(-J_n^{o}) - R^{o} \right]_{i,j}$$

where the superscript, ^{o}, indicates values taken from the previous time step, and the scaled form of the continuity equations are used.

Poisson's equation, which has no time derivatives, is identical in both the steady state and time dependent applications. As a result, the form of Poisson's equation used in the time dependent solving routine is the same as equation A1.49 used in the steady state solving routine. The form of the continuity equations described in equation A1.59 is implemented in the same manner as the steady state continuity equations, producing the following equations:

$$(A1.60) \qquad - \frac{2\ \mu_n|_{i,j-\frac{1}{2}}\ B(\psi_{i,j-1} - \psi_{i,j}\ ,\ U_t)}{k_{j-1}\ (k_{j-1} + k_j)}\ (n_{i,j-1} + \delta n_{i,j-1})$$

$$- \frac{2\mu_n|_{i-\frac{1}{2},j}\ B(\psi_{i-1,j} - \psi_{i,j}\ ,U_t)}{h_{i-1}\ (h_{i-1} + h_i)}\ (n_{i-1,j} + \delta n_{i-1,j})$$

$$+ \left[\frac{-2\mu_n|_{i,j-\frac{1}{2}}\ B(\psi_{i,j-1} - \psi_{i,j};\ -U_t)}{k_{j-1}\ (k_{j-1} + k_j)} - \frac{2\mu_n|_{i-\frac{1}{2},j}\ B(\psi_{i-1,j} - \psi_{i,j},\ -U_t)}{h_{i-1}\ (h_{i-1} + h_i)} \right.$$

$$+ \frac{\mu_n|_{i+\frac{1}{2},j}\ B(\psi_{i,j} - \psi_{i+1,j}\ ,\ U_t)}{h_i\ (h_{i-1} + h_i)} + \frac{2\mu_n|_{i,j+\frac{1}{2}}\ B(\psi_{i,j} - \psi_{i,j+1}\ ,\ U_t)}{k_j\ (k_{j-1} + k_j)}$$

$$\left. - \frac{2}{\Delta t} \right] (n_{i,j} + \delta n_{i,j}) + \frac{\partial R_{i,j}}{\partial n_{i,j}}\, \delta n_{i,j}$$

$$+ \frac{2\mu_n|_{i+\frac{1}{2},j}\ B(\psi_{i,j} - \psi_{i+1,j}\ ,\ -U_t)}{h_i\ (h_{i-1} + h_i)}\ (n_{i+1,j} + \delta n_{i+1,j})$$

$$+ \frac{2\mu_n|_{i,j+\frac{1}{2}} B(\psi_{i,j} - \psi_{i,j+1}, -U_t)}{k_j (k_{j-1} + k_j)} (n_{i,j+1} + \delta n_{i,j+1})$$

$$- \frac{2\,DN|_{i+\frac{1}{2},j} (\delta\psi_{i+1,j} - \delta\psi_{i,j})}{h_i (h_{i-1} + h_i)} - \frac{2\,DN|_{i-\frac{1}{2},j} (\delta\psi_{i-1,j} - \delta\psi_{i,j})}{h_{i-1} (h_{i-1} + h_i)}$$

$$= \frac{2\,DN|_{i,j+\frac{1}{2}} (\delta\psi_{i,j+1} - \delta\psi_{i,j})}{k_j (k_{j-1} + k_j)} - \frac{2\,DN|_{i,j-\frac{1}{2}} (\delta\psi_{i,j-1} - \delta\psi_{i,j})}{k_{j-1} (k_{j-1} + k_j)}$$

$$- \frac{\partial R_{i,j}}{\partial p_{i,j}} - (R_{i,j} + R^o_{i,j})$$

$$- \frac{2\mu_n|_{i,j-\frac{1}{2}} B(\psi_{i,j-1} - \psi_{i,j}, U_t)}{k_{j-1} (k_{j-1} + k_j)} n^o_{i,j-1} - \frac{2\mu_n|_{i-\frac{1}{2},j} B(\psi^o_{i-1,j} - \psi^o_{i,j}; U_t)}{h_{i-1} (h_{i-1} + h_i)} n^o_{i-1,j}$$

$$+ \left[- \frac{2\mu^o_n|_{i,j-\frac{1}{2}} B(\psi^o_{i,j-1} - \psi^o_{i,j}, -U_t)}{k_{j-1} (k_{j-1} + k_j)} - \frac{2\mu^o_n|_{i-\frac{1}{2},j} B(\psi^o_{i-1,j} - \psi^o_{i,j}, -U_t)}{h_{i-1} (h_{i-1} + h_i)} \right.$$

$$+ \frac{2\mu^o_n|_{i+\frac{1}{2},j} B(\psi^o_{i,j} - \psi^o_{i+1,j}, -U_t)}{h_i (h_{i-1} + h_i)} + \frac{2\mu^o_n|_{i,j+\frac{1}{2}} B(\psi^o_{i,j} - \psi^o_{i,j+1}, -U_t)}{k_j (k_{j-1} + k_j)}$$

$$\left. + \frac{2}{\Delta t} \right] n^o_{i,j} + \frac{2\mu^o_n|_{i+\frac{1}{2},j} B(\psi^o_{i,j} - \psi^o_{i+1,j}, -U_t)}{h_i (h_{i-1} + h_i)} n^o_{i+1,j}$$

$$+ \frac{2\mu^o_n|_{i,j+\frac{1}{2}} B(\psi^o_{i,j} - \psi_{i,j+1}, -U_t)}{k_j (k_{j-1} + k_j)} n^o_{i,j+1} = 0$$

(A1.61)

$$
\begin{aligned}
&- \frac{2\ \mu_p|_{i,j-\frac{1}{2}}\ B(\psi_{i,j-1} - \psi_{i,j}\ ,\ -U_t)}{k_{j-1}\ (k_{j-1} + k_j)}\ (p_{i,j-1} + \delta p_{i,j-1}) \\
&- \frac{2\mu_p|_{i-\frac{1}{2},j}\ B(\psi_{i-1,j} - \psi_{i,j}\ ,\ -U_t)}{h_{i-1}\ (h_{i-1} + h_i)}\ (p_{i-1,j} + \delta p_{i-1,j}) \\
&+ \left[\frac{-2\mu_p|_{i,j-\frac{1}{2}}\ B(\psi_{i,j-1} - \psi_{i,j}\ ,\ U_t)}{k_{j-1}\ (k_{j-1} + k_j)} - \frac{2\mu_p|_{i-\frac{1}{2},j}\ B(\psi_{i-1,j} - \psi_{i,j}\ ,\ U_t)}{h_{i-1}\ (h_{i-1} + h_i)} \right. \\
&+ \frac{2\mu_p|_{i+\frac{1}{2},j}\ B(\psi_{i,j} - \psi_{i+1,j},-U_t)}{h_i\ (h_{i-1} + h_i)} + \frac{2\mu_p|_{i,j+\frac{1}{2}}\ B(\psi_{i,j} - \psi_{i,j+1},-U_t)}{k_j\ (k_{j-1} + k_j)} \\
&\left. + \frac{2}{\Delta t} \right] (p_{i,j} + \delta p_{i,j}) + \frac{\partial R_{i,j}}{\partial p_{i,j}}\ \delta p_{i,j} \\
&+ \frac{2\mu_p|_{i+\frac{1}{2},j}\ B(\psi_{i,j} - \psi_{i+1,j}\ ,\ U_t)}{h_i\ (h_{i-1} + h_i)}\ (p_{i+1,j} + \delta p_{i+1,j}) \\
&+ \frac{2\mu_p|_{i,j+\frac{1}{2}}\ B(\psi_{i,j} - \psi_{i,j+1}\ ,\ U_t)}{k_j\ (k_{j-1} + k_j)}\ (p_{i,j+1} + \delta p_{i,j+1}) \\
&- \frac{2\ DP|_{i+\frac{1}{2},j}\ (\delta\psi_{i+1,j} - \delta\psi_{i,j})}{h_i\ (h_{i-1} + h_i)} - \frac{2\ DP|_{i-\frac{1}{2},j}\ (\delta\psi_{i-1,j} - \delta\psi_{i,j})}{h_{i-1}\ (h_{i-1} + h_i)} \\
&- \frac{2\ DP|_{i,j+\frac{1}{2}}\ (\delta\psi_{i,j+1} - \delta\psi_{i,j})}{k_j\ (k_{j-1} + k_j)} - \frac{2\ DN|_{i,j-\frac{1}{2}}\ (\delta\psi_{i,j-1} - \delta\psi_{i,j})}{k_{j-1}\ (k_{j-1} + k_j)} \\
&- \frac{\partial R_{i,j}}{\partial n_{i,j}} + (\ R_{i,j} + R^{o}_{i,j}\ )
\end{aligned}
$$

$$- \frac{2\mu_p|_{i,j-\frac{1}{2}} B(\psi_{i,j-1} - \psi_{i,j}, -U_t)}{k_{j-1}(k_{j-1}+k_j)} p^o_{i,j-1}$$

$$- \frac{2\mu_p|_{i-\frac{1}{2},j} B(\psi^o_{i-1,j} - \psi^o_{i,j}, -U_t)}{h_{i-1}(h_{i-1}+h_i)} p^o_{i-1,j}$$

$$+ \left[- \frac{2\mu^o_p|_{i,j-\frac{1}{2}} B(\psi^o_{i,j-1} - \psi^o_{i,j}, U_t)}{k_{j-1}(k_{j-1}+k_j)} - \frac{2\mu^o_p|_{i-\frac{1}{2},j} B(\psi^o_{i-1,j} - \psi^o_{i,j}, U_t)}{h_{i-1}(h_{i-1}+h_i)} \right.$$

$$+ \frac{2\mu^o_p|_{i+\frac{1}{2},j} B(\psi^o_{i,j} - \psi^o_{i+1,j}, -U_t)}{h_i(h_{i-1}+h_i)} + \frac{2\mu^o_p|_{i,j+\frac{1}{2}} B(\psi^o_{i,j} - \psi^o_{i,j+1}, -U_t)}{k_j(k_{j-1}+k_j)}$$

$$\left. - \frac{2}{\Delta t} \right] p^o_{i,j} + \frac{2\mu^o_p|_{i+\frac{1}{2},j} B(\psi^o_{i,j} - \psi^o_{i+1,j}, U_t)}{h_i(h_{i-1}+h_i)} p^o_{i+1,j}$$

$$+ \frac{2\mu^o_p|_{i,j+\frac{1}{2}} B(\psi^o_{i,j} - \psi_{i,j+1}, U_t)}{k_j(k_{j-1}+k_j)} p^o_{i,j+1} = 0$$

Equations A1.60 and A1.61 are functionally equivalent to equations A1.51 and A1.52, so the same solution routines can be used in both steady state and time dependent routines. Stone's (1968) iterative pentadiagonal matrix solving routine was used in general for all three systems of equations in the time dependent routine. The SLOR method was also used for Poisson's equation in a few cases.

The principal quantity of interest from this routine is the total current at each time step. This is obtained by integrating the total current density through any surface which encloses one of the digits.

(A1.62) $$\oint_{\ell} \left(\vec{J}_n + \vec{J}_p + \frac{\partial(\epsilon \vec{E})}{\partial t} \right) \bullet d\ell$$

where $\frac{\partial(\epsilon \vec{E})}{\partial t}$ is the displacement current, and

ℓ is a closed path which encloses one digit.

The displacement current term in equation A1.62 makes the total current sensitive to small errors in the potential at any time step. These errors will tend to average out over the grid, so their effect on the total current can be minimized by calculating the total current for each vertical set of grid lines and using the average value.

The sensitivity of the current to different parameters varies through the device. This makes it difficult to choose general convergence criteria based on the dependent variables. Instead, convergence was based on the largest change in total current across the device per Newton iteration. When this change was less than a prescribed limit, then that time step was assumed to have converged and the program moved on to the next step.

APPENDIX 2: DEVICE FABRICATION

The materials used in device fabrication were semi – insulating GaAs, epi – layer GaAs, and silicon – on – sapphire wafers. These materials were described in detail in chapter 2. The general fabrication techniques are the same for all three materials and will be described below in step form with the details for each material specified.

(1) The wafers were scribed and broken into pieces approximately 1.5 cm on a side. These pieces were then used in the fabrication process.

(2) Each piece was organically cleaned by agitating in the following baths

–Deionized water (DIW)

–Methanol

–Acetone

–Trichloroethylene

–Acetone

–Methanol

–Rinse with flowing DIW.

(3) The SOS wafer were cleaned further using Hydrogen Peroxide based cleaning solutions (Kern 1970).

–10 min. in 5:1:1 : H_2O:NH_3OH:H_2O_2 ($75^0C - 85^0C$)

–Rinse in DIW

–10 min. in 5:1:1 : H_2O:HCl:H_2O_2 ($75^0C - 85^0C$)

–Rinse in DIW

(4) Surface oxide was removed from each of the three wafers using different methods.

–Epi – layer GaAs : the oxide etch was replaced by the etch to remove the top layer of n^+ GaAs.

1:100 : $Br:CH_3OH$ (4 min.)

This removed approximately 2 μm of material.

–Semi – insulating GaAs :

6:1 : Buffered HF (2 min.)

(buffer solution was 40% by weight NH_4F with water)

SOS :

6:1 : $H_2O:HF$ (2 min.)

(5) Rinse in DIW.

(6) Blow dry with clean N_2.

(7) Load into an e–beam evaporator (base pressure $\approx 10^{-6}$ torr).

(8) Evaporate a layer of Gold onto the surface. The thickness of gold was not routinely measured, but was always greater than 0.1 μm.

(9) Spin on positive photoresist.

(10) Soft bake at 90°C for 30 minutes.

(11) Expose to device mask.

(12) Develop.

(13) Etch the gold using

400 gm : 100 gm : 400 ml : $KI:I_2:H_2O$

diluted 1 part to 4 parts water.

(14) Remove photoresist in Acetone.

(15) Rinse in Methanol.

(16) Rinse in H_2O.

(17) Blow dry with clean N_2.

(18) Scribe and break into individual devices.

References

Alley, Gary D. (1970) "Interdigital Capacitors and Their Application to Lumped–Element Microwave Integrated Circuits," IEEE Trans. Microwave Theory Tech., vol. MTT–17, pp1028–1033.

Arfken, George. (1970), Mathematical Methods for Physicists. New York: Academic Press.

Bank, Randolph E., Rose, Donald J., and Fichtner, Wolfgang. (1983) "Numerical Methods for Semiconductor Device Simulation," IEEE Trans. Electron. Dev., vol. ED–30, pp 1031–1041.

Boudebous, F. Hobar, Pascal, D., and Laval, S. (1985) "A Comparison of Interdigital and Straight Structures for a Photoconductive Detector," IEEE Trans. Electron. Dev., vol. ED–32, pp836–837.

Bowers, John E., Burrus Jr., Charles A. (1987) "Ultrawide – Band Long – Wavelength p–i–n Photodetectors." J. Lightwave Technol. vol. LT–5, pp1339–1350.

Chen, Jun–Wei., Ko, Robert J., Brzezinski, Dennis W., Forbes, Leonard., Dell'oca, Conrad J. (1981) "Bulk Traps in Silicon – on – Sapphire by Conductance DLTS." IEEE Trans. Electron Dev. vol. ED–28, pp299–304.

Cullen, G.W. and Wang, C.C., (1978) Heteroepitaxial Semiconductors for Electronic Devices. New York: Springer–Verlag.

DeMari, A. (1968a) "An Accurate Numerical Steady – State One – Dimensional Solution of the P–N Junction," Solid -- State Electronics, vol. 11, pp 35–58.

DeMari, A. (1968b) "An Accurate One – Dimensional Solution of the p–n Junction Under Arbitrary Transient Conditions," Solid – State Electronics, vol. 11, pp 1021–1053.

Dumin, D.J. (1970) "Deep Levels within the Forbidden Gap of Silicon – on – Sapphire Films." Solid–State Electronics vol. 13, pp415–424.

Figueroa, L., Slayman, C.W. (1981), "A Novel Heterostructure Interdigital Photodetector (HIP) with Picosecond Optical Response." IEEE Electron Device Lett., vol. EDL–2, pp. 208–210.

Gammel, John Christopher, (1980) "Short Transit Time Photoconductive Detectors For High Speed Optical Communications. PhD. Thesis. Cornell University.

Garside, Brian K., Gouin, Francois L. (1982), "New devices and materials for ultrafast high speed photodetectors for the ultraviolet through to the infrared." Proc SPIE Int. Soc. Opt. Eng. vol. 355, pp27–36.

Gaudreault, M. and Stubbs, M.G. (1985) "Lumped–element components for GaAs monolithic microwave integrated circuits," Can. J Phys., vol. 63, pp736–739.
Grivitskas, V., Willander, M., Tellefsn, J.A. (1984) "Picosecond photoconductivity measurements of mobility and lifetime in silicon – on – sapphire films." J. Appl. Phys. vol. 55, pp3169–3172.

Gummel, H.K. (1964) "A Self – Consistent Iterative Scheme for One – Dimensional Steady State Transistor Calculations," IEEE Trans. Electron Devices; vol. ED–11, pp 455–465.

Gupta, K.C., Garg, Ramesh., Bahl,I.J. (1979), Microstrip Lines and Slotlines. Massachusetts: Artech House, Inc.

Henish, Heinz K., (1984) Semiconductor Contacts, An approach to ideas and models. Oxford: Clarendon Press.

Hsu, Sheng T. (1978) "Electron Mobility is SOS Films." IEEE Trans. Electron Dev. vol. ED–25, pp913–916.

Ito, Masanori. and Wada, Osamu. (1986) "Low Dark Current GaAs Metal – Semiconductor – Metal (MSM) Photodiodes Using WSi_x Contacts." IEEE J. Quantum Electronics, vol. QE–22, pp1073–1077.

Jackson, D.J., Persechini, D.L. (1986a) "Large Area, High – speed PIN Detectors in GaAs." Electron. Lett. vol. 22, pp. 202–3.

Jackson, D.J., Persechini, D.L. (1986b) "Monolithically Integrable High Speed Photodetectors." SPIE Vol. 716 High Frequency Optical Communications.

Kern, Werner. (1970) "Cleaning Solutions Based on Hydrogen Peroxide for use in Silicon Semiconductor Technology." RCA Review, June, pp187–206.

Klopfenstein, Ralph W. and Chung, P. Wu. (1975) "Computer Solution of One – Dimensional Poisson's Equation," IEEE Trans. Electron. Devices, vol. ED–22, pp 329–333.

Kurata, Mamoru, (1982) "Numerical Analysis for Semiconductor Devices,' Lexington, Massachusets: Lexington Press.

Laux, S.E., Lomax, R.J. (1987) "Numerical Investigation of Mesh Size Convergence Rate of the Finite Element Method in MESFET Simulation," Solid – State Electron., vol. 24, pp 485–493.

Levy, A.M. (1987) High Speed GaAs Surface Barrier Detectors.. M.Eng. Thesis, McMaster University.

Reiser, Martin. (1973) "A Two – Dimensional Numerical FET Model for DC, AC, and Large – Signal Analysis," IEEE Trans. Electron. Devices, vol. ED–20, pp 35–45

Roth, Walter., Schumacher, Hermann., Kluge, Jurgen., Geelen, H.J., Benecking, Heinz., (1985). "The DSI Diode – A Fast Large Area Optoelectronic Detector." IEEE Trans. Electron Devices. vol. ED–32, pp. 1034–1036.

Scharfetter, D.L., Gummel, H.K. (1969) "Large – Signal Analysis of a Silicon Read Diode Oscillator," IEEE Trans. Electron. Devices. vol. ED–16, pp 64–76.

Schumacher, H., Leblanc, H.P., Soole, J., Bhat, R. (1988) "An Investigation of the Optoelectronic Response of GaAs/InGaAs MSM Photodetectors." IEEE Electron Device Lett., vol. 9, pp. 607–609.

Scott, Ronald E. (1965), Elements of Linear Circuits. Reading, Massachusetts: Addison – Wesley Publishing Company, Inc.

Selberherr, Siegfried. (1984) Analysis and Simulation of Semiconductor Devices, New York: Springer – Verlag/Wien.

Seymour, R.J. and Garside, B.K. (1984) "Ultrafast silicon photodiodes for ultraviolet applications." Can. J. Phys., vol. 63, pp707–711.

Seymour, R.J., Garside, B.K., and Park, R.E. (1986) "Ultrafast surface barrier photodetectors." Proc. SPIE Int. Soc. Opt. Eng., vol. 663, pp30–36.

Seymour, R.J., and Garside, B.K. (1988) "Intrinsic and extrinsic factors limiting the time response of interdigital photodetectors." Can. J. Phys., vol. 67, pp440–443.

Shampine, Lawrence F., Allen Jr., Richard C. (1973), Numerical Computing: an introduction Toronto: W.B. Saunders Company.

She, X.Y. and Chow, Y.L. (1986) "Interdigital microstrip capacitor as a four–port network," IEE Proceedings, vol. 133, Pt H, pp191–197.

Slayman, C.W., Figueroa, L. (1981) "Frequency and Pulse Response of a Novel High Speed Interdigital Surface Photoconductor (IDPC)." IEEE Electron Device Lett., vol. EDL-2, pp. 112–114.

Smith, John I. (1971) "The Even– and Odd–Mode Capacitance Parameters for Coupled Lines in Suspended Substrate," IEEE Trans. Microwave Theory Tech., vol. MTT–19, pp424–431.

Stone, Herbert L. (1968) "Iterative Solution of Implicit Approximations of Multidimensional Partial Differential Equations," SIAM J. Numerical, vol. 5, pp 5300–558.

Sugeta, Takayuki., Urisu, Tsuneo. and Sakota, Seizo. (1980) "Metal – Semiconductor – Metal Photodetector for High–Speed Optoelectronic Circuits." Jap. J. Appl. Phys., vol. 19, sup 19–1, pp. 459–464.

Sze, S.M. (1981) Physics of Semiconductors Devices. Toronto: John Wiley & Sons.

Sze, S.M., Coleman, D.J. and Loya, A. (1971) "Current Transport in Metal – Semiconductor – Metal (MSM) Structures." Solid–State Electronics vol. 14, pp1209–1218.

Van Zeqhbroeck, Bart J., Patrick, William., Halbout, Jean–Marc., Vetliger, Peter. (1988) "105–GHz Bandwidth Metal–Semiconductor–Metal Photodiode." IEEE Electron Device Lett., vol. 9, pp. 527–529.

Wada, Osamu., Sakurai, T., Nakagami, Takakyo. (1986a) "Recent Progress in Optoelectronic Integrated Circuits (OEICs)." IEEE J. Quantum Electron., vol. QE–22, pp. 805–821.

Wada, O., Hamaguchi, H., Makiuchi, M., Kumai, T., Ito, M., Nakai, K.,Horimatsu, T., Sakurai, T. (1986) "Monolithic Four–Channel Photodiode/Amplifier Receiver Array Integrated on a GaAs Substrate." J. Lightwave Technol. vol. LT–4, pp1694–1702.

Wasserstrom, E., and McKenna, J. (1970) "The Potential Due to a Charged Metallic Strip on a Semiconductor Surface," Bell System Tech. J., May – June, pp 853–877.

Wojtczuk, S.J.,Ballantyne, J.M., Wanuga, S. and Chen, Y.K. (1987) "Comparative Study of Easily Integrable Photodetectors." J. Lightwave Technol., vol. LT–5, pp. 1365–1370.

Yamashita, Eikichi (1968) "Variational Method for the Analysis of Microstrip–Like Transmission Lines," IEEE Trans. Microwave Theory Tech., vol. MTT–16, pp529–535.

Yoshii, Akira, Kitazawa, Hitoshi, Tomizawa, Masaki, Horiguchi, Shoji, and Sudo, Tsuneta. (1982) "A Three–Dimensional Analysis of Semiconductor Devices," IEEE Trans. Electron. Devices, vol. ED–29, pp 184–189.