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**AN INTEGRATED HIGH SPEED FLYWHEEL ENERGY
STORAGE SYSTEM FOR PEAK POWER
TRANSFER IN ELECTRIC VEHICLES**

By

UWE SCHAIBLE, B.ENG.MGT., M.ENG.

A Thesis

Submitted to the School of Graduate Studies

in Partial Fulfilment of the Requirements

for the Degree

Doctor of Philosophy

McMaster University

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**PEAK POWER TRANSFER IN
ELECTRIC VEHICLES**

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ABSTRACT

An investigation is conducted into the practical electric vehicle implementation of a high speed flywheel energy storage system that can supply and accept peak acceleration and braking power. Electric vehicle battery life cycle can be extended considerably by supplying peak energy requirements from a secondary source. Simulations are performed to determine the peak power and energy requirements over the SAE recommended electric vehicle test procedure. A scaled prototype secondary energy storage unit is built using flywheel energy storage. Tests are conducted to determine the energy transfer capabilities of a flywheel coupled high speed permanent magnet synchronous machine through the proposed system's energy storage tank. Results are presented that indicate the necessity of the energy storage tank. A system evaluation is also included which indicates its near-term practicality when compared to conventional regenerative control applications.

Construction techniques are discussed for the development of high speed drive circuits used in electrically noisy environments. Shielding and electromagnetic interference reduction methods are proposed for application to an actual high efficiency sinusoidal phase current, microprocessor interfaced, vector controlled, high speed permanent magnet synchronous machine drive. A discussion on the theory and construction of such a drive is provided to demonstrate the implementation of a laboratory prototype high speed flywheel energy storage system.

An experimental investigation is conducted using the developed high speed drive

to determine permanent magnet synchronous machine parameter behaviour in the high speed flux weakening operating range. Special computer assisted measuring techniques are used to determine the realtime operating characteristics for two commercially available machines. The repeatable experimental results show a significant variation in the machine parameters as a function of the speed and torque angle. Implications of the newly identified dynamic parameters are discussed regarding their application to, and effect on, high performance permanent magnet synchronous machine torque control.

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NOMENCLATURE

A	amperes
Arms	root mean square amperes
$a_{\Delta t}$	interval acceleration (m/s^2)
A_{enc}	enclosed loop area (m^2)
AGV	Automatically Guided Vehicle
A_v	effective frontal area of the vehicle (m^2)
A/D	Analog to Digital conversion
B	magnetic flux density (webers/ m^2)
C	capacitance (Farads)
C_D	air drag coefficient (dimensionless)
C_R	coefficient of rolling resistance (dimensionless)
CCVSI	Current Controlled Voltage Source Inverter
CPU	Central Processing Unit
CSI	Current Source Inverter
CT	Current Transformer
δ	angle between phase current fundamental and the back-EMF fundamental
d	distance (m)
dc	direct current
DAS	Data Acquisition System
DOD	Depth of Discharge
D/A	Digital to Analog conversion
E	energy (J)
E_{AUX}	auxiliary loss energy (J)
E_{DRIVE}	drive loss energy (J)
E_{NRE}	net required energy (J)
E_o	back-emf per pole (V)
E_{ROAD}	road loss energy (J)
E_{TRANS}	transient energy (J)
EMF,emf	Electromotive Force
EMI	Electromagnetic Interference
EPA	Environmental Protection Agencies
ESR	Equivalent Series Resistance
EV	Electric Vehicle
ϕ	magnetic flux (Webers)
F	Farad
F_A	air drag force (N)
F_R	rolling resistance force (N)
FESS	Flywheel Energy Storage System

g	gravitational acceleration constant (m/s^2)
h	hour
HTS	High Temperature Superconductor
i_a, i_b, i_c	phase a, b, and c current
i_d	direct axis current (A)
i_f	field current (A)
i_q	quadrature axis current (A)
I	current (A)
I_o	simplified equivalent circuit PMSM phase current (A)
$I\phi$	phase current magnitude (A)
IC	Integrated Circuit
ICE	Internal Combustion Engine
IGBT	Insulated Gate Bipolar Transistor
IPMSM	Interior Permanent Magnet Synchronous Machine
I/O	Input and Output
ISR	Interrupt Service Routine
k_o	PMSM back-EMF constant (V/krpm)
kg	kilogram
km	kilometer
krpm	thousands of rotations per minute
kV	kilovolt
kW	kilowatt
kWh	kilowatt hour
λ	flux linkage
L	inductance (Henries)
L_{aa0}	space fundamental air gap flux self-inductance (Henries)
L_{af}	stator to rotor mutual inductance magnitude (Henries)
L_{al}	stator leakage flux self-inductance (Henries)
L_{ff}	rotor circuit self inductance (Henries)
L_{ψ^2}	amplitude of the cosinusoidally varying stator self-inductance (Henries)
L_o	zero sequence inductance component (Henries)
m	meter
μs	microseconds
ms	milliseconds
M	mutual inductance (Henries)
M_{EV}	total mass of the vehicle (kg)
MMF	Magneto Motive Force (ampere-turns)
MTCE	Maximum Torque Conversion Efficiency
MUT	Machine Under Test
n_f	flywheel speed (rpm)

n_{Fk}	flywheel speed (krpm)
N	Newton
η_B	electric vehicle battery efficiency
η_{CC}	control chopper
η_{ED}	electric drive efficiency
η_F	flywheel energy storage system efficiency
η_G	gearbox efficiency
η_M	motor efficiency
Ω	ohms
P	power (watts)
PC	Personal Computer
PI	Proportional Integral
PIA	Peripheral Interface Adapter
PID	Proportional Integral Derivative
p.u.	per unit
$P_{m\phi}$	mechanical phase power
$P_{c\phi}$	electrical phase power
PMSM	Permanent Magnet Synchronous Machine
Ψ_{mag}	permanent magnet flux linkage ($L_{\sigma i}$)
PWM	Pulse Width Modulation
ρ	air density (kg/m^3)
R	resistance (ohms)
R_c	core loss resistance (Ω)
RF	radio frequency
R_s	stator resistance (Ω)
rads	radians
rpm	rotations per minute
s	frequency domain operator ($s=j\omega$)
s	seconds
S	stator variable to be transformed to the rotor reference frame
SAE	Society of Automotive Engineers
SESU	Secondary Energy Storage Unit
t	time (s)
T	torque (N·m)
$T_{c\phi}$	instantaneous developed phase torque (N·m)
θ	reference current compensation angle (deg)
v	speed (m/s)
V	voltage
V_a, V_b, V_c	phase a, b, and c voltage (V)
V_d	direct axis voltage (V)

V_q	quadrature axis voltage (V)
VA	Volt-Ampere
Vrms	root mean square volts
Vdc	dc voltage (V)
V_ϕ	phase voltage (V)
V_f	field circuit voltage (V)
V_{TANK}	energy storage tank voltage (V)
VSI	Voltage Source Inverter
X_d	direct axis reactance (Ω)
X_q	quadrature axis reactance (Ω)
X_s	stator reactance (Ω)
ω	frequency (rads/sec)
ω_r	mechanical speed (rads/s)

CHAPTER 1

INTRODUCTION

1.1 BACKGROUND INFORMATION

Environmental concerns and the resulting political pressures have helped generate much interest for the development of practical and highly efficient zero pollution emission Electric Vehicles (EVs). Though many advances have occurred, one of the major obstacles, yet to be overcome, is the lack of a suitable EV power supply. Industry experts have concluded that practical EVs must have energy storage devices capable of a minimum power of 400 W/kg, energy of 200 Wh/kg, a life cycle of 2500 at a cost of around \$75 /kW, and a 40% to 80% recharge capability in less than 30 minutes [1]. To date, such requirements have not been met.

The lack of an adequate, yet affordable energy storage device, has prompted much research into the reduction of EV energy consumption. Many schemes have been proposed, some of which include the use of regenerative braking and load levelling. Regenerative braking is easily implemented on vehicles that receive energy from external power sources. For vehicles not connected to an external power supply, the braking energy must be stored 'on board'. Advanced lead-acid batteries provide higher performance at lower cost. Such batteries have been designed to achieve a specific energy density of 42 Wh/kg and a power density of up to 500 W/kg [2][3]. With such advances, using electrochemical batteries to

store energy during regenerative braking still leads to a greatly oversized vehicle battery pack. Peak power stresses during vehicle acceleration and braking also shorten the battery life cycle. A reduced life cycle translates into high maintenance costs since the batteries have to be replaced regularly throughout the lifetime of the vehicle. Such high maintenance costs, in addition to the high vehicle cost, make it prohibitive for a consumer to own an electric vehicle.

Researchers focus on improving the batteries or reducing the peak power requirements to overcome the problem of peak power stresses on electric vehicle batteries. Peak power requirements can be decreased by designing a lighter vehicle, reducing the vehicle rolling resistance, reducing the aerodynamic drag, and limiting the use of accessories. Some researchers, however, have investigated the concept of using a Secondary Energy Storage Unit (SESU) within the electric vehicle to both store and supply peak power during periods of regenerative braking or rapid acceleration. This process is referred to as load levelling and is the focus of this research.

1.2 LOAD LEVELLING WITH FLYWHEELS

There are many ways to provide secondary energy storage for use in a load levelling process. The SESU can consist of electric, kinetic, elastic, hydraulic, or pneumatic energy storage. This investigation uses a kinetic energy storage device in the form of a high speed flywheel directly coupled to an electric machine. Chrysler corporation has recently investigated the use of a high speed flywheel in its AFS20 non-running concept car [4]. No working model has been developed to date.

The mechanical suitability for the flywheel has already been thoroughly investigated [5][6]. Extractable flywheel energy is expressed as:

$$\Delta E = \frac{1}{2} \cdot J \cdot (\omega_{\max}^2 - \omega_{\min}^2) \quad (1.1)$$

where:

- E = extractable flywheel energy (J)
- J = flywheel moment of inertia (kg·m²)
- max = maximum flywheel operating speed (rads/sec)
- min = minimum flywheel operating speed (rads/sec)

The formulation in (1.1) illustrates the advantage of high speed flywheel operation. Since extractable energy is proportional to the square of the operating speed, low mass, high speed units can be designed to provide high energy densities.

Advanced high speed flywheels can provide power bursts in the 5 to 10 kW/kg range with negligible effect on their life cycle. Hence, they are immune to the peak power stresses that are otherwise destructive to the electrochemical batteries. Current flywheel designs use high strength graphite fibres that can operate at 80 000 rpm over temperature ranges from -40 to 100 °C [6]. Such flywheels can provide an energy of 1 kWh, more than twice the capabilities of advanced lead acid batteries, while weighing less than 11 kg.

Figure 1.1 provides the basic block diagram of an electric vehicle flywheel energy storage system used in a load levelling strategy. A flywheel and electric machine are connected through a dc link to the drive system and battery pack. Peak acceleration power used by the drive system is supplied by the flywheel and electric machine through the dc link. The post acceleration power is used to maintain the momentum of the vehicle and is supplied by the vehicle's battery pack once acceleration has been completed. If necessary, the battery pack also supplies post acceleration power to the flywheel and the electric machine

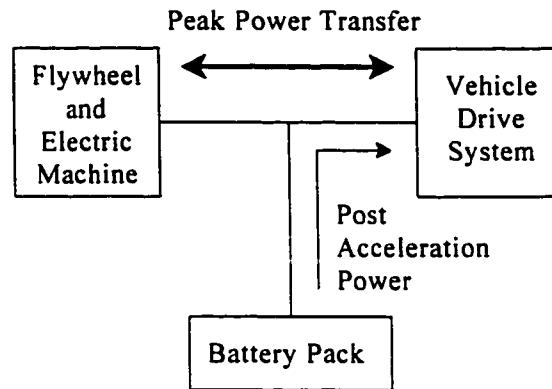


Figure 1.1. Load levelling strategy

to ensure that a minimum stored energy level is maintained. Peak regenerative braking power from the drive system is transferred through the dc link to the flywheel/electric machine combination. Use of this strategy can reduce the peak power stresses on the batteries.

The block diagram in Figure 1.1 uses an electric machine to convert energy between its electric and kinetic states. Such a machine must be able to operate efficiently at the high speeds required to store large amounts of energy in a flywheel. The recent development of permanent magnet type bearingless motors for potential use in super high speed applications, provides an excellent candidate for electromechanical energy conversion [7][8][9]. Both the electric machine and the high speed flywheel have to be contained in a cooled vacuum housing to reduce the windage losses associated with the high speed operation of the electric machine and flywheel. Recent developments in high temperature superconductors have provided a possible solution to the energy losses in flywheel bearings. The equivalent coefficient of friction for a High Temperature Superconductor (HTS) bearing has been reported to be about 2×10^{-6} , or approximately one hundred times better than the best alternative bearing [10]. This translates into achievable idling losses in the order of 0.1

percent per hour for vacuum housed, HTS bearing equipped flywheels.

1.3 SUMMARY OF PREVIOUS WORK

Previous work conducted by this author has provided an implementation strategy for a practical Flywheel Energy Storage System (FESS) that can be used for load levelling in an electrical vehicle [11]. The implementation strategy calls for a commercially available high speed Permanent Magnet Synchronous Machine (PMSM) to be directly coupled to a flywheel, torque controlled through the use of a vector control algorithm, and interfaced to the EV dc bus. An expanded block diagram of the proposed FESS is shown in Figure 1.2. The 3-phase PMSM and its associated power converter is connected to the dc bus through an energy storage tank. Voltage and power flow on the dc bus is maintained by a bidirectional chopper, and the drive system and battery pack are connected to the FESS

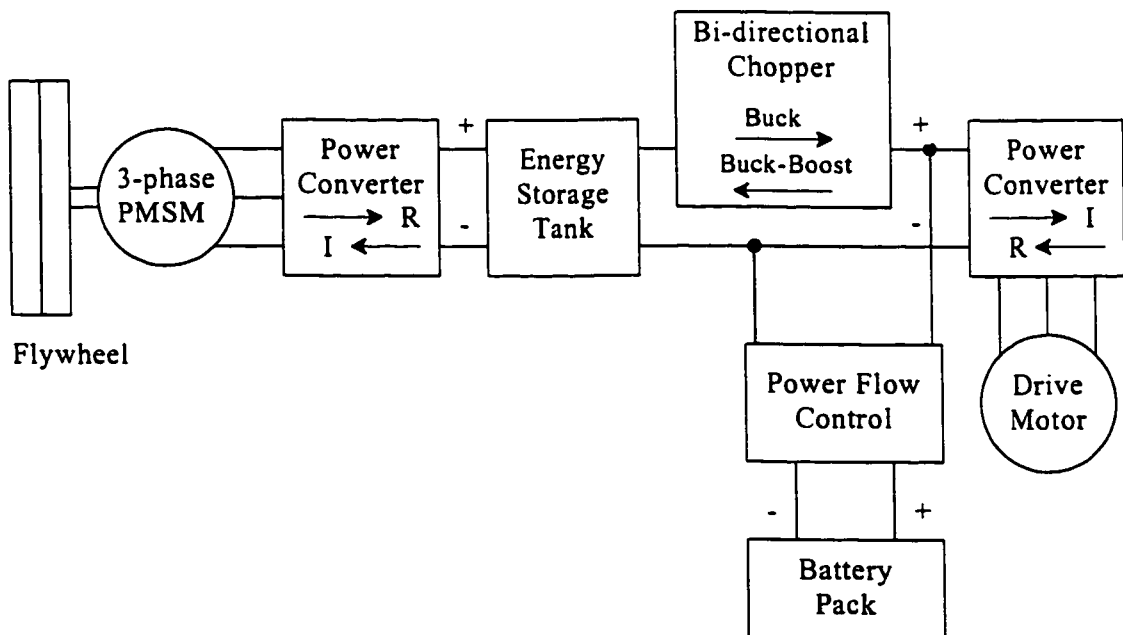


Figure 1.2. Proposed electric vehicle drive system with flywheel energy storage

through the dc link. The purpose of the bidirectional chopper is to regulate the dc link. A regulated dc link allows the EV battery pack to be electrically connected with the flywheel energy storage system. Link regulation prevents peak power stressing of the batteries and also allows for the possibility of paralleling flywheel energy storage systems, which may be necessary once system optimization has been considered.

Vehicle acceleration requires peak power from the drive motor. The voltage on the energy storage tank will fall as power is drawn from the FESS, until the PMSM can respond and replenish the lost energy. The bidirectional chopper is operated in its forward direction which corresponds to the buck regulation mode. Storage tank voltage is required to be higher than the dc link voltage for buck regulation. This necessitates the requirement to have a minimum amount of energy stored in the tank. It is essential that energy drawn out of the tank is replenished as quickly as possible by the PMSM, to keep the energy storage tank as small as possible, and still achieve the minimum voltage requirement.

The dc link voltage is allowed to float during vehicle braking. The high voltage rise associated with regenerative braking must be limited so that the energy storage tank ratings are not exceeded. Bidirectional chopper operation is required in the buck-boost regulation mode since there are no assurances of what the braking voltage will be relative to the voltage on the energy storage tank. Braking energy from the dc link is forced into the energy storage tank during the buck-boost mode. At the same time, electric energy is drawn out of the tank by the PMSM and converted into the kinetic energy of the flywheel. The tank voltage rises and falls depending on the response time of the PMSM and the rate at which energy flows into and out of the tank during the braking operation. Tank voltage will

fall to the level associated with its undisturbed state once braking has been completed. The proposed scheme allows energy to be transferred to the FESS in a controlled manner. Hence, controlled braking of the electric vehicle can be accomplished.

A scaled laboratory prototype was constructed to demonstrate the principle of the proposed implementation strategy. A PMSM was purchased and interfaced with a specially constructed Insulated Gate Bipolar Transistor (IGBT) Voltage Source Inverter (VSI) drive. Current control through the VSI was investigated and an error-triangle modulated Current Controlled Voltage Source Inverter (CCVSI) was partially constructed. Plans and algorithms were developed for the implementation of torque control of the FESS through a commercially available 16 bit, 20 MHz microcontroller. Initial testing was conducted to simulate the acceleration mode of an EV operation. Tests were conducted to determine how quickly the PMSM can compensate the energy requirement of a 0.3 p.u. step load demand drawn from the energy storage tank. Test results indicated the necessity of the energy storage tank, and also showed that the generation capabilities of the PMSM can replenish the energy storage tank more rapidly than initially believed.

1.4 RESEARCH OUTLINE

1.4.1 Measurable Objectives

The research conducted in this thesis is a continuation of the previous work by this author [11]. The objectives of this thesis are to complete the construction of the test bench model for the proposed FESS and to conduct an investigation into the EV braking mode energy transfer capabilities in the same manner as was done during the EV acceleration

mode tests in [11, pp. 71-74]. It is desired by this author to conduct further acceleration mode tests to enhance the findings in [11] and apply them to a component sizing analysis on a full scale FESS equipped EV.

The additional objectives of this thesis involve the PMSM and power electronic drive used to convert SESU energy between its electrical and mechanical state. It is desired by this author to develop a sinusoidal current, high efficiency, Current Controlled Voltage Source Inverter (CCVSI), microprocessor supervised, power electronic drive that is capable of operating the PMSM at speeds of up to 8000 rpm. It is also desired to interface this high speed drive to a PC on which a real-time high performance torque control algorithm is implemented using the dynamic parameters of the PMSM.

1.4.3 Technical Problems

Several technical problems must be investigated before developing an integrated high speed sinusoidal current drive system. Electrical noise problems are a common occurrence in such a drive system and will cause unstable drive operation. An understanding of electrical noise and interference is essential before an attempt is made at applying noise reduction techniques. Real-time high performance torque control of the high speed drive system requires rapid data processing and transfer capabilities. A novel approach must be developed to implement such a drive system. High performance torque control of PMSMs requires the knowledge of the PMSM parameters. An accurate and repeatable experimental method must be developed to determine these parameters over the wide torque and speed operating range of the proposed drive system. The work conducted in this thesis will ad-

dress and solve these technical problems.

1.4.3 Organization of Thesis

The following research begins with an investigation into the energy requirements and peak power transfer capabilities of a simulated electric vehicle. Sizing requirements are determined for the proposed flywheel energy storage components, used to enhance EV operation through load levelling. A refined investigation of the FESS energy transfer characteristics is conducted in Chapter 3 using a modified version of the previous laboratory test bench. Electric vehicle acceleration and deceleration peak power transfer capabilities are determined with a test bench model of the proposed FESS.

The remainder of the thesis directs focus on the design and construction of a working prototype, high speed, microprocessor controlled, three phase, sinusoidal CCVSI drive, capable of high performance flux weakening torque control of PMSMs used in FESS applications. Chapter 4 outlines the various electric and magnetic noise reduction and shielding techniques necessary for the construction of such a drive. Chapter 5 deals with the construction and implementation of the actual drive, and investigates the extra resources and special techniques necessary to achieve 8000 rpm machine operation.

Machine torque development, and its control in the flux-weakening region are discussed in Chapter 6. Flux-weakening torque control requires specific knowledge of machine parameters that are unavailable from the manufacturer. Chapter 7 develops the theory and application of a novel parameter identification method using the newly developed synchronous machine drive. Parameters of two different commercially available PMSMs are

determined and compared with the manufacturer supplied specifications. The research for this thesis concludes in Chapter 8 with the implementation of the required control parameters in the software torque control algorithm component of the working prototype drive.

CHAPTER 2

ELECTRIC VEHICLE SIMULATION INVESTIGATION

2.1 VEHICLE SPECIFICATIONS AND ENERGY LOSSES

General acceptance and widespread use of electric vehicles depends on their ability to be able to compete directly with Internal Combustion Engine (ICE) powered vehicles in terms of performance, comfort, and price. A previous study has shown that a 2200 kg vehicle requires approximately 78 kWh of stored energy and a peak power 94 kW to attain a maximum driving range of 200 to 250 km with an acceleration capability of 0-96 km/h in 10 seconds [12]. The reported findings were based on a mid-sized vehicle, offering the same level of room, comforts, and accessories as current ICE powered vehicles.

The purpose of this investigation is to use a standard driving cycle to determine the energy and peak power requirements of an electric vehicle capable of offering performance and comforts comparable to commonly used ICE powered vehicles. The results of this investigation will be used to extend the previous work in [12] and to provide SESU sizing for the FESS equipped electric vehicle drive proposed in [11].

Energy consumption and required drive power depend directly on the vehicle's specifications, drive and conversion efficiencies, and environmental losses. The following two sections detail the assumptions made for this EV simulation.

2.1.1 Electric Vehicle General Specifications

The electric vehicle simulation is conducted according to the vehicle specifications listed in Table 2.1. The acceleration capabilities are chosen based on a comparison with the capabilities of popular mid-sized ICE powered vehicles, namely the Ford Contour, Dodge Avenger, and Honda Accord, whose 0-96 km/h acceleration performance was found to be just within the 10 second range [13]. Non-emergency deceleration capabilities refer to the ability to perform regenerative braking without the use of friction braking from conventional vehicle brakes. The simulated electric vehicle is specified to be able to comfortably decelerate using regenerative braking from 96 km/h to standstill in 7 seconds. Vehicle, passenger, and luggage mass are chosen to be comparable to the previously mentioned class of vehicles, seated with five passengers and storing the type of luggage that would normally be taken on a weekend excursion.

The combined city/highway maximum driving range between recharges is set to 200 km. A 200 km setting represents a compromise between the 400 to 500 km range normally associated with ICE powered vehicles and the 100 km city, 145 km highway range specified by the GE Impact, the only currently available North American passenger EV [13].

Table 2.1
Summary of Simulated EV General Specifications

Vehicle Acceleration (0-96 km/h)	10 sec.
Vehicle Non-Emergency braking (96-0 km/h)	7 sec.
Vehicle Mass	1600 kg
Passenger Mass	400 kg
Luggage and Accessories Mass	200 kg
Range at 85% Depth of Discharge (DOD)	200 km

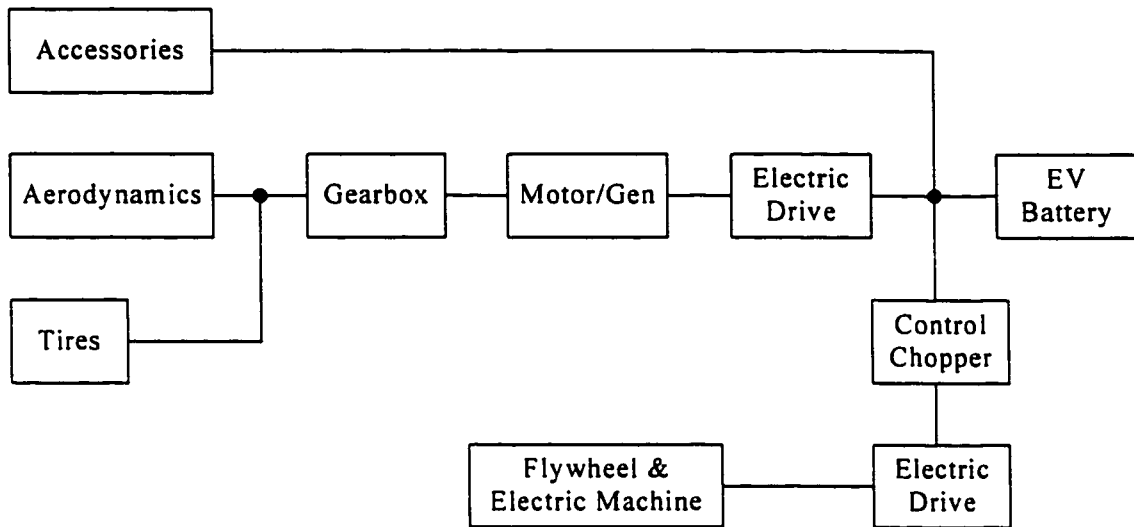


Figure 2.1 Loss Components of the Proposed FESS Equipped EV

2.1.2 Operating Losses of the Proposed FESS Equipped EV

Electric vehicle simulation and performance analysis over a standard driving cycle requires specific knowledge of the various energy losses during operation. Figure 2.1 shows a block diagram of the various loss components associated with the proposed FESS equipped EV. Loss component estimation and analysis can be more easily performed through loss classification into the categories of Drive Losses, Road Losses, and Auxiliary Losses.

Drive Losses

Drive losses consist of those losses associated with the transfer of either EV battery or FESS energy to the vehicle's tires. A breakdown of the different drive component efficiencies is provided in Table 2.1. These efficiencies were determined from assumptions in the previous work published in [12] and through direct discussions with the authors. Analysis of these drive efficiencies indicates that approximately 18% of the energy stored in the EV batteries will be lost upon transfer to the EV tires. Further analysis shows that

Table 2.2
Drive Component Efficiencies

Motors (η_M)	93%
Gearboxes (η_G)	99%
Electric Drives (η_{ED})	97%
Control Chopper (η_{CC})	98%
EV Batteries (η_B)	92%
FESS (η_F)	92%

vehicles equipped for load levelling through the use of a FESS will lose approximately 39% of the net recoverable vehicle energy over a full charge/discharge cycle. Though the load levelling losses seem high and disappointing at first glance, they are put into perspective when compared with the 100% recoverable energy losses associated with today's ICE powered vehicles.

Road Losses

Drive energy transmission to the EV tires incurs energy losses that are commonly referred to as road losses. Road losses consist mainly of tire rolling resistance losses and vehicle aerodynamic losses. The simulated electric vehicle is assumed to operate on a paved road with no grade. All tires are assumed to be at equilibrium temperature. The previous assumptions allow for the formulation of the vehicle's rolling resistance according to (2.1) [14].

$$F_R = C_R \cdot M_{EV} \cdot g \quad (2.1)$$

where:

$$\begin{aligned} F_R &= \text{rolling resistance (N)} \\ C_R &= \text{coefficient of rolling resistance (dimensionless)} \\ M_{EV} &= \text{total mass of vehicle (kg)} \\ g &= \text{gravitational acceleration constant (9.81 m/s}^2\text{)} \end{aligned}$$

Rolling resistance coefficients are highly dependent on tire construction and material. Tire manufacturers continuously try to reduce tire rolling resistance, while maintaining road handling performance. Extremely low rolling resistance tires use Neoprene Polychloroprene rubber as well as reduced deformation bead, sidewall, shoulder and tread areas [15][16]. Tires for electric vehicles can be readily manufactured with rolling resistance coefficients as low as 0.0074. This compares with an average rolling resistance coefficient of 0.0127 for tires on most mid-size passenger vehicles [16]. Unfortunately, extremely low rolling resistance tires do not offer the road handling capabilities sought by most safety conscious consumers. The tires chosen for this simulated EV were Michelin P185/65R-14 XGT4s. They offer a low rolling resistance coefficient of 0.0108 without compromising safety through traction loss.

Aerodynamic losses can be expressed as in (2.2) [14].

$$F_A = 0.5 \cdot \rho \cdot C_D \cdot A \cdot v^2 \quad (2.2)$$

where:

$$\begin{aligned} F_A &= \text{air drag (N)} \\ \rho &= \text{air density (kg/m}^3\text{)} \\ C_D &= \text{air drag coefficient (dimensionless)} \\ A_v &= \text{effective frontal area of the vehicle (m}^2\text{)} \\ v &= \text{vehicle velocity (m/s)} \end{aligned}$$

The air density is assumed to be 1.2 kg/m³, based on the air density found in a low altitude, room temperature environment. The effective frontal area of the car was chosen as 1.9 m², typical of the previously mentioned class of vehicle used for this investigation. An air drag coefficient of 0.34 was chosen, based on the type of aerodynamic design found on today's most common ICE passenger vehicles. In contrast, the GE Impact is specified to have an

Table 2.3
EV Road Loss Parameters

Coefficient of Rolling Resistance	0.0108
Air Density	1.2 kg/m ³
Air Drag Coefficient	0.34
Effective Frontal Area	1.9 m ²

Table 2.4
EV Auxiliary Loss Components

Air-conditioning	3.0 kW
Windshield wipers	0.1 kW
Lights	1.0 kW
Radio/Hi-fi equipment	0.2 kW
Power Windows, seats and door locks	0.2 kW
Motor cooling pump and fan	1.5 kW

air drag coefficient of 0.19. A summary of the assumed parameters used to determine the road losses for the simulation of the proposed FESS equipped EV is shown in Table 2.3.

Auxiliary Losses

Losses associated with vehicle accessories are referred to in this investigation as auxiliary losses. Vehicle accessories are assumed to be 2/3 utilized and consist of the same accessories that consumers are accustomed to in conventional ICE powered vehicles. The total auxiliary losses for this simulation are expressed as $P_A = 6.0 \text{ kW} \times 2/3 = 4.0 \text{ kW}$. Table 2.4 lists a breakdown of the individual power consumption for the simulated EV auxiliary loss components.

2.2 DRIVING SCHEDULES FOR EV TESTING

Several choices exist for the selection of a standard driving cycle over which the energy and peak power requirements of an electric vehicle can be determined. The Environmental Protection Agency (EPA) uses separate highway and urban cycles when conducting ICE vehicle emission compliance tests. The same EPA driving cycles have also been adopted for vehicle emissions testing by Transport Canada and are shown in Figures 2.2 and 2.3¹. Much criticism has been raised on the complexity of these driving cycles, resulting in limited use of these cycles for EV testing.

A more simplistic driving cycle has been proposed by European EV researchers [17]. It uses four consecutive 200 second start/stop cycles, representing a city driving cycle, followed by a 400 second higher speed 'highway' cycle. The speed profile of the EUROPE cycle is shown in Figure 2.4.

The most common, and now standard EV driving cycle test procedure is the Society of Automotive Engineers (SAE) Recommended Practice SAE J227a. It consists of four different test cycles which allow the EV to be tested under conditions that best match its use. The test can be used to determine energy consumption and maximum travel range of an EV when operated on a level surface over a repeatable driving cycle. The test is intended to be a standard procedure which will allow the performance of electric vehicles to be compared against one another when operated over a fixed driving pattern.

A summary of the different driving schedules within SAE J227a is provided in

¹ Based on information provided by Denis Boucher, Senior Engineer, Energy Research, Road Safety and Motor Vehicle Regulation, Transport Canada

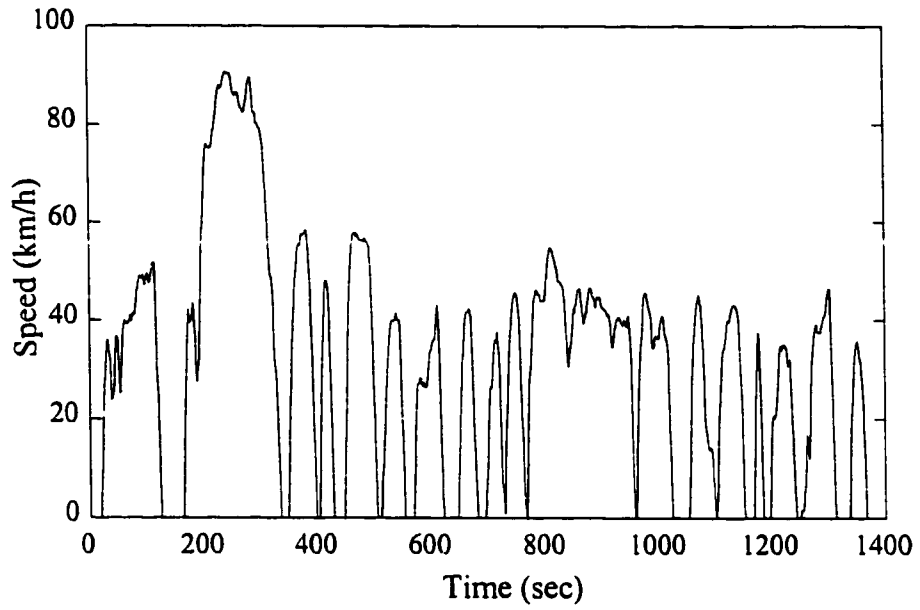


Figure 2.2 EPA urban cycle speed profile

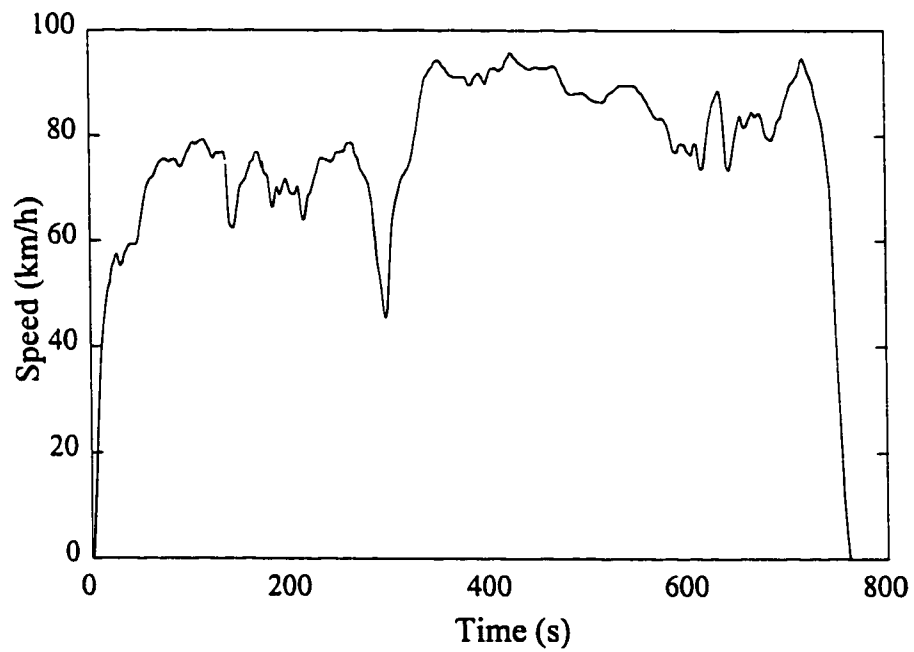


Figure 2.3 EPA highway cycle speed profile

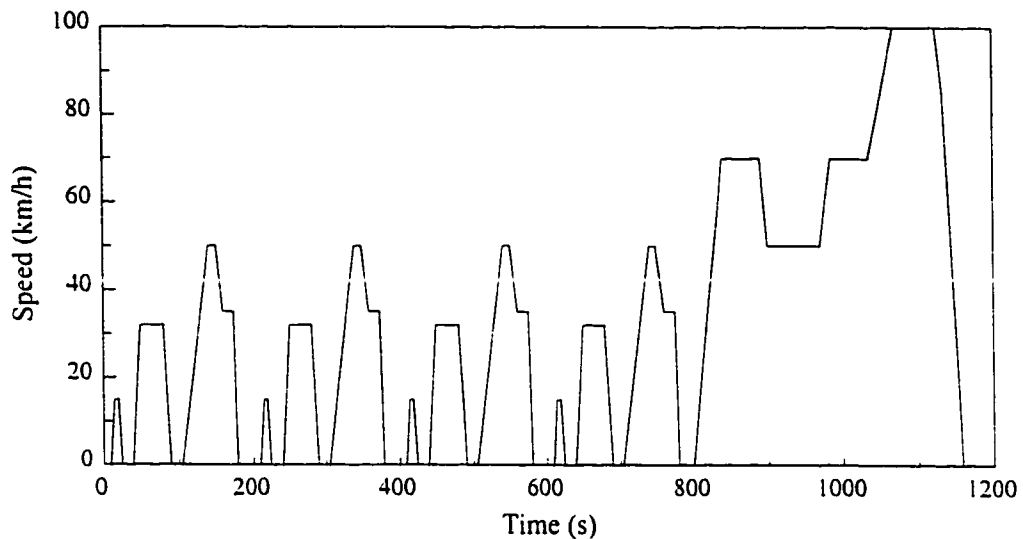


Figure 2.4 EUROPE driving cycle speed profile

Table 2.5 (SAE, 1992). Figure 2.5 offers a visual speed profile of the various schedules. Schedule A is used for the testing of EVs such as milk trucks and postal delivery vans, whose operation requires high frequency starts and stops. Schedule B is used for the testing of medium frequency stop and go operation vehicles such as shuttle buses and bakery trucks. Variable route, medium frequency stop and go operation vehicles, such as parcel post delivery vans, can be tested according to Schedule C. Commuter cars, whose suburban operation is characterized with a variable route stop and go operation, can be tested according to Schedule D.

Acceleration capabilities of most ICE vehicles are specified according to their 0-60 mph (0-96 km/h) times. The general public is familiar and comfortable with such specifications, and for this reason, the author feels that EVs should also be tested according to their 0-96 km/h acceleration capabilities. Braking of ICE powered vehicles is usually measured in terms of the distance travelled on a level grade from the point at which brakes are applied,

Table 2.5
SAE J227a EV Test Schedule

Schedule	A	B	C	D
Vehicle Cruise Speed (km/h)	16 ± 1.5	32 ± 1.5	48 ± 1.5	72 ± 1.5
Acceleration Time (s)	4 ± 1	19 ± 1	18 ± 2	28 ± 2
Cruise Time (s)	0	19 ± 1	20 ± 1	50 ± 2
Coast Time (s)	2 ± 1	4 ± 1	8 ± 1	10 ± 1
Braking Time to 0 km/h (s)	3 ± 1	5 ± 1	9 ± 1	9 ± 1
Idle Time at 0 km/h (s)	30 ± 2	25 ± 2	25 ± 2	25 ± 2
Total Cycle Time (s)	39 ± 2	72 ± 2	80 ± 2	122 ± 2

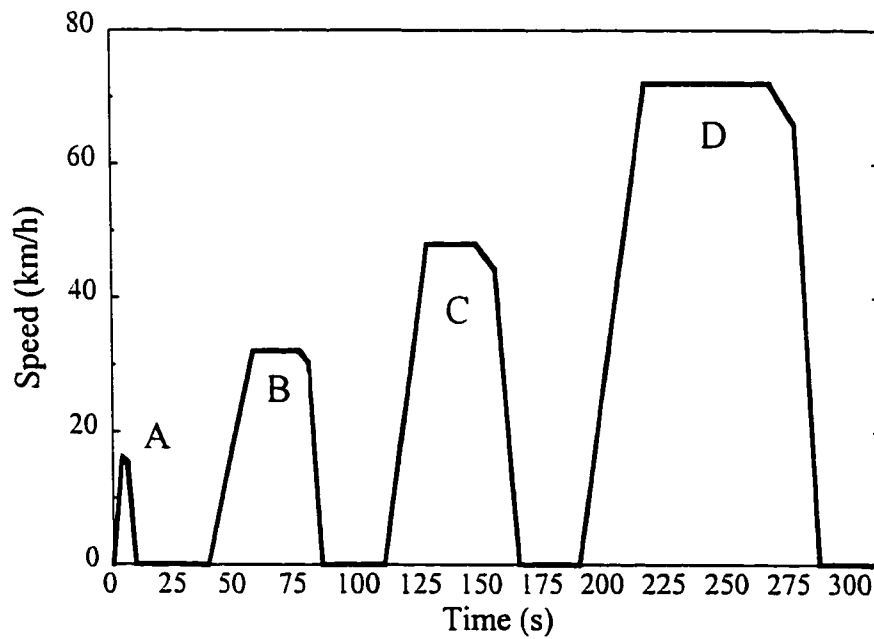


Figure 2.5 SAE J227a test cycle speed profile

at 96 km/h, to the point at which the vehicle comes to a standstill. Electric vehicles equipped with regenerative braking should have an additional specification reflecting their non friction braking capabilities. The author feels that this specification should be in terms of the amount of time it takes for an EV travelling at 96 km/h to slow down to a complete stop using only regenerative, non-friction, braking. Such a specification would provide useful information on the regenerative energy storage capabilities of the EV.

2.3 DRIVING CYCLE ENERGY FORMULATION

All of the driving cycles mentioned in Section 2.2 can be broken down into the EV modes of operation corresponding to acceleration, cruising, coasting, braking, and idling. The energy requirements for each mode of operation are calculated according to the general EV energy balance expression shown below.

$$\begin{array}{l} \text{NET} \\ \text{REQUIRED} \\ \text{ENERGY} \end{array} = \begin{array}{l} \text{TRANSIENT} \\ \text{ENERGY} \end{array} + \begin{array}{l} \text{DRIVE} \\ \text{LOSS} \\ \text{ENERGY} \end{array} + \begin{array}{l} \text{ROAD} \\ \text{LOSS} \\ \text{ENERGY} \end{array} + \begin{array}{l} \text{AUXILIARY} \\ \text{LOSS} \\ \text{ENERGY} \end{array} \quad (2.3)$$

Transient energy refers to the energy required (or available) to increase (or decrease) the kinetic energy of the EV. Estimates for the energy requirements of the four distinct modes of operation are developed in the following sections according to (2.3).

2.3.1 Acceleration/Braking Mode Energy Requirements

The acceleration/braking characteristics for any of the previously mentioned driving cycles are assumed to be constant over a small time interval $\Delta t = t_2 - t_1$. A time interval of 0.2 seconds was chosen for this investigation. The distance $d(t_2)$ and speed $v(t_2)$ at the

end of the time interval can be determined according to (2.4) and (2.5) for a given constant interval acceleration $a_{\Delta t}$, and initial distance $d(t_1)$ and speed $v(t_1)$ at the start of the time interval.

$$d(t_2) = d(t_1) + v(t_1)\Delta t + \frac{1}{2} a_{\Delta t} \Delta t^2 \quad (2.4)$$

$$v(t_2) = v(t_1) + a_{\Delta t} \Delta t \quad (2.5)$$

The incremental road loss energy ΔE_{ROAD} , auxiliary loss energy ΔE_{AUX} , and transient energy ΔE_{TRANS} , can be calculated as shown below using (2.4) and (2.5) with back-substitution into (2.1) and (2.2).

$$\Delta E_{ROAD} = F_A(v(t_1)) \cdot \Delta d + F_R \cdot \Delta d \quad (2.6)$$

$$\Delta E_{AUX} = P_A \cdot \Delta t \cdot \eta_B^{-1} \quad (2.7)$$

$$\Delta E_{TRANS} = M_{EV} \cdot a_{\Delta t} \cdot \Delta d \quad (2.8)$$

Constant auxiliary loss energy requirements are assumed to be supplied only by the EV battery. The remaining net energy requirements are assumed to be supplied entirely by the FESS, thereby reducing the peak power stresses on the EV batteries. The incremental net required energy ΔE_{NRE} can be calculated according to (2.9) for a positive EV acceleration $a_{\Delta t}$, and according to (2.10) for a negative $a_{\Delta t}$ representing an EV braking.

$$\Delta E_{NRE} = (\Delta E_{ROAD} + \Delta E_{TRANS}) \cdot (\eta_M \cdot \eta_G \cdot \eta_{ED} \cdot \eta_{CC} \cdot \eta_{ED} \cdot \eta_F)^{-1} + \Delta E_{AUX} \quad (2.9)$$

$$\Delta E_{NRE} = (\Delta E_{ROAD} + \Delta E_{TRANS}) \cdot (\eta_M \cdot \eta_G \cdot \eta_{ED} \cdot \eta_{CC} \cdot \eta_{ED} \cdot \eta_F) + \Delta E_{AUX} \quad (2.10)$$

The efficiencies in (2.9) and (2.10) correspond to the drive losses incurred as energy is transferred to and from the FESS. Incremental drive loss energy ΔE_{DRIVE} incurred during

acceleration can be calculated using the energy balance expression (2.3).

2.3.2 Cruising Mode Energy Requirements

The EV cruising mode corresponds to the maintaining of an EV at a constant non-zero speed. Equations (2.3) to (2.8), with $a_{\Delta t}$ set to zero, can be used to determine the incremental road, auxiliary, and transient energy requirements during this type of operation. Energy requirements are supplied by the EV battery during this mode. Hence, (2.11) should be used to calculate the net required energy to operate the EV.

$$\Delta E_{NRE} = (\Delta E_{ROAD} + \Delta E_{TRANS}) \cdot (\eta_M \cdot \eta_G \cdot \eta_{ED} \cdot \eta_B)^{-1} + \Delta E_{AUX} \quad (2.11)$$

2.3.3 Coasting Mode Energy Requirements

Auxiliary losses are the only energy demands necessary to operate the EV during the coasting mode of operation. The incremental net required energy ΔE_{NRE} can be calculated according to (2.12).

$$\Delta E_{NRE} = \Delta E_{AUX} \quad (2.12)$$

The road loss deceleration force experienced by the coasting EV can be calculated according to (2.2). The average deceleration over the small time interval Δt can be approximated using (2.13).

$$a_{\Delta t} = - (F_A(v(t_1)) + F_R) \cdot M_{EV}^{-1} \quad (2.13)$$

Incremental road loss energy can be determined by substituting $a_{\Delta t}$ into (2.4) and (2.5), with further substitution into (2.6). The transient energy will equate to the negative of the road loss energy, and the required drive energy is equal to zero for this EV mode of operation.

2.3.4 Idle Mode Energy Requirements

The idle mode of EV operation requires that energy is supplied to compensate for only the auxiliary losses. Drive loss, road loss, and transient energies are all equal to zero for this mode of operation. The incremental net required energy ΔE_{NRE} can be calculated according to (2.12) while the speed remains at zero and the distance travelled remains unchanged.

2.4 SIMULATION RESULTS FOR A COMBINED SAE J227a DRIVING CYCLE

The standard EV driving cycle test procedure SAE J227a was chosen for this EV simulation. The vehicle and environmental specifications outlined in Section 2.1 were applied to the simulated EV. Energy calculations were conducted according to the formulations proposed in Section 2.3. All four schedules of SAE J227a were simulated for 200 km as both individual and combined Schedule A-B-C-D driving patterns. A summary of the simulation results is shown in Table 2.6.

The energy and power requirements of the EV are shown in Figures 2.6 and 2.7 for one cycle of the combined Schedule A-B-C-D driving pattern. The benefits of regenerative braking can be visually appreciated by inspection of the ‘dips’ in the Net Energy requirement curve of Figure 2.6. Inclusion of a FESS as a SESU provides the ability to perform non-destructive regenerative braking. A 36% reduction in the required battery energy is obtained when performing regenerative braking on the combined schedule driving pattern. The effects of regenerative braking on the EV battery energy are even greater for schedules C and D, as shown in the last row of Table 2.6.

Table 2.6
SAE J227a Driving Cycle Simulation Results

Schedule	A	B	C	D	A-B-C-D
Maximum Net Required Energy E_{NRE} (kJ) (one cycle)	186.8	448.6	619.7	1551	2806
Maximum Net Required Energy E_{NRE} (MJ) (200 km)	1563	290.2	228.0	184.6	220.3
Maximum Required Battery Energy (kJ) (one cycle)	170.4	367.3	445.8	1003	1986
Maximum Required Battery Energy (MJ) (200 km)	1426	237.6	164.1	129.4	162.9
Maximum Required FESS Energy (kJ) (one cycle)	30.5	138.2	291.6	695.9	967.4
Maximum Required FESS Energy (MJ) (200 km)	137	52.7	64.1	55.4	57.6
FESS Peak Power Delivered (kW)	14.9	14.6	32.8	51.5	51.5
FESS Peak Power Accepted (kW)	9.1	22.2	25.6	58.1	58.1
Distance per cycle (m)	23.9	309.0	544.1	1553.7	2430.7
Cycles per 200 km	8368	647	368	129	82
Reduction in Required Battery Energy due to Regenerative Braking into FESS	15%	26%	38%	40%	36%

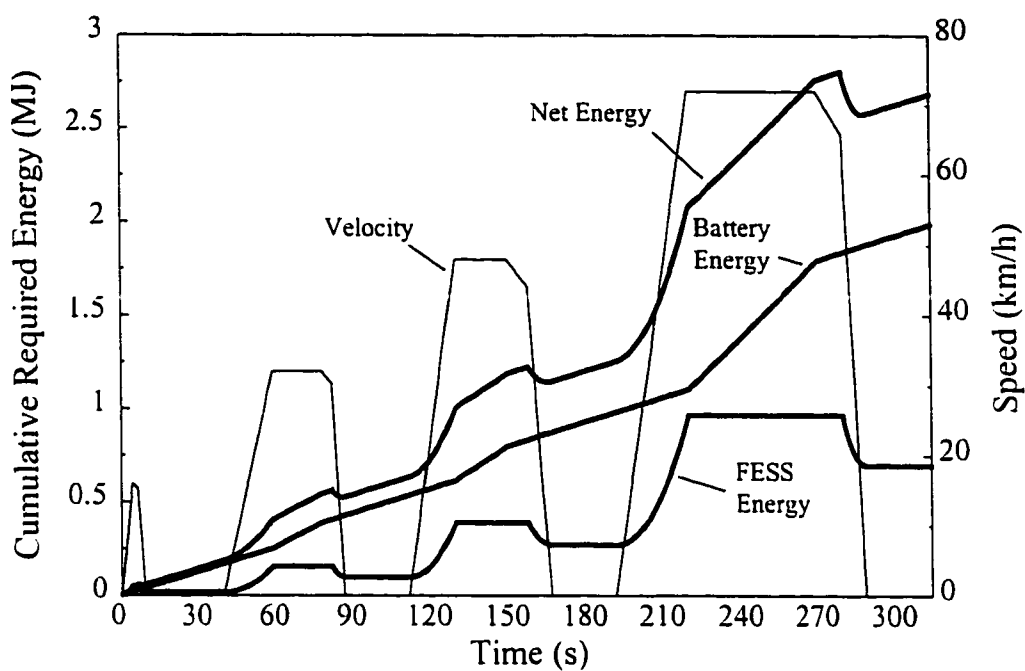


Figure 2.6 SAE J227a driving cycle EV simulation energy requirements

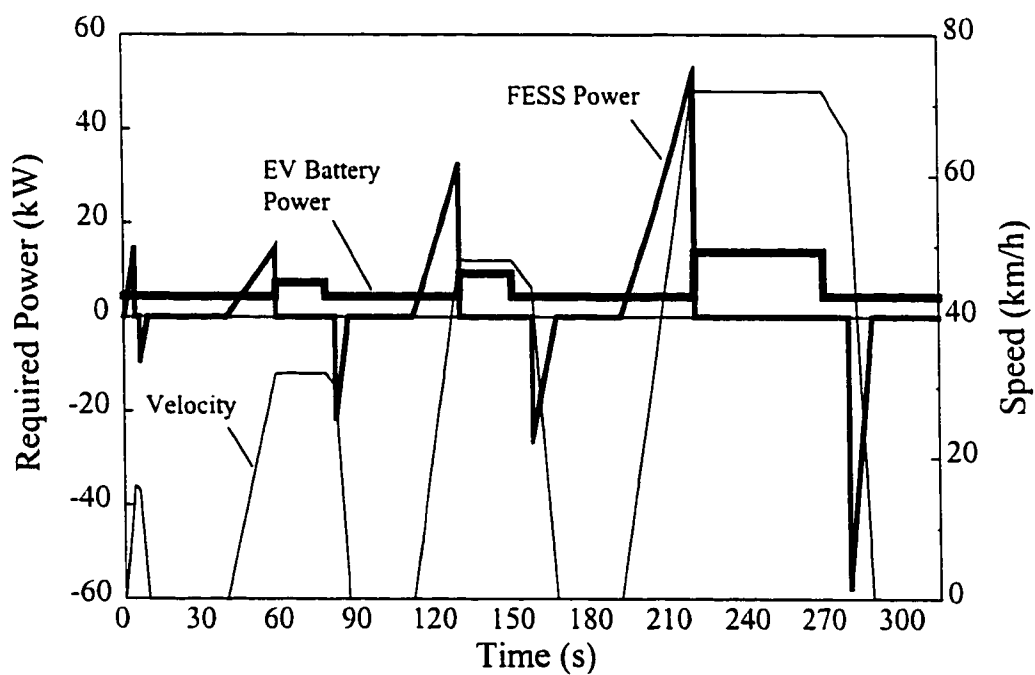


Figure 2.7 SAE J227a driving cycle EV simulation power requirements

Load levelling not only offers the possibility of reducing the EV battery size, but more importantly, it offers the possibility of reducing the peak power stresses on the EV batteries. The power profiles in Figure 2.6 show that transient, or ‘peak’ power requirements of up to 58 kW are diverted from the EV batteries and supplied by the FESS. Hence, the detrimental peak power stresses on the EV batteries are reduced. Peak power stress reduction offers a greater benefit for driving schedules such as A, B, and C, whose high and medium frequency stop and go operation will quickly damage the life-cycle capabilities of standard lead acid EV batteries.

Step changes in the EV battery power profile of Figure 2.6 are a result of the assumption that all of the transient power requirements are either supplied or accepted by the FESS. The conducted simulation also assumes that energy from the EV batteries is not used to recharge the FESS. Low power recharging of the FESS with EV battery energy will allow for further stress reduction by providing a more constant EV battery power demand. Section 2.7 proposes an investigation into the optimization of the EV battery power demand profile for power step reduction as one of the recommendations for further work.

2.5 SIMULATION RESULTS FOR 0-96-0 km/h ACCELERATION/BRAKING

An additional simulation was conducted to determine the energy and peak power requirements during a 0 to 96 km/h acceleration in 10 seconds, followed immediately by a 96 to 0 km/h regenerative braking in 7 seconds. Identification of these energy and power requirements provides insight into the EV battery and FESS sizing requirements necessary to provide an EV with the acceleration and braking capabilities specified in Table 2.1.

Table 2.7
0-96-0 km/h Driving Cycle Simulation Results

Schedule	0-96-0 km/h
Maximum Net Required Energy E_{NRE} (kJ)	1109
Maximum Required Battery Energy (kJ)	71.7
Maximum Required FESS Energy (kJ)	1065
FESS Peak Power Delivered (kW)	216.5
FESS Peak Power Accepted (kW)	150.5
Distance per cycle (m)	226.7
Effect of FESS on EV Battery Size Reduction	93%

The simulated EV energy and power requirements are shown in Figures 2.8 and 2.9, with key results summarized in Table 2.7. The results indicate that the simulated EV must be able to draw at least 221 kW of power from its stored energy units during the specified 0-96 km/h acceleration in 10 seconds. Peak power stresses can be supplied by a SESU consisting of a 217 kW FESS, while the remaining 6 kW auxiliary power demand is supplied by the EV batteries, as shown in Figure 2.9. Hence, the damaging effects of peak power demands on the EV batteries can be avoided.

A seven second, 96-0 km/h regenerative braking requires 159 kW of net peak power acceptance capability. Regenerative braking at these power levels will damage standard EV batteries and will require a greatly oversized battery pack. The EV simulation shows

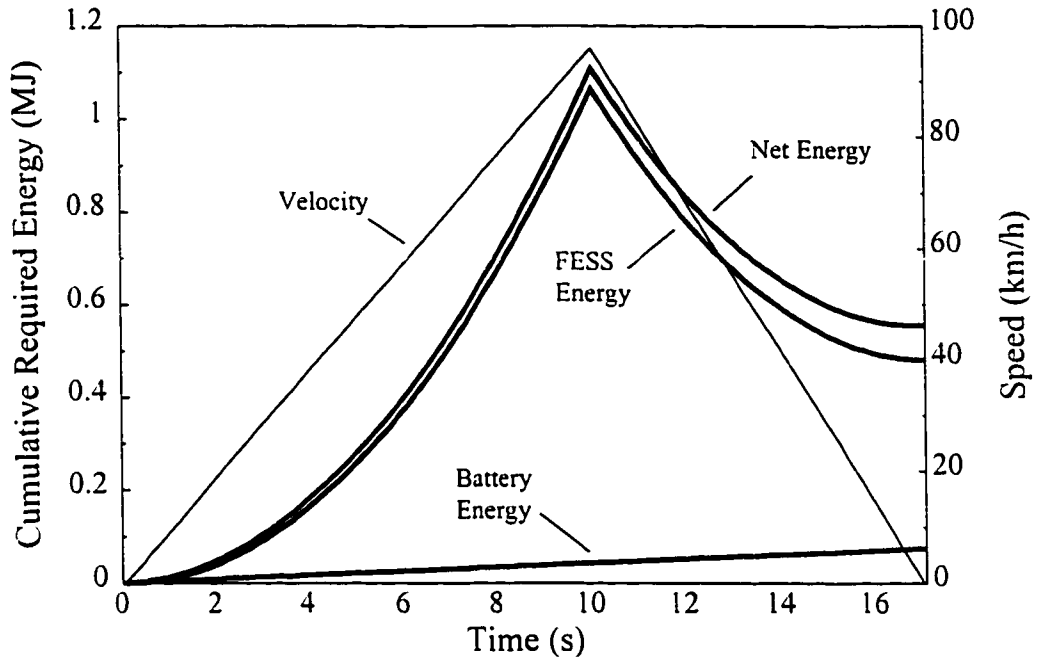


Figure 2.8 0-96-0 km/h driving cycle EV simulation energy requirements

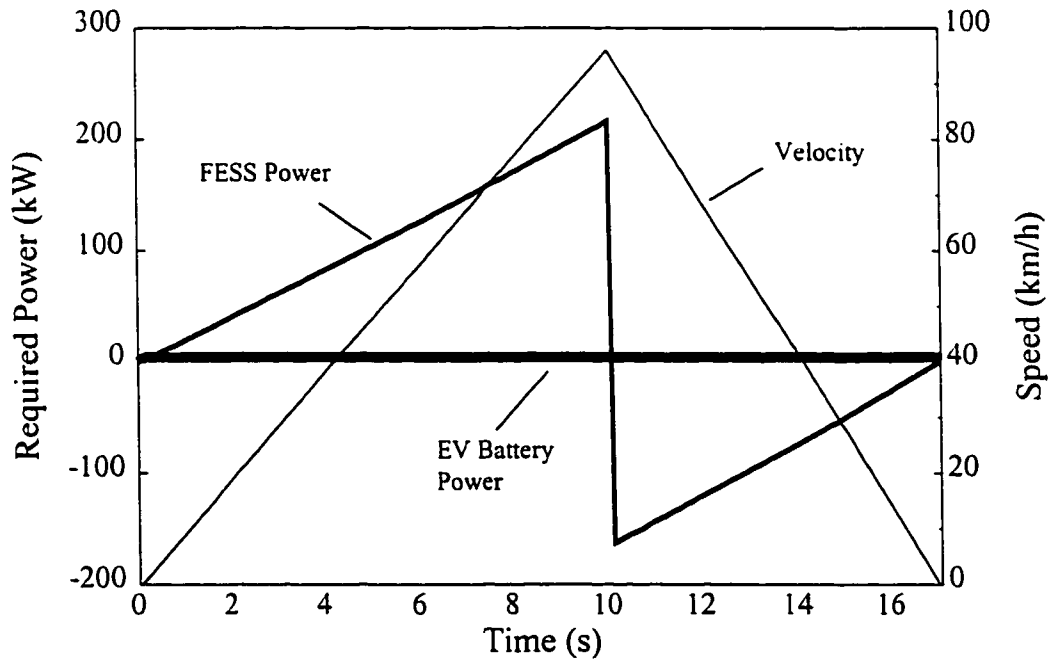


Figure 2.9 0-96-0 km/h driving cycle EV simulation power requirements

that a SESU consisting of a 163 kW FESS will allow the EV to meet the 7 second regenerative braking capability specifications, while recovering nearly 55% of the drive energy used to accelerate the vehicle. Further simulation shows that a 217 kW FESS is required to provide the EV with a 10 second 0-96 km/h acceleration capability. The same FESS will also allow for a 96-0 km/h regenerative braking capability of less than 5.4 seconds.

2.6 EV ENERGY STORAGE COMPONENT SIZING

2.6.1 Practical Energy Storage Unit Specifications

Simulation often provides results that cannot be easily met with current technology. The simulation results of the previous two sections provide information on the EV energy storage requirements necessary for EV operation according to those particular driving schedules. Practical validity of the simulation results necessitates that the energy storage requirements are compared with the energy storage capabilities of current EV batteries and near-term flywheels. Table 2.8 lists the energy and power densities of the possible

Table 2.8
Current Energy Storage Unit Capabilities

ENERGY STORAGE UNIT	ENERGY DENSITY	POWER DENSITY
ADVANCED LEAD ACID BATTERY	42 Wh/kg (100 Wh/l)	240 W/kg @ 80% DOD (571 W/l)
INTEGRATED FESS	22.7 Wh/kg (25 Wh/l)	250 W/kg (275 W/l)
DOUBLE LAYERED CAPACITORS	5 Wh/kg (4.5 Wh/l)	Variable
ELECTROLYTIC CAPACITORS	0.055 Wh/kg (0.05 Wh/l)	Variable
GASOLINE	12880 Wh/kg (9688 Wh/l)	--

components used for energy storage in the EV. The energy density of gasoline is provided for comparison [12].

Near-term high speed flywheels having the size and outline of a large frisbee, can store 1 kWh of energy with less than 11 kg of flywheel mass [10]. Power densities of greater than 1 kW/kg are also specified for this type of flywheel. The mass of a protective vacuum housing, electrical machine, and the necessary control electronics must still be included in these specifications. The author believes that a 1:3 ratio between the flywheel mass and the remaining FESS component masses, including the electrical machine, is a realistic target. A 1 kWh integrated FESS unit will have a total mass of 44 kg, a volume of 40 litres, an energy density of 22.7 Wh/kg, and a power density of 250 W/kg.

Double layered and electrolytic capacitors can also be used to meet energy storage requirements. Near term double layered, or 'supercapacitors', are specified as having an energy density of up to 5 Wh/kg [18]. The 20 kg, 22 litre, electrolytic capacitor energy storage tank used in [11, p.70] yields a low 0.055 kW/kg energy density. The useful power obtained from capacitors is limited by their Equivalent Series Resistance (ESR). Hence, their power densities are variable according to their rates of discharge. The use of double layered and electrolytic capacitors will be discussed in Section 2.7.

2.6.2 Energy Storage Unit Sizing of the Simulated EV with no FESS

The simulation results in Table 2.6 indicate the necessary energy and power requirements to operate a simulated FESS equipped EV over the various SAE J227a schedules. A similar simulation was conducted to determine different energy requirements be-

tween an EV with no regenerative braking, and an EV that uses regenerative braking into the EV batteries. Table 2.9 is used to translate the energy requirements into the energy storage unit masses that need to be integrated into the two different 2200 kg total mass EVs. The required stored battery energy is determined on the basis of a maximum 80% DOD and recharging efficiency of 70% [19]. All of the attempted regenerative braking into the EV batteries is assumed to be accepted by the EV batteries at the recharging efficiency.

Table 2.9 indicates that minimum power capabilities for both vehicles are well within the Figure 2.9 power requirements that will provide the EV with the desired 0-96-0 km/h performance characteristics. The unacceptable high equivalent battery masses indicate that current technology cannot produce a viably sized, advanced lead acid battery,

Table 2.9
Non-FESS Equipped EV Energy Storage Unit Sizing for 200 km Operation

Schedule	A	B	C	D	A-B-C-D
Required Stored Battery Energy (kWh) (no regen. braking)	579	112	92.4	74.7	87.9
Equivalent Battery Mass (kg) (no regen. braking)	13796	2670	2199	1778	2092
Minimum Power Capability (kW) (no regen. braking)	3310	641	528	427	502
Required Stored Battery Energy (kWh) (regen. braking)	547	102	80.3	64.9	79.3
Equivalent Battery Mass (kg) (regen. braking)	13016	2424	1913	1545	1888
Minimum Power Capability (kW) (regen. braking)	3120	582	459	371	453
% Battery Reduction Through Regenerative Braking	5.7	9.1	13	13	12

energy storage unit that can be integrated into a 2200 kg net mass EV and provide it with a range of 200 km over any of the SAE J227a driving schedules.

Regenerative braking into the EV battery does show promise for operation according to Schedule D, with an approximately 13% reduction of the required energy storage unit size. The advantage gained by regenerative braking into the EV batteries will, however, be rapidly lost as such braking will reduce the lifetime of the lead acid batteries. Experience with Automatically Guided Vehicles (AGV) at a large automotive plant has shown that lead acid batteries are destroyed within a few months when subjected to peak power regenerative braking². Use of a FESS as a SESU for load levelling may provide a solution to the EV energy storage unit sizing difficulties.

2.6.3 Energy Storage Unit Sizing of the Simulated EV with a FESS

The FESS equipped EV simulation results of Table 2.6 are translated into actual energy storage component masses by using the energy storage capabilities in Table 2.8. The required stored battery energy and the required stored FESS energy are both determined on the basis of a maximum 80% DOD. An 80% DOD operation of the FESS corresponds to operation between maximum and 45% of maximum speed. Energy storage unit sizing results for the simulated FESS equipped EV are listed in Table 2.10.

The peak power transfer simulations in Sections 2.4 and 2.5 showed how a FESS can be used to perform load levelling and reduce the peak power stresses on the EV batter-

² Based on information provided by Dr. Barna Szabados, Director of the Power Research Laboratory, McMaster University, Hamilton, Ontario, Canada, and by Chris Dilelo, AGV Maintenance Supervisor, General Motors, Oshawa, Ontario, Canada.

ies. The sizing results in Table 2.10 indicate that current technology cannot produce a viably sized energy storage unit for a FESS equipped EV, that will allow the EV to operate for 200 km along the SAE J227a schedules. Both the advanced lead acid battery and the integrated FESS have net energy densities that fall below those which will be necessary to provide the simulated 2200 kg EV with the desired 200 km driving range and characteristics. The required minimum power densities are satisfied, as shown by the results in Table 2.10. A FESS equipped EV incorporating the 2701 kg energy storage unit required for a 200 km repeated combined SAE J227a schedule, will also be able to meet the 0-96-0 km/h acceleration/braking specification. The major problem with the practical realization of such an EV is the integration of the 2701 kg energy storage unit with EV so that the total mass

Table 2.10
FESS Equipped EV Energy Storage Unit Sizing for 200 km Operation

Schedule	A	B	C	D	A-B-C-D
Required Stored Battery Energy (kWh)	543	101	79.2	64.1	76.5
Equivalent Battery Mass (kg)	12300	2405	1886	1526	1821
Required Stored FESS Energy (kWh)	47.6	18.3	22.3	19.2	20.0
Equivalent FESS Mass (kg)	2090	805	981	845	880
Total Mass of Energy Storage Unit (kg)	14390	3210	2867	2371	2701
Minimum FESS Peak Power Capability (kW)	524	201	245	211	220
% Battery Reduction Through Inclusion of a FESS as a SESU	5.5	0.8	1.4	1.2	3.5

does not exceed the simulated specification of 2200 kg.

It is important to note that the presented results reflect the required sizing of an unoptimized system. The Table 2.6 and 2.10 results are from a simulation that assumes all of the transient energy is supplied by the FESS during EV acceleration and braking. Optimization of the power sharing between the FESS and the EV batteries during acceleration and braking will lead to a higher than proposed ratio between the EV battery and FESS energies. Power sharing will also maintain a smoother battery power profile, as has already been mentioned in Section 2.6. The author believes that the proposed total mass of the energy storage unit will fall by several 100 kg during the optimization process. An optimized FESS equipped EV will have a net energy storage unit mass somewhere within the optimization limits specified by the equivalent battery mass (regen. braking) listed in Table 2.9, and the total energy storage unit mass listed in Table 2.10. It is unfortunate that with current technology, the resulting optimized energy storage unit will still not produce a viably sized unit that can be readily integrated with the EV. The proposed optimization, and the results of this investigation will, and do, show that the FESS equipped EV total energy storage unit masses are close enough in comparison with those of Table 2.9 to warrant the consideration of using a FESS to reduce the peak power stresses on the EV batteries.

2.6.4 Effects of Technological Developments on Energy Storage Unit Sizing

Near term technology developments may improve the energy storage capabilities of lead acid batteries to 80 Wh/kg. Experimental units with densities of 52 Wh/kg have already been reported [2]. EV batteries can also be optimized for operation with a load

levelling SESU such as a FESS. Sodium sulphur batteries already provide energy densities of above 80 Wh/kg [20]. Their prohibitive cost may be overcome through life cycle improvements when used with a SESU.

The effects of a technological advancement on the energy storage capabilities of the EV batteries are shown in Table 2.11. The listed results provide the new limits for FESS equipped EV energy storage unit optimization if the EV battery energy density is improved to 80 Wh/kg. Optimization of the FESS equipped EV energy storage unit for power sharing operation along the SAE J227a combined and D schedules, could reduce the energy storage unit mass to near, or below, 1000 kg. A 1000 kg energy storage unit will allow another 1000 kg for the EV body, wheels, and drive, as well as 200 kg for passengers and luggage. Even though the vehicle specifications are currently not fully met, the results of this investigation have shown that the proposed FESS is almost feasible with only a small change in current technology. The proposed FESS will also become a viable solution for peak power stress removal from EV batteries as the near-term technology improvements are made com-

Table 2.11
Improved Optimization Limits for Energy Storage Unit Sizing

Schedule	A	B	C	D	A-B-C-D
Mass of Required Batteries (Regen. through EV batteries) (kg)	6833	1272	1004	811	968
Unoptimized Mass of FESS Equipped EV Energy Storage Unit (kg)	8551	2067	1971	1646	1836

mercially available.

2.6.5 Energy Storage Unit Sizing Comparison with the GM Impact

The results from the conducted EV simulations have provided battery and battery/FESS sizing specifications that seem, at first glance, to be greatly overstated. The previously mentioned GM Impact EV boasts a 110 city and 145 km highway driving range. It can provide these specifications with a battery capacity of only 16.8 kWh, and a net curb weight of only 1323 kg [2]. The Impact's 400 kg battery pack is less than 26% of the lowest energy storage unit specification provided in Tables 2.9 and 2.10. Further investigation shows why.

A new simulation was conducted to determine the energy requirements of the GE Impact over the same SAE J227a driving schedules used for the previous energy storage sizing unit simulations. The simulated vehicle drag coefficient was reduced to 0.19, and its net mass was reduced to 1583 kg, representing the Impact's mass, two passengers, and half of the luggage used in the previous simulations. Accessories were maintained at 2/3 utilization and the same tires were used as in the previous simulations. The energy requirements and resulting driving ranges over the SAE J227a test schedules are provided in Table 2.12.

Inspection of the Table 2.12 data shows that GM Impact will only provide a maximum SAE J227 range of 64 km when equipped with a 16.8 kWh, 80% DOD, battery energy storage unit. The required battery masses for a 200 km range over the repeated cycles indicate the same overweight problems that were determined in Sections 2.6.2 and 2.6.3. The GM specified driving ranges are significantly different from those determined from the

simulated Impact. An adjustment of the simulated Impact's auxiliary power requirements revealed the cause for the driving range difference. All accessories were turned off and the simulated Impact was once again driven through the SAE J227a test cycles. The resulting cycle energy requirements and attainable driving range on a 16.8 kWh battery supply are shown in the last two rows of Table 2.12. The combined schedule A-B-C-D driving range of 108 km is very comparable to the 110 km city driving range specified by GM. Additional driving range improvements can be made for the simulated Impact by simply omitting the 100 kg luggage and one 80 kg passenger.

It is evident that current EV specifications provide energy storage unit sizings and driving ranges for only the optimal, minimum weight, and minimum accessories operation.

Table 2.12
GM Impact Energy Storage Unit Sizing Requirements for 200 km of SAE J227a

SCHEDULE	A	B	C	D	A-B-C-D
Cycle Net Required Battery Energy (ACCESSORIES ON) (Wh)	50.9	115	151	323	640
Driving Range with 16.8 kWh Battery (ACCESSORIES ON) (km)	6.3	36	48	64	51
Required Battery Mass for 200 km Range (kg)	12667	2706	1657	1241	1562
Cycle Net Required Battery Energy (ACCESSORIES OFF) (Wh)	6.03	36.7	73.8	217	303
Driving Range with 16.8 kWh Battery (ACCESSORIES OFF) (km)	53	113	99	96	108

The poor performance of the GE Impact over the simulated operation of the SAE J227a driving cycles validates the results of Tables 2.9 and 2.10, and provides clear evidence that current technology cannot meet the required desired performance characteristics that were specified in the onset of this investigation. The results in this section have provided insight into the minimum requirements that will allow EVs to compete directly with ICE powered vehicles in terms of performance and comfort. Electric vehicle pricing depends on a maturing of the technology and is beyond the scope of this research. The inclusion of a FESS for secondary energy storage can provide the benefits of added performance and increased battery life that can outweigh the additional cost. Practical realization of a FESS equipped EV will require additional research into the actual integrated FESS.

2.7 SIMULATION IMPROVEMENTS AND FURTHER WORK

The conducted simulation results represent the initial work for a full scale EV simulation and test program. The simulation program would require user inputs for vehicle specifications, driving schedules, driving terrain, loss coefficients, EV battery sizing, SESU sizing, load levelling power sharing ratios, and pricing. Similar inputs would be required for ICE powered vehicle specifications which would allow a comparison to be made to determine in what applications EVs can best compete. Optimization of the power sharing ratios between EV batteries and SESUs, such as integrated FESSs, would also be performed using this simulation and test program. The European and EPA driving schedules should be investigated with this program for added validity when comparing EVs to ICE powered vehicles.

The EV simulation results of this investigation have demonstrated the principle of peak power sharing between EV batteries and an integrated FESS. The simulation results have also revealed the requirements for the practical implementation of such peak power sharing. Previous work in [11, p.70] has indicated that the proposed FESS may not be able to accommodate the instantaneous power transients incurred during regenerative braking. These findings are now supported with the 0-96-0 km/h simulation study, which reveals a 367 kW transient power reversal in the FESS energy requirements, as shown in Figure 2.9. Simulations of the SAE J227a driving cycle, shown in Figure 2.7, reveal a 58 kW maximum transient power requirement on the FESS during Schedule D regenerative braking.

An energy storage tank, proposed in [11, p.70], temporarily stores the EV braking energy until the FESS's electric machine can convert it into the kinetic energy of the flywheel. A suitable energy storage tank could be made from a capacitor bank. The capacitor bank can be made of the newly developed double layered or the standard electrolytic capacitors that were introduced in Section 2.6.2 and specified in Table 2.8. Current technology can produce 1 volt double layered capacitor modules with a 1.5 F capacitance and an ESR of 0.1 ohm [18]. Double layered capacitors do not exhibit the peak power transfer induced lifetime degradation effects found with electrochemical batteries. Hence, double layered capacitors could prove to be a viable candidate, not only for temporary energy storage use in a FESS unit, but also for sole use as the secondary energy storage unit of an EV

An EV energy storage tank made of double layered capacitors would require approximately 400, 1 volt modules stacked in series. A 400 volt double layered capacitor

module would have a net capacitance of 3750 μF and an ESR of 40 Ω . The low net capacitance and high ESR makes it infeasible to construct high voltage energy storage tanks using double layered capacitors. The high energy density of double layered capacitors (up to 5 Wh/kg, see Table 2.8) and low voltage power transfer capabilities, does warrant their consideration for use in a low voltage energy storage tank. Voltage level conversion between the EV dc bus voltage, energy storage tank, and FESS electrical machine will add complexity and increased losses to the integrated FESS. The added complexity and losses make standard electrolytic capacitors a more suitable candidate for use as an energy storage tank in a 300 V dc bus EV. Hence, further investigations into the FESSs energy transfer characteristics will make use of an electrolytic capacitor energy storage tank.

Low voltage double layered capacitor modules for use as the sole secondary energy storage device in a load levelling strategy, could be a competitive solution to peak power stress reduction in EV batteries. The focus of this research is solely on the development of an integrated FESS. An investigation into the SESU use of low voltage double layered capacitor modules is recommended for further work.

Previous work done by in [11] has demonstrated the principle of flywheel stored energy transfer through an electrolytic capacitor energy storage tank to a power electronic regulated dc bus. The transient power levels determined by simulations in this chapter have indicated the need to enhance the findings in [11], and to conduct further investigation into the regenerative braking mode energy transfer capabilities through the energy storage tank. An investigation into these energy transfer capabilities will now become the focus of the remainder of this research.

CHAPTER 3

PEAK POWER TRANSFER INVESTIGATION

3.1 PREVIOUS TEST RESULTS

The energy transfer capabilities from the FESS to the regulated dc bus of the electric vehicle drive system, shown in Figure 1.2, was previously demonstrated in [11, pp.71-74]. Energy was transferred from a flywheel coupled directly to a commercially available 3 hp PMSM, thru a 0.094 F electrolytic capacitor bank, and into a step current load demand from a resistive load bank. Tests conducted using a 0.3 p.u. step load current showed that a resonant surge current of approximately 2.5 p.u. was supplied by the PMSM to rapidly replenish energy lost from the storage tank. The magnitude of this surge current was proportional to the difference between the back-emf of the PMSM and the voltage level on the energy storage tank.

The results of the initial study in [11] indicate that rapid energy transfer can be achieved through the energy storage tank during a simulated vehicle acceleration. The size of the required energy storage tank depends on the peak power (and hence torque) rating of the PMSM. A 0.3 p.u. step load current represents only a 30% utilization of the PMSM rated capabilities. Testing at higher levels of step load current is needed to determine the response of the system when full utilization is made of the PMSMs capabilities. Electric vehicle braking requires energy transfer into the FESS. Testing for the EV braking mode

operation of the prototype FESS is still required.

The research in this chapter was conducted to enhance the acceleration mode findings in [11] and to test the EV braking mode energy transfer capabilities of the test bench FESS. Experimental analysis of the braking mode requires control capabilities over the 3500 to 7500 rpm speed range of the 3-phase PMSM. Limited previous research has been conducted into the integral hp machine control at speeds above 3600 rpm. This research will focus on the development and testing of a simple, cost effective, and reliable method of such control for the 3 phase PMSM/flywheel combination of Figure 1.2.

3.2 VOLTAGE SOURCE INVERTER CONTROL REALIZATION

3.2.1 Theoretical Development of VSI Switching Pattern

A Voltage Source Inverter (VSI) method of control was chosen by this author as the quickest and simplest method of performing high speed PMSM control. Figure 3.1 shows the basic switching component diagram of a VSI. The commutation logic and control algorithm block is used to determine the required switching states of switches S1 to S6.

A PMSM can be designed with back-EMF waveshapes ranging from a trapezoidal to a purely sinusoidal nature [21]. Stepped current waveform switching can be used with trapezoidal back-EMF machines to produce near constant output torque. Sinusoidal back-EMF machines excited with sinusoidal current waveforms can produce ripple-free constant torque at high efficiencies. Stepped current waveform switching offers the advantages of simplistic control and low frequency VSI operation when compared with the requirements for sinusoidal current waveform generation. Such advantages make stepped current wave-

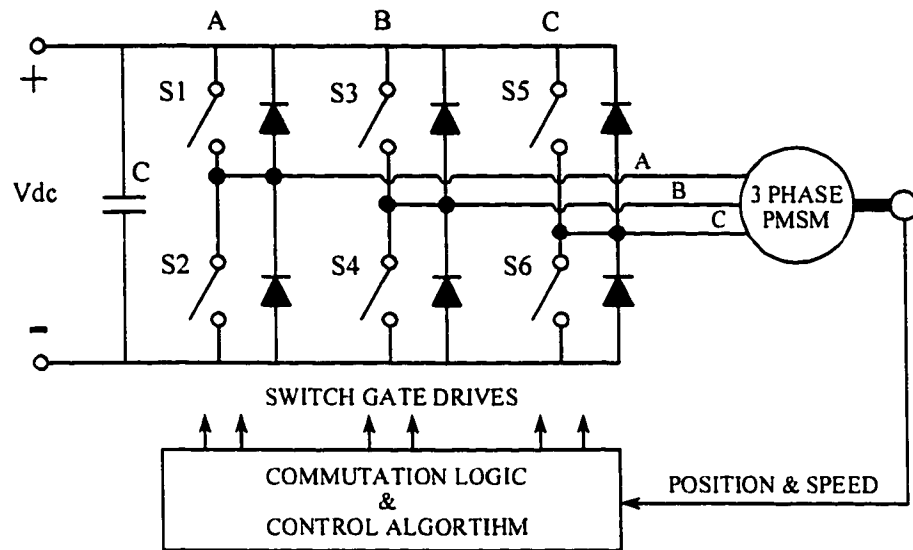


Figure 3.1 Voltage source inverter switching component diagram

form switching ideal for use in high speed PMSM applications such as the proposed FESS. The periodic torque ripple component developed with stepped current operation of trapezoidal or sinusoidal back-EMF PMSMs are negligible when the PMSM is used at high speeds and directly coupled with the high inertia of a flywheel.

A stepped current waveform can be produced by operating a VSI according to six distinct modes of operation. Figure 3.2 shows the switch positions and current paths corresponding to these six modes of operation. The back-EMF of a PMSM is used to develop the required full wave switching algorithm for the desired stepped current waveform control. Figure 3.3 shows the fundamental components of the back-EMF and the required VSI switching action over one electrical cycle of the PMSM. The resulting 3-phase current waveshapes produced by this type of switching algorithm are shown in Figure 3.4.

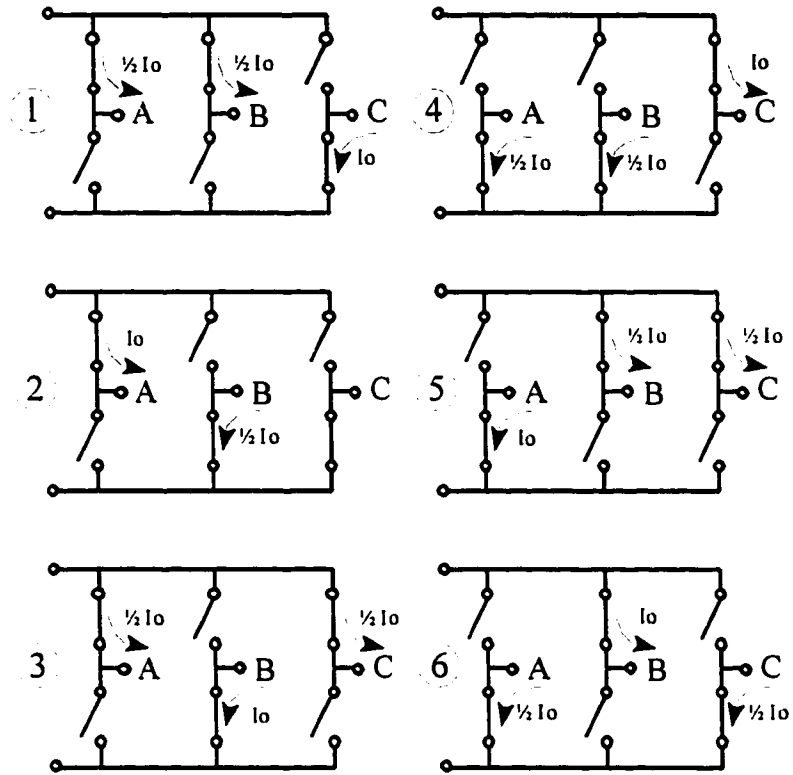


Figure 3.2 Six modes of VSI operation

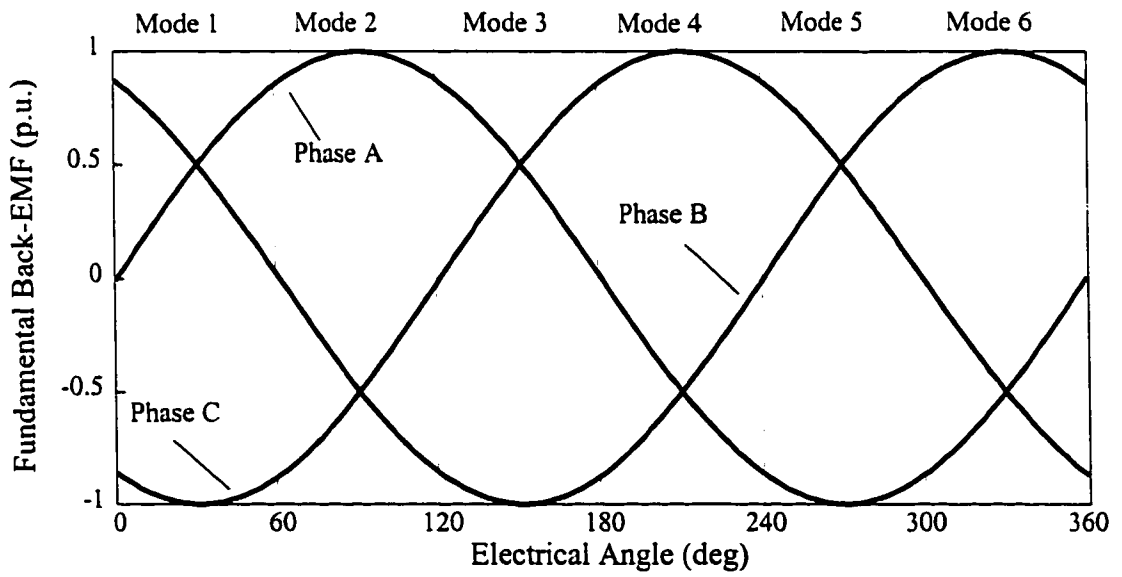


Figure 3.3 VSI mode timing with fundamental back-EMF waveforms

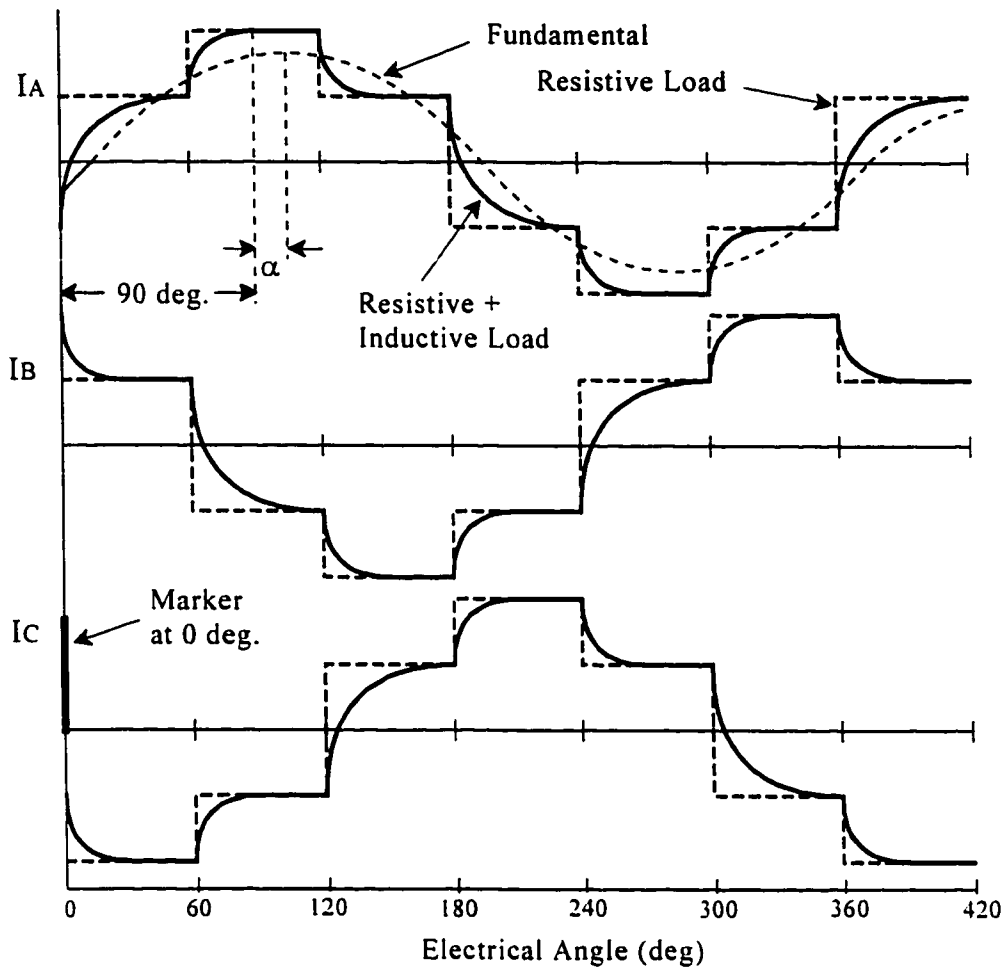


Figure 3.4 Current waveshapes produced by VSI

3.2.2 Simplified Current Vector Control

Switching the VSI into a partially inductive load will produce fundamental phase current components that will lag the VSI phase voltages. Voltage source inverter switching according to the back-EMF patterns in Figure 3.3 produce fundamental component waveform patterns that will also lag the PMSMs back-EMF waveforms. The angle α , in Figure 3.4, is used to represent the amount of phase lag between the phase current and back-EMF fundamental component. The phase lag can be reduced to near 0 degrees by advancing the

switching modes in Figure 3.3 by the angle α . Advancing and delaying the VSI switching patterns provides a simple method of fundamental current vector control that can be used to experimentally adjust the step phase current waveforms and provide the highest achievable PMSM performance.

3.2.3 Laboratory Implementation of the Voltage Source Inverter Drive

Figure 3.5 shows the basic control diagram for the proposed high speed step current VSI controlled PMSM drive. A laboratory test setup was constructed according to Figure 3.5. The setup uses a shaft position encoder, connected to the 3 phase PMSM rotor, to generate one marker pulse and 1250 timing pulses per mechanical revolution. The encoder and the PMSM are identical to the ones used for the initial demonstration in [11, p.59]. A presetable counter is used to count the number of encoder timing pulses, reset itself after 1250 timing pulses, and preset its count to an adjustable preset value each time a marker signal occurs. The commutation logic block is used to translate the value of the counter to an appropriate switching action according to Table 3.1. The switching action

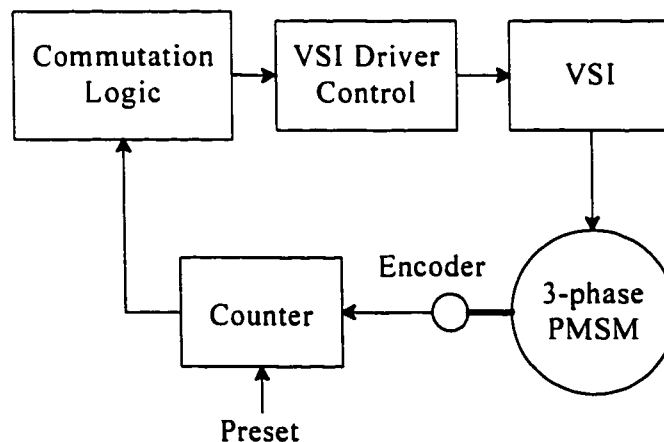


Figure 3.5 Control structure of high speed step current VSI controlled PMSM drive

'A^{TOP}_{ON}' refers to setting the top switch of the phase A inverter leg to the 'on' position. The switching action 'A^{BOT}_{OFF}' refers to setting the top switch of the phase A inverter leg to the 'off' position.

A four degree electrical angle deadtime is used to avoid inverter leg shoot-through faults. The commutation logic in Table 3.1 will produce the Figure 3.4 current waveshapes if the preset value to the counter is set to binary 0000 0000 0000. The simplified current

Table 3.1
VSI Commutation Logic

Trigger Angle (deg)	Trigger Function	Binary Equivalent	
		MSB	LSB
-2	A ^{BOT} _{OFF}	1111	1111 1001
2	A ^{TOP} _{ON}	0000	0000 0111
58	B ^{TOP} _{OFF}	0000	1100 1001
62	B ^{BOT} _{ON}	0000	1101 1000
118	C ^{BOT} _{OFF}	0001	1001 1001
122	C ^{TOP} _{ON}	0001	1010 1000
178	A ^{TOP} _{OFF}	0010	0110 1010
182	A ^{BOT} _{ON}	0010	0111 1000
238	B ^{BOT} _{OFF}	0011	0011 1010
242	B ^{TOP} _{ON}	0011	0100 1001
298	C ^{TOP} _{OFF}	0100	0000 1010
302	C ^{BOT} _{ON}	0100	0001 1001
358	A ^{BOT} _{OFF}	0100	1101 1011
360	RESET COUNTER	0100	1110 0010

vector control in Section 3.2.2 is realized by adjusting the counter preset value. A continuous current vector angle adjustment of -57° to $+359^\circ$ is possible by adjusting the preset value from 1111 0011 1010 to 0100 1101 1110. Switching signals can be manually enabled and disabled through the VSI driver control block. A lockout circuit is included in this block to protect against a logic error induced by either electronic failure or electrical noise. A fail-safe mode is employed to ensure that all switching signals are forced 'off' rather than 'on' during an accidental power loss while the inverter is operating.

The VSI used for this investigation is identical to the one proposed and constructed in [11, pp.29-45]. It consists of Insulated Gate Bipolar Transistors (IGBT), IGBT gate drivers, snubber circuits and a sinusoidal back-EMF Interior Permanent Magnet Synchronous Machine (IPMSM). The 0.094 F energy storage tank is connected directly across the dc supply to the VSI. The complete schematics and connection diagrams for the laboratory implemented high speed step current VSI controlled PMSM drive is provided in the supplementary document for this thesis.

3.3 LABORATORY SETUP FOR ENERGY TRANSFER TESTING

3.3.1 Step Current Source and Load Setup

This investigation uses a step current source and load for the EV braking and acceleration mode testing of the proposed FESS. Figure 3.6 indicates the blocks required to construct the desired current source and load circuits. A step current source into the energy storage tank is created by chopping the laboratory dc voltage supply with a dedicated power electronic chopper. The storage tank current is measured and a proportional signal is fed

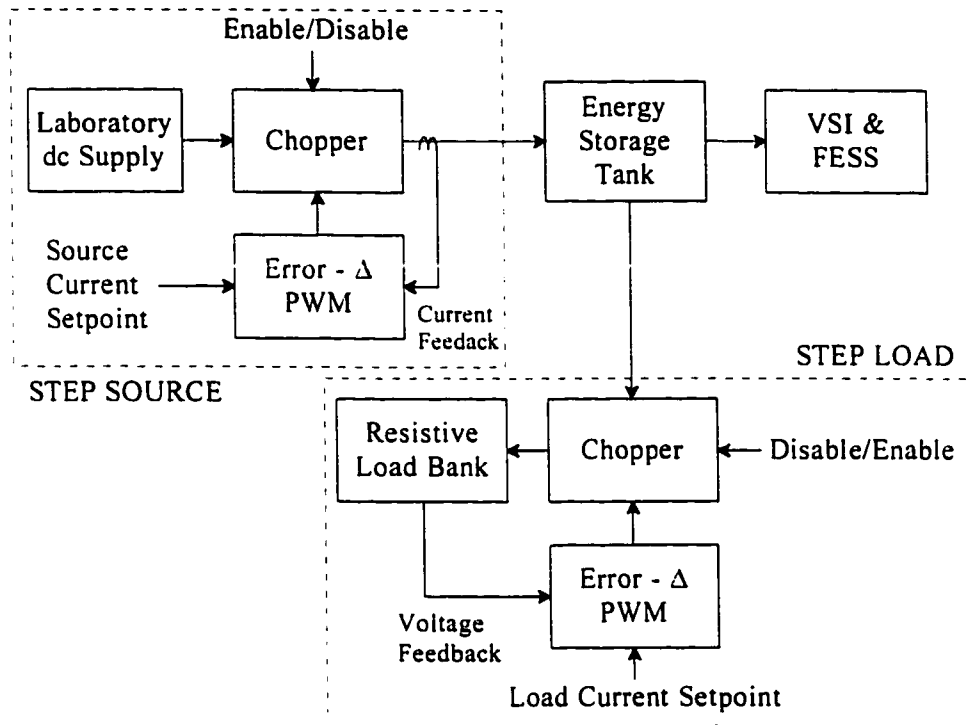


Figure 3.6 Step current source and load circuit setup

back to an error- Δ Pulse Width Modulation (PWM) controller that is used to generate the switching signals to the chopper. A step current is generated by enabling the chopper and varying the current setpoint into the error- Δ PWM controller from one preset point to another.

A step current load out of the energy storage tank is created by adding another dedicated power electronic chopper and chopping the dc tank voltage across a resistive load bank. The resistive load bank voltage is measured and a proportional signal is fed back to the error- Δ PWM controller. A step load current is generated by enabling the chopper connected to the resistive load bank and varying the desired current setpoint from one preset value to another. The complete schematics and connection diagrams for the laboratory implemented step current source and load circuitry are provided in the supplementary docu-

ment to this thesis.

3.3.2 Data Measurement Circuit Setup

Energy transfer testing of the proposed FESS requires knowledge of the FESS speed, energy storage tank voltage, and tank input/output current. Figure 3.7 provides a block diagram for the data measurement components used during the tests. A Tektronix TM504 current amplifier is used to measure the current between the current load/source and the energy storage tank, as well as between energy storage tank and the FESS. A voltage divider circuit provides a signal proportional to the tank voltage. Timing signals from the encoder are applied to a tachometer circuit to produce a signal proportional to the speed of the FESS. The measured signals are applied to a scaling and adjust circuit so that they can

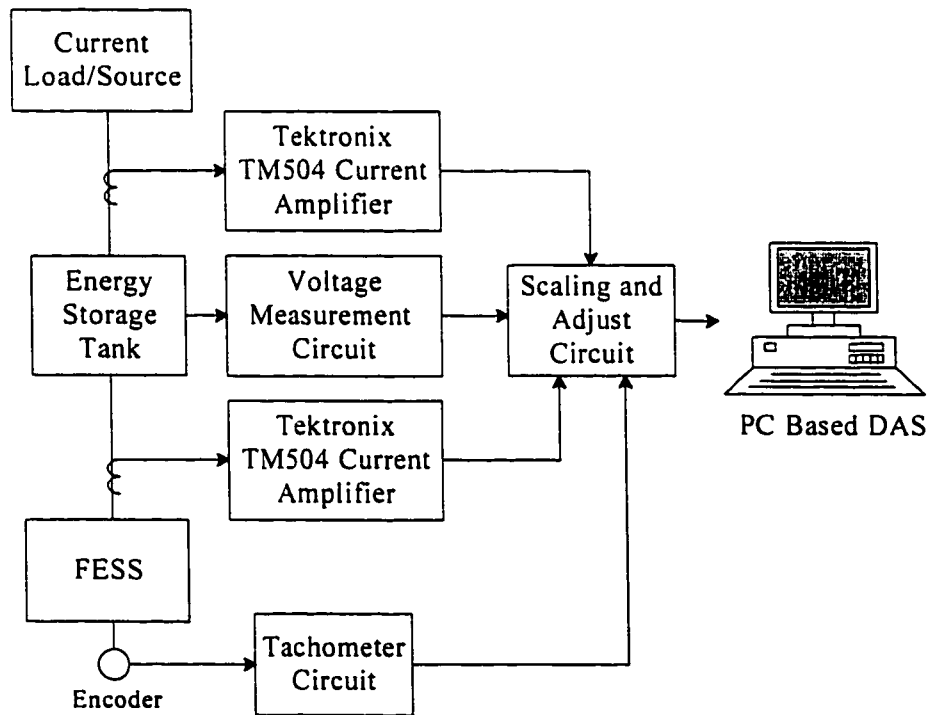


Figure 3.7 Data measurement components

be interfaced to a four channel PC-based Data Acquisition System (DAS). The PC-based DAS simultaneously records the measured signals in real time to allow for post-test data processing.

3.3.3 Combined Laboratory Test Setup for Energy Transfer Testing

The overall test setup for the energy transfer testing of the FESS is constructed by combining the dedicated function blocks displayed in Figures 3.1, 3.5, 3.6, and 3.7. The combined block diagram for the laboratory test setup is shown in Figure 3.8. A mode select switch provides rapid re-configuration of the testing mode. The laboratory dc power supply is connected directly to the energy storage tank during the initial charging of the FESS. The dc supply and the VSI counter preset are adjusted to a level that produces the desired steady state PMSM operation.

Electric vehicle braking mode tests are performed by switching the mode select

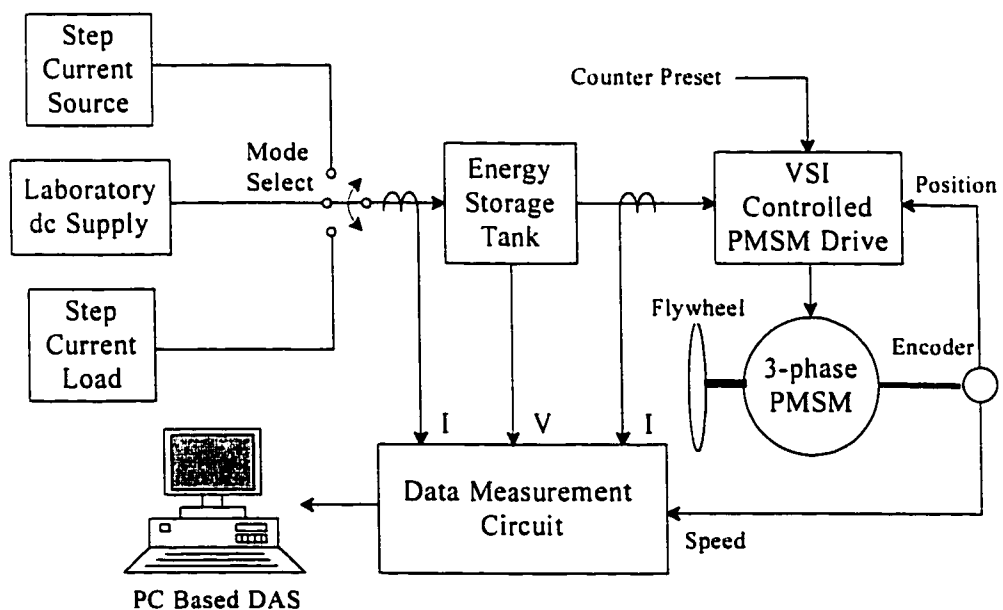


Figure 3.8 Laboratory test setup block diagram

switch to the step source circuit once steady state PMSM/flywheel operation has been obtained. A step source current charges the energy storage tank, causing the tank voltage to rise. The increase in tank voltage produces an increase in the step current waveforms to the PMSM, and the PMSM/flywheel combination will increase in operating speed. The response of the PMSM to an increase in storage tank voltage is adjusted through the simplified current vector control described in Section 3.2.2. Desired PMSM response is obtained through experimental manipulation of the counter preset value for the VSI.

Acceleration mode tests are conducted by switching the mode select switch to the step load circuit after reaching steady state PMSM/flywheel operation. The step load current discharges the energy storage tank and causes the tank voltage to fall. Generation of electricity occurs naturally from the PMSM through VSI antiparallel diodes. Desired generation response is obtained through experimental manipulation of the voltage level on the energy storage tank with respect to the back-EMF level of the PMSM at the operating speed of the FESS. Figure 3.9 shows a photograph of the actual laboratory setup used to determine the energy transfer capabilities of the prototype FESS.

3.4 PEAK POWER TRANSFER TESTS

3.4.1 Flywheel Rundown Loss Testing

Flywheel rundown testing is conducted to estimate some of the energy losses associated with the PMSM/flywheel combination. The dual element 0.0889 kg·m² flywheel, shown in Figure 3.9, is streamlined with cardboard and epoxy to reduce windage losses. The FESS is charged to 7500 rpm, representing a net stored energy of 7.6 Wh, and is

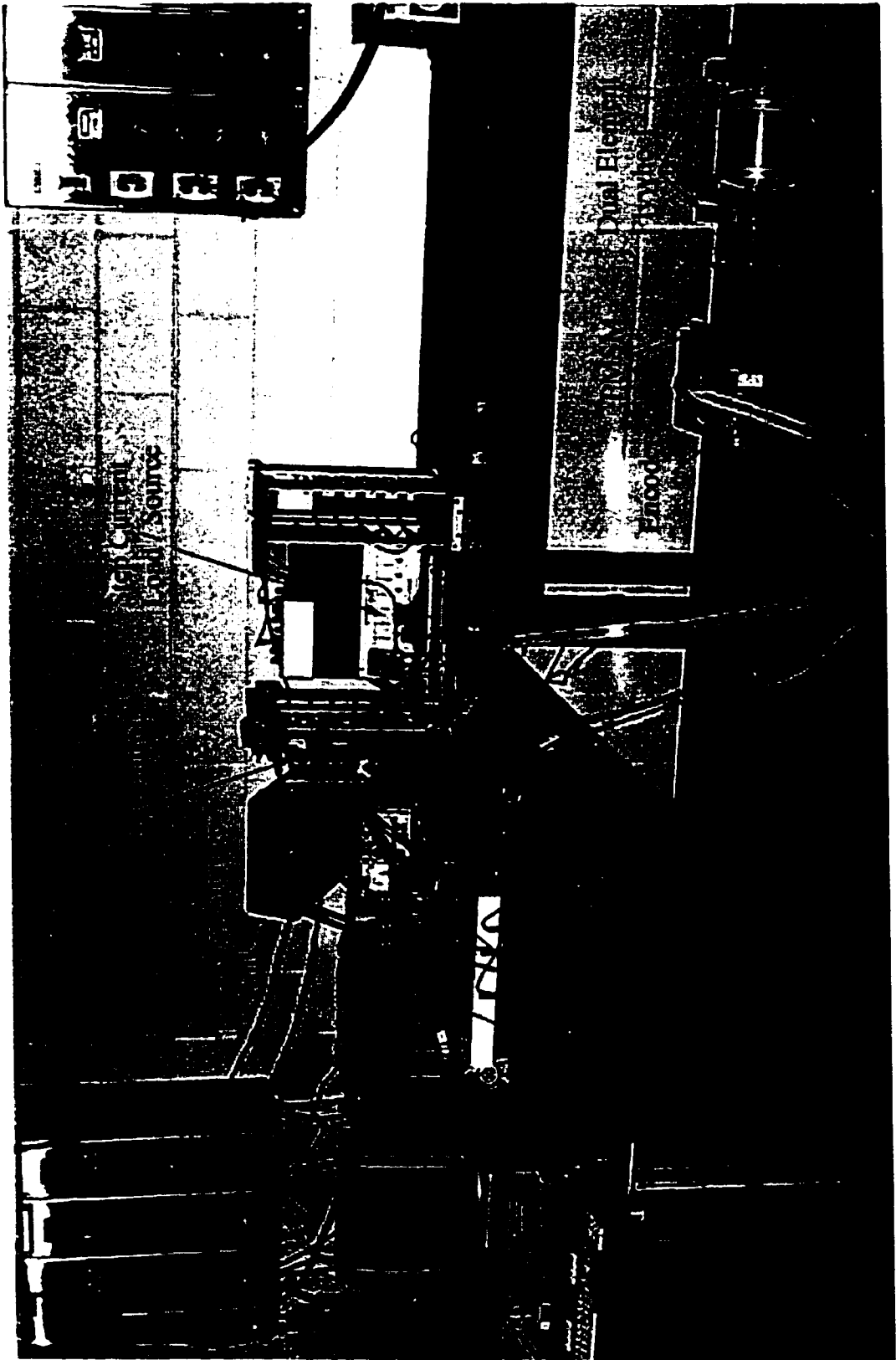


Figure 3.9 Laboratory test setup

allowed to rotate freely with the VSI drive disabled and the energy storage tank disconnected. A speed measurement is recorded every 15 seconds and the resulting speed and stored energy decay profile is illustrated in Figure 3.10.

A fourth order polynomial fit is performed on the measured data. The resulting expression, shown by (3.1), allows the FESS speed to be calculated as a function of time to within 0.6% over the 3500 to 7500 rpm operating range. The instantaneous power lost during the flywheel rundown test is determined through the use of (3.2). Power losses during the flywheel rundown test consist of bearing losses, windage losses, and the eddy current and hysteresis losses created in the PMSM stator by the rotating magnetic field on the rotor. Comparison of speed and power values calculated in (3.1) and (3.2) yields the data for Figure 3.11. The power loss, shown in (3.3), is derived from (3.2) and can be

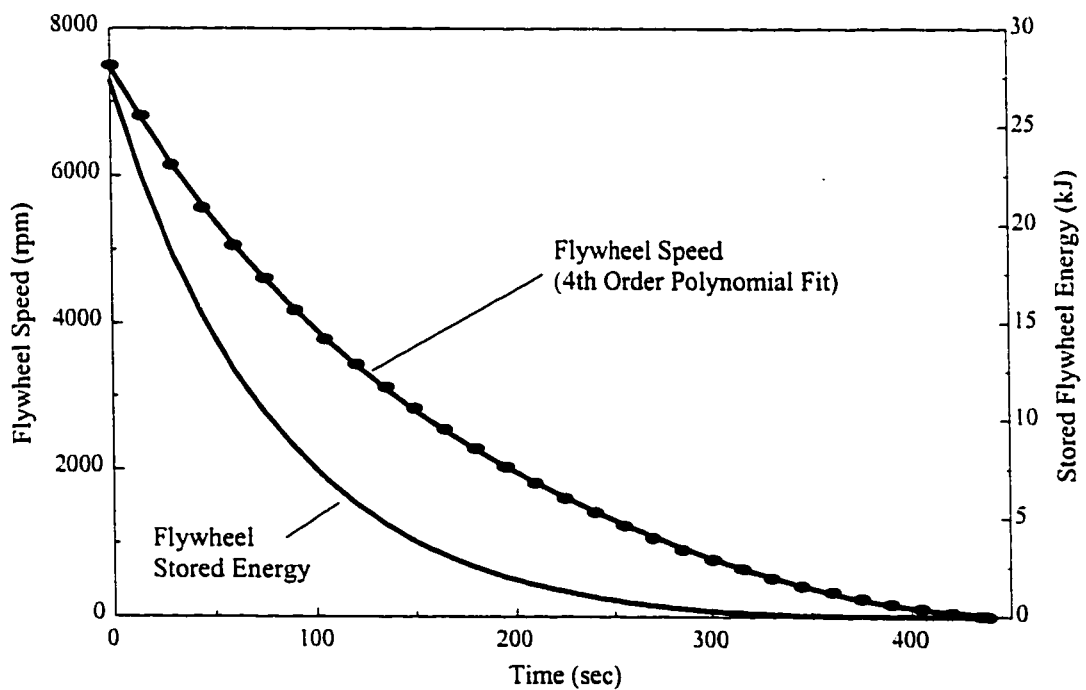


Figure 3.10 Flywheel rundown speed decay profile

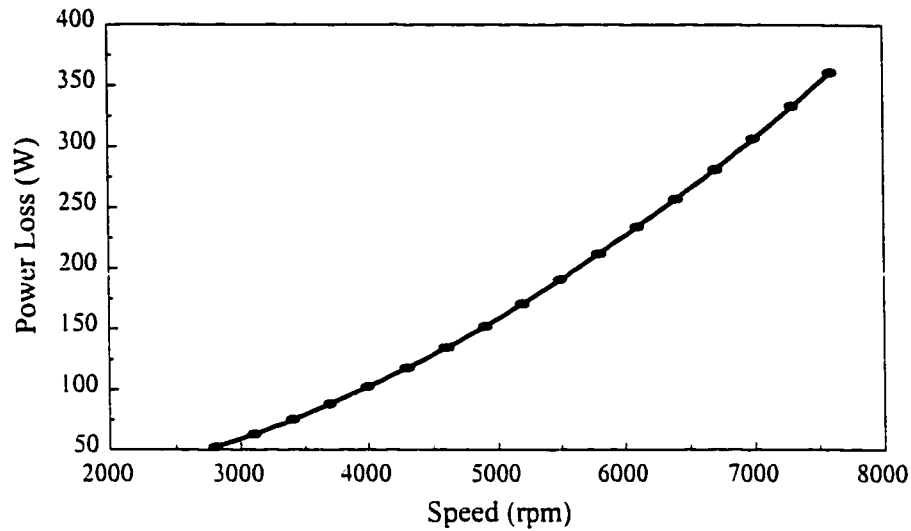


Figure 3.11 FESS power loss as a function of speed

expressed as a second order polynomial with a worst case accuracy of 1%. Expression (3.3) provides a means to calculate the instantaneous power loss as a function of speed, thereby providing a means to estimate the FESS losses during the peak power transfer tests.

$$n_F(t) = 2.33E-07 \cdot t^4 - 0.00028 \cdot t^3 + 0.148 \cdot t^2 - 47.9 \cdot t + 7481 \quad (3.1)$$

$$P_{FL} = I \cdot n_F(t) \cdot d(n_F(t))/dt \quad (3.2)$$

$$P_{FL}(n_F) = 6.189 \cdot n_{Fk}^2 - 0.09307 \cdot n_{Fk} + 3.8765 \quad (3.3)$$

where: n_F = flywheel speed (rpm)
 t = time (s)
 n_{Fk} = flywheel speed (krpm)
 P_{FL} = FESS power loss (W)
 I = total flywheel inertia (0.0889 kg·m²)

3.4.2 Acceleration Mode Peak Power Transfer Tests

Acceleration mode testing is performed according to the procedure described in Section 3.3.3, using the test setup in Figures 3.8 and 3.9. The testing is conducted in accordance with the prescribed operation of the proposed FESS in Figure 1.2 and Section 1.3.

An artificial dc bus voltage of 55V is chosen to simulate the buck-mode operation of the bidirectional chopper. The FESS is pre-charged to approximately 7500 rpm and the energy storage tank voltage is set to 100 V. The 100 V setting is chosen with the knowledge that the line-to-line peak back-EMF voltage of the PMSM is close to 100 V at 7500 rpm. A 100 V tank setting produces no resonant surge at the onset of PMSM generation, as the PMSM does not begin generation until the tank voltage falls below the back-EMF level.

The acceleration mode testing is conducted for various step load current demands on the energy storage tank. Figures 3.12 to 3.15 show the averaged values for the step load current, the storage tank input current from the PMSM, the storage tank voltage, and the flywheel speed for the duration of the 10 A step load demand. Figure 3.12 shows that a 10 A, 110 ms rise time, step load demand is applied at 2.4 seconds of the recorded data. The energy storage tank voltage immediately falls from 100 V and reaches 67 V in 420 ms (Figure 3.14). Figure 3.13 shows that the PMSM begins to generate current through its VSI and into the tank as soon as the tank voltage falls below 100 V. The resonant surge current, observed in [11, p.73] during the 0.3 p.u. acceleration mode test, is absent due to the matching of the energy tank voltage to the PMSM back-EMF. Current supplied by the PMSM to the tank reaches the level of current drawn out of the tank in 420 ms. Once equilibrium is reached, the energy storage tank voltage falls gradually due to the decay in PMSM speed and hence back-EMF.

The storage tank voltage falls below 55 V at 11.3 seconds and the buck chopper to the load can no longer sustain a constant load current. The load current begins to decay with the energy storage tank voltage. Removal of the step load at 12.2 seconds causes the tank

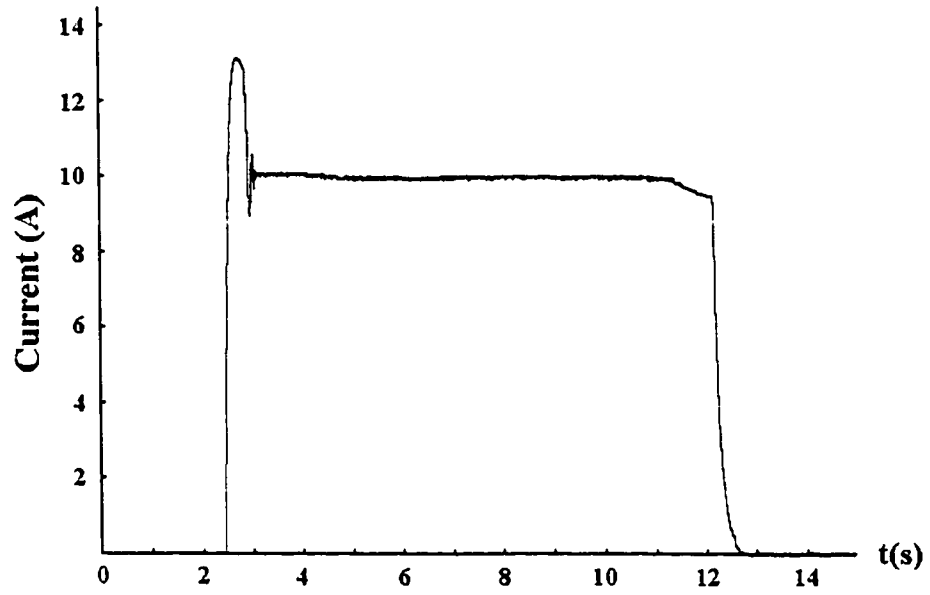


Figure 3.12 Step load current (10A test)

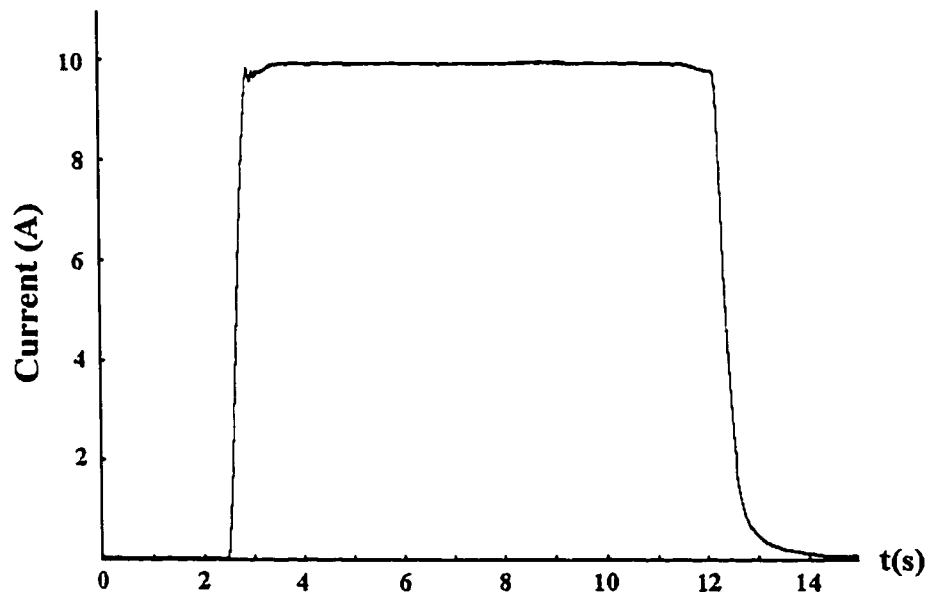


Figure 3.13 Storage tank input current from the PMSM (10A test)

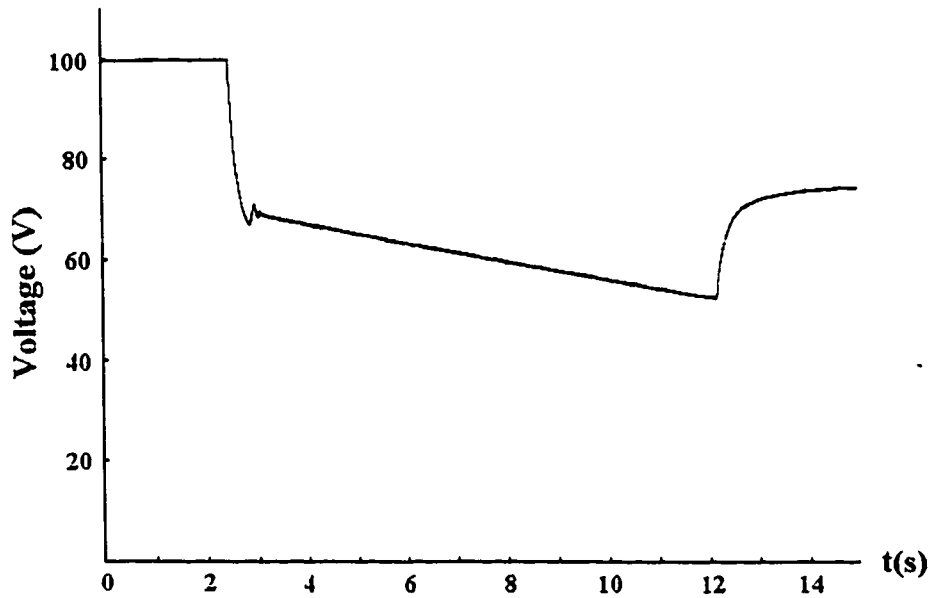


Figure 3.14 Energy storage tank voltage (10A test)

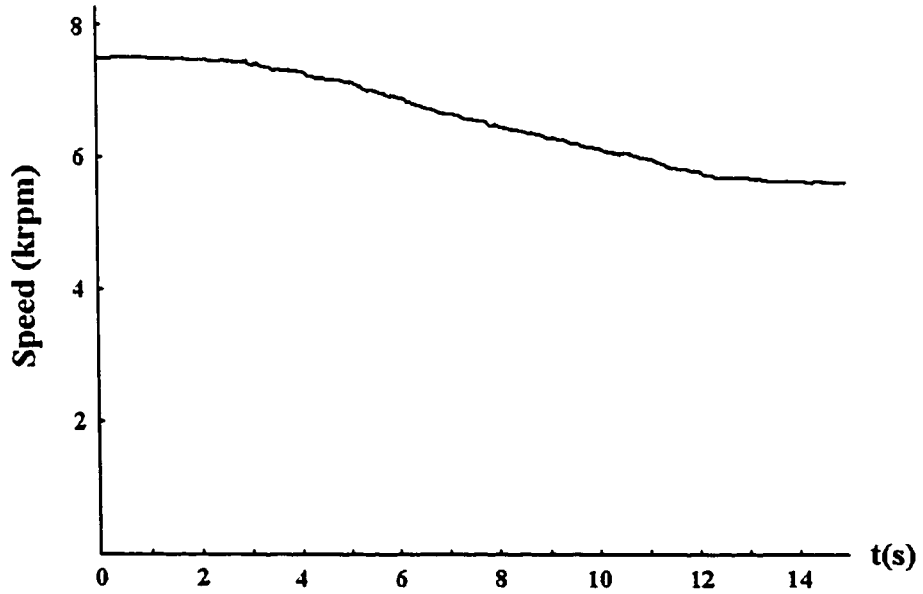


Figure 3.15 Flywheel speed (10A test)

voltage to rise to the point where the voltage on the tank matches the back-EMF voltage of the PMSM. The storage tank input current from the PMSM does not fall to zero until equilibrium is reached at 76 V with an approximate flywheel speed of 5700 rpm.

Extracted flywheel energy is determined through an examination of the drop in flywheel speed over the duration of the test. Figure 3.15 shows that the flywheel speed falls from 7460 to 5730 over the 9.8 second test, representing an extraction of 11.1 kJ or approximately 40% of the stored energy. The FESS power loss is estimated from a 0.5 second interval step approximation of Figure 3.15 and application of (3.3). A total FESS loss of 2720 J was estimated to occur during the 9.8 second test, representing approximately 24% of the extracted flywheel energy.

A 15 A step load demand test is used to investigate the effects of higher energy demands on the FESS. Figure 3.16 shows a 15 A average current, 250 ms rise time, step load demand that is extracted from the energy storage tank. The PMSM fully responds to the step load current in 440 ms, as shown by the average storage tank input current in Figure 3.17 and the average storage tank voltage in Figure 3.18. The storage tank voltage falls from 100 to 59 V during the initial 440 ms response time. A 15 A load current is maintained for only a few seconds as the delayed response from the PMSM allows the tank energy to deplete to a level which is close to the cutoff level for the buck chopper.

The flywheel speed falls from 7500 to 5240 rpm over the 11.2 second duration of the 15 A step load test. Figure 3.19 shows the flywheel speed decay resulting from an extraction of 14 kJ, or approximately 50% of the stored flywheel energy. Power loss in the FESS is estimated in the same manner as for the 10 A step load test. A total FESS power

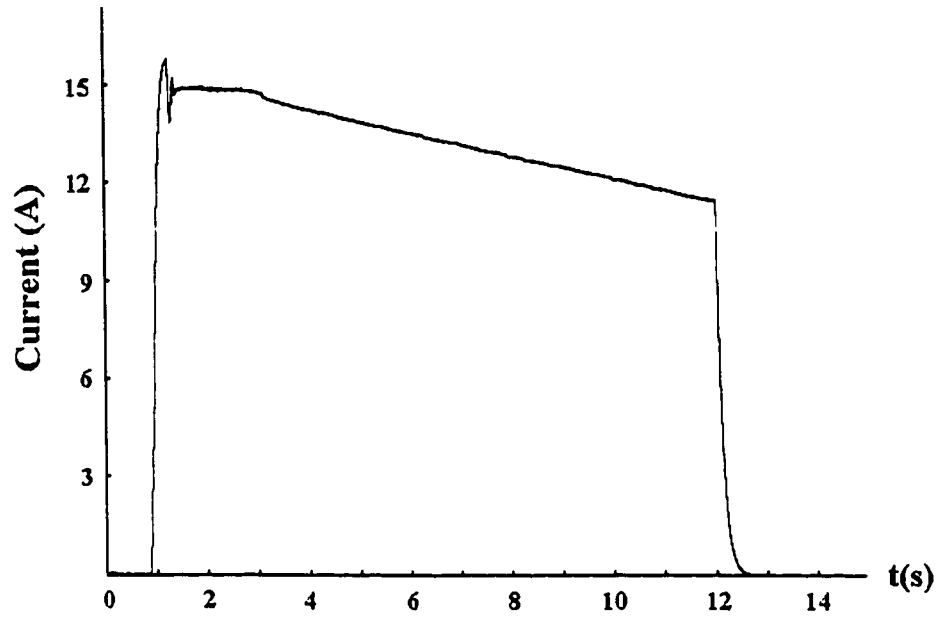


Figure 3.16 Step load current (15A test)

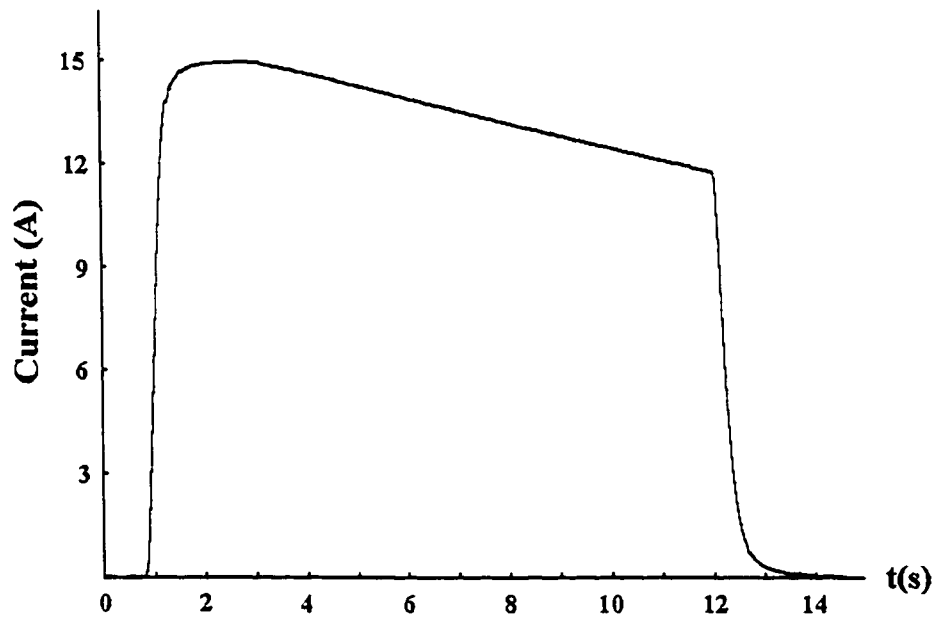


Figure 3.17 Storage tank input current from the PMSM (15A test)

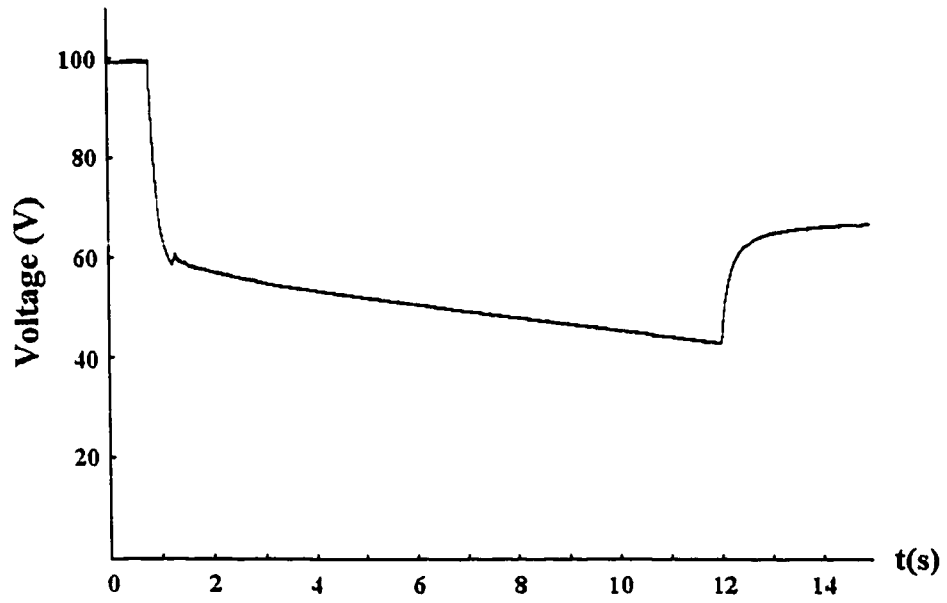


Figure 3.18 Energy storage tank voltage (15A test)

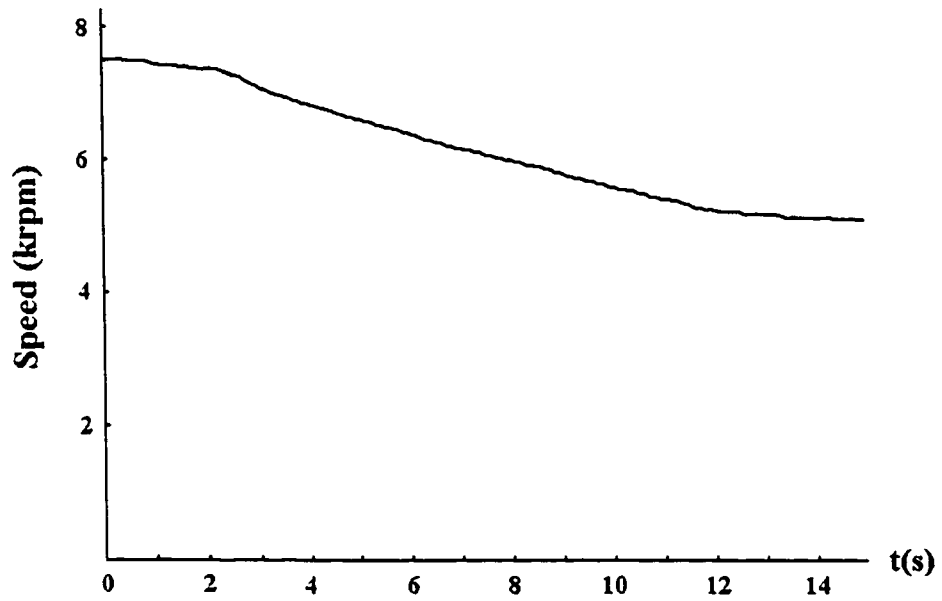


Figure 3.19 Flywheel speed (15A test)

loss of 2836 J was estimated to occur during the 11.2 second test, representing approximately 20% of the extracted flywheel energy.

3.4.3 Design Implications of the Acceleration Mode Peak Power Transfer Tests

The acceleration mode test results indicate the influence of the design variables that can be used to optimize the FESS. Energy storage tank sizing depends on the basic role that the energy storage tank is required to perform. The energy control strategy for the FESS, proposed in Section 1.3, specifies that the energy storage tank is operated at a voltage level that is always higher than the EV dc bus voltage. A high storage tank voltage corresponds to the high PMSM back-EMF obtained at high speeds. Figure 3.20 shows the simplified per-phase equivalent circuit of a lossless 3-phase PMSM operating in the generating mode [21]. The back-EMF phase amplitude E_{bo} is proportional to the rotational frequency ω_r as shown in (3.4).

$$E_{bo} = k_o \cdot \omega_r \quad (3.4)$$

where: k_o is the back-EMF constant (volts/krpm)

The instantaneous phase power converted from mechanical form ($P_{m\phi}$) into electrical form ($P_{e\phi}$) can be expressed by (3.5).

$$P_{e\phi} = E_{bo} \cdot I_o = P_{m\phi} = T_{e\phi} \cdot \omega_r \quad (3.5)$$

where: I_o is the phase current flowing out of the PMSM
 $T_{e\phi}$ is the instantaneous developed phase torque

Generated phase current (I_o) is calculated from the equivalent circuit as (3.6).

$$I_o = (E_{bo} - V_\phi) / X_s \quad (3.6)$$

where: V_ϕ is the phase terminal voltage
 X_s is the stator reactance

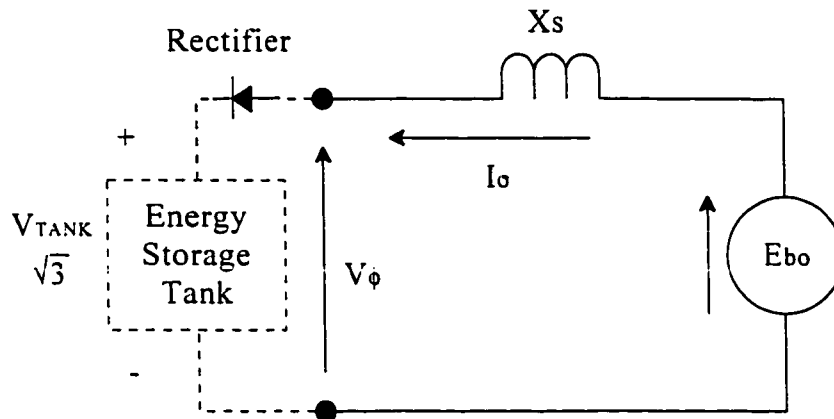


Figure 3.20 Simplified PMSM generation mode equivalent circuit

The expression in (3.6) indicates that the generation response of a PMSM is proportional to the difference between its back-EMF and its terminal voltage. Connection of the PMSM to the energy storage tank through the rectification diodes, as outlined in Figure 3.20, directly influences the rate of generation. Hence, the size of the energy storage tank determines the rate of change in the PMSM current generation response during the acceleration mode. A smaller energy storage tank will experience a faster tank voltage decay which will in turn produce a more rapid response from the PMSM. The rapid response of the PMSM must be limited to avoid damage from current and torque transients. The energy storage tank size can be reduced to a minimum level, to act only as a transient energy buffer between the EV dc bus and the PMSM, if the peak power ratings of the PMSM used in the FESS matches or exceeds the power demands on the FESS.

A large energy storage tank can be used to enhance the peak power transfer capabilities of a FESS. The results of the 15A step load test show that the energy storage tank can be used to temporarily supply more peak power than the FESS is capable of. The electrolytic capacitor energy storage tank used in this investigation can supply 7.52 kW for

0.5 seconds when discharged from 300V to 100V. Comparison with the PMSM shows that the PMSM is rated only for a continuous 2.29 kW operation. A trade-off exists between the high burst power, low energy storage, capabilities of the electrolytic capacitor energy storage tank, and the medium to high power burst, medium energy storage capabilities of the FESS. Figures 3.14 and 3.18 indicate that the storage tank energy will recharge naturally through the PMSM to an equilibrium voltage, once the step load is removed. Hence, a storage tank/PMSM combination needs no extra control circuitry to provide repeatable peak power burst capabilities. An optimization of the acceleration mode must be conducted to match the FESS components to the maximum acceleration mode peak power levels. Such optimization will provide information on the energy storage tank and PMSM size required to provide the peak power demands specified by the EV driving cycle simulations.

3.4.4 Braking Mode Peak Power Transfer Tests

Electric vehicle braking mode testing is conducted according to the same procedures used for the acceleration mode testing, differing only in the requirement that a step current was applied to, rather than demanded from, the load side of the energy storage tank. The applied step current represents a simulated step increase in regenerative braking power from the EVs drive motors. Measurements are taken to investigate the ability of the flywheel/PMSM combination to accept a 3.6 A and 10 A tank input current step.

The PMSM is operated in its motoring mode to overcome the flywheel losses. Flywheel speed is maintained near 3900 rpm before application of the step current. An energy storage tank voltage of 50 V is set to represent the EV dc bus, and an artificial

maximum storage tank voltage level was set near 85 V to demonstrate the implementation of a maximum allowable storage tank energy. The counter preset value in Figure 3.8 is determined through trial and error observations of the PMSM response to a storage tank voltage increase. A preset value of 1111 1010 0000 is chosen, representing a 27° phase voltage electrical switching angle advance, and corresponding current vector advance, with respect to the back-EMF fundamental voltage. The desired preset value is found to provide the most rapid PMSM response to storage tank voltage changes while also providing near 4000 rpm operation at 50 V.

Figures 3.21 to 3.24 show the averaged values for the step input current to the energy storage tank, the storage tank output current to the PMSM, the storage tank voltage, and the flywheel speed for the duration of the 3.6 A step current source. Figure 3.21 shows that the 3.6 A, 59 ms rise time, step current source is applied to the storage tank after 4 seconds of data recording. The voltage on the energy storage tank rises to 60 V before the VSI controlled PMSM fully compensates for the tank input current. The current response into the PMSM matches the storage tank step input current in 196 ms. Motoring response current into the PMSM and the storage tank voltage swing resulting from the application of the step load are shown in Figures 3.21 and 3.22 respectively.

The energy storage tank voltage initially decays from its peak response value of 60 V as the simplified VSI control overcompensates for the step input current. An increase in the speed of the PMSM/flywheel combination causes a corresponding increase in the PMSM back-EMF, thereby creating a gradual rise in the equilibrium storage tank voltage. Continuous adjustment of the counter preset to produce a phase advance angle greater than 27°

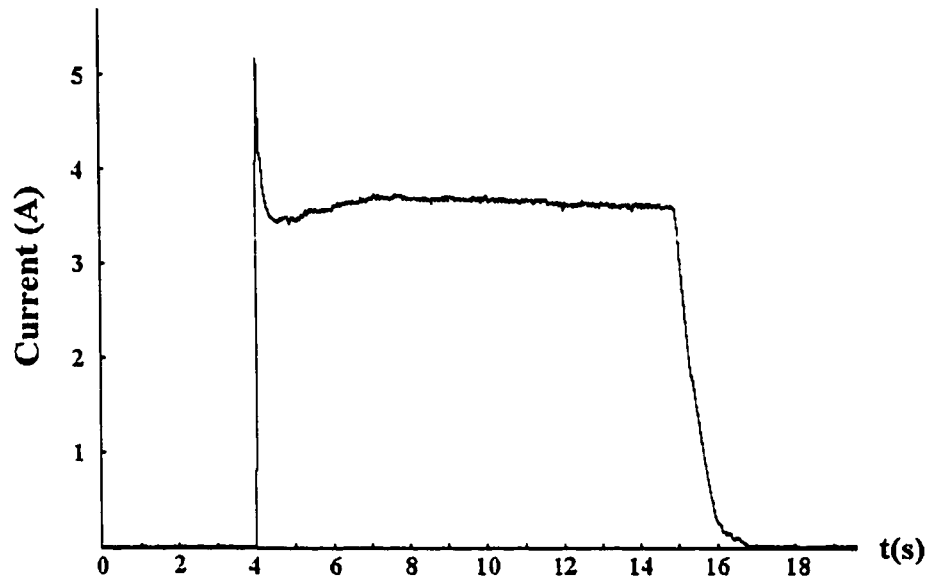


Figure 3.21 Storage tank step input current (3.6 A test)

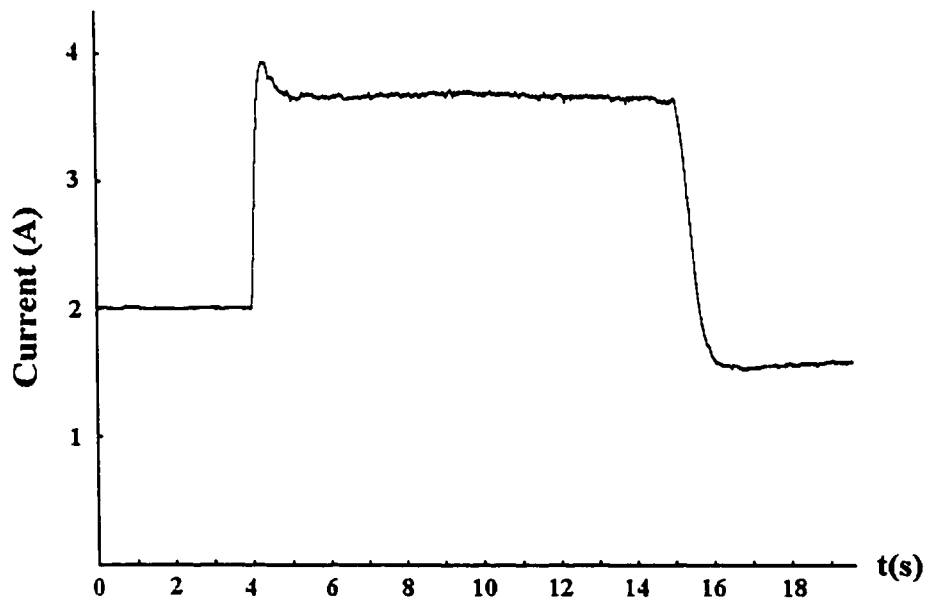


Figure 3.22 Storage tank output current to the PMSM (3.6 A test)

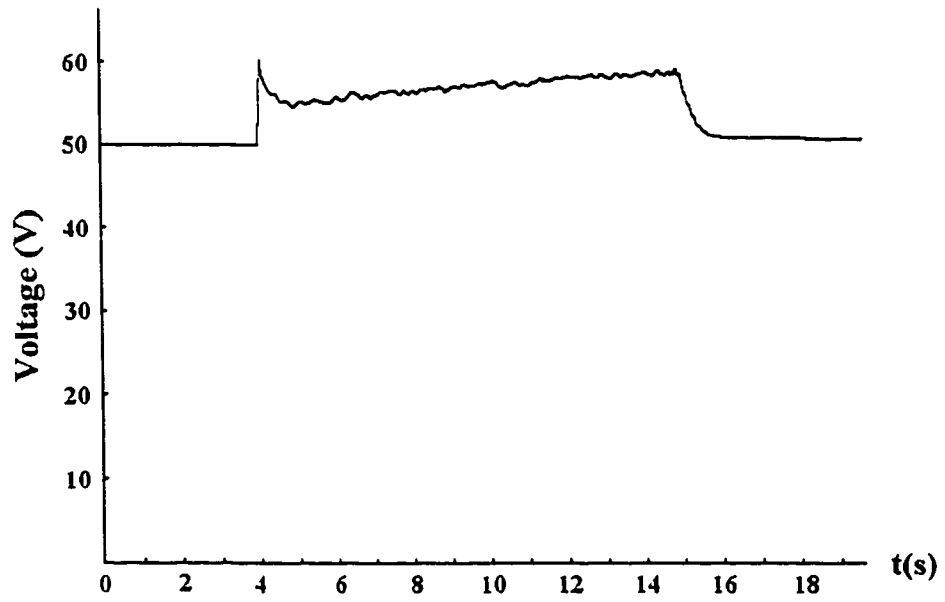


Figure 3.23 Energy storage tank voltage (3.6 A test)

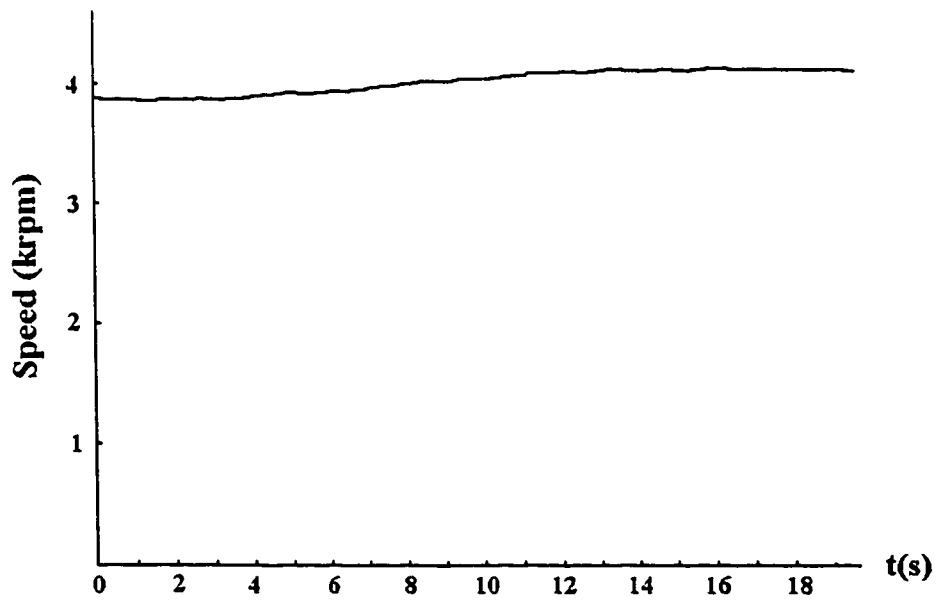


Figure 3.24 Flywheel speed (3.6 A test)

will provide a means to counteract the storage tank voltage rise. Counter preset adjustments are not performed during these tests to preserve the simplicity of this investigation. The step current is turned off after 10.9 seconds and the storage tank voltage falls to its minimum allowed level. Current to the PMSM decays as the voltage to the VSI is no longer high enough to supply current to the PMSM.

Stored flywheel energy is increased by 1.1 kJ, or 16 %, as the flywheel speed rises from 3840 to 4130 rpm during the test. Figure 3.24 shows the increase in flywheel speed over the 10.9 seconds of the step input current. The FESS power loss is estimated from a 0.5 second interval step approximation of Figure 3.24 and application of (3.3). A total FESS loss of 1126 J is estimated to occur during the test, representing approximately 100% of the net increase in stored flywheel energy. Hence, less than 50% of the step input current energy remains as kinetic flywheel energy at the end of the test.

A 10 A step input current test is conducted to investigate the FESS response to a higher regenerative braking power. Figure 3.25 shows that the input current to the storage tank reaches 10 A in approximately 714 ms. The VSI controlled PMSM responds to this step current and matches the tank input current after 1.22 seconds, as shown in Figure 3.26. The delay in the response from the PMSM causes the storage tank voltage to rise to 83V. Chopper control limits the tank input current so that the maximum allowable tank energy is not exceeded. Figure 3.27 shows the controller limited storage tank voltage over the 12.2 second test.

The experimental results of the 10 A step input current test demonstrate that for this experimental configuration of storage tank size, maximum tank voltage level, and fly-

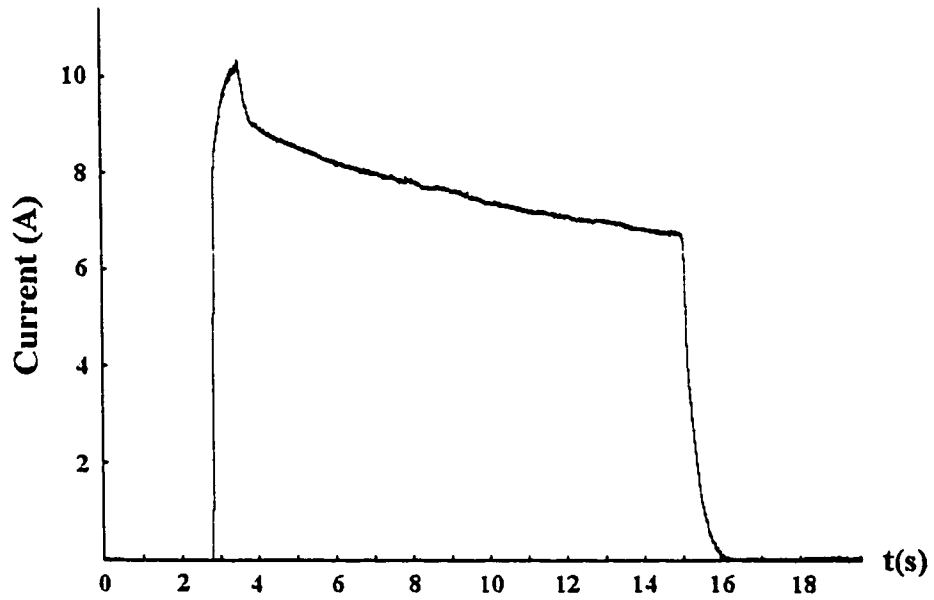


Figure 3.25 Storage tank step input current (10A test)

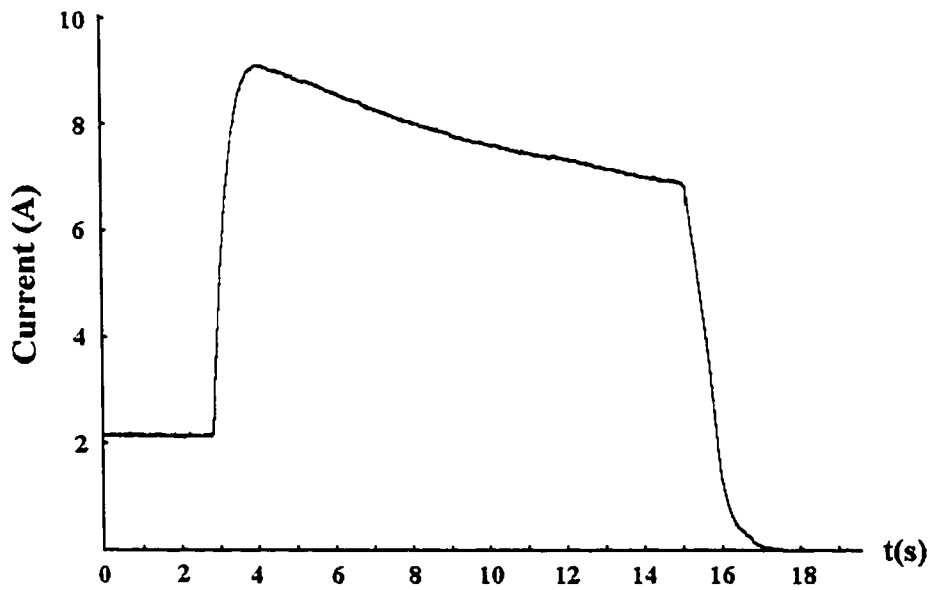


Figure 3.26 Storage tank output current to the PMSM (10A test)



Figure 3.27 Energy storage tank voltage (10A test)



Figure 3.28 Flywheel speed (10A test)

wheel/PMSM size, a 10 A step input braking current to the energy storage tank is not sustainable. The results also indicate that the FESS will sustain as much current as possible and the storage tank energy is automatically reduced to its pre-step input current value, once the input current is removed.

Measurement of the speed response in Figure 3.28 shows that the flywheel speed rises from 3870 to 4830 rpm during the 12.2 second test. Stored flywheel energy increases by 4 kJ, or to approximately 156% of its initial value. The FESS power loss is estimated from a 0.5 second interval step approximation of Figure 3.28 and application of (3.3). A total FESS loss of 1517 J is estimated to occur during the test, indicating that approximately 73% of the step input current energy remains as kinetic flywheel energy at the end of the test.

3.4.5 Design Implications of the Braking Mode Peak Power Transfer Tests

The braking mode experimental results indicate that a PMSM/flywheel combination can be used to accept a rapid increase in EV braking power. Examination of the tank output current to the PMSM shows that the response of the VSI controlled PMSM is slower than what was found during the acceleration mode tests. The difference in the PMSM responses is due to the fact that optimal regeneration occurs naturally in the acceleration mode FESS operation, while the braking mode operation requires VSI control of the phase current inputs to the PMSM. A possible solution to the slower braking mode response is to increase the maximum allowable storage tank voltage to 100 V, thereby allowing the FESS to sustain a 10 A step input current. Increasing the storage tank capacitance will also allow

the energy storage tank to temporarily store more energy until the PMSM can convert the energy into its kinetic form. Energy storage tank sizing can be used to compensate for a poor PMSM response at the expense of a larger energy storage tank.

3.4.6 Test Results Implications for Further Work

Experimental results show that flywheel losses account for more than 20% of the extracted flywheel energy, and as high as 50% of the recovered flywheel energy. High losses associated with the conventional bearing, non-vacuum housing operation of the FESS must be significantly reduced for a practical unit. The use of magnetic bearings, or a bearingless PMSM, with a vacuum housed flywheel will reduce the high losses experienced in this investigation. An investigation into the use of a bearingless PMSM coupled to a vacuum housed flywheel is recommended for further investigation.

The acceleration mode results provide the necessary information for the design of an efficient method to naturally extract FESS energy. The braking mode test results indicate that a more rapid method must be developed for charging energy into the FESS. Continuous control of the counter preset value in Figure 3.8 will allow for continuous current control. Microprocessor implementation of the counter preset value control and experimental adjustment of the preset value with respect to the PMSM speed will produce an improved FESS response time. The proposed additions to the simplified VSI controlled PMSM drive represent a non-parametric approach to control of the PMSM. The test results show that such non-parametric control will work. A simple, small, and inexpensive drive can be constructed using this approach and may provide satisfactory operation of the FESS.

Construction of such a drive is recommended for further work.

Torque control through phase current vector manipulation will allow for fixed dc bus voltage PMSM operation at speeds above those obtainable from the proposed simplified VSI controller. Optimization of the proposed FESS cannot be conducted without an investigation into the improvement of the torque generation capabilities of the PMSM drive. High performance torque control and sinusoidal phase current waveform generation are required to fully utilize the potential of the PMSM for high speed operation [21]. Six step switching of the current waveforms produces a high harmonic content in the PMSM phase current waveforms. The current harmonics reduce the efficiency of the PMSM during motoring operation. Sinusoidal current waveform excitation will improve motoring efficiency, thereby improving the rate of energy conversion from the energy storage tank to the fly-wheel.

The remainder of this thesis is based on the work conducted to develop a high performance, current vector controlled, high efficiency sinusoidal phase current, high speed PMSM drive prototype. The developed drive is intended to operate in the proposed FESS to produce fast braking mode response times, and to be controlled through a microprocessor implemented torque control algorithm. It is this author's desire to implement the high performance PMSM drive so that it can be evaluated against the simplified VSI drive proposed in this chapter.

CHAPTER 4

ELECTRICAL NOISE AND SHIELDING

4.1 IMPORTANCE OF UNDERSTANDING ELECTRICAL NOISE

The implementation of a high speed, microprocessor controlled, sinusoidal Current Controlled Voltage Source Inverter (CCVSI) drive cannot proceed without an understanding of the proper techniques to construct electronic circuitry for an electrical noisy environment. Previous work in [11, p.32] proposed an error-triangle Pulse Width Modulation (PWM) method to produce sinusoidal current waveshapes through the high frequency switching operation of a VSI. High frequency VSI operation produces a high rate of change in voltage (dv/dt) on the switched circuits. Parasitic capacitance and inductance coupling produces charge/discharge impulse currents that flow into the dc link of the proposed FESS and cause Electromagnetic Interference (EMI) problems throughout the electronic control circuitry.

The extents of the noise problems are often not noticeable in simplified VSI control systems such as the one implemented in Chapter 3. Simplified VSI operation requires six voltage switches per electrical cycle, one marker signal per revolution, and six position counts per electrical cycle. A maximum switching and position feedback signal frequency of 1.6 kHz is produced at 8000 rpm, for the 4 pole PMSM used in the Chapter 3 investigation. Noise problems are present with the simplified VSI but do not pose a serious problem

as the position feedback signal is synchronized with the voltage switching waveform. The voltage transient (dv/dt) experienced by a VSI switching action can produce EMI only after the desired logic action has been performed. A 60 degrees electrical angle spacing between the switching actions provides enough time for the voltage transients to decay, thereby avoiding the problem of EMI with the logic signals of the next switching action.

An error-triangle PWM strategy in the proposed CCVSI requires VSI switching at fixed rate between 10 and 20 kHz. The high frequency switching is not synchronized with the position signals from the PMSM, which are required to provide a resolution of several electrical degrees. The problems of EMI occur when the noise generated by the 10 kHz or higher switched voltage interacts in a non-synchronous manner with the required 32 kHz position encoder signal and the electronics associated with such high resolution current vector control. Position encoder signals become distorted and false triggering occurs on noise induced logic levels. Figure 4.1 shows the influence of EMI on the marker pulse train and the occurrence of a false marker trigger. The effect of a false marker trigger on the

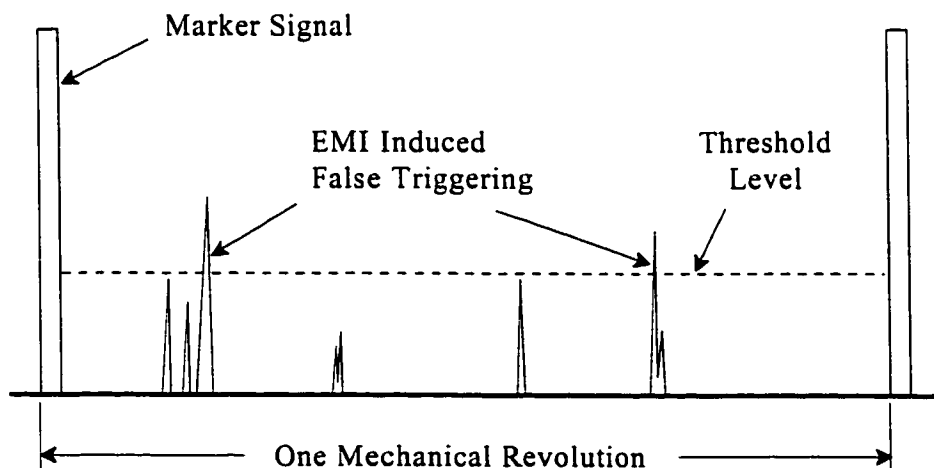


Figure 4.1 False marker signal triggering

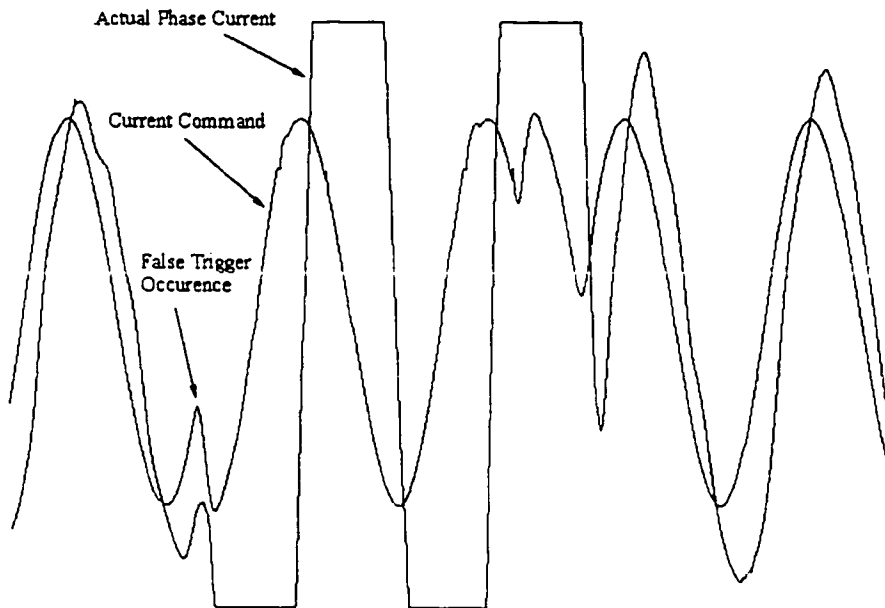


Figure 4.2 False triggering effects on waveform generation

sinusoidal current waveform generation was captured and is shown in Figure 4.2. The false trigger causes a discontinuity in the phase current waveforms for at least one cycle until the actual marker signal can correct the phase current commands.

Commutation signals to the CCVSI are also susceptible to EMI. Shoot through faults occur when a false triggering signal is applied to one side of an inverter leg while the other side is on. The resulting short circuit across the dc link can destroy VSI components. Careful consideration must be made to reduce the effects of EMI before such expensive damage occurs.

4.2 CLASSIFICATION OF ELECTRICAL NOISE

Electrical noise in an inverter can take on several forms. Classification of the EMI must be performed before EMI protection and suppression techniques can be investigated.

The four major classifications of EMI will now be discussed.

4.2.1 Conductively Coupled Noise

Conductors that run through noisy environments pick up noise and conduct it to other circuits. The conducted noise causes interference in the victim circuit. An example of conductively coupled noise is the crackling sound heard on a radio when a vacuum cleaner is operating on the same power supply line. Conductive noise most commonly enters a circuit through the power supply leads.

4.2.2 Noise Coupling Through a Common Impedance

Two circuits connected to ground through a common impedance will influence one another. Figure 4.3 shows the connection of two circuits through a common ground [22, p.22]. Circuit 1 sees its ground potential modulated by ground current 2 flowing in the common ground impedance. Noise in circuit 2 is coupled to circuit 1 through the ground impedance and can influence the operation of circuit 1.

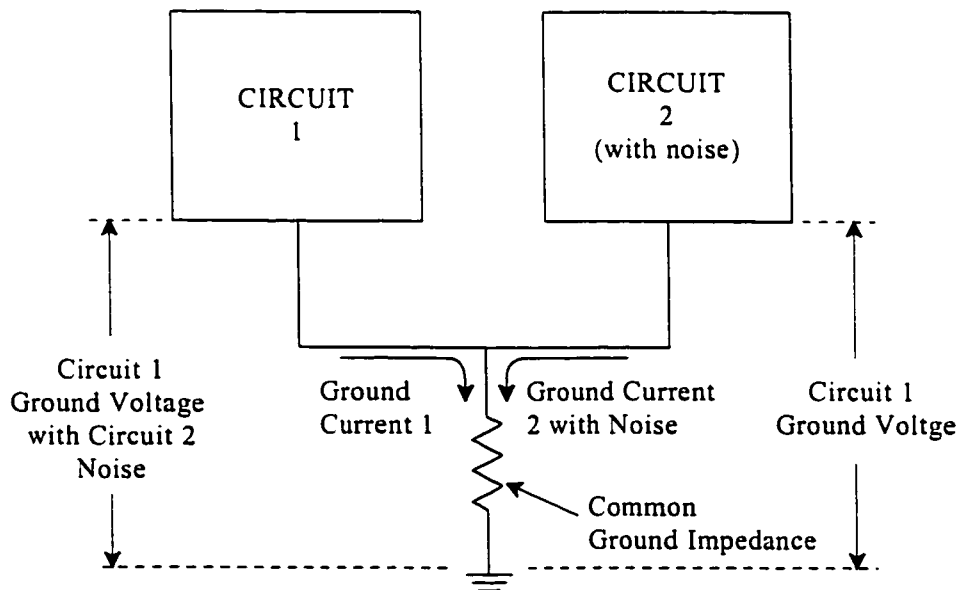


Figure 4.3 Common ground impedance noise coupling

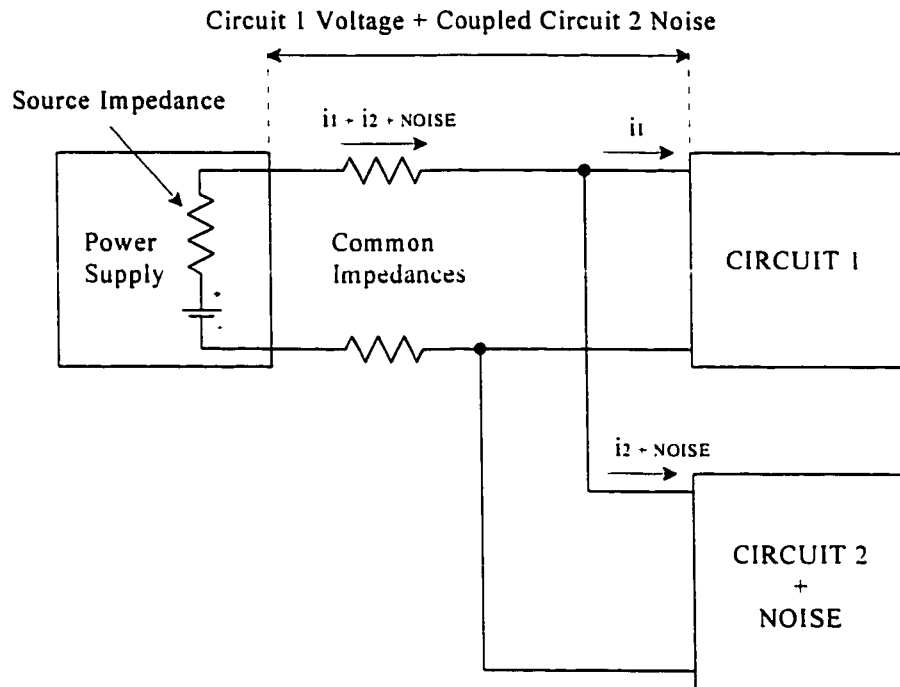


Figure 4.4 Common power supply noise coupling

Noise coupling through a common impedance does not have to occur through ground. Figure 4.4 shows how two circuits connected to a common power supply can be susceptible to noise coupling [22, p.23]. Both currents 1 and 2 see a common line impedance and internal power supply impedance. A change in the supply current drawn by circuit 2 will affect the voltage at the terminals of circuit 1. Noise in circuit 2 is thereby coupled to circuit 1 through the common impedances and directly influences the operation of circuit 1.

4.2.3 Electromagnetic Fields

The switching action of a VSI will impose a voltage rate of change of approximately $3 \text{ kV}/\mu\text{s}$ on the line to line voltages of the 3-phase PMSM. Each portion of the PMSM windings, feed cables to the PMSM, and semiconductor switches can act as a capacitor plate with respect to the grounded metal frame of the test setup. The charging and

discharging impulse currents created by the switching transients flow through the distributed capacitances along numerous paths to both ground and the dc link. All of the conducting elements radiate an electromagnetic field whenever charge is moved. The conducting elements also have stray inductance and resistive losses through which the complex ringing patterns in the EMI spectrum are created [23]. Electromagnetic interference effects can be categorized as being caused by either capacitive coupling, inductive coupling, or RF interference.

Capacitive Coupling

Capacitive coupling is commonly referred to as electric field coupling. It involves the passage of an interfering signal through mutual or stray capacitances. An example of capacitive coupling is the variation of an unstable oscillator frequency when a person's hand is moved over the oscillator circuit. Capacitive coupling also produces the crosstalk in multi-wire digital systems which can lead to spurious and difficult to trace logic errors.

The capacitive coupling between two current carrying conductors can be represented as shown in Figure 4.5 [22, p.30]. The voltage V_1 on conductor 1 represents the source of interference which is impressed on the receptor conductor 2. Capacitance between conductor 1 and ground has no effect on the noise coupling and is shown as C_{1G} . The resistance of the circuitry connected to conductor 2 is represented as R , while the stray capacitance between the two conductors is represented as C_{12} . Capacitance C_{2G} represents the capacitance between conductor 2 and ground, and the effect of the circuitry connected to conductor 2. The noise voltage on conductor 2 with respect to ground is determined through application of Kichhoff's voltage law and is expressed as shown in (4.1) [22, p.30].

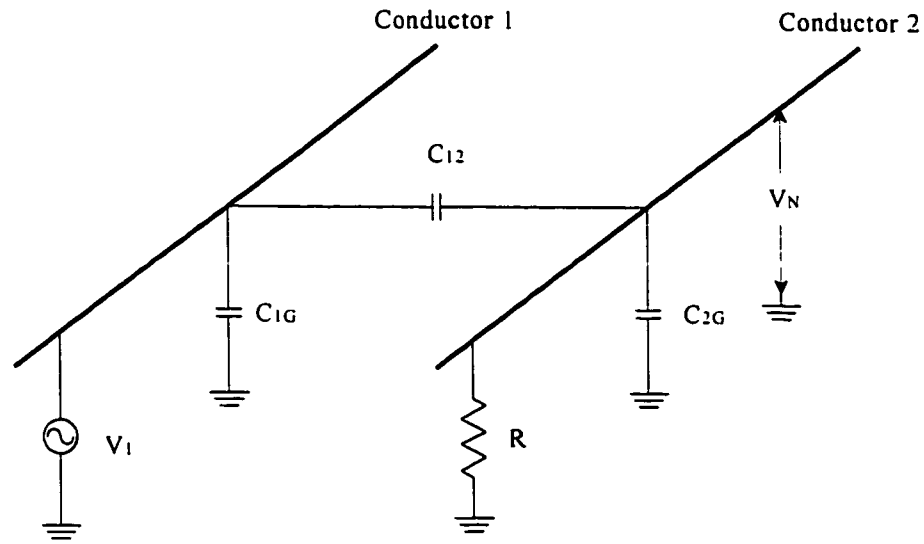


Figure 4.5 Representation of capacitive coupling between two conductors

$$V_N = V_1 \cdot \frac{j\omega R C_{12}}{j\omega R (C_{12} + C_{2G}) + 1} \quad (4.1)$$

In most practical cases, R is a lower impedance than the sum of C_{12} and C_{2G} . Hence, for $R \ll (j\omega (C_{12} + C_{2G}))^{-1}$ the equation (4.1) can be simplified to (4.2) [22, p.31].

$$V_N = j\omega R C_{12} V_1 \quad (4.2)$$

The noise voltage expression in (4.2) indicates that the noise induced on conductor 2 is directly proportional to the frequency ω of the noise, the resistance R of the receptor circuit, the capacitance between conductors 1 and 2, and the magnitude of the voltage V_1 . Equation (4.2) can be used to model capacitive coupling as a current generator of magnitude $j\omega C_{12} V_1$ connected between the receptor circuit and ground. Figure 4.6 shows the equivalent circuit for electric field (capacitive) coupling [22, p.40]. Resistances R_1 and R_2 are the termination impedances of the receptor conductor.

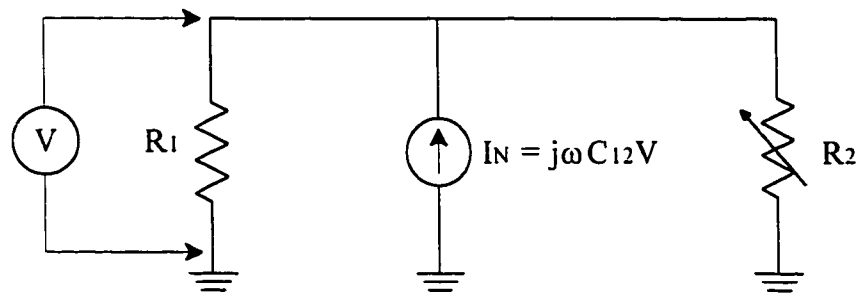


Figure 4.6 Equivalent circuit for electric field coupling in the receptor conductor

Inductive Coupling

Current in a closed circuit produces a magnetic flux ϕ which is proportional to the current. The constant of proportionality is expressed as the inductance L , which is used to define the magnetic flux according to (4.3) [22, p.37].

$$\phi = L \cdot I \quad (4.3)$$

Current in one circuit can produce a flux in a second circuit. The mutual inductance between two circuits is expressed in (4.4), where ϕ_{12} is the flux in circuit 2 due to current I_1 in circuit 1 [22, p.38].

$$M_{12} = \frac{\phi_{12}}{I_1} \quad (4.4)$$

The voltage induced in a closed loop of area A_{enc} due to a magnetic field of flux density B is determined from Lenz's and Faraday's laws and defined in (4.5) [22, p.38]. Vector notation

$$V_N = -j \frac{d}{dt} \int_A \bar{B} \cdot d\bar{A}_{enc} \quad (4.5)$$

is used for A_{enc} and B . Flux density B is assumed to be constant over the stationary loop area A_{enc} and to vary sinusoidally with time. The preceding assumptions allow (4.5) to be rewritten as (4.6), where ω is the frequency of the sinusoidally varying flux density B , V_N is the rms value of the induced voltage, and θ is the angle at which the magnetic field vector

cuts the closed loop [22, p.38].

$$V_N = j\omega B A_{enc} \cos\theta \quad (4.6)$$

The term $B A_{enc} \cos\theta$ in (4.6) is used to represent the total magnetic flux coupled to the receptor circuit 2. Equations (4.4) and (4.6) are combined into (4.7) to express the voltage induced in the receptor circuit as a function of the mutual inductance M_{12} between the two circuits [22, p.38].

$$V_N = j\omega M_{12} I_1 \quad (4.7)$$

Equation (4.7) shows that the inductive coupling between two circuits is directly proportional to the frequency of the sinusoidally varying flux density and the magnitude of the coupled flux. Figure 4.7 provides a physical representation of a magnetic field (inductive) coupling between two electrically isolated conductors [22, p.39]. Voltage V_1 produces a sinusoidal magnetomotive force that drives a sinusoidal current I_1 through the ter-

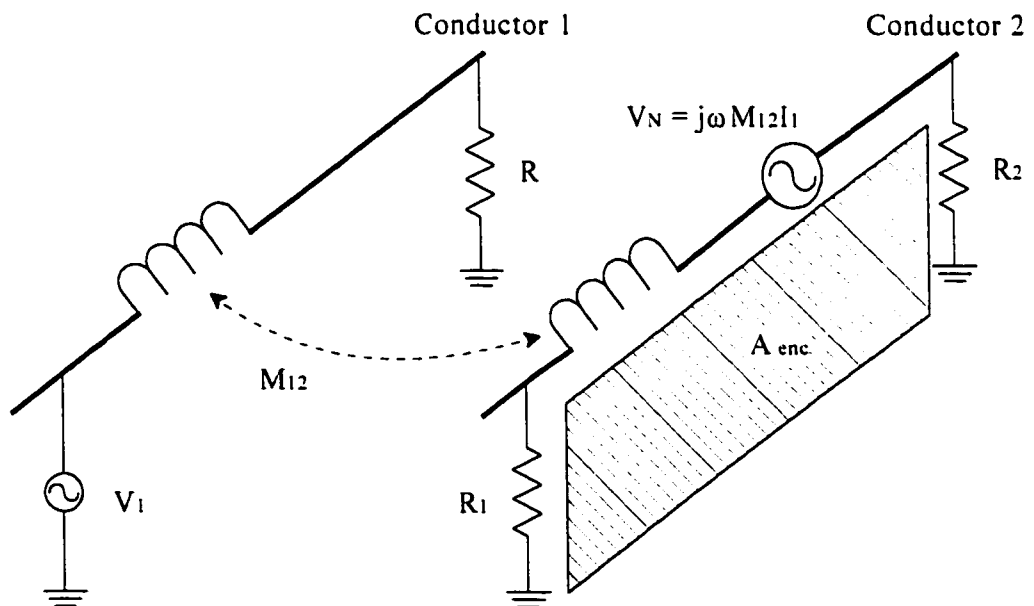


Figure 4.7 Representation of inductive coupling between two conductors

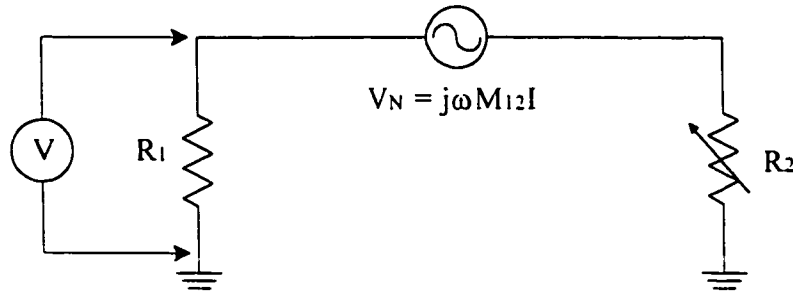


Figure 4.8 Equivalent circuit for magnetic field coupling

mination resistance R of conductor 1. The time varying current I_1 produces a time varying flux ϕ_{12} which is coupled to conductor 2 through the mutual inductance M_{12} . Flux ϕ_{12} produces a time varying magnetic field density vector B which cuts the area A_{enc} at an angle of θ and generates a noise voltage V_N . Conductor 2 is connected to a source impedance R_1 and load impedance R_2 . The equivalent circuit for magnetic field coupling is shown in Figure 4.8 [22, p.40].

RF Interference

Radio frequency (RF) interference is created by a combination of electric and magnetic fields through what is appropriately called electromagnetic coupling. A time varying electric field generates a time varying magnetic field, and vice-versa. The ratio of the electric E -field to the magnetic H -field amplitudes is 377Ω when far from the source. The near field, has a field ratio that is significantly different from 377Ω . A near field emission extends approximately $1/6$ of a wavelength from the source, or about 46 m for a 1 MHz field [24, p.6-10]. RF interference problems in inverter switching circuits, such as the circuit proposed for this test setup, are almost always caused by an EMI source in the near field.

A whip antenna has an E/H ratio in the near field higher than 377Ω , meaning that

it is mainly an E-field generator. A good example of a whip antenna is a wire wrap post, of which many examples are found in the laboratory test setup circuits constructed in this thesis. The interference from a whip antenna would be through electric field (capacitive) coupling. A loop antenna has a near field E/H ratio lower than 377Ω , meaning that it is mainly an H-field generator. Loop antennas are formed by any current loop. Interference from loop antennas is produced through magnetic field (inductive) coupling [24, p.6-10].

4.3 ELECTRICAL NOISE REDUCTION TECHNIQUES

4.3.1 Conductively Coupled Noise Reduction

Conductively coupled noise entering a circuit through the power supply leads can be reduced with the addition of decoupling capacitors. Decoupling capacitors across the power supply act as a nearby source of charge that can supply current spikes through a smaller line impedance. Decoupling capacitors also define a smaller loop area for the high frequency components of EMI, thereby reducing the EMI induced noise components on the otherwise long, larger loop area, power supply leads.

Two different kinds of decoupling capacitors should be used. Board decouplers, consisting of 10 to 100 μF electrolytic capacitors, should be placed at the point where the power supply enters the printed circuit or wire-wrap board [24, p.6-15]. Board decouplers are used to refresh the charge on the chip decouplers, which are what is used to actually supply and absorb the current spikes on the power supply lines. Chip decouplers usually consist of 0.1 to 1 μF ceramic capacitors that are connected across the power supply pins of an integrated circuit chip so as to minimize the loop area formed between the capacitor and

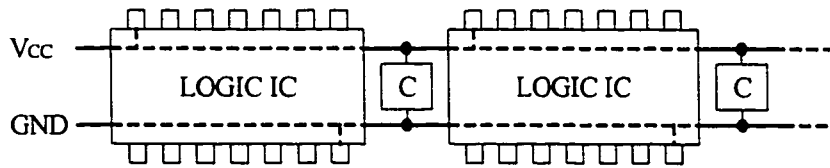


Figure 4.9 Chip decoupling capacitor placement

the chip. Figure 4.9 shows a suitable configuration for the placement of chip decoupling capacitors in a logic circuit [24, p.6-16].

4.3.2 Common Impedance Coupling Noise Reduction

A popular solution to the common impedance coupling problem in Figure 4.3 is to provide a separate 'earth' ground to each of the two circuits, thereby avoiding a common ground impedance. Figure 4.10 shows the effect of adding another 'earth' ground to the circuitry in Figure 4.3 [24, p.6-5].

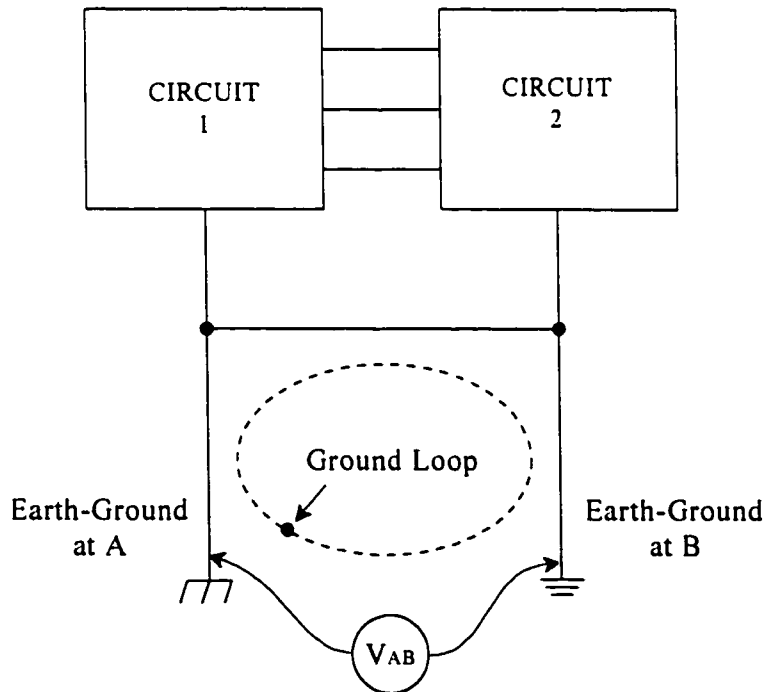


Figure 4.10 Creation of a ground loop

The addition of another ground in Figure 4.10 solves the problem of common impedance noise coupling and introduces the problem of a ground loop. Ground loops are created when multiple circuits are connected to an 'earth' ground that is not the same potential in all locations. A potential difference V_{AB} between the true 'earth' grounds A and B can drive several amperes of unwanted and unexpected current through the ground wire. The proper way to eliminate common impedance noise coupling through ground is to use one point as the ground connection and run multiple ground lines to the individual circuits that require ground. Ground connections are not allowed between circuits. Figure 4.11 shows the layout of the preferred ground connection which is often referred to as a 'parallel' or 'star' connection [24, p.6-13].

A parallel connection of ground wires eliminates ground impedance and ground loop problems at the expense of using a lot of wire. Parallel connection of the power supply lines in the same manner as the ground lines helps to reduce the common power supply

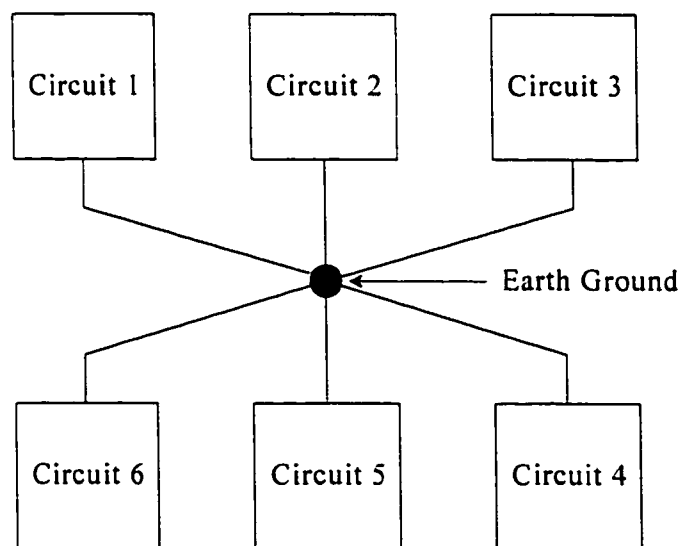


Figure 4.11 Preferred parallel ground connection

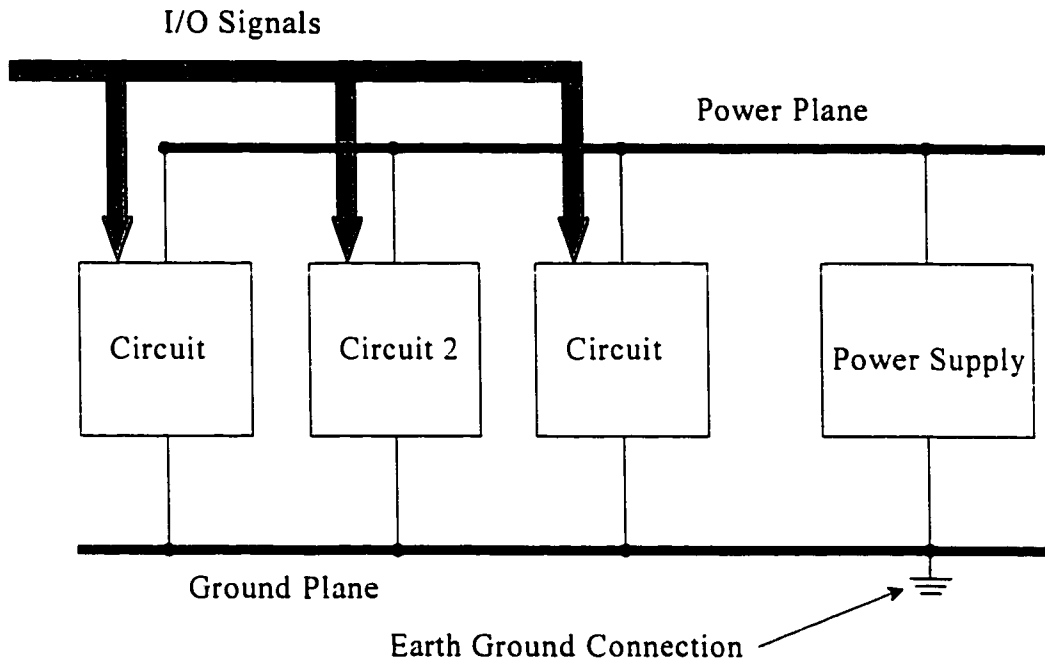


Figure 4.12 Multipoint power and ground connection

noise coupling illustrated in Figure 4.4. Noise coupling through the power supply source impedance will still remain. A less expensive method of connecting multiple circuits to ground and power is to use a multipoint grounding system. Multipoint connection systems use common ground and power planes to which the various circuits having the same noise properties are connected through short leads. Figure 4.12 shows the connection of multiple circuits to the power supply and ground of a multipoint system [24, p.6-13].

Preferred grounding practice uses separate planes for analog, digital, and noisy ground to provide parallel isolation of circuits having the same noise properties. Noisy ground contains switching elements, motors, and high power circuits that are predicted to produce large electromagnetic fields. Hardware ground, used to ground the chassis and printed circuit board racks, should also be segregated from the other grounds with a separate parallel 'earth' ground connection [24, p.6-13].

4.3.3 Electromagnetic Field Induced Noise Reduction

Shielding against electromagnetic field induced noise must be done by individually reducing the effects of interference from electric, magnetic, and RF fields. Techniques used to shield against one type of field can also help to reduce the interference effects from another type of field or coupling process.

Shielding Against Capacitive Coupling

The stray capacitance between two circuits drops off linearly as the distance between the two circuits is increased. Electric field coupling is reduced by simply increasing the distance between the receptor, or victim, circuit and the noisy circuit. Electric field coupling is also reduced by avoiding high circuit and conductor termination impedances, thereby reducing the value of R in (4.2). Noise coupling through the electric field of a noisy circuit is broken by surrounding the victim circuit in a metal enclosure called an electrostatic or Faraday shield. The Faraday shield is grounded to ensure that shield capacitances do not produce crosstalk and feedback elements [24, p.6-7].

Shielding Against Inductive Coupling

Interference caused by inductive coupling is reduced by minimizing the area of the current loops in both the noisy circuit and the victim circuit. Equation (4.5) shows that the induced noise voltage produced by inductive pick-up is proportional to the enclosed area A_{enc} of the conducting path. Reduction of A_{enc} is performed through the use of coaxial cable, twisted pairs, ground planes, and gridded circuit board construction [24, p.6-7].

Coaxial cable is made by surrounding a centre conductor with a cylindrical shield. The inner conductor carries current I^+ , while the outer shield carries a current equal to that

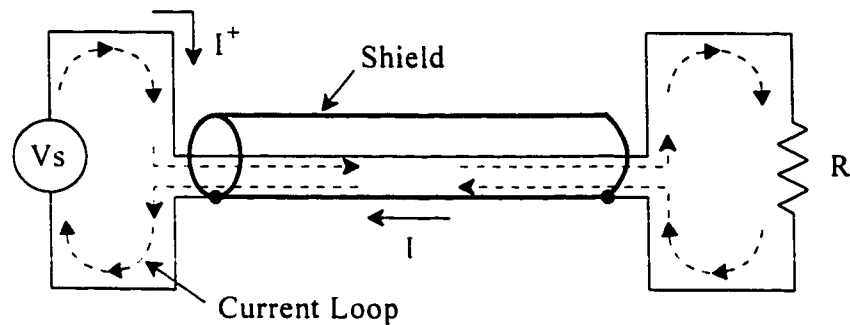


Figure 4.13 Coaxial cable connection

of the inner conductor in the opposite direction. Figure 4.13 shows the configuration used with a coaxial cable to reduce the effects of inductive coupling [24, p.6-8]. The magnetic field produced by the current I^+ in the centre conductor is cancelled by the magnetic field I in the shield. The net result of the coaxial cable operation is that no magnetic field is produced outside of the cable by the current carrying conductor inside the cable, thereby adding an effective zero area to the current loop. Magnetic field cancellation also makes the coaxial cable immune from inductive pick-up from external magnetic fields. Hence, coaxial cable is used to transport noisy signals through clean environments as well as to transport clean signals through noisy environments [24, p.6-8].

Full magnetic shielding in a coaxial cable occurs only when the shield carries the same current as the centre conductor. Practical applications in circuits such as the desired VSI have both the receiver and the signal source connected to a common signal ground. Coaxial cables used in such applications should always have both ends of the shield connected to ground. Figure 4.14 shows the effects of three different cable configurations used to connect a grounded signal source to a grounded load [24, pp.6-8,6-9]. Grounding of the shield at only one end allows no current to flow in the shield and produces no magnetic

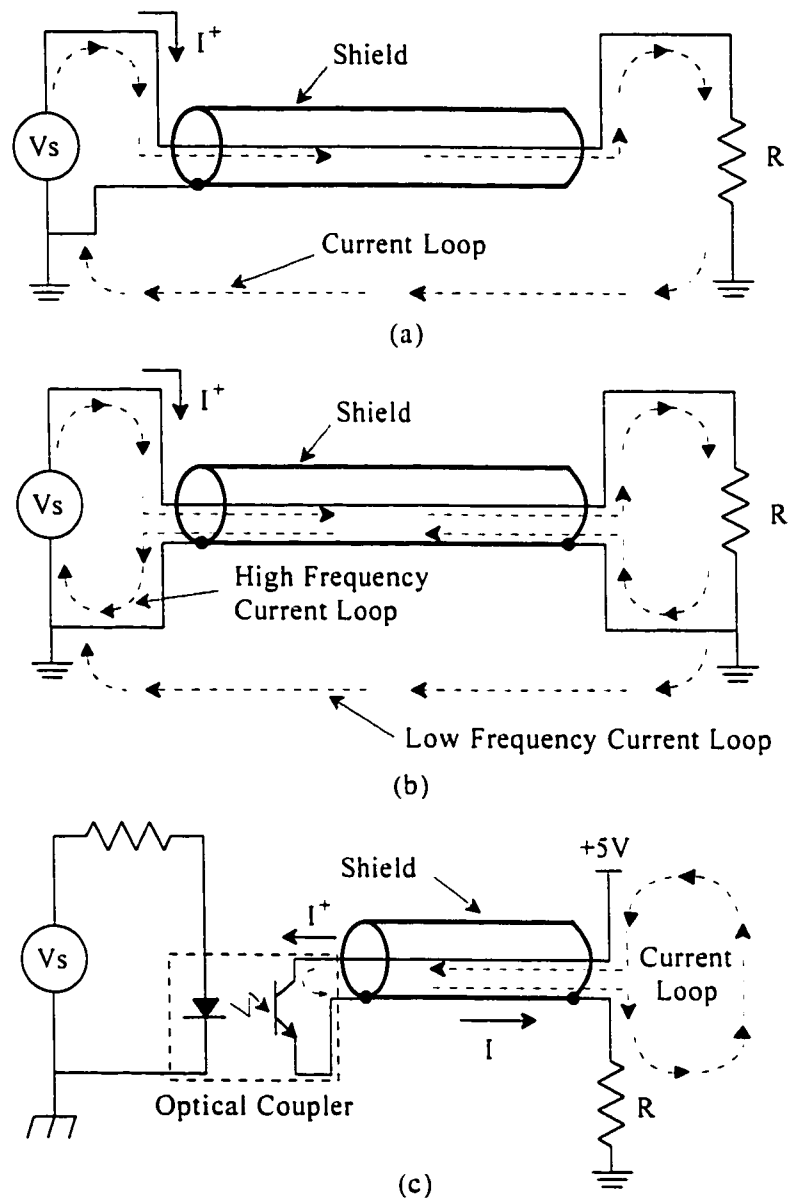


Figure 4.14 Coaxial cable connection of grounded signal source to grounded receiver shielding. The coaxial shield does still provide electrostatic shielding over the conductor area enclosed by the shield. The separated 'earth' grounds create a ground loop and a large current loop area, as shown in Figure 4.14 (a), and discussed previously in Section 3.3.2.

A coaxial cable grounded at both ends will provide an alternate current path for the loop current, as shown in Figure 4.14 (b). The loop current will generally follow the path of

least impedance. Inductive reactance is small at frequencies below several kHz, and the loop current will follow the path of least impedance. The path of least impedance may or may not be through the coaxial cable shield. Inductive reactance is high at frequencies above several kHz, and the current will follow the path of least inductance. The zero effective loop area of the coaxial cable provides this path of least inductance, thereby producing an effective shield against the generation and reception of EMI [24, p.6-8].

Digital circuits used in a noisy environment are enhanced by breaking the ground loop of Figure 4.14 (b). The circuit in Figure 4.14 (c) provides an ideal solution for the transmission of remotely generated switching circuit firing signals through a noisy environment and to a VSI [24, p.6-9]. An optical coupler is inserted at the digital signal source to redefine the source as being ungrounded. Ungrounding the digital signal source allows the same current magnitude to flow in the shield as in the centre conductor, thereby producing magnetic field cancellation. Optical coupler insertion can also be done at the receiving end of the cable to redefine the receiving load as being ungrounded. Gate driver circuits, such as those for the VSI in this thesis, are prepackaged with optocouplers to allow a circuit designer to configure a switching application for reduced EMI.

A twisted conductor pair is used as an inexpensive alternative to a coaxial cable. Feed and return wires can be twisted together to minimize their loop area. The noise picked up by one twist will cancel out the noise picked up in the next twist. Twisted conductor pairs are almost as effective as coaxial cables in providing magnetic shielding. A twisted pair does not provide shielding against capacitive coupling [24, p. 6-8].

Ground planes are used as conducting surfaces to function as return conductors for

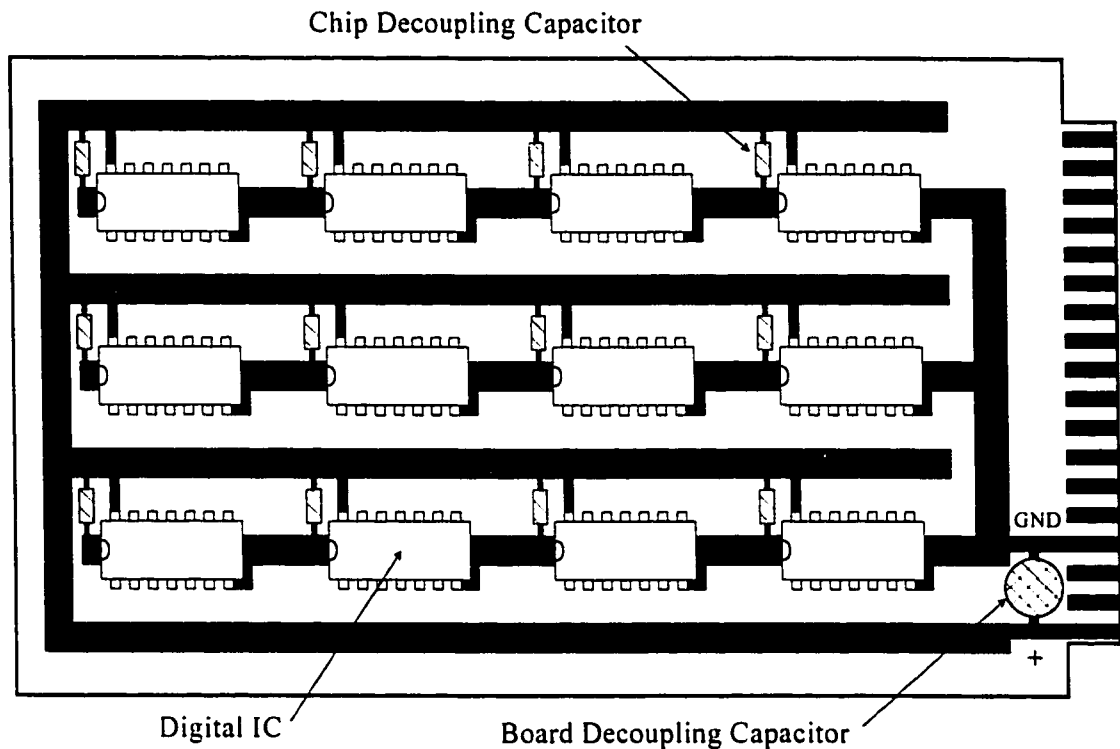


Figure 4.15 Gridded circuit board layout

all of the current loops in a circuit. Ground planes are used primarily for higher frequencies where the ground path impedance is mainly due to the inductive reactance of the circuit. A current that zig-zags along the feed path of a circuit that employs a ground plane is free to return in a zig-zag fashion along the ground plane so as to minimize the inductance formed by the loop. A minimal loop inductance results in both a minimal susceptance to EMI, as well as a minimal generation of EMI. Circuits that use multiple power connections can also use a power plane to further reduce EMI susceptibility in the same manner as with the ground plane [24, p.6-9].

A gridded circuit board construction is used in applications where it is not possible to use ground and power planes. Figure 4.15 shows the type of gridded circuit board struc-

ture that is used throughout the prototype electronic test setup for this thesis. The gridded circuit board is almost as effective as the ground and power plane approach since current loops have the freedom to follow any of multiple paths that reduce the loop area [24, p.6-10]. The illustration in Figure 4.15 also shows the location of the board and chip decoupling capacitors described in Section 3.3.1.

The inductive coupling noise reduction techniques described so far have all focused on the reduction of the enclosed area A_{enc} of the conducting path. Examination of (4.5) shows that the noise voltage generated from the inductive coupling is also proportional to the time derivative of the magnetic flux density B . The flux density produced by a magnetic field generator in air will drop with the square of the distance from the magnetic field generator. An effective method of reducing the susceptibility of a circuit to the EMI from magnetic fields is to increase the distance between the victim circuit and the suspected source of the magnetic field. Another method of shielding from low frequency magnetic fields is to divert the magnetic field by presenting a low reluctance path to the magnetic flux [24, p.6-12]. A high permeability material such as mumetal is often used for this type of shielding. At frequencies above a few kHz, magnetic shielding is accomplished through the use of steel, as will be discussed in the next section.

Shielding Against RF Interference

The generation and characteristics of RF interference were briefly outlined in Section 3.2.3. Shielding against the E-field generation of a whip antenna, such as a wire wrap post, is most effectively done through the use of a Faraday cage. It is impractical to construct a Faraday cage for each wire wrap post on a prototype gridded circuit board of the

type used in this thesis. The most practical solution is to avoid the use of wire wrap in circuits, such as high frequency PWM oscillators, that are suspected of producing RF interference. Careful consideration of the circuit operation and layout must be made before its construction. Interference produced from RF current loop antennas is reduced by applying methods that are used to protect a circuit from inductive coupling. A gridded ground structure, such as the one outlined in Figure 4.15, is very effective in reducing the loop antenna area [24, p.6-10].

Snubber circuits connected directly across the VSI switching devices limit the dv/dt and di/dt stresses on the switching device. Limiting the rate of change in the voltage and current also reduces the generation of RF interference from the VSI. Snubber circuit design should not only be used by a designer to reduce switching stresses, but should also be used to reduce EMI induced noise problems [23].

Difficult cases of RF interference may require the use of metallic shielding. Time varying electromagnetic fields will induce currents in a metallic material. The induced currents dissipate energy through I^2R losses in the metal shield and through radiation losses as they re-radiate their own fields. Absorption losses are commonly used to refer to the I^2R losses, while reflection losses are commonly used to refer to the re-radiation losses. The weakening of a time varying H-field as it penetrates a metallic shield is mainly due to absorption losses. Absorption loss is increased through the use of a thicker shield with higher permeability and conductivity. Figure 4.16 shows the typical absorption loss of steel and copper as a function of the electromagnetic field frequency [24, p.6-10].

Reflection losses are the primary shielding mechanisms for E-fields. The reflec-

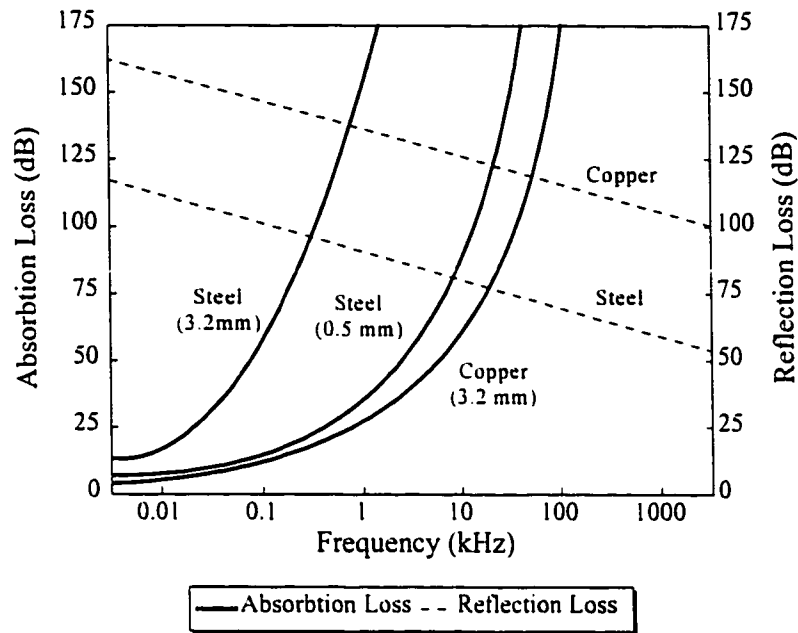


Figure 4.16 E and H-field shielding effectiveness

tion loss occurs on the surface of a material, and is independent of the material thickness. Shielding of the E-field is more effective if the shielding material has a high conductivity and a low permeability. Figure 4.16 also shows the reflection loss of steel and copper as a function of the electromagnetic frequency. The different EMI attenuation characteristics of the various materials make it apparent that an educated guess must be made regarding the E/H composition of the electromagnetic field before choosing a shielding material. Holes and seams in the shielding material will also reduce the effectiveness of the metallic shield and should be avoided [24, 6-11].

Radio frequency emissions from a VSI drive are created mainly through the high frequency current loops in the power transmission lines and near the actual switching devices. Shielding from RF emissions is accomplished by using coaxial conductor power cables. Enclosure of all high power current carrying conductors with 1.5 mm thick steel

conduit is used if coaxial power cables are not available, or are too expensive for the application. Additional shielding is realized by encasing the actual switching circuits and all RF interference susceptible circuits in 1.5 mm thick steel boxes.

A low impedance path for RF ground current is created by adding grounding capacitors from both the +ve and -ve rails of the inverter dc link to the grounded heat sink of the inverter switching devices. A grounding capacitance value of 0.022 μf may be sufficient [23]. Connection of a low ESR, low internal inductance, line capacitor across the dc bus and close to the VSI switching devices, will provide a low impedance path for differential mode RF current generated in the switching devices. A 1 or 2 μF ceramic capacitor will be much more effective in reducing differential mode RF current than the proposed high capacitance, and comparatively high ESR, energy storage tank.

The noise reduction techniques presented in this chapter represent a critical part of the design process for any power electronic system. High speed operation of an inverter driven machine produces large quantities of EMI when compared with low speed operation. All of the different types of EMI generation are present in the proposed high speed CCVSI, and must be carefully considered during construction.

CHAPTER 5

DESIGN AND CONSTRUCTION OF A HIGH PERFORMANCE MICROPROCESSOR CONTROLLED PMSM DRIVE

5.1 DESIGN LAYOUT

5.1.1 Previously Proposed Implementation Strategy

The Chapter 3 peak power transfer tests have directed the focus for the remainder of this thesis on the development of a high performance, high efficiency sinusoidal phase current, microprocessor interfaced, vector controlled, high speed PMSM drive. The implementation procedure for the realization of such a PMSM drive was previously discussed in [11, pp.29-45]. Figure 5.1 shows the block diagram for the system proposed in [11]. The proposed drive uses an advanced microcontroller to read the current, position, and speed feedback signals from the PMSM, and to develop the required current error signals for an error- Δ comparison PWM switching current controller. Firing signals developed by the error- Δ current controller are applied to a VSI to generate a three phase balanced set of currents to the PMSM of the FESS.

The system proposed in [11] uses microcontroller generated current error signals that are proportional to the difference between the actual phase currents and the reference phase currents. Reference phase currents are used to position the actual phase current so that current vector control can be performed relative to the back-EMF of the PMSM. A

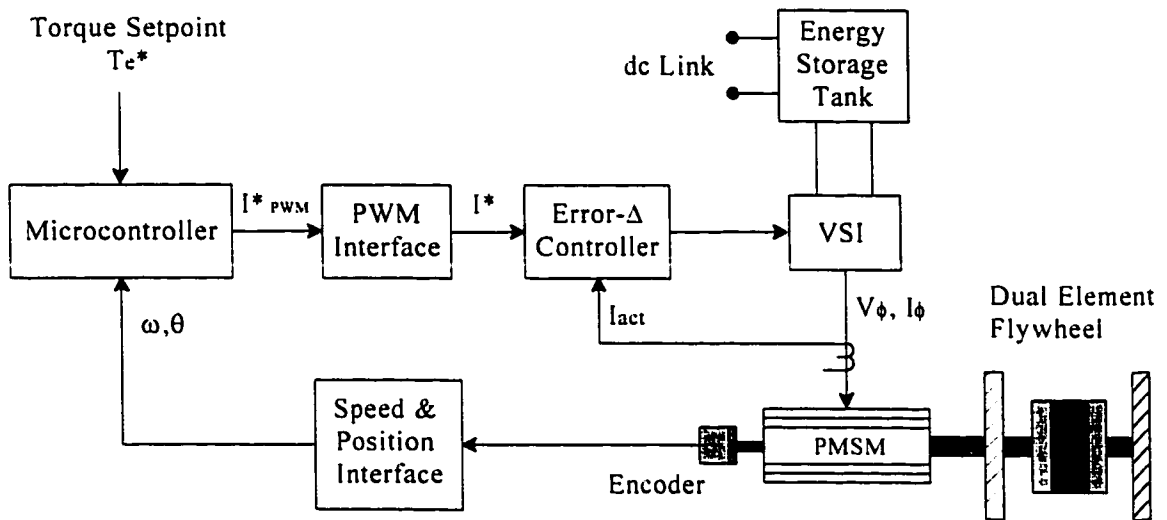


Figure 5.1 Initial high performance microprocessor controlled PMSM drive system

torque control algorithm is to be implemented on the microcontroller so that the PMSM electrical torque follows a desired user set torque control input T_e^* .

5.1.2 Current Control Strategy

Current control of a VSI inverter was chosen to allow for the control of the phase current magnitude I_ϕ , and the angle δ between the phase current fundamental and the fundamental of the PMSM back-EMF. Control of I_ϕ and δ provides the ability to control the speed and torque of a PMSM [25, p.422]. Multiple current controlled voltage source inverters can be connected to the same dc bus to provide parallel FESSs. The frequency range of a VSI is much higher than that of a Current Source Inverter (CSI), thereby providing the advantage of high speed PMSM operating capabilities. A VSI inverter drive coupled to a dc source is much smaller and more affordable than a CSI. Sinusoidal current generated by the CCVSI contains high frequency harmonics which have little effect on the operation of the PMSM. The electrical torque produced by the sinusoidal current generated by the CCVSI

will occur at a high efficiency and is ripple free. The previously stated advantages of the CCVSI make it ideal for use in a high speed FESS drive investigated in this thesis.

Synchronous operation of the PMSM requires that the Magnetomotive Force (MMF) produced by the permanent magnets on the rotor remains synchronized with the revolving MMF produced by the stator phase currents. A true synchronous mode of operation uses a current supply frequency that is controlled from an independent oscillator. The frequency setpoint is used as a control parameter since the PMSM rotor speed is dependent on the frequency of the stator MMF. Torque produced by the PMSM varies with the electrical angle between the stator and rotor MMFs. A load disturbance on the rotor temporarily disrupts the equilibrium torque angle and results in a torque angle oscillation. A large load disturbance will pull the rotor out of synchronism with the stator MMF and cause the loss of torque control. The hunting and stability problems associated with the true synchronous mode of operation make it unfavourable for use in variable speed torque control led PMSM applications.

The self-controlled mode of synchronous operation uses speed feedback from a shaft position encoder to synchronize the frequency of the sinusoidal stator currents to the frequency of the revolving rotor MMF. Self-controlled synchronous operation provides the advantages of eliminating hunting and stability problems as well as ensuring that the rotor will not pull out of step with the stator MMF. An increase in the machine loading will simply cause the rotor to slow down as the stator frequency is automatically decreased to maintain the same electrical torque angle. Examination of the simplified PMSM generation mode equivalent circuit, presented in Section 3.4.3, shows that the generated phase current

is proportional to the difference between the terminal voltage V_t and the back-EMF E_{bo} of the machine. A similar relationship exists for the motoring operation of the PMSM, where a decrease in the rotor speed decreases the rotor back-EMF and causes a corresponding increase in the phase current. An increase in phase current increases the electrical torque production until an equilibrium point between the load torque and the electrical machine torque is reached at a lower rotor speed. The effective operation of a PMSM using self-controlled synchronization is very similar to that of a conventional dc machine.

The phase current magnitude I_ϕ and angle δ is adjusted to increase the electrical torque of the PMSM until the machine torque equals the load torque at a desired speed level. Speed control is achieved indirectly through the control of the machine torque [25, p.422]. The simplified VSI used in the Chapter 3 tests is an example of the self-controlled mode of PMSM operation. Position signals from the shaft position encoder are used to generate the firing signals, creating a phase voltage firing frequency that is always equal to the rotational frequency of the rotor. Successful operation of the simplified VSI has demonstrated the advantages of the self-controlled mode of operation. A self-controlled mode of operation will be implemented in the proposed high performance CCVSI so that the same advantages can be realized as with the simplified VSI.

5.1.3 Modified Microprocessor Control Strategy

The advantages of self-synchronization make this mode of operation ideal for use in the proposed high performance microprocessor controller drive. Implementation of self-synchronized low harmonic sinusoidal current generation requires a rotor position feedback

resolution of no larger than a few electrical degrees to ensure smooth torque control and low harmonic current generation [21]. A reference current waveform with 125 points per cycle requires a 2.88 electrical degree resolution. Such resolution corresponds to a reference phase current waveform update rate of 33 333 times per second at 8000 rpm PMSM operation. The microcontroller proposed in [11, p.57] is capable of providing 2.88 electrical degree waveform generation at an 8000 rpm PMSM operating speed. The addition of torque control algorithm execution, phase current and voltage A/D conversion, and current error generation requirements reduces the resolution of the microcontroller generated reference current waveforms to an unacceptable 49 electrical degrees [11, p.55]. A reconfiguration of the tasks assigned to the microcontroller is necessary for successful implementation of the proposed drive.

A microcontroller can provide the flexibility of high speed I/O, A/D and D/A functions. Distortion free sinewave generation and execution of the previously mentioned functions is not possible if the microcontroller must implement the additional tasks required for the control of the PMSM torque through current vector manipulation. A microprocessor or Digital Signal Processor (DSP) is more suitable than a microcontroller to perform the lengthy calculations required for the current vector control of the PMSM torque. Task decoupling between the microcontroller and a separate microprocessor is used to enhance the overall execution of the control. The microprocessor is used optimally for its ability to execute the calculation intensive algorithms and reasoning, while the microcontroller is used optimally for its ability to perform the reference waveform generation and signal conversion functions of the drive.

Figure 5.2 illustrates a block diagram for the modified microprocessor control strategy. The microprocessor and the microcontroller write to and read from shared memory. Shared memory allows each device to perform its specific task without having to wait for the other device. Additional circuitry is used to measure and calculate the speed, true rms phase current, true rms phase voltage, and average phase power of the PMSM. The microprocessor reads the speed, current, voltage and power values and uses them to compute the

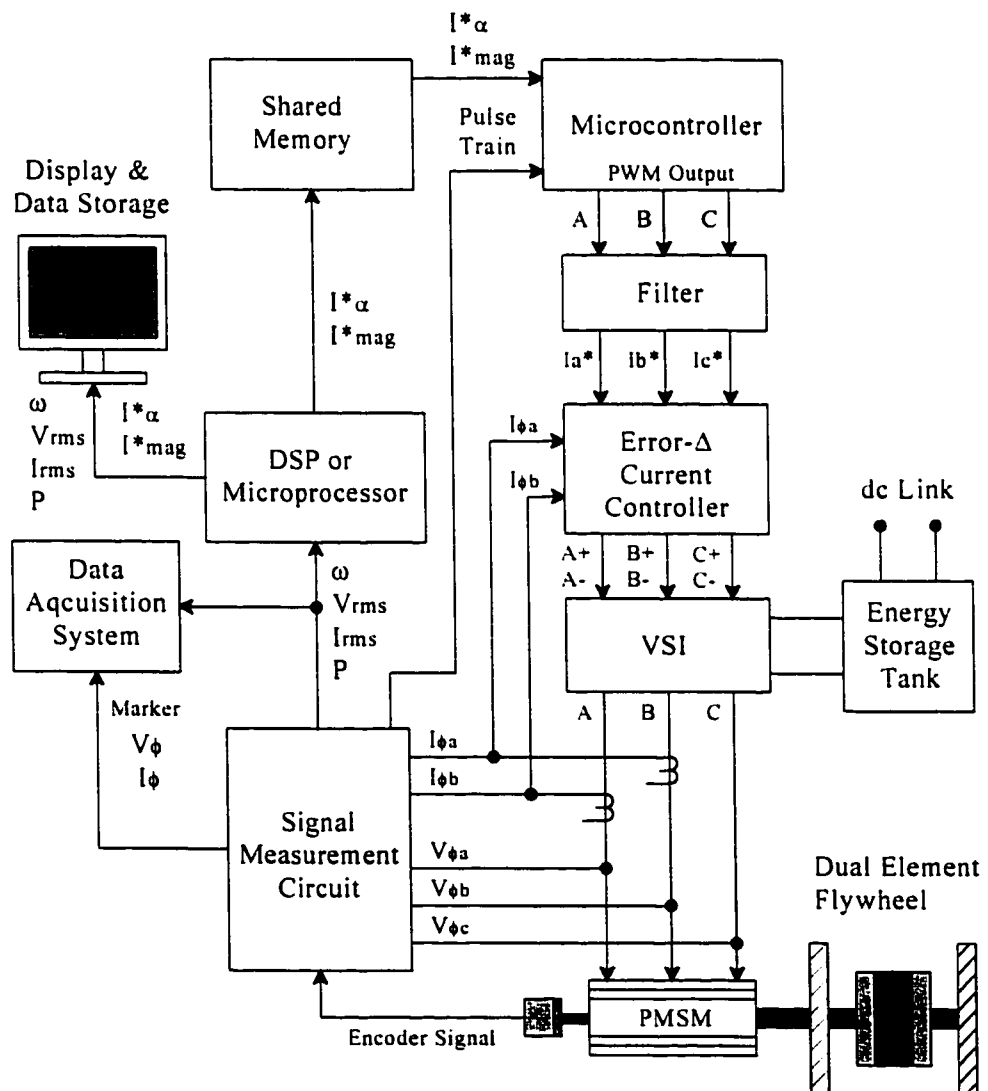


Figure 5.2 Modified high performance microprocessor controlled PMSM drive system

desired reference current waveform magnitude I_{mag}^* and angle I_{α}^* . A user display and interface is also provided through the microprocessor to allow for manual control and data acquisition functions. The desired phase current magnitude and angle values are repeatedly written to shared memory by the microprocessor, and read by the microcontroller at different, non-synchronized rates. Pulse width modulated outputs are generated by the microcontroller according to the desired phase current magnitude and angle, as well as the realtime position of the rotor. The PWM reference current waveforms are filtered to generate realtime analog reference currents that are applied to the error- Δ current controller.

The error- Δ current controller determines the error between the actual measured phase currents and the microcontroller/microprocessor generated reference currents. The error is determined through the use of analog summation circuits, thereby reducing the processing requirements of the microcontroller. Use of an error- Δ current controller guarantees that the VSI will operate over a predictable switching frequency. A predictable switching frequency allows for easier filtering of the measured feedback signals which can be used for the direct calculation of the PMSM phase inductance.

Realtime calculation of the PMSM phase inductance has been proposed as a method to eliminate the use of a shaft position encoder [26]. Shaft position encoder elimination makes the high speed drive more reliable as it removes a component that is very susceptible to failure and high speed noise problems. Figure 5.3 shows the block diagram of the reconfigured proposed system that is capable of shaft position encoder elimination through realtime phase inductance calculations. A fast A/D converter is interfaced with a microprocessor or DSP which performs all of the position and speed estimation. The estimated

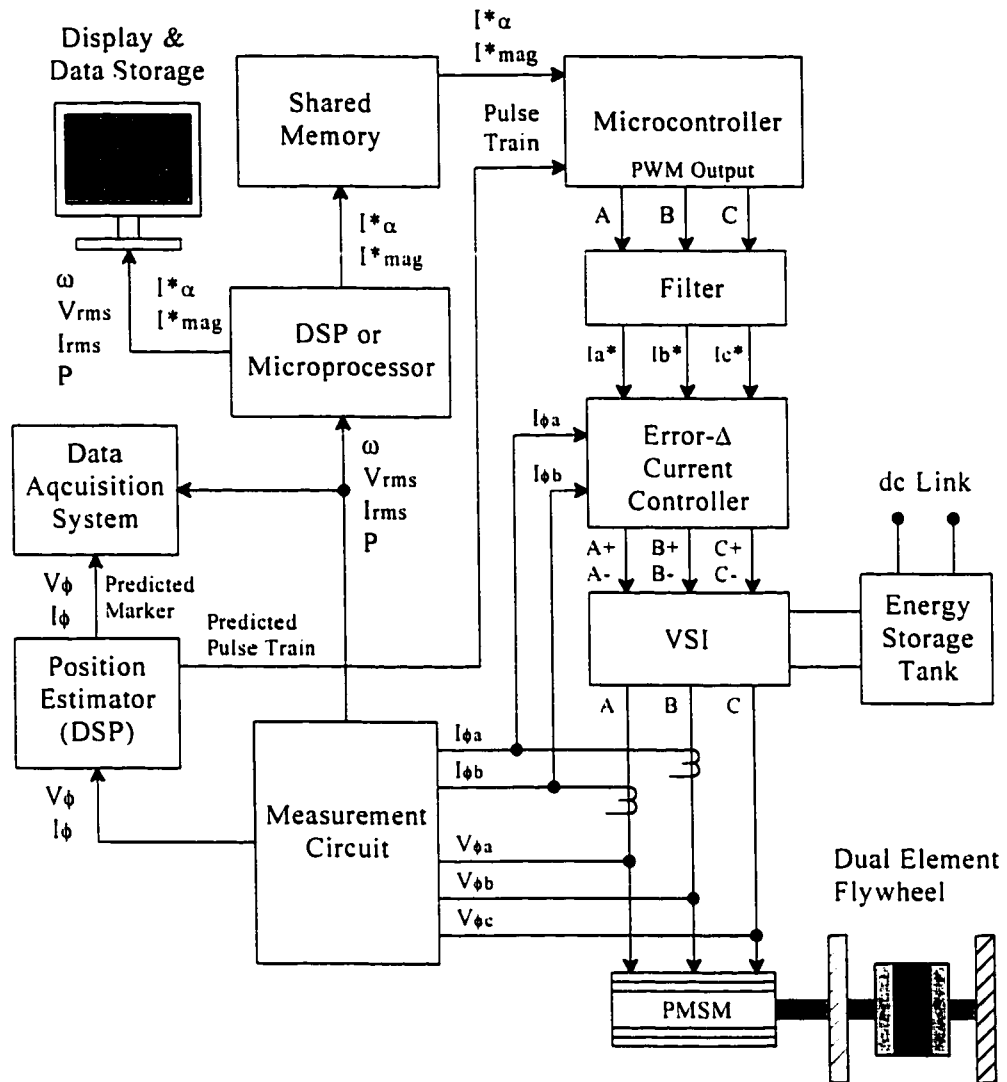


Figure 5.3 Encoderless high performance microprocessor controlled PMSM drive system

value of the position is used to generate a predicted pulse train that is interfaced with the microcontroller. The estimated speed is interfaced directly with the DSP or microprocessor.

Shaft position encoder elimination is not implemented in this thesis. The modified microprocessor control strategy, illustrated in Figure 5.2, has been constructed to allow for the flexibility of implementing the shaft position encoder elimination technique at a later

date. An investigation into the use of an additional microprocessor or dedicated DSP to perform phase inductance calculation and position estimation is recommended for further work. The remainder of this chapter is dedicated to explaining the design and implementation of each of the function blocks in the actual laboratory constructed working model of the proposed high performance microprocessor controlled high speed PMSM drive system.

5.2 DRIVE CONSTRUCTION

5.2.1 PMSM and Encoder

The PMSM used for the construction of the proposed high performance drive is identical to the one used for the simplified VSI control in Chapter 3. The power cables and connections to the PMSM are improved from the previous test setup to reduce line resistance. Conduit is used extensively in the new test setup to shield the environment from the power cable EM radiation. A coaxial cable transmits the PMSM shaft position encoder signals to the measurement circuit, and the entire position encoder is electrically isolated from the shaft and frame of the PMSM to provide ground isolation. The PMSM is mounted on the same frame as the previous test setup so that it can be coupled either directly to the dual element flywheel, or through a speed reducer to a dc machine.

5.2.2 Voltage Source Inverter

The VSI for the proposed high performance drive is a reconstructed version of the VSI proposed in [11] and used in Chapter 3. Grounding to the heat sink has been improved along with the firing signal cable and connections to the VSI. Shielding techniques described in Chapter 4 are used throughout the reconstructed VSI. Steel conduit is used to

enclose the dc link cables from the energy storage tank to the VSI. The energy storage tank is contained in a steel cabinet to shield the environment from EM field radiation. A steel enclosure also shields the firing signal cable termination and IGBT gate drivers from EMI, while a separate metal enclosure around the inverter shields the environment from the EM waves generated by the IGBTs and their snubber circuits. A 0.022 μF ceramic capacitor is connected between each side of the dc link and the heat sink of the inverter, while three 0.33 μF polypropylene-film capacitors are connected across the dc link into the inverter. New snubber circuits are employed to further limit the rate of turn-on and turn-off of the VSI and reduce the RF emissions. A full schematic of the modified VSI and its associated components are found in the supplementary document to this thesis.

5.3 ERROR- Δ CURRENT CONTROLLER CONSTRUCTION

5.3.1 Current Controller Layout

The error- Δ current controller used in the high performance drive is similar to the one proposed in [11]. Figure 5.4 shows the functional diagram for the error- Δ current controller. Analog reference current waveforms are compared to the actual current waveforms for each phase. An error signal proportional to the difference between the actual and the reference current is modulated with a high frequency triangle waveform to produce a phase leg switching pattern that will reduce the current for a positive current error and increase the current for a negative current error. A lockout circuit is employed to ensure that the error- Δ current controller cannot command the VSI to turn on both sides of a phase leg at the same time. The full schematic for the error- Δ current controller is provided in the

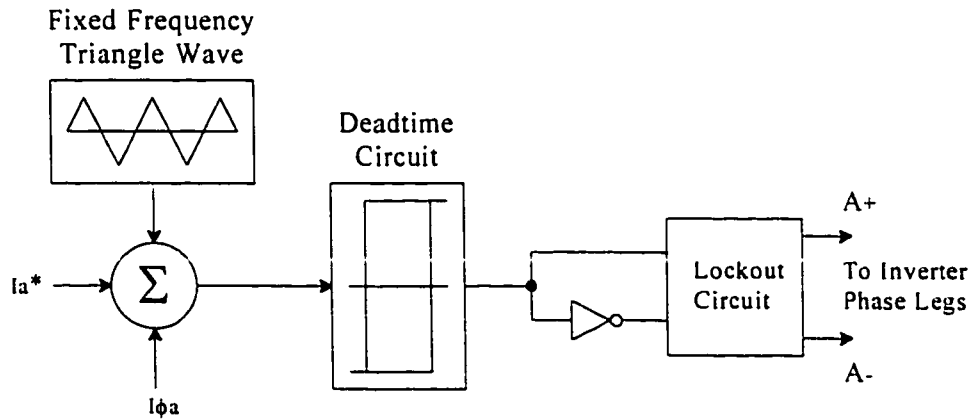


Figure 5.4 Error- Δ current controller functional diagram

supplementary document for this thesis and additional information on the error- Δ current controller can be found in [27] and [28].

5.3.2 Phase Current Feedback

Feedback Layout

Measured current signals from two of the three phases are fed back to the error- Δ current controller. The third phase is calculated according to (5.1) with the assumption that all three phases of the PMSM are balanced. (See manf. specs. in Appendix A4 & A5.)

$$I\phi_A + I\phi_B + I\phi_C = 0 \quad (5.1)$$

Feedback of two phase currents, rather than three, allows for a reduction in the feedback electronics. The current feedback signals are measured using the configuration shown in Figure 5.5. Current in phases A and B of the PMSM are measured using two Hall-effect current transformers. The current transformers are mounted directly to a printed circuit board and enclosed in a steel box to reduce EMI. A pre-gain and offset adjust circuit is used to pre-calibrate the phase current measuring circuit and provide 1 Vrms for every 10 Arms

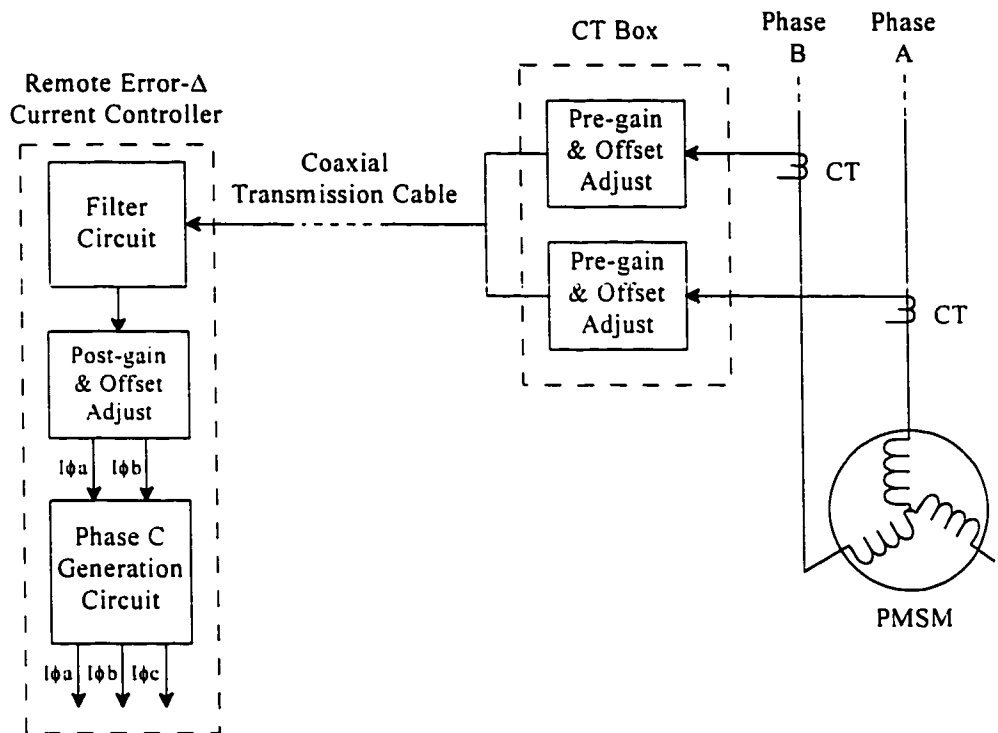


Figure 5.5 Phase current feedback block diagram

of phase current. Coaxial cable is used to transmit the measured phase current signals from the Current Transformer (CT) box to the remote error- Δ current controller.

A 3rd order Butterworth filter circuit is used to low pass filter each of the two phases and isolate the low frequency components of the phase current. Figure 5.6 shows the actual gain and phase angle delay as measured on the 1941 Hz cutoff frequency filters. A maximum phase current frequency of 267 Hz is expected for 8000 rpm PMSM operation. Figure 5.6 indicates that linear gain and phase delay approximations can be made for the Butterworth filter at frequencies under 300 Hz. Attenuation of the phase current signal is assumed to be negligible as there is less than a 0.5% reduction in the filtered signal below 300 Hz. The phase angle delay varies significantly over the 0 to 300 Hz range and needs to be estimated.

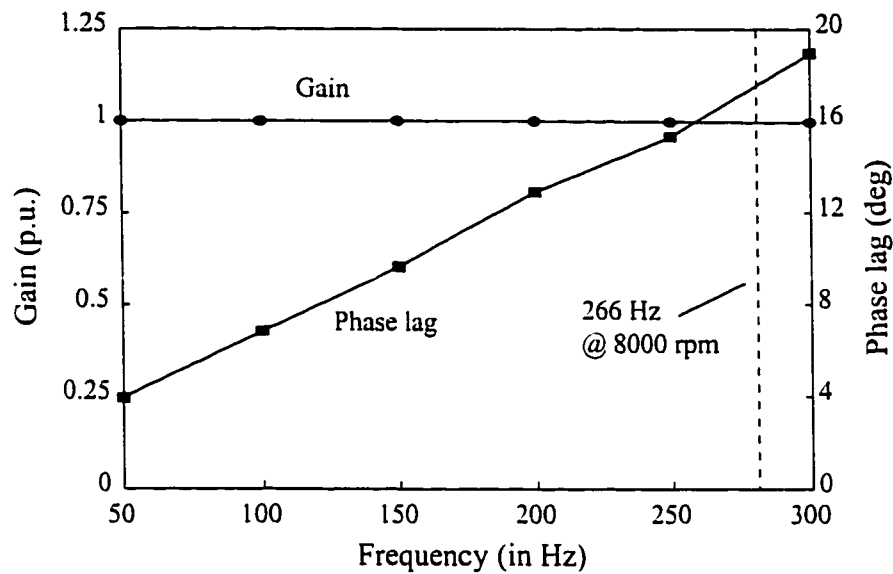


Figure 5.6 3rd order, 1941 Hz cutoff frequency Butterworth filter characteristics

A final calibration circuit is used to set the post-filter offset to 0 V. The post-filter gain is set so that 1 Vrms of the measured current signal represents 4 Arms of the actual phase current. A maximum 28 Arms phase current can be accurately measured using this feedback circuitry. Phase C generation is performed by implementing (5.1) through the use of analog inversion and summation circuits. The full schematics for the current measurement and feedback circuitry are found in the supplementary document for this thesis.

Delay Measurement

Two significant delays occur in the proposed error- Δ current controller. Figure 5.7 shows the location of the two delays. Current controller delay represents the delay between the phase current commanded values I_{ϕ}^* and the actual phase current I_{ϕ} that is supplied to the PMSM. The current controller delay is inherent with an error- Δ modulation strategy and will vary according to the operating speed and loading of the PMSM. Phase current feedback delay represents the delay between the actual phase current supplied to the PMSM

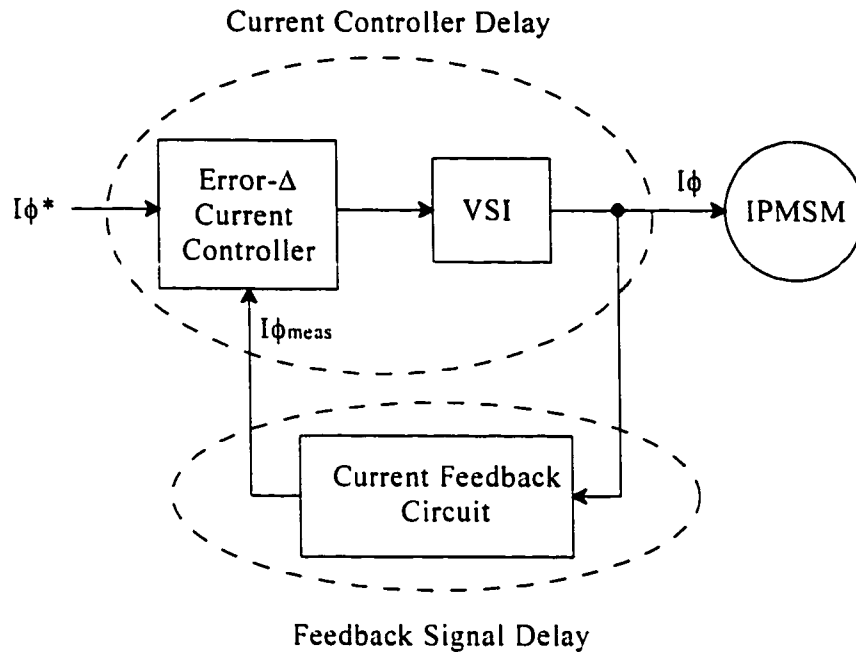


Figure 5.7 Phase current generation and feedback delay

and the filtered, post-gain and offset adjust, calibrated measured signal applied to the error- Δ current controller. Measurement of the phase current feedback delay allows for the calculation and placement of the actual phase current vector using information obtained only from the current controller feedback signals.

The effect of the feedback delay is to offset the current controller delay. The error- Δ switching signals are generated to force a reduction in the error between the phase current command and the feedback signal applied to the error- Δ current controller. Ideally, a feedback signal that is exactly in phase with the reference phase current signal will effectively produce an error- Δ switching action that creates an actual phase current that is phase advanced from the reference current signal by an amount equal to the feedback delay. Knowledge of the feedback delay provides a means to estimate the actual phase current, and thereby estimate the current controller delay.

The feedback signal delay is measured through the construction of additional circuitry in the current feedback loop. Zero crossing detectors are connected to the output of the post-gain and offset adjust circuit, and across the output of a function generator. The function generator is used to provide a variable frequency sine wave to the inputs of the pre-gain offset and adjust circuit. The sine wave is adjusted to produce 5 V_{rms} at the post-gain and offset adjust circuit, representative of a 20 Arms phase current. All signals are calibrated for 0 V_{dc} offset. Feedback signal delay is measured by recording the time delay between the zero crossing of the function generator output, and the zero crossing of the post-gain and offset adjust circuit. Measurements are conducted at frequencies between 100 Hz and 300 Hz on both feedback signal circuits, and the time delay is converted to electrical degrees. Table 5.1 provides the results of the feedback signal delay measurement.

Inspection of Table 5.1 reveals that the feedback signal delay is linear with respect

Table 5.1
Measured Feedback Signal Delay

Frequency	Phase A delay (elec. deg.)	Phase B delay (elec. deg.)
100	6.9	6.9
125	8.6	8.6
150	10.3	10.4
175	11.8	12.1
200	13.5	13.8
225	15.2	15.6
250	16.9	17.3
275	18.6	19.0
300	20.3	20.7

to the electrical angle over the measured frequency range. The linearity of the results allows for the development of equation (5.2) which is used to determine the feedback signal delay to an accuracy of $\pm 1\%$. Equation (5.2) provides a simple and accurate method of calculating what angular adjustment is required on the feedback signal to determine the actual phase current vector.

$$\text{Feedback Signal Delay} = 190 \mu \text{sec} \cdot \text{line frequency} \cdot 360^\circ \quad (5.2)$$

The full schematic diagrams of the zero-crossing detect circuitry used in the measurement of the feedback signal delay are provided in the supplementary document to this thesis.

5.3.3 Error- Δ Control Circuit

Error Calculation

Error- Δ current controllers use subtractor circuits to determine the difference, or ‘difference error’, between the commanded phase current value I_ϕ^* and the measured phase current $I_{\phi \text{ meas}}$. The error- Δ current controller used in this high performance drive adds the measured phase current $I_{\phi \text{ meas}}$ to the commanded phase current value I_ϕ^* to determine what is called the ‘summation error’. The error- Δ modulation strategy generates a switching pattern that switches each phase leg of the VSI in a manner that will reduce the error signal. A reduction of the error signal, which is now the sum of the commanded and measured phase currents, forces the actual phase current to follow the negative of the commanded phase current. Such current control allows for a more stable controller operation than what is experienced with the ‘difference error’ approach.

The error- Δ current controller generated switching pattern forces the feedback sig-

nal to equal the reference current signal. The presence of feedback delay produces an actual phase current that leads the reference current signal. Figure 5.8 shows a simulation of the reference current, feedback signal, error signal and the actual current produced using the 'difference error' method. The error signal is amplified with a gain of 4. Current controller delay guarantees that the switching action of the error- Δ current controller will never reduce the pure 'difference error' signal to zero. Hence, the feedback current will lag behind the reference current by a few degrees. The actual phase current leads the feedback current by 18° at 8000 rpm (see (5.2)), and thereby also leads the reference current. Control of the actual phase current translates into a requirement that the reference current must be adjusted to position a current phasor that precedes it in time.

Indirect control of signals that have already occurred is accomplished by adding 360° to the actual phase current signal. Indirect control is awkward and can easily be avoided by performing control through the 'summation error' method. Figure 5.9 shows a simulation of the reference current, feedback signal, error signal and the actual current produced using the summation error method. The 'summation error' method effectively shifts the current control by 180° so that the actual phase current always lags the reference current. The reference current is adjusted in advance to produce a desired response in the actual phase current.

Inherent stability of the 'summation error' method was verified in the laboratory, as current controller operation with both the 'difference error' and 'summation error' methods was evaluated. Schematic diagrams of the circuitry constructed for the error calculation are provided in the supplementary document for this thesis.

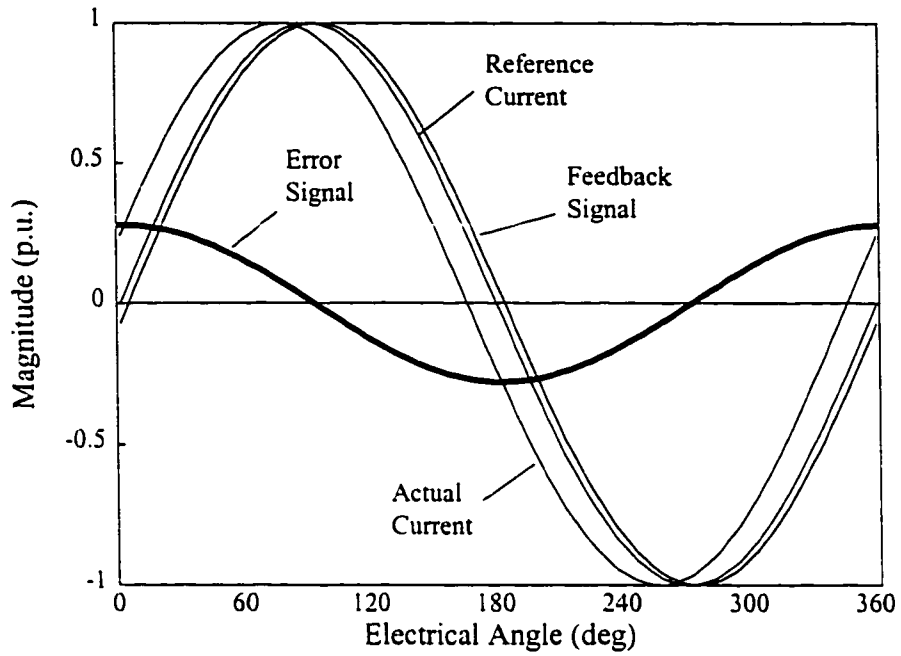


Figure 5.8 Error signal generation: difference error method

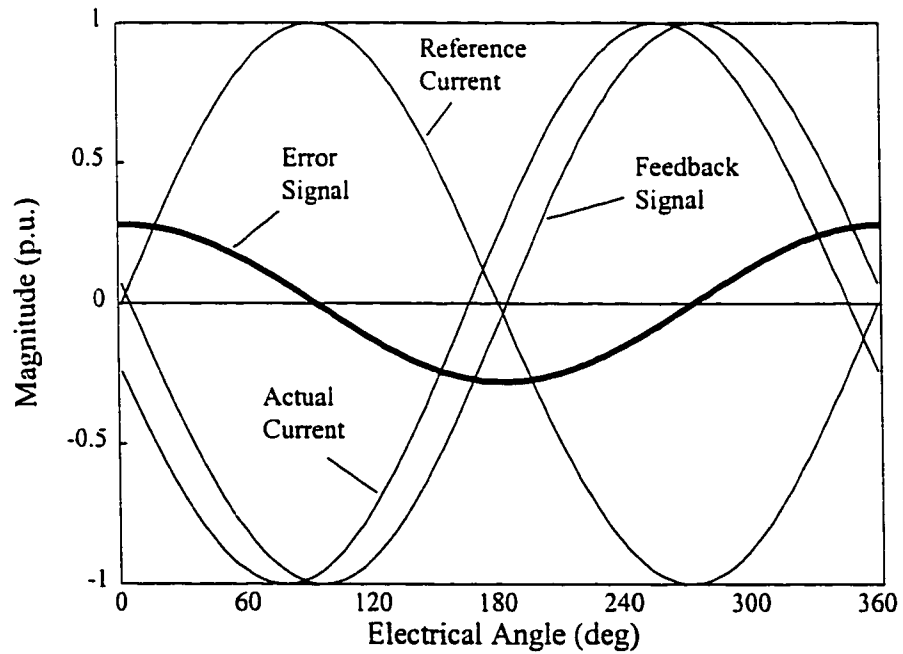


Figure 5.9 Error signal generation: summation error method

Error PID Control and Gain Adjust

The simulated error signals in Figures 5.8 and 5.9 are manipulated to alter the response of the error- Δ current controller. It is often recommended that a PI controller is added ahead of the triangle comparison [28]. Addition of proportional error gain provides a closer tracking between the feedback signal and the reference current. Figure 5.10 shows the influence of adding Integral (I), and Derivative (D) gain to the error signal.

Integral gain will create additional delay in the error signal and will effectively reduce the tracking capability of the controller. Integral delay is not necessary for this implementation of the error- Δ current controller, as the filtered feedback signals already contain enough attenuation and delay to provide high frequency roll-off capabilities. Figure 5.10 shows that adding derivative gain advances the error signal to the left, which in turn causes the feedback and actual phase current signals to also shift to the left. The

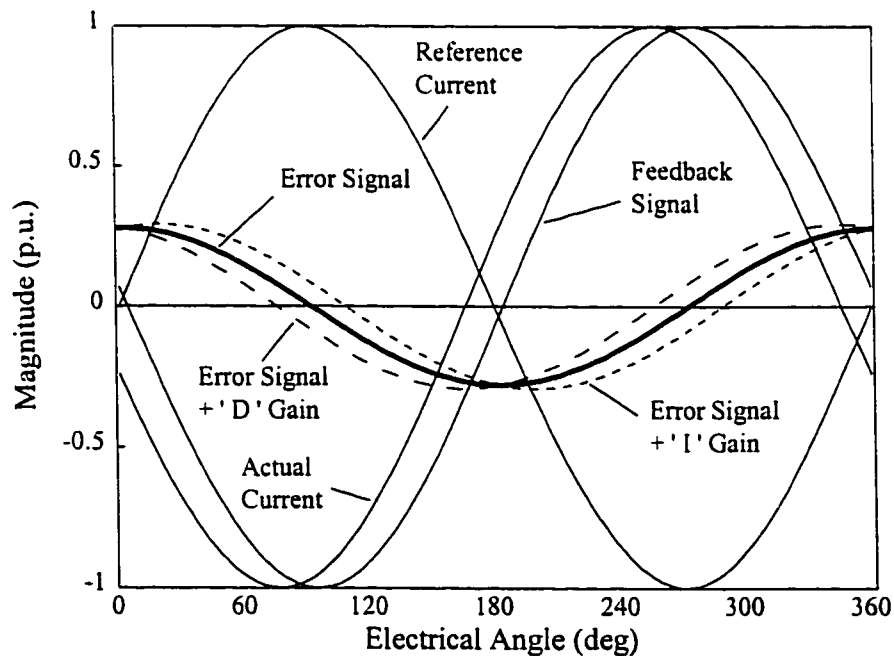


Figure 5.10 Integral 'I' and Derivative 'D' gain influence on error signal generation

addition of derivative gain to the error signal provides a means to counteract the current controller delay and enforce the tight adherence of the filtered feedback signal to the reference current. Tight adherence to the reference current provides the capability to predict the actual phase current angle through knowledge of the reference current angle and (5.2). Hence, control of the current vector angle δ is achieved through a simple manipulation of the reference current phase angle.

A separate error gain circuit with proportional and derivative gain is implemented for each phase of the error- Δ current controller. Shielding and noise reduction techniques are used throughout the constructed circuitry. The proportional and derivative gains are manually adjusted for each phase to provide the desired measured phase current response. The adjustment process begins with a minimum proportional gain setting of 2 and a derivative gain of 0. Proportional gain is increased until a desired phase current response is achieved. The derivative gain is then increased to reduce the phase error between the feedback signal and the reference current. A schematic diagram for the proportional and derivative error gain and adjust circuits is provided in the supplementary document for this thesis.

Error- Δ Switching Circuit

The post PD gain error signals are modulated with a triangle wave. A 10 kHz triangle wave oscillation frequency is chosen to provide a high frequency switching component that can easily be filtered out with a 1941 Hz cutoff frequency Butterworth filter. The oscillation frequency is not increased beyond 10 kHz to avoid additional RF emission interference. Figure 5.11 shows the switching patterns developed when the post PD gain error signal for phase 'A' is modulated with a triangle wave. Error signals greater than the trian-

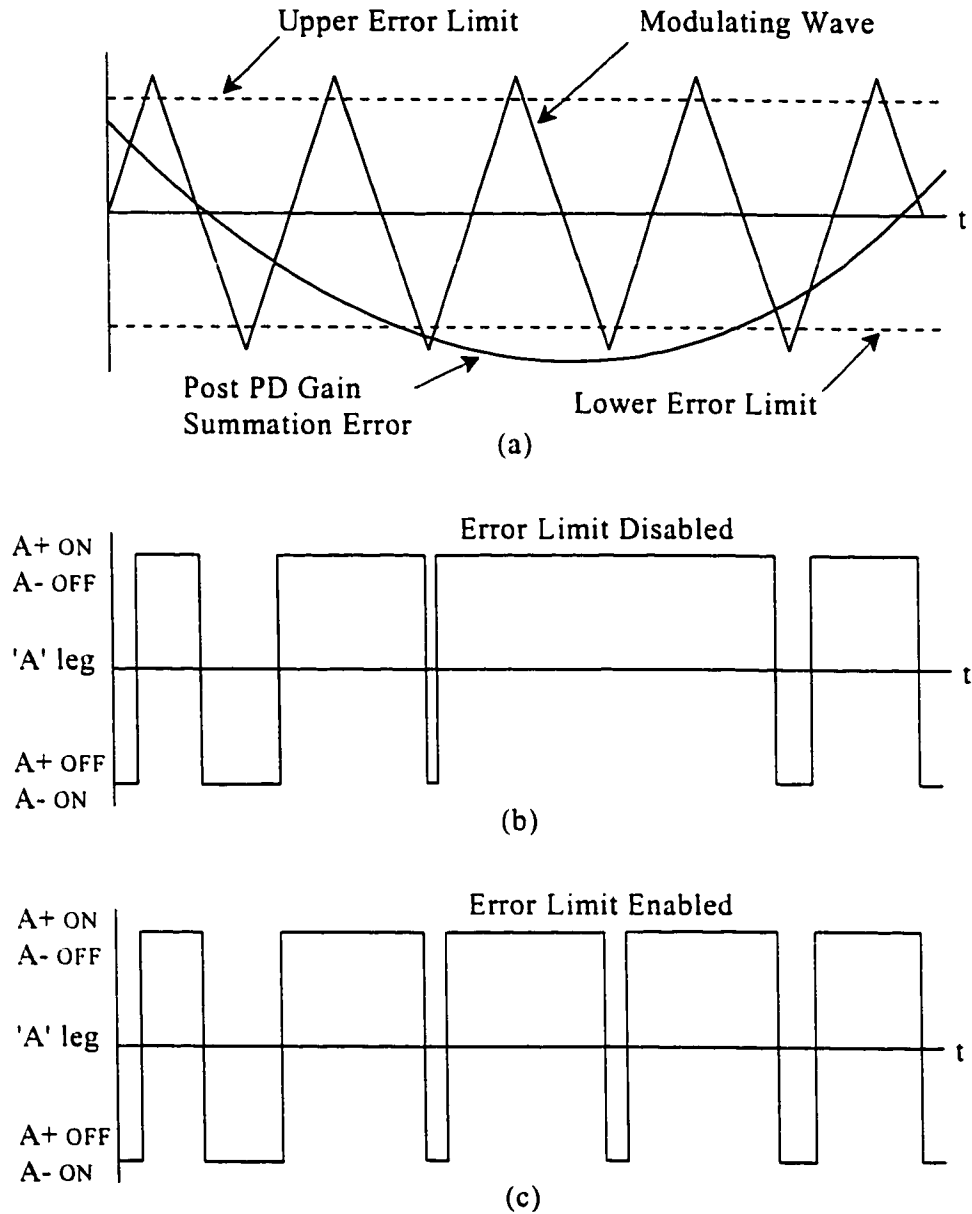


Figure 5.11 VSI phase 'leg' switching pattern generation

gle waveform produce a negative phase 'A' leg switching command so that the actual phase current is forced in the negative direction. The summation error is reduced as both the actual phase current and the inherently delayed feedback signal become more negative. Error signals that are less than the triangle waveform produce a positive phase 'A' leg

switching pattern so that the phase current and the summation error is increased.

An artificial error-gain limit is used to limit the maximum value of the error signal. Figure 5.11 (a) shows the location of such error signal limits. The error signal limits guarantee that each side of the VSI phase 'leg' is switched once per cycle of the 10 kHz triangle modulating wave. Error-gain limiting avoids the pulse-dropping phenomenon experienced with non-error-gain limiting, as illustrated in (b) and (c) of Figure 5.11. Pulse dropping can produce distortions in the low pass filtered feedback signals as lower frequency switching components are added to the pre-filtered phase current.

An error-gain limit circuit is included in the error- Δ switching circuit for this high performance drive. The error gain limit circuit can be disabled through in-circuit dip switches. Lockout and dead-time circuits are used to guarantee that the switching signals to a phase 'leg' of the inverter will not command both sides of the inverter to be on at the same time. Shoot through faults are avoided through logic circuitry that maintains the minimum time between the 'off' command of one side of a phase 'leg' and the 'on' command of another side of a phase leg at 1.8 μ s. Shielding and noise isolation techniques, that were discussed in Chapter 4, are used throughout the error- Δ switching circuit. Phase 'leg' firing signals produced by the switching circuits are interfaced to the IGBT gate drivers of the VSI. Schematic diagrams of the error- Δ switching circuits and their interface to the VSI are provided in the supplementary document to this thesis.

5.4 ANALOG REFERENCE CURRENT GENERATION

5.4.1 PWM to Analog Signal Conversion

The modified microprocessor control strategy, proposed in Section 5.1.3, specifies the use of a high performance microcontroller to calculate and generate self-synchronized reference current waveforms. Analog reference current waveforms are required as inputs to the error- Δ current controller. A PWM output is used to convert the digital reference current values into an analog form as indicated in Figure 5.2.

The 80C196KD-20 microcontroller, investigated in [11, p.56], provides three PWM outputs as well as serial and parallel port functions. A summarized list of specifications for the 80C196KD-20 microcontroller is provided in Appendix A. The microcontroller's parallel ports are required for the rapid interface shared memory function. Serial transmission of the digital reference current values consumes 63 μ s for each point. The PWM outputs repeat every 25.6 μ s, or at a rate of approximately 39 kHz. Pulse width modulation outputs operate independently and do not steal processing time from the microcontroller program code execution. A 39 kHz repetition rate translates into the capability of 125 PWM updates per electrical cycle at 9375 rpm PMSM operation. An 8000 rpm resolution of 125 points per cycle for all three phases is well within the capabilities of the 80C196KD-20 microcontroller.

A pulse width modulated signal is converted to an analog signal through the use of a low pass filter. Figure 5.12 shows the filtering strategy required to convert the microcontroller PWM signals to analog current reference signals. A reference current waveform generation algorithm calculates the desired self-synchronized reference current wave-

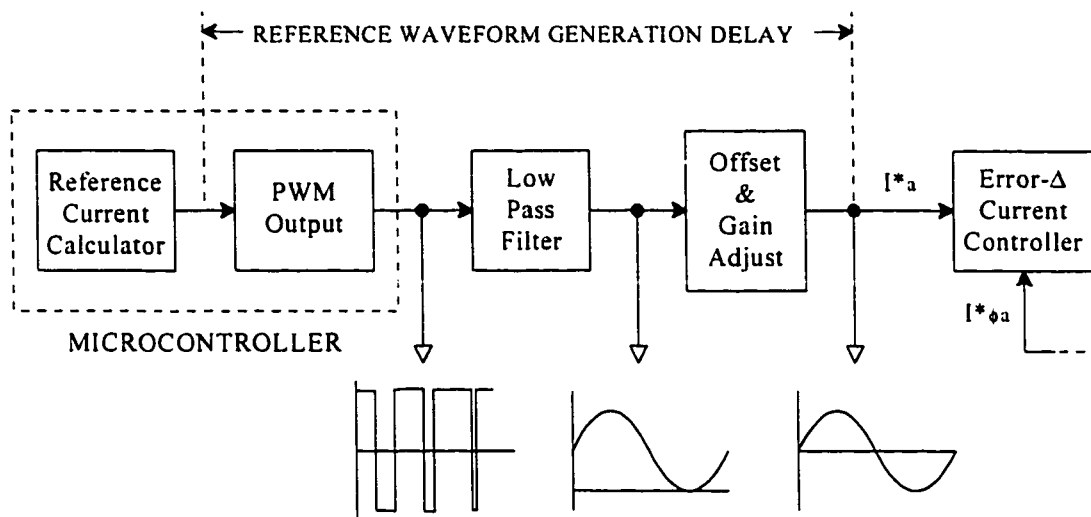


Figure 5.12 Reference current waveform generation and filtering

form magnitudes and writes these values to the microcontroller PWM generation registers. The microcontroller's internal PWM circuitry produces the corresponding PWM signals at its three PWM outputs. Signals from the PWM outputs are low pass filtered into their analog form. The 1941 Hz cutoff frequency Butterworth filters, described in Section 5.3.2 and used to filter the feedback signals, are ideal for filtering the 39 kHz PWM signals. Filtered phase current reference waveforms are applied to an offset and gain adjust circuit to adjust the dc offset to zero and amplify the maximum possible reference current magnitude to approximately 10V. A resolution of 78 mV, or approximately 0.4 % of the maximum peak-to-peak value, is obtained from the microcontroller's 8-bit PWM ports.

The analog reference current signal is applied directly to the error- Δ current controller. Reference current signal frequency varies between 117 and 267 Hz for a 4-pole PMSM operation between 3500 and 8000 rpm. A unity gain is assumed for this frequency range, as illustrated in Figure 5.6. Hence, a 10 V maximum peak value reference current waveform produces a 28 Arms phase current for previously described feedback current in

Section 5.3.2. A schematic for the PWM interface and circuitry between the microcontroller and the error- Δ current controller is provided in the supplementary document for this thesis.

5.4.2 Reference Waveform Delay and Delay Measurement

A phase angle delay is present during reference waveform generation, as is shown in Figure 5.12. The reference waveform delay is assumed to change linearly with frequency and consists of the summation of the digital-to-PWM conversion delay, the Butterworth filter phase angle delay, and the reference current adjust and offset circuitry delay. Reference waveform delay is compensated for by simply phase advancing the microcontroller calculated reference waveform by an angle equal to the delay.

Delay measurement is conducted by commanding the microcontroller to produce a self-synchronized 125 point reference current waveform. The PMSM is coupled to a conventional dc machine and driven at speeds of up to 8000 rpm. The marker signal from the PMSM rotor mounted position encoder triggers the start of the cycle so that the microcontroller commands a 0 magnitude reference waveform at the 0 electrical degree marker position. An oscilloscope is used to display the marker and the actual analog reference current waveform I_a^* . The observed difference between the marker signal and the measured reference current waveform is equal to the reference waveform delay and is illustrated in Figure 5.13 (a).

The reference waveform delay is adjusted to zero by phase advancing the calculated reference current by the compensation angle θ_c , as shown in Figure 5.13 (b). The compensation angle is variable in 2.88° steps, corresponding to the 125 point waveform

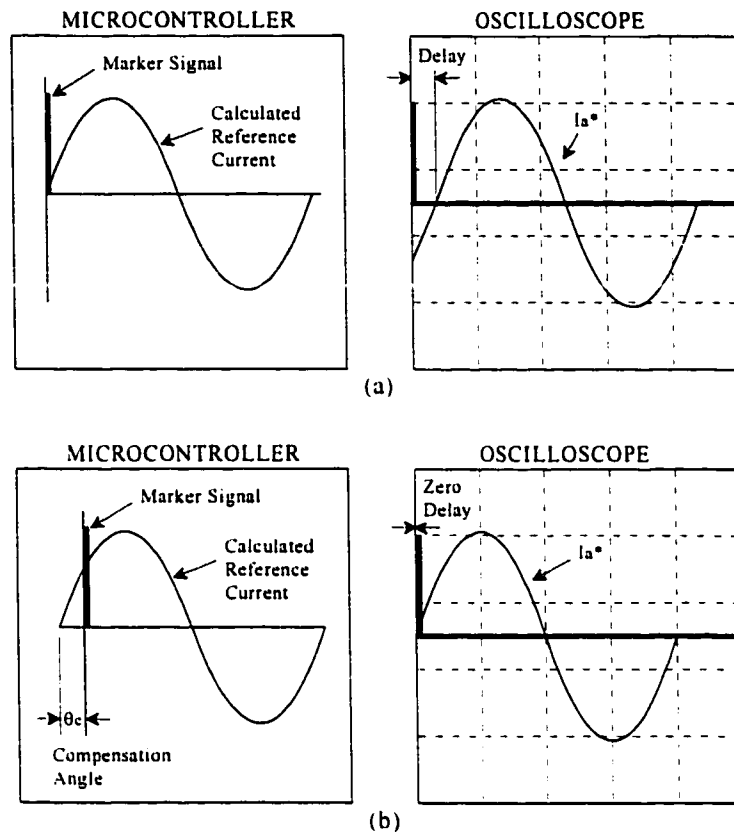


Figure 5.13 Reference waveform delay compensation

Table 5.2
Microcontroller Compensation Angle

Speed (rpm)	Compensation Angle (elec. deg.)
500	2.88
1000	5.76
2000	8.64
3000	11.52
4000	14.40
5000	17.28
6000	20.16
7000	23.04
8000	25.92

resolution. Table 5.2 lists the required compensation angle values that provide a near zero delay in the analog reference current waveform I_a^* for a 500 to 8000 rpm operating range. Reference waveform delays are assumed to be identical for all three phases. Hence, Table 5.2 provides a means to adjust the microcontroller calculated reference waveforms to allow for the accurate vector control of the analog reference current waveforms relative to the marker signal.

5.4.3 Actual Analog Reference Waveform Harmonic Content

Low harmonic content sinusoidal current waveforms are required for the high efficiency operation of a PMSM. The proposed high performance drive can generate sinusoidal low harmonic phase currents only if the reference current waveforms are also sinusoidal with a low harmonic content. Figure 5.14 shows the actual self-synchronized analog reference waveform I_a^* applied to the error- Δ current controller over one revolution of the PMSM rotor at an 8000 rpm rotor speed. Visual analysis of Figure 5.14 reveals that it is possible to

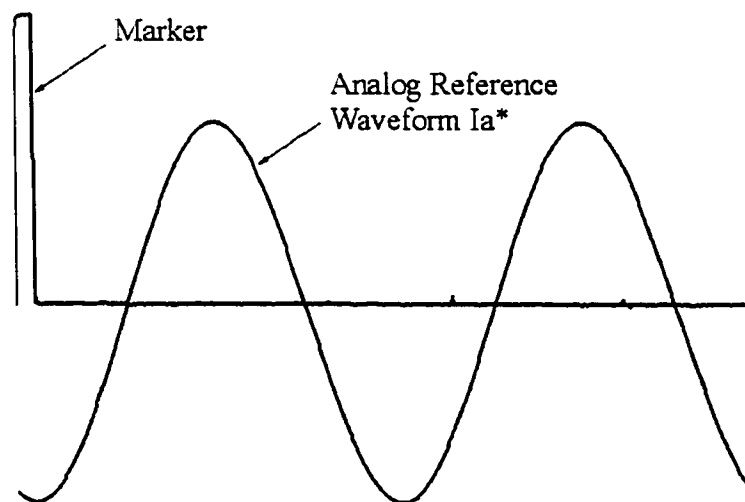


Figure 5.14 Actual analog reference waveform at 8000 rpm

Table 5.3
Reference Waveform Harmonic Content

PMSM Speed (rpm)	Harmonic Content			
	Fundamental	2nd Harmonic	3rd Harmonic	4th Harmonic
8000	100 %	1.00 %	0.27 %	0.04 %
4000	100 %	0.48 %	0.18 %	0.03 %
2000	100 %	0.22 %	0.08 %	0.01 %

generate low harmonic content, higher frequency waveforms using the high performance microcontroller and PWM to analog conversion method described in this section.

A harmonic analysis of the reference current waveforms for different PMSM rotor speeds yields the data for Table 5.3. The harmonic content of the waveforms are listed as a percentage of the fundamental. The tabulated results verify that the proposed reference current generation technique is very successful in generating negligible harmonic sinusoidal reference current waveforms.

5.5 MICROCONTROLLER IMPLEMENTATION

The previous section has detailed the high performance microcontroller PWM to analog reference current signal conversions. This section describes the methodology, software, and circuitry required by the microcontroller to implement the generation of a 3-phase set of self-synchronized, variable amplitude, variable phase angle, vector controllable reference current waveforms. Thorough optimization of the microcontroller implemen-

tation has been performed to enhance the execution speed of the waveform generation process. Near full utilization of the 80C196KD-20 microcontroller resources is required to generate the reference current waveforms necessary for 8000 rpm PMSM operation.

5.5.1 Microcontroller Port Reconstruction

The modified high performance microprocessor controlled PMSM drive system, illustrated in Figure 5.2, employs shared memory between a DSP or Microprocessor and the microcontroller used to generate the reference current waveforms. The shared memory is used solely to store the values of the reference current magnitude I_{mag}^* and phase angle I_a^* in a 16-bit word calculated by the DSP or Microprocessor. Ports 3 and 4 of the 80C196KD-20 microcontroller provide rapid 16-bit parallel I/O that is ideal for the implementation of the shared memory function for this high performance drive. The 80C196KD-20 uses a multiplexed address bus (AD0-AD15) that shares pins with the I/O ports 3 and 4. Ports 3 and 4 are read at the memory locations 1FFEh and 1FFFh when the ports are enabled and operated as bus pins.

Ports 3 and 4 are reconstructed using the simple bus transceiver shown in Figure 5.15. The port input values are buffered using two octal three-state buffers which are interfaced with the octal transparent latches used to demultiplex the address bus. Logic circuitry on the address bus is used to generate the $\text{-ADDR} = P3, P4$ signal. Ports 3 & 4 are enabled only when the address lines contain the address of either port 3 (1FFEh) or port 4 (1FFFh) and the microcontroller read signal (-RD) is LO. The full schematics of the circuitry used to reconstruct ports 3 & 4 is provided in the supplementary document for this thesis. Addi-

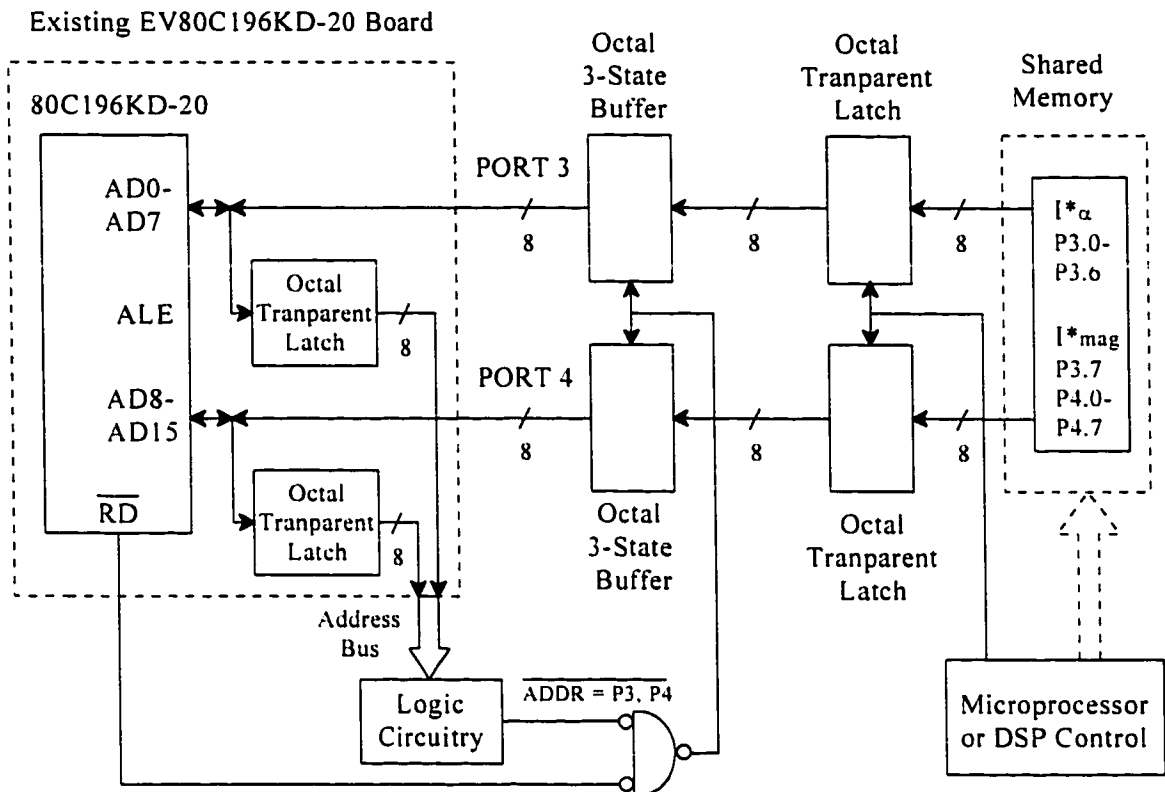


Figure 5.15 Port 3 & 4 reconstruction for shared memory inputs

tional information on the ports and timing of the 8096 series of microcontrollers is obtained from the Intel manuals listed as references in this thesis.

Shared memory values of I^*_α and I^*_{mag} are latched to the reconstructed ports. The port values are read by first writing all '1's to the ports to place them in the high impedance mode. Microcontroller memory location 1FFEh is then read and stored as a word value into an internal register. The internal register is separated according to the bit-length of the variables written to ports 3 & 4. A 7-bit value for I^*_α is required for the phase control of a 125 point waveform. The remaining 9-bit block is used to store the value for I^*_{mag} . Different assignments for the 16-bit shared memory are possible by simply changing the microcontroller code. Ports 3 and 4 are read once per electrical cycle of the microcontroller

generated reference waveforms. The timing between the microcontroller reading of ports 3 & 4 and external changes to the port values does not need to be synchronized, as changes to I_a^* and I_{mag}^* occur at a much slower rate than the frequency of the reference current waveforms required for high speed PMSM operation.

5.5.2 Microcontroller Algorithm Design and Implementation

Self-synchronization

The shaft position encoder used in this investigation provides two channels, A and B, with a resolution of 1250 pulses per mechanical revolution, or 625 pulses per electrical cycle of the 4-pole PMSM. A third channel provides one marker pulse for each mechanical revolution. Specifications for the shaft position encoder are found in Appendix A. Self-synchronization of the microcontroller generated 125 point sinusoidal reference waveforms is accomplished by counting 5 channel A pulses before generating the next point on the sine waves. Reference waveforms generated in this manner are always synchronized in frequency with the speed of the PMSM rotor. The marker pulse is used for re-synchronization once per revolution in case noise or a spurious logic error has created a miscount in the channel A pulses.

The 80C196KD-20 has a high speed input pin (HSI.1) that is configured through software to trigger an on-board timer called TIMER2. Channel A position pulses are applied to the enabled HSI.1 pin and TIMER2 is assigned the task of setting the high speed output pin (HSO.1) to logic 1 when its value reaches 5. Software monitoring of the HSO.1 pin determines the instant when 5 channel A pulses have occurred. A logic 1 detected on

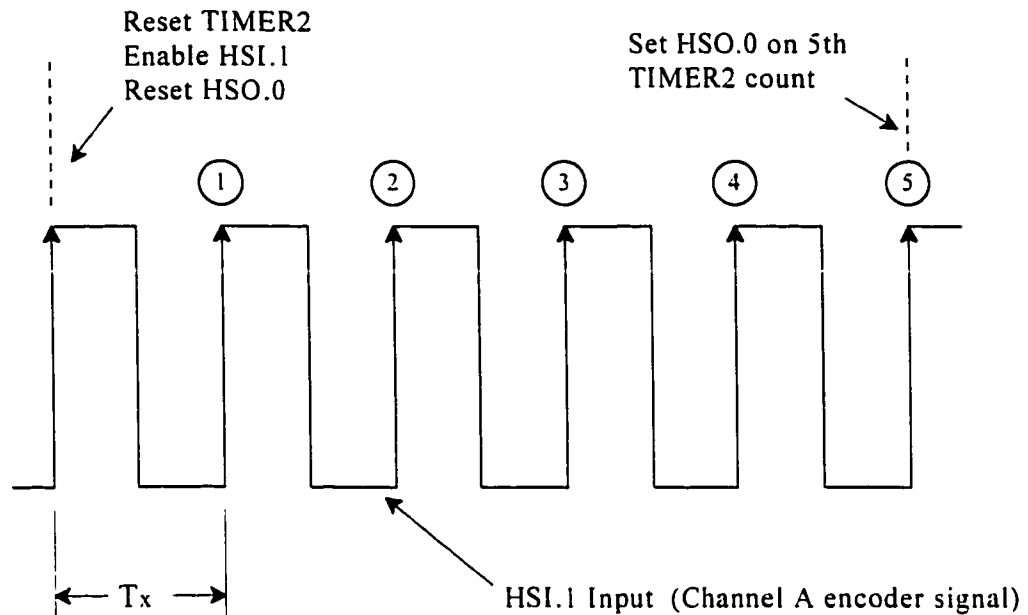


Figure 5.16 Self-synchronization timing

the HSO.1 pin signifies that it is time to generate another point on the reference waveforms. The HSO.1 pin is reset to logic 0, Timer 2 is cleared, and the HSI.1 pin is re-enabled. The process is repeated to provide accurate synchronization of the reference waveform generation with the PMSM rotation. Figure 5.16 shows the timing of the self-synchronization process relative to the channel A pulse train. The setting of HSO.0, clearing of TIMER2, and re-enabling of HSI.1 must be accomplished within the minimum period of T_x to avoid a timing error. The minimum period of T_x is $6 \mu\text{s}$ at an 8000 rpm PMSM rotor speed.

The marker signal is applied to the 80C196KD-20 external interrupt EXTINT1. A rising edge in the marker signal produces a microcontroller interrupt causing the main program execution to halt. The Interrupt Service Routine (ISR) is executed to reset the position of the reference current waveform according to the value of phase angle I^*_α specified in the shared memory. Ideal operation of the microcontroller results in a position reset to the

point that the main program is currently generating. Main program execution continues from its last instruction once the ISR is complete. Marker re-synchronization ensures that noise-induced synchronization errors will not affect more than one rotor revolution of the PMSM.

Waveform Calculation

The microcontroller employs a look-up table to determine the values of the reference current waveform. A look-up table eliminates the need to calculate the sine wave, thereby saving valuable processing time. The 125 point waveforms stored in the look-up table correspond to an angle resolution of 2.88° . The look-up table is pre-calculated to contain the absolute values of $\sin\theta$ and $\cos\theta$ for θ varying from 0 to 360° in 2.88° steps. Figure 5.17 graphically illustrates the contents of the look-up table. Reference waveform

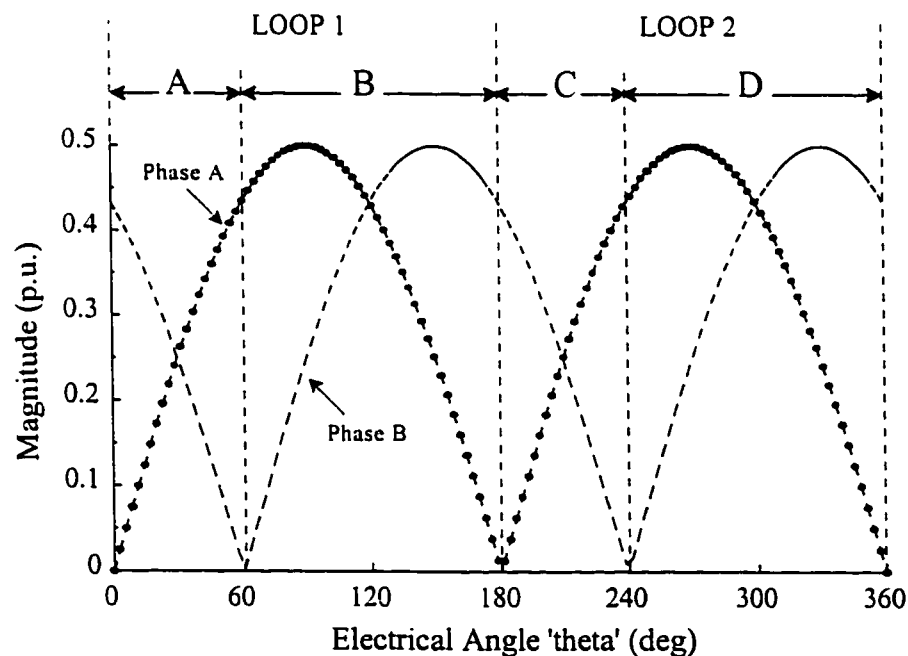


Figure 5.17 Phase A and B reference waveform look-up table values

generation is performed according to two separate loops. Loop 1 is executed for theta values corresponding to a positive phase A reference waveform, while Loop 2 is executed for theta values corresponding to a negative phase A reference waveform. Each of the two loops is broken into two additional sections corresponding to theta values for which the phase B reference waveforms are positive and negative.

Section A of Loop 1 contains the values of θ where both phase A and B reference waveforms are positive. The reference waveform values, corresponding to the current value of theta, are read from the look-up table and scaled according to the value of I_{mag}^* read from the shared memory. An offset of 0.5 p.u. is added to both of the reference waveforms to provide a fixed dc offset in the post-filtered PWM output. Phase C of the balanced three phase reference waveforms is calculated from phases A and B through knowledge that the summation of all three waveforms must equal 1.5 p.u. Section B of Loop 1 contains the values of θ where phase A is positive and phase B is negative. Generation of reference current waveforms for a theta value in section B follows the same methodology as in section A, except that the phase B reference waveform is subtracted from, rather than added to, the 0.5 p.u. offset.

Section C in Loop 2 contains the values of θ where both phase A and B reference waveforms are negative. The magnitude adjusted waveforms in section C are both subtracted from 0.5 p.u. Section D contains the θ values that require a negative phase A and positive phase B reference waveform generation. Magnitude adjusted reference waveform values for phase A are subtracted from 0.5 p.u., while phase B values are added to 0.5 p.u.

The value of θ is reset to zero after the generation of the reference waveforms

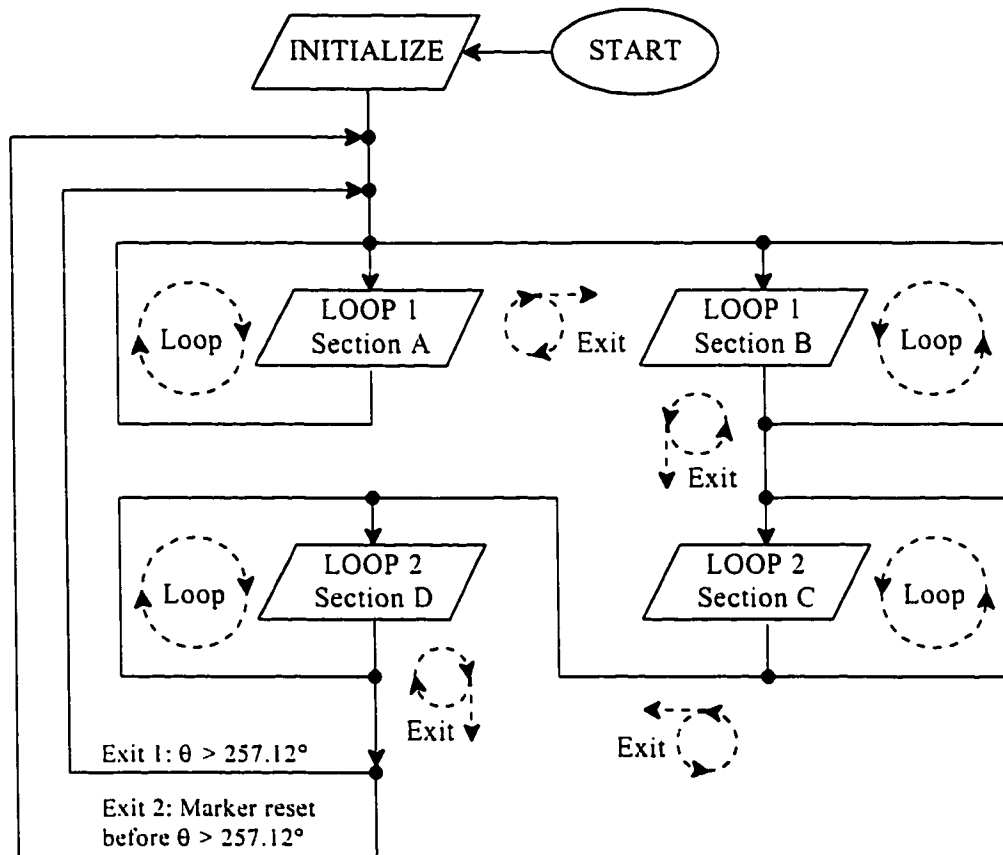


Figure 5.18 Microcontroller code condensed flowchart

corresponding to $\theta = 357.12^\circ$. Reference waveform generation is continuous and is only interrupted by the marker signal re-synchronization procedure described previously. Figure 18 shows the condensed flowchart of the microcontroller code written to perform the desired reference waveform generation. The full flowchart for the microcontroller code, with execution times (in state times), is provided in Appendix B. The actual ASM-96 code is listed in the supplementary document for this thesis.

Performance Evaluation and Predicted Improvements

The 80C196KD-20 requires $0.1 \mu\text{s}$ to execute one state time. A maximum of 60 state times can be executed during the $6 \mu\text{s}$ Tx at 8000 rpm. Table 5.4 summarizes the state

Table 5.4
Required State Times for Code Execution

LOOP EXECUTION	STATE TIMES FOR CODE EXECUTION DURING Tx	STATE TIMES FOR REMAINING CODE EXECUTION	TOTAL REQUIRED STATE TIMES
LOOP 1: Section A - Loop	44	191	235
LOOP 1: Section A - Exit	52	187	239
LOOP 1: Section B - Loop	52	187	239
LOOP 1: Section B - Exit	49	187	236
LOOP 2: Section C - Loop	44	191	235
LOOP 2: Section C - Exit	44	207	251
LOOP 2: Section D - Loop	44	207	251
LOOP 2: Section D - Exit 1	44	203	247
LOOP 2: Section D - Exit 2	44	202	246

times required to execute the individual sections of code that correspond to the various paths in Figure 5.18. The code execution is broken into the state times required to be executed in Tx of Figure 5.16, and the state times required to be executed after Tx but before the 5th rising edge of the encoder signal. Figure 5.19 graphically illustrates the resource utilization of the 80C196KD-20 microcontroller during the generation of reference waveforms at an 8000 rpm rotor speed.

The Figure 5.19 illustration indicates that the 80C196KD-20 is operating at 87 % of its maximum capability when generating reference current waveforms at 8000 rpm PMSM rotor speeds. Code execution in the Loop 1 section A exit, and the section B loop, represent

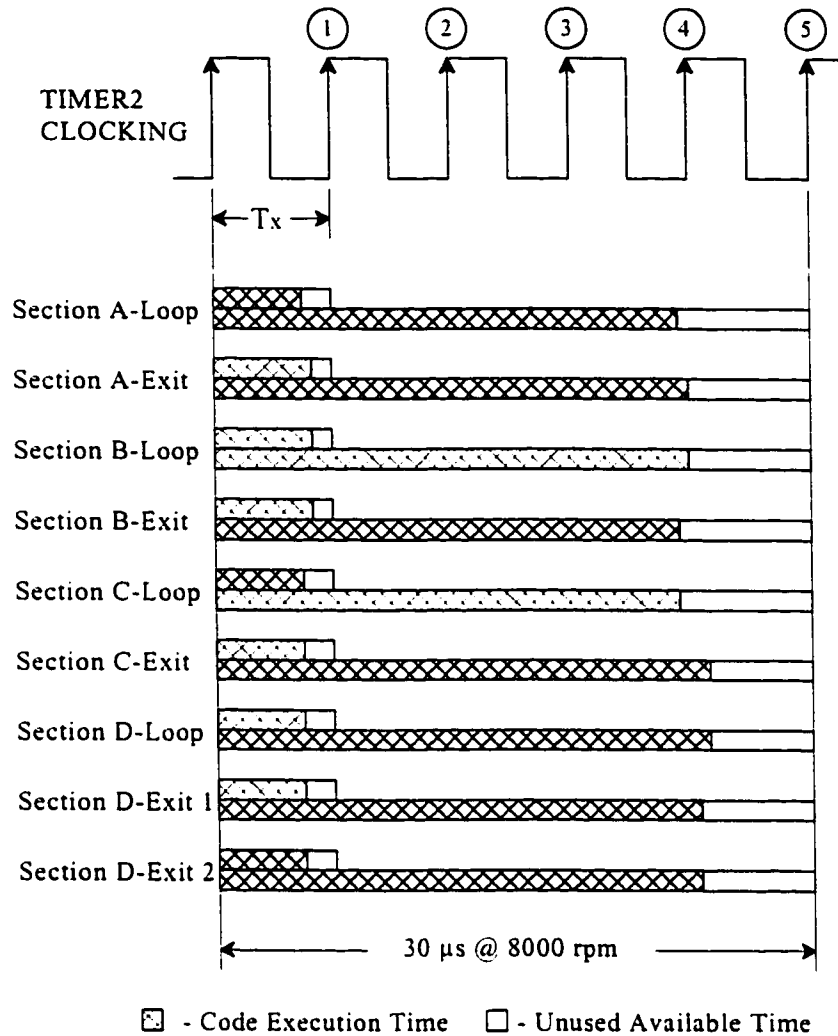


Figure 5.19 Resource utilization of 80C196KD-20 at 8000 rpm PMSM rotor speed

the critical code sections. Reference waveform generation at a rotor speed of up to 9320 rpm is possible when using the microcontroller and code implemented for this high performance drive. The code execution state times in Table 5.4 are for the optimized code and little to no further performance improvements are possible through microcontroller code refinement. A 40 MHz version of the same microcontroller can be used to increase the speed of the reference current waveform generation. State time execution will be twice as fast and the maximum allowed rotor speed can be increased to 18 460 rpm. The channel A

pulse train can be divided by 5 so that a new point on the reference waveform is generated each time the TIMER2 count reaches 1. The rotor speed can be increased since the execution of 52 state times in the Tx period is no longer required. A decrease in the reference waveform resolution will also enable a higher PMSM rotor operating speed. A 90 point reference wave (4° spacing) will allow for a 12 820 rpm rotor operation with the current microcontroller used for this high performance drive.

The analog reference current generation method described in this section provides error free, self-synchronized, phase angle and magnitude adjustable sinusoidal waveforms to the error- Δ controller of this high performance drive. Table 5.5 lists the maximum al-

Table 5.5
Reference Waveform Generation
Performance Improvement Options

Option #	Performance Improvement	Maximum Allowed Rotor Speed (rpm)
1	None	9230
2	Divide channel A pulses by 5	9561
3	Use 90 point reference waves	12 820
4	Use a 40 MHz microcontroller	18 461
5	Option 2 & 3	13 280
6	Option 2 & 4	19 123
7	Option 3 & 4	25 641
8	Option 2 & 3 & 4	26 560

lowed rotor speeds that will produce error free 3-phase reference current waveform generation for the various performance improving options. The maximum stated 26 560 rpm rotor speed indicates that only a few simple modifications to this unique high performance drive will provide an 828 % increase in the energy storage capabilities of the proposed FESS.

5.6 CURRENT CONTROL PERFORMANCE TESTING

A snapshot of the feedback and reference current waveforms for phases A and B are shown in Figure 5.20. Operational tests of the high performance drive are used to examine and tune the response of the actual phase current to changes in the commanded reference current. A BLM4035 PMSM is connected to the VSI and the 1250 ppr shaft position encoder is mounted on the BLM4035. Manufacturer supplied specifications for

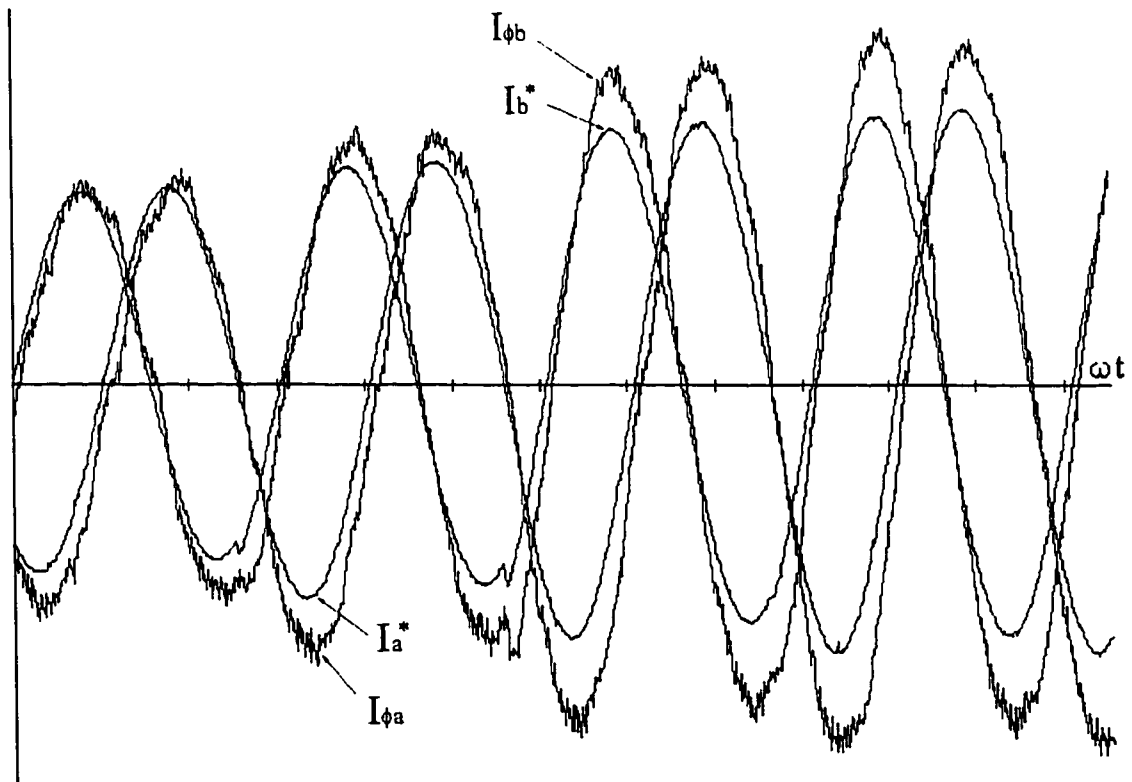


Figure 5.20 Actual reference and feedback current waveforms at 6000 rpm

the BLM4035 PMSM used in this investigation are provided in Appendix A. A bank of dip-switches is used to manually set the values of the I_{α}^* and I_{mag}^* shared memory inputs to ports 3 & 4 of the microcontroller. The PMSM is operated at a steady state before a step increase in the value of I_{mag}^* is applied. Application of a step increase in the reference current waveform produces a response such as the one shown in Figure 5.19. The error- Δ current controller P and D gains are adjusted to provide a rapid response and a small tracking error between the reference and feedback waveforms. A proportional gain of approximately 4 and a small derivative gain provide a desirable current controller performance. The gains are fixed for the PMSM and readjustment is needed only if a different PMSM is connected to the current controller.

The work so far has described the development and implementation of a high performance drive that can be used to successfully operate a PMSM at speeds up to 8000 rpm. Manual control of the reference waveform magnitudes I_{mag}^* and phase delay I_{α}^* is used to position the actual phase current relative to the PMSM encoder marker signal. High performance vector control requires a microprocessor interface with the shared memory input to the microcontroller to provide automatic current vector control capabilities. The remainder of this chapter focuses on the implementation of the required resources for automatic current vector control.

5.7 MICROPROCESSOR INTERFACE

5.7.1 The Peripheral Interface Adapter

A 486DX-2, 66 MHz, PC is used to provide the 'DSP or Microprocessor' and the

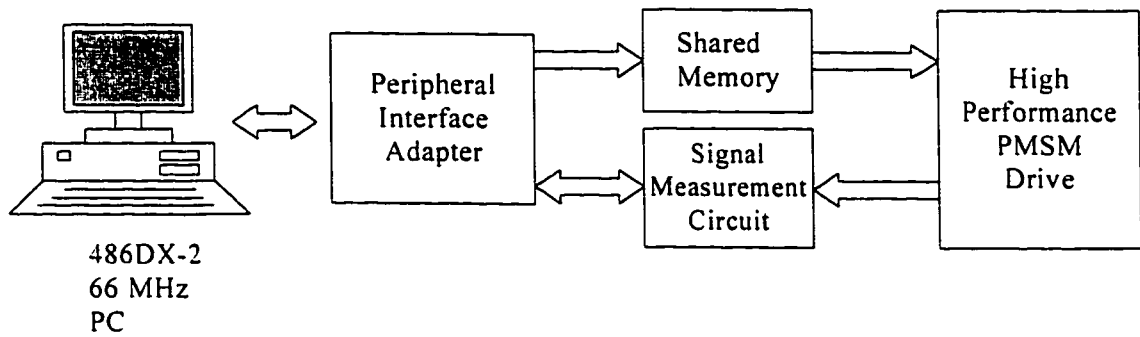


Figure 5.21 PC interface through the Peripheral Interface Adapter

'Display & Data Storage' functions of the Figure 5.2 block diagram. The PC is interfaced to the high performance drive system through a peripheral interface adapter (PIA), as shown in Figure 5.21. The PIA is used as a means to perform rapid data transfer between the PC and the high performance drive system. Software on the PC uses the PIA to control the measurement of the PMSM true-rms phase current, true-rms phase voltage, true-rms phase power, and rotor speed. Measured values are read into the PC memory through the PIA. Reference waveform phase angle I_{α}^* and magnitude I_{mag}^* values calculated by the PC software are written to the shared memory block through the PIA.

The PIA is constructed by creating a 24-bit bidirectional port that is interfaced directly with the 62-pin PC bus. A PC-slot plug in card holds the PIA circuit and a 25-pin D-sub connector provides an external cable connection to which the shared memory and signal measurement circuits are interfaced. The block diagram for the construction of the PIA is shown in Figure 5.22. Logic circuitry is used on the address lines of the PC bus to decode the address of the PIA port. The PIA port is set to occupy the unused PC low memory address space 3ECH to 3EFH. Port information is read and written to the PC data bus through the use of a bus transceiver and an 8255A dedicated parallel I/O interface

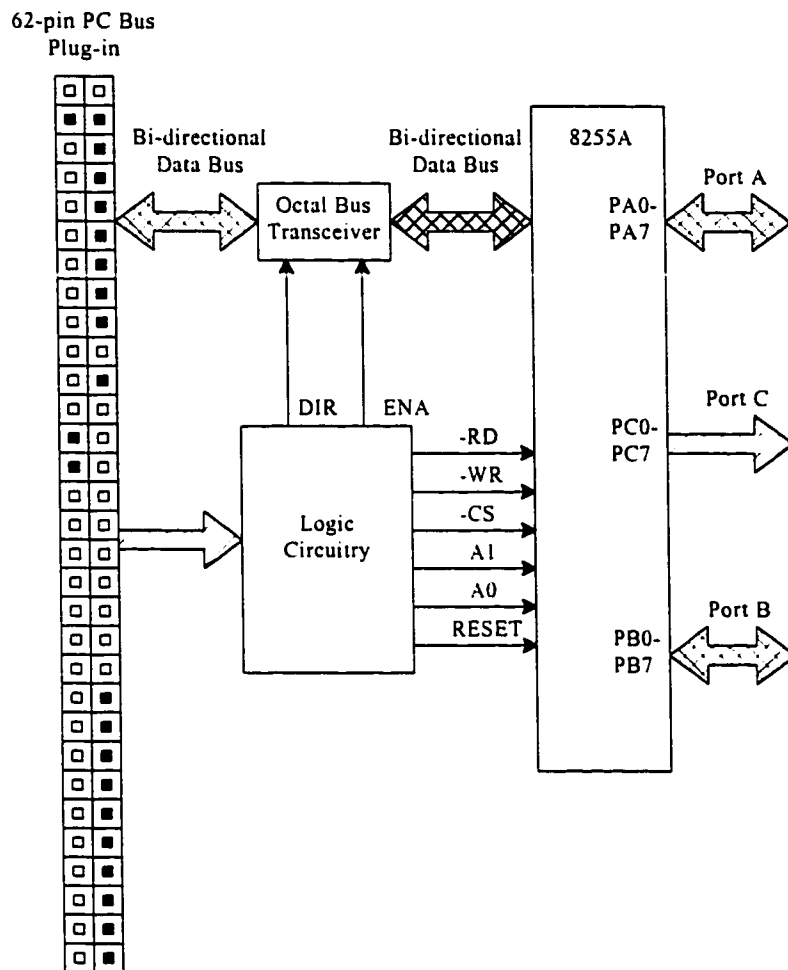


Figure 5.22 Peripheral Interface Adapter block diagram

adapter. The 24 bits of the PIA port are divided into three separate 8-bit bidirectional ports, A, B, and C. Ports A, B, and C occupy the memory locations 3ECH, 3EDH, and 3EEH respectively. The control register for the functionality configuration of the 8255A port occupies the memory location 3EFH.

The truth table for Figure 5.22 is listed in Table 5.6. Bus lines A1 and A0 are used to address the 8255A and select either of the three ports or the control register. The read line -RD is used to send data along the data bus from the 8255A to the CPU when enabled with a 'LO'. Writing data from the CPU to the 8255A ports requires that the write line -WR

Table 5.6
Peripheral Interface Adapter Truth Table

A1	A0	-RD	-WR	-CS	OPERATION
0	0	0	1	0	Read Port A to the data bus
0	1	0	1	0	Read Port B to the data bus
0	0	1	0	0	Write the data bus to Port A
0	1	1	0	0	Write the data bus to Port B
1	0	1	0	0	Write the data bus to Ports C
1	1	1	0	0	Write the data bus to the Control Register
X	X	X	X	1	All ports as high impedance outputs

is enabled with a 'LO'. Communication between the CPU and the 8255A is enabled with a 'LO' on the -CS line. A 'HI' on the RESET line clears the control register and sets all of the ports to the input mode.

Ports A and B of the PIA are configured to operate in a bidirectional manner to write values of I_{α}^* and I_{mag}^* to the shared memory microcontroller interface, and to read the measured speed, phase current, phase voltage, and average phase power into the CPU. Port C is used as an output port to control the bidirectional 16-bit bus connected to Ports A and B, and to control the timing and reading of the measured values from the signal measurement circuit. The writing of data to the ports is performed through the PC software by first making sure that the ports are configured for output, and then writing the desired 8-bit value to the memory location corresponding to the port being written to. Ports A, B, and C are configured as outputs by writing 80H to the control register at memory location 3EFH.

Reading from Ports A and B is conducted by first verifying that those ports are configured as inputs, and then reading the desired 8-bit value from the memory location corresponding to the port being read. Reconfiguration of Ports A and B as inputs, and Port C as an output, is performed by writing 92H to the control register at memory location 3EFH. Alternate port re-configurations are available by writing different values to the control register [29]. A full schematic diagram of the PIA circuitry is provided in the supplementary document to this thesis.

5.7.2 Communications Control

A common data bus is used to transfer the data to and from ports A and B. The transfer of data is controlled through the PC software and Port C. Figure 5.23 shows the control configuration for the communications between the PC, the shared microcontroller

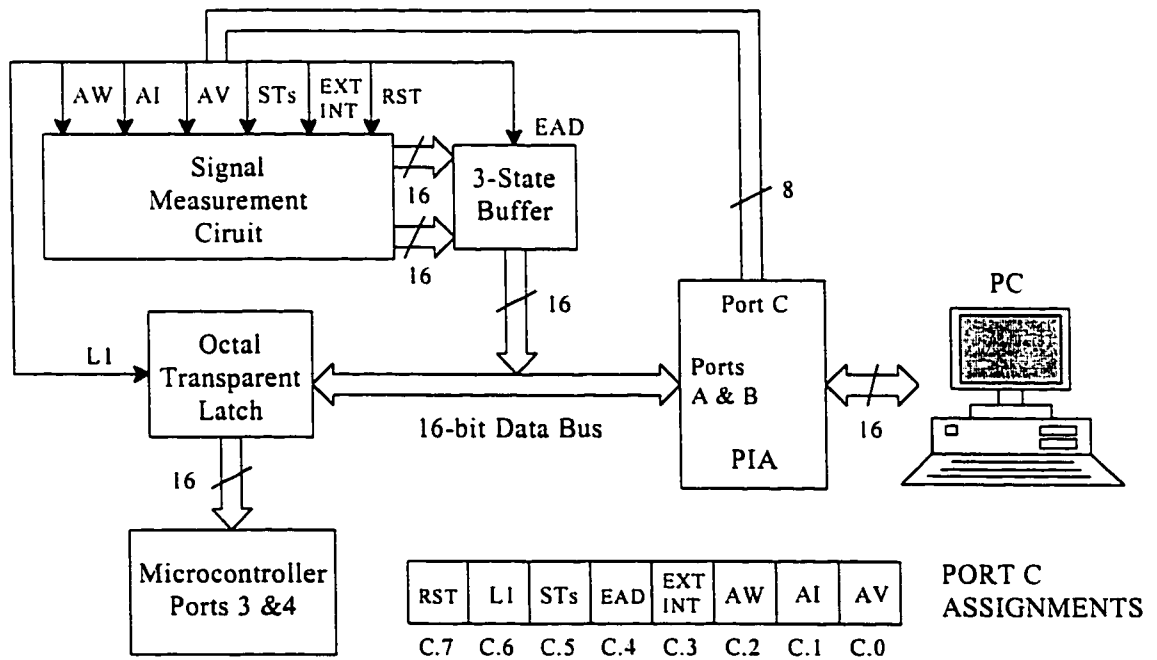


Figure 5.23 Communications control block diagram

memory, and the signal measurement circuit. The 8 bits of port C are assigned the various functions shown in Figure 5.23. An external interrupt (EXT INT) is used to interrupt the signal measurement process and notify the measurement circuit that the PC would like to read a measurement. The 'enable the A/D' bit (EAD) is set to connect the signal measurement circuit to the 16-bit data bus, and cleared to disconnect the measurement circuit from the bus. Measured voltage, current, or power are requested from the signal measurement circuit by setting AV, AI, or AW respectively. Rotor speed is requested by setting the speed strobe bit (STs). A measurement circuit reset operation is performed by setting the RESET bit.

Shared memory is created through the latching function of the octal transparent latch. The latching signal (L1) is used to latch the port A and B values to the inputs of ports 3 and 4 of the microcontroller. Writing to shared memory is performed by clearing the EAD bit, thereby disconnecting the measurement circuit from the data bus. Ports A and B are configured for output and the pre-calculated values of I_{mag}^* and I_{α}^* are written to the ports. The port A and B values are latched to ports 3 and 4 by first setting and then clearing L1. A full schematic of the communications control block is provided in the supplementary document to this thesis.

5.8 SIGNAL MEASUREMENT

5.8.1 Phase Voltage Measurement

The PMSM phase voltage cannot be measured directly as only the three power lines are accessible outside of the machine. A phase voltage reconstruction circuit is neces-

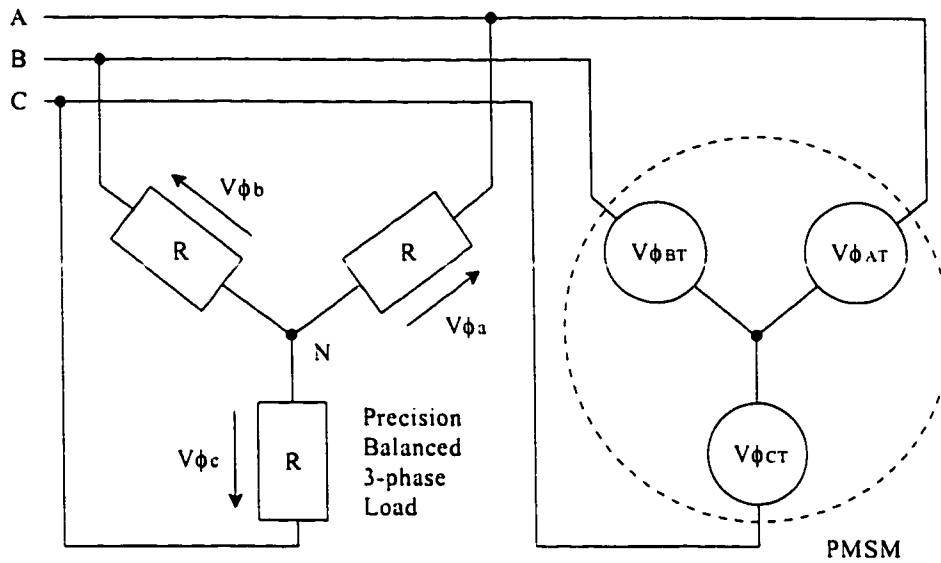


Figure 5.24 Phase voltage reconstruction circuit

sary for the measurement of the PMSM phase voltages. Figure 5.24 illustrates the methodology for the indirect measurement of the phase voltages. A balanced three phase Y-connected set of precision resistors is connected across the power lines to the PMSM. The PMSM phases are assumed to be ideally balanced, as specified by the manufacturer. A balanced set of 3-phase terminal voltages, $V_{\phi AT}$, $V_{\phi BT}$, and $V_{\phi CT}$, are assumed to be produced inside the PMSM.

A balanced three phase resistive load draws a balanced set of three phase currents from a balanced three phase voltage source. The balanced set of three phase currents load currents produces an in-phase, balanced, set of three phase load voltages across the precision load resistors. The midpoint 'N' of the Y-connected load provides a simulated floating neutral point that is used as a reference point for measuring the reconstructed phase voltages. Precision load resistance values are chosen to be high enough to draw less than 0.1% of the rated current at rated voltage. The measurement circuit is assumed to have a negligible

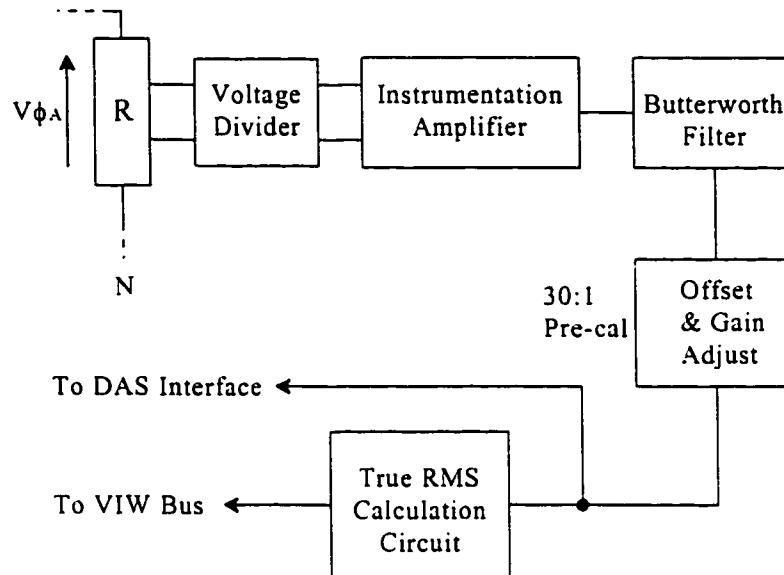


Figure 5.25 Phase voltage measurement

influence on the terminal voltage of the PMSM.

Reconstructed phase voltages are attenuated through the use of a high impedance voltage divider. Coaxial cables are used to transmit the attenuated signals to the remote signal calibration and processing circuitry. The shielding techniques, described in Chapter 4, are used throughout the construction of the phase voltage measurement circuit. Figure 5.25 provides the block diagram for the phase voltage measurement part of the signal measurement circuit. An instrumentation amplifier is used to ground reference the differential input attenuated phase voltage signals. The ground referenced signals are low-pass filtered using 3rd order, 1941 Hz cutoff frequency, Butterworth filters. The Butterworth filters are identical to the ones used for the current feedback circuitry described in Section 5.3.2. Gain and offset adjust circuitry is used to pre-calibrate the measured phase voltage signals so that 1 V_{rms} measured is equal to 30 V_{rms} actual phase voltage.

The components used for the instrumentation amplifier, Butterworth filter, and the

offset and gain adjust circuitry, are nearly identical to the components used in the current feedback circuit. The measured phase voltage signal delay is assumed to be identical to the phase current feedback delay measured in Section 5.3.2 and calculated with (5.2). Pre-calibrated phase voltage signals are connected to BNC connectors so that they can be interfaced with the realtime Data Acquisition System (DAS) described in section 5.8.3. Phase A of the phase voltage signals is applied to a true rms calculation circuit. A dedicated true rms-to-dc conversion IC is used to produce a 0-5 Vdc signal for a 0-7 Vrms input. The resulting dc signal is applied to the VIW measurement circuit. A full schematic diagram of the phase voltage reconstruction and measurement circuit is provided in the supplementary document to this thesis.

5.8.2 Phase Current Measurement

Measured PMSM phase current signals are already provided by the current feedback circuits. Feedback signals representing the filtered phase current are buffered and connected to BNC connectors for interface with the realtime Data Acquisition System described in section 5.8.3. The measured phase A current signal is applied to a true rms-to-dc calculation circuit that is identical to the one used for the phase voltage. A 0-5 V dc signal is produced for a 0-7 V true rms current signal input corresponding to a 0-28 A true rms actual phase current. The dc signal produced by the true rms-to-dc calculation circuit is applied to the VIW measurement circuit. A schematic diagram for the phase current measurement circuit is provided in the supplementary document for this thesis.

5.8.3 Realtime Data Acquisition Interface

The phase voltage and current signals are measured in realtime using a dedicated 10-bit resolution Data Acquisition System (DAS). Coaxial BNC connector cable is used to interface the phase current and voltage signals to a gain adjust and voltage limit circuit. The encoder marker and the reference phase current signals are also applied to the gain adjust and voltage limit circuit to provide a reference frame for the acquired data. Waveform magnitudes are adjusted to a peak amplitude close to, but under, 5V peak to produce the highest resolution without exceeding the $\pm 5V$ maximum input specifications of the DAS. Specifications for the DAS are provided in Appendix A, and a schematic for the measured signal to DAS interface is provided in the supplementary document for this thesis.

A DAS software program, named FSCOPE, is used to acquire the phase, voltage, current, reference current and marker signals in real time³. Figure 5.26 provides a sample of

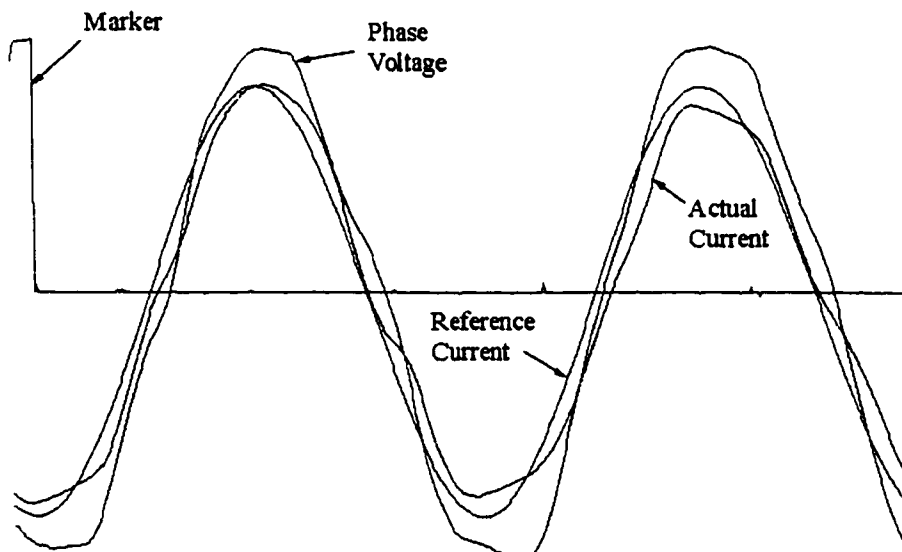


Figure 5.26 DAS measured waveforms at 8000 rpm

³ ZABSCOPE and FSCOPE are in-house programs written by Dr. Barna Szabados and Frank Bourguet, at the Power Research Laboratory, McMaster University, Hamilton, Ontario, Canada.

the DAS measured phase voltage, phase current, reference current, and marker signals for near rated load, 8000 rpm operation of the BLM4035 PMSM. All four signals are sampled simultaneously at up to 20 kHz per channel. An 80 kHz per channel maximum sampling resolution is obtained by using the marker signal to trigger the start of the data acquisition. A resolution of 300 points per cycle at 8000 rpm is possible using this method. Sampled waveforms are viewed, cropped, merged, and processed using a program called ZABSCOPE. Fourier series representations are calculated from the ZABSCOPE processed waveforms to determine the fundamental component magnitudes and phase angles with respect to the marker signal for the phase voltage and current.

5.8.4 Phase Power Measurement

The mean power in a periodic waveform is theoretically determined using (5.3).

$$\text{Mean Power} = \frac{1}{T} \int_0^T v(t) i(t) dt \quad \text{where } T = \text{period} \quad (5.3)$$

Practical application of (5.3) requires realtime multiplication and integration of the measured phase current and voltage signals. Accurate microprocessor calculation of the mean power is possible for voltage and current signals less than or equal to 60 Hz. An 8000 rpm PMSM rotor speed produces phase current and voltage waveshapes with 267 Hz fundamental frequencies. Accurate mean power calculation requires the use of dedicated analog circuitry.

A four quadrant analog multiplier/divider IC is employed to implement the function $W=XY/U$. Pre-calibrated measured phase current and voltage signals are applied to the X and Y inputs of the multiplier IC. The full scale measured phase current and voltage

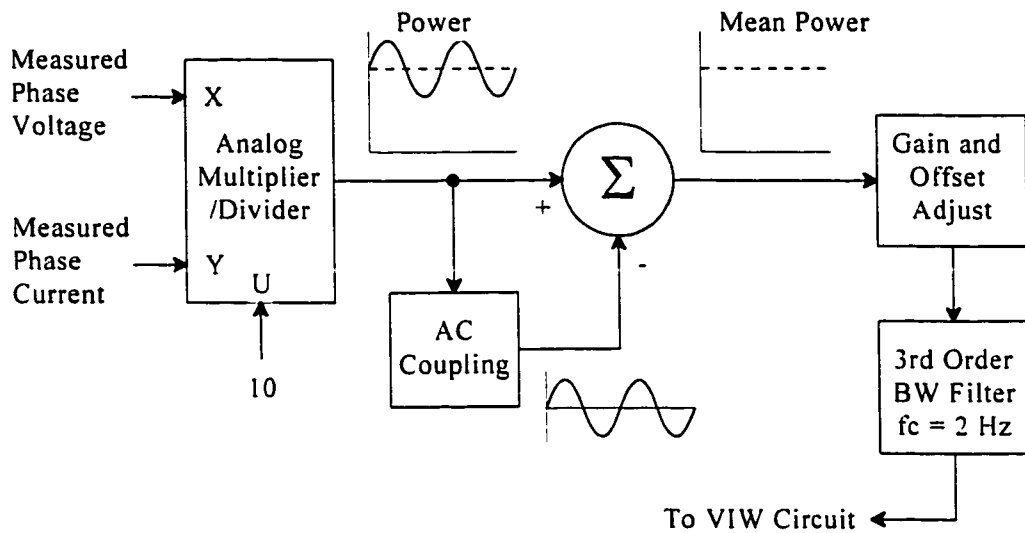


Figure 5.27 Mean power calculation circuit

signal input values are set to 7 V true rms, providing a maximum 5.88 kVA ac power measuring capability. The value of U is set to 10 to limit the multiplier/divider IC full scale output to 9.8 peak-to-peak. Mean power is calculated by isolating and subtracting the AC component from the output of the analog multiplier/divider circuit, as illustrated in Figure 5.27. A gain and offset adjust circuit is used to amplify and adjust the mean power signal before it is applied to a 2 Hz cutoff frequency Butterworth filter. The gain and offset are adjusted so that the dc output of the Butterworth filter is equal to 5 V for an in-phase 7 V true rms X and Y input to the multiplier/divider IC. The output of the Butterworth filter is applied to the VIW measurement circuit. A full schematic of the phase power measurement circuit is provided in the supplementary document to this thesis.

5.8.5 VIW Circuit

The VIW circuit is used to perform A/D conversion on the analog voltage levels corresponding to the true rms values of the measured phase voltage, current, and mean

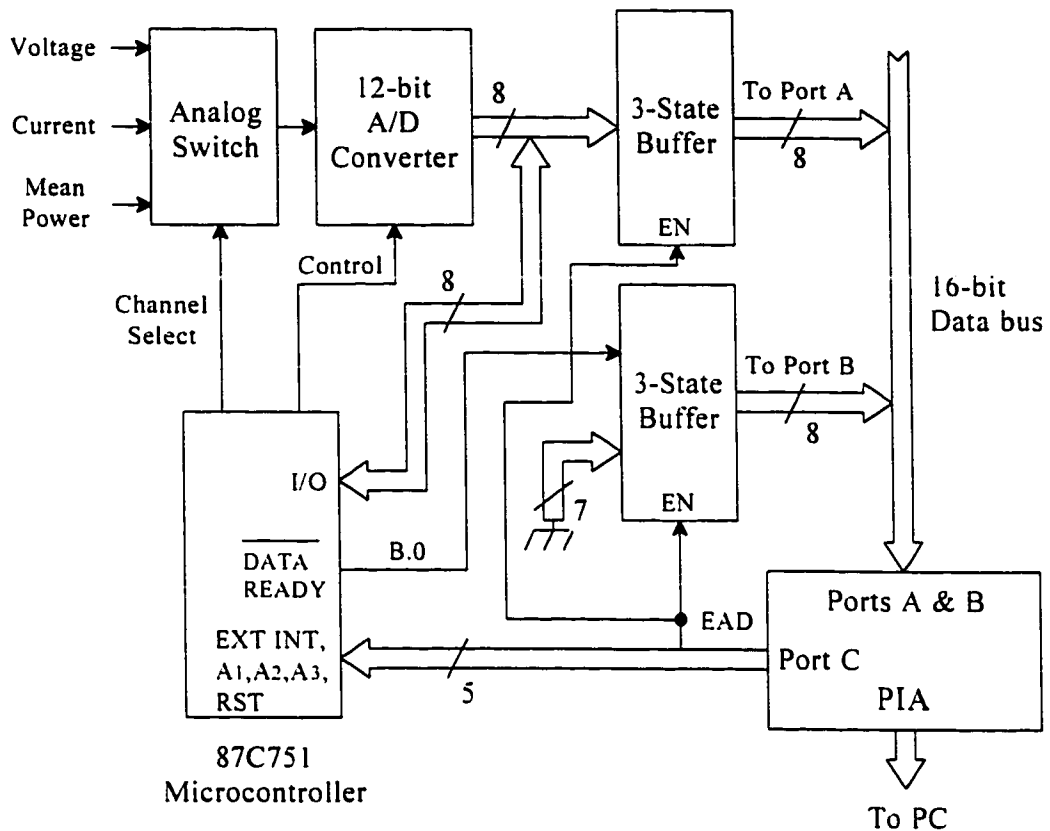


Figure 5.28 VIW circuit block diagram

phase power. EMI susceptibility reduction is essential for the successful operation of the VIW circuit. Noise reduction techniques described in Chapter 4 are used throughout the circuit construction. Figure 5.28 shows the block layout of the VIW circuit. A high speed analog switch is used to connect the analog signal for either the phase voltage, phase current, or mean power to a 12-bit microprocessor compatible A/D converter. The outputs of the A/D converter are transferred to a 3-state buffer which is used to connect the digital converted values to the 16-bit PIA interface data bus.

Microprocessor control of the A/D converter is accomplished through the use of a Philips 87C751 microcontroller. The microcontroller controls the channel selection of the analog switch as well as the A/D conversion timing. An 8-bit bidirectional port on the

microcontroller is used to read the converted values of the analog signals into the microcontroller memory. Two read operations are required to store each 12-bit converted value into memory. Memory stored converted values are updated continuously as the microcontroller supervises a repeated and endless loop conversion of the phase voltage, phase current, and mean phase power. Free running operation of the microcontroller supervised A/D conversion process provides an uninterrupted performance of 2500 updates per second for each memory stored converted value.

An external interrupt (INT), from Port C of the PIA, is employed to halt the endless loop operation of the microcontroller and start the execution of a data output ISR. Data output is controlled by the logic values of the AV, AI, and AW bits on Port C. A logic 'HI', written by the PC to AV (C.0), acts as a request for the microcontroller to output the memory stored converted value for the phase voltage. Similar requests are made by using the AI (C.1) and AW (C.2) bits, and multiple requests are not allowed. A logic 'HI' is written by the PC to the A/D enable bit EAD (C.3) to enable the 3-state buffers connected between the A/D converter outputs and the 16-bit PIA interface data bus.

The microcontroller ISR polls the AV, AI, and AW bits to determine which measured value is requested by the PC. A phase voltage read request detected by the microcontroller causes the microcontroller to immediately place the A/D converter outputs in the high impedance mode and to write the most significant 4 bits of the measured true-rms phase voltage value to the lower nibble of the 8-bit bidirectional microcontroller port connected to the A/D converter outputs. Port A of the PIA is effectively connected to the microcontroller bidirectional port through the Port A 3-state buffer. A logic 'LO' -DATA

READY signal is applied by the microcontroller to the least significant bit of the Port B buffer once data is written to the microcontroller bidirectional port. The microcontroller waits for a response from the PC by polling the AV bit.

The PC software polls Port B of the PIA to determine if the most significant 4 bits of data has been applied to the lower nibble of Port A. A logic 'LO' at Port bit B.0 signals that the data is ready and the PC software reads the value of Port A. The PC software clears the AV bit once Port A is read, and polls the Port bit B.0 to determine if its has been set to logic 'HI'. A logic 'LO' at the AV bit is interpreted by the microcontroller as a signal that the PC has successfully read the Port A value. The microcontroller writes a logic 'HI' to the -DATA READY bit and waits for an acknowledgement from the PC by polling AV. A logic 'HI' is detected by the PC on Port bit B.0. The PC responds by setting AV to logic 'HI' to indicate that it is now ready to read the least significant byte of the digital value for the true-rms phase voltage. Port B of the PIA is polled by the PC software as it waits to determine if the remaining 8 bits of data have been applied to Port A.

A logic 'LO' at the AV bit is interpreted by the microcontroller as a request for the remaining 8 bits of the true-rms phase voltage. The remaining 8 bits are written to the bidirectional port of the microcontroller which is still effectively connected to Port A of the PIA. A logic 'LO' -DATA READY signal is applied by the microcontroller to the least significant bit of the Port B buffer to signify that the data is ready. The microcontroller waits for a response from the PC by polling the AV bit.

A logic 'LO' at Port bit B.0 signals that the data is ready and the PC software reads the value of Port A. The PC software clears the AV bit once the data has been successfully

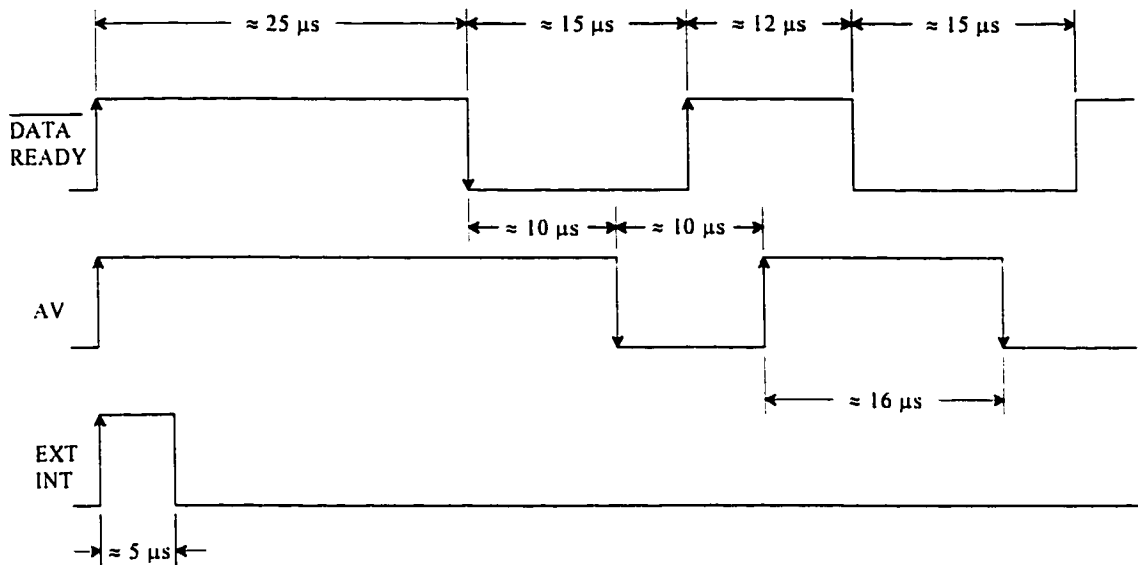


Figure 5.29 VIW circuit and PC communications timing

read and disconnects the VIW circuit from the 16-bit data bus by clearing the Port C A/D enable bit EAD. The microcontroller detects a logic 'LO' at the AV bit and interprets the logic level change as a signal to end communication. Analog to digital conversion of the measured signals resumes as the microcontroller sets the -DATA READY signal to logic 'HI', switches the bidirectional microcontroller port to the 'read' mode, and enables the A/D converter.

Figure 5.29 provides the timing waveforms for the communication between the VIW circuit and the PC. The indicated times are obtained by measuring these logic waveforms in the actual VIW circuit when interfaced with the 486 DX2, 66 MHz PC. Identical waveforms are obtained during the reading of the phase voltage, phase current and mean phase power values. Less than 200 μs is required to read all three quantities into the PC. A flowchart for the communications ISR and A/D control program for the 87C751 is provided in Appendix B. The corresponding assembly language code and the full schematic dia-

grams for the VIW circuit are provided in the supplementary document for this thesis.

5.8.6 Speed Measurement

The digital speed measurement circuit, discussed in [11, p.59], is used to determine the PMSM rotor velocity. The measured speed value consists of the number of shaft position encoder pulses counted in 10 msec. Rotor operation at 8000 rpm provides approximately 1667 pulses in the fixed 10 msec time frame. A maximum measurable rotor speed of 19656 rpm is possible with this speed measurement circuit configuration.

The speed strobe signal STs is used to disable the speed value update during the read operation so that the last value of the measured speed is read by the PC. Figure 5.30

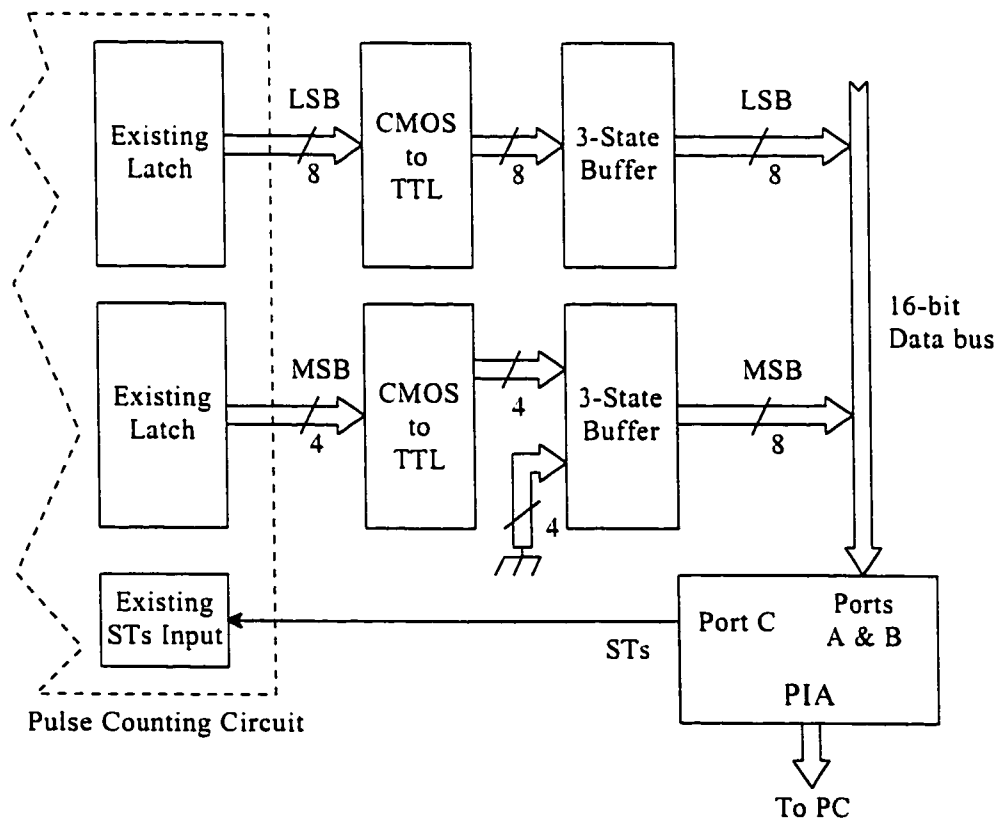


Figure 5.30 Speed measurement circuit block diagram

shows a block diagram for the connection and operation of the speed measurement circuit. The STs input and 12-bit Latch outputs are accessed through the existing speed measurement board constructed in [11]. Latched speed values are level-shifted and interfaced to a three-state buffer which is used to connect the measured speed values to the 16-bit PIA interface data bus.

Measured speed is read into the PC memory using PC software control. Ports A and B of the PIA are enabled as inputs. The three state buffer from the VIW circuit is set to high impedance by ensuring that EAD is at logic 'LO'. A logic 'HI' is applied to the speed strobe bit STs to connect the latched measured speed value to the data bus. The 12-bit speed value is read into Ports A and B and processed to convert the measured speed signal into rpm. A full schematic of the speed measurement circuit is provided in the supplementary document to this thesis.

5.9 PC CONTROL

A software program called PMSMCON8 is executed on the 486DX2-66MHz PC to control and monitor the operation of the high speed PMSM drive. The specially designed program communicates with the microcontroller shared memory ports and with the signal measurement circuitry through the PIA. The details of the communication procedures between the PC and the external circuitry have already been discussed in the previous sections.

5.9.1 Program Structure

The PMSMCON8 program structure consist mainly of input, processing, output,

and control functions. The program is required to read the measured speed, phase current, phase voltage, and mean phase power. Measured signals are processed to calibrate and convert them to units of rpm, true rms current, true rms voltage, and mean power in watts. Power factor is calculated from the ratio between the phase power and the product between the true rms phase voltage and current. The torque conversion ratio is calculated as the ratio between the speed and the product between the true rms phase voltage and current. Torque conversion ratio is used to indicate how well the PMSM is converting its electrical input power into electrical torque. The calculated values are displayed to the monitor along with the most recently acquired values of the reference current magnitude and phase angle.

Control parameters I^*_α and I^*_{mag} are written by the PC to the microcontroller through the PIA. Values of I^*_α and I^*_{mag} are determined according to whether the program is being executed in the 'manual' or 'auto' mode. The PC-based PMSM control program starts in the 'manual' control mode. The user manipulates the reference current magnitude I^*_{mag} by pressing the 'up' and 'down' arrow keys of the keyboard. Reference current phase angle is manipulated by pressing the 'left' and 'right' arrow keys. Figure 5.32 shows a screen shot of the PMSMCON8 program as it is operated in the 'manual' mode.

Automatic control is invoked by pressing 'A' on the keyboard and disabled by pressing 'M'. Figure 5.32 shows a screen shot of the PMSMCON8 program as it is operated in the 'auto' mode. Values of I^*_α and I^*_{mag} are automatically determined according to the user input settings for the operating speed and torque limit. Automatic control is performed so that the actual speed tracks the desired speed setting without exceeding the torque limit setting. Desired speed is adjusted through the 'up' and 'down' arrow keys, and the

torque limit setting is adjusted using the 'left' and 'right' arrow keys of the keyboard. Control of the PMSM speed is performed through the use of a torque control subroutine within PMSMCON8. The torque control subroutine can be rewritten to perform both simple and high performance torque control schemes such as those proposed in [21], [30], [31] and [32].

The PC based control program records the displayed data when the 'ENTER' key is pressed on the keyboard. Displayed data is catalogued with the 'shot number' and stored in an ASCII file. Program termination is accomplished at any time by pressing the 'ESC' key. Flowcharts for the operation of the main program and major subroutines of PMSMCON8 are provided in Appendix B. A listing of the source code for the manual mode control program operation, with expansion capabilities for the full implementation of the automatic control mode functions, is provided in the supplementary document for this thesis.

5.9.2 Signal Measurement and Calibration

The phase voltage, phase current, mean phase power and rotor speed are read by the PC according to the handshaking protocol discussed in Sections 5.8.5 and 5.8.6. Measured values are read by the PC approximately once every 75 ms and added to a running total. The number of successful reads of the measured signals is recorded so that the measured signal values are correctly averaged after the 15th attempted measured signal read operation. Averaging is used to provide a smoothed update for the monitor displayed measured signal values which are updated approximately once per second.

The 12-bit speed input count is calibrated in-circuit with a clock oscillator. The 10

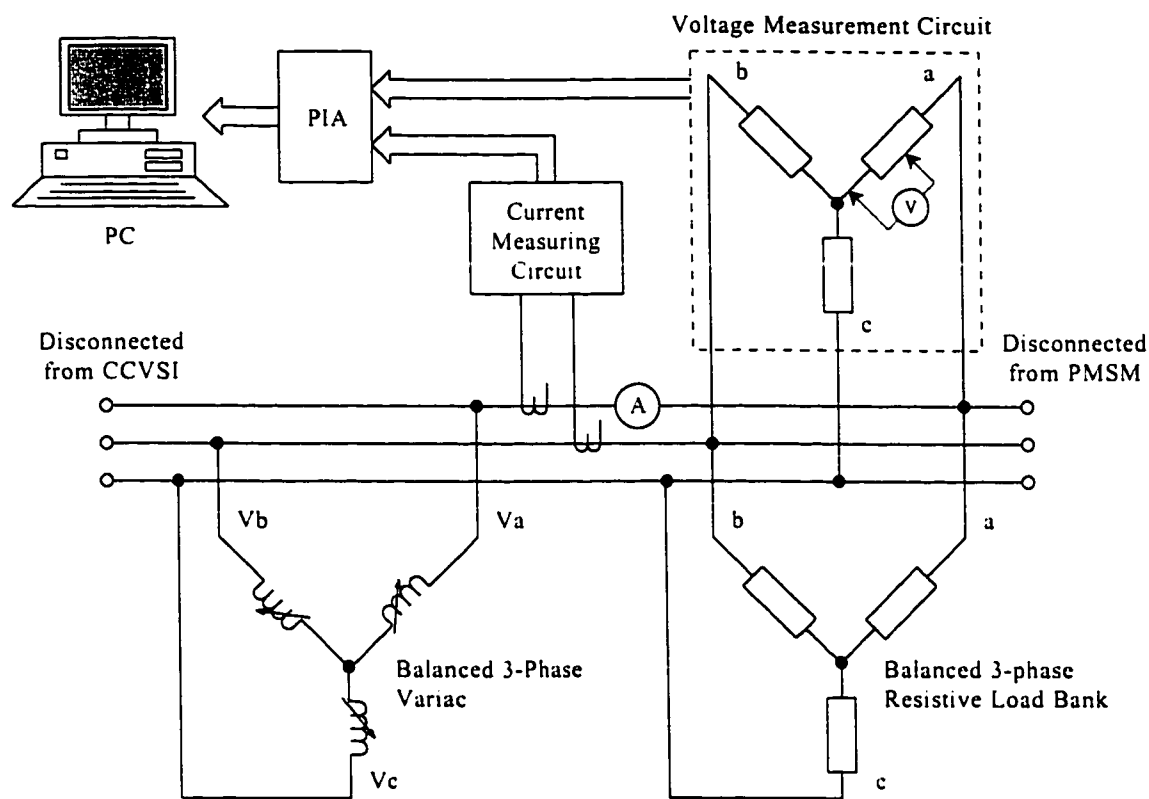


Figure 5.33 Final calibration setup block diagram

ms time base used for the speed count is accurate to within 0.1%. Speed values are converted to rpm for the visual display, and are considered to be as accurate as needed. True rms phase voltage, phase current, and mean phase power are pre-calibrated in-circuit as specified in Sections 5.8.1, 5.8.2, and 5.8.4 respectively. The monitor displayed values of the true rms phase voltage, phase current, and mean phase power are calculated according to the pre-calibrated settings, but must be subjected to a final calibration.

Final calibration is performed by calculating the necessary numerical expression required to adjust the monitor displayed measured signal values to equal the actual values measured with conventional measuring equipment. Figure 5.33 shows the block diagram of the setup used for the final calibration of the monitor displayed voltage, current, and

power values. The PMSM and the CCVSI are disconnected from the 3-phase power lines. A 3-phase variac is used to apply a balanced set of three phase voltages and a resistive load bank is connected and adjusted to draw an in-phase balanced 3-phase current. A digital meter is connected in series with the phase A line to the resistive load. The BBC M2110 digital multimeter used to measure the true rms current is accurate to within $\pm 0.5\%$ of the full scale current. A high impedance input Fluke 76 digital multimeter is used to measure the actual true rms phase voltage. The voltmeter is connected across the voltage divider output of the voltage measurement circuit and is accurate to within $\pm 1.5\%$ of the full scale voltage reading.

The three phase variac and load bank are adjusted to provide current measurements from 0 to 15 A in 2 A steps, and voltage measurements from 0 to 45 V in 5 V steps. The current and voltage are also adjusted simultaneously to provide phase power measurements from 0 to 500 W in 75W steps. Digital multimeter and PC monitor values are recorded and compared. Monitor measured values of phase voltage, current, and power are plotted against the multimeter measured values. A linear regression is performed for each of the three plots to obtain an expression in the form $y = ax + b$. Monitor measured values are subtracted with b , and then divided by a to obtain values that map within 1% of the actual multimeter measured values. Hence, PC monitor measured phase voltage, phase current, and phase power are assumed to be worst case accurate to within $\pm 2.5\%$, $\pm 1.5\%$, and $\pm 4\%$ respectively. The regression results, and measurement error comparison tables for the measured voltage, current, and power signals are listed in the supplementary document to this thesis.

5.9 DRIVE REALIZATION AND TEST SETUP

The preceding sections have described the design and construction of the proposed high performance microprocessor controlled PMSM drive. Figure 5.34 shows the test bench and power connections for the two PMSMs used in this investigation. The PMSMs are coupled through a speed reducer to a dc motor/generator that is used for drive debugging and for variable loading. A dual element flywheel, shown in Figure 3.9, can be coupled directly to the PMSMs, once the dc motor/generator and the speed reducer are removed.

The exposed parts of the EMI shielded voltage and current measurement circuits are shown in Figure 5.35. Shielded cables and steel conduit are used throughout the drive construction to shield the sensitive circuitry from EMI emissions. The CCVSI is shown along with its connection to the energy storage tank and dc link. Separate steel enclosures are used to house the VSI and the VSI switching signal electronics. The degree of EMI shielding used for this prototype may seem excessive, however, expensive accidents through noise induced glitching and intermittently unreliable drive operation are avoided with this setup.

Drive control and signal processing are performed at a location remote from the actual CCVSI and PMSMs. Figure 5.36 shows the location and interconnection of the microcontroller, control PC, and the PC based DAS. The dc motor/generator control panel is located close to the control PS to allow for simultaneous PMSM drive and loading adjustments. Figure 5.37 shows a closer view of the control and signal processing electronics. The electronics rack on the left side holds the gridded printed circuit boards used for the PWM to reference waveform conversion, error- Δ PWM signal generation, speed measure-

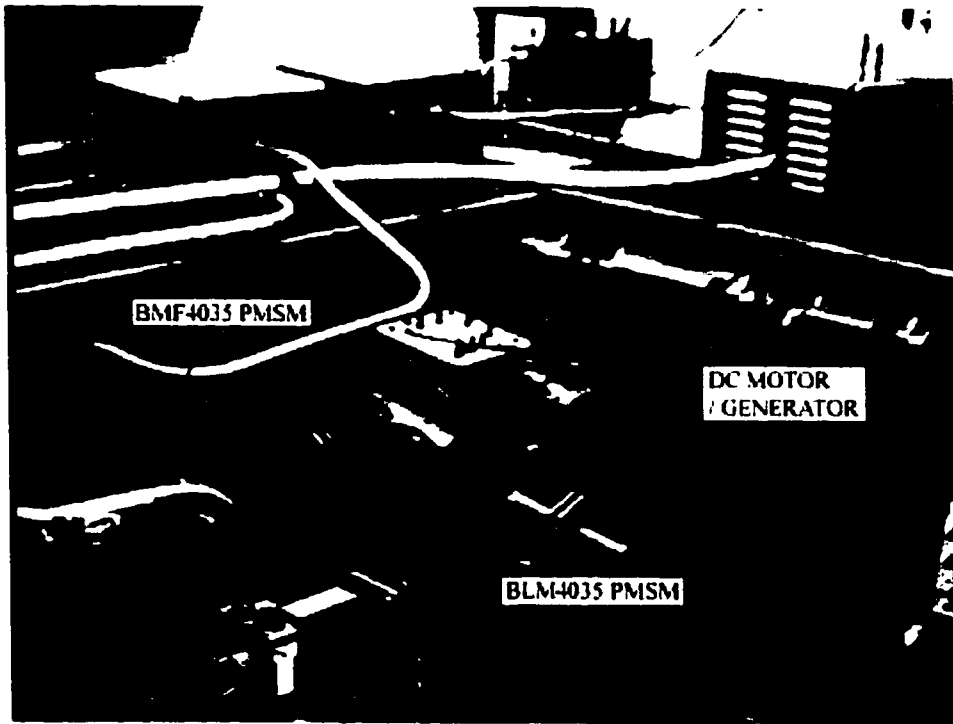


Figure 5.34 PMSM testbench

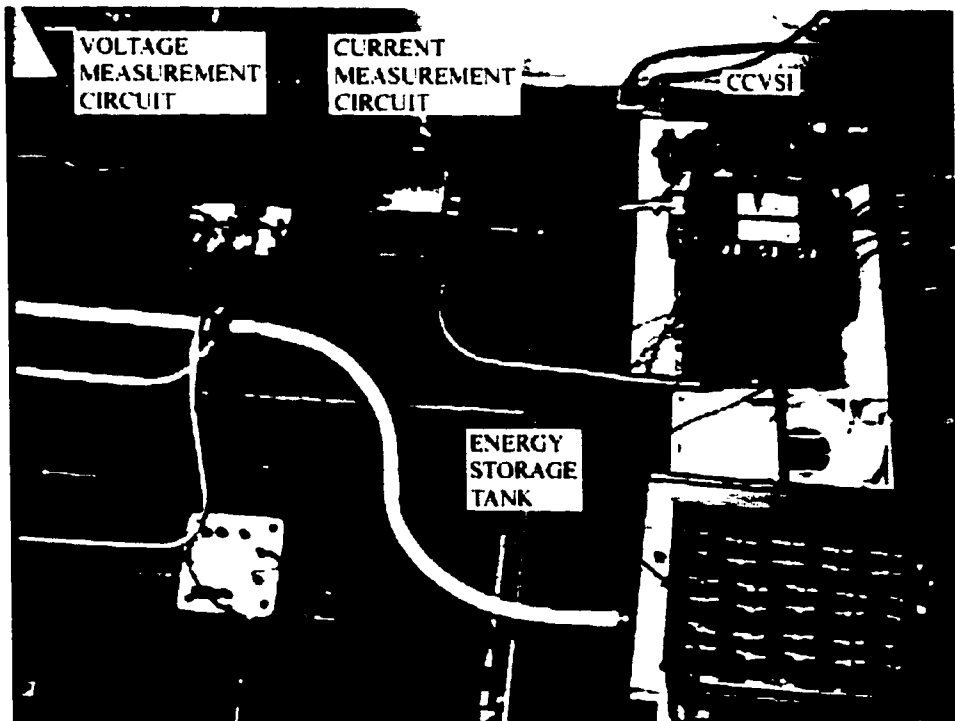


Figure 5.35 Shielded measurement circuit implementation and drive components

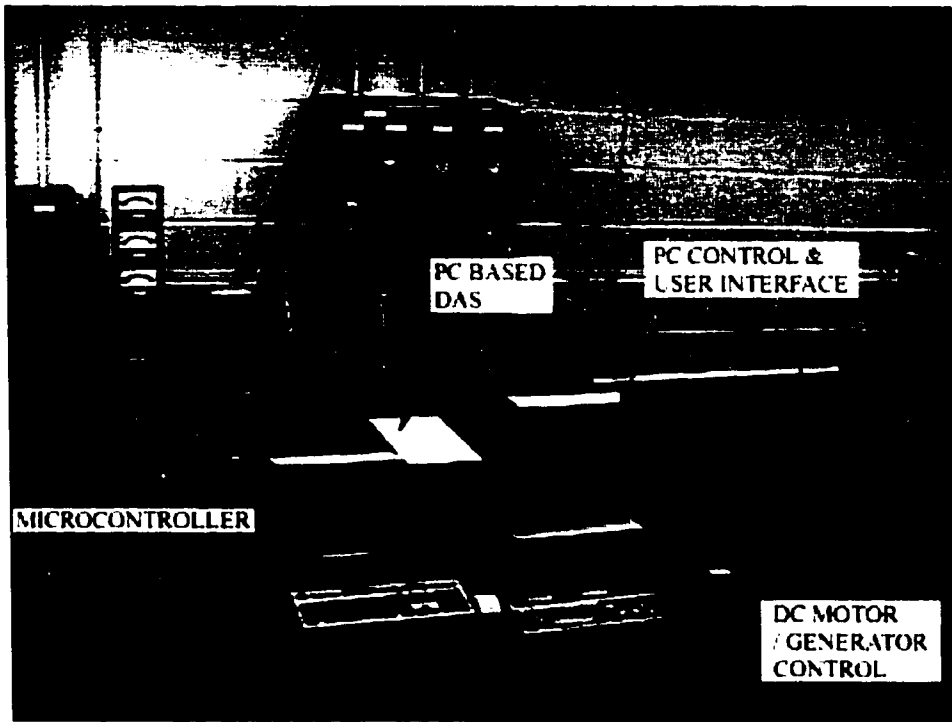


Figure 5.36 Control and signal processing test setup

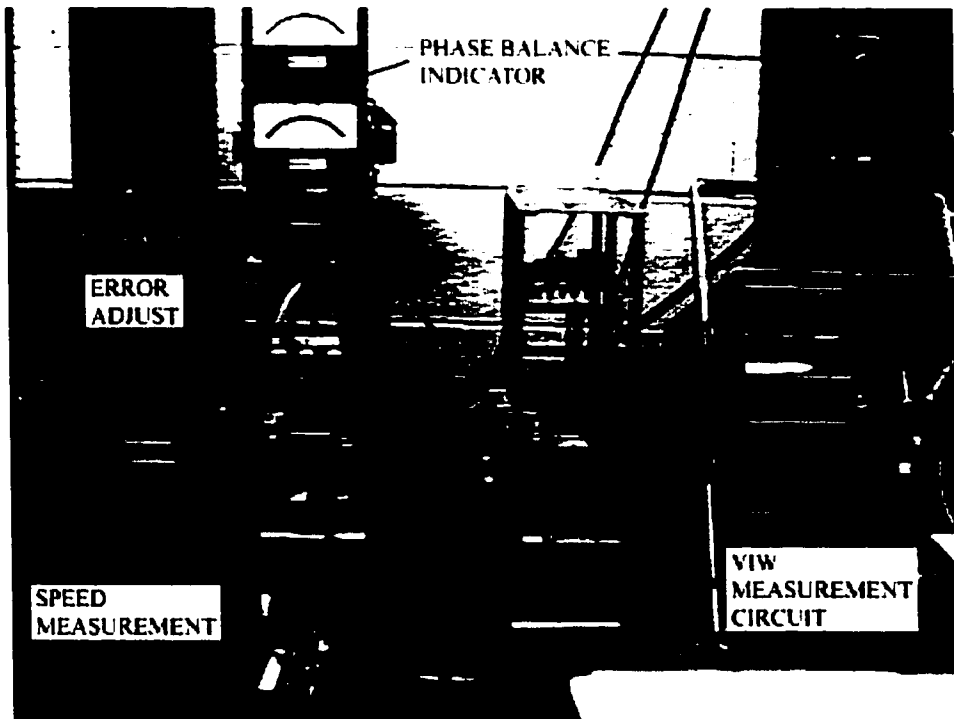


Figure 5.37 Control and signal processing

ment, and feedback current circuitry. A phase balance indicator circuit is used to validate the assumption that all three phases of the PMSM are indeed well balanced. The electronics rack on the right holds the VIW circuit boards, the PIA interface, and the DAS interface circuitry. Gain and offset adjustments are provided so that the inputs to the PC based DAS can be adjusted to provide full amplitude within the $\pm 5V$ maximum range. The oscilloscopes are externally triggered by the marker signal and display the reference current, measured current, and measured voltage waveforms.

Manual control of the high performance drive is achieved at speeds of up to 8000 rpm at a dc bus voltage of 140 V. Interchangeability of both of the PMSMs is accomplished through the use of a dedicated encoder for each machine and a manual adjustment of the initial phase current angle command I_{α}^* . Automatic control is implemented with the addition of an, as yet, undeveloped torque control software function on the control PC. Torque control requires the knowledge of an estimate for the PMSM machine parameters. Manufacturer supplied parameters for both machines are listed in Appendix A.

Suppliers of off-the-shelf PMSMs are reluctant to provide technical information about the rotor construction and equivalent circuit parameters. High performance torque control in the high speed operating region of a PMSM requires a detailed understanding of the PMSM parameters. The technical information listed in Appendix A is inadequate for high performance PMSM torque control, and any additional information requested from the supplier is deemed 'factory proprietary'. Automatic mode high performance torque control can only be implemented if the parameters required for such control can be readily identified. The focus of this investigation will now shift to the development of a repeatable

procedure to accurately identify the parameters required for the high performance torque control of the PMSMs. Torque control parameter identification requires an understanding of the process in which torque is actually developed in an electric machine. Parameter identification cannot proceed without such theoretical development.

CHAPTER 6

THEORETICAL DEVELOPMENT OF ELECTRIC MACHINE TORQUE

6.1 MODEL SELECTION AND SIMPLIFYING ASSUMPTIONS

An estimate for the air gap torque developed in a salient pole brushless permanent magnet synchronous machine can be derived from first principles using an idealized doubly fed synchronous machine. The idealized machine has a balanced 3 phase armature winding on the stator, and a dc field winding on the rotor. The idealized model does not include damper windings, slot reluctances, and eddy current paths. Machine iron is assumed to be linear and lossless, and all leakage paths are simple. Inductances are also assumed to vary as simple harmonic functions in space. The model is developed using sign convention corresponding to the motoring operation of the synchronous machine. Finally, the machine is assumed to operate under balanced steady-state conditions, meaning that the mmf of the stator windings rotates at the same speed as the mmf of the rotor field. Hence, the airgap flux relative to the rotor is essentially a fixed waveform. A fixed airgap flux relative to the rotor implies that the flux linkages with the rotor circuits are time invariant and produce no induced voltages within the rotor circuit. The main field windings become the only current carrying rotor circuit [33, p. 268].

An idealized representation of a doubly fed synchronous machine is shown in Fig-

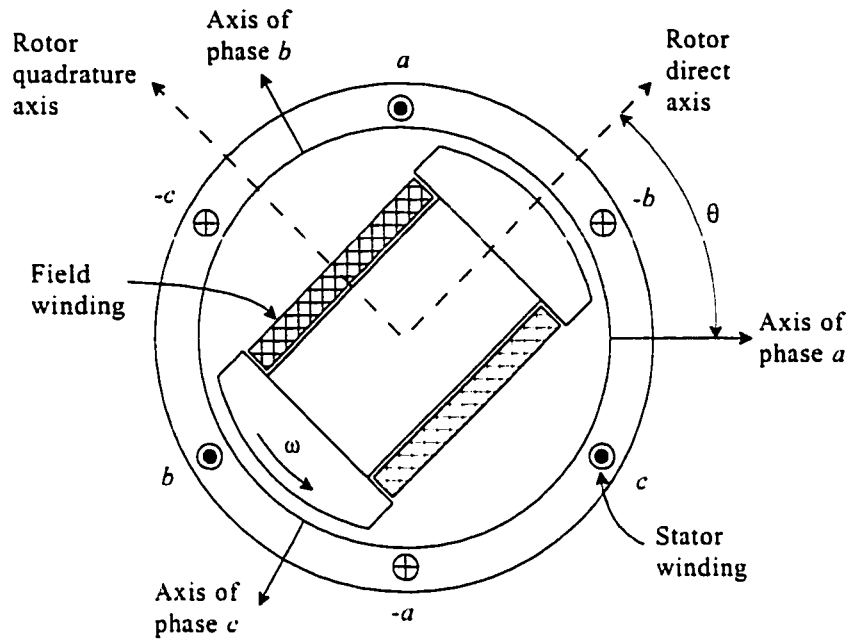


Figure 6.1 Idealized synchronous machine

Figure 6.1 [33, p. 271]. Figure 6.1 contains a stator circuit for each of the three phase windings and a rotor circuit corresponding to the field winding. Each of the circuits contains its own resistance, self inductance, and mutual inductance with respect to each of the other circuits. Equation (6.1) shows the flux-current relationship in terms of the three phase stator windings and the rotor field winding [33, p. 273]. The \mathcal{L}_{xx} terms represent the self-inductances of each of the windings, and the \mathcal{L}_{xy} terms represent the mutual inductances of the windings with respect to each other.

$$\begin{bmatrix} \lambda_a \\ \lambda_b \\ \lambda_c \\ \lambda_d \end{bmatrix} = \begin{bmatrix} \mathcal{L}_{aa} & \mathcal{L}_{ab} & \mathcal{L}_{ac} & \mathcal{L}_{af} \\ \mathcal{L}_{ba} & \mathcal{L}_{bb} & \mathcal{L}_{bc} & \mathcal{L}_{bf} \\ \mathcal{L}_{ca} & \mathcal{L}_{cb} & \mathcal{L}_{cc} & \mathcal{L}_{cf} \\ \mathcal{L}_{fa} & \mathcal{L}_{fb} & \mathcal{L}_{fc} & \mathcal{L}_{ff} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \\ i_d \end{bmatrix} \quad (6.1)$$

6.2 INDUCTANCE REPRESENTATION

6.2.1 Stator Self-Inductances

The air gap permeance for a salient pole rotor synchronous machine is assumed to have a constant component as well as a smaller component (L_{g2}) that varies cosinusoidally with the rotor angle θ , shown in Figure 6.1. Application of this assumption to a balanced three phase system allows the stator self-inductances to be expressed as [33, pp. 222 & 273]:

$$\mathcal{L}_{aa} = L_{aao} + L_{al} + L_{g2} \cos(2\theta) \quad (6.2)$$

$$\mathcal{L}_{bb} = L_{aao} + L_{al} + L_{g2} \cos(2\theta + 120^\circ) \quad (6.3)$$

$$\mathcal{L}_{cc} = L_{aao} + L_{al} + L_{g2} \cos(2\theta - 120^\circ) \quad (6.4)$$

where: L_{aao} is the component of self-inductance due to space fundamental airgap flux
 L_{al} is the component of self-inductance due to stator leakage flux

6.2.2 Stator to Rotor Mutual Inductances

The stator to rotor mutual inductances vary periodically with the rotor angle q . The mutual inductance between the phases and the field windings varies as a cosine function of the rotor angle for an assumed sinusoidal space MMF and airgap flux distribution. Hence, the stator to rotor mutual inductances are rewritten as in (6.5) thru (6.7) [33, p. 221].

$$\mathcal{L}_{af} = \mathcal{L}_{fa} = L_{af} \cos(\theta) \quad (6.5)$$

$$\mathcal{L}_{bf} = \mathcal{L}_{fb} = L_{af} \cos(\theta - 120^\circ) \quad (6.6)$$

$$\mathcal{L}_{cf} = \mathcal{L}_{fc} = L_{af} \cos(\theta - 120^\circ) \quad (6.7)$$

6.2.3 Rotor Self-Inductance

The assumption of a cylindrical stator with no harmonic effects from the stator slots implies that the self-inductance of the field winding is independent of the rotor posi-

tion θ . This allows the rotor circuit self-inductance to be rewritten as a constant.

$$\mathcal{L}_f = L_f \quad (6.8)$$

6.2.4 Stator-to-Stator Mutual Inductance

Stator-winding to stator-winding mutual inductances are determined from the assumption that the mutual inductance is derived solely from the space-fundamental airgap flux. The stator phase windings are spaced 120° apart, allowing the mutual inductances between phases to be determined by multiplying $\cos(\pm 120^\circ)$ by (6.2) thru (6.4) and neglecting the stator leakage flux component. The equations simplify to (6.9) thru (6.11) [33, p. 222].

$$\mathcal{L}_{ab} = \mathcal{L}_{ba} = -\frac{1}{2} L_{aa0} + L_{g2} \cos(2\theta - 120^\circ) \quad (6.9)$$

$$\mathcal{L}_{bc} = \mathcal{L}_{cb} = -\frac{1}{2} L_{aa0} + L_{g2} \cos(2\theta) \quad (6.10)$$

$$\mathcal{L}_{ac} = \mathcal{L}_{ca} = -\frac{1}{2} L_{aa0} + L_{g2} \cos(2\theta + 120^\circ) \quad (6.11)$$

6.3 EQUIVALENT CIRCUIT TERMINAL VOLTAGE

The development of idealized synchronous machine inductances allows for the characterization of the machine's equivalent circuit terminal voltages. Terminal voltages for each of the four circuits are equal to the sum of the winding resistance voltage drop and the induced voltage in each circuit. The general form for the terminal voltages is given by (6.12).

$$V = R_s i + \frac{d\lambda}{dt} \quad (6.12)$$

The stator phase resistance on the balanced 3-phase windings is represented by the term R_s .

Equation (6.12) is used to express the voltage equations for each of the four windings in the

form shown in (6.13) to (6.16).

$$V_a = R_s i_a + \frac{d}{dt}(\mathcal{L}_{aa} i_a) + \frac{d}{dt}(\mathcal{L}_{ab} i_b) + \frac{d}{dt}(\mathcal{L}_{ac} i_c) + \frac{d}{dt}(\mathcal{L}_{af} i_f) \quad (6.13)$$

$$V_b = R_s i_b + \frac{d}{dt}(\mathcal{L}_{ba} i_a) + \frac{d}{dt}(\mathcal{L}_{bb} i_b) + \frac{d}{dt}(\mathcal{L}_{bc} i_c) + \frac{d}{dt}(\mathcal{L}_{bf} i_f) \quad (6.14)$$

$$V_c = R_s i_c + \frac{d}{dt}(\mathcal{L}_{ca} i_a) + \frac{d}{dt}(\mathcal{L}_{cb} i_b) + \frac{d}{dt}(\mathcal{L}_{cc} i_c) + \frac{d}{dt}(\mathcal{L}_{cf} i_f) \quad (6.15)$$

$$V_f = R_f i_f + \frac{d}{dt}(\mathcal{L}_{fa} i_a) + \frac{d}{dt}(\mathcal{L}_{fb} i_b) + \frac{d}{dt}(\mathcal{L}_{fc} i_c) + \frac{d}{dt}(\mathcal{L}_{ff} i_f) \quad (6.16)$$

The solution of (6.13) thru (6.16) is simplified by performing a linear transformation on the stator currents, voltages, and fluxes, and replacing them with equivalent quantities rotating at the speed of the rotor. The linear transformation, known as the dqo transformation, and sometimes referred to as the Blondel two-reaction method, produces a stationary frame of reference in which stator quantities are analyzed as seen by an observer on the rotor. A dqo transformation of the stator variable S to the rotor frame of reference is written in the form of (6.17) [33, p. 270].

$$S = \begin{bmatrix} S_d \\ S_q \\ S_o \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta) & \cos(\theta - 120^\circ) & \cos(\theta + 120^\circ) \\ -\sin(\theta) & -\sin(\theta - 120^\circ) & -\sin(\theta + 120^\circ) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} \quad (6.17)$$

The inverse of (6.17) is written as (6.18).

$$S^{-1} = \begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} = \begin{bmatrix} \cos(\theta) & -\sin(\theta) & 1 \\ \cos(\theta - 120^\circ) & -\sin(\theta - 120^\circ) & 1 \\ \cos(\theta + 120^\circ) & -\sin(\theta + 120^\circ) & 1 \end{bmatrix} \begin{bmatrix} S_d \\ S_q \\ S_o \end{bmatrix} \quad (6.18)$$

Application of (6.17) allows the three phase stator currents to be replaced by their transformed quantities:

- i_d - the direct axis current component
- i_q - the quadrature axis current component
- i_o - the zero sequence current component (zero under balanced conditions)

The physical significance of the dqo transformation is that the transformed quantity direct axis components lie along the axis of the field winding, while quadrature axis components lie along an axis perpendicular to the field winding. A revolving rotor sees untransformed mutual inductance between the stator phase windings and the rotor circuits change with rotor position and hence time. Transformed stator variables remain fixed in the rotor frame, resulting in mutual inductances that remain constant with time. The dqo transformation is applied to the flux linkages and currents of (6.1). The manipulations are purely algebraic and as such have been omitted here. The resulting transformed flux linkages are expressed as shown in (6.19) to (6.22).

$$\lambda_d = L_d i_d + L_{af} i_f \quad (6.19)$$

$$\lambda_q = L_q i_q \quad (6.20)$$

$$\lambda_o = L_o i_o \quad (6.21)$$

$$\lambda_f = \frac{3}{2} L_{af} i_d + L_{ff} i_f \quad (6.22)$$

Equations (6.19) to (6.22) contain the following new inductance terms that are no longer functions of the rotor position.

$$L_d = L_{at} + \frac{3}{2} (L_{aao} + L_{g^2}) \quad (6.23)$$

$$L_q = L_{at} + \frac{3}{2} (L_{aao} - L_{g^2}) \quad (6.24)$$

$$L_o = \frac{1}{2} L_{at} \quad (6.25)$$

The voltage equations of (6.13) thru (6.16) are similarly transformed to produce (6.26) to 6.29).

$$v_d = R_s i_d + \frac{d}{dt} \lambda_d - \omega \lambda_q \quad (6.26)$$

$$v_q = R_s i_q + \frac{d}{dt} \lambda_q + \omega \lambda_d \quad (6.27)$$

$$v_o = R_s i_o + \frac{d}{dt} \lambda_f \quad (6.28)$$

$$v_f = R_f i_f + \frac{d}{dt} \lambda_f \quad (6.29)$$

Equations (6.26) and (6.27) are rewritten using (6.19) thru (6.22) as shown below.

$$v_d = R_s i_d + \frac{d}{dt} L_d i_d + \frac{d}{dt} L_{af} i_d - \omega L_q i_q \quad (6.30)$$

$$v_q = R_s i_q + \frac{d}{dt} L_q i_q + \omega L_d i_d + \omega L_{af} i_f \quad (6.31)$$

The transformer terms $\frac{d}{dt} L_d$, $\frac{d}{dt} L_q$, and $\frac{d}{dt} L_{af}$ are assumed to be negligible with respect to ωL_d and ωL_q . Transformer terms are neglected in this analysis since the parameter identification for this torque control application requires only the steady state solution. Hence, (6.30) and (6.31) can be simplified to (6.32).

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} R_s & -\omega L_q \\ \omega L_d & R_s \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} 0 \\ \omega \Psi_{mag} \end{bmatrix} \quad (6.32)$$

6.4 TORQUE EXPRESSION DEVELOPMENT

A torque expression is developed by examining the machine's power equation, shown in (6.33), and in matrix form in (6.34).

$$P = i_a \dot{v}_a + i_b \dot{v}_b + i_c \dot{v}_c \quad (6.33)$$

$$P = \mathbf{i}_s^T \mathbf{V}_s \quad (6.34)$$

Application of the dqo transformations (6.17) and (6.18) to equation (6.34) yields (6.35).

$$P = (S^{-1} I_s)^T S^{-1} V_s = I_s^T (S^{-1})^T S^{-1} V_s \quad (6.35)$$

The $(S^{-1})^T S^{-1}$ term in (6.35) is evaluated as (6.36).

$$(S^{-1})^T S^{-1} = \begin{bmatrix} \frac{2}{3} & 0 & 0 \\ 0 & \frac{2}{3} & 0 \\ 0 & 0 & 3 \end{bmatrix} \quad (6.36)$$

Substitution of (6.36) into (6.35) yields a dqo representation of the p pole pair machine's power, as shown in (6.37).

$$P = \frac{3}{2} p (i_d v_d + i_q v_q + 2 i_o v_o) \quad (6.37)$$

Zero sequence components i_o and v_o are negligible for the balanced 3-phase synchronous machine operation. Substitution of (6.32) into (6.37) yields (6.38).

$$\begin{aligned} P &= \frac{3}{2} p (R_s i_d^2 - \omega L_q i_d i_q + \omega L_d i_d i_q + R_s i_q^2 + \omega \Psi_{mag} i_q) \\ &= \frac{3}{2} p R_s (i_d^2 + i_q^2) + \frac{3}{2} p \omega \Psi_{mag} i_q + \frac{3}{2} p \omega i_d i_q (L_d - L_q) \\ &= \text{ohmic loss} + \text{air gap power} \end{aligned} \quad (6.38)$$

The developed air gap torque is equal to the air gap power divided by the mechanical speed.

Hence, the general torque expression for an idealized synchronous machine is derived from (6.38) and is shown in (6.39).

$$T = \frac{3}{2} p [\Psi_{mag} i_q + i_d i_q (L_d - L_q)] \quad (6.39)$$

Equation (6.39) corresponds to two distinct aspects of torque production. The first term arises from the interaction of the rotor direct axis magnetic flux with the q-axis stator

current. This interaction produces a field alignment torque proportional to the $\Psi_{mag} i_q$ product. The second term arises from the interaction of the current induced magnetic fluxes along the two axis $L_d i_d$ and $L_q i_q$, with the orthogonal current components. The torque from this second term is called the reluctance torque and is caused directly by the rotor saliency. The reluctance torque is proportional to the difference in axis inductance ($L_d - L_q$). Axis inductance varies with the machine geometry. Hence, synchronous machines can be designed with geometries that produce $L_d > L_q$, $L_d = L_q$, or $L_d < L_q$. Equation (6.39) suggests that the PMSM should be interpreted as a hybrid combination of the conventional synchronous reluctance machine and the surface PM machine.

The derivation of a simplified representation for the air gap torque provides the parameters required for the implementation of high performance torque control. Parameters Ψ_{mag} , L_d , and L_q are required to exploit equation (6.39) through the current vector control in the dqo coordinate frame. This investigation will now focus on the identification of these parameters.

CHAPTER 7

PERMANENT MAGNET SYNCHRONOUS MACHINE PARAMETER IDENTIFICATION

7.1 EXPERIMENTAL INVESTIGATION

7.1.1 Test Setup Components

The experimental modified high performance microprocessor controlled PMSM drive system, described in Chapter 5 and illustrated in Figure 5.2, contains all of the control capabilities and feedback signals necessary for the identification of the PMSM parameters for high speed operation. Flywheel energy storage elements, shown in Figure 5.2, are replaced with the conventional dc machine shown in the Figure 5.34 photograph of the PMSM testbench. The BLM4035 and BMF4035 commercially available brushless PM synchronous machines used in this investigation were purchased from the same manufacturer. Both machines are specified as having a sinusoidal back-EMF, balanced on all three phases. A summary of the manufacturer supplied technical specifications, found in Appendix A, is provided in Table 7.1.

The BMF4035 neodymium-iron-boron magnets represent the latest advancement in permanent magnet technology. The BMF4035 PMSM is recommended by the manufacturer as a suitable replacement for the now obsolete BLM4035. Operating speed for the parameter identification procedure is limited to 7500 rpm to ensure safety and prevent PMSM

Table 7.1
Manufacturer Supplied Technical Specifications

Parameter	BLM4035	BMF4035
Max. Operating Speed (rpm)	8000	6000
Max. Cont. Power (W)	2290	1490
Max. Stall Torque (N·m)	4.11	3.95
Line-Line Resistance (Ω)	0.27	0.57
Line-Line Inductance (mH)	1.86	2.30
Back-EMF (Volts/krpm)	24.9	19.9
Torque Sensitivity (N·m/Amp)	0.235	0.235
Permanent Magnet Type	Ferrite-Ceramic	Neodymium-Iron-Boron

damage. Assurances are provided from the manufacturer that the 6000 rpm rated speed BMF4035 can also withstand continuous operation at 7500 rpm. Ratings supplied by the manufacturer reflect PMSM operation using the manufacturer supplied drive using conventional simplified torque control that does not exploit the reluctance torque component of (6.39). The validity of the manufacturer supplied data is questionable.

7.1.2 Control Methodology

Sinusoidal back-EMF is a characteristic obtained from brushless permanent magnet machines incorporating a buried or interior permanent magnet rotor configuration [34]. This type of rotor configuration causes the reluctance to be greater along the d-axis flux paths than along the q-axis flux paths, translating into a higher q-axis inductance (L_q) than d-axis inductance (L_d). Hence, the second term in (6.39) can be exploited to produce positive torque in addition to the main magnetizing torque, only if there is a negative d-axis

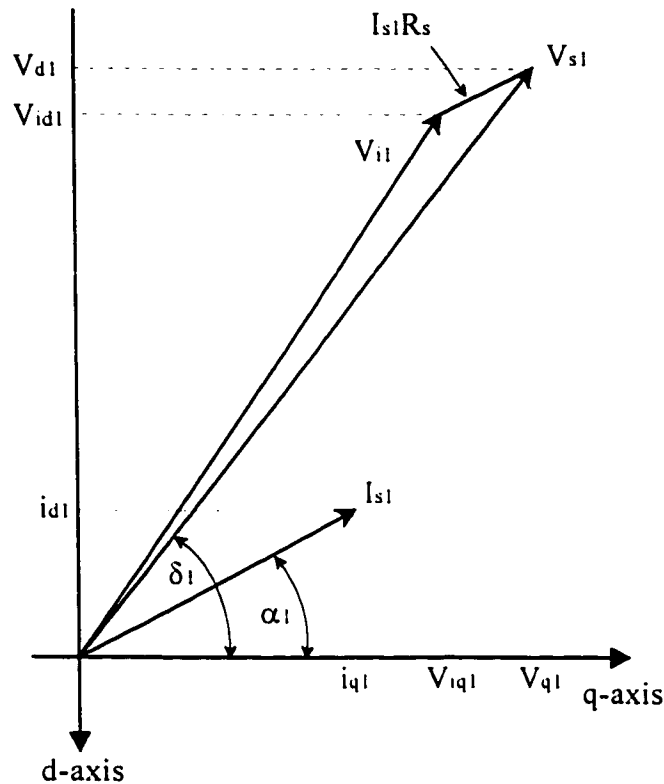


Figure 7.1 Fundamental frequency phasor diagram

current component (i_d). Field weakening operation is possible by using vector control that produces such positive reluctance torque by actively manipulating the input current phasor in the second quadrant of the synchronously rotating d-q axis reference frame.

The manufacturer's sinusoidal back-EMF specification implies that the test machines have interior permanent magnet rotors and also the saliency to cause L_q to exceed L_d . A phasor diagram for the near rated load field weakening operation, commonly referred to as flux weakening operation, of a brushless PM synchronous machine is shown in Figure 5.1. The current phasor I_{s1} is offset from the q-axis to establish a negative d-axis current component. Hence, a positive reluctance torque is developed for an interior permanent magnet machine. It is desired to operate the BLM4035 and BMF4035 machines in this

manner.

The phasors shown in Figure 7.1 consist of only the fundamental frequency components, denoted by subscript 1, and are derived from the measurable input quantities to the Machine Under Test (MUT). The influence of higher order harmonics on the MUT torque production are neglected by maintaining near sinusoidal current and voltage excitation waveforms. Conventional synchronous machine drives employ sinusoidal waveform excitation at speeds up to 3500 rpm, after which the excitation is switched to a simpler six step square wave scheme [35]. The laboratory constructed 7.5 kVA vector controlled drive, described in Chapter 5, is capable of supplying low harmonic sinusoidal excitation for high speed machine operation up to 8000 rpm.

7.1.3 Test Procedure

Establishment of the q-axis

Reconstruction of the MUT's phasor diagram begins with the establishment of its q-axis. Once the q-axis is established, the d-axis is set to be 90 electrical degrees clockwise from the q-axis. The conventional dc machine is connected to operate as a motor and drive the MUT over the desired operating range. Current control is disabled from the VSI drive while the open circuit terminal voltage of the test machine and the encoder marker signal are simultaneously measured at 40 kHz/channel sampling rate using the PC based DAS. The fundamental component of the terminal voltage is reconstructed from the measured data, and plotted with respect to the marker signal. The angular displacement of the crest of the reconstructed sinusoid with respect to the marker is used to establish the q-axis, and

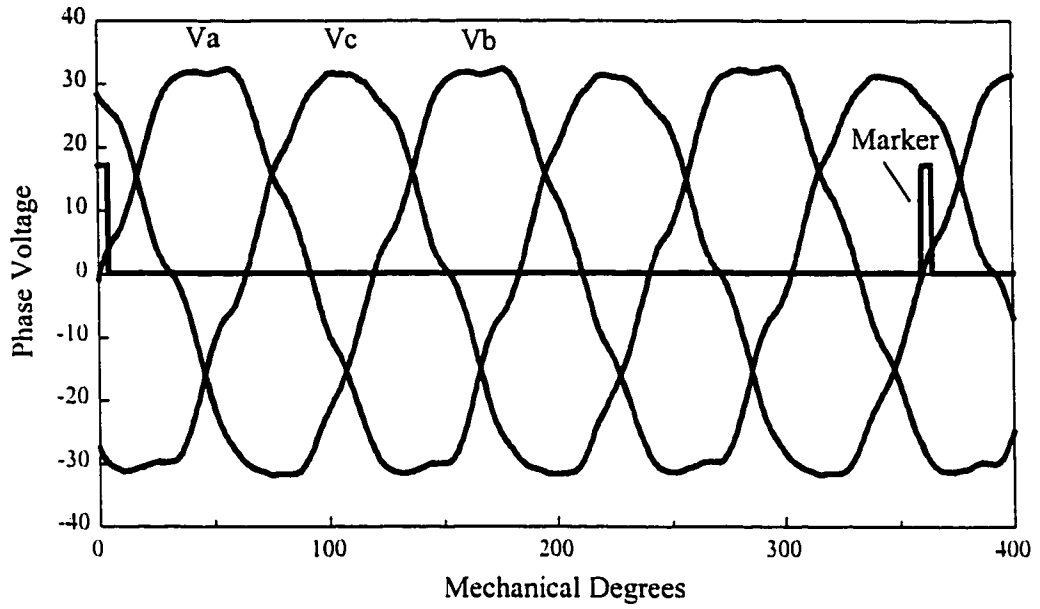


Figure 7.2 BLM4035 back-EMF at 4000 rpm

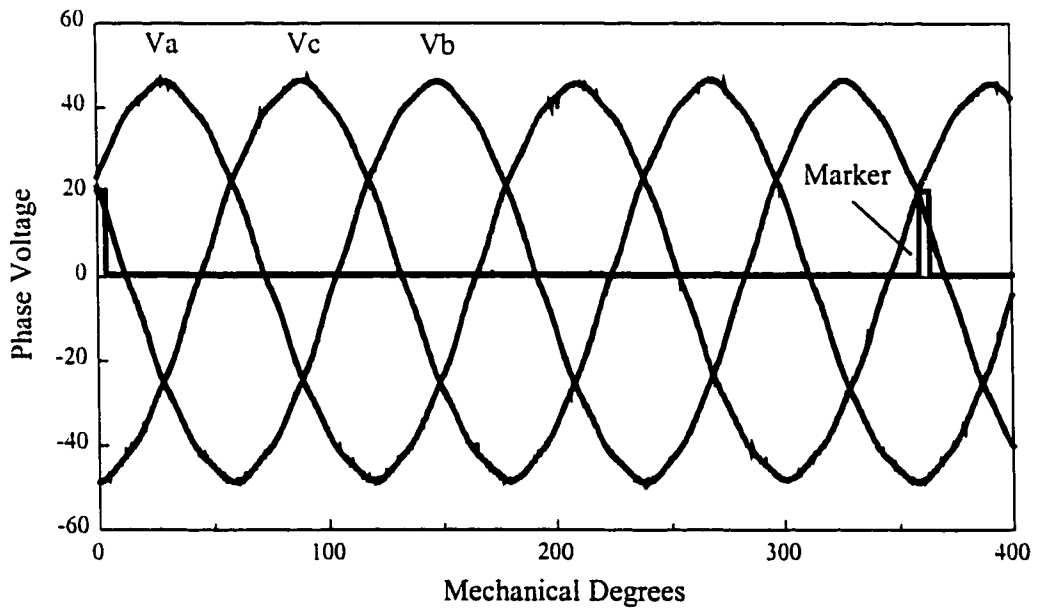


Figure 7.3 BMF4035 back-EMF at 4000 rpm

thereby the d-axis. All measured values for the angular displacement are adjusted by the phase voltage measurement circuit delay, established in Section 5.3.2 as (5.2). A DAS sampling error correction factor is used to adjust the angular displacement by one sampling width. The correction factor is necessary to offset the error produced when the marker and phase voltage signals are split for data analysis. Figures 7.2 and 7.3 show the actual back-EMF waveforms as measured by the DAS at 4000 rpm MUT operation.

The BLM4035 PMSM exhibits a sinusoidal back-EMF with a total harmonic distortion factor that is less than or equal to 5% over a 3000 to 8000 rpm speed range. The BMF4035 provides a higher quality sinusoidal back-EMF with a total harmonic distortion factor that is less than or equal to 1.6% over a 3000 to 8000 rpm speed range. Figure 7.4 shows a plot of the measured rms values for the fundamental back-EMF waveforms. The back-EMF constant calculated from the linearization of the illustrated data is indicated on the plot. Comparison with the peak voltage line-to-line back-EMF constants in Table 5.1

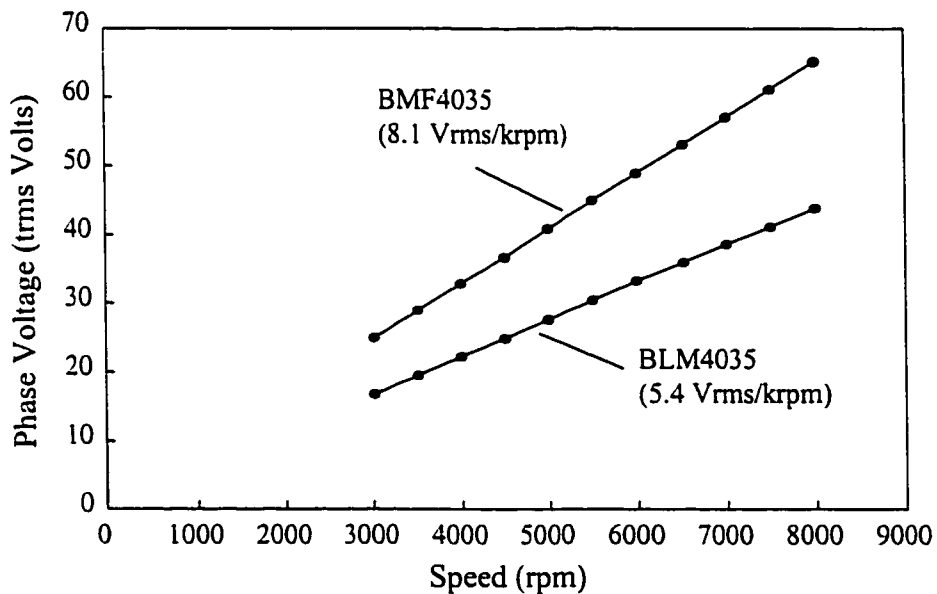


Figure 7.4 Measured back-EMF phase voltages

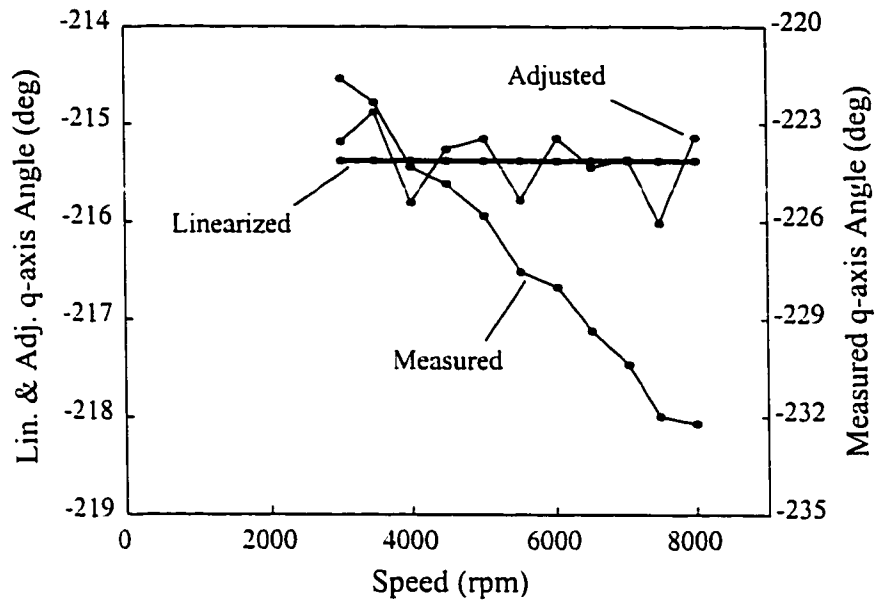


Figure 7.5 BLM4035 q-axis determination

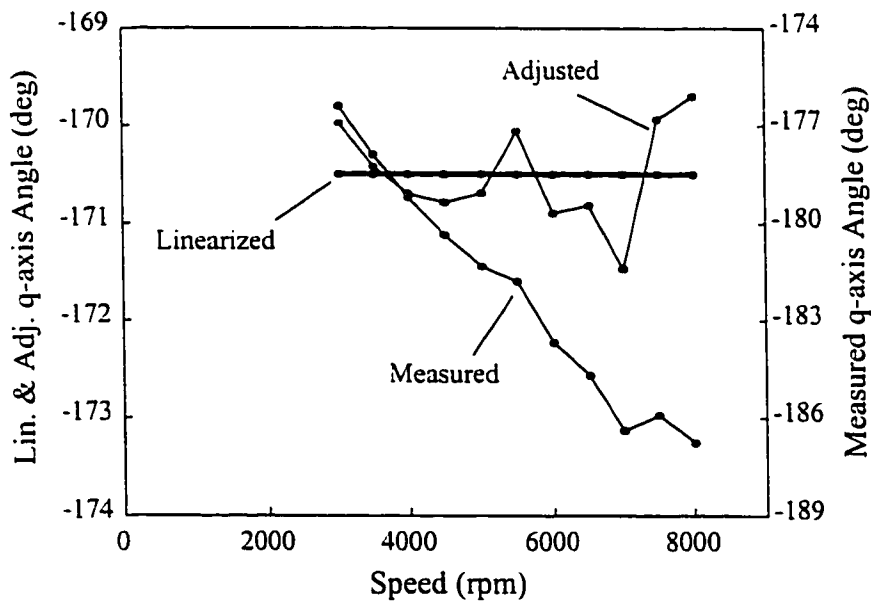


Figure 7.6 BMF4035 q-axis determination

reveals a discrepancy between the manufacturer supplied data for the BLM4035 and what was actually measured.

The q-axis angles are determined with respect to the marker signal for each machine. Figures 7.5 and 7.6 summarize the measured, compensated, and linearized q-axis angles with respect to the marker. The graphs indicate that for each machine, one fixed angle with respect to the marker signal will establish the q-axis to within $\pm 1^\circ$ electrical. A q-axis angle, with respect to the marker, of 215.4° and 117.5° is determined for the BLM4035 and BMF4035 PMSMs respectively. The q-axis is assumed to be fixed over the entire range of machine speed and loading, and the d-axis is assumed to be fixed at 90 electrical degrees clockwise from the q-axis. A summary of the data obtained for the establishments of the q-axis using DAS snapshots over the full operating speed range is provided in Appendix C.

Machine Operating Setpoint

Establishment of the synchronously rotating d-q axis reference frame allows for dqo control of the phase currents. The VSI is reconnected to the MUT and the conventional dc machine is reconfigured as a separately excited generator. Control of the MUT is performed by executing the 'manual' mode operation of the PC based PMSM control program. The reference current phasor magnitude I_{mag}^* and angle I_α^* is varied to place the actual current phasor to the MUT at desired positions relative to the d- and q-axis. Control parameters I_{mag}^* and I_α^* are set to produce the maximum torque conversion efficiency (MTCE) for a specific loading by monitoring the ratio between the operating speed and the product between the input phase current and voltage. Tests are conducted by establishing the MTCE

operating points at different loadings while maintaining a constant speed. Loading is varied by adjusting the excitation field of the conventional dc machine through the dc motor/generator control panel shown in Figure 5.36. The dc bus voltage is maintained at 140 V for all tests. A real-time snapshot of the MUT's excitation waveforms is obtained from the data acquisition system for each MTCE operating point. Speed, voltage, current and power information is simultaneously recorded by the microprocessor by pressing the 'ENTER' key on the control PC keyboard.

7.1.4 Measured Results

The real-time snapshots of the excitation current and voltage waveforms for 7500 rpm, rated load and light load operation of the BLM4035 and BMF4035 PMSMs are shown in Figures 7.7 thru 7.10. In both cases, the total harmonic distortion factor of the waveforms is less than 10% when operation is near rated load. The distortion in the phase current waveforms increases significantly when the machines are operated under light loading. All waveforms are measured with respect to the marker at 0 mechanical degrees. The q-axis is assumed to remain fixed with respect to the marker, allowing for a fundamental frequency diagram reconstruction at any operating point.

Tests are conducted on both machines for constant speed operation between full load and no load. The tests are repeated at intervals of 500 rpm over the 3500 to 7500 rpm range. Loading is adjusted to provide multiple measurements over the range of the test. A summary of the measured data for the phasor diagram reconstruction of the two machines is provided in the supplementary document to this thesis.

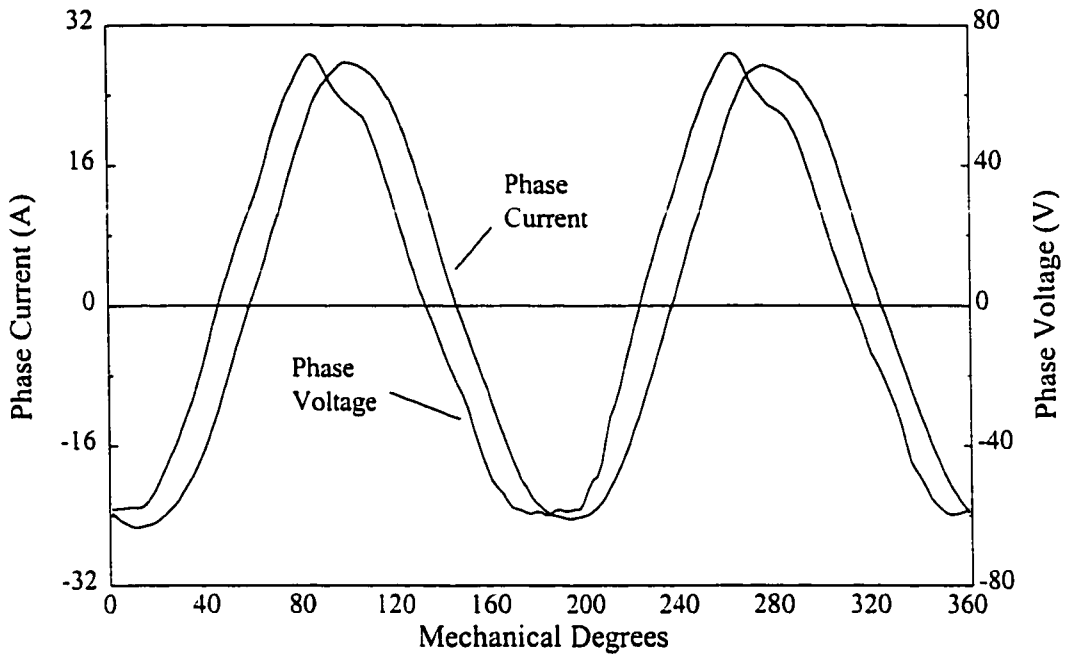


Figure 7.7 BLM4035 measured waveforms at 7500 rpm and rated load

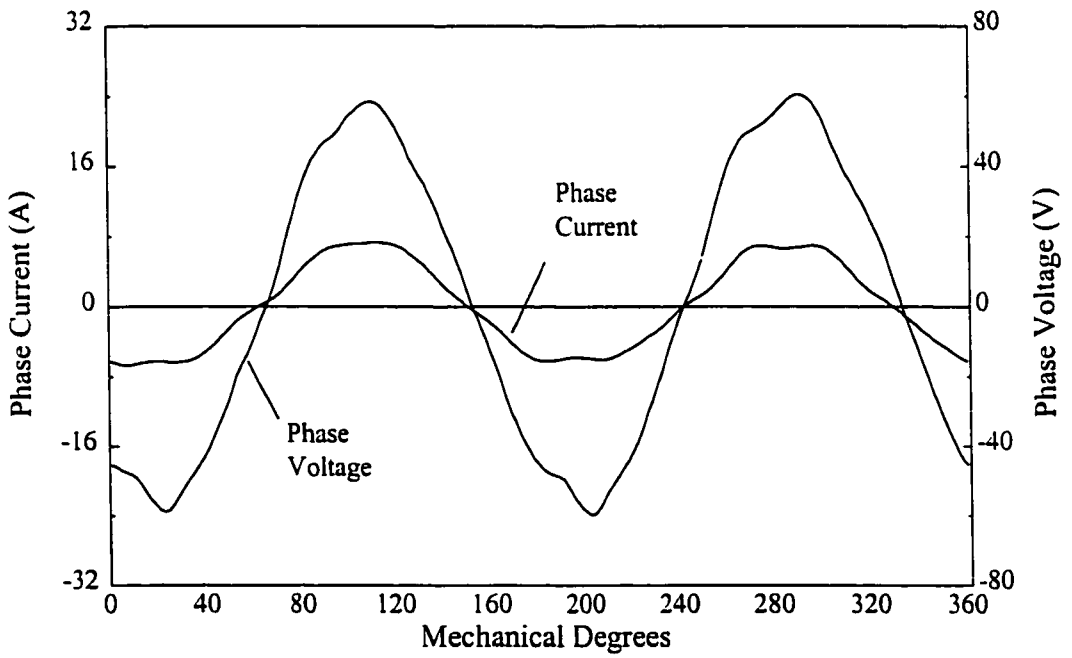


Figure 7.8 BLM4035 measured waveforms at 7500 rpm and light load

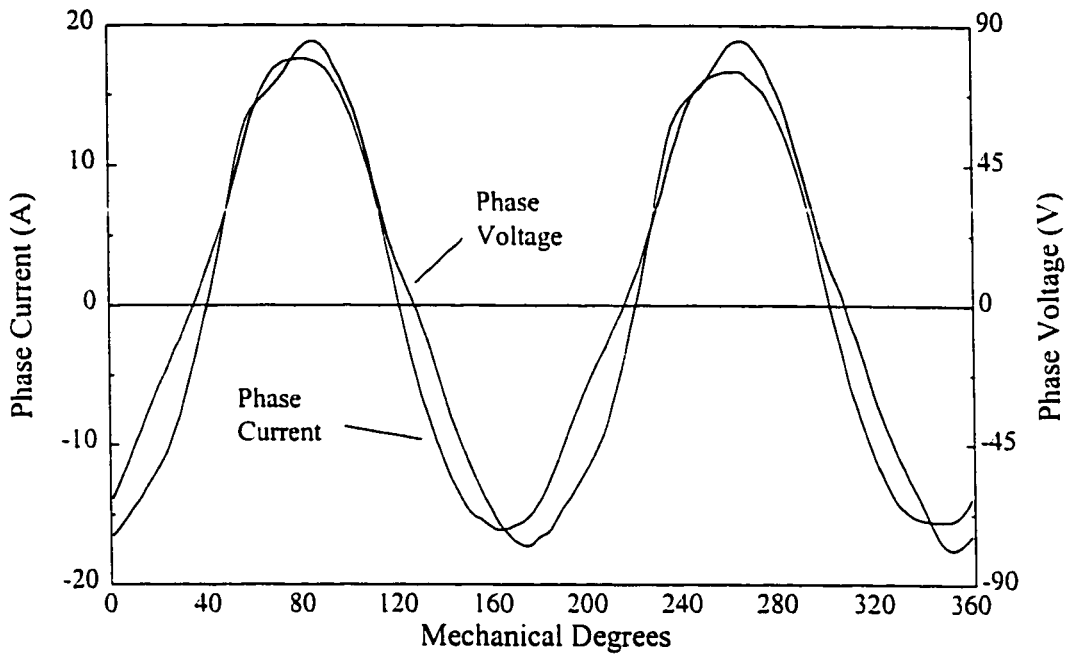


Figure 7.9 BMF4035 measured waveforms at 7500 rpm and rated load

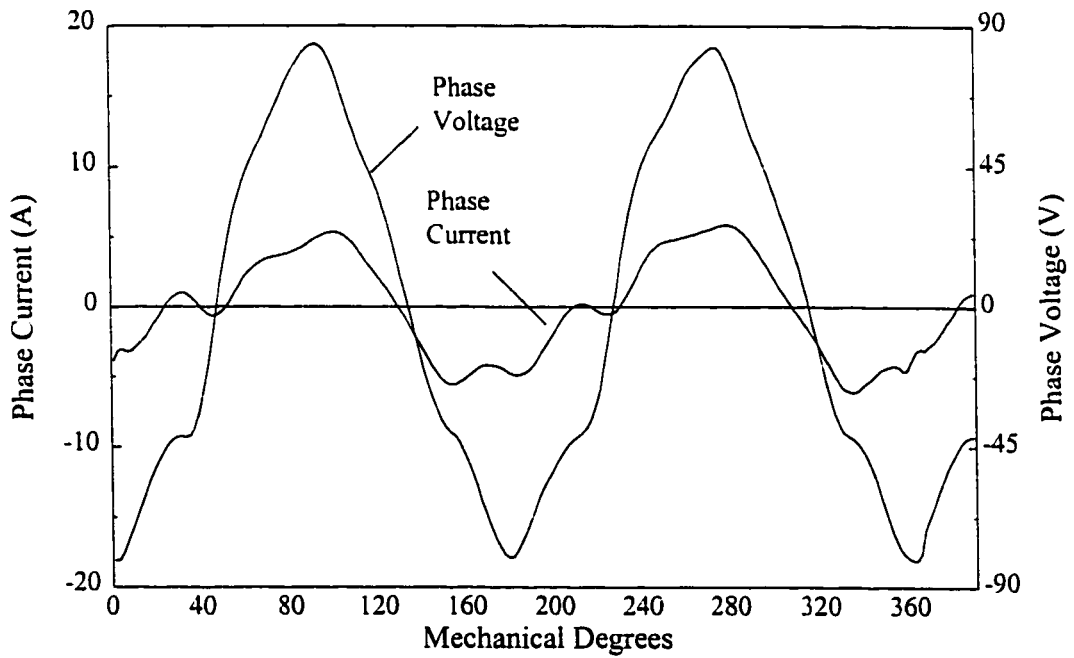


Figure 7.10 BMF4035 measured waveforms at 7500 rpm and light load

7.2 DATA ANALYSIS

7.2.1 Phasor Diagram Reconstruction

Phasor diagram reconstruction provides the necessary data required to identify load dependent trends in the d-q axis representation of the excitation waveforms. Significant errors are developed through an inaccurate determination of the Figure 7.1 phasor diagram angles δ and α . Accurate analysis is possible by computing a Fourier analysis of the excitation waveforms over a complete mechanical revolution. Phasor angles δ and α are determined by measuring the electrical angle of the peak of the fundamental and adjusting for the q-axis. Phasor magnitudes are determined by calculating the measured waveform's distortion factor and adjusting the microprocessor measured true rms value for that waveform.

Reconstruction of Figure 7.1 is completed by using an empirical relationship to calculate the value of the frequency and temperature dependent stator resistance R_s . An LCR meter is used to determine the dc, 120 Hz, and 1 kHz resistances for each phase of the two machines at ambient and operating temperature. Equations (7.1) and (7.2) provide the empirical relationships used to determine the phase resistances at the operating temperature as a function of the frequency f in Hz.

$$R_{\text{phase (BLM4035)}} = 0.000776 \cdot f^{1.015} + 0.35 \Omega \quad (7.1)$$

$$R_{\text{phase (BMF4035)}} = 0.000116 \cdot f^{1.283} + 0.42 \Omega \quad (7.2)$$

A summary of the phase resistance measurements and the phase resistance calculation at different PMSM speeds is provided in Appendix C.

The d-q axis transformed excitation waveform voltage and current magnitudes are plotted against their calculated electrical torque angle δ from Figure 7.1. A relationship

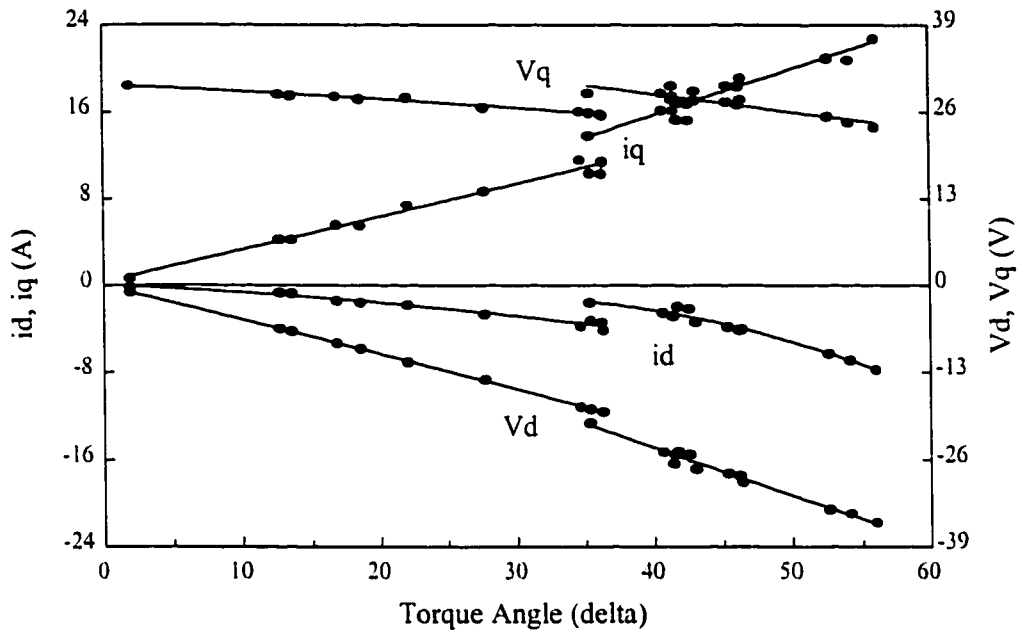


Figure 7.11 BLM4035 measured data and polynomial fits at 5500 rpm

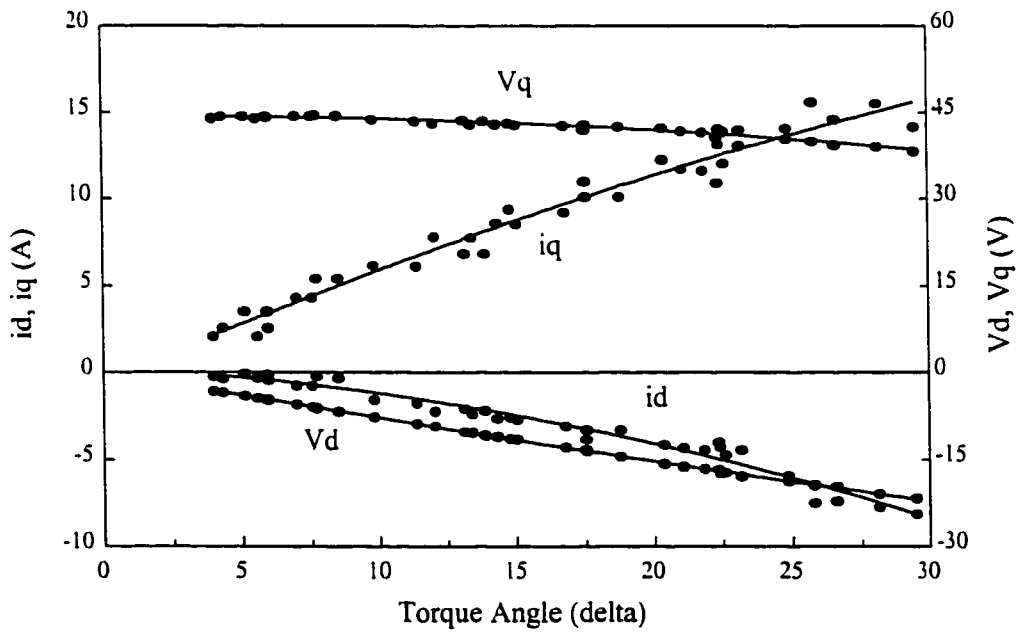


Figure 7.12 BMF4035 measured data and polynomial fits at 5500 rpm

between the excitation inputs and the corresponding electrical torque angle is established by fitting a polynomial through the measured points. The polynomial fits resulting from the measured data of a 5500 rpm loading test on each of the machines are shown in Figures 7.11 and 7.12. The polynomial fits for the other loading tests over the 3500 to 7500 rpm speed range of the two machines are provided in the supplementary document to this thesis.

The BLM4035 PMSM has an operating discontinuity at $\delta \approx 35^\circ$. A discontinuity is detected by a sudden change in the trend of I_α^* at the MTCE. The discontinuity characteristic, shown in Fig. 7.11, is repeatable and is believed to be caused by a change in the reluctance of the flux paths in the machine. Certain critical sections along the flux path come out of saturation as the machine undergoes increased flux weakening at higher speeds and loadings. The torque angle at the discontinuity shifts from an angle of $\delta \approx 48^\circ$ to a lower angle of $\delta < 20^\circ$ as the speed setpoint is increased from 4000 to 7500 rpm. No discontinuities are observed at 3500, 4000 and 7500 rpm. The lack of discontinuities at these speeds indicates that for the tested load range, the critical flux path sections remain unsaturated at 7500 rpm, and fully saturated at speeds ≤ 4000 rpm. No discontinuities are found for the BMF4035 over the entire operating range. The difference between the two machines is most likely caused by the use of higher field strength neodymium-iron-boron magnets in the BMF4035. The BMF4035 critical flux path sections remain unaltered, even when it is subjected to higher levels of flux weakening.

7.2.2 Data Modelling

The general model for a brushless PM synchronous machine consists of only a

highly simplified representation of the actual operation of the machine. The static parameter model assumes lossless operation without the effects of magnetic saturation and nonlinearities. Acceptable results are possible when using this model at lower speeds and over a narrow speed range. The effects of core losses and non-linear behaviour do become more prevalent at higher speeds and over a wide speed range.

Core losses must be included when modelling the higher frequency PM synchronous machine operation. Figure 7.13 shows the d- and q-axis equivalent circuits derived from (6.32) and proposed for use in modelling the high speed operation. The terms $X_d = \omega L_d$, $X_q = \omega L_q$, and $E_o = \omega \Psi_{mag}$ are the unknown frequency and load dependent parameters to be determined. The model includes copper losses which are represented by resistance R_s . Core losses are represented by including a loss component proportional to the internal volt-

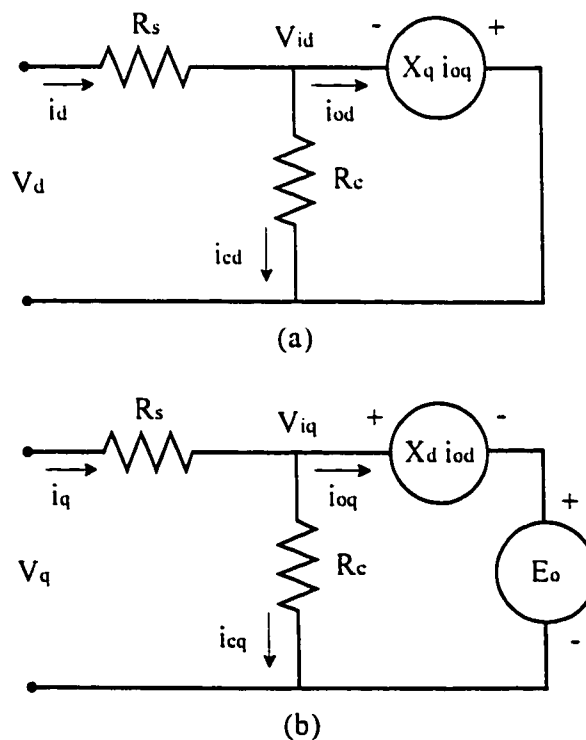


Figure 7.13 (a) d-axis equivalent circuit (b) q-axis equivalent circuit

age V_i of the machine [32][36]. A resistance R_c is included for this investigation. All vector controllable losses are accounted for in this model, however, the model does not account for stray load losses such as those incurred by circulating flux in the machine's back-EMF harmonics.

7.2.3 Parameter Identification

Evaluation of the general torque expression, given by (6.39), requires the knowledge of the unknown parameters X_d , X_q , and E_o . Mathematical analysis of the Figure 7.13 d- and q-axis equivalent circuits yields (7.3) and (7.4).

$$R_c = \frac{i_q X_q R_s - X_q V_q}{V_d - i_d R_s - X_q i_q} \quad (7.3)$$

$$E_o = \frac{1}{K} V_q - \frac{1}{K} i_{oq} R_s + X_d i_{od} \quad (7.4)$$

where:

$$K = 1 + \frac{R_s}{R_c}$$

$$i_{oq} = i_q - \left(\frac{V_q - R_s i_q}{R_c} \right)$$

$$i_{od} = i_d - \left(\frac{V_d - R_s i_d}{R_c} \right)$$

The desired unknown parameters are calculated by assuming that the parameters remain constant for small changes in the operating point. Polynomial fits, such as those in Figures 7.11 and 7.12, are used to predict a new operating point at δ_2 by perturbing the torque angle δ_1 with a small perturbation angle $\Delta\delta \approx 0.1^\circ$ [37][38]. Setting $X_d = X_{d1} = X_{d2}$, $X_q = X_{q1} = X_{q2}$,

and $E_o = E_{o1} = E_{o2}$ over a small change in δ yields the desired parameters through (7.5) and (7.6), with back substitution into (7.3) and (7.4).

$$X_q = \frac{V_{d1} - A V_{d2} - R_s (i_{d1} - A i_{d2})}{i_{q1} - A i_{q2}} \quad (7.5)$$

where:

$$A = \frac{V_{q1} - i_{q1} R_s}{V_{q2} - i_{q2} R_s}$$

$$X_d = \frac{V_{q1} - V_{q2} + R_s (i_{oq2} - i_{oq1})}{K (i_{od2} - i_{od1})} \quad (7.6)$$

The $\Delta\delta \approx 0.1^\circ$ value is the result of a trial and error stability analysis. Larger values of $\Delta\delta$ produce inaccurate solutions to (7.5) and (7.6) as the assumption that $X_d = X_{d1} = X_{d2}$, $X_q = X_{q1} = X_{q2}$, and $E_o = E_{o1} = E_{o2}$ can no longer be made. Values of $\Delta\delta$ that are less than 0.1° cause the denominator in (7.6) to become very small. Unstable solutions result. Hence, an optimal value for $\Delta\delta$ must be determined through trial and error.

Perturbation analysis results for both machines are shown in Figures 7.14 thru 7.21 for 3500, 5500, and 7500 rpm operation. Results for the other speeds in the 3500 to 7500 rpm testing range are provided in the supplementary document to this thesis. The characteristics indicate that the q-axis reactance (X_q) remains almost linear and constant with torque angle for both machines. The magnet excited voltage (E_o) varies considerably for the BLM4035 PMSM, yet remains approximately linear and constant with torque angle for the BMF4035. The difference is mainly due to less fluctuation in the flux path reluctance of the BMF4035 for variations in speed and loading. A wide variation in the d-axis reactance (X_d) and the core loss resistance (R_c) is observed for both machines.

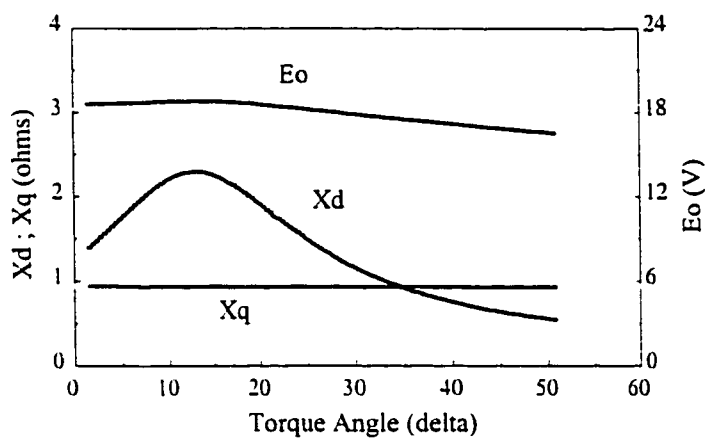


Figure 7.14 BLM4035 computed parameters at 3500 rpm

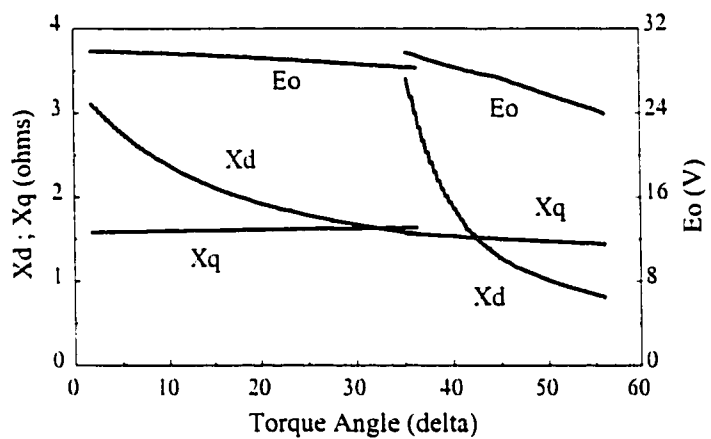


Figure 7.15 BLM4035 computed parameters at 5500 rpm

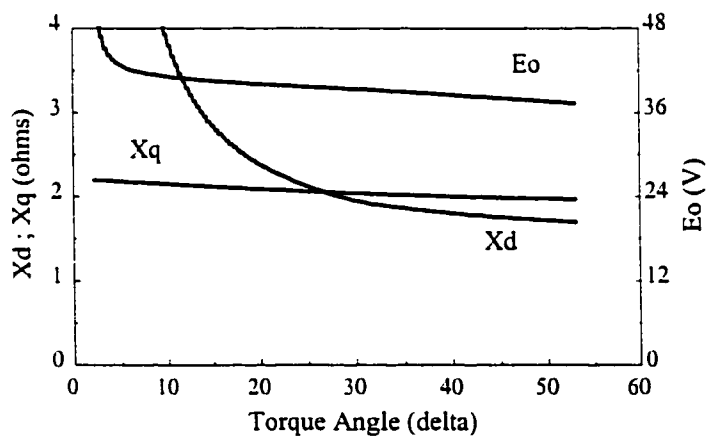


Figure 7.16 BLM4035 computed parameters at 7500 rpm

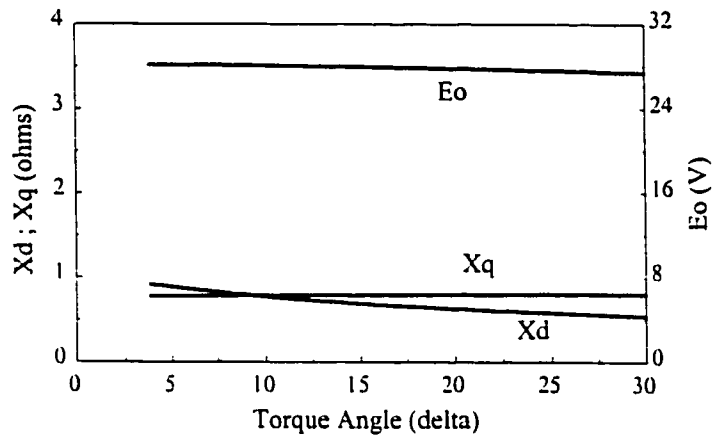


Figure 7.17 BMF4035 computed parameters at 3500 rpm

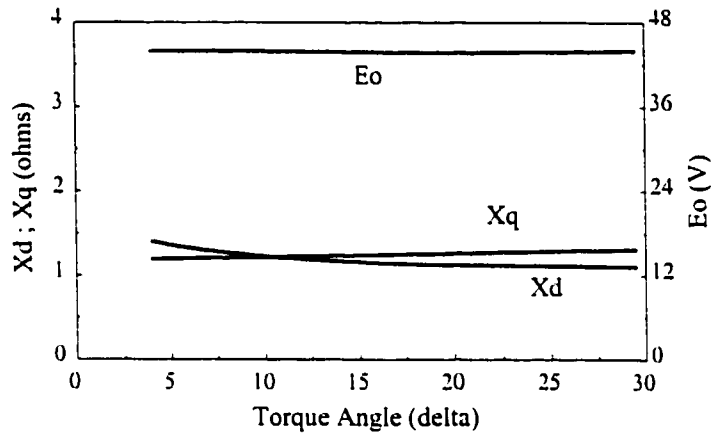


Figure 7.18 BMF4035 computed parameters at 5500 rpm

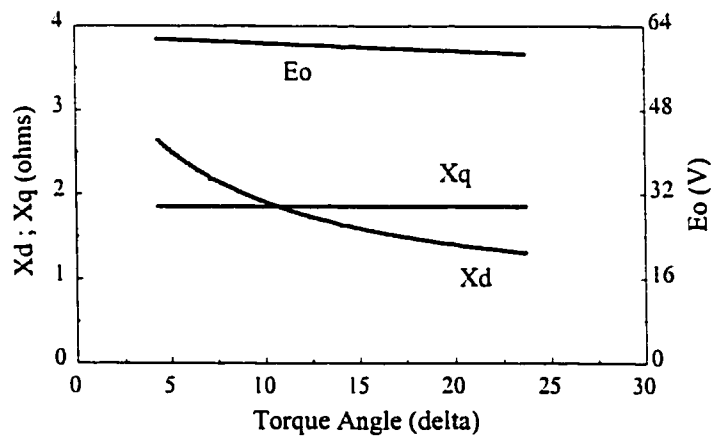


Figure 7.19 BMF4035 computed parameters at 7500 rpm

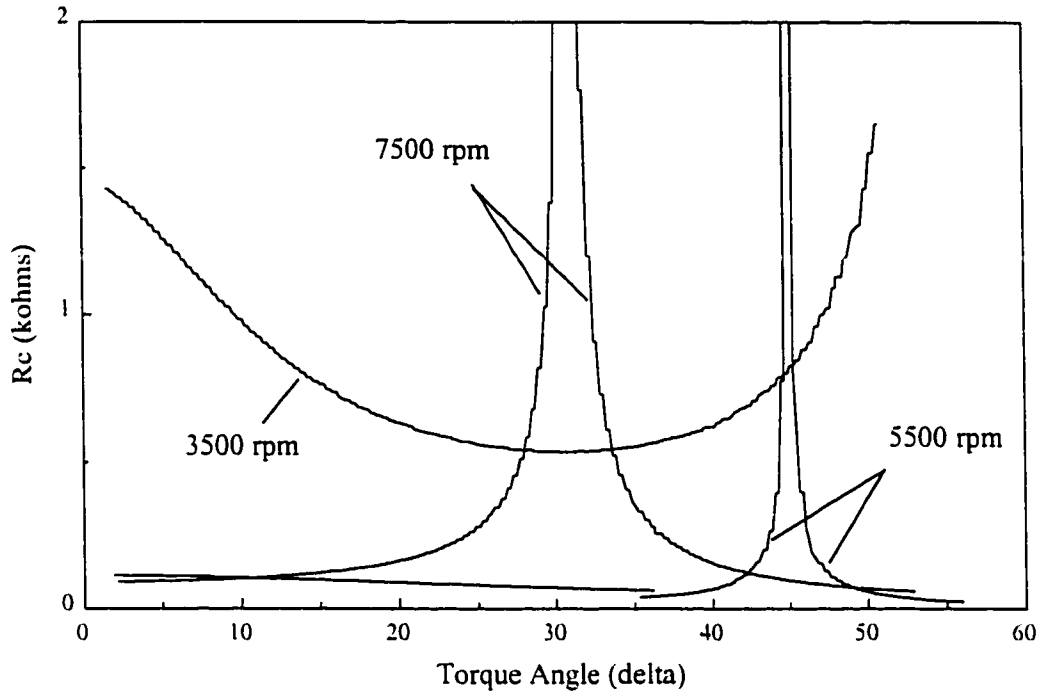


Figure 7.20 BLM4035 computer R_c

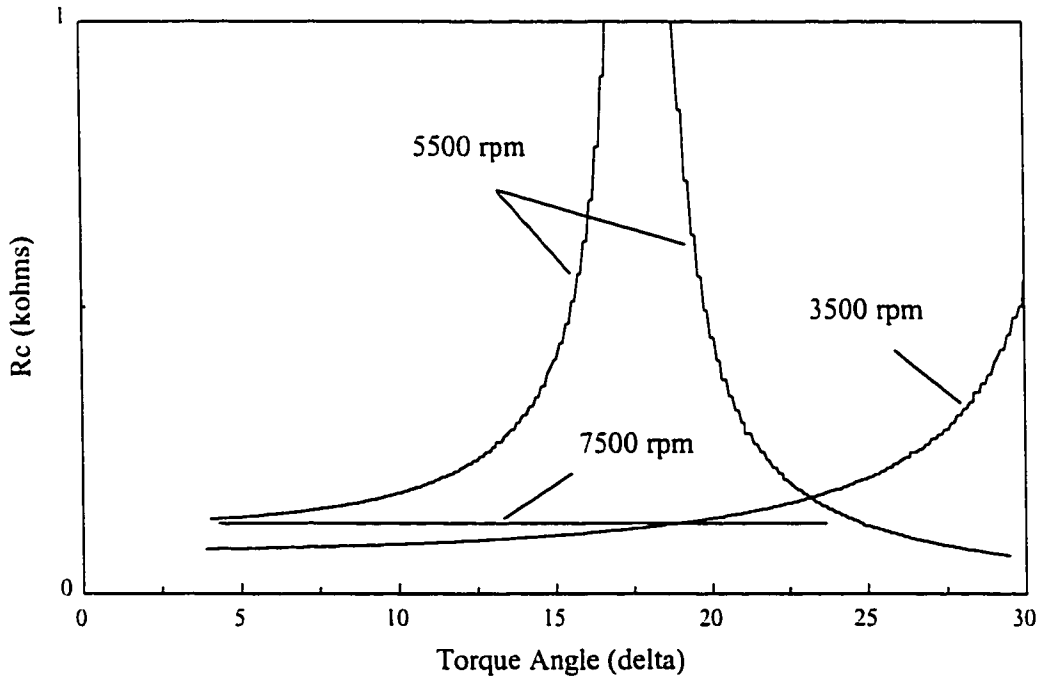


Figure 7.21 BMF4035 computed R_c

The work presented in this chapter provides a repeatable and accurate method to determine the dynamic parameters of the Figure 7.13 simplified equivalent circuit of a PMSM. Parameters identified with this method provide the necessary information to estimate the PMSM electrical torque and to determine the control rules for the high performance utilization of the torque producing terms in (6.39).

CHAPTER 8

TORQUE CONTROL

8.1 DYNAMIC PARAMETER TORQUE PRODUCTION

The parameters identified in the previous chapter provide the necessary information to calculate the theoretical electrical torque produced by the PMSMs. The general torque expression (6.39) is restated in terms of the excitation frequency dependent variables X_d , X_q , and E_o as (8.1).

$$T_e = \frac{3}{2} \cdot \frac{P}{\omega} \cdot [E_o i_q + i_d i_q (X_d - X_q)] \quad (8.1)$$

Variable values of X_d , X_q , and E_o are used to determine the dynamic parameter equivalent of (8.1) as shown in (8.2).

$$T_e(\delta, \omega) = \frac{3}{2} \cdot \frac{P}{\omega} \cdot [E_o(\delta, \omega) i_{oq} + i_{do} i_{qo} (X_d(\delta, \omega) - X_q(\delta, \omega))] \quad (8.2)$$

where:

$$i_{oq} = \frac{R_c(\delta, \omega) i_q - X_d(\delta, \omega) i_d - E_o(\delta, \omega)}{R_c(\delta, \omega) + R_c(\delta, \omega)^{-1} X_d(\delta, \omega) X_q(\delta, \omega)}$$

$$i_{do} = i_d + \frac{R_c(\delta, \omega) i_q - X_d(\delta, \omega) i_d - E_o(\delta, \omega)}{R_c(\delta, \omega)^2 X_q(\delta, \omega)^{-1} + X_d(\delta, \omega)}$$

Equation (8.1) is evaluated for the speed (ω) and torque angle (δ) ranges measured during the parameter identification tests. The dynamic characterization of X_d , X_q , E_o , and R_c is used to compare the calculated $T_e(\delta, \omega)$ with the manufacturer specified continuous

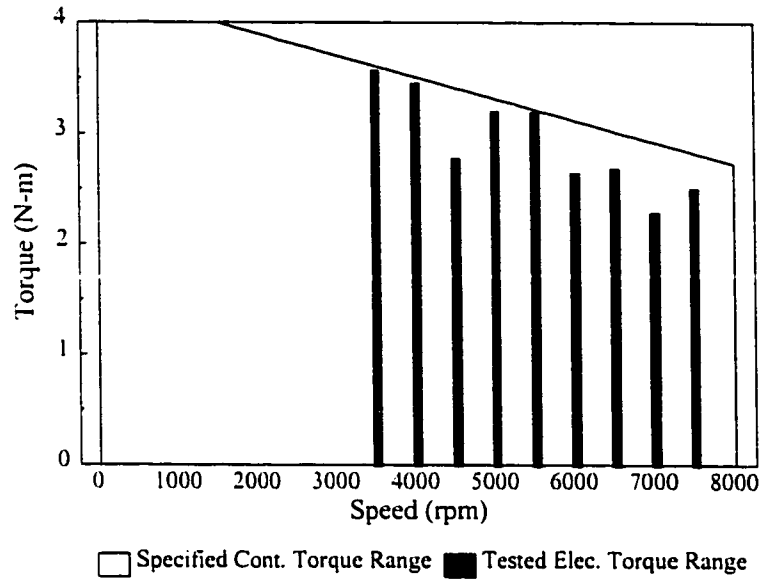


Figure 8.1 BLM4035 specified and tested torque range

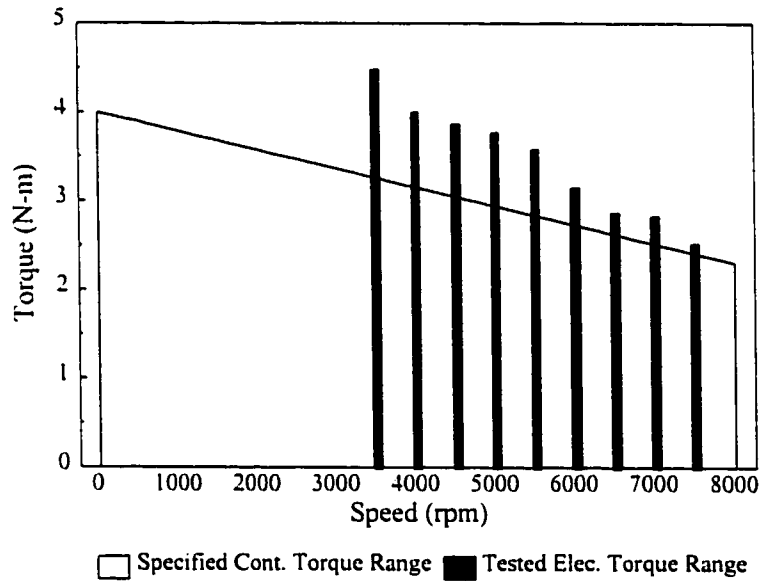


Figure 8.2 BMF4035 specified and tested torque range

torque capabilities. Figures (8.1) and (8.2) illustrate the results of this comparison. Parameter identification is conducted up to the maximum limits of the test machine. The results show that the continuous torque capabilities of the BLM4035 have been overstated by the

manufacturer. The calculated electrical torque should be higher than the manufacturer specified continuous torque as mechanical and stray load losses are not accounted for in (8.2). Evidently, the manufacturer has also realized this and is now recommending a 2 hp BMF4035 PMSM as a direct replacement for its 3 hp BLM4035 PMSM.

8.2 CONTROL IMPLICATIONS

8.2.1 Conventional Flux Weakening Control Trajectories

The high performance flux weakening current vector control setpoints i_d^* and i_q^* are typically programmed to optimize some drive performance criterion based on the knowledge of the PMSM parameters. A maximum torque per ampere trajectory was originally proposed in [34] as an efficient trajectory over which to control the stator currents of a PMSM. The current trajectory is calculated according to (8.3) and (8.4).

$$T'_{en} = \sqrt{i'_{dn} (i'_{dn} - l)^3} \quad (8.3)$$

$$T'_{en} = i'_{qn} \left[l + \sqrt{l + 4(i'_{dn})^2} \right] \quad (8.4)$$

Intermediate variables are determined by (8.5) thru (8.7).

$$T_{en} = \frac{T_e}{T_{eb}} \quad i_{qn} = \frac{i_q}{i_b} \quad i_{dn} = \frac{i_d}{i_b} \quad (8.5)$$

$$i_b = \frac{\Psi_{mag}}{(L_q - L_d)} \quad (8.6)$$

$$T_{eb} = \frac{3}{2} p \Psi_{mag} i_b \quad (8.7)$$

Equations (8.6) and (8.7) use constant values of Ψ_{mag} , L_d , and L_q that are assumed to

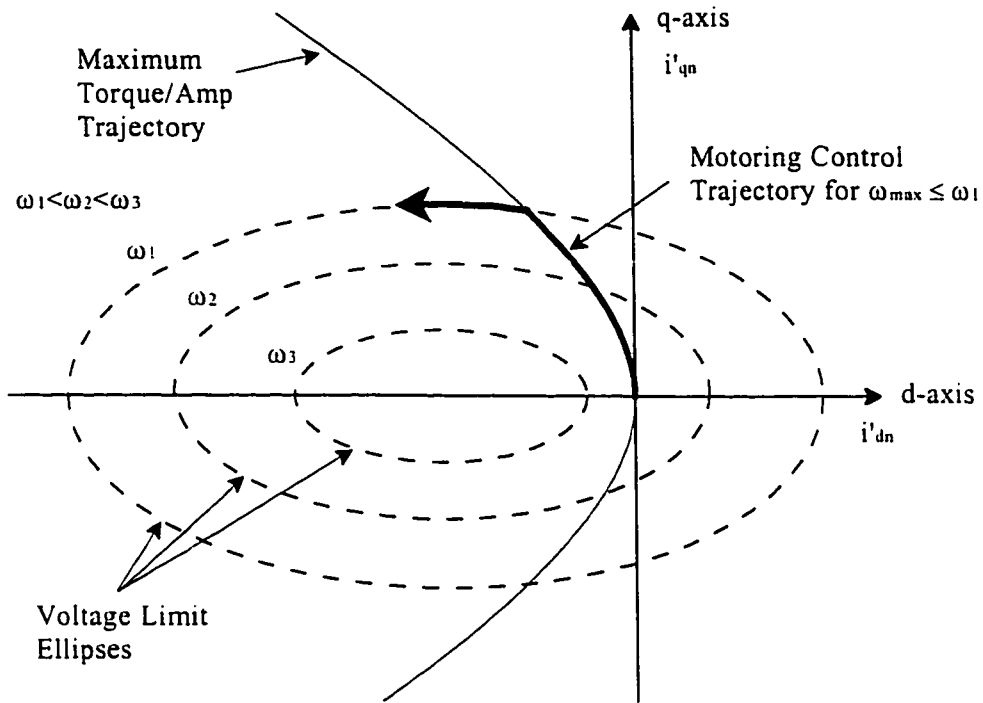


Figure 8.3 Conventional flux weakening motor control trajectory

be known by the drive designer. The values for i'_{dn} and i'_{qn} are calculated by simultaneously solving (8.3) and (8.4) at a set value for T'_{en} . Repeating the procedure for a range of T'_{en} values produces a maximum torque per ampere trajectory with the characteristic shown in Figure 8.3. The production of the commanded currents i'_{dn} and i'_{qn} is dependent on the machine parameters, the machine speed, and the voltage on the dc bus. Equation (8.8) provides a means to calculate the upper limit of current control allowed for a specific PMSM at a fixed dc bus voltage V_{dc} [39].

$$\left[\frac{V_o}{X_q} \right]^2 = i_q^2 + \left[\frac{X_d}{X_q} \right]^2 \cdot \left[i_d + \frac{\omega_e \Psi_{mag}}{X_d} \right]^2 \quad (8.8)$$

$$\text{where: } V_o = \frac{2}{\pi} V_{dc}$$

The voltage limit ellipses obtained from (8.8) take on the form shown in Figure 8.3. An increasing machine speed produces a smaller voltage limit ellipse. Improved flux weakening control is possible by forcing the operating point to the right once current regulator saturation is encountered at the voltage limit ellipse.

The concept of high performance torque control through current vector control along maximum torque per ampere trajectories and voltage limit ellipses has been widely implemented. Much work has been published in this area, however, only a few researchers have indicated that the assumption of a constant Ψ_{mag} , X_d , and X_q over the entire operating range of the machine may not be accurate [40][9]. The results from the parameter identification clearly show that the parameters Ψ_{mag} , X_d , and X_q vary significantly with the speed, loading, and machine type. Dynamic parameter identification of a PMSM allows the predicted maximum torque per ampere trajectories and voltage limit ellipses to be adjusted to account for operating point variances in the parameters. Equations (8.6) thru (8.8) should be converted to their dynamic parameter form by using the data obtained from the proposed parameter identification procedure. Adjustment of the pre-calculated control curves provides the capability to model the actual operation of the PMSM. An investigation into the influence of dynamic parameter utilization on the conventional high performance control trajectories is recommended for further work.

High performance current control based on the maximum torque per ampere trajectory determined by (8.3) and (8.4) does not provide operation at the highest possible efficiency. Other researchers have proposed alternative control methods, such as loss minimization control, to improve on the efficiency obtained with the maximum torque per ampere

strategy [41]. The proposed alternative control strategies still use fixed Ψ_{mag} , X_d , and X_q terms over the wide speed and loading operation of the PMSM, and as such, are subject to the same modelling inaccuracies as mentioned previously.

Maximum efficiency machine operation must consider the dynamic behaviour of both the phase current and voltage when calculating the efficiency of the torque production. The maximum torque conversion efficiency trajectories used in the PMSM parameter identification procedure reflect the need to operate the PMSM at the highest possible efficiency. Values of the actual d- and q-axis current components measured along the MTCE trajectory operation of both machines are shown for various speeds in Figures 8.4 and 8.5. The measured current components follow neither the characteristic of the maximum torque per ampere, nor the voltage limit ellipse trajectories of Figure 8.3. The presence of a discontinuity at 5500 rpm in Figure 8.4 indicates the requirement for dynamic control capabilities in the selection of i_d^* and i_q^* to maintain the highest efficiency operation of the PMSM. A com-

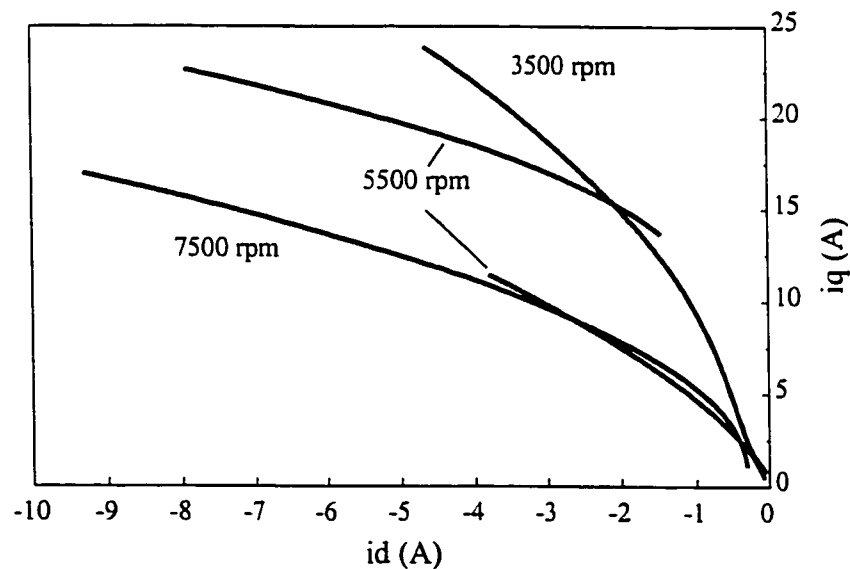


Figure 8.4 BLM4035 current trajectories for maximum torque conversion efficiency

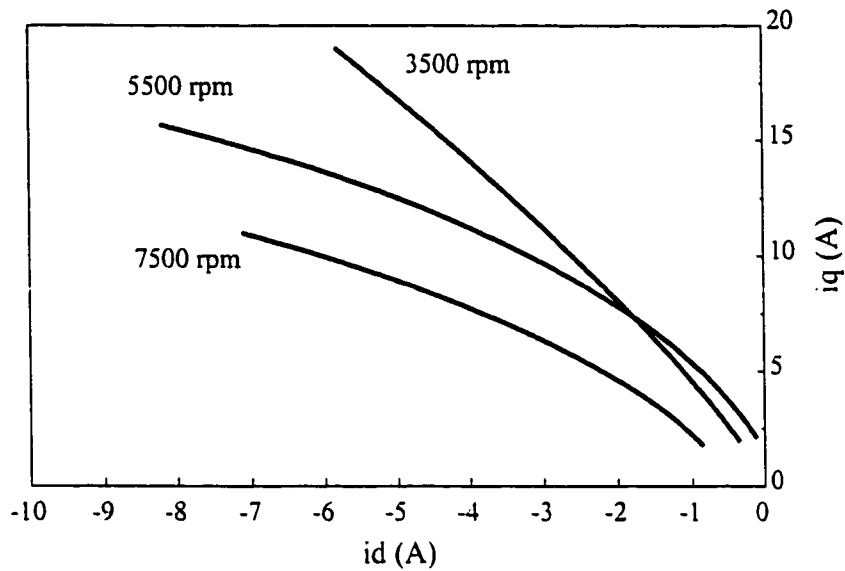


Figure 8.5 BMF4035 current trajectories for maximum torque conversion efficiency

parison between Figures 8.4 and 8.5 indicates that a wide variance in the current command values is possible for the MTCE operation of two different machines. Careful consideration of the desired machine type and operation should be made before adopting a strategy to produce the high performance flux weakening current vector control setpoints i_d^* and i_q^* .

8.2.2 High Performance FESS Torque Control

Many different control schemes are used to perform torque control of a PMSM in the high speed range of operation. The high performance drive in Chapter 5 allows for the flexibility to implement various types of control strategies by simply altering the 'torque control' routine in the 'auto' mode operation of the PMSMCON8 PC control program. A PMSM used in an EV high speed FESS requires the most efficient torque control possible to reduce losses and improve the driving range of the EV. Current control of the PMSM along the MTCE trajectories provides a suitable control strategy for the EV application of a FESS.

A high performance torque control block diagram that is suitable for the PC control implementation of MTCE trajectory operation of a high speed PMSM FESS is shown in Figure 8.6. A speed setpoint, corresponding to a desired stored flywheel energy value, is applied to the system and compared with the feedback value of actual speed of the PMSM. The contents of the control transfer function block is of PID type control and is optimized for a desired control response. An expanded version of the control transfer function block is provided in Figure 8.7 to illustrate the s-plane error gains K_1 to K_3 , and the block implementation.

The control transfer block determines the commanded speed control variable ω^* . A lookup table is used to determine the desired value of T_e^* for a particular value of ω^* . Rapid energy transfer into a FESS requires that the highest possible value for T_e^* is chosen for a specific ω^* . The upper envelope of the safe operating area torque-speed curve is used

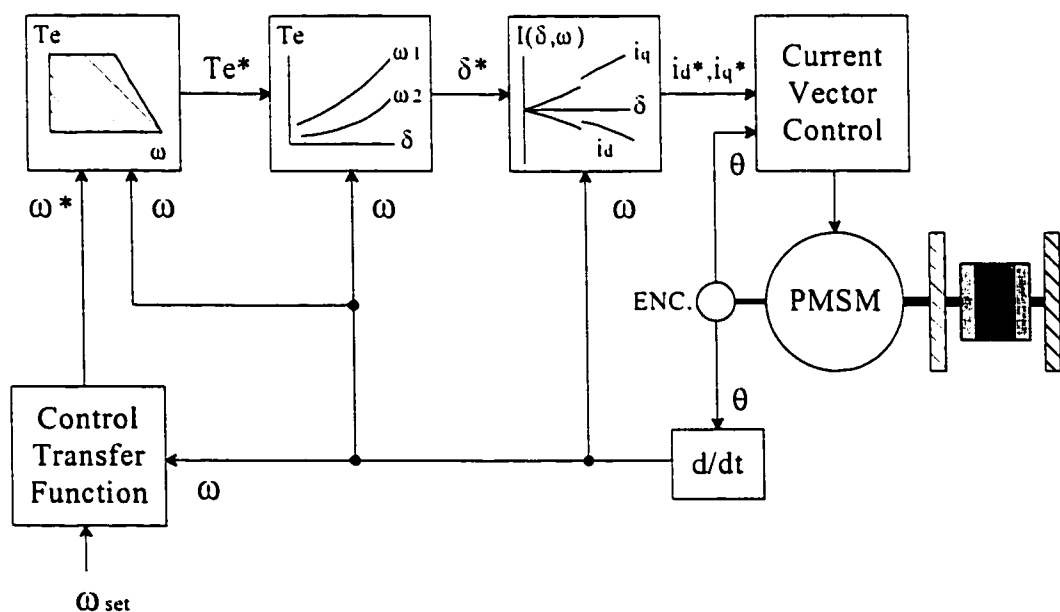


Figure 8.6 High performance torque control block diagram

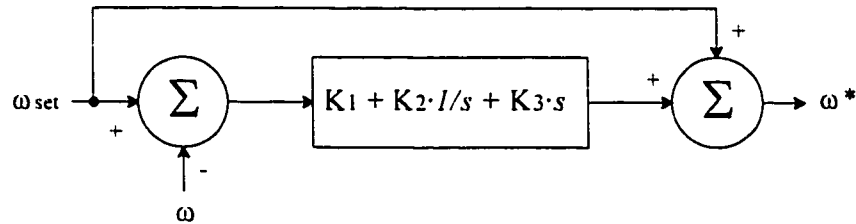


Figure 8.7 Control transfer function block layout

for this application, and is set according to the tested torque ranges illustrated in Figures 8.1 and 8.2.

Commanded electrical torque values are converted into the corresponding electrical torque angle commands δ^* through the application of the dynamic parameter general torque expression in (8.2). The dynamic parameters, determined in Chapter 7, are utilized to generate the T_e^* to δ^* mappings required for PMSM operation along the MTCE trajectories. Figures 8.8 and 8.9 show a sample of the required mappings for 3500, 5500, and 7500 rpm operation of the two PMSMs. Lookup tables are employed to calculate the values of δ^* as a function of T_e^* and the actual machine speed ω .

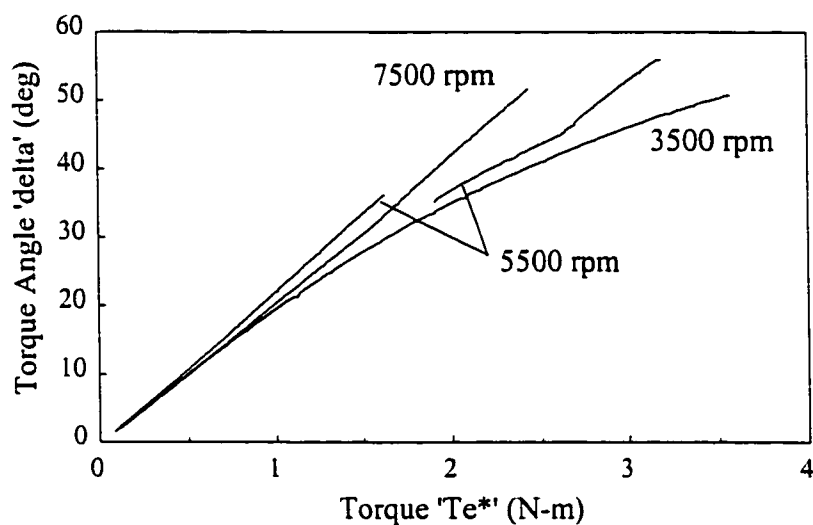


Figure 8.8 BLM4035 T_e^* to δ^* mapping for MTCE

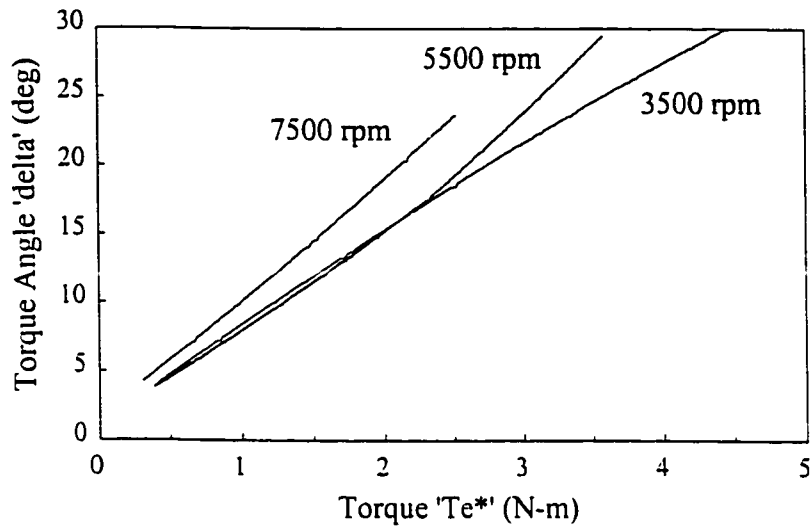


Figure 8.9 BMF4035 T_e^* to δ^* mapping for MTCE

The commanded torque angle values δ^* are processed further to determine the MTCE δ^* to i_d^* and i_q^* mappings. The speed and torque angle dependent values of i_d^* and i_q^* are calculated through the implementation of additional lookup tables in the PC control program. Figures 8.10 and 8.11 illustrate the δ^* to i_d^* and i_q^* mapping process for 3500, 5500, and 7500 rpm operation of the two PMSMs. The direct and quadrature current command

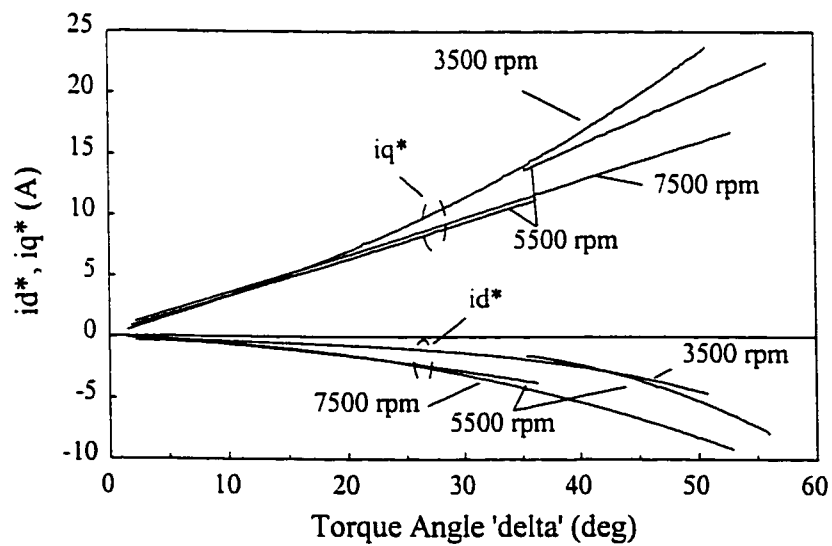


Figure 8.10 BLM4035 δ^* to i_d^* and i_q^* mapping for MTCE

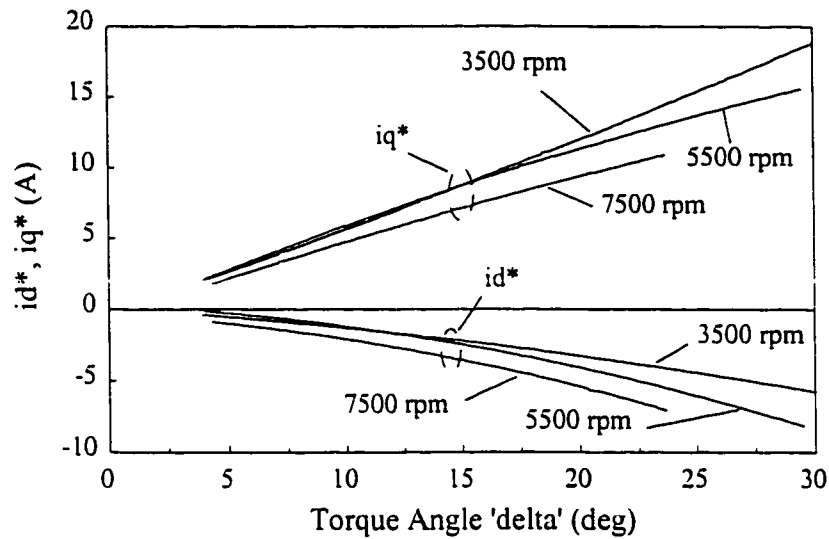


Figure 8.11 BMF4035 δ^* to i_d^* and i_q^* mapping for MTCE

values are converted into their phasor form to obtain the values of I_{mag}^* and I_{α}^* that are written by the high performance drive's control PC to the microcontroller shared memory. Processing speed is increased by using a direct mapping of the T_c^* command to the required I_{mag}^* and I_{α}^* values for a particular machine. Separate mapping of the control variables is used to demonstrate the implementation of the control process. A flowchart for the 'auto' mode implementation of the Figure 8.6 proposed high performance torque control is provided in Appendix B.

8.3 SIMULATION EXTENSIONS FOR THE PROPOSED TORQUE CONTROL

The parameter characterization of the test PMSMs allows for an accurate theoretical simulation of various high performance torque control strategies. Improved high speed performance through feedforward current regulator compensation of interior magnet type PMSM drives has been proposed in [42]. Current regulator compensation requires the modelling of the current regulator. Figures 8.12 shows the model used for the stationary

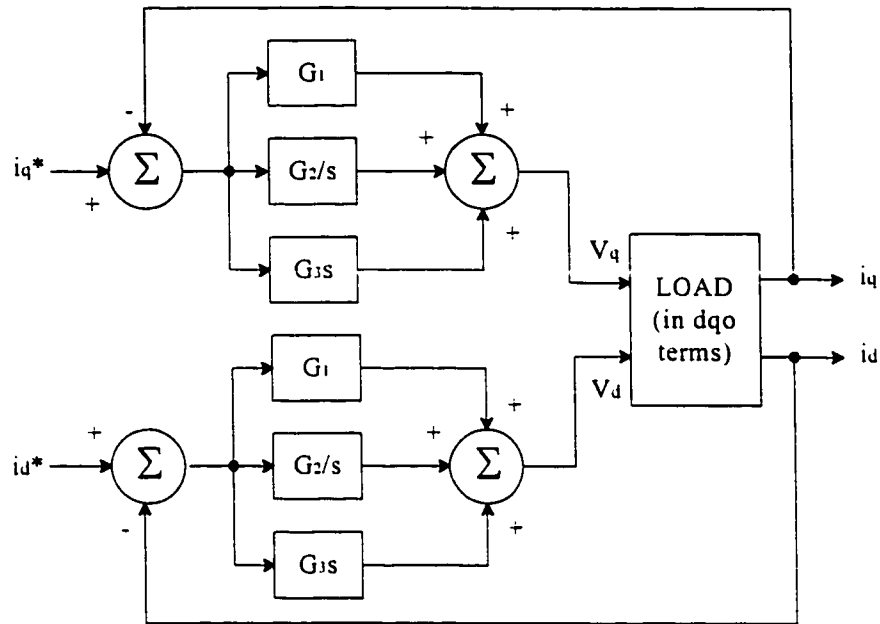


Figure 8.12 PID controlled current regulator representation in the stationary frame

frame representation of a PID controlled current regulator. The modelled current regulator reflects the type of CCSI used in the high performance drive for this thesis. Feedforward compensation is used to counteract the degrading influences of the reactive and back-EMF voltage drops on the stationary current regulator performance. Hence, i_d^* and i_q^* current control commands determined using the maximum torque per ampere and voltage limit ellipse trajectories are compensated to reflect the actual characteristics of the machine. Compensation is performed by replacing i_d^* and i_q^* with the compensated i_{dc}^* and i_{qc}^* current command values through the application of (8.9).

$$\begin{bmatrix} i_{qc}^* \\ i_{dc}^* \end{bmatrix} = \frac{1}{G'} \begin{bmatrix} (R_s' + G') & \omega_e L_d' \\ -\omega_e L_q' & (R_s' + G') \end{bmatrix} \cdot \begin{bmatrix} i_q^* \\ i_d^* \end{bmatrix} + \begin{bmatrix} \omega_e \\ 0 \end{bmatrix} \cdot \frac{\Psi_{mag}'}{G'} \quad (8.9)$$

The parameters R_s' , L_d' , L_q' , and Ψ_{mag}' are the measured values of the conventional PMSM equivalent circuit and G' is the gain operator ($G_1 + G_2s^{-1} + G_3s$) of the PID control.

The compensation scheme proposed in [42] acknowledges that it requires an accurate prior knowledge of the PMSM parameters, yet it uses constant parameter values. Improved feedforward compensation is possible through the use of the dynamic parameters identified in Chapter 7. Dynamic parameter characterization also allows for the accurate modelling of the load block in Figure 8.12. Figure 8.13 shows the model of a dynamic parameter characterized PMSM that can be used in conjunction with Figure 8.12 to study the effects of different torque control trajectories and feedforward compensation strategies. This novel model is derived from the implementation of the dynamic parameter torque

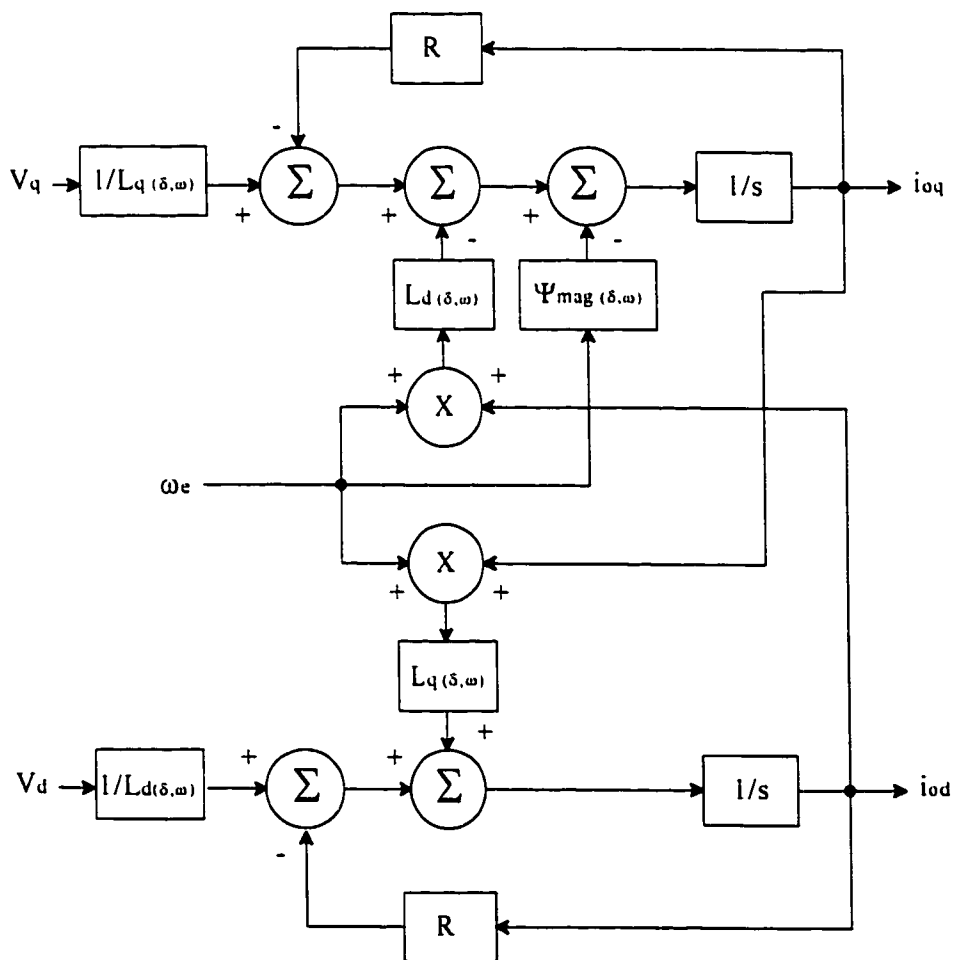


Figure 8.13 PMSM 'load' using dynamic parameter characterization

equation (8.2).

It is possible, in principle, to regulate the PMSM phase currents without any current feedback by using a feedforward compensator that is the exact inverse of the PMSM transfer function. Dynamic parameter identification allows for the determination of the PMSM transfer function and thereby provides a means to implement accurate high speed machine control without the need for current feedback. An investigation into the effects of the use of dynamic parameters, as opposed to the currently used static parameters, is proposed for further work.

CHAPTER 9

CONCLUSIONS AND FURTHER WORK

9.1 CONCLUSIONS

The work conducted for this thesis provides a practical guideline and reference for the actual implementation of a novel high speed flywheel energy storage system that can be used as a secondary energy storage unit for peak power transfer in an electric vehicles. Simulation and laboratory test results presented in this document have isolated problem areas and answered many questions relating to the realization of the proposed energy storage system.

The investigation into the simulated EV power and energy consumption reveals the large magnitudes and high rates of occurrence of the peak power stresses on the EV power supply. Simulation results of an electric powered standard passenger vehicle over the combined SAE J227a driving schedule show that approximately 88 kWh of stored energy, and approximately 70 kW of peak power capability are required to travel a distance of 200 km. Regenerative braking reduces the EV battery size by up to 13%, at the expense of applying additional peak power stresses on the battery. Simulation results show that the addition of a flywheel energy storage system effectively reduces the peak power stresses on the EV batteries and reduces the required battery size at the expense of adding more mass and complexity to the EV.

Optimization of the peak power sharing between the flywheel energy storage system and the EV batteries will reduce the overall EV energy storage requirements. Current technology, used to build an optimized energy storage system with both batteries and flywheel energy storage, will not provide a viably sized unit that can be used to provide EV performance that is similar to that of an ICE powered vehicle. Near-term technological improvements will reduce the energy storage system mass required for a 200 km operation of the optimized simulated EV from approximately 2200 kg to close to 1000 kg. The goal of a 1000 kg energy storage unit for the simulated EV represents the maximum size that can be allowed in order to produce a practical passenger type EV that is competitive with a conventional ICE powered vehicle. Though a practical flywheel energy storage system equipped EV is not possible with current technology, an investigation into the control requirements, implementation, and capabilities of a working prototype system that will compete with the ICE is still warranted.

Peak power transfer testing conducted on a laboratory prototype flywheel energy storage system has identified that a considerable delay exists between the peak acceleration and deceleration power requirements of the EV and the ability for the flywheel energy storage system to accommodate these requirements. Test results show that the use of a capacitor bank as a temporary energy storage tank improves the energy transfer capabilities of the FESS. The test results also show that while flywheel energy storage system discharging occurs at acceptable rates, the charging mode operation during EV braking must be improved.

The contributions of this thesis also include the development of a unique and prac-

tical, high efficiency sinusoidal phase current, microprocessor interfaced, vector controlled, high speed PMSM drive, that is suitable for the high performance charging mode operation of the flywheel energy storage system. Such a drive has been successfully demonstrated with this research. Sinusoidal phase current excitation is possible for up to 8000 rpm operation of the tested commercially available PMSMs. The laboratory prototype drive, interfaced with a real-time microprocessor based control scheme, has successfully demonstrated that it is possible to provide smooth current control over the entire high speed operating range of the test PMSMs.

High performance PMSM torque control is possible only through knowledge of the non-linear load dependent parameters of the PMSM, namely, X_d , X_q , R_s , and E_b . The novel parameter identification method, proposed in this thesis to identify the unknown machine parameters, demonstrates that it is possible to provide a repeatable and accurate characterization of the PMSM using only measurements of the input waveforms to the machine. Such characterization allows for the identification of machine discontinuities and provides a means to perform continuous current vector control through the PMSMs full operating range. The test machine characterization clearly indicates that there is a significant variation in the parameters required for high speed flux weakening operation of brushless permanent magnet synchronous machines, a fact often overlooked, or ignored, by many experts in this field. Assumptions of constant PMSM parameters for high performance torque control are incorrect. The parameter identification results should be used to supplement incomplete and inaccurate manufacturer data to allow for the high performance torque control of commercially available PMSMs.

Microprocessor control of the prototype PMSM drive provides a flexible means to implement dynamic parameter high performance torque control for different high speed machines without the need for drive reconfiguration. The work in this thesis has successfully isolated the machine drive from the control algorithm. New current vector control algorithms can be implemented using the control PC without any previous knowledge of the construction or operation of the actual drive.

9.2 RECOMMENDATIONS FOR FURTHER WORK

This investigation has identified five research areas that could provide additional theses topics. In the area of simulation, the EV simulation studies conducted in this thesis should be used as the initial work for a full scale EV simulation and test program. Completion of this work will allow for a comparison to be made to determine in what applications EVs can best compete with internal combustion engine powered vehicles.

A practical study should be conducted into the use of low voltage double layered capacitor modules as the sole secondary energy storage device in a load levelling strategy. Recent advances in power electronics provide an efficient means to provide a high EV dc bus voltage to low voltage double layered capacitor interface. Control of this interface could provide a light, inexpensive, and reliable means to store and supply peak EV power.

Peak power transfer testing of the laboratory prototype VSI drive indicates that the use of magnetic bearings, or a bearingless PMSM, with a vacuum housed flywheel will reduce the high losses experienced in this investigation. The use of a bearingless PMSM coupled to a vacuum housed flywheel is also recommended for further investigation.

The simplified current vector controlled voltage source inverter drive investigated during the peak power transfer testing in this thesis, should be enhanced to provide a micro-processor implementation of the counter preset (or phase angle advance) value. Such enhancement will produce a simple non-parametric controlled PMSM drive that is capable of higher speed operation than the high performance sinusoidal phase current, parametrically controlled PMSM drive developed in Chapter 5. The simplified drive will be a smaller and less expensive, but also less efficient, alternative to the high performance drive.

Dynamic parameter identification through the novel procedure demonstrated in this thesis provides a broad range of new information that can be applied to current static parameter control schemes. The effects of dynamic parameter application and load modelling on the current 'high' performance PMSM drive schemes should be investigated. Advances in microprocessors and the affordability of new digital signal processors makes high speed dynamic parameter control a realistic option for the enhancement of electric machine drives. The parameter identification method is not limited to PMSMs, and can be extended to determine the dqo vector control parameters of other synchronous machines. An investigation should be conducted to extend the identification procedure to determine parameters of vector controlled induction machines.

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APPENDIX A

TEST EQUIPMENT SPECIFICATIONS

A-1 80C196KD-20 MICROCONTROLLER

Part Number: 80C196KD20 Commercial CHMOS Microcontroller
Manufacturer: Intel
Specifications:

- 20 MHz Execution Speed
- 1024 Byte Register RAM
- 32 KByte of OTPROM
- Register to Register Architecture
- 28 Interrupt Sources / 16 Vectors
- 1.4 μ s 16x16 Bit Multiply
- 2.4 μ s 32/16 Bit Divide
- Powerdown and Idle Modes
- Five 8-Bit I/O Ports
- 16-Bit Watchdog Timer
- Dynamically Configurable 8-Bit or 16-Bit Buswidth
- Full Duplex Serial Port
- High Speed I/O Subsystem
- 16-Bit Timer
- 16-Bit Up/Down Counter with Capture
- Three Pulse Width Modulated Outputs
- Four 16-Bit Software Timers
- 8 or 10-Bit A/D Converter with Sample/Hold

A-2 SHAFT POSITION ENCODER

Part Number: CP-850-1250 Incremental Optical Shaft Encoder
Manufacturer: Computer Optical Products
Specifications:

- Incremental code
- +5Vdc @ 50mA power supply
- Channels A & B outputs in quadrature plus index pulse
- Linedriver outputs
- 100 kHz frequency response

A-3 87C751 MICROCONTROLLER

Part Number: S87C751-1N24 OTP CMOS Single Chip Microcontroller
 Manufacturer: Philips
 Specifications:

- 80C51 based architecture
- Inter-integrated serial bus interface
- 12MHz oscillator frequency
- Idle mode, power down mode
- 2kx8 ROM
- 64x8 RAM
- 16-bit auto reloadable timer
- Fixed-rate timer
- Boolean processor
- CMOS and TTL compatible
- LED drive outputs

A-4 BLM4035

Part Number: BLM4035A-ATAB00T
 Manufacturer: Cleveland Machine Controls (distributed by Electromate Industrial Sales)
 Specifications:

Continuous Torque (T_c):	36.4 lb-in	(4.11 N·m)
Peak Torque (T_p):	122 lb-in	(13.78 N·m)
Inertia (J_m):	0.008 lb-in-sec ²	(0.000904 N·m)
Maximum Speed:	8000 rpm	(837.76 rad/sec)
Static Torque (T_s):	0.89 oz-in	(6.285 E-03 N·m)
Vicious Friction (F):	3.9 oz-in/krpm	(27.54 E-03 N·m/krpm)
Cogging Torque (T_c):	2.5 lb-in	(17.65 E-03 N·m)
Thermal Resistivity (R_{th}):	0.6 deg C/watt	
Thermal Time Constant (T_{th}):	60 minutes	
Mechanical Time Constant (t_m):	4.4 msec	
Electrical Time Constant (t_e):	6.9 msec	
Weight (W):	19 lbs	(8.62 kg)
Max Continuous Power (P_m):	3.07 hp	(2.29 kW)
Magnet Type:	Interior Ferrite/Ceramic	
Motor Efficiency Characteristic:	Approximately 90%	
Number of Pole Pairs:	Two pairs, four poles total	
Form Factor (K_D, K_Q):	0.910	
Stator Inductance:	1.863 mH balanced on all 3 phases	
Back EMF (k_v):	24.9 Volts/krpm	(0.228 V/rad/sec)
Stator Resistance Line-line (R_λ):	0.27 ohms	
Torque Sensitivity (K_T):	2.1 lb-in/Amp	(0.237 N·m/Amp)

A-5 BMF4035

Part Number: BMF4035FHB000500A
 Manufacturer: Cleveland Machine Controls (distributed by Electromate Industrial Sales)
 Specifications:

Continuous Torque (T_c):	35 lb-in	(3.95 N·m)
Peak Torque (T_p):	134 lb-in	(15.1 N·m)
Inertia (J_m):	0.0032 lb-in-sec ²	(0.00036 N·m)
Maximum Speed:	6000 rpm	(837.76 rad/sec)
Static Friction (T_s):	125 oz-in	(.014 N·m)
Weight (W):	12 lbs	(5.4 kg)
Max Continuous Power (P_m):	1.49 hp	(2.29 kW)
Magnet Type:	Neodymium-Iron-Boron	
Motor Efficiency Characteristic:	Approximately 90%	
Number of Pole Pairs:	Two pairs, four poles total	
Stator Inductance:	Not Specified, balanced on all 3 phases	
Back EMF (k_v):	19.9 V/krpm	(0.182 V/rad/sec)
Stator Resistance Line-line (R_λ):	0.57 ohms	
Torque Sensitivity (K_T):	2.35 lb-in/Amp	(0.265 N·m/Amp)

A-6 DATA ACQUISITION SYSTEM

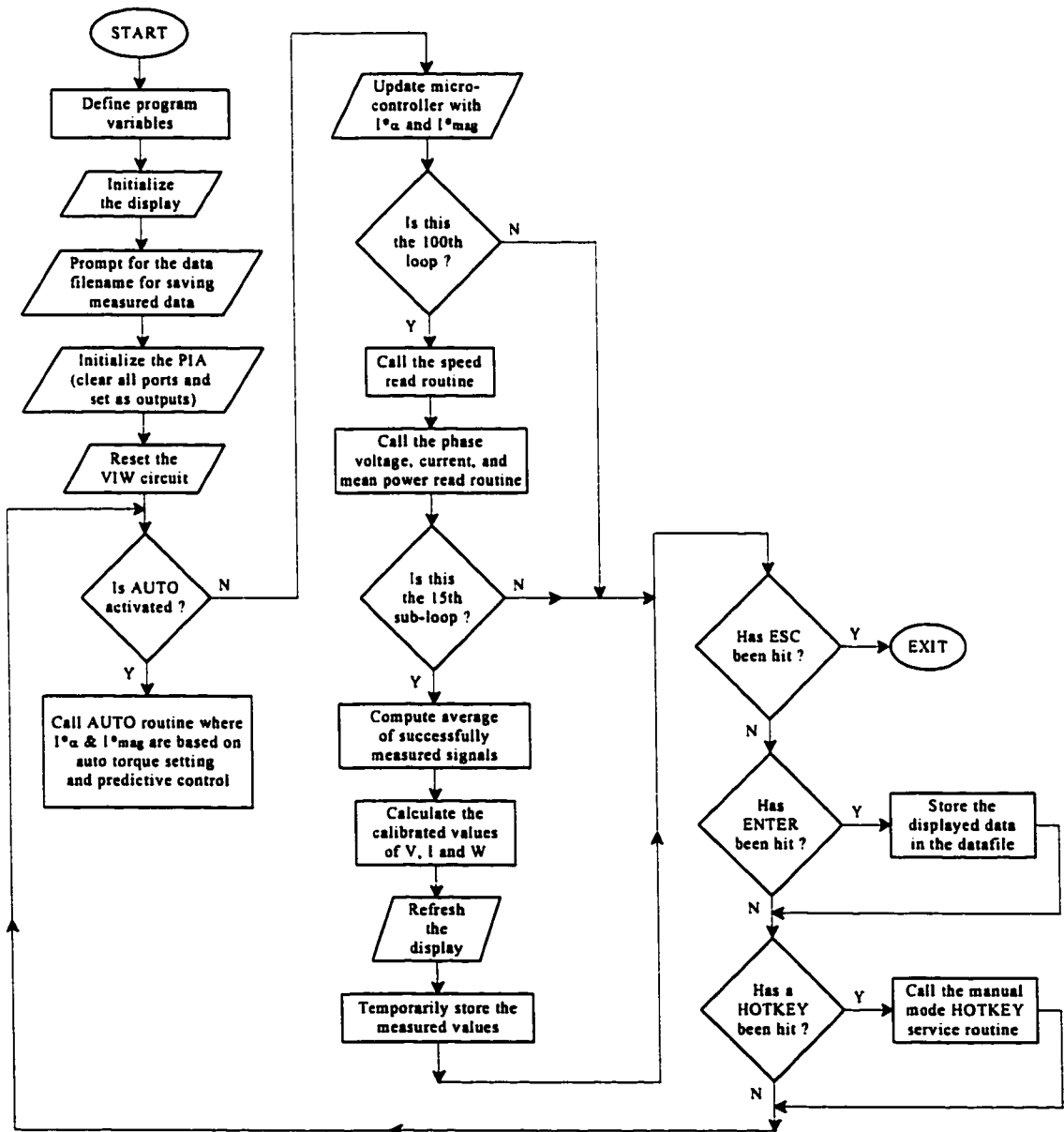
Part Number: DAS-1600
 Manufacturer: Keithley Metrabyte
 Specifications:

- 16 single ended or eight differential analog input channels
- Unipolar (0-10V) or bipolar ($\pm 5V$) analog inputs
- Programmable input gains
- 12-bit sampling resolution at a maximum 100 ksamples/s
- Switch configurable base address and Direct Memory Address
- Burst mode sampling capability
- Software, onboard pacer clock, or external pacer clock A/D start
- 8-bit data transfers to the ISA bus
- 3-channel programmable counter/timer
- Four unidirectional digital inputs and 4 unidirectional digital outputs

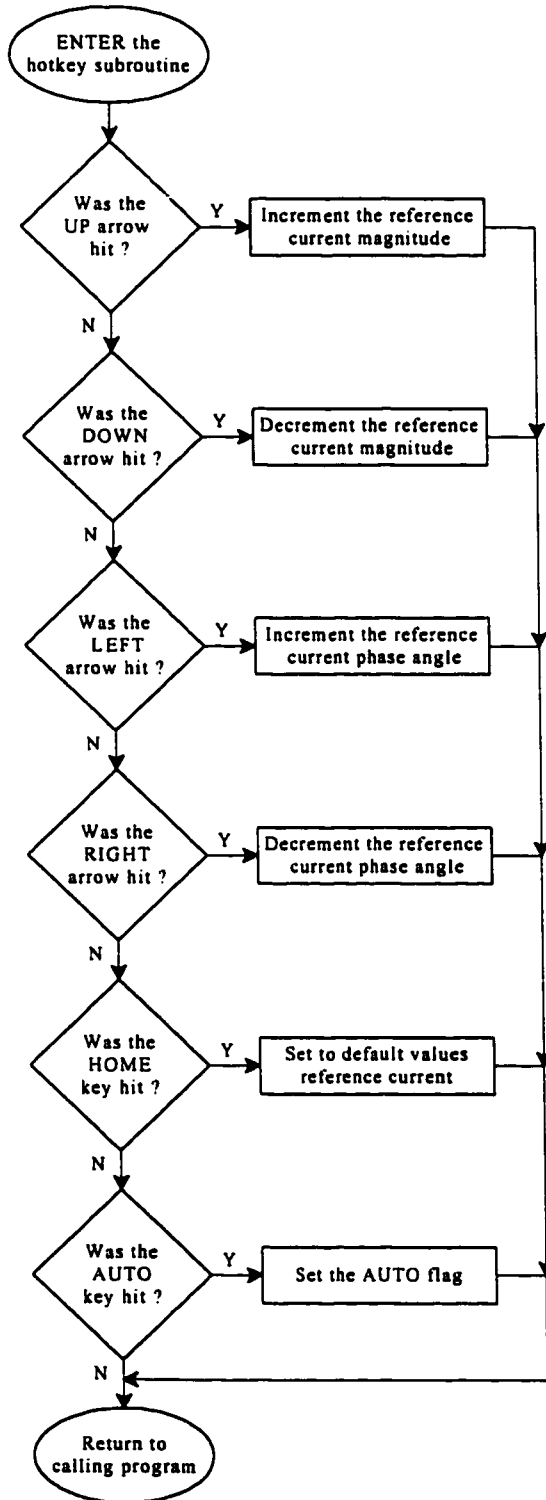
APPENDIX B FLOWCHARTS

B-1 PC CONTROL PROGRAM

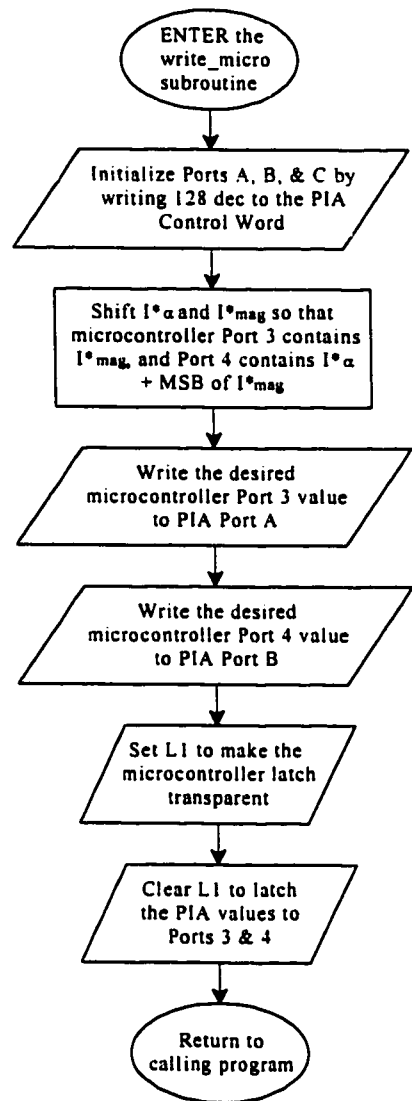
Main Program



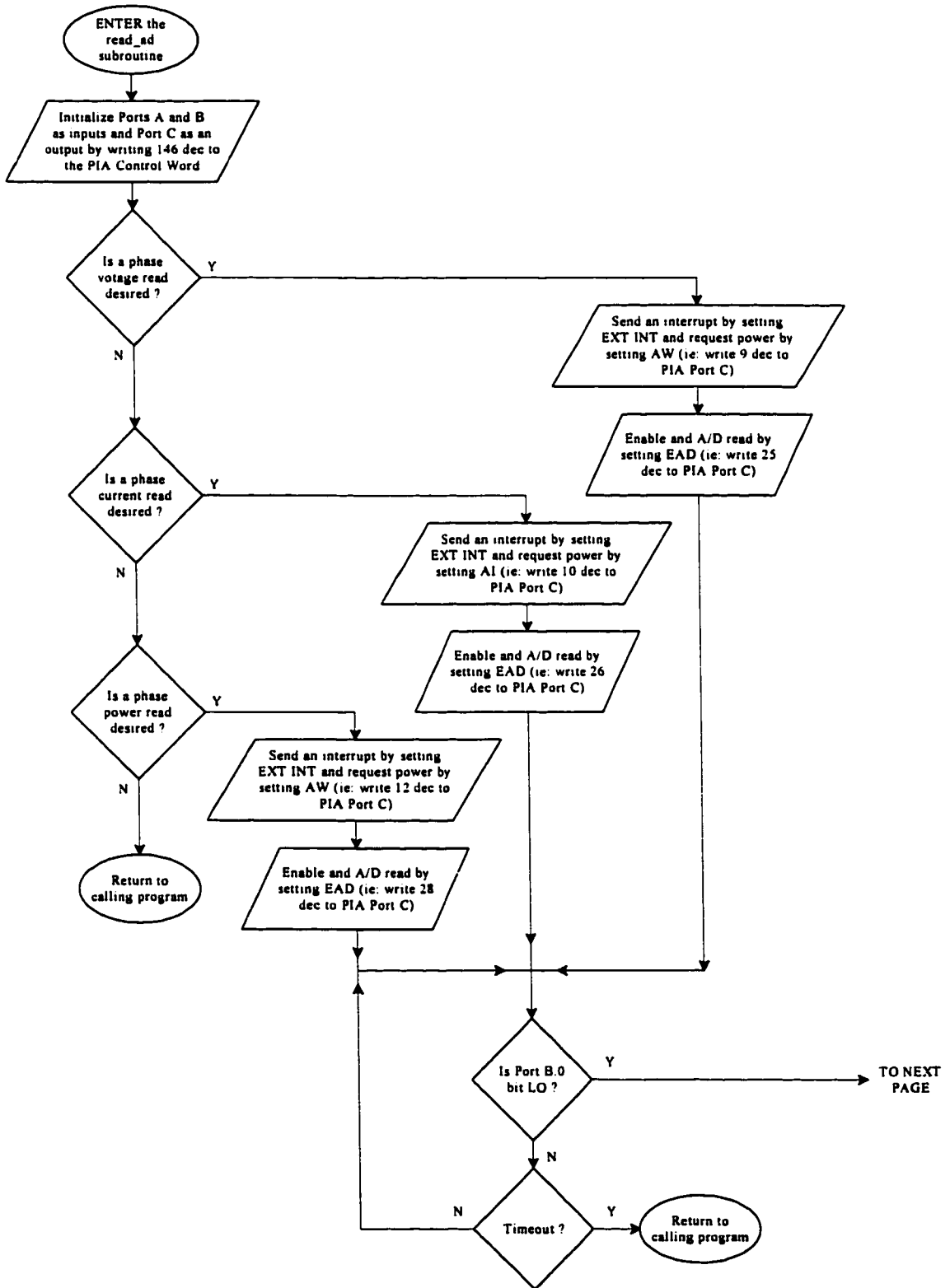
Manual Mode Hotkey Subroutine



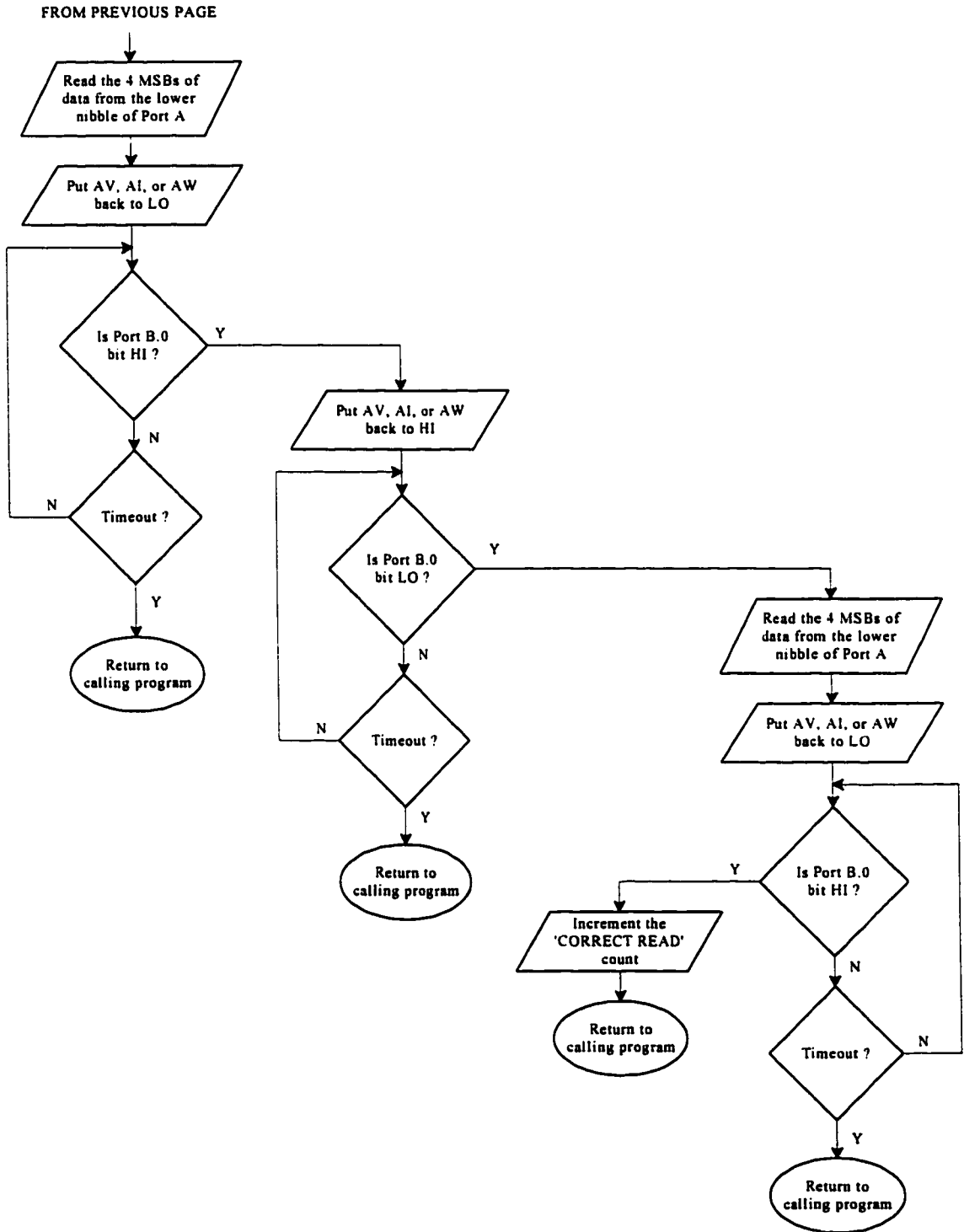
Write to Microcontroller Subroutine



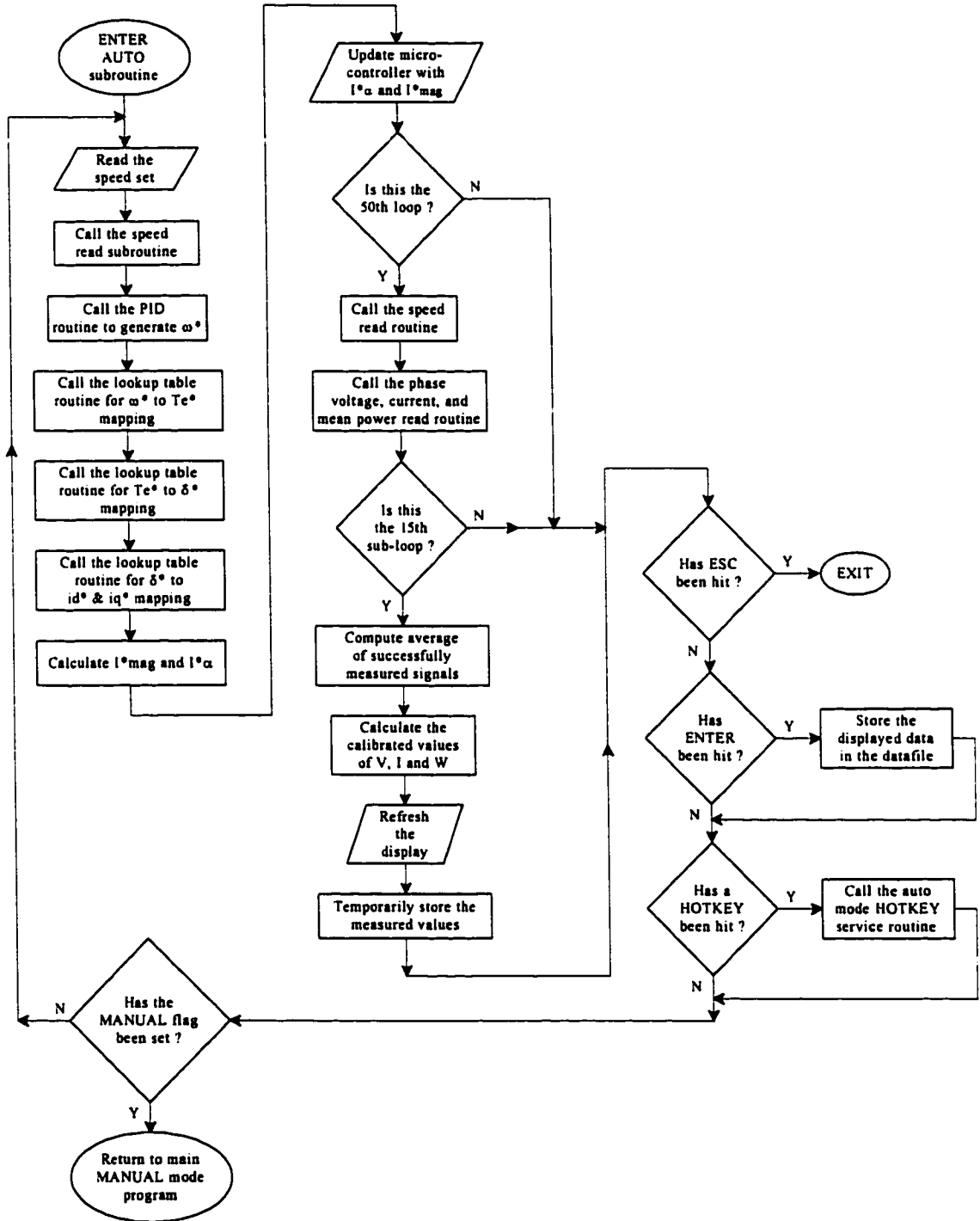
Analog Signal (VTW) Read Subroutine



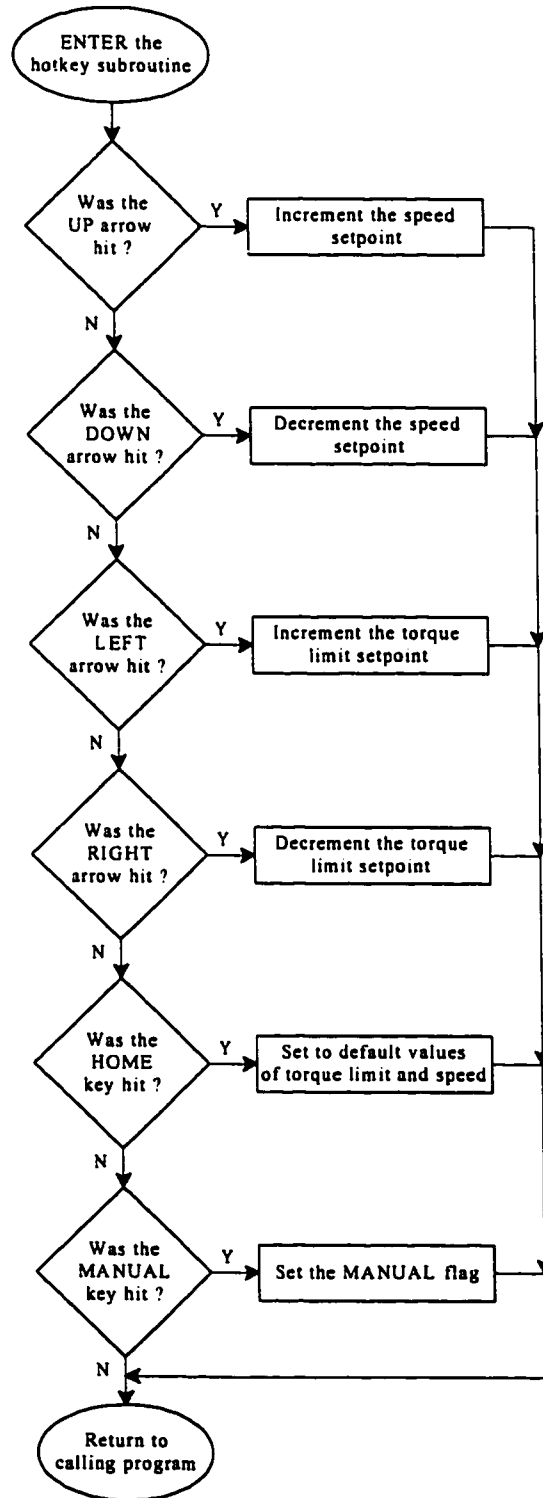
Analog Signal (VTW) Read Subroutine (contd.)



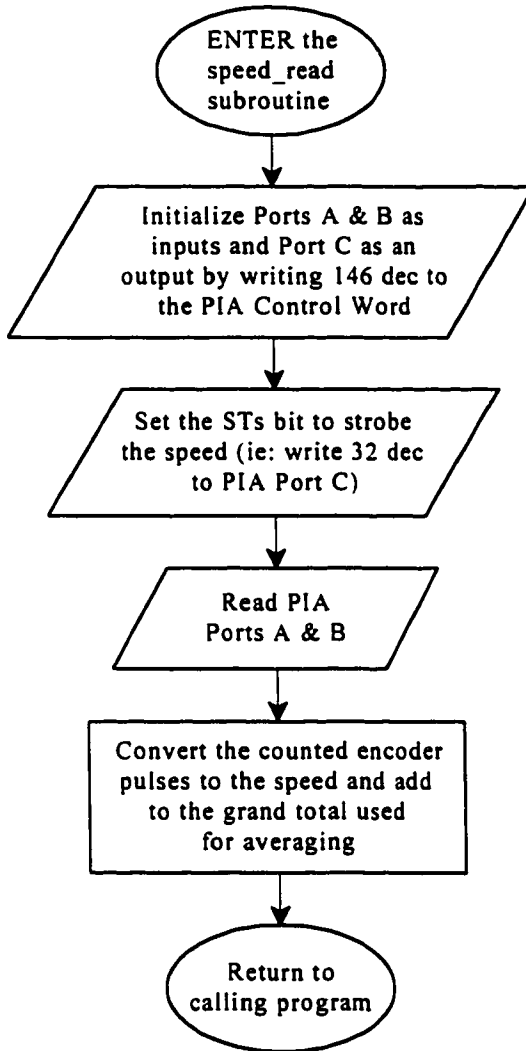
Auto Control Mode Subroutine



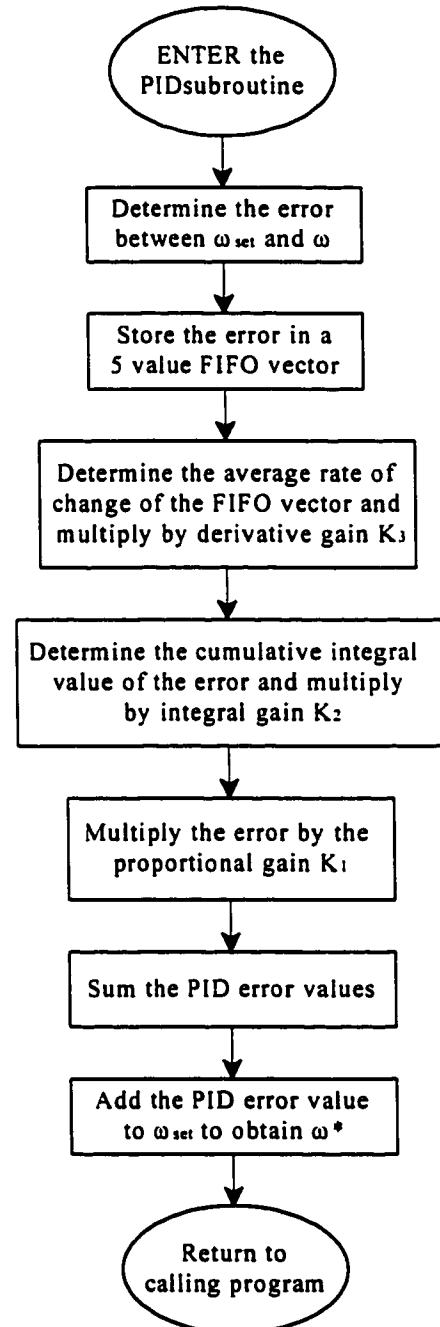
Auto Mode Hotkey Subroutine



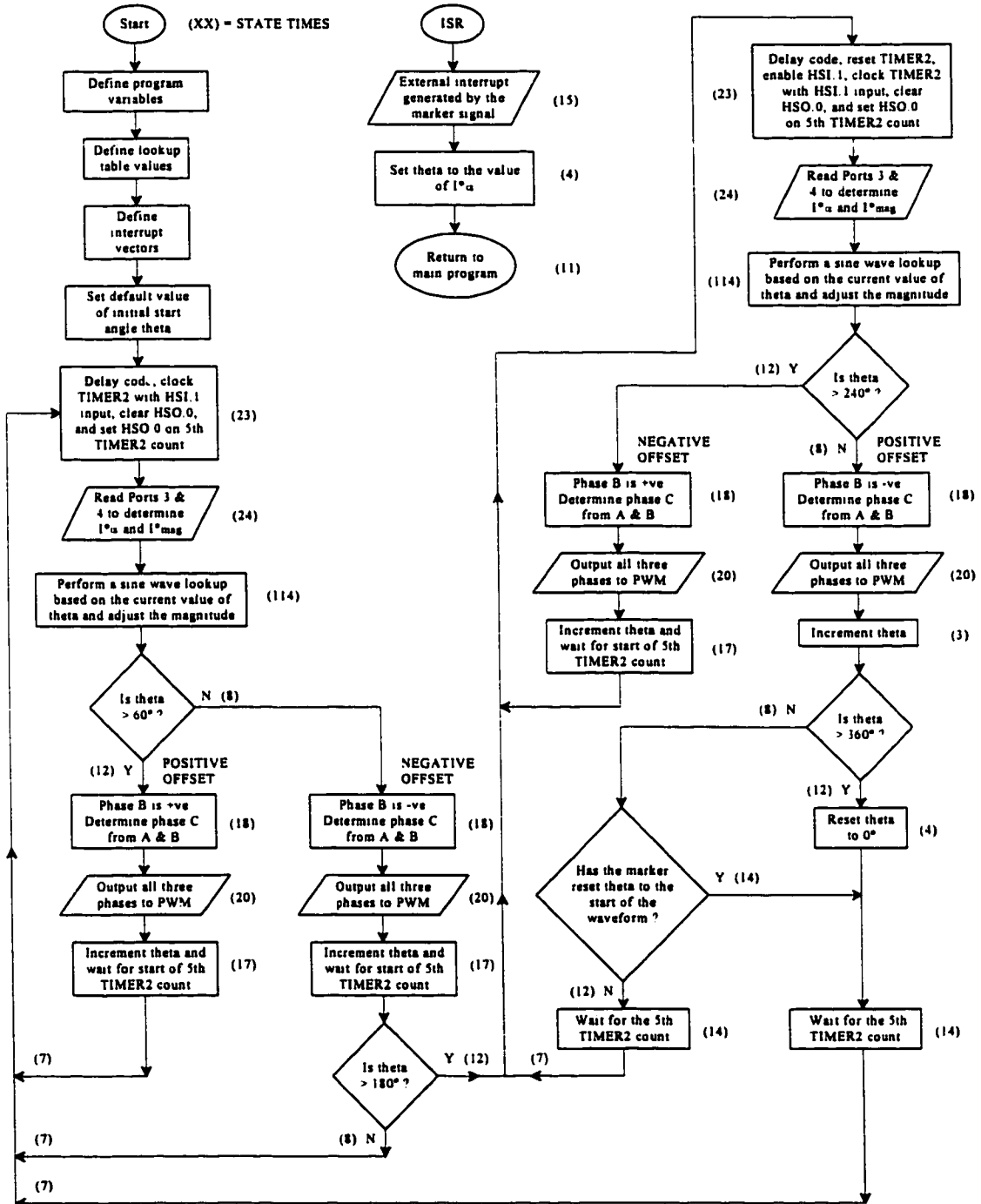
Speed Read Subroutine



PID Control Subroutine

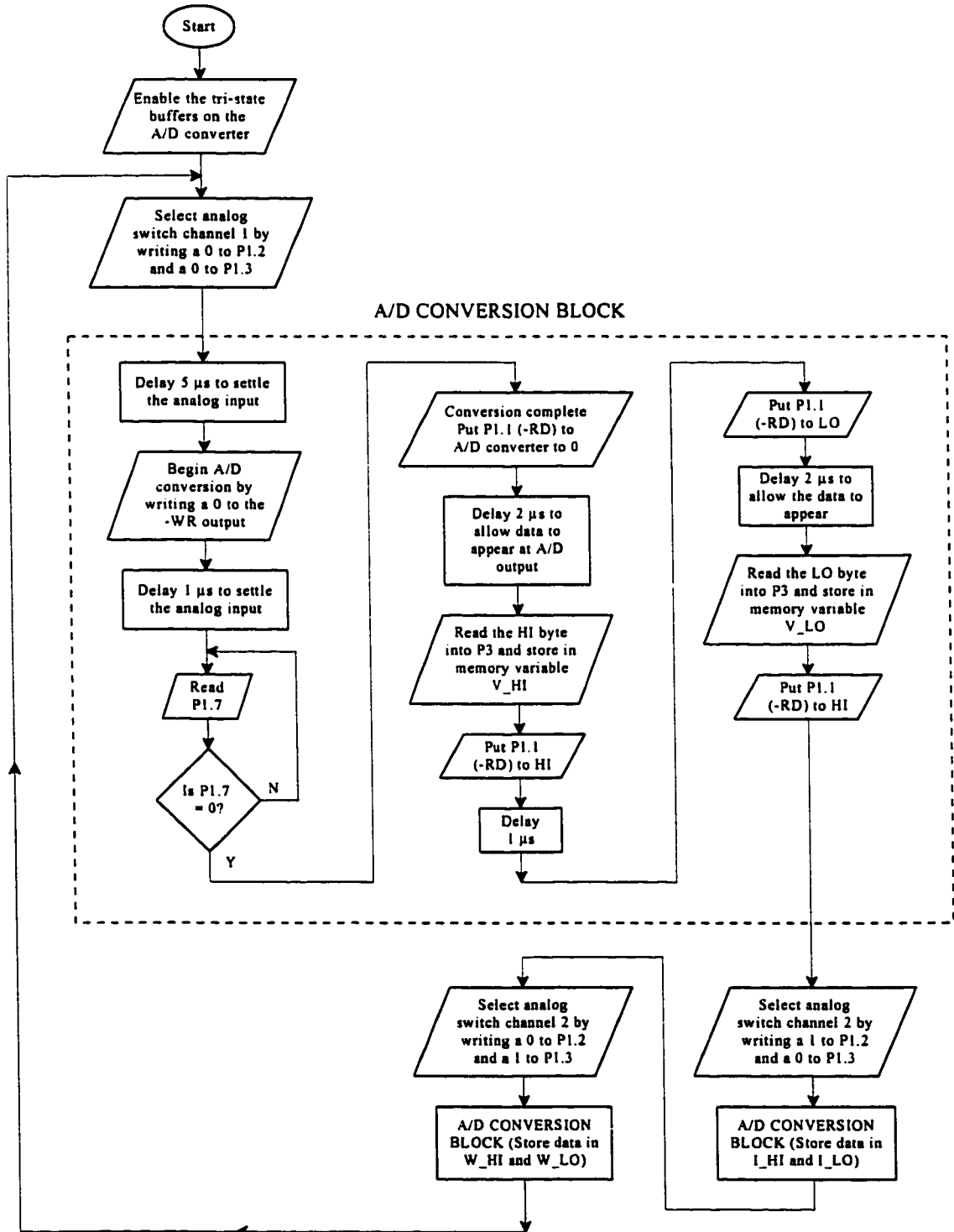


B-2 80C196KD20 MICROCONTROLLER PROGRAM

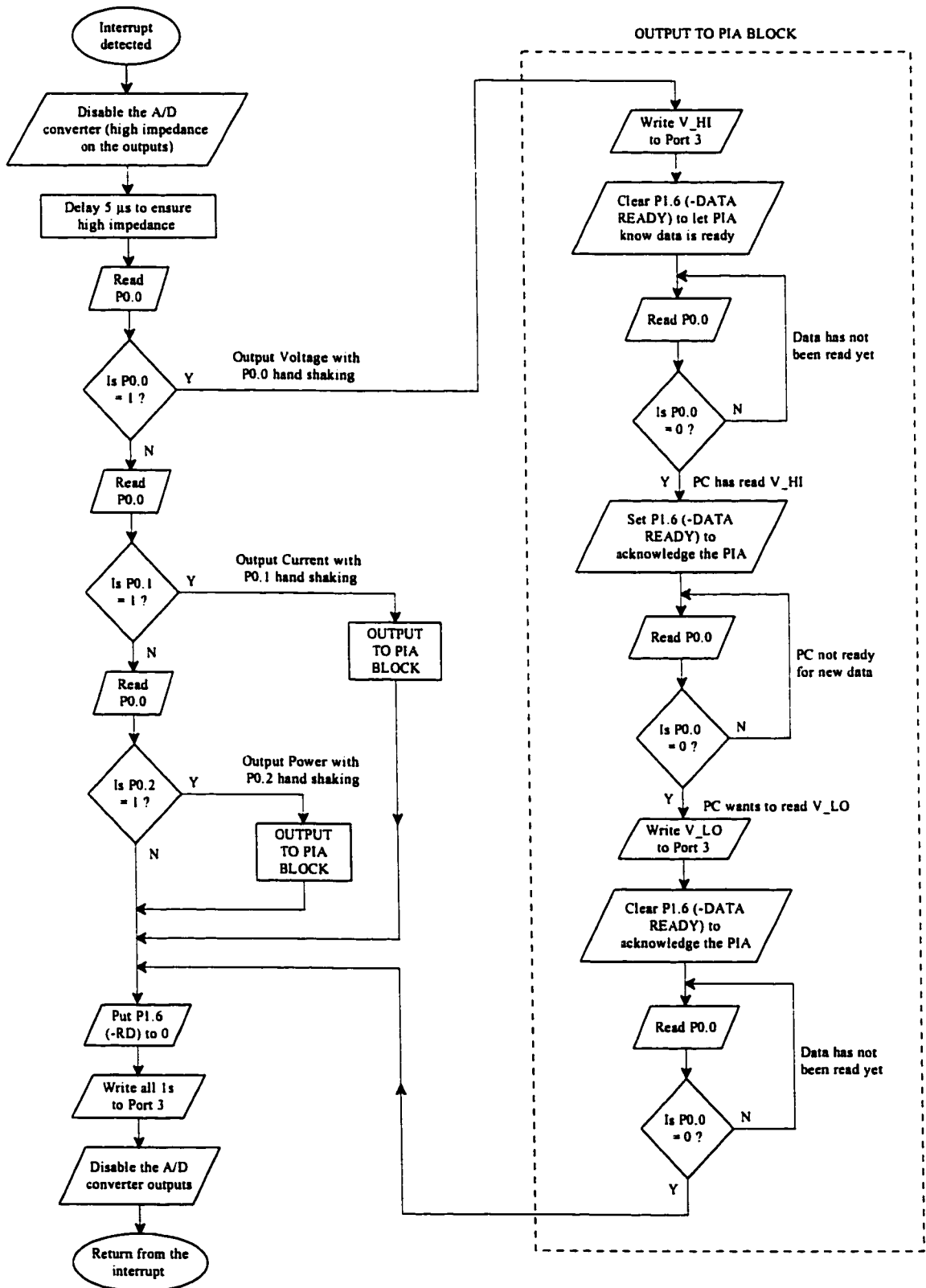


B-3 87C751 (VIW CIRCUIT) MICROCONTROLLER PROGRAM

Main Program



Interrupt Service Routine



APPENDIX C

MEASURED PROPERTIES

C-1 BACK-EMF MEASUREMENT AND Q-AXIS ESTABLISHMENT

BLM4035 Back EMF Measurement and q-axis Establishment

Fltname	Speed (rpm)	V Phase A	DF (%)	THDF	Adjusted V Phase A	Calculated phi-q	BW Filter CF	Adjusted phi-q	Sampling Error CF	Final phi-q	Lowpassd phi-q
VM30 FUR	1009	18.81	1.07	1.001287	18.81	-221.19	6.86	-214.73	0.43	-215.18	-215.18
VM35 FUR	1503	19.51	1.07	1.001286	19.50	-222.34	7.99	-214.15	0.53	-214.88	-215.18
VM40 FUR	4002	22.23	1.03	1.001287	22.22	-224.33	9.12	-213.21	0.60	-215.81	-215.18
VM45 FUR	4503	24.98	1.01	1.001258	24.95	-224.83	10.27	-214.58	0.68	-215.26	-215.18
VM50 FUR	1010	27.71	1.08	1.001241	27.68	-222.82	11.42	-214.40	0.73	-215.15	-215.18
VM55 FUR	1520	30.50	1.91	1.001210	30.46	-227.34	12.59	-214.95	0.83	-215.78	-215.18
VM60 FUR	6040	13.22	1.90	1.001202	13.28	-228.01	13.77	-214.24	0.91	-215.14	-215.18
VM65 FUR	4527	14.04	1.75	1.001128	14.00	-229.15	14.88	-214.47	0.98	-215.45	-215.18
VM70 FUR	7050	18.72	1.69	1.001101	18.68	-230.18	16.07	-214.31	1.06	-215.36	-215.18
VM75 FUR	7490	41.18	1.57	1.001048	41.14	-231.97	17.08	-214.89	1.12	-216.02	-215.18
VM80 FUR	8010	43.93	1.56	1.001040	43.88	-232.20	18.26	-213.84	1.20	-215.14	-215.18

PHASE VOLTAGE REGRESSION

Regression Statistics

Multiple R: 0.999988671
R Square: 0.999977343
Adjusted R Square: 0.999974825
Standard Error: 0.043272246
Observations: 11

Analysis of Variance

df	Sum of Squares	Mean Square	F	Significance F	
Regression	1	814.12640835913	814.12640835913	197216	1.244982689213E-22
Residual	9	0.018048186256615	0.0020053540729572		
Total	10	814.14282454544			

	Coefficients	Standard Error	t Statistic	P-value	Lower 95.0%	Upper 95.0%
Intercept	0.545718726	0.049381225546987	11.011041343884	6.53E-07	0.43203083291607	0.6534468190358
x1	0.005423462	8.60524445011318E-06	630.25071482066	0	0.00540339951741338	0.005443292800778

BACK EMF Coefficient: 5.423462 Volts/krpm

BMF4035 Back EMF Measurement and q-axis Establishment

Fltname	Speed (rpm)	V Phase A	DF (%)	THDF	Adjusted V Phase A	Calculated phi-q	BW Filter CF	Adjusted phi-q	Sampling Error CF	Final phi-q	Lowpassd phi-q
VM30CRP FUR	3019	24.99	1.39	1.000124	24.99	-176.41	6.88	-169.53	0.43	-169.98	-170.5
VM35CRP FUR	1512	28.94	1.34	1.000119	28.94	-177.90	8.01	-169.89	0.53	-170.42	-170.5
VM40CRP FUR	4001	32.88	1.41	1.000130	32.88	-179.22	9.12	-170.10	0.60	-170.70	-170.5
VM45CRP FUR	4499	36.76	1.47	1.000109	36.76	-180.37	10.26	-170.11	0.67	-170.79	-170.5
VM50CRP FUR	5004	40.88	1.42	1.000130	40.87	-181.33	11.41	-169.94	0.73	-170.69	-170.5
VM55CRP FUR	5509	44.98	1.44	1.000104	44.98	-181.79	12.56	-169.23	0.83	-170.06	-170.5
VM60CRP FUR	6006	49.02	1.42	1.000131	49.01	-183.69	13.69	-170.00	0.90	-170.90	-170.5
VM65CRP FUR	6517	53.2	1.35	1.000091	53.20	-184.70	14.86	-169.86	0.98	-170.62	-170.5
VM70CRP FUR	7008	57.18	1.02	1.000022	57.16	-186.79	15.97	-170.42	1.05	-171.47	-170.5
VM75CRP FUR	7504	61.18	1.04	1.000024	61.16	-185.92	17.11	-168.81	1.13	-169.94	-170.5
VM80CRP FUR	8004	65.23	0.97	1.000047	65.23	-184.75	18.25	-168.50	1.20	-169.70	-170.5

PHASE VOLTAGE REGRESSION

Regression Statistics

Multiple R: 0.9999970183
R Square: 0.9999815466
Adjusted R Square: 0.9999795118
Standard Error: 0.040540141
Observations: 11

Analysis of Variance

df	Sum of Squares	Mean Square	F	Significance F	
Regression	1	1791.7183340251	1791.7183340251	488212.8	1.282616358088E-22
Residual	9	0.0130229181288742	0.0014469934765291		
Total	10	1791.7313569434			

	Coefficients	Standard Error	t Statistic	P-value	Lower 95.0%	Upper 95.0%
Intercept	0.32064092	0.046251812548143	7.8286317043486	1.38E-05	0.37077790722016	0.6705219318774
x1	0.008079643	1.1543454101178E-05	698.72227434287	0	0.00806934844214445	0.0081058013222

BACK EMF Coefficient: 8.879643 Volts/krpm

C-2 PHASE RESISTANCE MEASUREMENT AND FORMULA DETERMINATION

Phase Resistance Determination for BLM-4035 and BMF-4035

BLM 4035

	DC Resistance (Ambient)	DC Resistance (Operating)	120 Hz Resistance (Ambient)	120 Hz Resistance (Operating)	1k Hz Resistance (Ambient)	1k Hz Resistance (Operating)
Phase A-B	0.35	0.35	0.420	0.454	1.210	1.210
Phase B-C	0.35	0.35	0.440	0.454	1.210	1.210
Phase C-A	0.35	0.35	0.420	0.429	1.210	1.210
Analysis Value		0.35		0.454		1.210

Emperical Formula: $R(f) = K * f^{pow(x)} + Rdc$
 Calculated Coeff.: $K = 0.000776 \quad x = 1.014856$

BMF 4035

	DC Resistance (Ambient)	DC Resistance (Operating)	120 Hz Resistance (Ambient)	120 Hz Resistance (Operating)	1k Hz Resistance (Ambient)	1k Hz Resistance (Operating)
Phase A-B	0.42	0.42	0.472	0.474	1.220	1.240
Phase B-C	0.42	0.42	0.472	0.474	1.220	1.240
Phase C-A	0.42	0.42	0.472	0.474	1.220	1.240
Analysis Value		0.42		0.474		1.240

Emperical Formula: $R(f) = K * f^{pow(x)} + Rdc$
 Calculated Coeff.: $K = 0.0001263 \quad x = 1.26543$

Speed (rpm)	MPID Resistance Input	
	BLM4035	BMF4035
0	0.175	0.210
500	0.182	0.212
1000	0.189	0.215
1500	0.196	0.219
2000	0.203	0.223
2500	0.210	0.227
3000	0.217	0.231
3500	0.224	0.236
4000	0.231	0.241
4500	0.238	0.246
5000	0.245	0.251
5500	0.252	0.256
6000	0.259	0.262
6500	0.266	0.267
7000	0.273	0.273
7500	0.280	0.278
8000	0.287	0.284