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DESIGN, FABRICATION AND CHARACTERIZATION OF N-CHANNEL InGaAsP-InP BASED INVERSION CHANNEL TECHNOLOGY DEVICES (ICT) FOR OPTOELECTRONIC INTEGRATED CIRCUITS (OEIC):

Double Heterojunction Optoelectronic Switches (DOES),
Heterojunction Field-Effect Transistors (HFET),
Bipolar Inversion Channel Field-Effect Transistors (BICFET) and
Bipolar Inversion Channel Phototransistors (BICPT).

By

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A Thesis
Submitted to the School of Graduate Studies
in Partial Fulfillment of the Requirements for the Degree
Doctor of Philosophy

McMaster University
Hamilton, Ontario, Canada

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ABSTRACT

This thesis demonstrates inversion channel technology (ICT) as a viable technique for realizing InGaAsP-InP based monolithic optoelectronic integrated circuits (OEIC). Inversion channel technology utilizes a common substrate and a common fabrication sequence to monolithically integrate electrical, optical and optoelectronic devices, therefore, requiring compatibility in both the device structure and fabrication sequence. This technology is demonstrated by designing, fabricating and characterizing four types of ICT devices, the DOES, HFET, BICFET and BICPT, on a common structure with a common fabrication sequence. These devices were selected because they are complementary in function and provide the circuit designer all the basic elements for building monolithic OEICs: optical emitter, optoelectronic switches, bipolar and unipolar transistors, and photodetectors.

Device models for InGaAsP-InP based DOES, HFET, BICFET and BICPT are developed and used to design the four device structures used in this work. These models identify the effect of device structure on the performance of the devices. The device models are also used to predict the input, output and transfer characteristics of each type of device. This provides an understanding of device physics and operation, and a basis for comparison with experimental results.

A common fabrication sequence and fabrication recipes for self-aligned n-channel InGaAsP-InP based DOES, HFET, BICFET and BICPT is designed, developed and demonstrated. This includes the photomask set for self-

aligned ICT devices, SiO_2 masking for self-aligned contact formation, SiO_2 sidewall passivation of mesas for ion-implantation, high accuracy RIE etching with a an in-situ QMS, implant activation for n- and p-implants in InGaAsP-InP, and metallization over tall vertical mesa structures.

The operation of the DOES, HFET, BICFET and BICPT is demonstrated experimentally. Complete sets of electrical, optical and optoelectronic measurements of the input, output and transfer characteristics of each type of device is performed. These characteristics are compared with the theoretical predictions made by the models to validate the operation of each type of device.

This work demonstrates ICT as a technology for realizing OEICs in the InGaAsP-InP material system, and presents the technology required to design, fabricate and characterize these integrated devices.

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"If I have seen farther it is by standing on the shoulders of giants.."
—Sir Isaac Newton

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CHAPTER 1

INTRODUCTION

1.1 TECHNOLOGICAL TRENDS AND DRIVING FORCES

The transition of our society from the industrial age to the information age began to take shape in the 1980's. This new age was brought about by the merger of telecommunication, microelectronic and microcomputer technologies to form information systems. Information systems are networks that provide a forum for electronic exchange of information. These networks rely on telecommunications for electronic transport of information, and microcomputers to source and process the information. The shift towards electronic distribution of information allows it to be gathered quickly and processed to the requirements of the user. This convenience and flexibility has fueled the demand for information systems.

Early information systems were used by the banking industry in the form of national networks to connect the head office with its branches. This allowed very quick, efficient and reliable exchange of information between geographically separated offices. The automated teller machines (ATM) allowed banking customers to experience the information age by allowing deposits, cash withdrawals, bill payments and account updates at numerous convenient

locations twenty-four hours of the day. Automated debit machines (ADM) are a further advancement of electronic banking. These machines, available at many retail stores, allow electronic exchange of money between the consumer, retailer and financial institution to take place within seconds.

Electronic access to national and international sources of information is available through the internet on the world-wide-web (WWW). Access to the web is easily accomplished by using a WWW browser on a personal computer. These sources of information are diverse in content and cover a wide range of topics including economics, politics, social issues, careers, health, weather and entertainment. This information is presented in multi-media format incorporating interactive data, audio and video. Public acceptance of information systems has also fueled the introduction of new video-based communication services including videophones, interactive video, switched video-on-demand and enhanced pay-per-view.

The information age offers widespread availability of multi-media sources made possible by information systems. This has been and will be instrumental in changing the structure of our society and economies. Information systems will form the backbone of society and also serve as the driving force for change in this era just as manufacturing did for the industrial age [1].

The vision for the information systems of the future is that of humans and machines exchanging information in a simple, reliable, secure and cost-effective manner at any time, in any place, using a combination of voice, video and data. This vision necessitates the evolution towards high speed microelectronics, powerful multi-media based microcomputer systems and high-bandwidth telecommunication systems.

1.2 TELECOMMUNICATION SYSTEMS

The information age has forced telecommunication systems to evolve from systems designed and optimized for voice to systems for multi-media: data, voice and video. Table 1.1 shows that there is, at least, a 100 times increase in bandwidth for active connections for real-time full-motion video compared with digitized voice. It is estimated that a metropolitan area with a population of 10 million requires an aggregate capacity of 1.5 Tb/s to support multimedia telecommunication [2].

Table 1.1 and 1.2 show that the large bandwidths required for multi-media transmission have limited twisted wire-pair and co-axial transmission systems to short-haul applications. These include intra-building networks or home-to-local switch networks. The enormous transmission capacity required between switches for trunking and distribution can only be satisfied by optical transmission. Optical transmission systems have a potential bandwidth of 10,000 GHz* which can transported without repeaters over large distances with the use of Er^{3+}-doped fibre amplifiers [4,5]. It is this apparently limitless transmission capacity that allows optical transmission systems to meet the present and future transmission requirements of the information age.

Although it is clear that optical transmission will become more important in telecommunications systems, how such systems are to be implemented and what form they will take is still a hotly debated issue. Much research in hardware and software is required to develop the systems of tomorrow and to exploit the large bandwidth potential of optical transmission.

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* Optical bandwidth for a 100 nm transmission window centered at $\lambda = 1.55$ µm.

Table 1.1: *Transmission bandwidth requirements for various forms of media [2].*

Media	Transmission Bandwidth Required
Voice	16–64 kb/s
Video (VCR Quality)	1.5 Mb/s
Video (NTSC Quality)	3–4 Mb/s
High Definition TV	20–40 Mb/s

Table 1.2: *Transmission capacity of various communication systems [3].*

Transmission System	Transmission Capacity
Twisted Wire Pair	3 Mb/s·km
Co-axial	270 Mb/s·km
Fibre Optic (1st Generation)	1–3 Gb/s·km
Fibre Optic (2nd Generation)	3–100 Gb/s·km
Fibre Optic (3rd Generation)	100–1,000 Gb/s·km
Fibre Optic (Current)	10,000 Gb/s·km

1.3 OPTICAL COMMUNICATION SYSTEMS

Optical communications was made feasible by the advent of the semiconductor laser and the optical fibre [6,7]*. The first commercial optical communication system introduced in the mid 1970's used AlGaAs-GaAs

* First reports of lasing in semiconductor diode lasers is credited to Hall et al. in 1962 [6] while the first proposal for use of optical fibres for transport of light was made in by Kao and Hockham in 1966 [7].

semiconductor diode lasers as λ = 0.85 μm optical sources, large core diameter multimode silica optical fibres and Si p-i-n photodetectors. This system had a transmission capacity of 0.1 Gb/s·km. Transmission capacities have increased exponentially with current systems capable of achieving 10,000 Gb/s·km [8].

Increases in the system capacity over the past decade has been achieved by improvement of laser diode and optical fibre technology. Specifically, these efforts have been focused on minimizing attenuation and dispersion, and increasing modulation speed. The four generations of evolution can be readily identified in Fig. 1.1. In the late 1970's there was a shift from large-core multimode fibre to much narrower-core single-mode fibre to eliminate modal dispersion. Also in this time frame, an increase in the transmission wavelength from 0.85 μm to 1.3 μm was made to exploit the dispersion minima of the silica

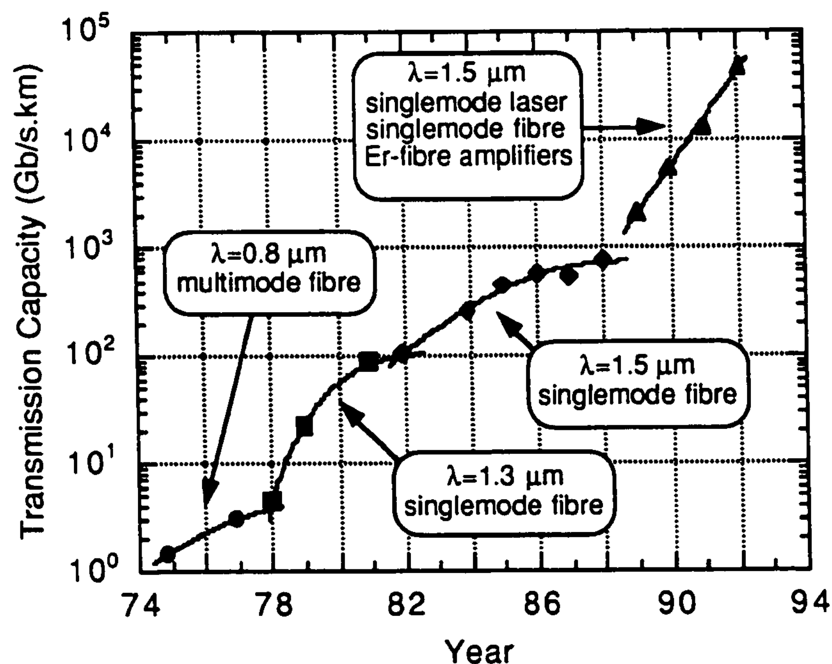

Figure 1.1: Progress of optical transmission system capacity [3].

fibre. In the early 1980's, there was another shift in the transmission wavelength to 1.55 μm to exploit the attenuation minima of the optical fibre. This evolution in transmission wavelengths has required a switch from AlGaAs-GaAs to InGaAs-InGaAsP-InP based semiconductor lasers. It has also required a change from Si-based photodetectors to Ge or InGaAs based devices.

Further increases in transmission capacity have been provided by the development of single frequency distributed feedback (DFB) and distributed Bragg reflector (DBR) lasers to further reduce dispersion, and Er^{3+}-doped fibre amplifiers to significantly increase the distance between repeaters.

1.4 MONOLITHIC OPTOELECTRONIC INTEGRATED CIRCUITS (OEIC)

Monolithic optoelectronic integration is a technology where both electrical devices (laser drivers and photodetector amplifiers) and optical device (lasers and photodetectors) are grown and fabricated on a common substrate. This technology allows devices to be placed physically close to each other and interconnections between devices to be made during the fabrication sequence. The optoelectronic integrated circuit (OEIC) architecture minimizes the parasitic impedances associated with the circuit, allowing for increased operating bandwidth and signal-to-noise ratio. Monolithic fabrication of OEIC's also offers a cost advantage and improved system reliability which results from reduced component counts, and simplification in assembly and testing [9].

Furthermore, OEIC technology can also be adapted for photon transport between devices and circuit elements. This ability to achieve optical interconnectivity between devices and circuits on a wafer scale can overcome the

interconnection bottleneck associated with electron transport and allow for a dramatic increase in the operational bandwidth of systems.

The ability to monolithically integrate electronics and optoelectronic components increases the functionality of OEIC's to applications beyond that of transmitters or receivers. With the integration of signal processing and decision making functions, it is possible to design complex application specific OEIC (ASOEIC) for use in residual gas sensing, structural-stress sensing and optical interconnections. These applications typically require a self-contained ASOEIC which is able to generate and detect light as well as perform signal processing.

The advantages offered by OEIC's are fundamentally important to achieving low cost, high functionality, high reliability, large bandwidth information systems. Although monolithic integration is relatively new to optoelectronics, it has been proven in Si-based microelectronics with microprocessors and application specific integrated circuits (ASIC), and in GaAs-based monolithic microwave integrated circuits (MMIC).

The Intelligent Sensing for Innovative Structures project (ISIS) sponsored by the Canadian Federal government is an example of an application that benefits from the use of OEIC's [10]. In this project an ASOEIC is required as part of a system to monitor the structural stresses of buildings. Structural stresses are measured by determining the wavelength shift which results from a deformation of an optical fibre that is embedded in the structure. The task requires an OEIC to generate the coherent light that is passed through the optical fibre and detecting the wavelength shift of the light after it travels through the fibre. This requires the integration of a laser diode and a laser driver, photodetector and amplifier as well as signal processing electronics.

1.5 OEIC TECHNOLOGY

Over the past two decades research into optoelectronic integration has been intense and many schemes for achieving monolithic integration have been demonstrated. These efforts at monolithic integration can be divided into three approaches: vertical integration (VI), horizontal integration (HI) and common structure (CS) [11].

In vertical integration, electronic and optoelectronic device structures are grown sequentially on top of each other. Isolation between different devices is achieved with the inclusion of an electrically insulating layer between devices. Contact is then made to the appropriate device layers to form the integrated circuit. This approach is difficult to implement, as it is difficult to grow sufficiently insulating layers to minimize coupling between devices. In addition, the non-planar nature of electrical interconnects between electronic and optoelectronic components causes severe difficulty in fabrication and limits the ultimate complexity that can be achieved.

Horizontal integration, on the other hand, utilizes multiple growth and selective area removal of epitaxy to localize individual device structures on a common substrate. This technique is able to overcome the isolation and planarity difficulties associated with vertical integration; however, it requires a complex set of growth-etch-regrowth sequences in order to achieve integration.

Although the advantages offered by OEIC's are staggering, the difficulties associated with materials and fabrication of very different device structures, photonic and electronic, on a single chip must be overcome for it to become a truly viable technology.

1.6 INVERSION CHANNEL TECHNOLOGY FOR OEIC'S

Inversion channel technology (ICT) was introduced by Taylor and Simmons in 1980 as an approach to achieving planar monolithic OEIC's with a single epitaxial growth and a common device fabrication sequence. This technology, in the n-channel manifestation, consists of a p-type wide-bandgap (WBG) emitter, a highly doped n-type WBG charge sheet, a p-type narrow-bandgap (NBG) active layer followed by an n-type WBG collector. The charge sheet is designed to be fully depleted under all bias conditions, and acts as a source of fixed charge which induces an electron inversion channel at the p-p heterointerface. All ICT devices have in common this inversion-channel based device structure.

Intense research effort to demonstrate and develop ICT based on the AlGaAs-GaAs material system has been carried out. This has culminated in the demonstration of an entire family of electronic and optoelectronic devices which include the double-heterostructure optoelectronic switch (DOES) [12–14], the heterojunction field effect transistor (HFET) [15–17], the bipolar inversion-channel field-effect transistor (BICFET) [18–20], the bistable field-effect transistor (BISFET) [19], two- and three-terminal switching lasers (SL) [22–24], field-effect detectors (HFED) [25] and optical modulators [26]. Small and large scale integrated circuits have also been demonstrated with ICT devices. These include transmitter, receiver and repeater circuits [27–31], re-configurable optical interconnections [32–34], logic gates and switches [35], and dynamic memory elements [36,37]. Although most of the work has been in the GaAs-based materials, several ICT devices have also been demonstrated in other material

systems. These include the DOES, HFET and BICFET in the SiGe-Si [38–40] and the two-terminal DOES in the InP based material system [41,42].

Inversion channel technology based on GaAs has been demonstrated as a potentially viable technology for application in $\lambda = 0.85\ \mu m$ systems. The advantages of monolithic optoelectronic integration with ICT make it a promising candidate for implementation in InGaAs-InGaAsP-InP based materials for application in $\lambda = 1.3\ \mu m$ and $\lambda = 1.55\ \mu m$ based optoelectronic systems.

1.7 MOTIVATION AND SCOPE

This project was undertaken to demonstrate inversion channel technology for monolithic optoelectronic integration in the InGaAsP-InP material system. This work, being the first attempt, to achieve ICT in the InGaAsP-InP based material system is focused primarily on the development of technology for designing, fabricating and characterizing ICT devices. Four types of ICT devices, the DOES, HFET, BICFET and BICPT, were selected for integration as they are complementary in function and provide the circuit designer with all the basic elements for designing monolithic optoelectronic circuits: optical emitter, optoelectronic switches, bipolar and unipolar transistors and photodetectors.

Inversion channel technology is based on the common substrate (CS) approach to achieving monolithic optoelectronic integration. In this approach, all devices are fabricated from a common device structure with a common fabrication process. Such a technology requires the device structure and device fabrication process to be compatible with all the types of devices to be integrated.

This added constraint of requiring compatibility in device structure and fabrication is a considerable challenge that is overcome in this project.

The electrical and optical characteristics of the DOES, HFET, BICFET and BICPT are highly dependent on the composition and doping of the 5 primary layers that make up the device structure: emitter, charge sheet, undoped, active and collector layer. Fully optimizing for the performance of a particular device type will result in a severe degradation in the performance of other device types. A suitable device structure will trade-off the performance of each device type to ensure functionality of all devices. In this early stage of technology development, the device structure was designed solely to demonstrate operation of each type of device.

To design a suitable device structure requires a thorough understanding of device operation of each device type and also the influence of device structural parameters on the performance of each device. Device models for InGaAsP-InP based DOES, HFET, BICFET and BICPT are developed in Chapters 2–4. These device models identify the influence of device structural parameters on device performance and were used extensively in the design of the four device structures: S1601, S1602, S1603 and S1604. In addition, these device models also provide an understanding of device physics and operation by providing a view of the internal potentials, charge distribution and current flows. This allows for a comparison of experimental measurements with modeling results to verify the operation of the fabricated devices, critically analyze device performance and suggest improvements to the device structure or device fabrication process.

The device fabrication process and process recipes, discussed in Chap. 5, were designed to be compatible for all device types, to achieve self-alignment

between gate/emitter and inversion channel contacts, and to provide for maximum flexibility in electrical and optical characterization. In total, six styles of devices were fabricated with each device having up to four electrical contacts and an optical window. The entire fabrication process requires a total of 11 photolithography steps, 2 ion implantations, 4 metal depositions, 4 wet etch processes, 5 reactive ion etching steps and 2 thermal anneals.

This project represents the most complex set of devices that have been fabricated at the CEMD facilities. Since the CEMD facilities were in an early state of development when this project was undertaken, much effort was spent installing clean-room facilities and fabrication equipment, and developing fabrication recipes for InGaAsP-InP based materials processing. Fabrication technology designed specifically for fabricating InGaAsP-InP ICTs include:

1) Photomask set for self-aligned ICT devices

2) SiO_2 masking for self-aligned contact formation

3) SiO_2 sidewall passivation of mesas for ion-implantation

4) High accuracy (to within ± 100 Å) RIE mesa etching with in-situ QMS

5) Implant activation for n- and p-implants in InGaAsP-InP

6) Metallization over tall vertical mesa structures

More generic and conventional fabrication processing recipes and techniques that also had to be developed include: photolithography for etching, lift-off and ion-implantation, wet etching, CVD oxide deposition and p- and n-type metallizations for InGaAsP-InP based materials.

The ICT devices designed and fabricated provided for up to 4 contact pads for electrical probing and one window for optical probing allowing for detailed experimental characterization of each device. This is important in demonstrating

the functionality of these devices, and understanding their physics and operation.

Detailed experimental characterization of the input, output, transfer characteristics of the DOES, HFET, BICFET and BICPT was performed. Also examined were the internal junction voltages of the devices as a function of the driving bias. Chapters 6–8 also present these operational characteristics for the DOES, HFET, BICFET and BICPT. Comparisons between experimental and modeling results demonstrated that all types of devices were functional. In addition the full electrical and optical characterization of each device provided insight into device physics and operation, and into areas for future optimization of device performance.

The first part of Chap. 9 summarizes this project which involves the development of technology for design, fabrication and characterization of InGaAsP-InP based ICT devices. Through the course of this project many concerns and questions, beyond the scope of this project, were raised. These questions and concerns involve device modeling, structure, fabrication and characterization. The remainder of Chap. 9 attempts to identify the main concerns and proposes possible directions for future work.

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CHAPTER 2

DESCRIPTION AND THEORY OF THE DOES

The double heterostructure optoelectronic switch (DOES) is a device from the ICT family which possesses bistable electrical and optical states. In the ON state, the device has low resistance and emits light. In the OFF state, the device has high resistance and does not emit light. This device can be switched between the ON and OFF states either electrically, optically or with a combination of both electrical and optical inputs. Such operating characteristics make it a potential candidate for application in electrical, optical or optoelectronic switching operations. The DOES device structure is fully compatible with other devices from the ICT family allowing it to be monolithically integrated with devices including the BICFET, HFET and BICPT.

This chapter is an introduction to the 4-terminal n-channel InGaAsP-InP based DOES device. It begins with a presentation of the DOES device structure followed by the development of a model to describe device operation. This semi-analytical model is derived on the basis of charge conservation and current continuity [1]. The model provides a view of the internal potentials, charge distribution and current flows under a variety of biasing conditions including

current injection into the inversion channel and active layers, and optical injection. This allows for a detailed understanding of device physics and operation, a comparison of experimental measurements with modeling results, verifying the operation of the fabricated devices, critical analysis of device performance, and insights into improving the device structure and fabrication process.

This model is also used to identify the influence of emitter, charge sheet, active layer and collector layer doping concentration on the switching voltage of the device. Such relationships were used extensively in the design of the device structures to ensure compatibility with the HFET, BICFET and BICPT.

2.1 DEVICE STRUCTURE

Figure 2.1 provides a cross-sectional view of a 4-terminal n-channel InGaAsP-InP based DOES. The device consists of a p-InP emitter, a thin, highly doped n-InP charge-sheet layer, an undoped-InGaAsP (λ=1.3 μm) layer, a p-InGaAsP (λ=1.3 μm) active layer and an n-InP collector layer. This entire structure is grown on a highly doped n-type InP substrate. Contacts to the structure are made to the emitter, inversion channel, active layer and collector. A window present in the emitter contact metal allows for optical injection and for detection of optical emissions. The thickness and doping concentration of the charge sheet layer is designed to be almost fully depleted under all operating conditions, while the thickness and doping concentration of p-type active layer is designed such that it is never fully depleted under all operating conditions. The structure of the DOES is designed to create an electron inversion channel at the

p-p heterointerface. This electron inversion channel is critical to the operation of the DOES device.

The equilibrium energy-band representation of the structure, shown in Fig. 2.2, illustrates the energy levels and energy gaps within the structure. In this figure, E_{ge}, E_{ga} and E_{gc} are the energy gaps of the emitter, active and collector layers; E_a is the dopant activation energy of the charge sheet layer; ΔE_{fe}, ΔE_{fa} and ΔE_{fc} are the Fermi energy levels in the emitter, active and collector layers; ΔE_{fi} is the quasi-Fermi level in the inversion channel and ΔE_c; and ΔE_v are the conduction and valence band offsets between the InP and InGaAsP (λ=1.3 μm) layers. This figure highlights the role of the charge-sheet layer in bending the bands at the p-p heterointerface to form the triangular potential well at this heterointerface. This triangular potential well provides an energetically favourable site for the accumulation of electrons.

2.2 DEVICE MODEL

2.2.1 Internal Potentials and Voltages

Figure 2.3 illustrates the DOES under bias and identifies the emitter-inversion channel (e-i), the active layer-inversion channel (a-i) and the active layer-collector (a-c) junctions (see Fig. 2.2 for energy levels and energy gaps). ϕ_e, ϕ_u, ϕ_{a1}, ϕ_{a2} and ϕ_c are the potentials of the emitter, undoped, active (closest to the undoped layer), active (closest to the collector layer) and collector layers. These potentials describe the extent of band bending at each of the p-n junctions within the structure. The undoped layer is assumed to be free of fixed charges

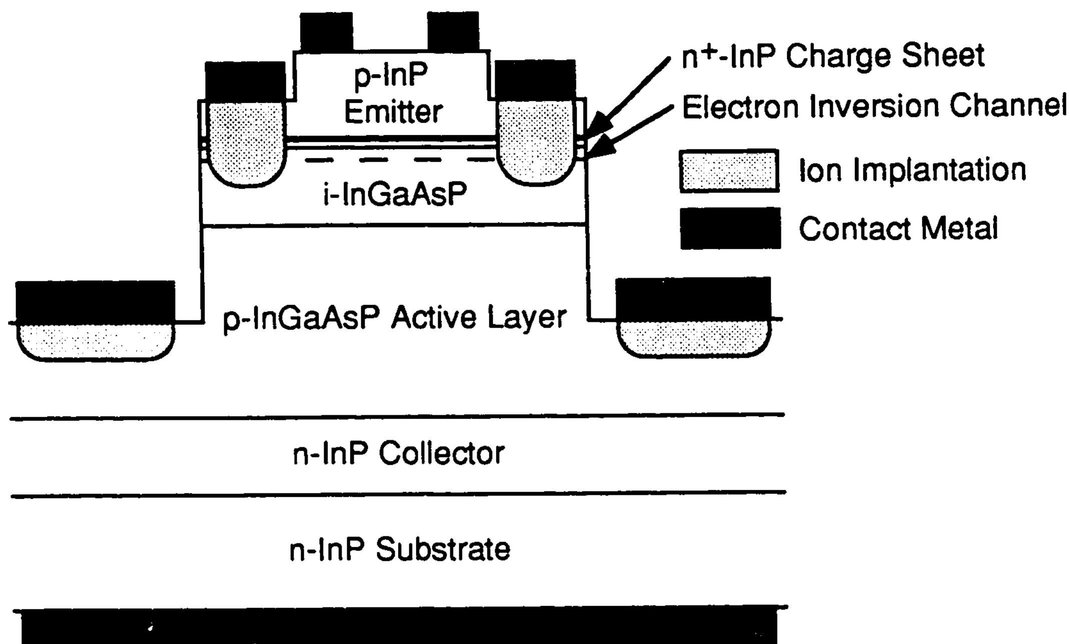


Figure 2.1: Schematic cross-section of a 4-terminal n-channel InGaAsP-InP double heterostructure optoelectronic switch (DOES).

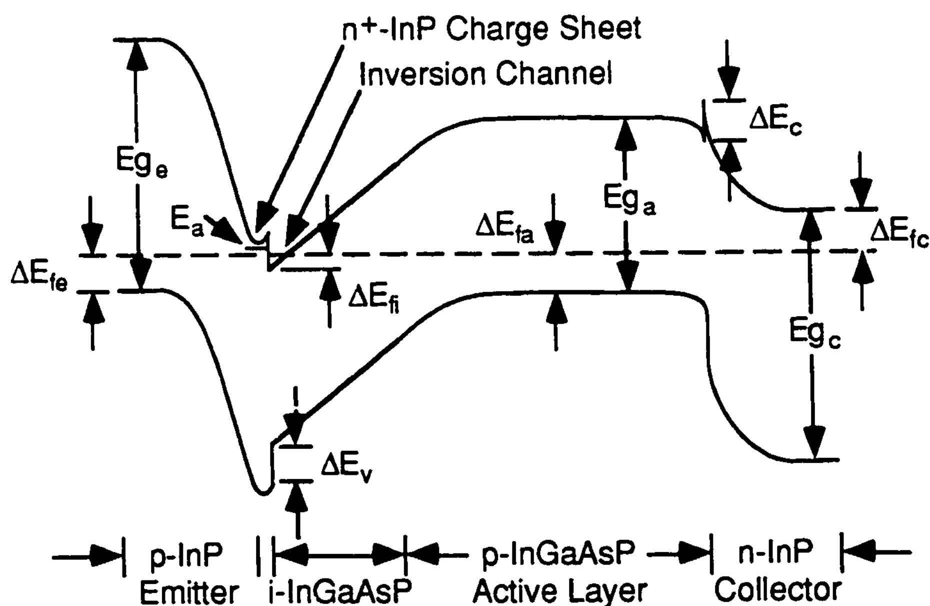


Figure 2.2: Equilibrium energy-band representation of the n-channel InGaAsP-InP DOES including the energy levels and energy gaps (see Figs. 2.3 and 2.5 also).

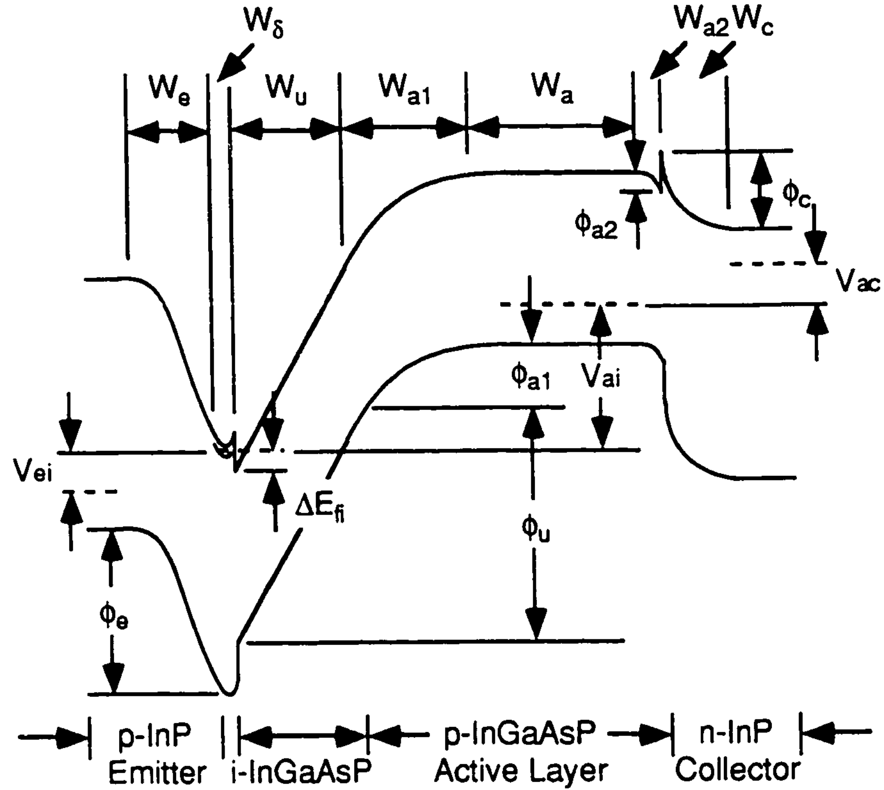


Figure 2.3: OFF-state energy band representation of the DOES device including the internal potentials, junction voltages and depletion layer thicknesses (see Figs. 2.2 and 2.5 also).

and therefore, ϕ_u is directly related to the field at the undoped-active interface (ξ_{ua}) and magnitude of the active layer depletion charge (Q_{a1})

$$\begin{aligned}\phi_u &= \xi_{ua} W_u \\ &= \frac{Q_{a1}}{\varepsilon_a} W_u\end{aligned} \tag{2.1}$$

W_e, W_{a1}, W_{a2} and W_c are the depletion layer widths associated with the emitter, active (closest to the undoped layer), active (closest to the collector layer) and collector layers; W_δ is the width of the charge sheet layer; W_u is the width of the undoped layer; and W_a is the width of the undepleted active layer.

Finally V_{ei}, V_{ai} and V_{ac} are the junction voltages of the e-i, a-i and a-c junctions. Relationships between the junction voltages and the internal potentials are as follows:

$$V_{ei} = -\phi_e + \Delta E_{fi} - \Delta E_{fe} - \Delta E_c + E_{ge} \tag{2.2}$$

$$V_{ai} = -\phi_u - \phi_{a1} + \Delta E_{fi} - \Delta E_{fa} + E_{ga} \tag{2.3}$$

$$V_{ac} = -\phi_{a2} - \phi_c - \Delta E_{fa} - \Delta E_{fc} - \Delta E_v + E_{gc} \tag{2.4}$$

By definition, the junction voltages are positive when the junction is forward-biased, negative when reverse-biased and zero under thermal equilibrium.

2.2.2 Charge Conservation and Fixed Charge Components

Charge Conservation

The DOES device structure is designed so that the active layer is never fully depleted under typical operating conditions. Since a portion of the active layer remains charge neutral, for charge analysis, the structure can be divided into two sections: the p-n-p section defined by the emitter-charge-sheet-inversion channel-active layers, and the p-n section defined by the active layer-collector layers.

In the p-n-p section, the source for positive fixed charge arises from the ionized dopant atoms in the charge sheet layer. The source for negative charge contribution arises from the ionized dopant atoms in the depletion regions of the emitter and active layers, and the accumulation of electrons in the inversion channel. Within this section of the device, charge conservation requires that

$$Q_e - Q_\delta + Q_{ni} + Q_{a1} = 0 \tag{2.5}$$

where Q_e, Q_δ, Q_{ni} and Q_{a1} are magnitudes of the areal charge density of the emitter, charge-sheet, inversion channel and active layers. The undoped layer is assumed to have no fixed charges and therefore, is not included in Eq. (2.5).

In the p-n section, the fixed charge components consist solely of the ionized dopant atoms in the depletion layers of the active and collector layers. Here, charge conservation requires that

$$Q_{a2} - Q_c = 0 \tag{2.6}$$

where Q_{a2} and Q_c are magnitudes of the areal charge density of the active layer and collector layers. In Eqs. (2.5) and (2.6), Q_e, Q_δ, Q_{ni}, Q_{a1}, Q_{a2} and Q_c bear units of charge per unit area (C/cm^2).

Depletion Layer Charges

Expressions for the magnitudes of areal charge density in the emitter, active and collector depletion layer are derived by solving Poisson's equation with the depletion-layer approximation to yield [2]:

$$Q_e = (2q\varepsilon_e N_e \phi_e)^{1/2} \tag{2.7}$$

$$Q_{a1} = (2q\varepsilon_a N_a \phi_{a1})^{1/2} \tag{2.8}$$

$$Q_{a2} = (2q\varepsilon_a N_a \phi_{a2})^{1/2} \tag{2.9}$$

$$Q_c = (2q\varepsilon_c N_c \phi_c)^{1/2} \tag{2.10}$$

where q is the electronic charge; N_e, N_a and N_c are the doping concentration of the emitter, active and collector layers respectively; and ε_e, ε_a and ε_c are the dielectric constants for the emitter, active and collector layers respectively. This approach for describing ionized fixed charge density at a junction is consistent with conventional p-n junction theory [2].

Charge Sheet Layer Charge

The only source of positive fixed charge in the p-n-p section arises from the ionized dopant atoms in the charge sheet layer. The extent of dopant activation within the charge sheet is determined by the relative positions of E_a and ΔE_{fi}. If the difference between E_a and ΔE_{fi} is assumed to be greater than $3V_T$ under all conditions, the Boltzmann approximation can be used to estimate the density of activated donors:

$$Q_\delta = \frac{N_\delta W_\delta}{1+\exp\left[-\left(\Delta E_c - E_a - \Delta E_{fi}\right)/V_T\right]} \tag{2.11}$$

where $V_T = kT/q$ is the thermal voltage, k is Boltzmann's constant and T is the temperature. A detailed derivation for the total ionized dopant concentration is presented by Pierret [3].

Inversion Channel Charge

The triangular potential well formed at the heterointerface between the charge-sheet and the active layer provides an energetically favourable location for electrons within the device structure to accumulate. Figure 2.4 provides a magnified view of this triangular potential well. The energy levels in the well are quantized and can be determined by solving the one-dimensional, time independent Schrödinger's equation, with the well potential $V(x)$. Since $V(x)$ is determined by the occupancy of states in the well, charge neutrality and current conservation across the structure, a closed-form analytical expression for the energy levels, which accounts for the curvature of the potential well, is unachievable. Analytical solutions for the energy levels in the well can be obtain by using a triangular potential well approximation where the electric field (ξ) is

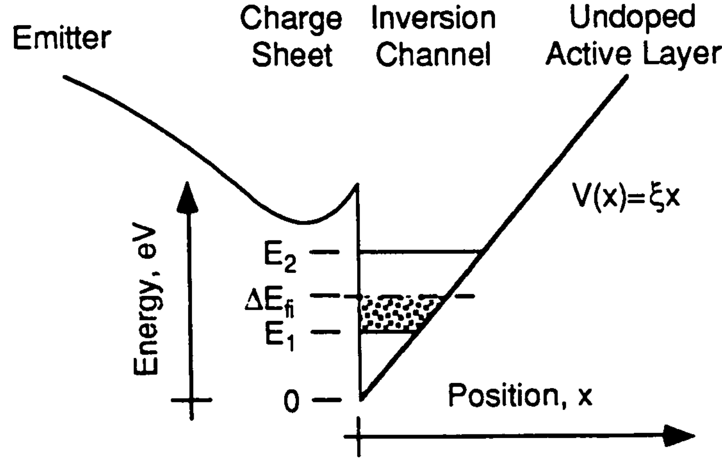


Figure 2.4: Magnified view of the triangular potential well formed at the p-p heterointerface of the DOES. The triangular potential approximation is applied to yield analytical solutions for the first and second energy levels (E_1 and E_2).

assumed to be constant across the well. ξ is defined as the field at the p-p heterointerface and is described as

$$\xi = \frac{Q_\delta - Q_e}{\varepsilon_e} \tag{2.12}$$

The potential of the well is therefore, directly proportional to position (x) as illustrated in Fig. 2.4. Approximate solutions for the first and second energy levels within the well, E_1 and E_2, are [4]

$$E_l \approx \beta_l \xi^{2/3} \tag{2.13}$$

where

$$\beta_l = \left(\frac{1}{2qm_n}\right)^{1/3} \left(150\pi\hbar(l - 1/4)\right)^{2/3} \tag{2.14}$$

$l = 1,2$; m_n is the effective mass of the electrons in the inversion channel; and $\hbar$ is Planck's constant. By further assuming that the majority of electrons occupy states between the first and second energy levels, the areal density of electrons in

the well is established by integrating to determine the number of occupied states between these energy levels. This yields

$$
\begin{aligned}
Q_{ni} &= \int_{E=0}^{\infty} g(E)f(E)dE \\
&= \int_{E_1}^{E_2} g(E)f(E)dE \\
&\approx \frac{qm_n}{\pi\hbar^2}\left\{(E_2 - E_1) + V_T \ln\left(\frac{1+\exp\left[\left(E_1 - \Delta E_{fi}\right)/V_T\right]}{1+\exp\left[\left(E_2 - \Delta E_{fi}\right)/V_T\right]}\right)\right\}
\end{aligned}
\tag{2.15}
$$

where $g(E)$ is the density of states function for a 2-D quantum well and $f(E)$ is the Fermi-Dirac function. This treatment for calculating the density of carriers in a triangular quantum well is consistent with those used in MOSFET or HEMT device modeling [5].

2.2.3 Current Continuity and Current Density Components

Current Continuity

The current density components considered in this model can be divided into five categories: diffusion, thermionic, recombination, generation and external sources (see Fig. 2.5). These current density components which describe the flow of carriers across the structure must satisfy the conditions for current continuity. In this model, current continuity across the structure is defined at points A and B shown in Fig. 2.5. Continuity of electron current density at point A requires that

$$J_{ne} - J_{ni} + J_{tei} + J_{tai} - J_{oei} - J_{oai} + J_i = 0 \tag{2.16}$$

while continuity of hole current density at point B requires that

$$J_{pe} - J_{pa} - J_{tai} - J_{ta} - J_{tac} + J_{oai} + J_a = 0 \tag{2.17}$$

where J_{ne}, J_{ni} and J_{na} are the electron current densities flowing (by diffusion) across the e-i, a-i and a-c junctions; J_{pe} is the net hole current density flowing (by thermionic emission) from the emitter across the emitter potential barrier; J_{pa} is the hole current density flowing (by diffusion) across the a-c junction; J_{tei}, J_{tai} and J_{tac} are the net thermal recombination current densities associated with the e-i, a-i and a-c junctions; J_{ta} is the recombination current density in the neutral portion of the active layer; J_{oei} and J_{oai} are optically generated current densities; and J_e, J_i, J_a and J_c are the current densities at the emitter, inversion-channel, active-layer and collector contacts. All of the current density components in Eqs. (2.16) and (2.17) have units of A/cm^2. The direction for positive current flow for each of these current density components is defined in Fig. 2.5.

Diffusion Currents

Expressions for J_{ne}, J_{ni}, J_{na} and J_{pa} are derived based on the principles of diffusion current flow described in Sze [1]. For the current density components J_{ne} and J_{pa}, it is assumed that all the minority electrons in the bulk of the emitter recombine before arriving at the emitter contact and that all minority holes in the bulk of the collector recombine before arriving at the collector contact. Solving the diffusion current equations under these approximations yields

$$J_{ne} = q\frac{D_{ne}}{L_{ne}} n_{poe}\left\{\exp(V_{ei}/V_T) - 1\right\} \tag{2.18}$$

$$J_{pa} = q\frac{D_{pc}}{L_{pc}} p_{noc}\left\{\exp(V_{ac}/V_T) - 1\right\} \tag{2.19}$$

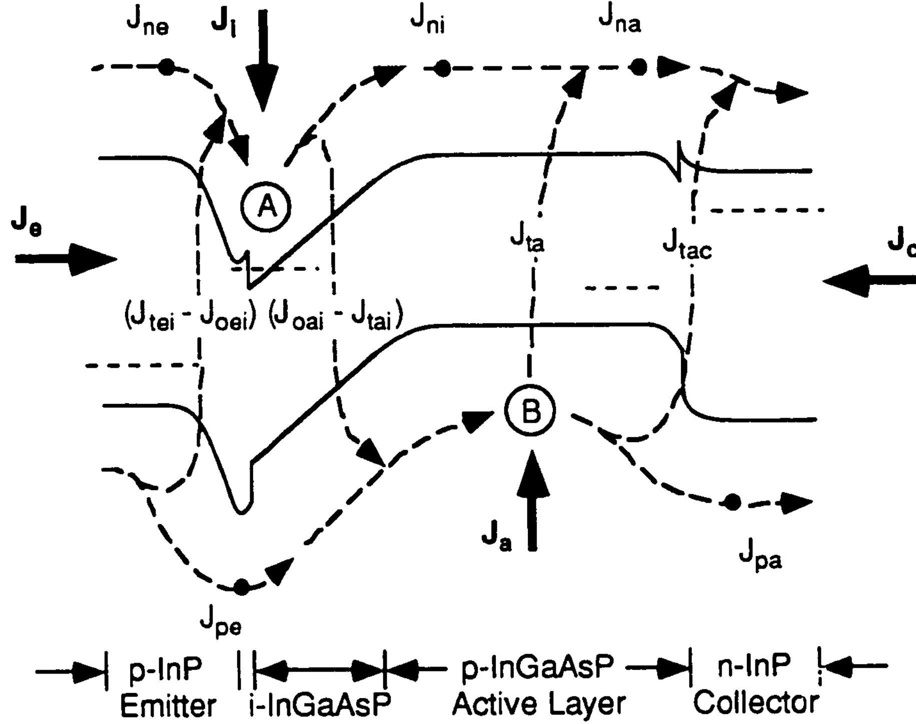


Figure 2.5: ON-state energy band representation of the DOES identifying the internal current density components, terminal current density components and direction of current flow (see Figs. 2.2 and 2.3 also).

where n_{poe} and p_{noc} are the minority carrier concentrations in the bulk of the emitter and collector layers, D_{ne} and L_{ne} are the diffusion coefficient and diffusion length for electrons in the emitter, and D_{pc} and L_{pc} are the diffusion coefficient and diffusion length for holes in the collector.

For current density components J_{ni} and J_{na}, the diffusion equations are solved across the neutral portion of the active layer to yield

$$J_{ni} = q\frac{D_{na}}{L_{na}}n_{poa}(A_1 - A_2) \tag{2.20}$$

$$J_{na} = q\frac{D_{na}}{L_{na}}n_{poa}\left\{A_1\exp(W_a/L_{na}) - A_2\exp(-W_a/L_{na})\right\} \tag{2.21}$$

where

$$A_1 = \frac{\{\exp(V_{ac}/V_T)-1\} - \exp(-W_a/L_{na})\{\exp(V_{ai}/V_T)-1\}}{2\sinh(W_a/L_{na})} \quad (2.22)$$

$$A_2 = \frac{\exp(W_a/L_{na})\{\exp(V_{ai}/V_T)-1\} - \{\exp(V_{ac}/V_T)-1\}}{2\sinh(W_a/L_{na})} \quad (2.23)$$

D_{na} and L_{na} are the diffusion coefficient and diffusion length for electrons in the active layer, n_{poa} is the minority electron concentration in the active layer and W_a is the width of the undepleted portion of the active layer. W_a is not a constant and varies with the applied bias.

This description of the diffusion current density components within the active layer of the DOES is consistent with that used in p-n junction diode and p-n-p bipolar junction transistor theory [2,6]. A more simplified method for solving J_{ne} and J_{pa} is to assume a linear approximation for the electron and hole concentrations across the undepleted portion of the active layer.

Thermionic Currents

The current density component J_{pe} is described by thermionic emission because the holes in the emitter have to overcome the potential barrier ϕ_e to flow into the active layer. Correspondingly, the holes in the active layer must overcome the potential barrier $\phi_{a1} + \phi_u + \Delta E_v$ to flow into the emitter layer. Thus, the expression for the net thermionic hole current density across the emitter barrier is [1]

$$J_{pe} = A_e^*\{\exp(V_{ea}/V_T)-1\} \quad (2.24)$$

where

$$A_e^* = \frac{4\pi m_p q^3 (V_T)^2}{h^3} \quad (2.25)$$

is Richardson's constant and m_p is the effective mass of the hole.

Net-Thermal Recombination Currents

Trapping states which exist within the energy gap of the semiconductor serve as recombination or generation centres for electron-hole pairs. These interactions are described by Shockley-Read-Hall statistics (S-R-H) [6]. Assuming that: 1) only one trapping level is active, 2) the trap is situated at midgap and 3) the recombination cross-sections for electrons and holes are equal, the net recombination rate ($U(x)$) at any position (x) in the semiconductor is

$$\begin{aligned} U(x) &= \frac{1}{\tau_r}\left\{\frac{p(x)n(x)}{p(x)+n(x)+2n_i} - \frac{n_i^2}{p(x)+n(x)+2n_i}\right\} \\ &= U_r(x) - U_g(x) \end{aligned} \tag{2.26}$$

where $p(x)$ and $n(x)$ represent the concentration of electrons and holes, n_i is the intrinsic carrier concentration, and τ_r is the recombination lifetime for electrons and holes. Equation (2.26) is written to clearly differentiate the recombination ($U_r(x)$) and generation ($U_g(x)$) components. $U(x)$ is positive when there is net-recombination and negative when there is net-generation.

Under forward-bias conditions, $p(x) >> n_i$ and $n(x) >> n_i$, the maximum recombination rate is given by

$$U_r(x) = \frac{1}{2\tau_r}(p(x)n(x))^{1/2} \tag{2.27}$$

Under reverse bias conditions, $n_i >> p(x)$ and $n_i >> n(x)$, the thermal generation rate is given by

$$U_g(x) = \frac{n_i}{2\tau_r} \tag{2.28}$$

Thus, the net recombination rate is

$$\begin{aligned} U(x) &= U_r(x) - U_g(x) \\ &= \frac{1}{2\tau_r}\left\{(p(x)n(x))^{1/2} - n_i\right\} \end{aligned} \tag{2.29}$$

Equation (2.29) explicitly shows that recombination or generation occurs when $p(x)n(x) \neq n_i^2$.

The current density resulting from net-recombination of electrons and holes across the depletion region of the e-i junction is:

$$\begin{aligned} J_{tei} &= q \int_{x=0}^{x=W_e} U(x)dx \\ &= q\frac{n_{ie}}{2\tau_{re}} W_e\{\exp(V_{ei}/2V_T) - 1\} \end{aligned} \tag{2.30}$$

Similarly, the net-recombination current density across the a-i junction is

$$J_{tai} = q\frac{n_{ia}}{2\tau_{ra}}(W_u + W_{a1})\{\exp(V_{ai}/2V_T) - 1\} \tag{2.31}$$

and the net-recombination current density across the a-c junction is

$$J_{tac} = q\left(\frac{1}{2\tau_{ra}} + \frac{1}{2\tau_{rc}}\right)\left(\frac{n_{ia} + n_{ic}}{2}\right)(W_{a2} + W_c)\{\exp(V_{ac}/2V_T) - 1\} \tag{2.32}$$

where W_e, W_u, W_{a1}, W_{a2} and W_c are the widths of the depletion regions associated with the emitter, undoped, active and collector layers (see Fig. 2.3); n_{ie}, n_{ia} and n_{ic} are the intrinsic carrier concentrations of the emitter, active and collector layers; and τ_{re}, τ_{ra} and τ_{rc} are the carrier lifetimes of the emitter, active and collector layers.

Carriers which flow across the neutral portion of the active layer also experience recombination. The current density component which accounts for this recombination is

$$J_{ta} = J_{na} - J_{ni} \tag{2.33}$$

Optically Generated Currents

Photons with energy (E_p) passing through a semiconductor with energy gap (E_g) will be absorbed by the semiconductor if $E_p > E_g$. The flux of photons absorbed by a semiconductor of thickness (W) is given by

$$\begin{aligned} \Phi_a &= \Phi(x=0) - \Phi(x=W) \\ &= \Phi_0 - \Phi_0 \exp(-\alpha W) \end{aligned} \tag{2.34}$$

where Φ_0 is the initial photon flux and α is the absorption coefficient.

When photons are absorbed in the InP or InGaAsP layers of the DOES, there is a finite probability that an electron-hole pair will be generated. Electron-hole pairs that are generated in the neutral sections of the device, where there is no electric field to separate them, will recombine with each other. However, electron-hole pairs that are generated in the depletion regions of the device will be separated by the electric field and contribute to current flow in the device.

The current density component J_{oei} is generated when a photon flux (Φ), incident on the device, is absorbed within the depletion regions of the e-i junction. Thus,

$$\begin{aligned} J_{oei} &= q\eta_e\{\Phi(t_e - W_e) - \Phi(t_e + W_\delta)\} \\ &= q\eta_e\Phi\{\exp(-\alpha_e(t_e - W_e)) - \exp(-\alpha_e(t_e + W_\delta))\} \end{aligned} \tag{2.35}$$

Similarly, J_{oai} represent the current density component that is generated when Φ is absorbed within the depletion region of the a-i junction,

$$J_{oai} = q\eta_a\{\Phi(t_e + W_\delta) - \Phi(t_e + W_\delta + W_u + W_{a1})\}$$
$$= q\eta_a\Phi\{\exp(-\alpha_a(t_e + W_\delta)) - \exp(-\alpha_a(t_e + W_\delta + W_u + W_{a1}))\} \quad (2.36)$$

where η_e and η_a are the quantum efficiencies of the emitter and active layers, and α_e and α_a are the optical absorption coefficients for the emitter and active layers, and t_e is the total thickness of the emitter layer.

Terminal Currents

In addition to the internal current components, contacts to the inversion channel layers provide a means for external injection or extraction of current from the structure. The current density which is injected into the inversion channel is defined as J_i while the current density which is injected into the active layer is defined as J_a. The ability to externally inject or extract current allows for external control of the carrier balance within the structure, allowing the switching point of the DOES to be controlled.

Expressions for the current density components J_e and J_c are:

$$J_e = J_{ne} + J_{pe} + J_{tei} - J_{oei} \quad (2.37)$$

$$J_c = -(J_{na} + J_{pa} + J_{tac})$$
$$= -(J_e + J_i + J_a) \quad (2.38)$$

The direction of positive flow is for the current density components J_e, J_i, J_a and J_c is defined in Fig. 2.5. Physically, positive current flow at the contacts is achieved by injecting holes into or extracting electrons from the contact and hence, the device.

2.2.4 Optical Emission

When an electron-hole pair recombines, energy is liberated in the form of phonons and photons. Photons which are emitted through the emitter contact (see Fig. 2.1) allow the DOES device to be used as an optical source. Within the DOES structure, recombination of electrons and holes take place within the depletion regions of the e-i, a-i and a-c junctions when these junctions are forward biased, and in the neutral region of the active layer. An expression for the photon flux (Φ) which is generated by recombination is

$$\Phi = \eta \frac{J_t}{q} \tag{2.39}$$

where η is the internal quantum efficiency and J_t is the net recombination current density. Of the photon flux that is generated at the depletion region, half is directed towards the emitter contact while the other half is directed towards the collector contact. Photons that are directed towards the collector contact are all absorbed by the structure and collector contact metal. The photons that are directed towards the emitter contact must travel through the structure to the edge of the emitter contact window before exiting the device. As a result, a fraction of the generated photon flux will be absorbed by the structure as described in Eq. (2.34). An expression for the photon flux, which is generated at the e-i junction, that exits the device through the emitter contact window (Φ_{ei}) is

$$\Phi_{ei} = \eta_e \frac{J_{tei}}{2q} \exp\left(-\alpha_e(\lambda)(t_e - W_e)\right) \tag{2.40}$$

Similarly, the photon flux, generated at the a-i junction, that exits the device through the emitter contact window (Φ_{ai}) is

$$\Phi_{ai} = \eta_a \frac{J_{tai}}{2q} \exp(-\alpha_e(\lambda)(t_e + W_\delta)) \tag{2.41}$$

where η_e and η_a are the internal quantum efficiencies of the emitter and active layers, $\alpha_e(\lambda)$ is the photon-wavelength dependent absorption coefficient of the emitter layer. Since Φ_{ei} is generated within the e-i junction, it has a photon-energy equal to E_{ge} while Φ_{ai}, which is generated within the a-i junction, has a photon-energy equal to E_{ga}.

2.2.5 Solution to DOES Device Equations

Equations (2.1)–(2.41) form a set of coupled equations which describe the operation of the DOES. These equations are solved numerically with a computerized model written in the Windows 3.1 version of MATLAB [8]. This model requires the user to enter the physical parameters for the device structure as well as the external applied biases J_e, J_i, J_a and Φ. Equations (2.1)–(2.41) are then solved numerically to provide a set of internal potentials ϕ_e, ϕ_u, ϕ_{a1}, ϕ_{a2}, ϕ_c and ΔE_{fi} which satisfy the conditions for charge neutrality and current continuity across the structure. This set of internal potentials is used to determine the charge, current and voltage components of the device at each bias point.

2.3 DEVICE OPERATION

2.3.1 The a-c, e-i and a-i Junctions of the DOES

A qualitative understanding of DOES device operation can be achieved by dividing its complex p-n-p-n structure into three separate p-n junctions: e-i, a-i and a-c junctions. This allows the operation of the DOES to be described by the operation of each p-n junction and the electrical coupling between them.

The current density-voltage (J-V) character of the a-c junction clearly shows two regimes of operation (see Fig. 2.6): recombination and diffusion dominated current transport. Under low-current injection conditions current transport is dominated by recombination (see Eq. (2.32)). A large fraction of the injected electrons which flow from the collector towards the active layer recombine in the a-c depletion layer, thus, very few reach the neutral portion of the active layer. Similarly, a large fraction of the injected holes which flow from the active layer toward the collector recombine in the depletion layer, thus, very few reach the neutral portion of the collector. When recombination dominates, most of the injected carriers recombine in the depletion regions of the p-n junction with only a small fraction of the carriers able to flow across the junction. Under low-current injection conditions, where recombination current transport dominates, the efficiency of minority carrier injection into the neutral portions of the structure is low.

Under high-current injection conditions, current transport becomes dominated by diffusion (see Eqs. (2.19) and (2.21)). A large fraction of the electrons injected into the collector reach the neutral portion of the active layer. Similarly, a large fraction of the holes injected into the active layer reach the neutral portion of the collector. Under high-current injection conditions, where diffusion current transport dominates, the efficiency of minority carrier injection into the neutral portions of the structure is high.

The operation of the a-c junction is representative of the e-i and a-i junctions, and is consistent with p-n junction theory [2]. For DOES device operation, minority carrier injection into the neutral portions of the structure provides the coupling between the three p-n junctions while the balance between

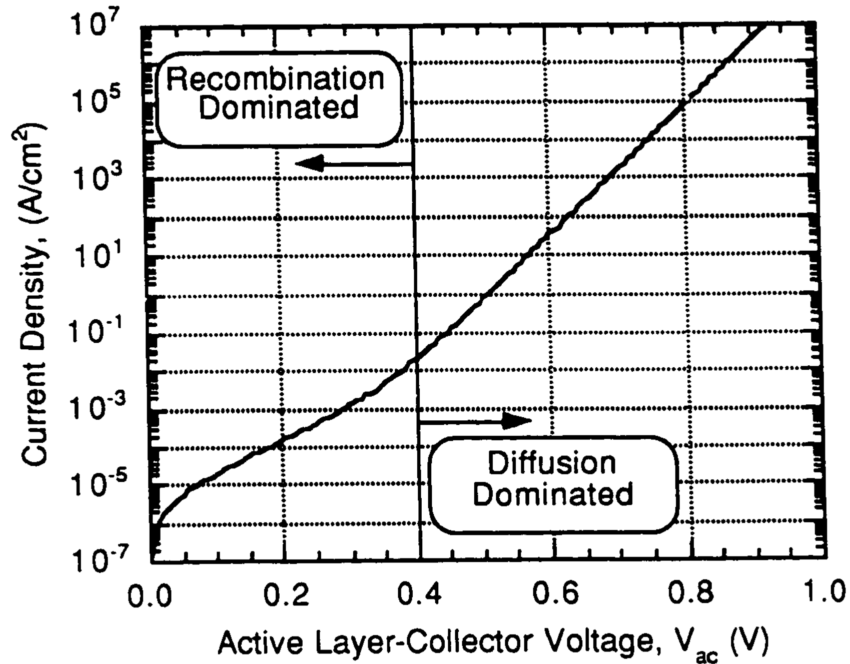


Figure 2.6: Current density-voltage (J-V) characteristics of the active layer-collector (a-c) junction of the DOES.

the recombination and diffusion current components dictates the switching of the device.

2.3.2 J-V Characteristics

Experimentally, the J-V characteristic of the DOES is obtained by grounding the collector and injecting current into the emitter. At each current injection level, the voltage across the emitter and collector terminals is measured to generate the J-V characteristic. This form of current biasing is required for devices that exhibit S-type negative differential resistance (NDR) because V is a function of J and therefore, a unique value of V is available for each value of J; the converse is not true. Figure 2.7 illustrates the J-V characteristics for a DOES device with structural parameters of Table 2.1. These parameters are typical of

***Table 2.1:** Device structure used in modeling of the DOES.*

Layer	Material	Layer Doping (cm^{-3})	Thickness (Å)
Emitter	p-InP	1×10^{17}	2000
Charge Sheet	n-InP	5×10^{18}	100
Undoped-Active Layer	i-InGaAsP	-	-
Active Layer	p-GaAsInP	1×10^{17}	5000
Collector	n-InP	2×10^{17}	3000
Substrate	n-InP	1×10^{19}	

the DOES devices which were fabricated and tested in this project. The J-V characteristics of the DOES can be divided into three operational states: OFF, NDR and ON. These states are divided by the switching point which is defined by the switching voltage (V_{sw}) and switching current density (J_{sw}), and the holding point which is defined by the holding voltage (V_h) and holding current density (J_h). Figure 2.8 shows the voltage across the e-i, a-i and a-c junctions as a function of J_e. This insight into the behaviour of each junction as a function of J_e allows for a better understanding of DOES device operation.

OFF State

The OFF-state is defined by the region of operation where $J_e < J_{sw}$. In this state, the current injection levels are low and the resistance across the device is high. Under low-levels of current injection, where $J_e < 10^{-2}$ A/cm^2, the e-i junction is forward biased and current transport across the e-i junction is

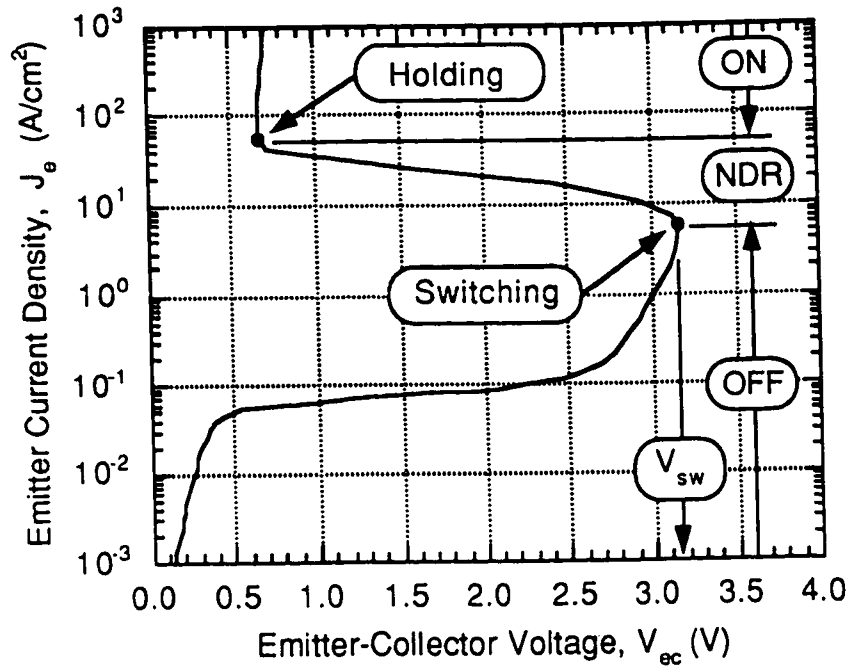


Figure 2.7: Dark, two-terminal J-V characteristic of the DOES.

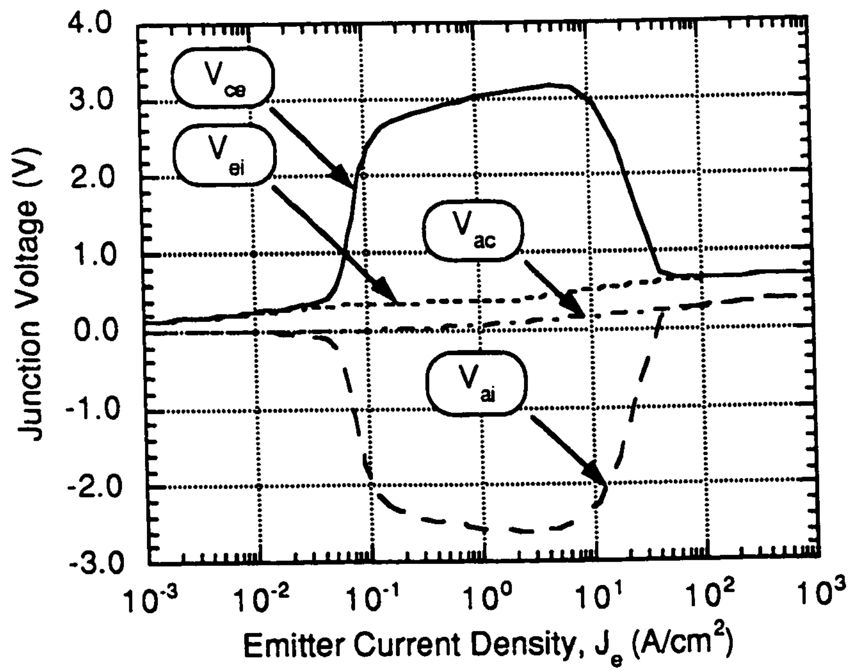


Figure 2.8: Voltage across the e-i, a-i and a-c junctions as a function of emitter current density.

dominated by recombination: $J_{pe} << J_{tei}$ and $J_{ne} << J_{tei}$. Thus, Eq. (2.37) reduces to

$$J_e \approx J_{tei} \tag{2.42}$$

Similarly, the a-c junction is forward biased and current transport across the a-c junction is also dominated by recombination: $J_{na} << J_{tac}$ and $J_{pa} << J_{tac}$. Thus, Eq. (2.38) reduces to

$$J_c \approx -J_{tac} \tag{2.43}$$

Current continuity for electrons at point A (see Fig. 2.5) reduces to

$$J_{tei} + J_{tai} = 0 \tag{2.44}$$

where $J_{ni} << J_{tac}$ is assumed because $J_{na} << J_{tac}$. Current continuity for holes at point B (see Fig. 2.5) becomes

$$J_{tai} + J_{tac} = 0 \tag{2.45}$$

where $J_{ta} << J_{tac}$ is assumed because $J_{na} << J_{tac}$.

To satisfy these conditions for current continuity across the structure, the a-i junction must produce a net-recombination current density of $-J_{tai}$. Physically, this condition requires the a-i junction to generate electron-hole pairs across the a-i depletion region by becoming reverse biased.

From a carrier flow perspective, holes which are injected into the emitter contact recombine with electrons at the forward biased e-i junction. These electrons are generated within the reverse biased a-i junction and drift towards the emitter to recombine at the e-i junction. Electrons which are injected into the collector recombine with holes in the forward biased a-c junction. These holes which participate in recombination are generated within the a-i depletion region.

They drift towards the active layer and diffuse across the neutral active layer and recombine with the injected electrons at the a-c junction. The carriers which are generated by the reverse-biased a-i junction are important in maintaining the current continuity for electrons and holes.

As J_e increases, while still in the recombination dominated regime of current transport, J_{tei} increases resulting in an increase in V_{ei}. J_{tac} also increases resulting in an increase in V_{ac}. To satisfy the conditions for current continuity, as J_{tei} and J_{tac} increase, requires a further decrease in the net-recombination current density. This is accomplished by an increase in the reverse bias voltage across the a-i junction to increase the generation rate of electron-hole pairs. The device voltage increases as a consequence of the increase in the forward bias of the e-i and a-c junctions and the increase in the reverse bias of the a-i junction.

As J_e increases further, current transport across the e-i junction begins to change from one which is dominated by recombination to one where both recombination and diffusion become significant: J_{ne}, J_{pe} and J_{tei}. Thus,

$$J_e = J_{ne} + J_{pe} + J_{tei} \qquad (2.46)$$

Similarly, current transport across the a-c junction also begins to change from one which is dominated by recombination to one where both recombination and diffusion become significant: J_{na}, J_{pa} and J_{tac}. Thus,

$$J_c = J_{na} + J_{pa} + J_{tac} \qquad (2.47)$$

Current continuity for electrons across point A (see Fig. 2.5) is

$$-J_{na} + J_{ta} + J_{tei} + J_{tai} = 0 \qquad (2.48)$$

and for holes across point B (see Fig. 2.5) is:

$$J_{pe} - J_{tai} - J_{ta} - J_{tac} = 0 \tag{2.49}$$

These expressions for current continuity indicate that the current continuity at points A and B are composed of current density components from the e-i, a-i and a-c junctions–all three junctions are involved. Furthermore, Eqs. (2.48) and (2.49) also show that current continuity is achieved by a balance between the diffusion and net-recombination current density components.

From a carrier flow perspective, holes which are injected into the emitter are divided into two flows: one which will recombine at the e-i junction while the remainder flows across the e-i junction. The holes which flow across the forward biased e-i junction drift across the reverse biased a-i junction and arrive at the neutral active layer. Since the a-i junction is reverse biased, electron-hole pairs are generated within the a-i depletion region. These generated holes also drift across the reverse biased a-i junction and arrive at the neutral active layer. The total number of holes that arrive at the neutral active layer is composed of holes which have flowed across the e-i junction and holes which have been generated across the a-i junction. These holes will diffuse across the neutral active layer toward the collector contact. A fraction of these holes recombine at the a-c junction with the remainder flowing across the a-c junction towards the collector contact.

Similarly, electrons which are injected into the collector are divided into two flows: one fraction will recombine at the a-c junction while the remainder flows across the a-c junction. The electrons which flow across the forward biased a-c junction, diffuse across the neutral active layer, drift across the a-i junction, as they flow toward the emitter. Since the a-i junction is reverse-biased, electron-

hole pairs are being generated. The generated electrons also drift across the a-i junction and flow toward the emitter. Thus, the total electron flow is composed of electrons which have flowed across the a-c junction and electrons which have been generated across the a-i junction. These electrons flow towards the emitter with a fraction of them recombining at the e-i junction while the remainder will flow across the junction towards the emitter contact.

With every increase in J_e, there is an increase in both the diffusion and net-recombination current density components across the e-i junction: J_{ne}, J_{pe} and J_{tei}. This results in an increase in the forward bias of the e-i junction. Similarly, there is an increase in both the diffusion and net-recombination current density components across the a-c junction: J_{na}, J_{pa} and J_{tac}. This also results in an increase in the forward bias of the a-c junction. If the incremental increase in J_{pe} and J_{na} is not sufficient to sustain the increase in J_{tei} and J_{tac}, a further decrease in the net-recombination current density across the a-i junction is required to compensate for the difference. This is effected by an increase in the reverse bias voltage across the a-i junction. If, however, the incremental increases in J_{pe} and J_{na} alone are able to sustain the increase in J_{tei} and J_{tac}, no further change in the net-recombination current density across the a-i junction is required. This represents the maximum reverse bias voltage across the a-i junction with J_e, and corresponds to the switching point of the device. The device resistance in the OFF state and the switching point (voltage and current) are important figures of merit used in describing the blocking efficiency and the stability of the device.

NDR State

The NDR state of operation resides between the switching and holding points of the DOES (see Fig. 2.7). In this regime of operation, as J_e increases, the incremental increases in J_{pe} and J_{na}, are larger than the incremental increase in J_{tei} and J_{tac}. This results in a reduction in the generation current, across the a-i junction, required to ensure current continuity and hence, a reduction of the reverse bias across the a-i junction. As J_e increases, the incremental change in J_{pe} and J_{na} becomes increasingly larger relative to the incremental increase in J_{tei} and J_{tac}. This further reduces the generation current density, across the a-i, that is required to maintain current continuity across the structure. This in turn reduces the reverse bias across the a-i junction and also the device voltage.

The reduction in the reverse bias voltage of the a-i junction and device voltage with increasing J_e continues until the diffusion current component becomes the dominant current transport mechanism. At this point, a-i becomes forward biased and the a-i junction becomes a source of current recombination. The current and voltage corresponding with this condition is referred to as the holding voltage (V_h) and holding current (I_h).

ON State

The ON state is defined by the region of operation where $J_e > J_h$. In this regime of operation, diffusion current transport is dominant across the structure and all three p-n junctions are under forward bias. As J_e increases, the diffusion current density components flowing across the structure increase, resulting in an increase in the forward bias of the e-i, a-i and a-c junctions. Since the voltage across the emitter-collector terminal is given by

$$V_{ec} = V_{ei} - V_{ai} + V_{ac} \tag{2.50}$$

the V_{ec} increases with increasing J_e. The resistance across the device in the ON state is an important figure of merit and should be minimized. The holding point and the ON-state resistance are also important in describing the switching character of the DOES device.

2.3.3 Two-Terminal L-J Characteristics

Figure 2.9 shows the light-current density (L-J) characteristic of the DOES device with the λ = 0.9 µm and λ = 1.3 µm optical emission components. The λ = 0.9 µm emissions originate from electron-hole pair recombination at the e-i junction while λ = 1.3 µm emissions originate from electron-hole pair recombination at the a-i junction. In the OFF and NDR states of operation, where $J_e < J_h$, the e-i junction is forward biased while the a-i junction is reverse biased. As a result, only λ = 0.9 µm are evident. As J_e increases, λ = 0.9 µm emissions increases essentially linearly. In the ON state, where $J_e > J_h$, both the e-i and the a-i junctions are forward biased. As a result, both λ = 0.9 µm and λ = 1.3 µm emission components are emitted from the device. As J_e increases, both λ = 0.9 µm and λ = 1.3 µm emissions increase essentially linearly with J_e. The rate of increase for λ = 1.3 µm emissions is approximately 5 times greater than that for λ = 0.9 µm emissions and therefore, the λ = 1.3 µm emissions rapidly becomes the dominant emission component.

2.3.4 Effect of Inversion-Channel Current

Figure 2.10 shows a family of J-V curves with J_i as the parametric variable. In this figure, J_i is negative because electrons are being injected into the inversion-channel contact and therefore, current flow is directed out of the

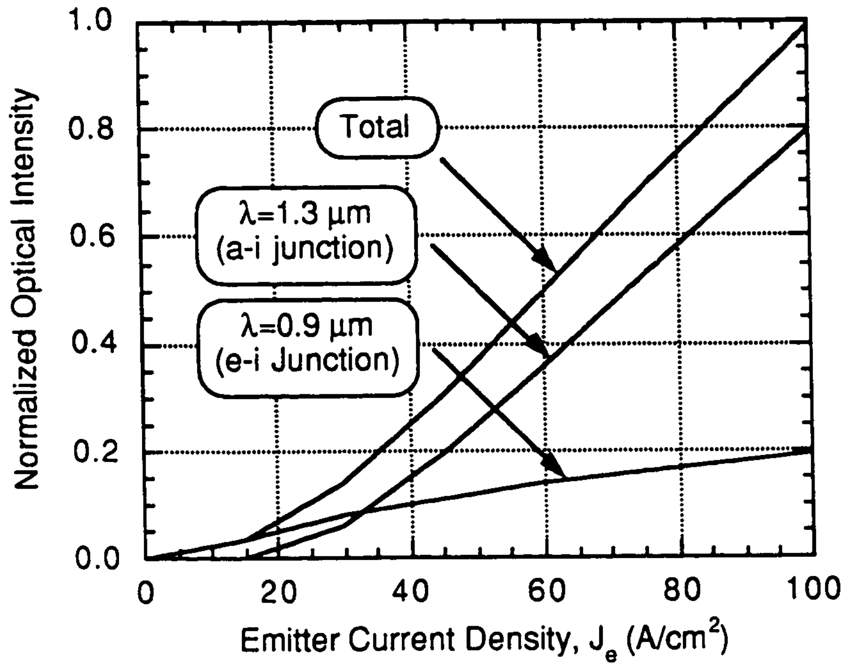


***Figure 2.9:** Light-current density (L-J) characteristic of the DOES.*

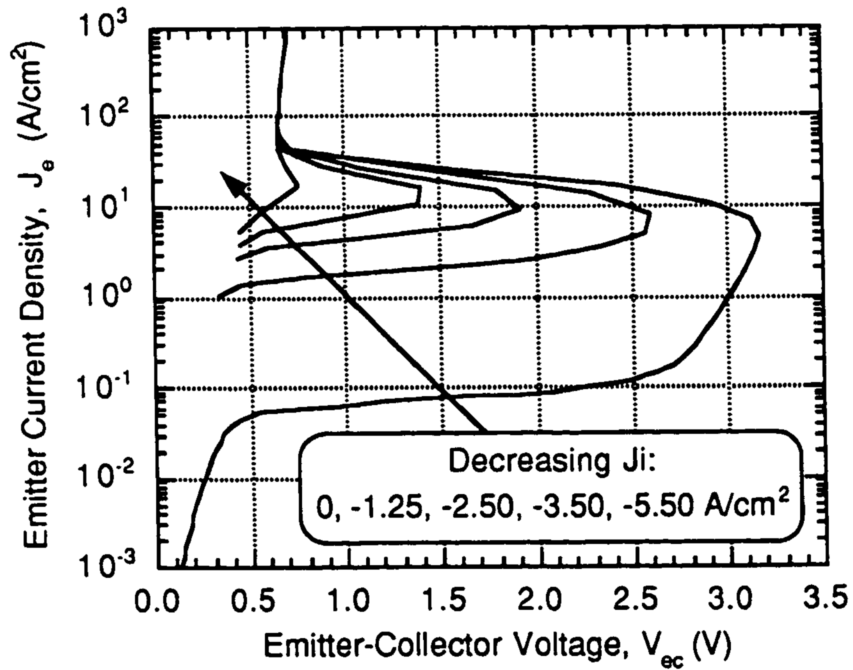


***Figure 2.10:** J-V characteristic of the DOES with inversion-channel current density (J_i) as the parametric variable.*

contact. The figure shows that J_i significantly influences the operation of the device in the OFF and NDR states, where $J_e < J_h$. As J_i decreases, the OFF state current density increases and V_{sw} decreases: V_{sw} = 3.16, 2.60, 1.92, 1.40 and 0.76 V for J_i = 0, -1.25, -2.50, -3.50 and -5.50 A/cm^2. In the ON state, where $J_e > J_h$, J_i has little influence on the operation of the device as there is no change in V_h, and in the ON state characteristics, with J_i.

Figures 2.11(a–c) show the effect of J_i on the operation of the e-i, a-i and a-c junctions. It shows that J_i does not change the J-V character of the e-i and a-c junctions but significantly affects the operation of the a-i junction. Electrons, which are injected into the inversion channel via the inversion-channel contact, flow across the e-i junction towards the emitter contact. To maintain current continuity across the structure, this flow of electrons is compensated by a corresponding reduction in the flow of electrons which are thermally generated at the a-i junction. This reduction in the thermal generation from the a-i junction results in a reduction in the maximum reverse-biased voltage across the a-i junction ($\hat{V}_{ai}$): $\hat{V}_{ai}$ = -2.58, -1.92 and -1.21 V for J_i= 0, -1.25 and -2.5 A/cm^2. This in turn results in a reduction in the switching voltage of the device.

2.3.5 Effect of Active-Layer Current

Figure 2.12 illustrates a family of J-V curves with J_a as the parametric variable. A positive value of J_a indicates that holes are being injected into the neutral portion of the active layer. The figure shows that J_a significantly influences the device in the OFF and NDR states, where $J_e < J_h$. As J_a increases, the OFF state current density increases and V_{sw} decreases: V_{sw} = 3.16, 2.59, 1.91, 1.25 and 0.70 V for J_a = 0, 5.0, 7.5, 10.0 and 13.0 A/cm^2. J_a has little influence on

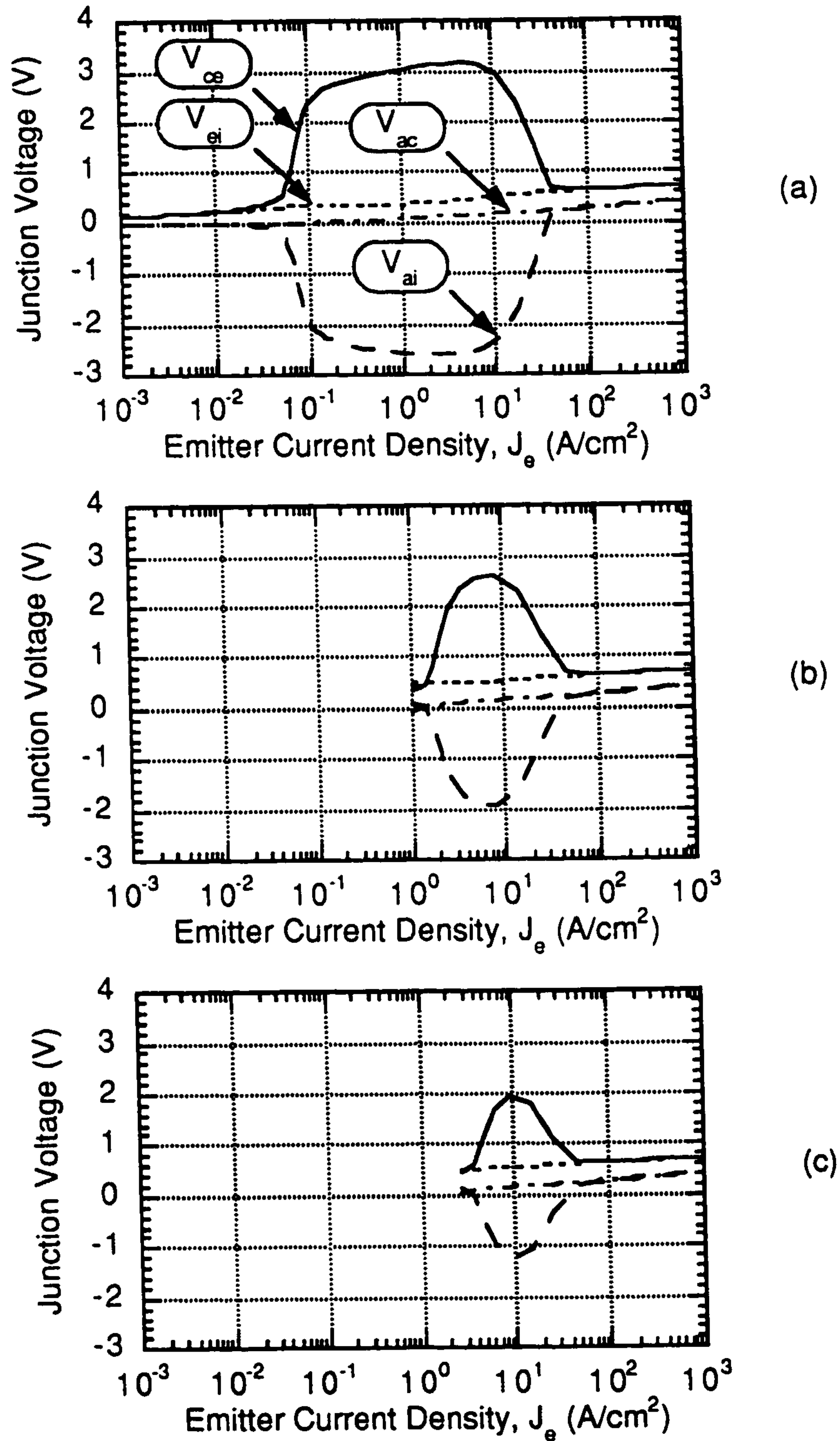


Figure 2.11: Voltage across the e-i, a-i and a-c junctions as a function of emitter current density with inversion-channel current density J_i = a) 0, b) -1.25 and c) -2.5 A/cm^2.

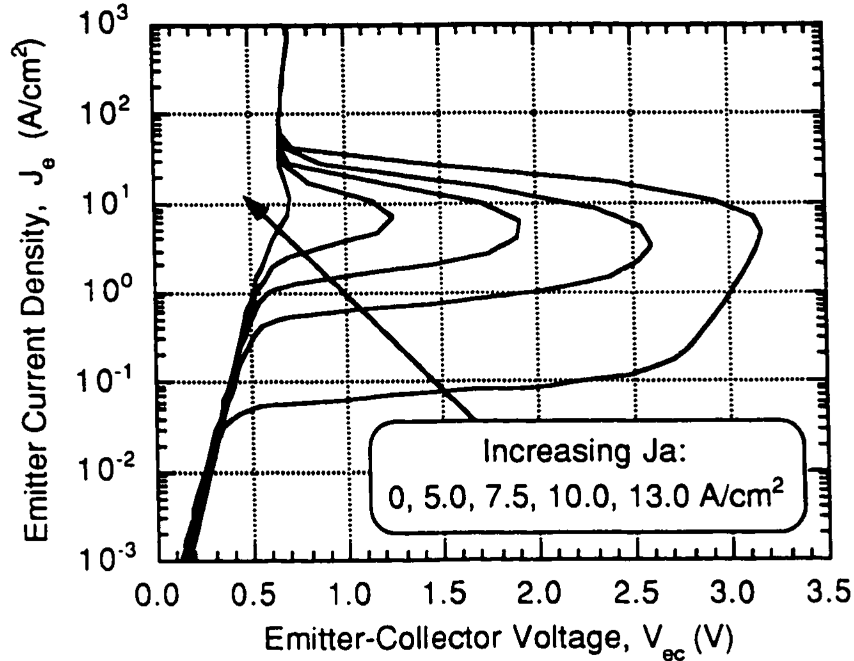


Figure 2.12: J-V characteristic of the DOES with active-layer current density (J_a) as the parametric variable.

the operation of the device in the ON state, where $J_e > J_h$ as there is no significant change in V_h, and in the ON state characteristics, with J_a.

Figures 2.13(a–c) show the effect of J_a on the operation of the e-i, a-i and a-c junctions. It shows that J_a does not change the J-V character of the e-i junction but affects the operation of the a-i and a-c junctions. Holes which are injected into the neutral active layer via the active layer contact flow across the a-c junction towards the collector contact, forward biasing the a-c junction. This is reflected in the increase of V_{ac} with J_a in the region of operation where $J_e < J_a$. To maintain current continuity across the structure, this flow of holes is compensated by a corresponding reduction in the flow of holes that are thermally generated at the a-i junction. This reduction in the thermal generation from the a-i junction results in a reduction of the maximum reverse bias voltage across the a-i junction ($\hat{V}_{ai}$):

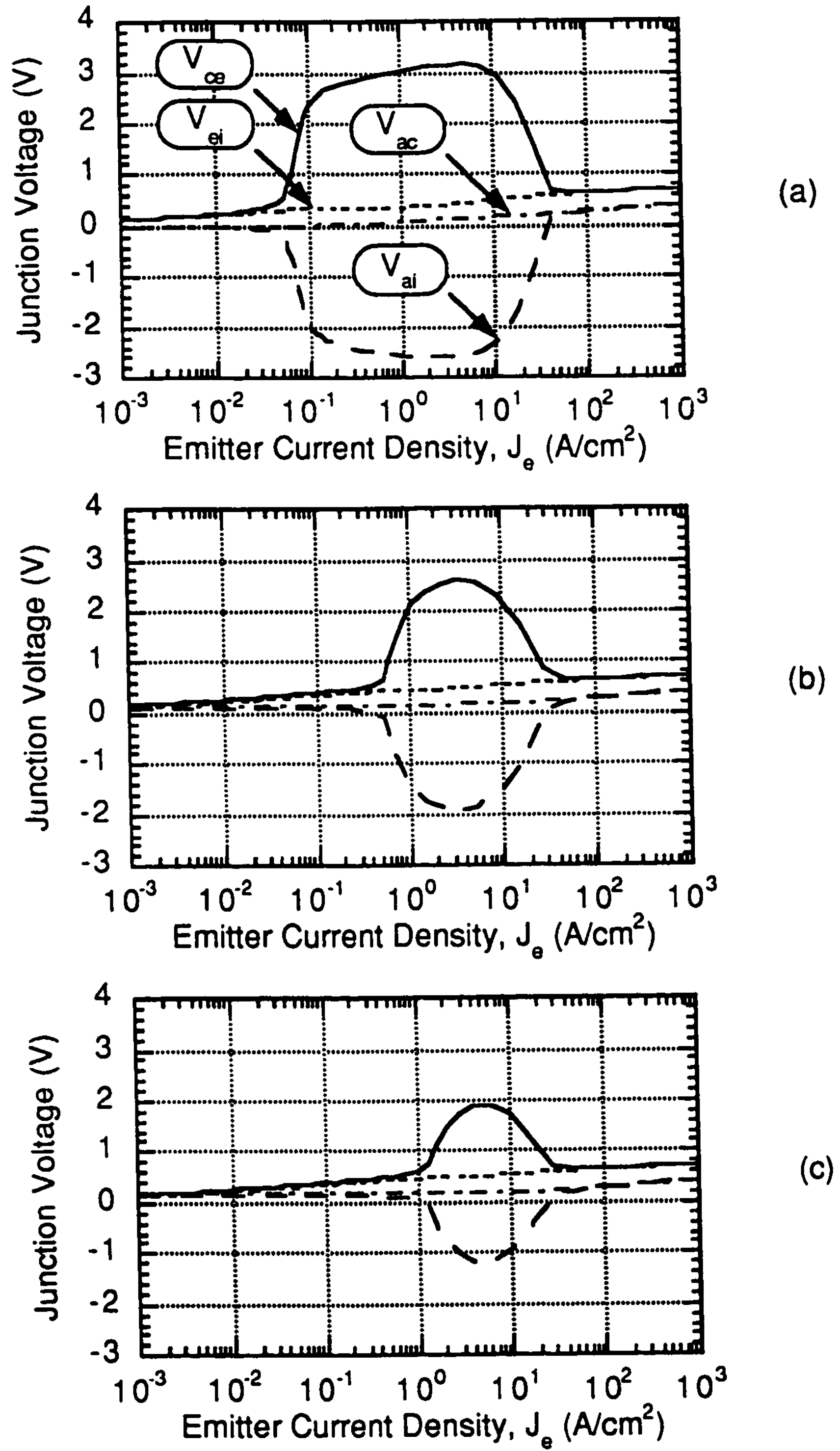


Figure 2.13: Voltage across the e-i, a-i and a-c junctions as a function of emitter current density with active-layer current density J_a = a) 0, b) 5.0 and c) 7.5 A/cm^2.

$\hat{V}_{ai}$ = -2.58, -1.93 and -1.19 V for J_a = 0, 5.0 and 7.5 A/cm^2. This in turn results in a reduction in the switching voltage of the device.

2.3.6 Efficiency of the Inversion-Channel and Active-Layer Current

Figure 2.14 shows the effect of J_i and J_a on V_{sw} by summarizing the results of Figs. 2.10 and 2.12. It also shows that J_i is more effective in reducing V_{sw} than J_a. This results primarily because the electrons that are injected into the inversion-channel contact can flow directly across the e-i junction towards the emitter contact. On the other hand, holes which are injected into the active layer must diffuse across part of the active layer before arriving at the a-c junction. This diffusion across the neutral active layer results in a loss of carriers through recombination. This loss is reflected by the reduction in switching efficiency of the active-layer contact.

2.3.7 Effect of Optical Injection

Figure 2.15 illustrates a family of J-V curves with the incident optical flux (Φ) with λ = 1.3 μm as the parametric variable. The figure shows that Φ significantly influences the device in the OFF and NDR states, where $J_e < J_h$. As Φ increases, the OFF state current increases and V_{sw} decreases: V_{sw} = 3.16, 2.68, 1.91, 1.38 and 0.76 V for Φ = 0, 2.5, 12.5, 20.0 and 37.5 s^{-1}cm^{-2}. Φ has little influence on the operation of the device in the ON state, where $J_e > J_h$, as there is no significant change in the ON state characteristic, and in V_h, with Φ. Figure 2.16 summarizes the results of Fig. 2.15 by showing the influence of Φ on V_{sw}.

Figures 2.17(a–c) show the effect of Φ on the operation of the e-i, a-i and a-c junctions. It shows that J_a does not change the J-V character of the e-i and a-c

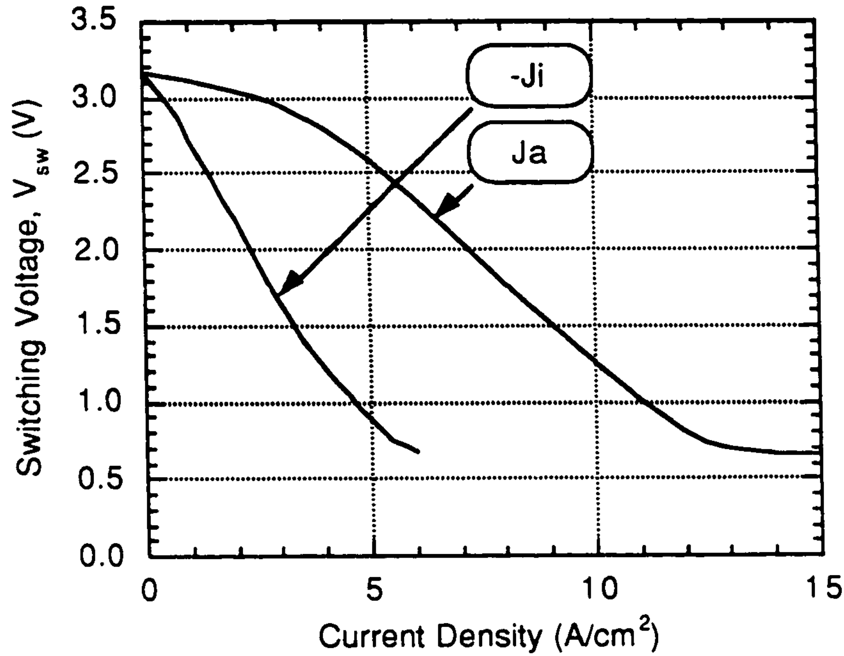


Figure 2.14: Switching voltage of the DOES as a function of the inversion-channel current density (J_i) and active-layer current density (J_a).

junctions but affects the operation of the a-i junction. The incident photons have a wavelength of 1.3 μm and therefore, will only be absorbed by the active layer. When these photons are absorbed within the active layer, electron-hole pairs are generated. These optically generated carriers supplement the thermal generation that takes place in the a-i junction and, thus, reduces $\hat{V}_{ai}$: $\hat{V}_{ai}$ = -2.58, -2.02 and -1.20 V for J_a= 0, 2.5 and 12.5 $s^{-1}cm^{-2}$. This in turn results in a reduction in the switching voltage of the device.

An interesting characteristic demonstrated by the DOES is that regardless of the wavelength of the incident light used to modulate the switching voltage, the light that is emitted from the device is still centered at λ = 1.3 and λ = 0.9 μm. This implies that the device has the potential of operating as a wavelength converter.

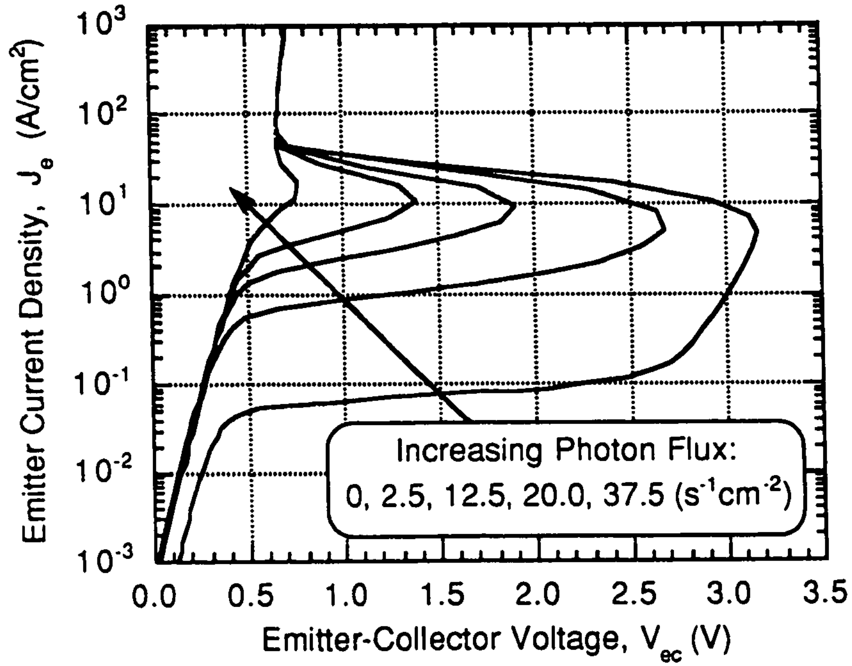


Figure 2.15: J-V characteristic of the DOES with incident photon flux as the parametric variable.

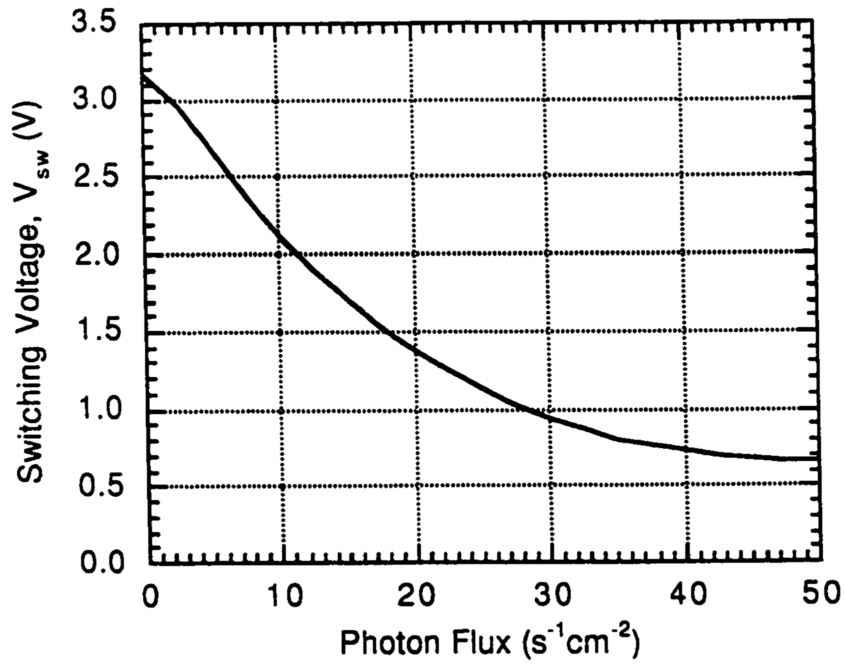


Figure 2.16: Switching voltage of the DOES as a function of the incident photon flux.

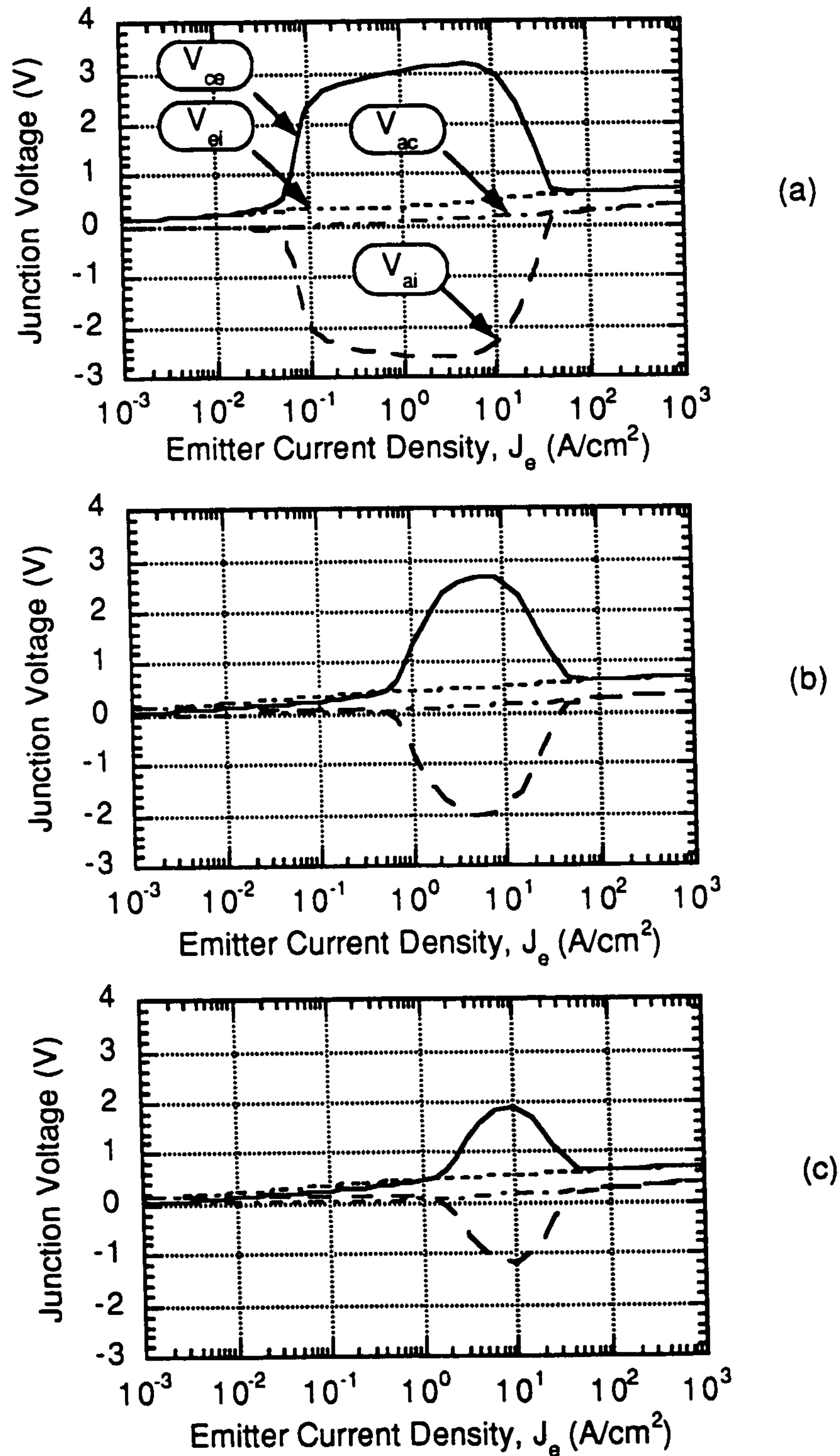


Figure 2.17: Voltage across the e-i, a-i and a-c junctions as a function of emitter current density with incident optical flux Φ = a) 0, b) 2.5 and c) 12.5 $s^{-1}cm^{-2}$.

2.4 DEVICE STRUCTURE DESIGN

Figure 2.18 shows the switching voltage of the device decreasing as the charge sheet doping (N_δ) increases. V_{sw} ranges from 0.6 to 15.5 V as N_δ ranges from 3×10^{18} to 1×10^{19} cm^{-3}. This rapid change in V_{sw} with N_δ emphasizes the importance of maintaining precise control over the doping density and thicknesses of this layer both during growth and through the device fabrication process. Figures 2.19(a) and (b) show that the switching voltage decreases as the doping of the emitter and active layers increases. A comparison of these plots show that the active layer has slightly more influence over the switching voltage. Figure 2.19(c) indicates that the collector layer doping does not significantly affect the switching voltage of the DOES.

The preceding discussions show that the DOES device affords the designer several degrees of freedom to tailor its performance for specific applications. This is an important feature as the DOES is designed to be part of an integrated technology. Invariably, in such an implementation the performance of each device in the circuit is traded-off to optimize the performance of the integrated circuit.

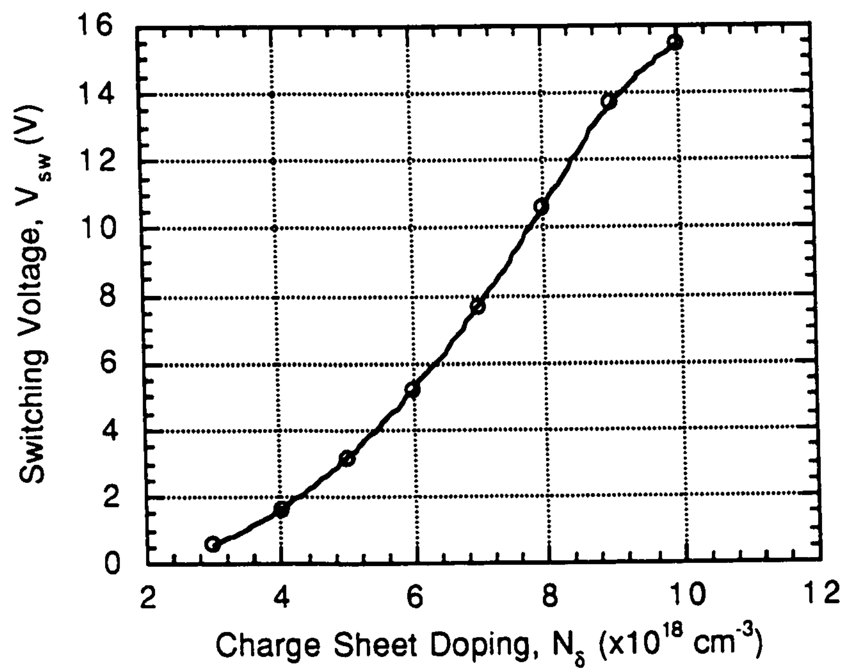
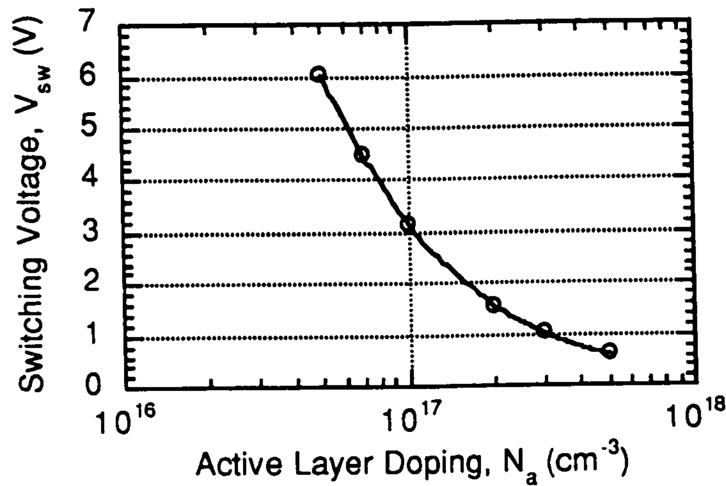
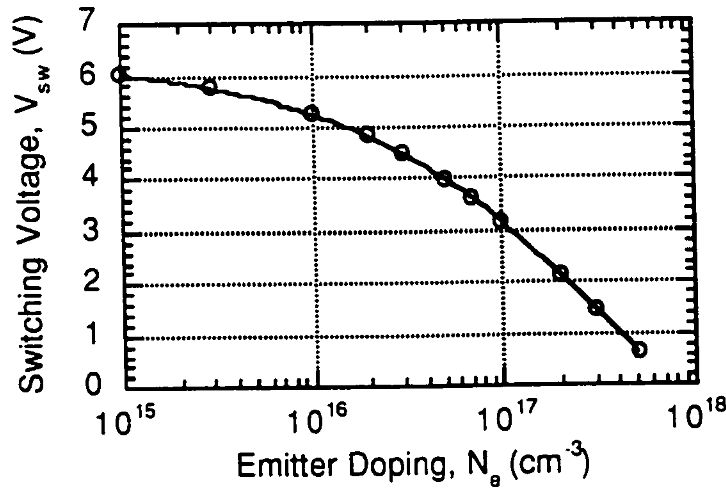


Figure 2.18: Switching voltage of the DOES as a function of the charge sheet doping (N_δ).





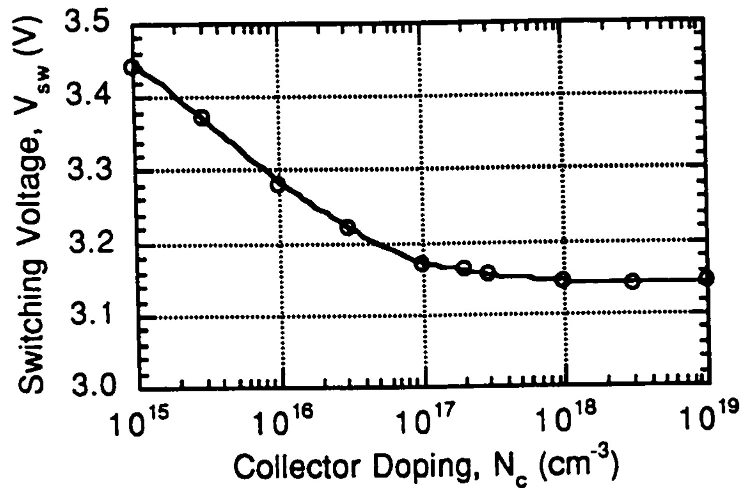


***Figure 2.19:** Switching voltage of the DOES as a function of a) emitter, b) active layer and c) collector layer doping.*

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CHAPTER 3

DESCRIPTION AND THEORY OF THE HFET

The heterojunction field-effect transistor (HFET) is another device from the ICT family. It is a unipolar transistor that is similar in operation to the modulation doped field-effect transistor (MODFET) or high-electron-mobility transistor (HEMT). The HFET can be utilized in signal processing applications as an amplifier or a switch, and in biasing applications as an active load or a voltage controlled current source. The HFET device structure is fully compatible with other devices from the ICT family allowing it to be monolithically integrated with devices including the DOES, BICFET and BICPT.

This chapter begins with a presentation of the n-channel InGaAsP-InP based HFET device structure followed by the development of a model to describe device operation. This semi-analytical model, derived by applying the Bulk Charge Theory [1] to the HFET structure, provides a qualitative understanding of input and output current-voltage characteristics, and transconductance characteristics. This allows for a detailed understanding of device physics and operation, and provides a comparison for experimental results presented in Chap. 6. This is important as it allows us to verify the operation of the fabricated

devices, critically analyze device performance and provide insights into improving the device structure and fabrication process. The model also identifies the influence of emitter, charge sheet and active layer doping concentration on the threshold voltage of the device. Such relationships were used in the design of the HFET structure to ensure its compatibility with the DOES, BICFET and BICPT.

3.1 DEVICE STRUCTURE

Figure 3.1 shows a schematic cross-section of the heterojunction field-effect transistor (HFET). The device structure of the HFET is identical to the DOES (see Fig. 2.1) and consists of a p-InP emitter, an n-InP charge sheet, an undoped-InGaAsP (λ=1.3 μm) voltage drop, a p-InGaAsP (λ=1.3 μm) active layer, an n-InP collector and an n-InP substrate layer. The doping concentration and layer thickness of the charge sheet is designed such that this layer is almost fully depleted under all operating conditions. This common device structure ensures compatibility of the DOES, BICFET, BICPT and HFET for monolithic integration. Although the HFET and DOES share the same device structure, the collector layer which is shown in Fig. 3.1 is not required for HFET operation. Operation of the HFET is based only on the emitter, inversion-channel, undoped-active and active layers only. Ohmic contacts to the HFET are made to each end of the inversion-channel and also to the emitter layer. To maintain consistency with conventional MODFET/HEMT terminology, the p-InP emitter layer and the ohmic emitter metal contact of the HFET will be referred to as the gate.

3.2 BIASING AND OPERATION

Figure 3.2 shows an n-channel HFET biased in the common-source circuit configuration. This circuit configuration is adopted in generating the device characteristics presented in this chapter. The input circuit is connected across the gate and source contacts, and the output circuit is connected across the source and drain contacts. The source which is common to both the input and output circuits is grounded. The drain is typically biased negatively relative to the source. Under typical operating conditions, the gate-source voltage (V_{gs}) is used to establish the density of electrons within the inversion channel (Q_{ni}), while the drain-source voltage (V_{ds}) establishes an electric field along the length of the inversion channel. This field causes the electrons within the channel to flow from the source contact towards the drain contact, generating the drain current (I_d).

Figure 3.3 presents a magnified cross-sectional view of the HFET showing the variation of Q_{ni} and V_c with position (x). A two-dimensional model is required to account for the behaviour of the HFETs because of the way V_{ds} and V_{gs} are applied. The application of V_{ds} and V_{gs} gives rise to a position-dependent channel voltage $(V_c(x))$ and electron density within the channel $(Q_{ni}(x))$. At the source end of the channel, $V_c(0) = V_{gs}$ and the electron density is at a maximum, while at the drain end of the channel, $V_c(L) = V_{gs} - V_{ds}$ and the electron density is at a minimum.

3.3 CHARGE CONSERVATION AND FIXED CHARGE COMPONENTS

Within the HFET structure, the source for positive fixed charge arises from the depleted charge-sheet layer. The sources for negative charge are:

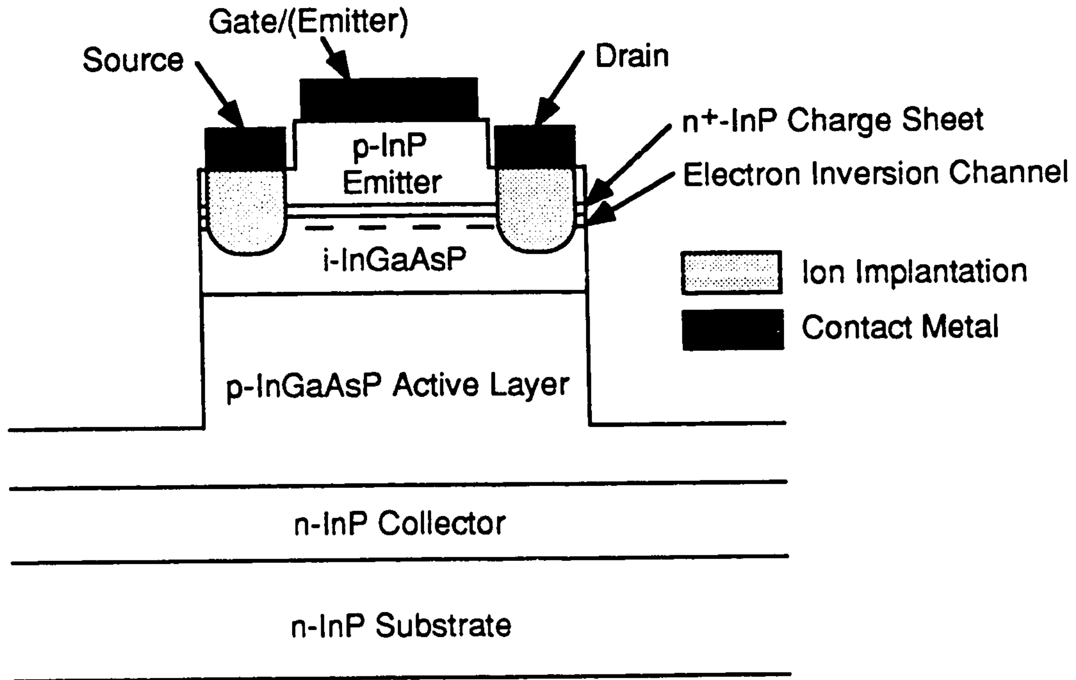


Figure 3.1: Schematic cross-sectional view of the n-channel InGaAsP-InP heterojunction field-effect transistor (HFET).

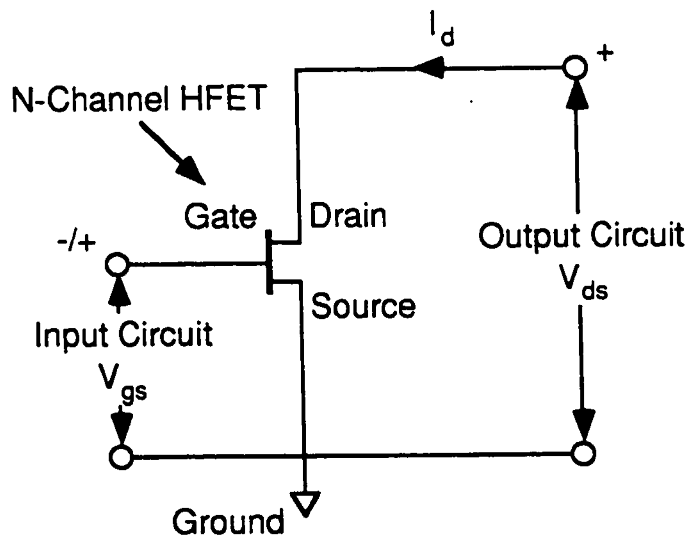


Figure 3.2: Typical biasing scheme for an n-channel HFET in the common-source circuit configuration.

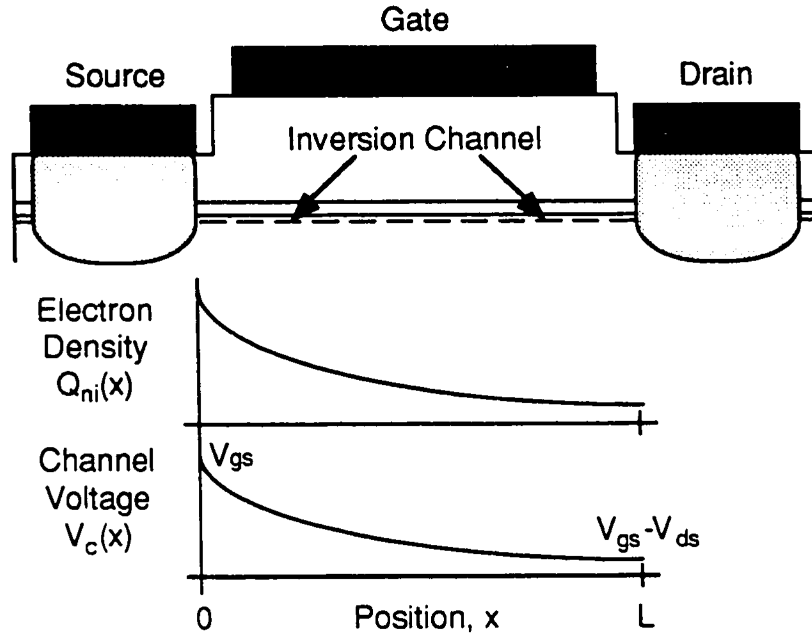


Figure 3.3: Magnified cross-sectional view of the HFET illustrating the variation of the electron density (Q_{ni}) and channel voltage (V_c) with position (x).

ionized dopants in the depletion regions of the gate(emitter) layer, the active layer and the accumulation of electrons in the inversion channel. As in the case of the DOES (see Sect. 2.2.2), charge neutrality across the HFET requires that

$$Q_e - Q_\delta + Q_{ni} + Q_{a1} = 0 \tag{3.1}$$

where Q_e, Q_δ, Q_{ni} and Q_{a1} represent the magnitude of the areal charge density of the emitter, charge sheet, inversion channel and active layers; and bear units of charge per unit area (C/cm^2). Expressions for the depletion charges Q_e, Q_{a1} and Q_δ, derived in Sect. 2.2.2, are

$$Q_e = \left(2q\varepsilon_e N_e \phi_e\right)^{1/2} \tag{3.2}$$

$$Q_{a1} = \left(2q\varepsilon_a N_a \phi_{a1}\right)^{1/2} \tag{3.3}$$

$$Q_\delta = \frac{N_\delta W_\delta}{1 + \exp\left[-\left(\Delta E_c - E_a - \Delta E_{fi}\right)/V_T\right]} \tag{3.4}$$

The relative magnitudes of charges in each of the layers, at any point (x) along the inversion channel, are governed by V_c, which is related to the internal potentials and energy levels by (see Fig. 3.4),

$$V_c = -\phi_e + \phi_u + \phi_{a1} + \Delta E_{fa} - \Delta E_{fe} + \Delta E_v \tag{3.5}$$

Experimentally, the active layer of the HFET is allowed to float to a potential dictated by the bias applied at the gate, source and drain contacts. This floating potential is position dependent and cannot be solved for analytically. To expedite a semi-analytical solution, the active layer is assumed to be at a potential such that $V_{ai} = 0$. With this assumption,

$$\Delta E_{fi} = \phi_u + \phi_{a1} + \Delta E_{fa} - E_{gu} \tag{3.6}$$

3.4 CHARGE STATES

The source of positive fixed charge within the HFET structure comes from the ionized dopants in the charge sheet layer, while the source of negative charge contribution arises from the ionized dopants in the depletion regions of the emitter, active layers and the accumulation of electrons in the inversion channel. The relative magnitudes of these charge components, Q_e, Q_δ, Q_{ni} and Q_{a1}, along the length of the HFET structure forms the basis for HFET operation. Two charge states can be defined based on the relative magnitudes of Q_{ni} to the carrier density in the bulk of the active layer. Following conventional MODFET theory [4], Q_{ni} can be described in terms of a surface potential (ϕ_s) defined by (see Fig. 3.4)

$$\phi_s = \phi_u + \phi_{a1} \tag{3.7}$$

and the carrier density in the bulk can be described by the bulk potential (ϕ_b) (see Fig. 3.4) defined as

$$\begin{aligned} \phi_b &= V_T \ln\left(\frac{N_a}{n_{ia}}\right) \\ &\approx E_{gu}/2 - \Delta E_{fa} \end{aligned} \tag{3.8}$$

The HFET is in a state of depletion when it is biased such that $\phi_s < 2\phi_b$, see Fig. 3.4(b). In this state, Q_{ni} is much less than the bulk majority carrier concentration in the active layer and is assumed to be negligible. There are no electrons in the inversion channel to participate in current conduction. The HFET is in a state of strong inversion when it is biased such that $\phi_s \geq 2\phi_b$, see Fig. 3.4(c). In this state, the electron concentration in the inversion channel is greater than the bulk majority carrier concentration and there is significant electron accumulation within the inversion channel. These electrons within in the inversion channel can participate in current conduction. The density of electrons in the inversion channel, at any point x along the channel is given by

$$Q_{ni} = Q_\delta - (Q_e + Q_{a1}) \tag{3.9}$$

The channel voltage at which $\phi_s = 2\phi_b$ marks the transition from a state of depletion to strong inversion. This marks the onset of electron accumulation within the inversion channel of the HFET where $Q_{ni} = 0$ for $\phi_s \leq 2\phi_b$, and $Q_{ni} > 0$ for $\phi_s > 2\phi_b$.

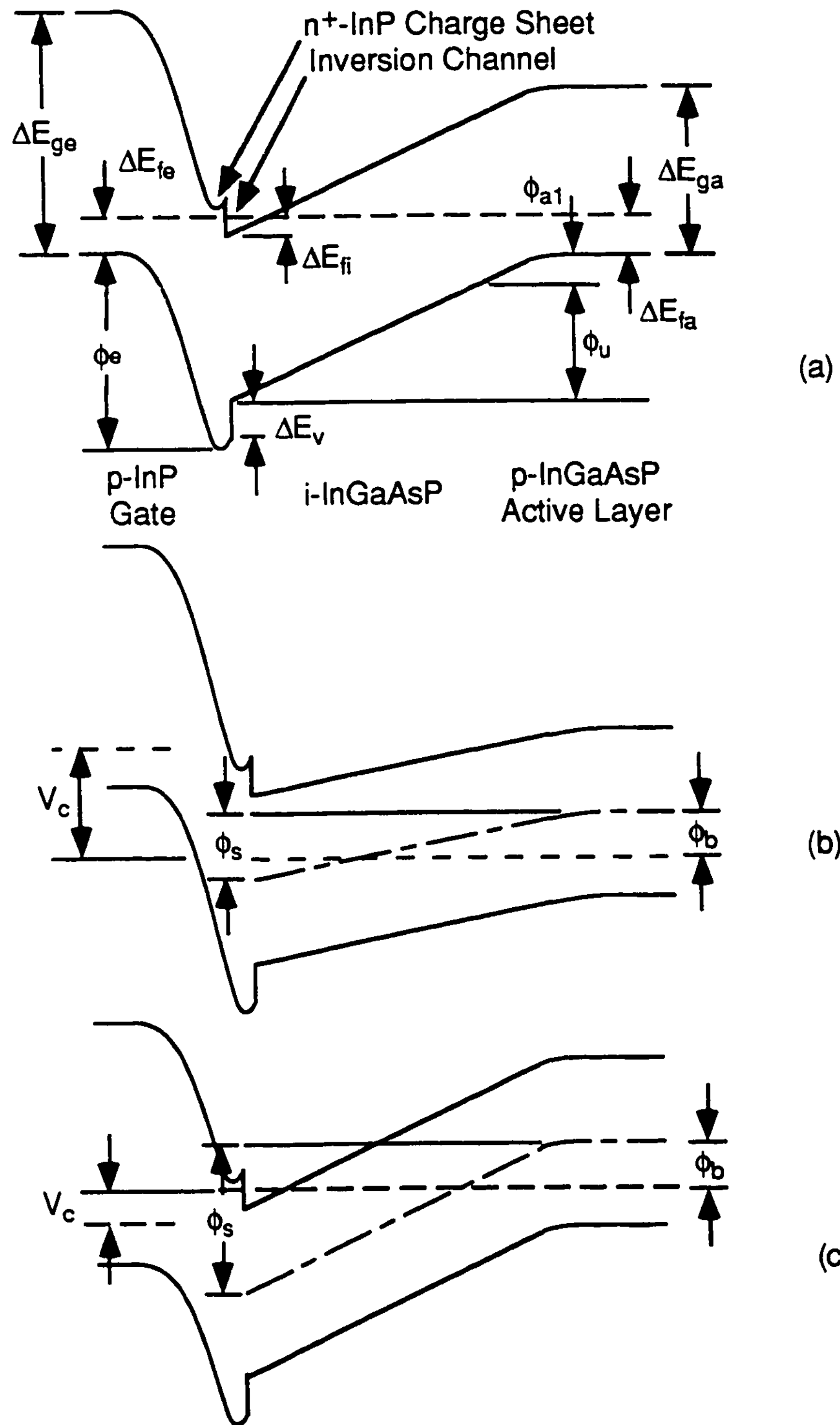


Figure 3.4: Energy band representation of the n-channel HFET under a) Equilibrium, b) Depletion and c) Strong Inversion.

Threshold Voltage

The threshold voltage (V_{th}) is defined as the gate-source voltage (at $V_{ds} = 0$) at which the onset of strong inversion ($\phi_s = 2\phi_b$) is achieved:

$$V_{th} = -\phi_{e,V_{th}} + 2\phi_b - \Delta E_{fe} + \Delta E_{fa} + \Delta E_v \tag{3.10}$$

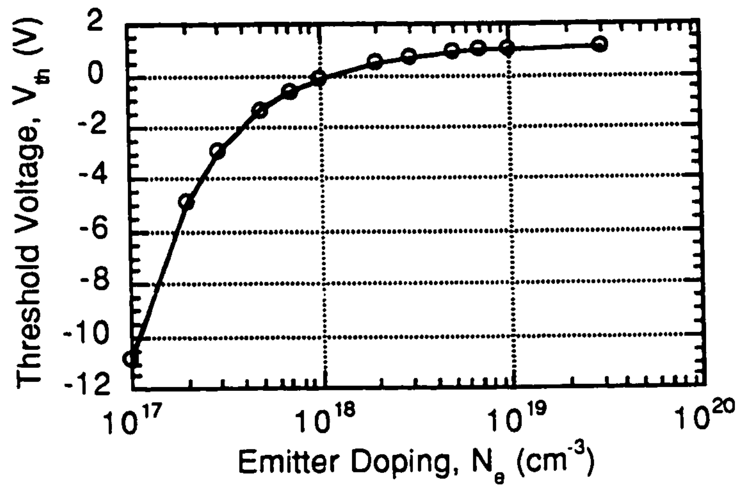
A relationship between $\phi_{e,V_{th}}$ and ϕ_b is obtained by imposing charge neutrality Eq. (3.1) and assuming $Q_{ni} = 0$ at threshold,

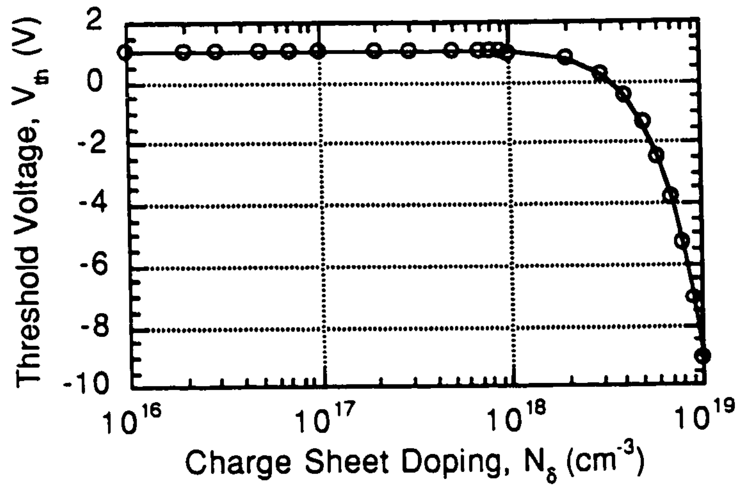
$$Q_e - Q_\delta + Q_a = 0 \tag{3.11}$$

Substituting Eqs. (3.2)–(3.4) into Eq. (3.11) and solving for $\phi_{e,V_{th}}$ yields

$$\phi_{e,V_{th}} = \frac{Q_\delta - \left(2q\varepsilon_a N_a (2\phi_b)\right)^{1/2}}{2q\varepsilon_e N_e} \tag{3.12}$$

The expression for V_{th} reveals the coupling between device structure and the charge states within the device. This allows V_{th} to be established by appropriate selection of doping concentration of the emitter, charge sheet and active layers. Figures 3.5(a–c) illustrate the dependence of V_{th} on the emitter, charge-sheet and active-layer doping. The trends indicate that V_{th} increases with increasing emitter and active layer doping, but decreases with increasing charge sheet doping. In all cases, depletion and enhancement mode devices can be achieved by varying the doping levels of the layers. These results show the HFET allows the device designer the flexibility to tailor its performance to match the requirements of the application.





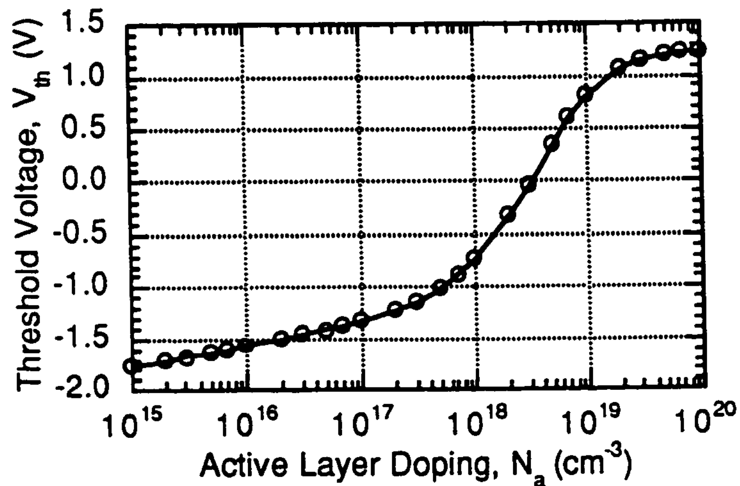


Figure 3.5: *Threshold voltage of the HFET as a function of the a) emitter, b) charge sheet and c) active layer doping.*

3.5 CURRENT-VOLTAGE CHARACTERISTIC

Current flow within the inversion channel of the HFET is modeled by assuming that the dominant carrier transport mechanism responsible for current flow along the length of the channel is drift. Also, assuming the absence of any current sources or sinks within the inversion channel, I_d can be obtained by integrating across the width (W) and length (L) of the HFET (see Fig. 3.6),

$$\begin{aligned} I_d &= \iint J_n\big|_{drift} dxdy \\ &= W\int Q_{ni}\bar{\mu}_n \xi dx \end{aligned} \tag{3.13}$$

where $J_n|_{drift}$ is the drift component of current and $\bar{\mu}_n$ is the effective mobility of electrons in the inversion channel. The electric field (ξ) along the length of the channel at x is given by

$$\xi = \frac{dV_c(x)}{dx} \tag{3.14}$$

Substituting Eq. (3.14) into (3.13) yields

$$I_d = -\frac{W}{L}\bar{\mu}_n \int_0^{V_{ds}} Q_{ni} dV_c \tag{3.15}$$

Equation (3.15) shows that $I_d \neq 0$ only when $Q_{ni} \neq 0$, a condition that exists when the device is biased in a state of strong inversion. Equations (3.15), (3.8) and (3.2)–(3.4) reveal the coupled nature of the expressions which make it impossible to obtain a closed form analytical solution for I_d. The solution to Eq. (3.15) is found by numerical integration. The solution to Eq. (3.15) is divided into two regions, linear and saturation, dictated by the state of the inversion channel.

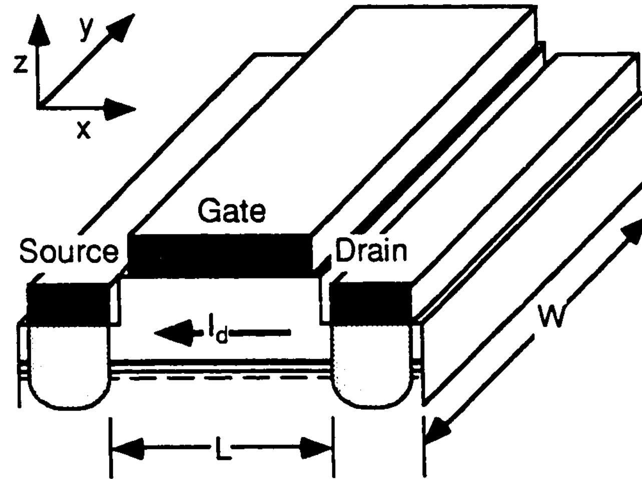


Figure 3.6: Three-dimensional view of the n-channel HFET.

Linear Region

When V_{ds} is applied across the drain and source, it is distributed along the length of the inversion channel reducing the channel voltage and, thus, the density of electrons in the inversion channel. At the source end of the channel $V_c(0) = V_{gs}$ and the electron density is at a maximum, however, at the drain end of the channel $V_c(L) = V_{gs} - V_{ds}$ and electron density is at a minimum (see Fig. 3.3). For small V_{ds}, the portion of the inversion channel at $x = L$ remains under strong inversion implying that the entire channel is also under strong inversion. Under these conditions, electrons within the channel experience unrestricted transport from source to drain and I_d is obtained by numerically integrating Eq. (3.15).

Saturation Region

As V_{ds} increases, $V_c(L)$ and, hence, $Q_{ni}(L)$ decreases until the inversion channel at the drain end makes the transition from being in a state of strong-inversion to depletion. When this condition is reached, the end of the channel

closest to the drain contact becomes pinched-off. The V_{ds} at which the channel is pinched-off is referred to as the saturation voltage and is defined as

$$V_{ds,sat} = V_{gs} + V_{th} \tag{3.18}$$

Further increases in V_{ds} above $V_{ds,sat}$ result in the additional voltage dropping across the pinched-off portion of the channel. As a result further increases in V_{ds} do not further influence the density of electrons within the inversion channel, hence, I_d saturates. For $V_{ds} \geq V_{ds,sat}$, I_d is constant and can be determined by numerically integrating

$$I_{d,sat} = \frac{W}{L}\bar{\mu}_n \int_0^{V_{ds,sat}} Q_{ni} dV_c \tag{3.19}$$

In practice, I_d continues to increase for $V_{ds} \geq V_{ds,sat}$ because the size of the pinched-off region increases, effectively decreasing the undepleted length of the inversion channel. This effect is not accounted for by this model.

Figure 3.7 illustrates the output current-voltage (I_d-V_{ds}) characteristic of the HFET with the structure listed in Table 3.1 Clearly identified on the figure are the linear and saturation regimes of operation. As expected, $V_{ds,sat}$ increases with increasing V_{gs}. The figure also shows V_{th} = -1.35 V and for V_{gs} < -1.35 V, I_d = 0.

***Table 3.1:** Device structure used in modeling of the HFET.*

Layer	Material	Layer Doping (cm^{-3})	Thickness (Å)
Gate/Emitter	p-InP	1×10^{17}	2000
Charge Sheet	n-InP	5×10^{18}	100
Voltage Drop	p-InGaAsP	6×10^{15}	2000
Active Layer	p-InGaAsP	1×10^{17}	5000

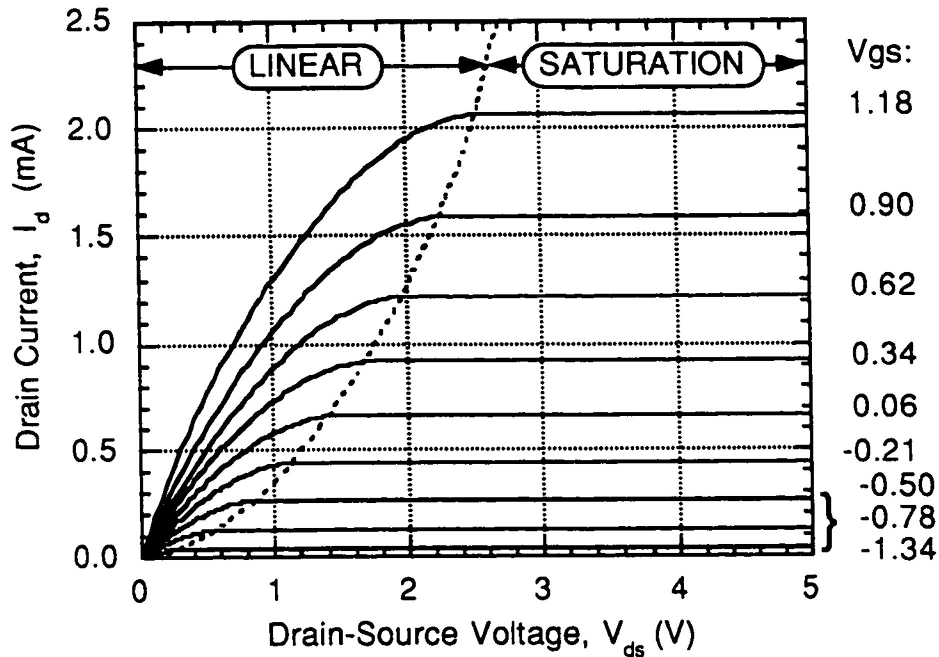


Figure 3.7: I_d-V_{ds} *characteristic of the HFET.*

3.6 TRANSCONDUCTANCE

Transconductance (g_m) is a figure of merit defined as

$$g_m = \frac{\Delta I_d}{\Delta V_{gs}} \tag{3.20}$$

where ΔI_d is the change in I_d which corresponds to a change of ΔV_{gs} for a fixed V_{gs}. This figure of merit quantifies the efficiency of V_{gs} in modulating I_d. Figure 3.8 shows the transconductance for the HFET structure of Table 3.1 at $V_{ds} > V_{ds,sat}$. For $V_{gs} < V_{th}$, there is no current conduction and thus, $g_m = 0$. The transconductance increases linearly between V_{gs} = -1.35 V and 0.5 V, but begins to increase superlinearly for V_{gs} > 0.5 V. This superlinear increase in

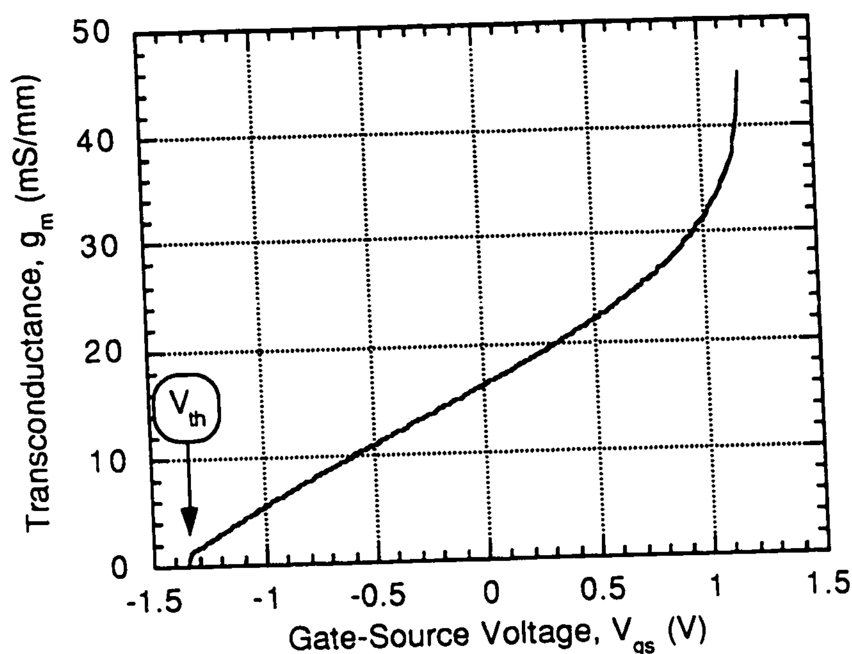


Figure 3.8: Transconductance characteristic of the HFET.

transconductance results from the exponential increase in Q_{ni} and, hence I_d, with V_{gs}.

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CHAPTER 4

DESCRIPTION AND THEORY OF THE BICFET AND BICPT

The bipolar inversion-channel field-effect transistor (BICFET) is another device from the ICT family. It is a bipolar transistor that is similar in operation to the bipolar-junction transistor (BJT) or heterojunction bipolar-junction transistor (HBT). The BICFET is capable of achieving high output current densities and high current gains. These devices are suitable for application as amplifiers, oscillators, current sources and electronic switches. The bipolar inversion channel photo-transistor (BICPT) is also another device from the ICT family. The BICPT is an optoelectronic device, consisting of a photodetector coupled to a transistor. This device can detect an optical signal and generate an amplified version of the photo-generated current. These devices find application in opto-electronic receiver circuits. Both the BICFET and BICPT are fully compatible with other devices from the ICT family allowing them to be monolithically integrated with devices including the DOES and HFET. The BICFET and BICPT are presented in the same chapter

because the two devices are based the same device physics and operation, and are described by the same device model.

This chapter is an introduction to the n-channel InGaAsP-InP based BICFET and BICPT devices. It begins with a presentation of the BICFET and BICPT device structures followed by the development of a model to predict device operation. This semi-analytical model is derived based on the principles of drift and diffusion [1] to provide a qualitative understanding of the current-voltage and current gain characteristic of these devices. This model is also used to identify the influence of emitter, charge sheet and collector layer doping on the current gain characteristics of the BICFET and BICPT. These relationships are used extensively in the design of the n-channel InGaAsP-InP based BICFETs and BICPTs to ensure compatibility with the DOES and HFET.

Other theoretical device model of the BICFET have been presented by Tan [2] and Taylor [3] for n-channel AlGaAs-GaAs based devices. To date, no BICPT device models have been reported in literature.

4.1 DEVICE STRUCTURE

Figure 4.1(a) shows a schematic cross-section of the BICFET while Fig. 4.1(b) shows a schematic cross-section of the BICPT. The BICFET and BICPT structures are identical to the DOES and HFET (see Figs. 2.1 and 3.1), and consist of a p-InP emitter, an n-InP charge sheet, an undoped InGaAsP (λ=1.3 μm) voltage drop, a p-InGaAsP (λ=1.3 μm) active layer, an n-InP collector and an n-InP substrate. The doping concentration and layer thickness of the charge sheet is designed such that this layer is almost fully depleted under all

Figure 4.1: Schematic cross-sectional view of the n-channel InGaAsP-InP based a) bipolar inversion channel field effect transistor (BICFET) and b) bipolar inversion channel phototransistor (BICPT).

operating conditions. This common device structure ensures compatibility of the DOES, HFET, BICFET and BICPT for monolithic optoelectronic integration. Although the BICFET, BICPT, DOES and HFET share the same overall device structure, BICFET/BICPT operation does not require the use of the collector layer shown in Fig. 4.1. Operation of the BICFET/BICPT is based only on the emitter, inversion-channel, undoped active and active layers only.

The BICFET, being an electronic device, is biased via ohmic contacts to the emitter, inversion channel and active layers (see Fig. 4.1(a)). The BICPT has electrical contacts to only the emitter and active layers, however, it possesses a window in the emitter contact metal to allow for optical injection (see Fig. 4.1(b)).

4.2 BIASING AND OPERATION

Figure 4.2(a) illustrates the biasing scheme for the BICFET connected in the common-emitter circuit configuration. This circuit configuration is adopted in generating the device characteristics presented in this chapter. In this scheme, the input circuit is connected across the inversion-channel and emitter contacts, and the output circuit is connected across the active layer and emitter contacts. The emitter which is common to the input and output circuits is grounded while the active layer is biased at a negative potential relative to the emitter. In the common-emitter circuit configuration, a current flowing in the input circuit (I_i) will generate an amplified replica of this current in the output circuit (I_a).

Figure 4.2(b) illustrates the typical biasing scheme for the BICPT. The output circuit is connected across the active and emitter contacts by grounding the emitter and negatively biasing the active layer contact relative to ground. The input to the BICPT consists of an optical signal which is injected through the window in the emitter contact metal. This optical signal generates a current which is amplified to produce a current (I_a) in the output circuit. I_a is, therefore, an electrical replica of the optical signal.

4.3 DEVICE MODEL

4.3.1 Internal Potentials and Voltages

Figure 4.3 illustrates the equilibrium energy band representation of the BICFET/BICPT structure showing the energy levels and energy gaps within the structure. The collector layer of the ICT structure is not shown in this figure as it does not influence the operation of the BICFET/BICPT. In this figure, E_{ge} and E_{ga} are the energy gaps of the emitter and active layers, E_a is the dopant activation energy of the charge sheet layer, ΔE_{fe} and ΔE_{fa} are the Fermi energy levels in the emitter and active layers, ΔE_{fi} is the quasi-Fermi level in the inversion channel, and ΔE_c and ΔE_v are the conduction and valence band offsets between the InP and InGaAsP (λ=1.3 μm) layers. This figure highlights the role of the charge-sheet layer in bending the bands at the p-p heterointerface and the triangular potential well that is formed at this heterointerface. This triangular potential well provides an energetically favourable site for the accumulation of electrons.

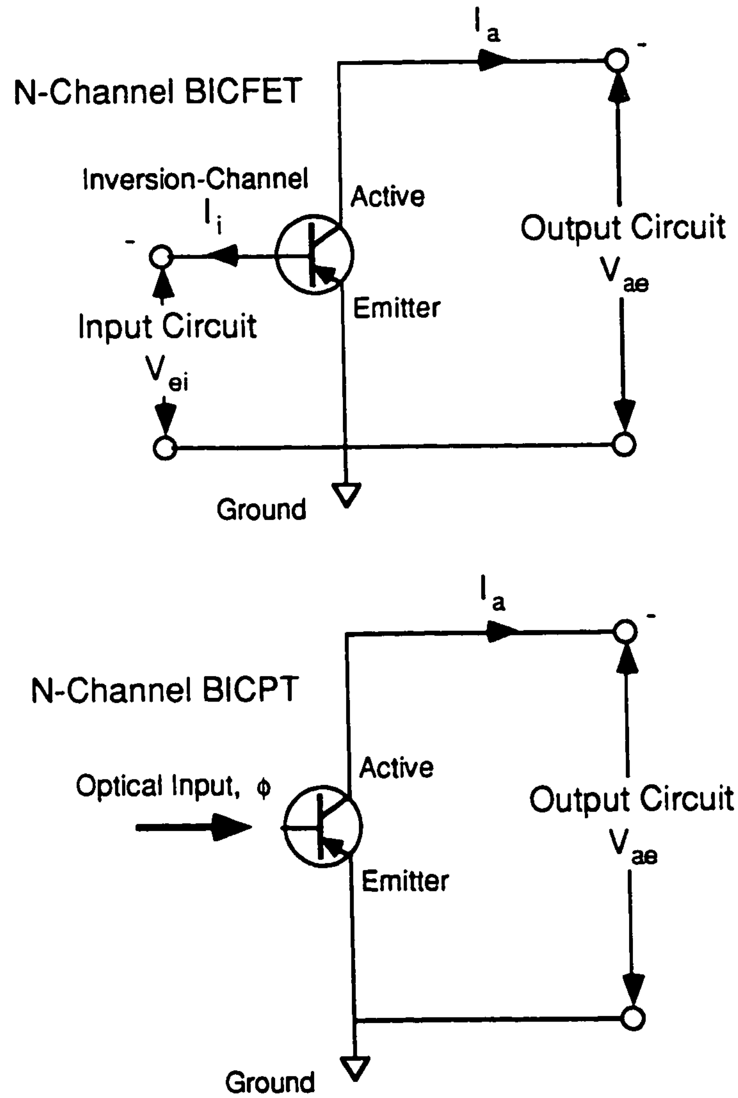


Figure 4.2: Typical biasing scheme for the n-channel a) BICFET and b) BICPT connected in the common-emitter circuit configuration.

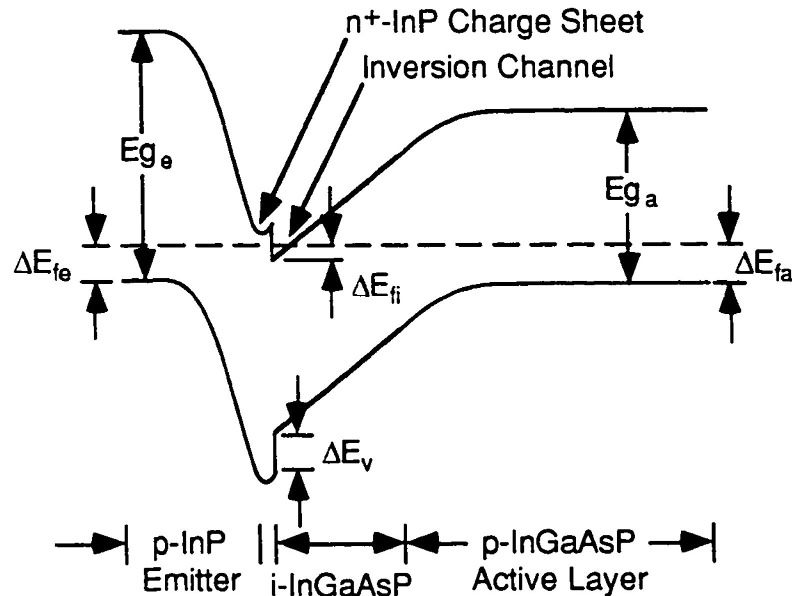


Figure 4.3: Equilibrium energy band representation of the n-channel InGaAsP-InP BICFET/BICPT showing the energy levels and energy gaps (see Figs. 4.4 and 4.5 also).

Figure 4.4 illustrates the BICFET/BICPT under bias conditions and identifies the emitter-inversion channel (e-i) and the active layer-inversion channel (a-i) junctions (see Fig. 4.3 for energy levels and energy gaps). ϕ_e, ϕ_u and ϕ_{a1} are the potentials of the emitter, undoped and active (closest to the undoped layer) layers. These potentials describe the extent of band bending at each of the p-n junctions within the structure. W_e and W_{a1} are the depletion layer widths associated with the emitter and active (closest to the undoped layer) layers, W_δ is the width of the charge sheet layer, and W_u is the width of the undoped layer. Finally V_{ei} and V_{ai} are the junction voltages of the e-i and a-i junctions. The junction voltages are defined such that they are positive when the junction is forward biased, negative when reverse biased and zero under thermal equilibrium. These conventions are consistent with those used in the model of the DOES (see Chap. 2). A comparison of the

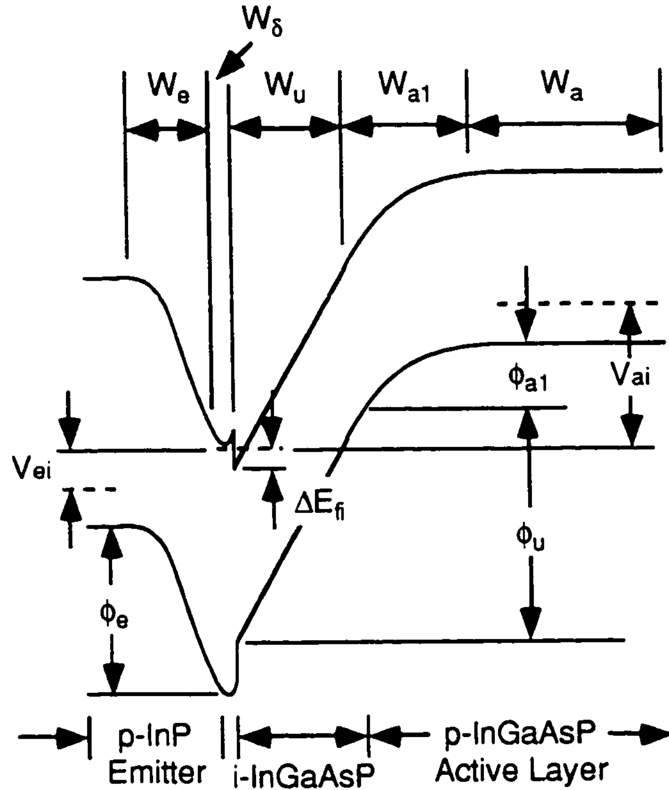


Figure 4.4: SATURATION-state energy band representation of the BICFET/BICPT showing the internal potentials, junction voltages and depletion layer thicknesses (see Figs. 4.3 and 4.5 also).

BICFET/BICPT and DOES energy band diagrams, Figs. 4.3 and 2.3, shows that the BICFET/BICPT structure is identical to the p-n-p section of the DOES structure. As a result, the device physics relating to the p-n-p section of the DOES can be directly applied to the BICFET/BICPT model. Expressions for the junction and terminal voltages are

$$V_{ei} = -\phi_e + \Delta E_{fi} - \Delta E_{fe} - \Delta E_c + E_{ge} \tag{4.1}$$

$$V_{ai} = \phi_e - \phi_u - \phi_{a1} + \Delta E_{fe} - \Delta E_{fa} - \Delta E_v \tag{4.2}$$

$$V_{ae} = \phi_e - \phi_u - \phi_{a1} + \Delta E_{fe} - \Delta E_{fa} - \Delta E_v \tag{4.3}$$

These terminal voltages are also defined such that the junction voltage is positive when forward biased, negative when reverse biased and zero under thermal equilibrium.

4.3.2 Charge Conservation and Fixed Charge Components

Charge conservation across the device structure is governed by solving Poisson's equation across the BICFET/BICPT structure to yield

$$Q_e - Q_\delta + Q_{ni} + Q_{a1} = 0 \tag{4.4}$$

where Q_e, Q_δ, Q_{ni} and Q_{a1} are the magnitudes of the fixed charge contributions in the emitter, charge sheet, inversion channel and active layers and bear units of charge per unit area (C/cm^2). Expressions for these charge components, derived in Chap. 2, are as follows:

$$Q_e = \left(2q\varepsilon_e N_e \phi_e\right)^{1/2} \tag{4.5}$$

$$Q_{a1} = \left(2q\varepsilon_a N_a \phi_{a1}\right)^{1/2} \tag{4.6}$$

$$Q_\delta = \frac{N_\delta W_\delta}{1+\exp\left[-\left(\Delta E_c - E_a - \Delta E_{fi}\right)/V_T\right]} \tag{4.7}$$

$$Q_{ni} \approx \frac{q m_n}{\pi \hbar^2}\left\{(E_2 - E_1) + V_T \ln\left(\frac{1+\exp\left[\left(E_1 - \Delta E_{fi}\right)/V_T\right]}{1+\exp\left[\left(E_2 - \Delta E_{fi}\right)/V_T\right]}\right)\right\} \tag{4.8}$$

4.3.3 Current Continuity and Current Density Components

Figure 4.5 illustrates the internal currents and terminal current flows associated with the device structure. J_{ne} and J_{ni} are the current density from electrons flowing (by diffusion) across the e-i and a-i junctions; J_{pe} is the net

hole current density flowing (by thermionic emission) across the emitter potential barrier; J_{tei} and J_{tai} are the net thermal recombination current densities associated with the e-i and a-i junctions; J_{oei} and J_{oai} are optically generated current densities; and J_e, J_i and J_a are the current densities at the emitter, inversion-channel and active-layer contacts. All of the current density components defined bear units of A/cm^2. The direction for positive current flow for each of these current density components is defined in Fig. 4.5. These definitions of the current density components are consistent with those defined for the DOES model of Chap. 2.

Current continuity for electrons across the structure, defined at point A (see Fig. 4.5) dictates that:

$$J_{ne} - J_{ni} + J_{tei} + J_{tai} - J_{oei} - J_{oai} + J_i = 0 \tag{4.9}$$

where

$$J_{ne} = q\frac{D_{ne}}{L_{ne}} n_{poe}\left\{\exp(V_{ei}/V_T) - 1\right\} \tag{4.10}$$

$$J_{pe} = A_e^*\left\{\exp(V_{ea}/V_T) - 1\right\} \tag{4.11}$$

$$J_{tei} = q\frac{n_{ie}}{2\tau_{re}} W_e\left\{\exp(V_{ei}/2V_T) - 1\right\} \tag{4.12}$$

$$J_{tai} = q\frac{n_{ia}}{2\tau_{ra}} (W_u + W_{a1})\left\{\exp(V_{ai}/2V_T) - 1\right\} \tag{4.13}$$

$$J_{oei} = q\eta_e\Phi\left\{\exp(-\alpha_e(t_e - W_e)) - \exp(-\alpha_e(t_e + t_\delta))\right\} \tag{4.14}$$

$$J_{oai} = q\eta_a\Phi\left\{\exp(-\alpha_a(t_e + t_\delta)) - \exp(-\alpha_a(t_e + t_\delta + t_u + W_{a1}))\right\} \tag{4.15}$$

Equations (4.10)–(4.15) have been derived in Chap. 2 and are repeated here for convenience.

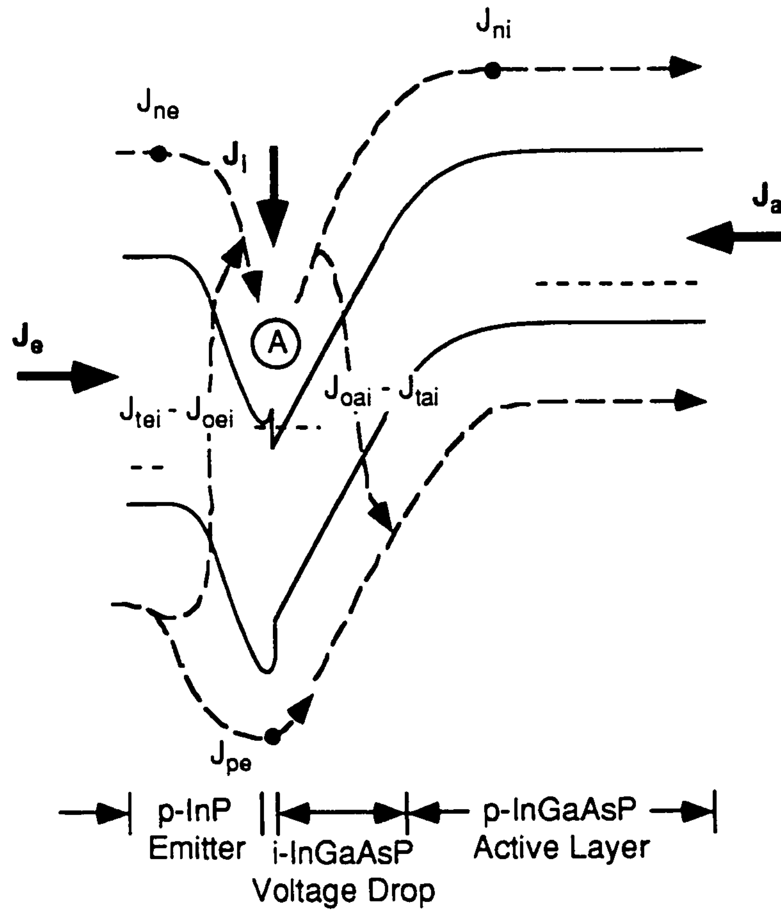


Figure 4.5: SATURATION-state energy band representation of the BICFET/BICPT showing the internal current components, terminal currents and direction of current flows (see Figs. 4.3 and 4.4 also).

Although most of the current components defined for the DOES are valid also for the BICFET/BICPT, a slight modification to J_{ni} (as defined in Eq. (2.19)) is required. In the DOES structure, minority carriers (electrons) which flow from the emitter into the active layer diffuse across the neutral region of the active layer enroute to the a-c junction. In the case of the BICFET/BICPT, carriers which arrive at the active layer will diffuse toward the active layer contact. Since the active layer contacts are placed on the periphery of the second mesa, the distance which the carriers must travel before they reach the

contact is much greater than their diffusion lengths. In this case, the long-diode approximation with $W_a >> L_{na}$, is used in Eq. 2.19 to yield [4]

$$J_{ni} = q\frac{D_{na}}{L_{na}}n_{p0a}(\mathrm{V})\left\{\exp(V_{ai}/V_T)-1\right\} \tag{4.16}$$

Terminal currents at the emitter and active layer contacts are defined as:

$$J_e = J_{ne} + J_{pe} + J_{tei} - J_{oei} \tag{4.17}$$

$$J_a = -\left(J_{ni} + J_{tai} - J_{oai} + J_{pe}\right) \tag{4.18}$$

By definition, a positive current represents hole current flowing into the contact. This definition is consistent with the convention for defining terminal current flows used in this thesis.

4.3.4 Solution to Device Equations

The computer model used to examine the operation of the BICFET and BICPT was written in the windows version of MATLAB [8]. This model requires the user to enter the physical parameters for the device structure as well as the external applied biases, V_{ae} and J_i for the BICFET and V_{ae} and Φ for the BICPT. Equations (4.1)–(4.17) are then solved to give provide a set of internal potentials ϕ_e, ϕ_u, ϕ_{a1} and ΔE_{fi} which satisfy the conditions for charge neutrality and current continuity across the structure. This set of internal potentials is then used to determine the charge, current and voltage components of the device at each bias point.

To solve for the output current density-voltage (J_a-V_{ae}) characteristic for the BICFET, the program is required to obtain solutions over a range of V_{ae} for a fixed J_i. At each bias point, the internal potentials are used to

determine J_a. To solve for the current-gain characteristics of the devices, V_{ae} is fixed while J_a is calculated at two closely spaced values of J_i . The current gain thus determined at a given value of J_i . To solve for the output current density-voltage (J_a-V_{ae}) characteristic for the BICPT, the program is required to obtain solutions over a range of V_{ae} for a fixed Φ. At each bias point, the internal potentials are used to determine J_a.

4.4 BICFET OUTPUT CURRENT-VOLTAGE CHARACTERISTIC

Figure 4.6 illustrates the output current density-voltage (J_a-V_{ae}) characteristic for the BICFET with J_i as the parametric variable. To provide insight into the operation of the device Fig. 4.7 shows the voltages across the e-i and a-i junctions as a function of V_{ae} for J_i = 500 A/cm^2. The physical parameters for the structure are listed in Table 4.1. The J_a-V_{ae} characteristic can be divided into three distinct states of operation: OFF, LINEAR, SATURATION.

OFF State

The OFF-state is defined as the portion of the J_a-V_{ae} curve where $0 > V_{ae} > -0.2$. In this region of operation V_{ae} is small and both the e-i and a-i junctions are forward biased. Under this condition, $\phi_e >> \phi_u + \phi_{a1}$, thus, all electrons injected into the inversion channel flow across the a-i junction to establish V_{ai}. Since there is very little electron flow across the e-i junction to induce a flow of holes from the emitter to the active layer, $J_a = J_i$. As V_{ae} decreases, V_{ai} remains constant while V_{ei} moves toward increasing forward bias.

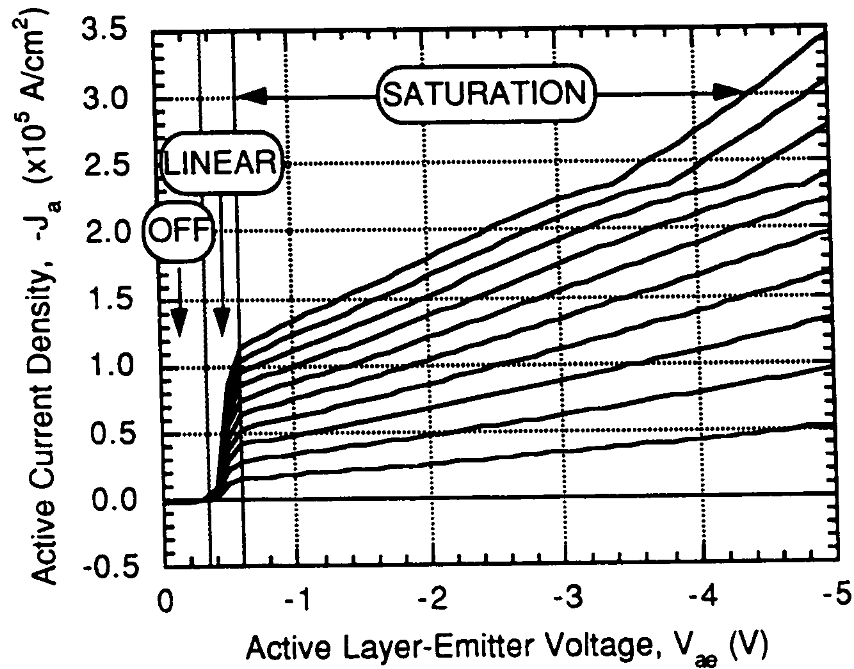


Figure 4.6: Common-emitter output characteristic (J_a-V_{ae}) of the BICFET with J_i as the parametric variable (J_i = 0 to -1000 A/cm^2 in -100 A/cm^2 increments).

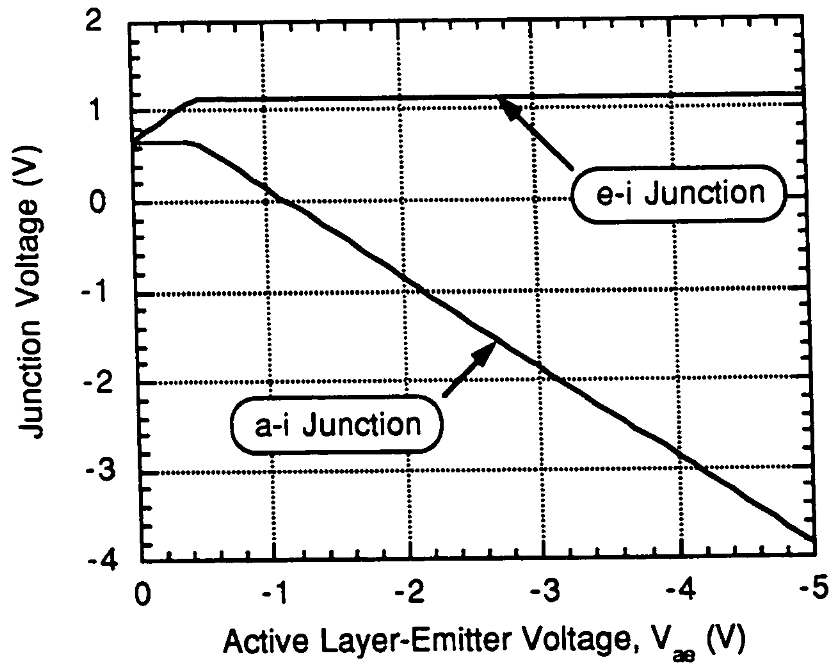


Figure 4.7: V_{ei} and V_{ai} as a function of V_{ae} for J_i = -500 A/cm^2.

***Table 4.1:** Device structure used in modeling of the BICFET and BICPT.*

Layer	Material	Layer Doping (cm^{-3})	Thickness (Å)
Emitter	p-InP	$5x10^{17}$	2000
Charge Sheet	n-InP	$5x10^{18}$	100
Undoped Active Layer	i-InGaAsP	-	-
Active Layer	p-InGaAsP	$1x10^{17}$	5000

LINEAR State

In the transition region of operation, where -0.2 V > V_{ae} > -0.6 V, the magnitudes of ϕ_e and $\phi_u + \phi_{a1}$ are comparable and thus, electrons injected into the inversion channel flow across both the a-i and the e-i junctions. When a portion of J_i flows across the e-i junction, a voltage V_{ei} is established and an induced hole current J_{pe} is generated. This hole flow from the emitter to the active layer is the main contributor to the increase of J_a in the transition region. As V_{ae} decreases further, ϕ_e decreases to the point where $\phi_e << \phi_u + \phi_{a1}$, a condition which forces all of J_i to flow across the e-i junction.

SATURATION State

In saturation, where V_{ae} > -0.6 V, $\phi_e << \phi_u + \phi_{a1}$ and all of J_i flows across the e-i junction. From this point on, V_{ei} is fixed at a bias that will support the flow of J_i. Since V_{ei} is fixed under saturation, the induced hole current J_{pe} and hence, J_a is expected to saturate. However, Fig. 4.6 shows J_a continues to increase with decreasing V_{ae}. This results because decreases in V_{ae} increases the reverse bias of the a-i junction and, hence, the density of

depleted charge across the active layer (Q_{a1}). To maintain charge neutrality across the structure, Q_e and Q_i decrease in a way that allows V_{ei} to remain constant. A reduction in Q_e causes a reduction in ϕ_e which results in an increase in J_{pe} and therefore, J_a.

4.5 BICFET/BICPT OUTPUT RESISTANCE

The output resistance (R) of the BICFET is defined as:

$$R = \frac{\Delta J_a}{\Delta V_{ae}} \qquad (4.19)$$

where ΔJ_a is a change in J_a that corresponds to the change ΔV_{ae} in V_{ae} about a fixed V_{ae}.

In circuit applications, a high output resistance is desired as this determines the transistor's ability to drive high impedance loads. Equation (4.19) shows that the output resistance is governed by the drop of V_{ae} across the e-i and a-i junctions. A higher output resistance is achieved if relatively more of V_{ae} is dropped across the a-i junction as opposed to the e-i junction. This is influenced by the relative doping concentrations of the layers. A high output resistance can be achieved by maximizing the layer doping ratios N_e/N_a and N_δ/N_a. This can be achieved by designing a structure with a very lightly doped active layer.

4.6 BICFET CURRENT GAIN CHARACTERISTIC

Figure 4.8 illustrates the current gain characteristic for the BICFET with parameters of Table 4.1. The current gain (G) is figure of merit which describes the ability of the transistor to amplify an input current and is defined as

$$G = \frac{\Delta J_a}{\Delta J_i} \tag{4.20}$$

where ΔJ_a is a change in J_a that corresponds to the change ΔJ_i in J_i about a fixed J_i.

Two distinctive regions of operation are distinguishable from the curve of Fig. 4.8. In the region between points a and b, the current gain increases rapidly with decreasing J_a and therefore, with decreasing J_i. This results because recombination current transport dominates, when J_i is small, reducing the efficiency of J_i in biasing ϕ_e. As J_i decreases, diffusion current transport increases its dominance and the efficiency of J_i in biasing ϕ_e increases. This results in an increase in the current gain. In the region of operation between points b and c, the current gain decreases with J_a and hence, J_i decreases. In this region of operation, as J_i increases, the accumulation of carriers in the inversion channel also increases. This results in an increase in ΔE_{fi} which reduces the effect of J_i in biasing ϕ_e.

Figures 4.9(a–c) show the effect of structural parameters on the maximum current gain (G_{max}) of the BICFET. The figures show that G_{max} increases as the emitter and active layer doping increases. On the other hand, G_{max} is shown to decrease with increases in the charge sheet doping.

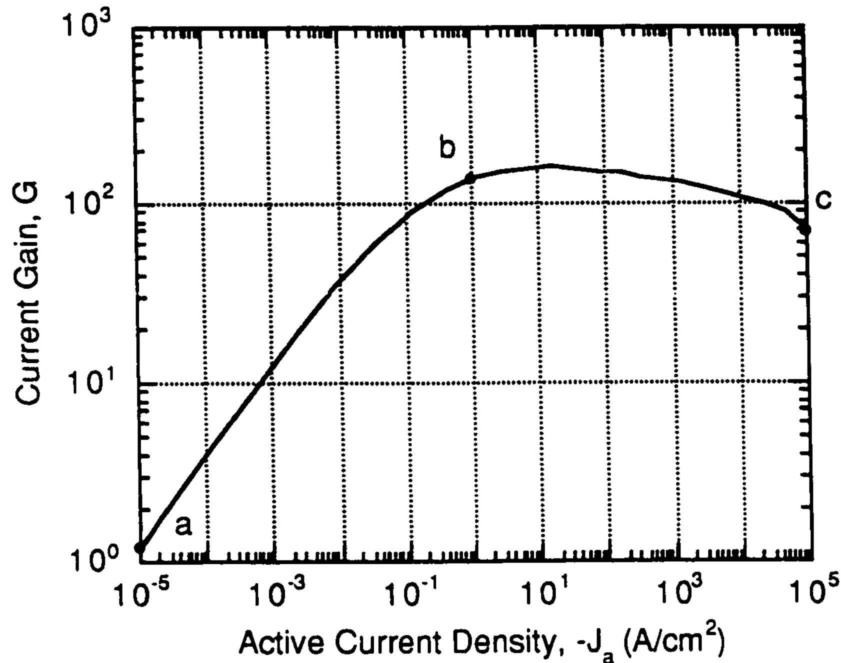
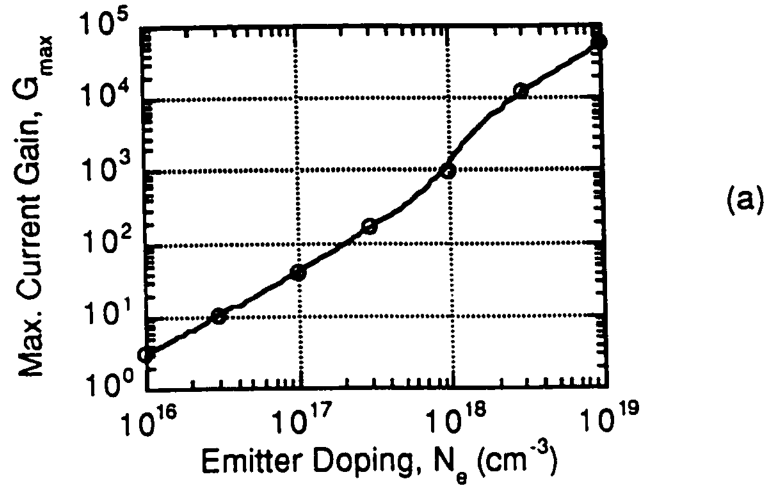


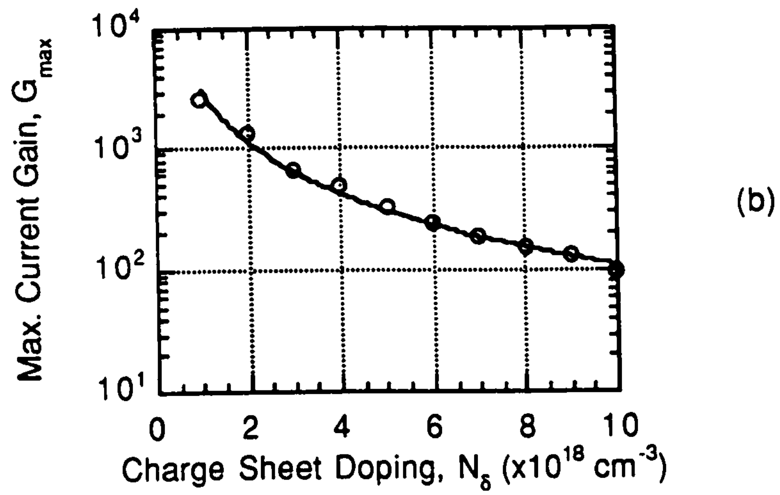
Figure 4.8: Current gain characteristics of the BICFET.

The two figures of merit, G_{max} and R, are clearly influenced by the selection of the doping in the emitter, charge sheet and active layers. A high doping in the emitter maximizes both G_{max} and R. The trade-off between G_{max} and R, in relation to the overall circuit performance, has to be considered when selecting the doping of the charge-sheet and active layers.

4.7 BICPT OUTPUT CURRENT-VOLTAGE CHARACTERISTIC

Figure 4.10 illustrates the J_a-V_{ae} characteristic of the BICPT with incident light level (at λ = 1.3 μm) as the parametric variable. In the BICPT, light incident on the device is absorbed by the active layer and generates electron hole pairs. Electron-hole pairs which are formed within the depletion region of the active layer are swept apart and contribute to the





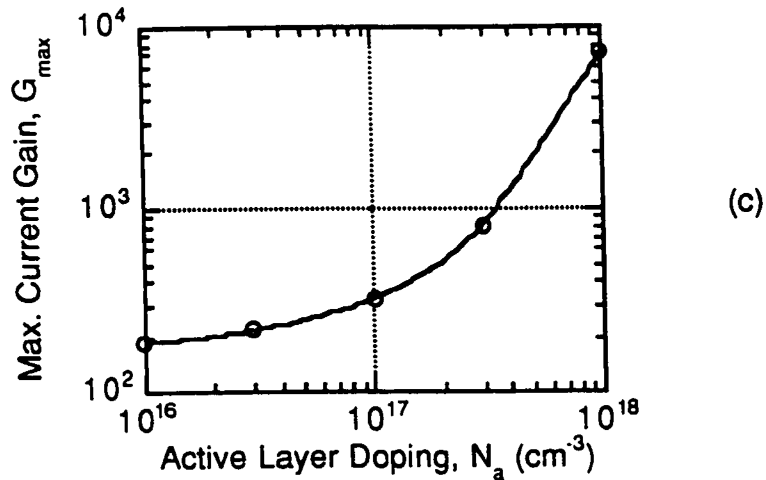


Figure 4.9: Maximum current gain of the BICFET as a function of the a) emitter, b) charge sheet and c) active layer doping.

internal current densities of the structure. The photogenerated electrons flow across the e-i junction to the emitter, and act in a manner similar to the electrons injected by the inversion-channel contact of the BICFET. The photogenerated holes flow across the active layer, across the a-c junction and out the collector. The operation of the BICPT is in principle identical to that of the BICFET, except that in the BICPT optically generated electrons are injected into the structure to influence the biasing conditions of the device, whereas in the BICFET, the electrons are injected via the inversion channel contact.

Figure 4.11 provides further insight into device operation by showing the behaviour of V_{ei} and V_{ai} with V_{ae} at ϕ = 100 cm^{-2}. In the BICPT light that is absorbed by the a-i depletion region generates electron-hole pairs. The photogenerated holes flow out of the active contact. The photogenerated electrons flow across the e-i junction and out of the emitter contact. This flow of electrons establishes V_{ei} and in turn induces J_{pe} to flow from the emitter to the active layer. Since the current component J_{pe} is the amplified version of the optically generated electron current, the resulting output current J_a is an amplified version of the optically generated current.

As shown in Figure 4.10, the output characteristics of the BICPT closely resembles that of the BICFET. The states of operation, OFF, LINEAR and SATURATION are clearly visible in the figure. The physics of operation of the BICPT is identical to that of the BICFET. As a result, the dependence of the output resistance and current gain on the doping of the emitter, charge sheet and active layers also follows that of the BICFET.

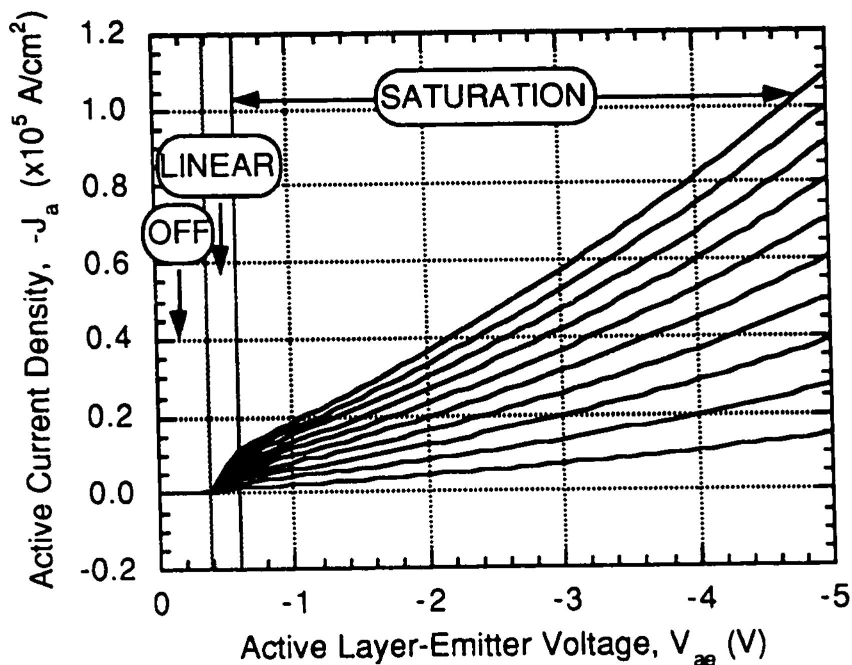


Figure 4.10: J_a-V_{ae} *characteristic of the BICPT with* Φ *as the parametric variable* (Φ = 0 *to* 1000 cm^{-2} *in* 100 cm^{-2} *increments).*

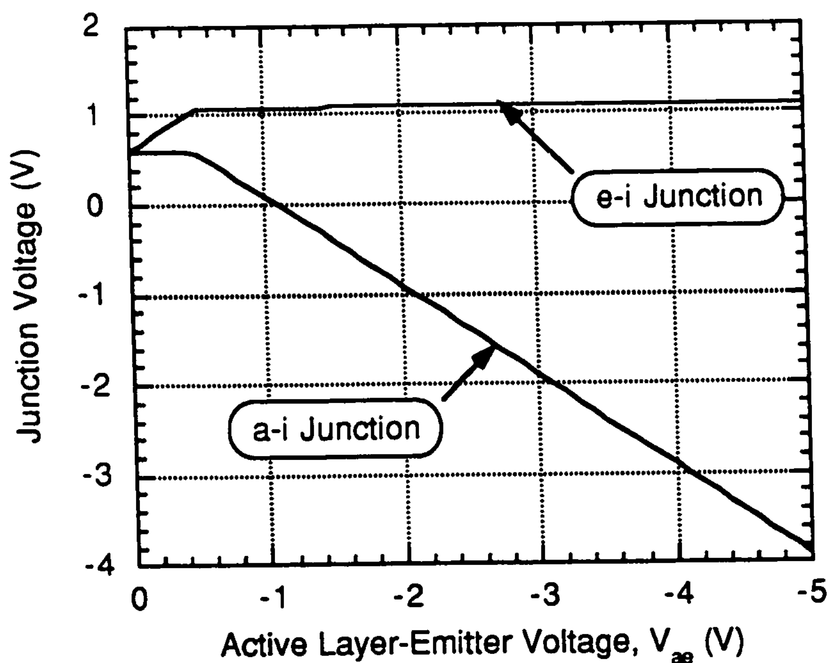


Figure 4.11: V_{ei} *and* V_{ai} *as a function of* V_{ae} *for* Φ = 100 cm^{-2}.

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CHAPTER 5

FABRICATION OF 4-TERMINAL N-CHANNEL InGaAsP-InP BASED ICT DEVICES

This chapter presents the fabrication sequence and processes for producing self-aligned 4-terminal n-channel InGaAsP-InP based inversion channel technology (ICT) devices. The chapter begins with a presentation of the four device structures grown for this work and results from physical analysis of these structures. This is followed by the presentation of the device fabrication sequence which provides an overview of the process steps involved. Finally, a detailed description and discussion of each process in the fabrication sequence is provided.

Most of device fabrication was carried out in the clean-room facilities at the Centre for Electro-photonic Materials and Devices (CEMD), McMaster University. The dielectric for device passivation was deposited at the Institute for Microstructural Sciences (IMS), National Research Council of Canada (NRCC).

5.1 DEVICE STRUCTURE

Figure 5.1 illustrates a detailed schematic cross section of a 4-terminal ICT device fabricated in this work including the nine semiconductor layers that were grown to form the device structure. The composition, thicknesses and doping concentrations for each of the layers that make up the four device structures are listed Table 5.1. The charge-sheet spacer, emitter contact and buffer layers are included in the structure to facilitate device growth and fabrication, and to improve the performance of the devices.

The four device structures listed in Table 5.1 were grown at Bell Northern Research (BNR) by Metal-Organic Chemical Vapour Deposition (MOCVD) [1]. secondary-ion mass spectroscopy (SIMS), x-ray crystal diffraction and photoluminescence spectroscopy (PL) were performed on the structures following their growth. Figure 5.2 illustrates the SIMS profile of the four structures. The Zn and Si profiles identify the regions of p- and n-type doping within the structure while the In+Ga profile shows the composition of the layers and identifies the InGaAs, InGaAsP and InP layers within the structure. These results show good agreement between the requested structures and the grown structures. The charge sheet layer is identified by the peak in the Si profile at a depth range of 2000–3000 Å. The limited depth resolution of the SIMS profile does not provide an accurate representation of the charge sheet thickness or doping concentration.

Photoluminescence spectra of the InGaAsP (λ=1.3 μm) layer in structure S1603 reveals a the peak at 1332.5 nm with a full width half maximum (FWHM) of 69.7 nm (see Fig. 5.3). This PL spectra is representative of all the four structures that were grown. Table 5.2 provides a summary of the PL results for S1601,

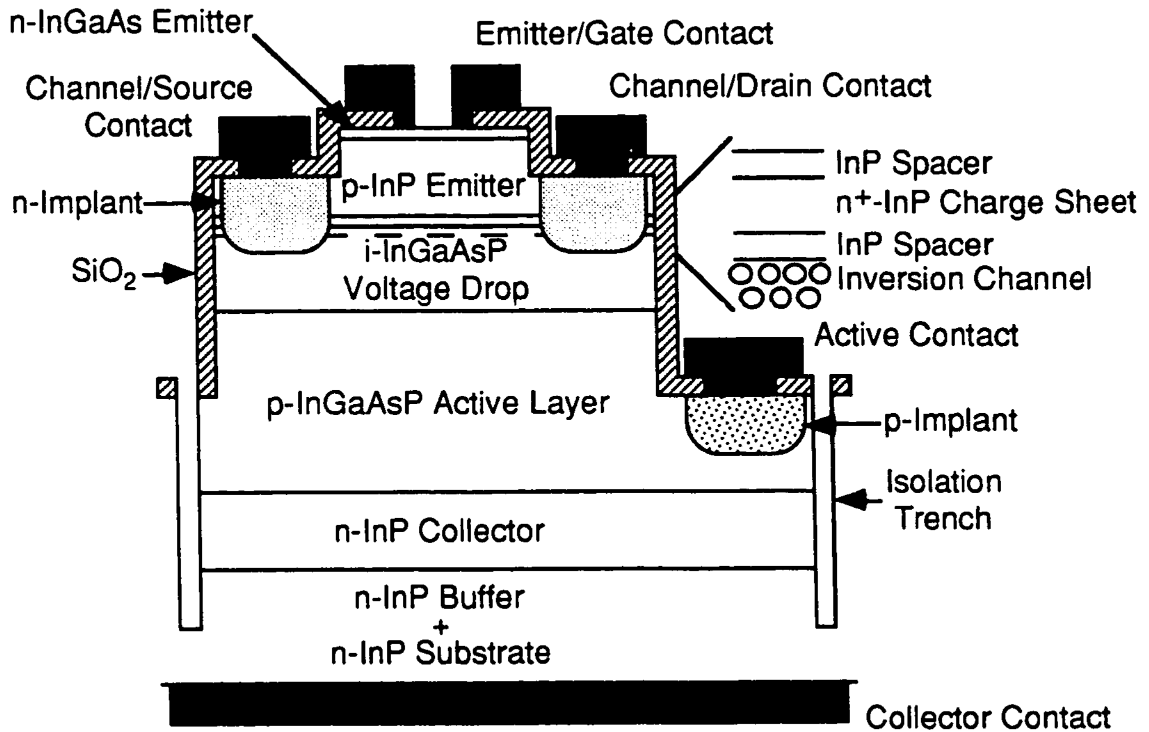

Figure 5.1: Schematic cross-sectional view of a 4-terminal n-channel InGaAsP-InP based inversion channel technology (ICT) device.

S1602, S1603 and S1604, and shows an average peak wavelength for the InGaAsP layers is 1332.5 ± 5.8 nm and an averaged FWHM of 72.6 ± 2.2 nm. These results indicate that the structures will absorb strongly, incident light with wavelengths that are shorter than 1.3 μm.

X-ray crystal diffraction results for structure S1603 is shown in Fig. 5.4. The more intense peak results from the InP layers which is lattice matched to the substrate, and the secondary peak results from the InGaAsP layer. The -238 arc sec. shift between the two peaks indicates that the quaternary layers are under compressive strain. The average difference in angle between the bulk and InGaAsP layers for all structures is -239 ± 44 arc sec. (see Table 5.3).

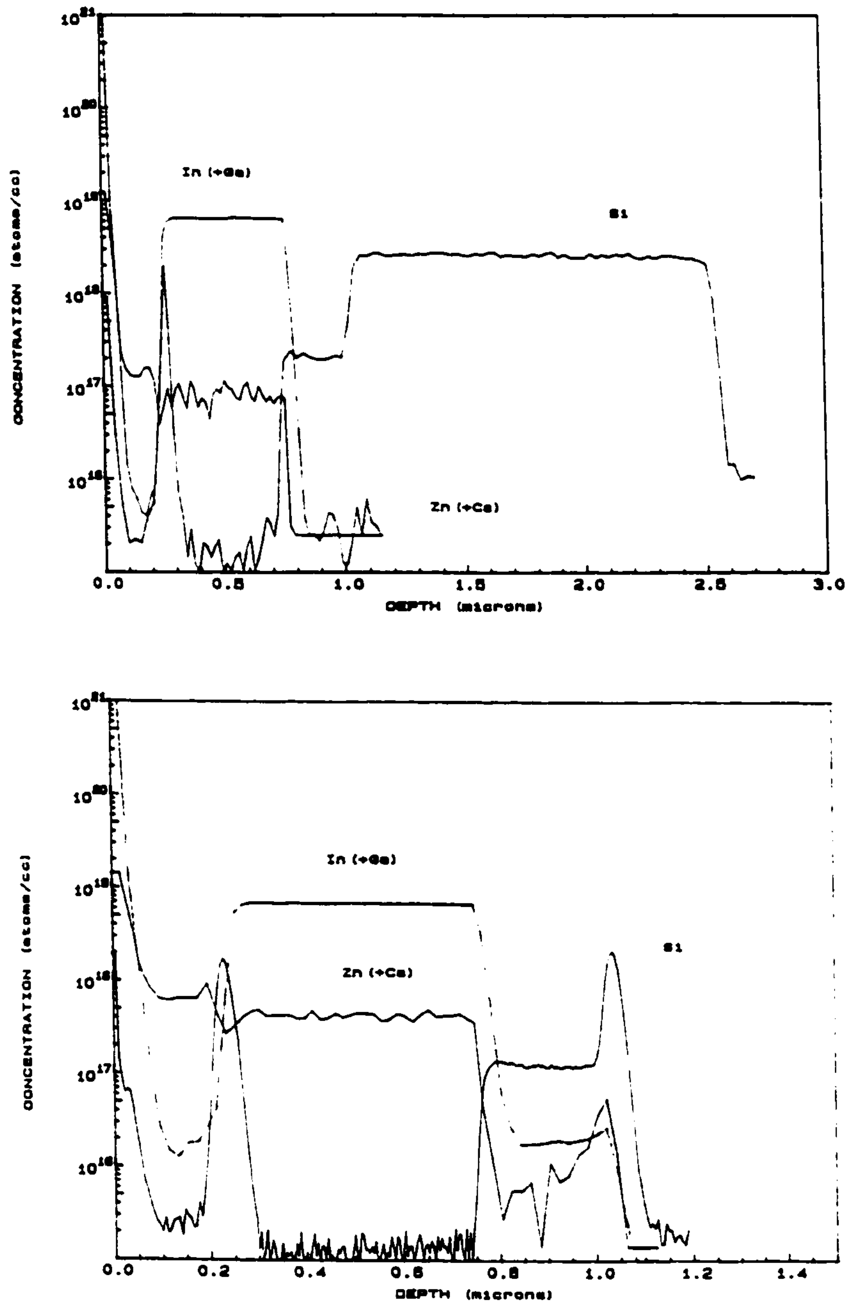

Figure 5.2: Secondary ion mass spectroscopy (SIMS) depth profile of structures a) S1601 and b) 1602.

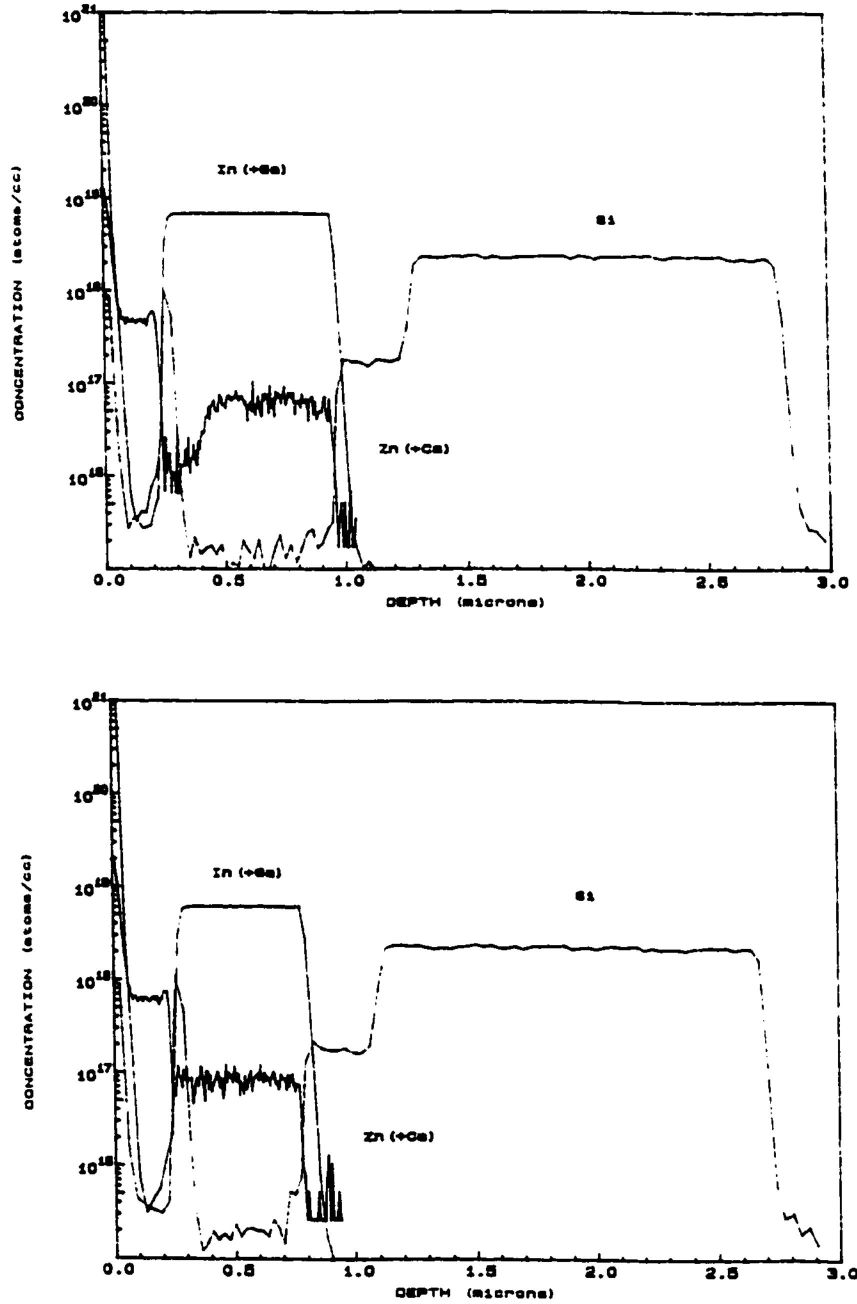

Figure 5.2: SIMS depth profiles of structures c) S1603 and d) S1604.

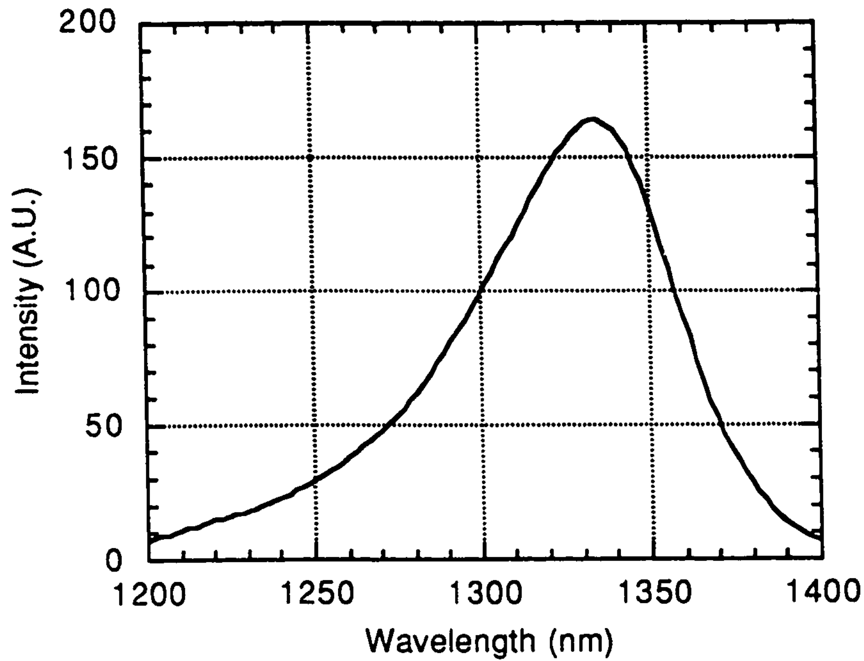

Figure 5.3: Photoluminescence spectra of the InGaAsP (λ=1.3μm) active layer of structure 1603.

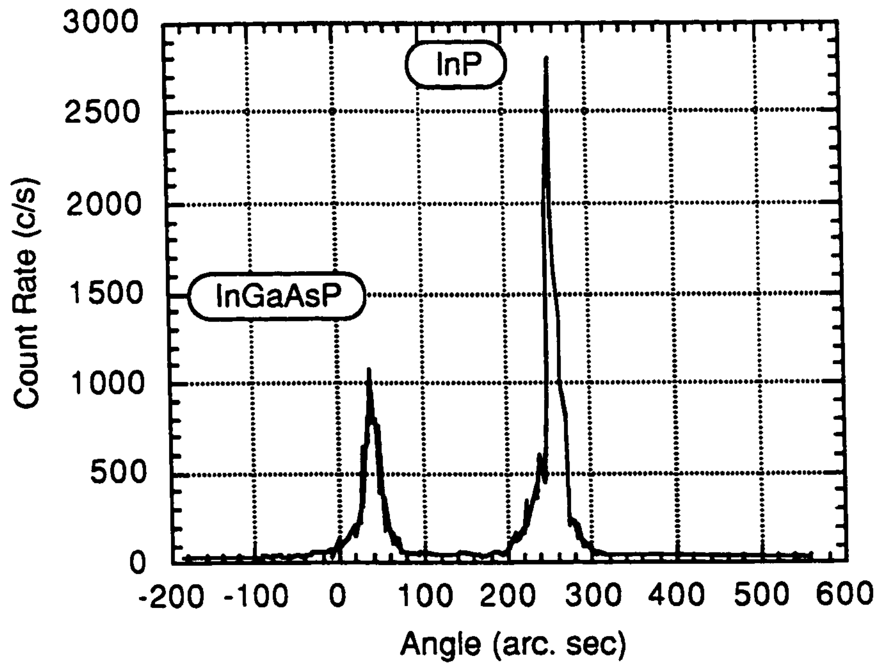

Figure 5.4: Double crystal x-ray diffraction spectra of structure S1603.

***Table 5.1:** Description, composition, thickness and doping concentrations of the layers in structures S1601, S1602, S1603 and S1604.*

Layer Description & Composition	Layer Thickness (Å)	Device Structure Doping Concentration (cm^{-3})			
		S1601	S1602	S1603	S1604
Emitter Contact InGaAs	200	Zn: $1x10^{19}$	Zn: $1x10^{19}$	Zn: $1x10^{19}$	Zn: $1x10^{19}$
Emitter InP	2000	Zn: $1x10^{17}$	Zn: $5x10^{17}$	Zn: $5x10^{17}$	Zn: $5x10^{17}$
Spacer InP	50	i	i	i	i
Charge Sheet InP	100	Si: $5x10^{18}$	Si: $5x10^{18}$	Si: $5x10^{18}$	Si: $5x10^{18}$
Spacer InP	50	i	i	i	i
Voltage Drop InGaAsP (λ=1.3μm)	2000	N/A	N/A	Zn: $6x10^{15}$	N/A
Active InGaAsP (λ=1.3μm)	5000	Zn: $1x10^{17}$	Zn: $5x10^{17}$	Zn: $1x10^{17}$	Zn: $1x10^{17}$
Collector InP	2000	Si: $2x10^{17}$	Si: $2x10^{17}$	Si: $2x10^{17}$	Si: $2x10^{17}$
Buffer InP	1.5 μm	Si: $2x10^{18}$	Si $2x10^{18}$	Si: $2x10^{18}$	N/A
Substrate InP	500 μm	S: $7x10^{18}$	S: $7x10^{18}$	S: $7x10^{18}$	S: $7x10^{18}$

***Table 5.2:** Summary of photoluminescence and double crystal x-ray diffraction for structures S1601, S1602, S1603 and S1604.*

Structure	Photoluminescence		X-Ray
	Peak (nm)	FWHM (nm)	Δ(InGaAsP-InP) (arc sec.)
S1601	1326.5	72.4	-200
S1602	1331.1	73.2	-217
S1603	1332.0	69.7	-238
S1604	1340.5	74.9	-300
Average	1332.5 ± 5.8	72.6 ± 2.2	-239 ± 44

5.2 FABRICATION SEQUENCE

Figures 5.5–5.9 illustrate the fabrication sequence used in this project for producing 4-terminal n-channel InGaAsP-InP based inversion-channel technology (ICT) devices. This sequence is presented to provide an overall understanding of fabrication process and therefore, does not include a detailed description of each step. Details of each processing step are presented in Sects. 5.3–5.12.

The fabrication process begins by cleaving 12 x 12 mm^2 samples from the 500 mm diameter InP wafer on which the device structures were grown. These 12 x 12 mm^2 samples were cleaned with a combination of solvents, ultra-violet (UV) ozone and acids to produce a surface that is free of contaminants, Fig. 5.5(a). A self-aligned SiO_2 mask is formed by first depositing 6 kÅ of SiO_2 onto the sample, Fig. 5.5(b). Metal lift-off is used to pattern Al features (3000 Å thick), in the shape of the first mesa, on the SiO_2 (mask level: MES1), Fig 5.5(c). The SiO_2 is

reactive ion etched (RIE) with a CF_4-based plasma, Fig. 5.5(d). The Al mask is removed to reveal SiO_2 patterns with very vertical sidewall profiles, Fig. 5.5(e). These SiO_2 features will be used to mask the RIE of the first mesa and second ion-implantation, thus, ensuring self-alignment between the first mesa and the second ion-implantation is achieved. This *dummy gate* method for achieving self-alignment was developed as an alternative to the refractory gate method.

The first mesa is etched by $CH_4/H_2/Ar$-based RIE to form mesas with vertical sidewalls. The etch depth of this mesa is crucial and etching must be terminated 1000 Å above the inversion channel, Fig. 5.6(a). Precise etch control is achieved with an in-situ quadrupole mass spectrometer which provides real-time identification of the layers being etched. Following the etch, a conformal coating of SiO_2 (2500 Å thick) is applied to the structure by plasma-enhanced chemical vapour deposition (PECVD), Fig. 5.6(b). This SiO_2 will form the mask for the isolation trench and second mesa etch, and serve as the sidewall passivation for the n-channel ion-implantation.

Isolation trenches around each device are formed to provide electrical isolation between devices. This is achieved by first patterning photoresist (mask level: ISO) and transferring the pattern into the SiO_2 by wet chemical etching, Fig. 5.6(c). The patterned SiO_2 is used to mask the $CH_4/H_2/Ar$-based RIE which removes approximately 2 μm of semiconductor and terminates within the buffer layer of the structure, Fig. 5.6(d). The remaining SiO_2 is again patterned (mask level: MES2) and wet chemical etched to mask the second mesa etch, Fig. 5.6(e). The second mesa is also etch by $CH_4/H_2/Ar$-based RIE and terminates half-way into the active layer, Fig. 5.7(a).

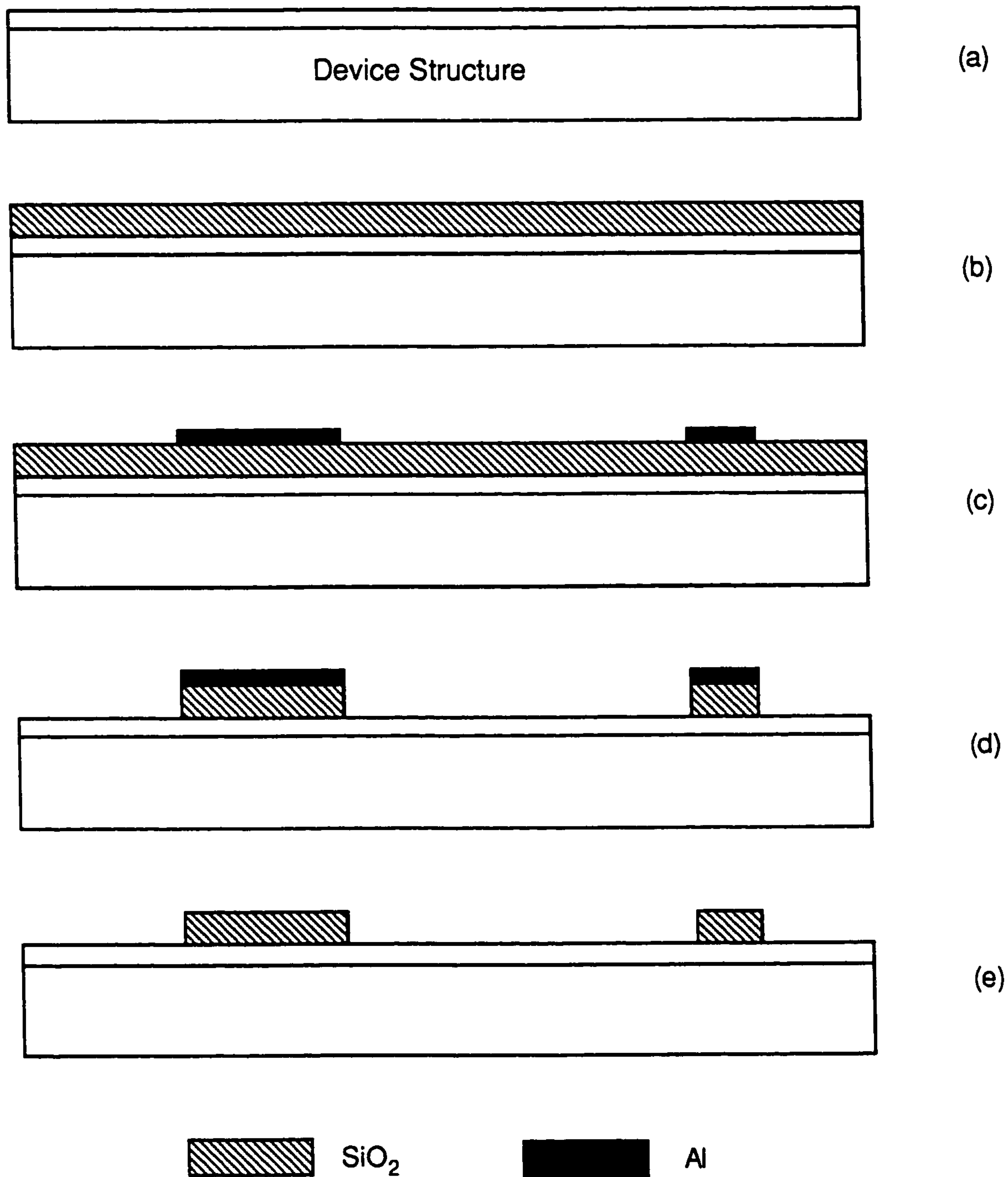

Figure 5.5: Fabrication sequence for 4-terminal n-channel InGaAsP-InP based ICT devices. Mask levels: (c) MES1.

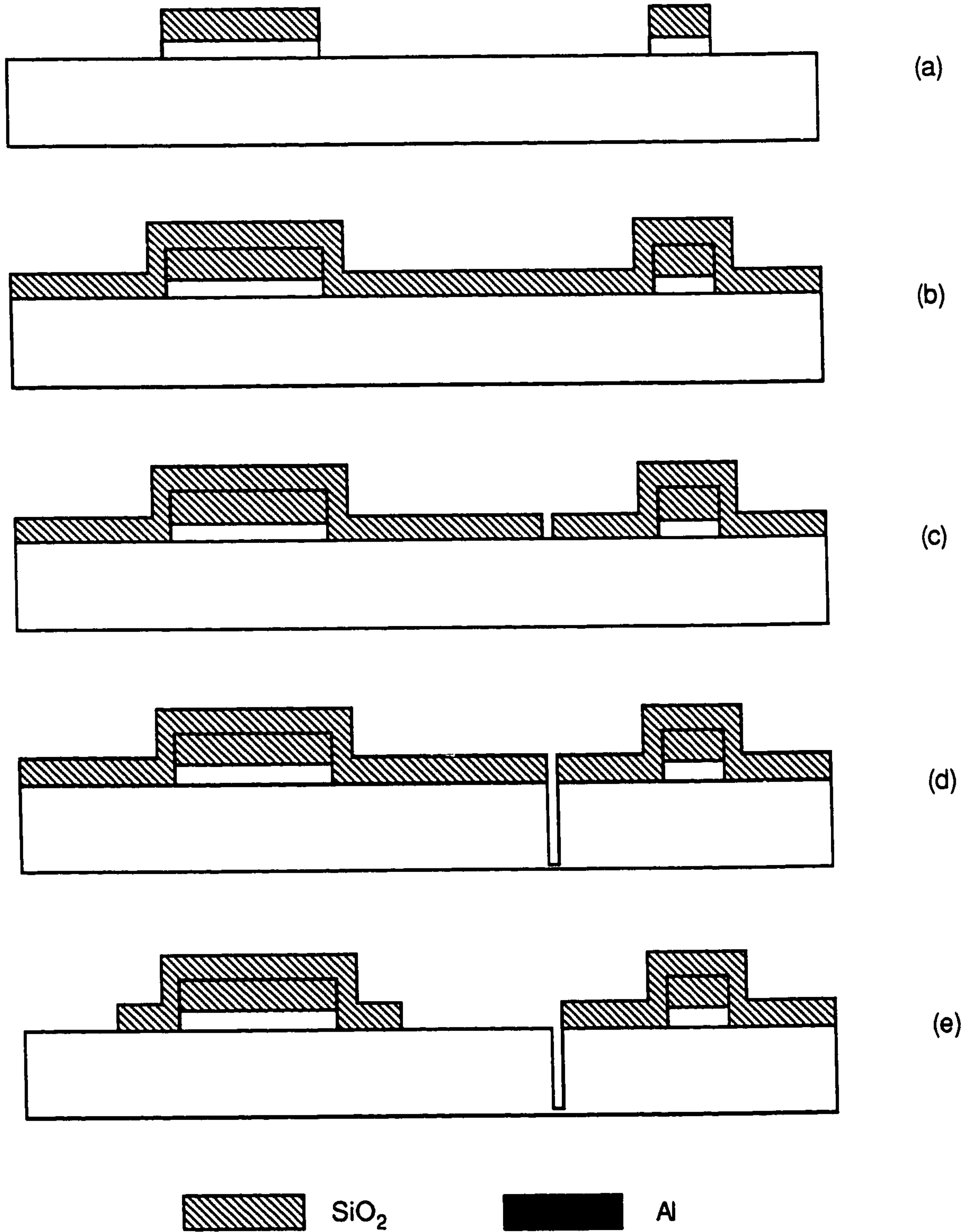

***Figure 5.6:** Fabrication sequence for 4-terminal n-channel InGaAsP-InP based ICT devices. Mask levels: (c) ISO, (e) MES2.*

The first ion-implantation is used to form low-resistance contacts to the active layer. The implantation is masked by patterning a 2 μm thick photoresist (mask level: IIM3), Fig. 5.7(b). Mg ions are then implanted uniformly across the sample surface, Fig. 5.7(c). Following the implantation, the hardened photoresist is removed with an oxygen plasma, Fig. 5.7(d).

The second ion-implantation is used to form contacts to the inversion channel. This requires the SiO_2 above the second mesa to be removed while leaving behind the self-aligned SiO_2 and the SiO_2 sidewall passivation layers. This is achieved by anisotropic CF_4-based RIE of the SiO_2, Fig. 5.8(a). Since all the SiO_2 is exposed to the etchant, precise control of the etch is required to ensure that the SiO_2 on top of mesa 2 is removed while leaving behind enough SiO_2 on the sidewalls and tops of mesa 1 to mask the ion-implantation. The structures are then patterned with photoresist to mask the ion-implantation, Fig. 5.8(b) (mask level: IIM3). Masking of the second ion-implantation is achieved by a combination of the self-aligned SiO_2, sidewall SiO_2 and photoresist. The structure is implanted with Se at 200 °C to produce a localized region of n-type doping, Fig. 5.8(c). Following the implantation, the photoresist is stripped with an oxygen plasma, Fig. 5.8(d). The photoresist is extremely cross-linked after this elevated temperature implant and complete removal is difficult. All SiO_2 is then removed from the surface by an etch in HF:DI solution followed by a thorough clean with solvents and acids, Fig. 5.9(a). The ion-implantation is activated by enclosing the samples in a graphite boat, which was designed and constructed for this project, and annealing them in a rapid thermal annealer (RTA) at 700 °C for 1 second.

A passivating oxide (thickness 2000 Å) is deposited with plasma enhanced chemical vapour deposition, Fig. 5.9(b). This layer of SiO_2 was deposited at the

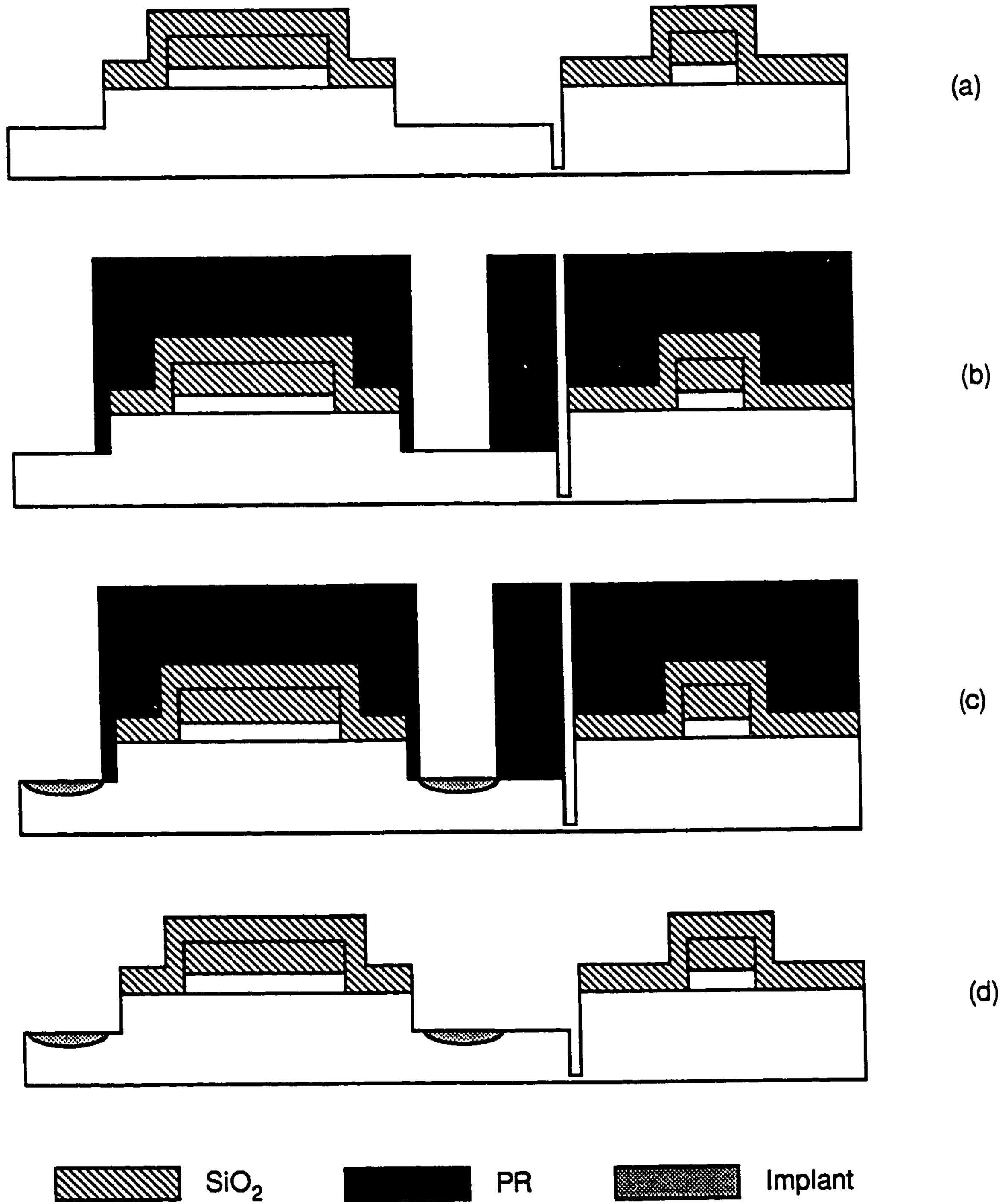

Figure 5.7: Fabrication sequence for 4-terminal n-channel InGaAsP-InP based ICT devices. Mask levels: (b) IIM3.

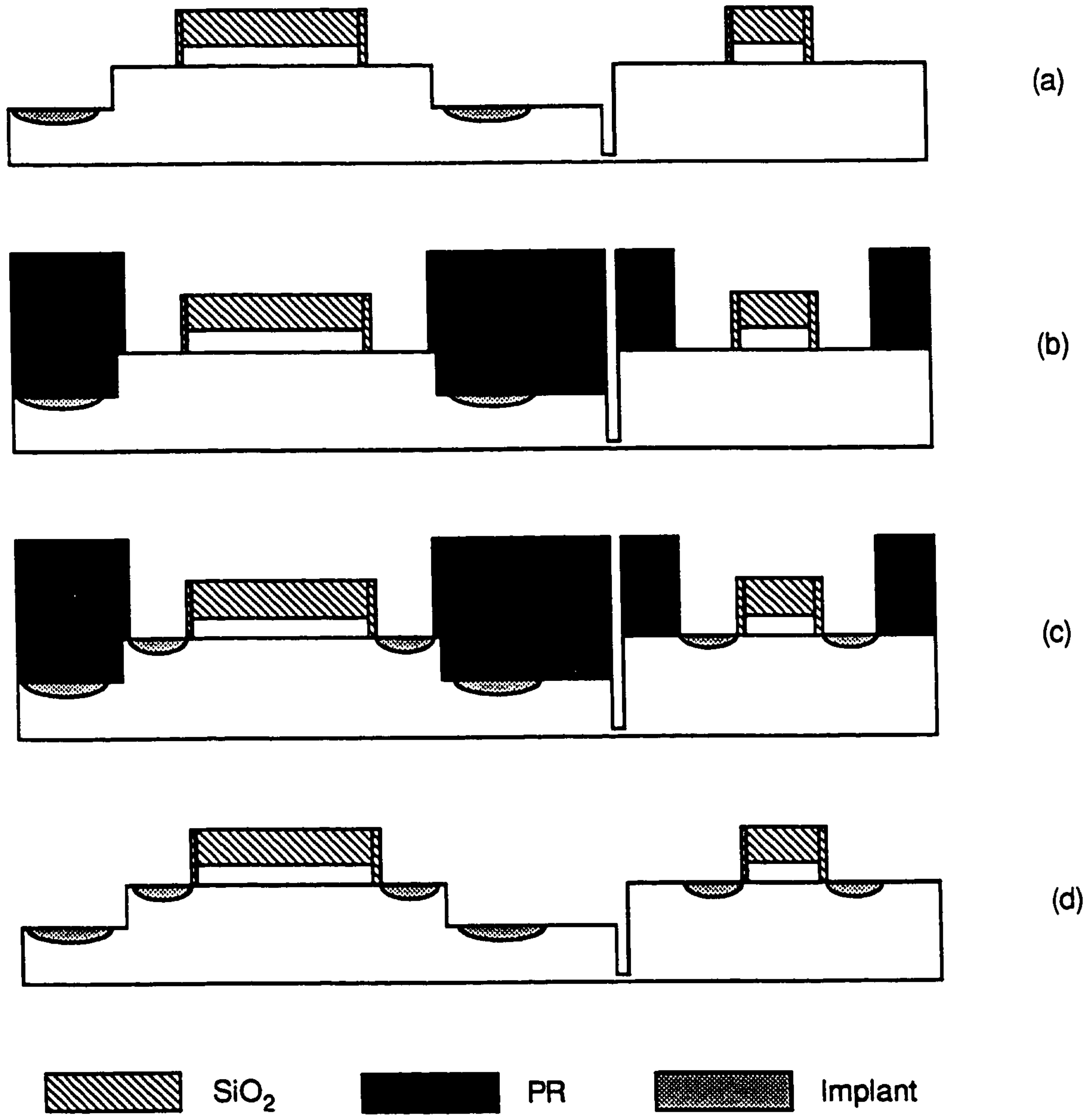

***Figure 5.8:** Fabrication sequence for 4-terminal n-channel InGaAsP-InP based ICT devices. Mask levels: (b) IIM1.*

Institute for Microstructural Sciences, National Research Council of Canada. Via holes were then patterned and wet chemically etched in the SiO_2 to allow electrical contact to each layer in the structure (mask level: VIA), Fig. 5.9(c). Since the mesas which form the structure possess vertical sidewalls, a tilt-stage metallization technology was developed to ensure a continuous coverage of metal from the tops of the mesas, along the sides and to the base of the mesa. This required first patterning with mask levels MET1, MET2 and MET3, depositing the topside metal with the tilt stage and then lifting off the metal, Fig. 5.9(d). A second patterning for lift-off is performed with mask levels MET1 and MET2. For the second metal deposition, the samples rotated 90°, relative to their mounting position in the previous deposition, to expose the other two sides of the mesa to the metallization. A lift-off of the metal is again performed after deposition, Fig. 5.9(d). Finally, a blanket metallization of Ni/Ge/Au is applied on the backside of the samples, Fig. 5.9(e).

The contacts are rapid thermal annealed at 400 °C for 20 seconds to realize their low resistivity nature. Following the anneal, a blanket metallization of Ti/Pt/Au is applied to the backside of the sample to build-up and passivate the annealed Ni/Ge/Au metal surface, Fig. 5.9(e).

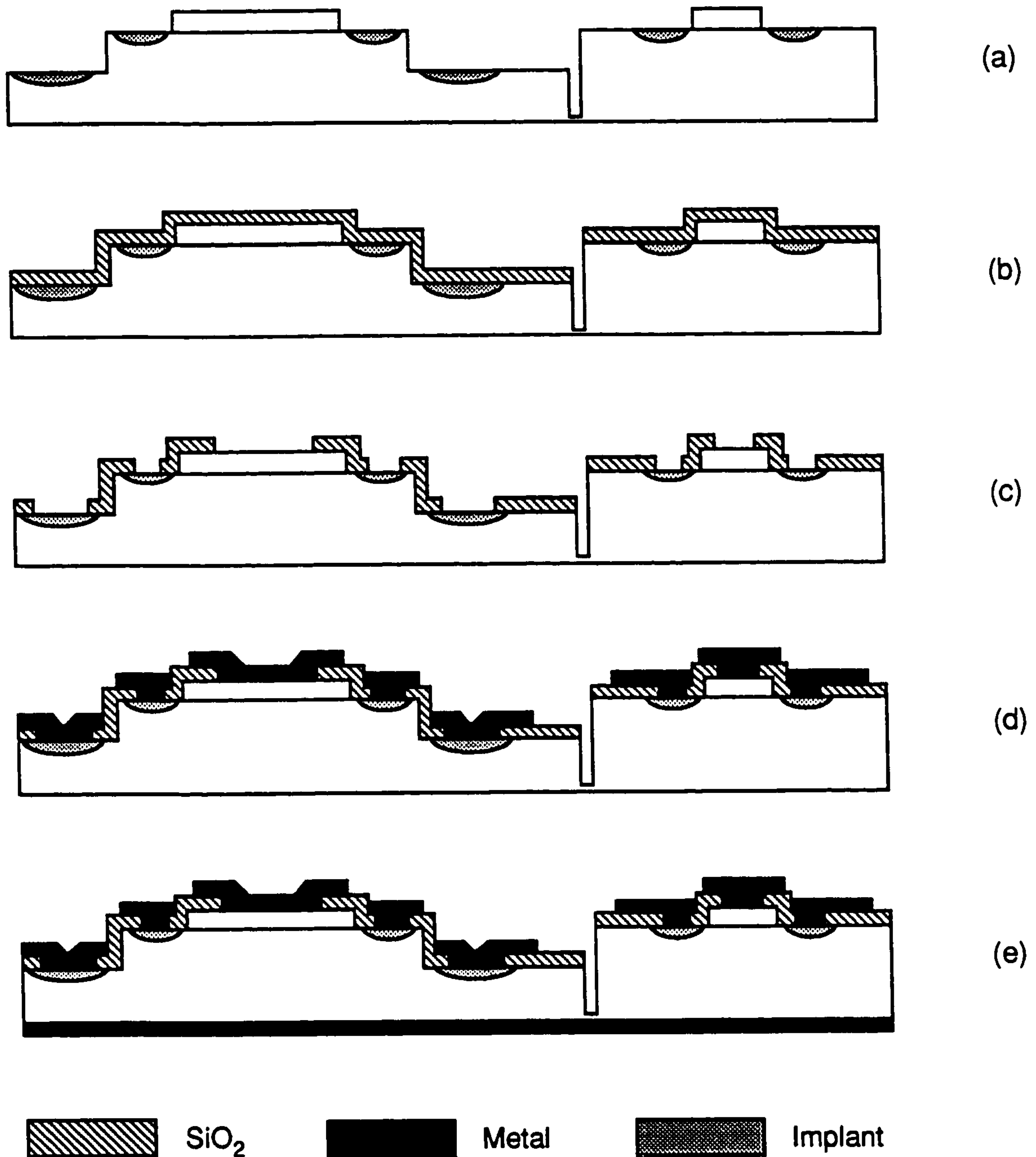

Figure 5.9: Fabrication sequence for 4-terminal ICT devices. Mask levels: (c) VIA, (d) MET1, MET2 and MET3.

5.3 PHOTOLITHOGRAPHIC MASK SET

To fabricate the 4-T ICT device, a total of eleven photolithographic steps involving nine mask levels are required. In photolithography, patterns imprinted on a chrome mask plate are transferred to a photoresist coating by first exposing the photoresist with ultra-violet (UV) light through the chrome-coated mask and then developing the photoresist to form the desired patterns. The mask set allows six distinct styles of devices of various sizes to be fabricated (see Fig. 5.10). Also present on the mask sets are transmission line measurement (TLM) structures for characterizing the contact resistance and sheet resistance of the layers within the structure [2] (see Fig. 5.11). The mask levels corresponding to each photolithographic step of the fabrication sequence have been shown in Fig. 5.5–5.9. Table 5.3 lists some critical parameters for each level of the mask set. The critical dimension represents the smallest feature to be transferred from the mask plate to the photoresist. The alignment tolerance represents the maximum allowable misalignment between the mask plate and substrate. For this mask set, the critical dimensions and alignment tolerances were designed to ensure a high yield of devices.

Mask to substrate alignment is performed by superimposing a set of alignment marks on the mask over ones which have been patterned into the sample. For the 4T-ICT mask set, two sets of marks are included for mask alignment. The first set consists of a rectangular frame that runs along the edges of the sample and provides coarse registration of the sample to the mask plate. The second set of alignment marks is based on a Maltese cross design shown in Fig. 5.12. In this scheme, a Maltese cross pattern, Figs. 5.12(c) and (d), is etched

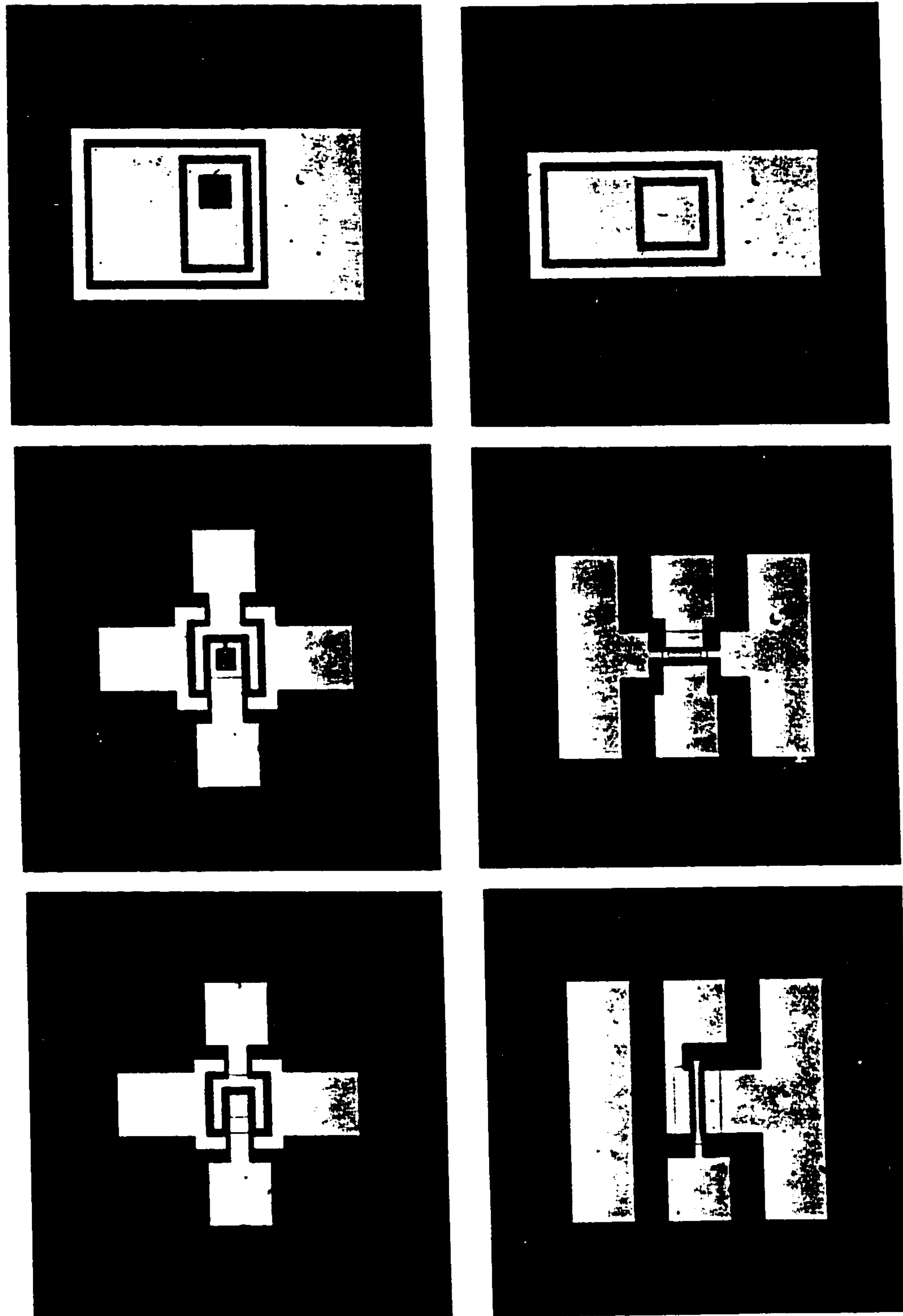

Figure 5.10: Photographs showing the top views of the 6 styles of devices fabricated in this project.

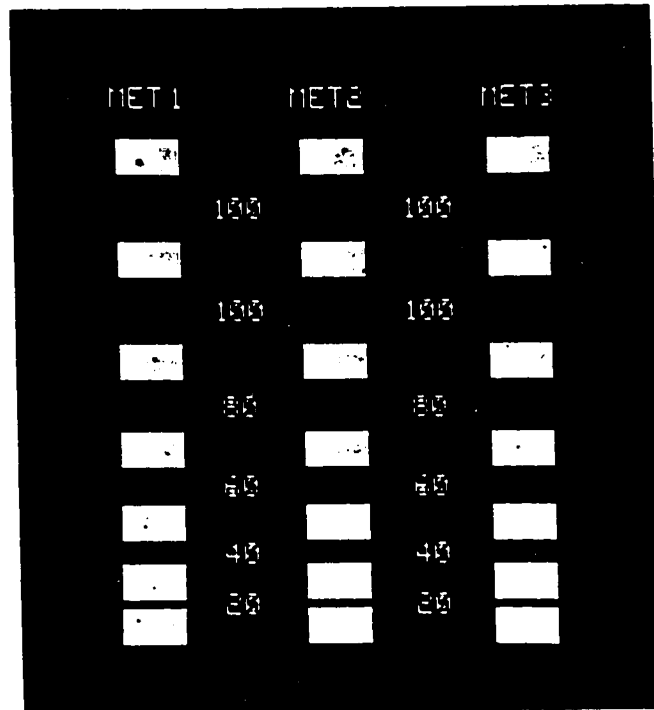

Figure 5.11: Photographs of transmission line measurement (TLM) structures fabricated on each wafer for evaluating contact resistance between metal and semiconductor.

into the sample during the patterning of the first mesa to serve as the base pattern to which all subsequent masks levels are aligned. The cross pattern, Figs. 5.12(a) and (b), located on the chrome mask represents the top pattern which must be positioned accurately over the base pattern. Proper positional alignment of substrate to mask requires that good registration of all six alignment marks, which are distributed across the 12 x 12 mm^2 sample, be achieved simultaneously. This Maltese cross alignment scheme allows for both medium and fine alignment to be accomplished using the same alignment features [3].

Also included on each mask level is a set of resolution targets which can be used to evaluate the quality of photolithography (see Fig. 5.13). In general one

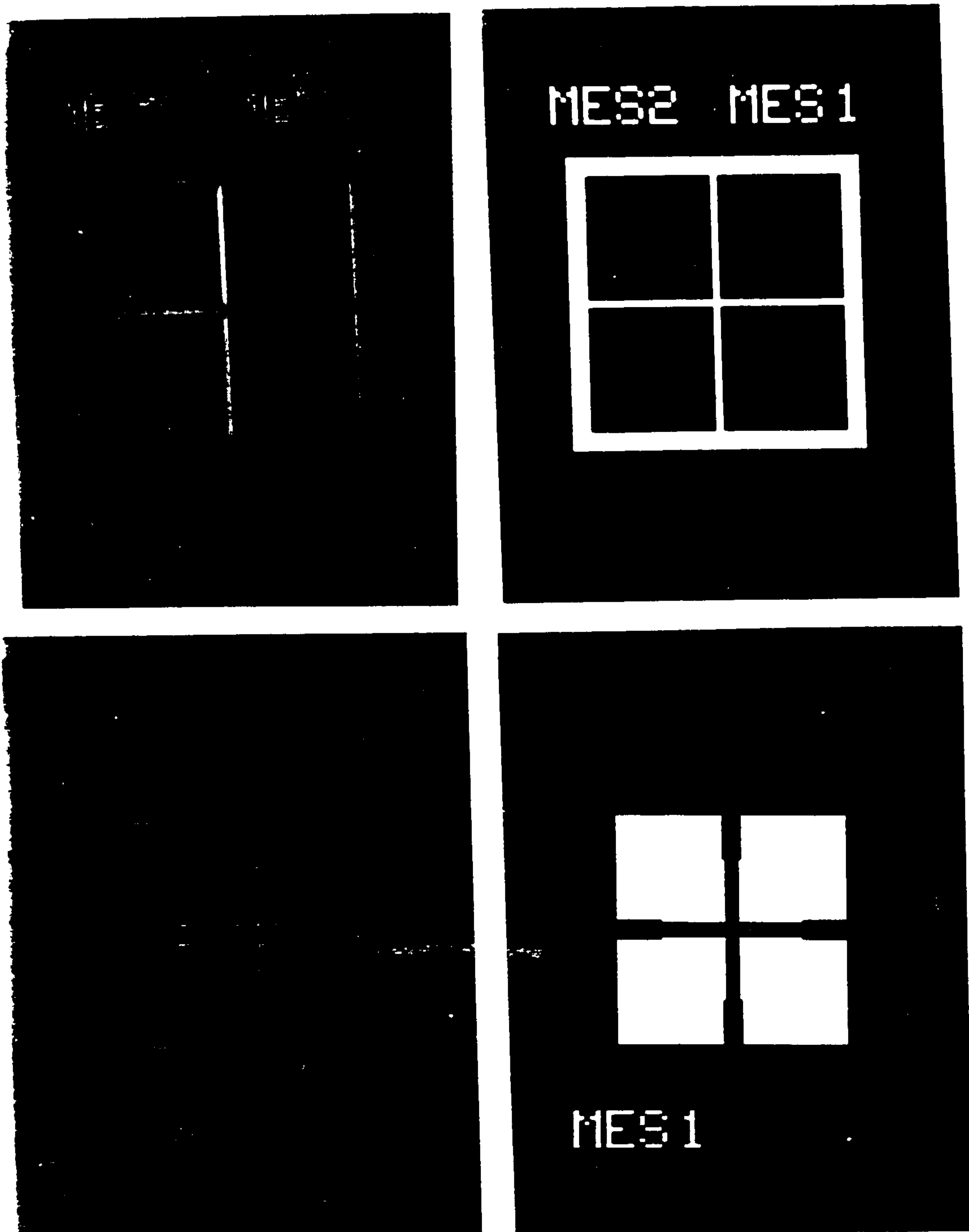

Figure 5.12: Photographs of the alignment marks used for mask to substrate alignments. a) and b) show cross pattern, c) and d) show Maltese cross pattern.

Table 5.3: *Specifications of each mask levels in the self-aligned 4-terminal ICT mask set.*

Mask Level	Field Type	Critical Dimension (μm)	Alignment Tolerance (μm)
1) Mesa 1	DF or LF	5	N/A
2) Isolation	DF	10	10
3) Mesa 2	LF	20	3
4) Ion-Imp3	DF	10	5
5) Ion-Imp1	DF	10	3
6) Via	DF	3	1
7) Met1	DF	5	3
8) Met2	DF	10	5
9) Met3	DF	20	5
10) Ion-Imp2	DF	20	5

can confirm that photoresist is adequately developed when areas which had been exposed to the UV light have cleared and the smallest features of the resolution targets are clearly defined.

Each mask level is designed and laid out with a computer aided design tool ICED32 [4] in the light-field format. Each mask level was designed to fit in a 18 x 18 mm^2 area allowing five of them to be tiled onto the active area of a 100 x 100 mm^2 mask plate. This reduces the total number of mask plates from 10 to 2 and minimizes the cost of mask production. These mask levels were patterned by e-beam on a chrome coated quartz substrate to a critical dimension (CD) of 1 μm ± 0.1 μm. Light- and dark-field copies of the mask were fabricated from the master on chrome coated soda-lime substrates with a CD of 1.0 μm ± 0.3 μm [5].

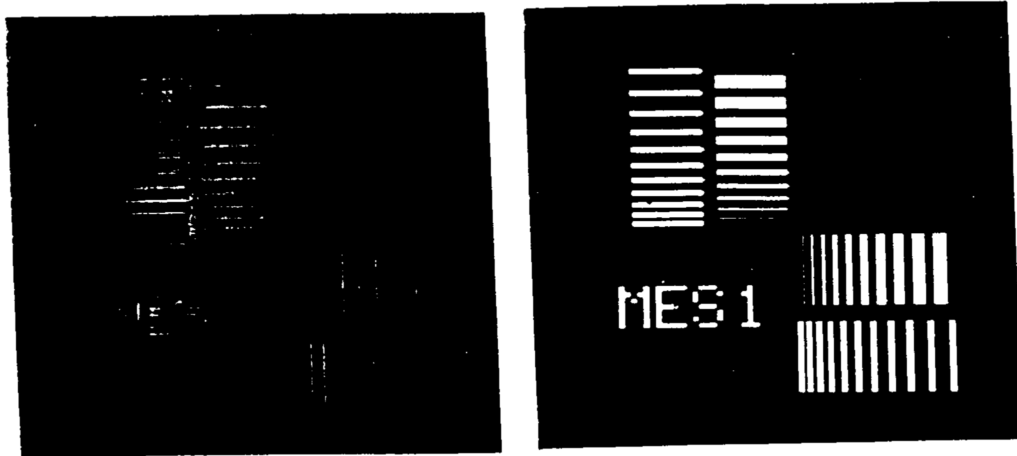

Figure 5.13: Photographs of resolution targets included on each mask level to evaluate quality of photolithography.

5.4 CLEAVING AND CLEANING OF SUBSTRATES

The 12 x 12 mm^2 samples processed for this thesis were cut using the scribe and cleave method. Scribing is performed by placing a short scratch with a diamond tipped instrument along the edge of the semiconductor on the polished side of the wafer. The scribe which is typically 5–10 μm deep, interrupts the normal surface tension of a crystal creating a high stress zone in the surface which will serve to initiate the cleave [6]. Cleaving is achieved by placing the wafer face down in a wafer box (Fluoroware) and applying light pressure to the backside of the wafer at the location of the scribe. This causes the semiconductor to break along a crystal plane.

The samples are cleaned by first spraying their surface with a jet of N_2 at 30 psi to remove weakly bonded particles. They are then immersed for 15

minutes in each of the following solvents: trichloroethylene or trichloroethane, 2-propanol, acetone and 2-propanol. These solvents are heated on a hot-plate to a temperature of 80 °C. Following the final soak in 2-propanol, the samples are removed and immediately blown off with N_2 to dry the surface. No subsequent rinse in DI is required as the 2-propanol evaporates rapidly. The samples are then placed in a UV Ozone system for 10 minutes to generate a 10–30 Å thick layer of an InP based oxide [7]. This layer of oxide is removed by etching in an HF:DI (1:1) solution for 30 seconds and rinsed in de-ionized water (DI) [8]. These cleaning procedures produce semiconductor surfaces that are low in oxygen and carbon contamination [9].

5.5 PATTERNING OF CVD-SiO_2

The SiO_2 used in this work is patterned by applying a coating of photoresist on the SiO_2, patterning the photoresist, etching the SiO_2 and then stripping the photoresist to leave behind patterned SiO_2 structures [10].

The sample surfaces are dusted off with N_2 and placed on the chuck of the spinner (Headway Research). Shipley photoresist primer is applied with a syringe via a 0.45 µm point-of-use filter, allowed to sit on the sample for 15 seconds and then spun at 5000 rpm for 30 sec. After a pause of 15 seconds, Shipley 1400-26 photoresist is applied with a syringe through a 0.45 µm point-of-use filter. The resist is applied so that it completely covers the entire sample surface and is held on the sample by surface tension. A 30 second pause allows the resist to settle and air bubbles in the photoresist to rise to the top before the sample is spun at 5000 rpm for 30 sec. The photoresist coated samples are air dried at room temperature for 5 minutes before being soft-baked at 110 °C for 90

seconds on a hot plate. This soft-bake removes a majority of the solvents from the photoresist coating and ensures that normal exposure speeds are achieved.

Mask alignment and exposure of the photoresist coated wafer is performed with a Karl Suss MJB3 mask aligner. When the chrome mask is satisfactorily aligned to the sample, vacuum contact between the sample and mask is established [11]. The vacuum contact exerts pressure between the mask plate and the sample to ensure that high-resolution pattern transfers from the mask to the underlying photoresist. The samples are then overexposed with an optical energy of 40 mJ/cm^2 at 365 nm, developed by immersion in a solution of Shipley 351 developer:DI (1:5) for 45 seconds, rinsed in DI and dried with an N_2 spray. The quality of this patterning is evaluated by examining the resolution targets which are transferred to the photoresist layer. The samples are then hardbaked at 130 °C for 2 minutes on a hotplate to stabilize the photoresist for use as an etch mask.

The CVD SiO_2 is etched in a buffered-oxide etchant (10:1 BOE)* because photoresist is compatible with this etchant [12]. At 20 °C, this solution etches CVD SiO_2 at a rate of between 1000 to 1500 Å/min. When etching SiO_2, visual observation and alpha-step measurements of the etched oxide are taken every 30 seconds to determine etch rate and total etch depth. The samples are over-etched by approximately 1000 Å to ensure that the surface is completely free of SiO_2. Following the etch, the samples are thoroughly rinse in DI for 10 minutes to ensure a clean surface that is free of any etchant. Any residual etchant will react and degrade the semiconductor surface [13].

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* 10:1 BOE is a solution consisting of 10 parts NH_4F(40%) to 1 part HF (by volume).

After the etching is completed, the photoresist is removed by immersing the samples in J.T. Baker-PRS1000 solution, which is heated on a hotplate to 80 °C, for 10 minutes. Then, the samples are thoroughly rinsed in DI for 10 min and N_2 dried. Baker PRS1000 is a very mild photoresist stripper formulation which does not noticeably etch III-V semiconductors. This formulation is only effective at stripping photoresist that has been hardbaked at less than 140 °C. In the initial stages of the project, EMT 130TX was used to strip the hardbaked photoresist. This aggressive stripper formulation etches III-V semiconductors at a rate of 10–20 Å/min and should not be used in III-V device processing.

5.6 PHOTORESIST MASK FOR ION-IMPLANTATION

To localize the first and second ion-implantation, a thick photoresist mask is used. This mask is prepared by following the process similar to that described in Sect. 5.5 except for the following changes: In this process, Shipley 1400-33 photoresist is spun at 4000 rpm for 30 seconds forming a coating which is 2.2 μm thick. This resist is exposed with an energy of 200 mJ/cm^2 at 365 nm. Hard-baking is performed by placing the sample on a hotplate stabilized at 150 °C. The hotplate temperature is ramped from 150 to 210 °C at a rate of 120 °C/hr. After a total 40 minutes of hard baking, the hotplate is turned off and the samples are slowly cooled to room temperature. This process produces a resist coating that is stabilized for the implantation temperatures of up to 200 °C.

Following the ion-implantation process, the resist must be stripped from the sample surface. This is a difficult process as ion-implanted photoresist is very tightly cross-linked by exposure to high temperatures and radiation. The photoresist is removed by etching it in an oxygen based plasma, generated with

the process conditions of Table 5.4, in a Technics 800 RIE system. The total etch time employed is one that will etch a total depth of 1.5 times the photoresist thickness. This overetch ensures the surface is free of photoresist. The oxygen plasma does not etch the underlying semiconductor although it leaves a very thin film of InP based oxide on the surface. This oxide is removed by immersing the samples in HF:DI (1:10) for 3 sec.

5.7 PATTERNING FOR METAL LIFT-OFF AND LIFT-OFF

Metal lift-off process is used to pattern metal films onto the device structure. In this process, the photoresist is applied to the sample with the methodology described in Section 5.5. The samples are then soft-baked on a hot plate at 80 °C for 90 seconds and exposed with an optical energy of 80 mJ/cm^2 at 365 nm. Following exposure, the samples are soaked in an aromatic solvent to harden the top 2000 Å of the photoresist. Two equivalent processes have been used: The first involves soaking the sample in chlorobenzene for 6 minutes, followed by a 15 second dip in trichlorotrifluoroethane. The sample is then blown dry with N_2 and baked at 80 °C for 45 seconds to ensure both the chlorobenzene and the trichlorotrifluoroethane have been completely removed from the sample surface. An alternate process involves a 7 minute soak in toluene after which the sample is blown dry with N_2 and baked at 80 °C for 45 seconds. The samples are then developed in 1:5 Shipley 351 developer:DI for approximately 2 minutes, thoroughly rinsed in DI and N_2 dried. This resist patterning process will form an undercut profile in the resist layer as shown in Fig. 5.14(a). This undercut profile is essential for successful lift-off as it ensures a clean separation in the metal at the patterned edges of the resist Fig. 5.14(b).

Table 5.4: *Process parameters for O_2 based plasma stripping of ion-implantation hardened photoresist.*

Process Variable	Process Setpoint
O_2 Flow Rate	20 sccm
Chamber Pressure	400 mTorr
RF Power	50 W
PR Etch Rate	350-450 Å/min

Following the metal deposition, the unwanted metal and photoresist is removed by soaking the samples in acetone for 30 minutes. The discontinuity in the metal cover allows the acetone to penetrate under the metal and remove the photoresist. To assist in the effectiveness of the lift-off process, the acetone is stirred at 300 rpm. When the photoresist under the metal has been dissolved, what remains is a thin continuous sheet/film of metal that is attached to the edges of the sample. This metallic film can be removed from the sample by a gentle stream of acetone dispensed from a spray bottle, leaving behind the desired metallic patterns on the sample. On occasion, the metal will tend to stick strongly to the edges of the sample. This metal can be removed by a gently wiping the edges of the wafer with a swab. Under no circumstances should the tops of the samples be wiped with the cotton swab as this will scratch and soil the sample surface. When all the metal has been removed, the samples are sprayed with a jet of acetone and immersed for 20 minutes in a clean beaker of acetone at 90 °C, followed by a 10 minute immersion in 2-propanol at 90 °C. The samples are then dried with an N_2 spray.

The lift-off process can also be aided by designing a photolithographic mask where all metal to be lifted-off is connected. In this way, as the entire sheet

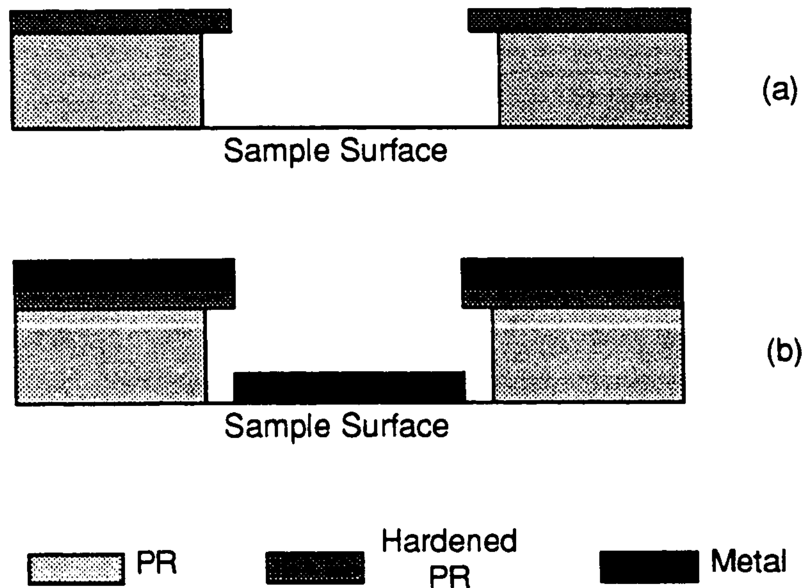


Figure 5.14: Schematic representation of a) the undercut photoresist profile and b) metal coverage for the metal lift-off process.

of metal is lifted-off the sample, the smaller features which tend to get stuck on the sample surface are drawn along with it. This feature is incorporated into the emitter contact patterns for opening windows in the emitter contacts of two styles of devices (see Fig. 5.6(d) and (e)).

5.8 SELF-ALIGNED SiO_2 AND SIDEWALL PASSIVATION MASK

The technique for fabricating self-aligned devices for this project relies on the use of a common, and hence, self-aligned SiO_2 mask for masking the first mesa etch and the second ion-implantation. The series of scanning electron photographs of Figs. 5.15(a)–(c) show the process taken to form the self-aligned SiO_2 mask.

Figure 5.15(a), shows a structure consisting of 3000 Å of Al and 6000 Å of PECVD SiO_2 on the substrate. This structure is formed by first depositing on the structure, 6000 Å of SiO_2 with a Technics 700 plasma enhanced chemical vapour deposition system (PECVD) system under the process conditions listed in Table 5.5. The 3000 Å Al is formed with the lift-off process described in Section 5.7. This Al pattern must possess a relatively smooth edge as any roughness will be transferred to the SiO_2 in the subsequent RIE and this in turn will be transferred to the first mesa when it is etched. The SiO_2 is etched with a CF_4-based plasma in a Technics RIE 800 to produce the features shown in Fig. 5.15(b). The process conditions for etching the SiO_2 are listed in Table 5.6. The etch process is carried out in 3 minute intervals with visual inspection, surface profiling and ellipsometry used to establish the total etch depth and the rate of etch. The SiO_2 is typically over-etched by approximately 1000–1500 Å to ensure that all the SiO_2 is removed. The total etch time for a 6000 Å thick SiO_2 mask is approximately 15 minutes. Since the selectivity between the SiO_2 and the underlying InP or GaAs is extremely high the etch essentially stops at the semiconductor.

Etching with a CF_4-based plasma inadvertently leaves behind a polymer film, consisting mainly of carbon, fluorine and oxygen, on the non-reactive surfaces: semiconductor and Al. This polymer must be removed as it will serve as a micro-mask when the first mesa etched. The polymer is removed by an 8 second dip in 1:20 $HF:NH_4F$ [14]. This 8 second dip in 1:20 $HF:NH_4F$ (1:20) etches 100 Å of CVD SiO_2 and also weakens the Al metallization.

The Al mask is removed by immersing the samples in concentrated Shipley 351 developer, a dilute NaOH based solution, for 10–15 minutes. The OH ions in this solution will react with and dissolve the remaining Al. Following

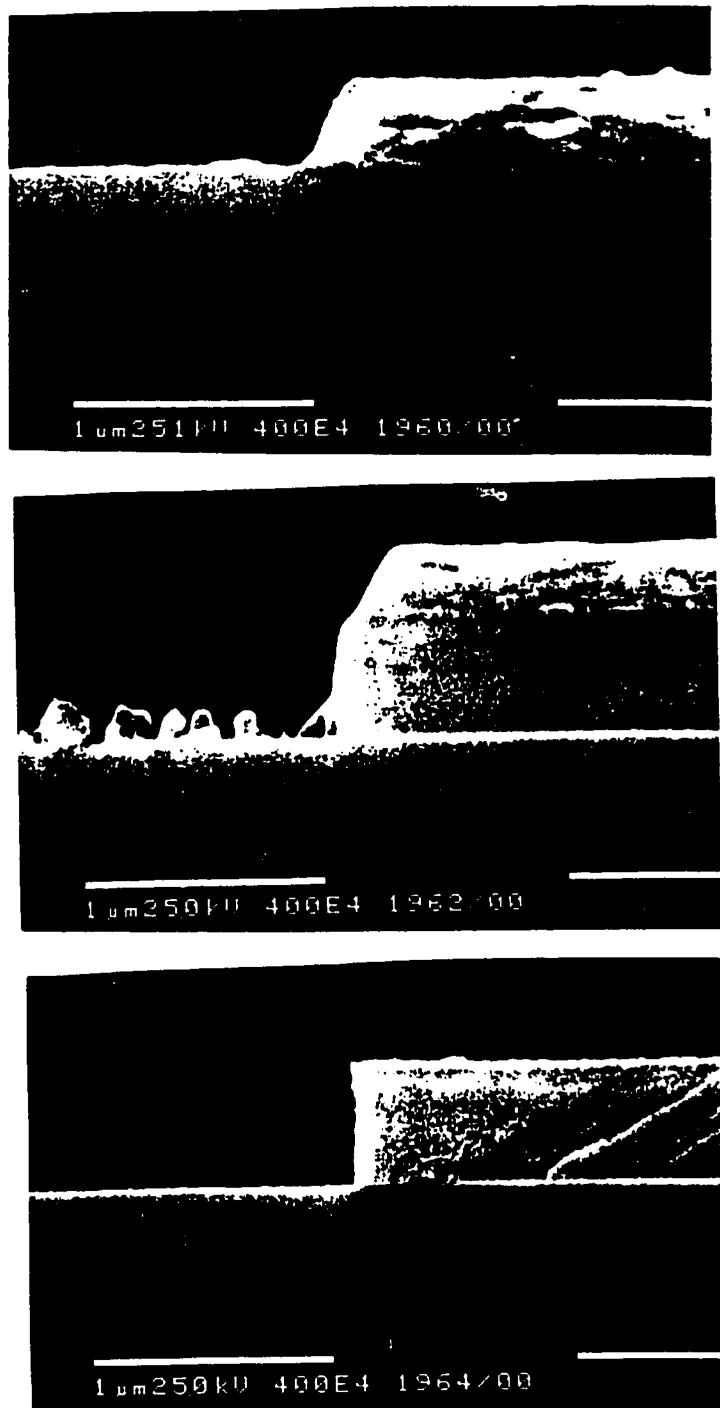


Figure 5.15: Scanning electron microscope (SEM) photographs showing intermediate steps in the formation of the self-aligned SiO_2 mask a) Al patterns on SiO_2/Substrate b) CF_4 reactive ion etch of SiO_2 and c) self-aligned SiO_2 on substrate.

Table 5.5: *Process parameters for chemical vapour deposition of SiO_2 used in the self-align mask process.*

Process Variable	Process Setpoint
SiH_4 Flow Rate	300 sccm
N_2O Flow Rate	12 sccm
Deposition Pressure	750 mTorr
RF Power	50 W
Substrate Temperature	300 °C
Deposition Time	30 min

Table 5.6: *Process parameters for CF_4 based RIE of SiO_2.*

Process Variable	Process Setpoint
CF_4 Flow Rate	20 sccm
Etching Pressure	275 mTorr
RF Power	200 W
SiO_2 Etch Rate	500 Å/min

this process, the samples are thoroughly rinsed in DI for 15 minutes and dried with N_2. This process leaves behind 6000 Å thick SiO_2 formations in the shape of the first mesa. The SEM photograph of Fig. 5.15(c) shows the sidewall profile of the SiO_2 mask as being nearly vertical with less than 1° angle to the vertical. The process also leaves behind a semiconductor surface that is relatively smooth and clean, allowing the first mesa to be etched without the effects of micromasking.

The first mesa is etched $CH_4/H_2/Ar$-based RIE to form the features of Fig. 5.16(a). To prevent the ion-implantation from penetrating the edges of the mesa, a layer of sidewall SiO_2 must be deposited along the exposed edges of the mesa.

The formation of the SiO_2 sidewall begins with the deposition of a 2500 Å of SiO_2 on the entire structure by ECR-CVD [15] or by PECVD. Figure 5.16(b) shows that with plasma deposition, the thickness of oxide on the vertical surfaces is approximately 0.6 times the thickness of oxide deposited on the horizontal surfaces: 2500 Å on the horizontal to 1500 Å on the vertical surfaces. This SiO_2 is etched back leaving behind the sidewall SiO_2 structure with the Technics RIE 800 under the process conditions listed in Table 5.6. This etch relies on the highly anisotropic nature of the RIE to remove SiO_2 from the horizontal surfaces while leaving the sidewall SiO_2, on vertical surfaces of the mesa, unetched. Etching is performed in 3 minute intervals with visual inspection, surface profiling and ellipsometry used to establish the total etch depth and etch rate. The total etch time of this step must be set so that 1) the SiO_2 along the bottom of the first mesa is completely removed but 2) the SiO_2 on the top of the first mesa is not overetched and is thick enough to serve as an ion-implantation mask. Following the CF_4-based RIE, the polymer on the samples must be removed by a 6 second dip into a 1:20 $HF:NH_4F$ solution. This produces the structure shown in Figure 5.16(c) which consists of sidewall SiO_2 that is approximately 1000 Å thick.

This process for self-aligned devices with a dummy SiO_2 mask was developed as an alternative to the refractory gate method as the CEMD did not have the technology for depositing refractory metals.

5.9 RIE WITH QMS

Reactive ion etching is used to form the first and second mesas, and the isolation trenches. This process relies on a reactive plasma to remove semiconductor material anisotropically, producing features with extremely

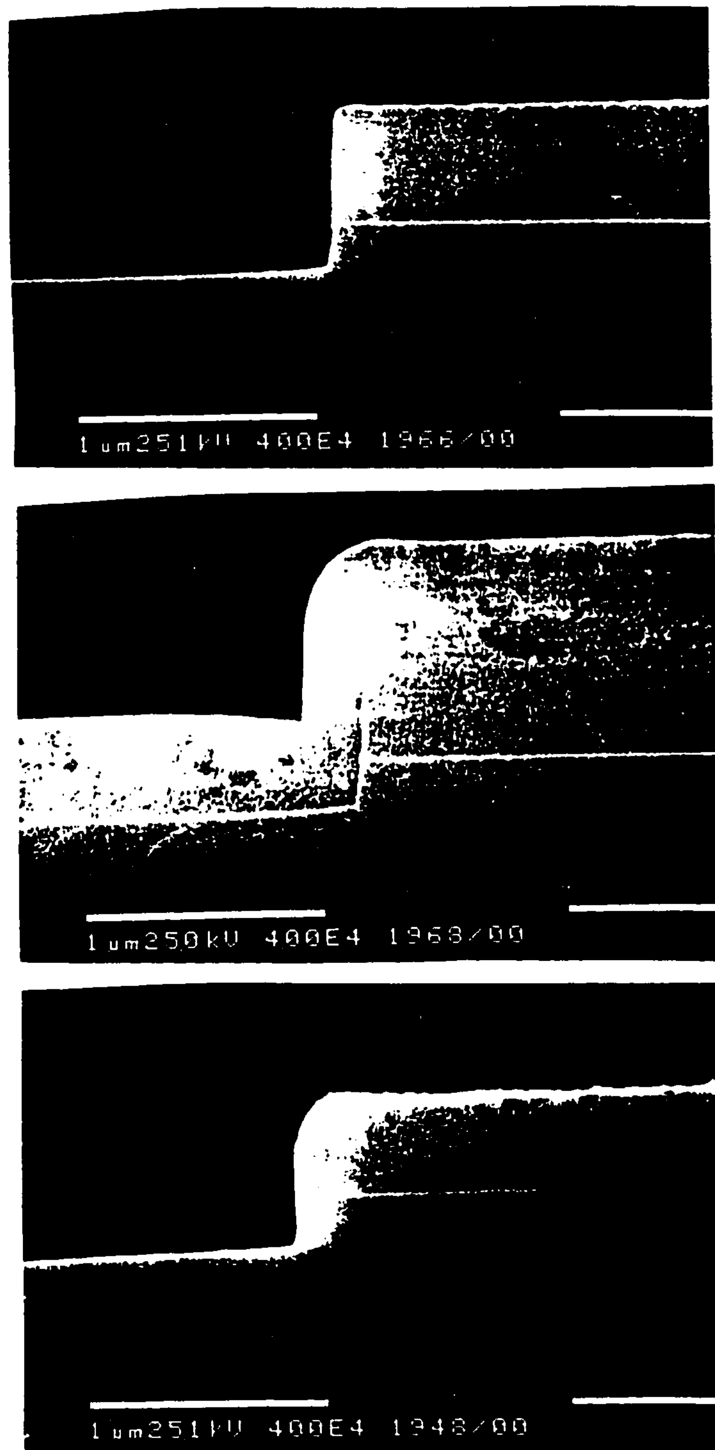


Figure 5.16: SEM photographs showing intermediate steps in the formation of SiO_2 sidewall passivation a) Mesa 1 with self-aligned SiO_2 mask, b) CVD Deposition of SiO_2 over structure and c) CF_4 reactive ion etch back of SiO_2.

vertical sidewall profiles [16]. The RIE system used for this work was constructed by UHV Instruments of Burlington, Ontario. It consists of a stainless steel chamber that is evacuated by a compound turbo-molecular pump combination that is capable of a pumping rate of 1000 Ls^{-1} and a base pressure of 10^{-8} Torr. The samples to be etched are placed on a tantalum substrate holder and transferred into the etching chamber via a load-lock.

The etching system has 5 input gases, Cl_2, CH_4, Ar, H_2 and O_2, whose flows are regulated by mass-flow controllers. The reactive plasma is generated with a ECR source Wavemat MPDR 300 (2.45 GHz) with a tuned cavity design which allows for a large number of ECR resonance modes to be selected. This form of plasma generation results in a very low bias voltage and hence, minimal damage to the substrate compared with conventional systems. Biasing of the substrate is achieved with an RF power supply by RF-Plasma Products (13.56 MHz). Attached to the etching system is a Quadrupole Mass Spectrometer (QMS), Langmuir probe and Optical Emission Spectrometer (OES) which allow for in-situ monitoring of the plasma during an etch.

5.9.1 Etching Parameters

$CH_4/H_2/Ar$-based chemistry is used for etching as it produces vertical sidewalls with smooth surfaces and has high selectivity between mask and InP or GaAs based semiconductors. The $CH_4/H_2/Ar$ based chemistry however, is limited by slow etch rates and polymer formation. The etch conditions used in this fabrication sequence for etching InP based materials are listed in Table 5.7 [17]. These conditions result in nominal etch rates for InP, InGaAsP, InGaAs and GaAs of 220, 150, 150 and 100 Å/min respectively. The actual etch rates of the

Table 5.7: *Process parameters for $CH_4/H_2/Ar$ based ECR-RIE of III-V compounds*

Process Variable	Process Setpoint
CH_4 Flow Rate	2.8 sccm
H_2 Flow Rate	18.0 sccm
Ar Flow Rate	8.0 sccm
Etching Pressure	2.3 mTorr
u-Wave Power	80 W
ECR Stub Tuner Pos.	86.5 mm
RF Bias Voltage	135 V
RF Power	~40 W

semiconductors vary depending on physical properties of the semiconductor including the physical size of the samples, doping concentration, stress in the layers, surface morphology and condition of process chamber. Uniformity of the etch is ±5 % across a 2" diameter area centered on the substrate holder. Figure 5.17 illustrates a profile of the RIE achieved with the process parameters of Table 5.7. The figure shows a mesa with sidewalls that are approximately 6° from the vertical.

Masking of the semiconductor from the RIE is achieved with a thin layer of CVD SiO_2 (500 Å). Since the mask is not etched by the plasma, a polymer will begin to form on the SiO_2 at a rate of about 50 Å/min. This carbon based polymer can be removed by etching in an oxygen plasma. The system used to remove the polymer is a Technics parallel plate RIE with the process parameters of Table 5.8.

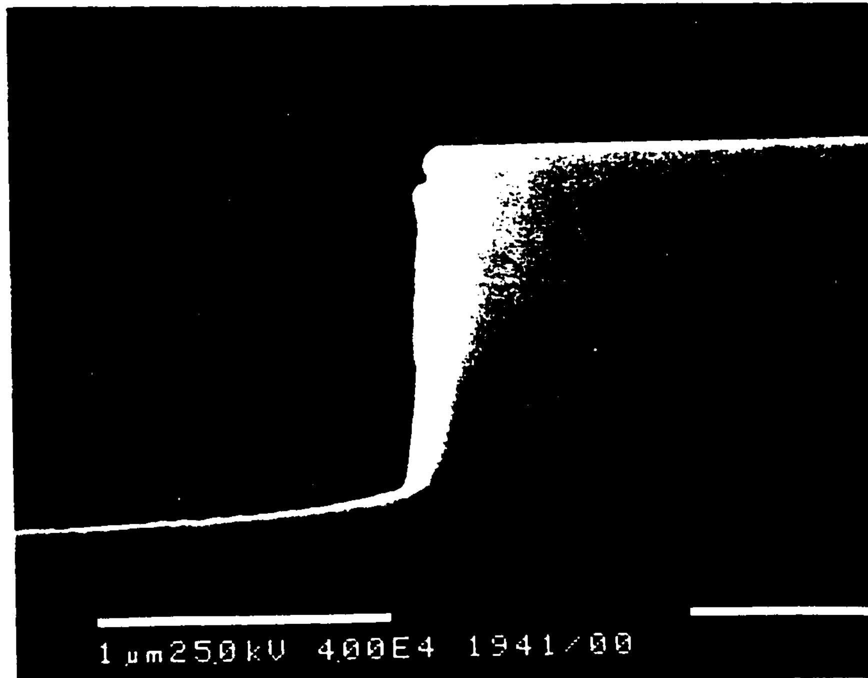


Figure 5.17: SEM photograph illustrating the cross-sectional view of a 1µm mesa etched with an $CH_4/H_2/Ar$ based plasma.

5.9.2 In-Situ Analysis With QMS

In-situ tracking of the etch is achieved by sampling the plasma with a quadrupole mass spectrometer (QMS). The Hiden QMS is a tool that allows the composition of charged ions within the plasma to be monitored during an etch. This instrument samples the ion species with a probe that is positioned at an angle of 17° with respect to the sample stage at approximately 6 cm from the sample. The QMS is differentially pumped through a 250 µm diameter aperture and operates at a pressure of 10^{-7} to 10^{-6} Torr. The QMS must be tuned for maximum sensitivity before each run. This is performed by etching a sacrificial piece of InP, with the conditions of Table 5.7, and adjusting the QMS operating

***Table 5.8:** Process parameters for the removal of polymer with an O_2 based plasma.*

Process Variable	Process Setpoint
O_2 Flow Rate	20 sccm
Chamber Pressure	400 mTorr
RF Power	50 W
Polymer Etch Rate	600 Å/min

parameters to maximize the signal for a mass/charge ratio (m/e) of 34. Typical conditions for the QMS that generate optimum sensitivity are listed in Table 5.9

Figures 5.18 and 5.19 illustrate a sampling of the plasma over four m/e ranges with and without InP and GaAs samples present. The results indicate the presence of dominant peaks at mass/charge ratios 34, 76, 99 and 145 which correspond to the volatile species PH_3^+, AsH_3^+, $Ga(CH_3)_2^+$ and $In(CH_3)_2^+$ respectively, identified by Melville [18]. The ability to track these ion species during the etching of the structures allows for very precise control of etch depth which is crucial in the etching of the first mesa in our devices.

Figure 5.20 illustrates the use of such a system for tracking m/e of 34, 76, 99 and 145 during an etch through the structures of the DOES device. The plot shows a large transient during the initiation of the discharge which takes about 30 seconds to stabilize. The first layer being etched is the InGaAs emitter layer, followed by the InP emitter and the InGaAsP voltage drop/active layer. The first transition from InGaAs to InP takes place at 2:10 min. and the second transition from InP to InGaAsP takes place at 15:15 min. From Fig. 5.20, the etch rate of InP is estimated to be 168 Å/min.

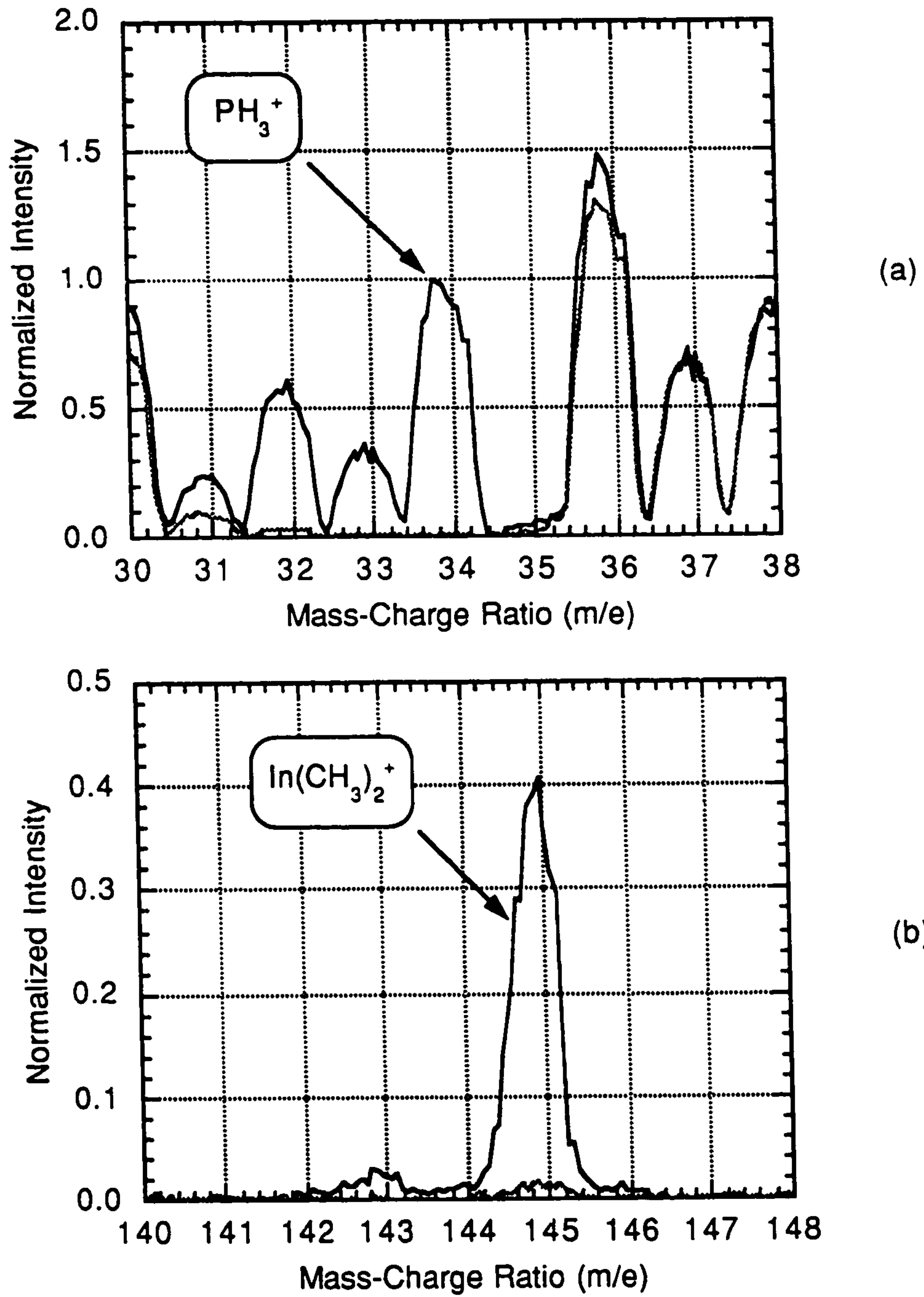


Figure 5.18: Mass/charge profiles of InP etched in a $CH_4/Ar/H_2$ based plasma. (Light trace shows the background profile).

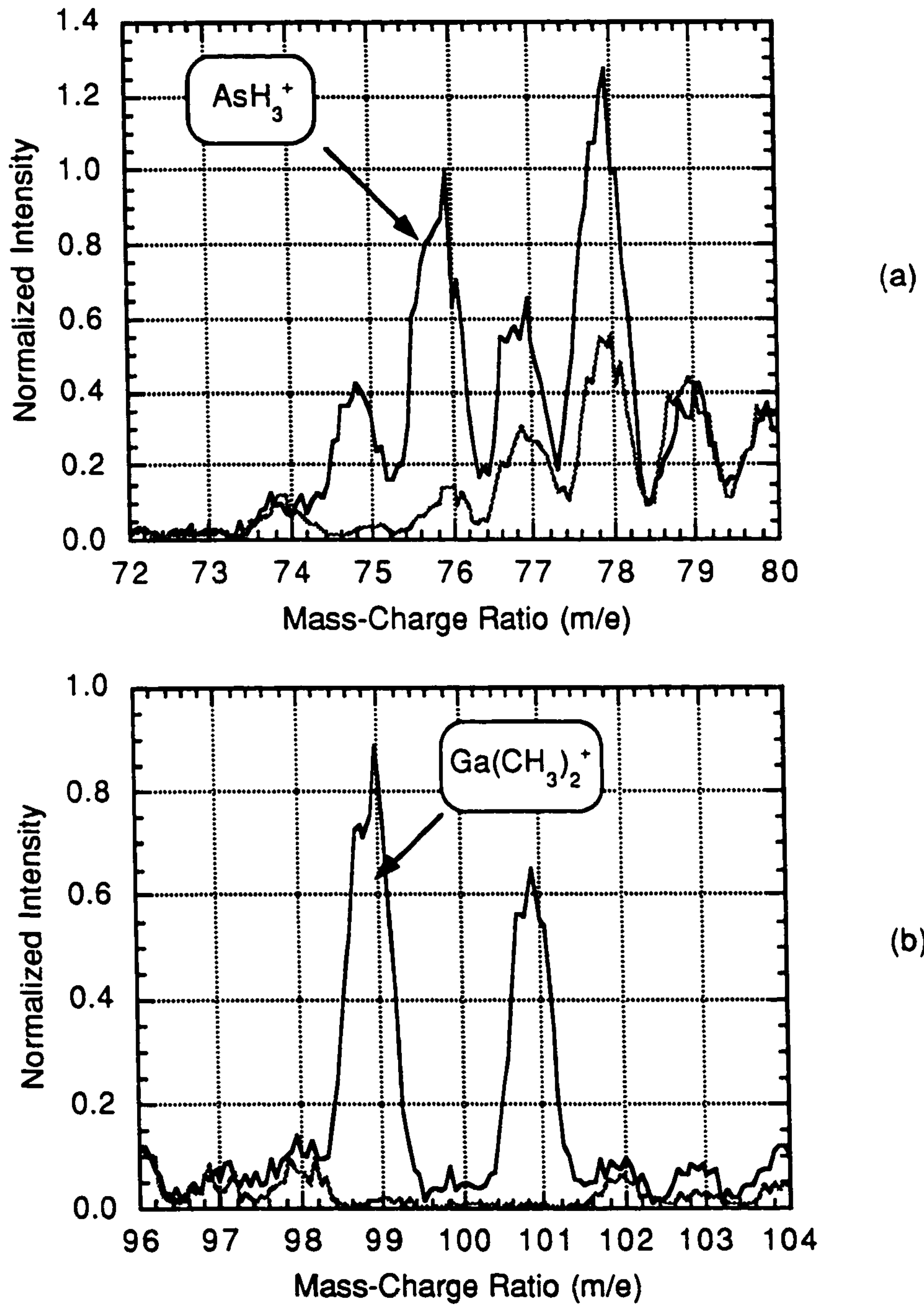


Figure 5.19: Mass/charge profiles of GaAs etched in a $CH_4/Ar/H_2$ based plasma. (Light trace shows the background profile).

Table 5.9: Process parameters for QMS optimized for maximum sensitivity for m/e=34.

Process Variable	Process Setpoint
Energy	25 V
Endcap	-95 V
Focus	-75 V
Supressor	-50 V
Cylinder	3.0 V
E. Energy	0 V
Lens	30 V
Extractor	-60 V

The fabrication process requires the first mesa etch to terminate 1000 Å above the inversion channel. This accuracy in the etch depth is achieved by using the QMS to first estimate the etch rate of the InP emitter material. Then, when etching the samples, the QMS is used to identify the transition from InGaAs to InP and allowed to proceed for an additional time of 7:08 minutes. This will ensure that the first mesa stops 1000 Å above the inversion channel. This method of etching is required because the process steps prior to the first mesa etch tend to thin the emitter contact layer, making it difficult to estimate the thickness of the InGaAs emitter and hence, a precise total etch time from the start of the etch.

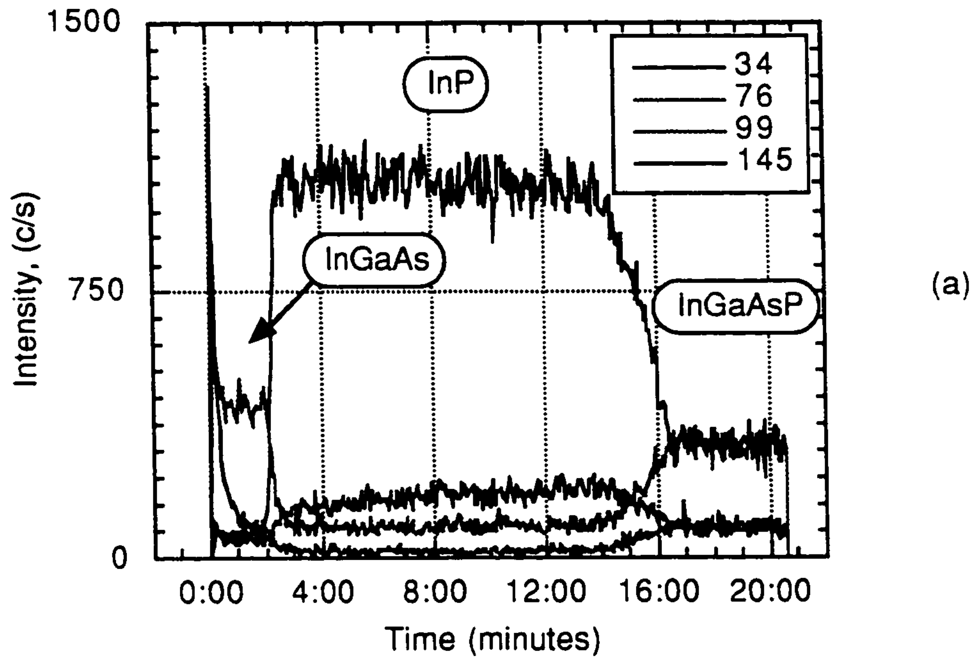


Figure 5.20: Time dependent tracking of the volatile species (m/e=34, 76, 99 and 145) in the plasma during the RIE of S1603.

5.9.3 Chamber Cleaning

The RIE chamber must be cleaned thoroughly before and after use to eliminate any memory effects of previous etches and ensure reproducible etch results. Prior to etching, the chamber and all gas lines are pumped down and purged. The chamber is then sputtered with an Ar plasma for 15 min (see Recipe #1, Table 5.10), followed by an Ar/H_2 plasma for 20 min. (see Recipe #2, Table 5.10). Finally, the chamber is conditioned by exposing it to the etch plasma for 15 min. Following every etch, the chamber must be cleaned with an oxygen plasma (see Recipe #3, Table 5.10) to remove all the polymer that is deposited on the chamber walls during the etch. The chamber should be exposed to the oxygen plasma for at least ⅓ the time it was exposed to the $CH_4/H_2/Ar$ plasma. The

Table 5:10: *Process parameters for cleaning of the ECR-RIE chamber with 1) O_2, 2)Ar and 3)Ar/H_2 based plasmas.*

Process Variable	Process Setpoint		
	Recipe #1	Recipe #2	Recipe #3
O_2 Flow Rate	N/A	N/A	20 sccm
H_2 Flow Rate	N/A	10.0 sccm	N/A
Ar Flow Rate	20.0 sccm	10.0 sccm	N/A
Chamber Pressure	10.0 mTorr	10.0 mTorr	10.0 mTorr
Microwave Power	100 W	100 W	100 W
Stub Tuner Position	88.5 mm	86.5 mm	86.5 mm
RF Bias Voltage	200 V	200 V	200 V
RF Power	~57 W	~60 W	~60 W

chamber should then be sputtered with an Ar plasma for 5 minutes followed by an Ar/H_2 plasma for 5 minutes (see Recipe #2 and #3 of Table 5.10).

5.10 N- AND P-TYPE ION IMPLANTATION

Ion-implantation is used in ICT device fabrication to form regions with localized doping as shown in Fig. 5.7(c) and 5.8(c). The first ion-implantation is used to increase doping in the p-InGaAsP active layer from the 10^{17} cm^{-3} to the mid 10^{18} cm^{-3} range to facilitate ohmic contact formation. The second ion-implantation is used to form a low resistance path for electrons through the p-InP emitter layer between the metal contact and the inversion channel. The ion-implanter at McMaster University is capable of accelerating singly charged ions

to a maximum energy of 120 keV. The charged ions originate from an oven where solid or gaseous source compounds are cracked under high temperatures. Implantations are performed by raster scanning the ion beam across the surface of the samples. The beam current density was limited to a maximum of 0.2 $\mu A/cm^2$ to eliminate amorphization of the III-V surface. The samples are mounted on a sample holder that is tilted 7° from the vertical such that the incident beam is not normal to the sample surface to minimize the effect of ion-channeling. A heater attached to the sample stage allows the implantation to be performed at elevated temperatures.

Se ions implanted at 120 keV with a dose of 5×10^{14} cm^{-2} are used to form an n-type layer for contact to the inversion channel. This implantation was performed at a substrate temperature of 200 °C to eliminate amorphization at the semiconductor surface which results in a substantially improved dopant activation and carrier mobility after annealing [19–21]. The calculated implanted ion and activated dopant profile of Se in InP is shown in Fig. 5.21. The implanted dopant distribution N(x) is derived by assuming a Gaussian distribution of the ions [22]:

$$N(x) = \frac{S}{\sqrt{2\pi}\Delta R_p} \exp\left[-\frac{(x - R_p)^2}{2\Delta R_p^2}\right] \tag{5.1}$$

where S is the implant dose, R_p is the projected range and ΔR_p is the longitudinal straggle. R_p and ΔR_p for Se at 120 keV being implanted into InP is 560 Å and 265 Å respectively [23]. Figure 5.21 shows the total and 20%-activated Se-ion profile. By assuming a dopant activation of 20%, the profile shows a surface doping concentration of 1.6×10^{18} cm^{-3} which increases to a maximum of 1.5×10^{19} cm^{-3} at 560 Å and then drops to 5×10^{17} cm^{-3} at a depth of 1250 Å. This profile shows that

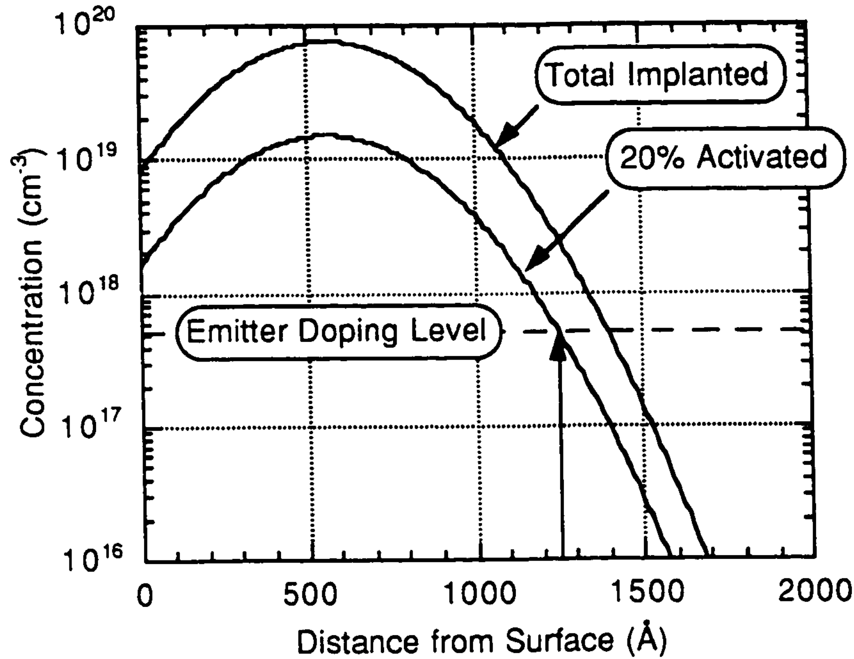


Figure 5.21: Calculated dopant distribution for $5x10^{14}$ cm^{-2} Se implanted into InP at 120 keV.

with these implant parameters, it is possible to convert a 1250 Å thick layer of the emitter from the p- to n-type, thus, dictating the etch depth of the first mesa. The figure also shows that there is a sufficiently high surface dopant concentration for the formation of low resistance ohmic contacts.

Mg ions at 30 keV with a dose of $2x10^{14}$ cm^{-2} are used for the formation of the p-type contact on the active layer. Mg is a relatively light ion possessing a range and lateral straggle in InP of 441 Å and 332 Å respectively when implanted at 30 keV [23]. Since the implant energy is relatively low, surface concentrations in excess of 10^{18} cm^{-3} and carrier activation of 50% can be achieved with proper annealing. The doping profile shown in Fig. 5.22 indicates that a surface concentration of $5x10^{18}$ cm^{-3} is achieved with these implantation parameters. Even in the worst case scenario where only 25% carrier activation is achieved, a

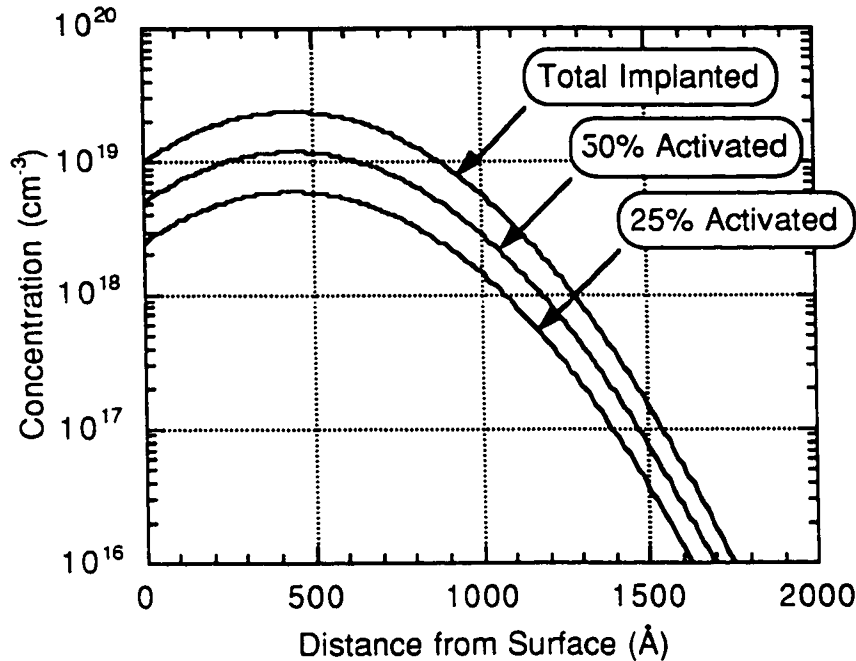


***Figure 5.22:** Calculated dopant distribution for $2x10^{14}$ cm^{-2} Mg implanted into InP at 30 keV.*

relatively high surface concentration of $2.5x10^{18}$ cm^{-3} is still achieved. Such a high surface concentration of dopants will facilitate the formation of ohmic contacts.

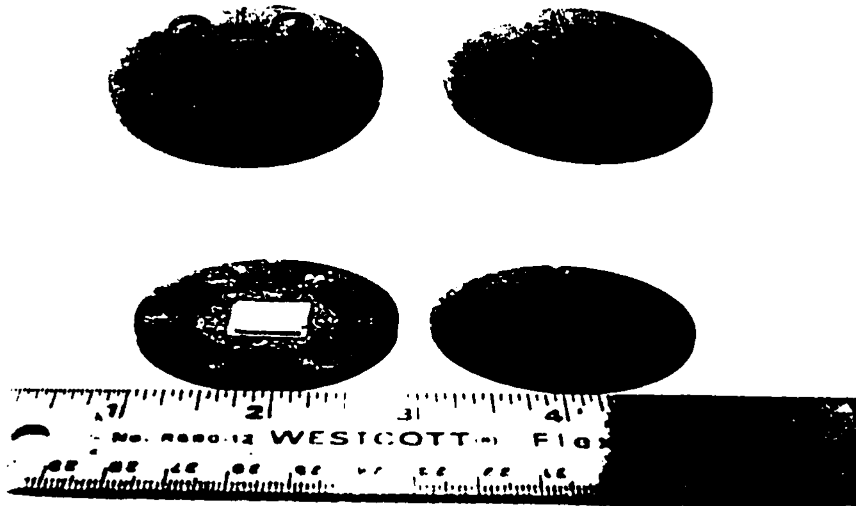
Localization of the implantation is achieved by masking with 2.2 µm thick photoresist layer (see Section 5.6). The range and lateral straggle for Se and Mg in photoresist (see Table 5.11) indicates that the 2 µm thick photoresist is sufficiently thick for masking these implants. Although Be and Si are often used for p- and n-type implants in III-V based semiconductors, they were not readily available at the CEMD facility and therefore, not used in this project.

Table 5.11: *Range and lateral straggle for Se and Mg in InP and Photoresist.*

Substrate	Implant Species and Energy			
	Se^{78} @ 120 KeV		Mg^{24} @ 30 KeV	
	Rp	ΔRp	Rp	ΔRp
InP	560 Å	265 Å	441 Å	332 Å
Photoresist	895 Å	189 Å	1397 Å	178 Å

5.11 IMPLANT ACTIVATION BY RTA

After the implantation, the samples must be subjected to a high temperature (greater than 500 °C) anneal in order to activate the implanted ions and restore the crystal structure of the semiconductor [24]. Annealing of InP based materials is complex as the congruent sublimation temperature of InP is 360 °C. When InP is subjected to temperatures greater than 360 °C, the surface suffers from a proportionally higher rate of P evaporation compared to that of In. This leaves behind pitted surfaces that are In rich in composition [25,26]. Figure 5.23 shows a photograph of the graphite boat that was designed and constructed, for this project, for annealing the samples. The annealing boat is loaded by first placing a thin highly doped InP substrate, which is about 1–2 mm larger than the sample, in the centre of the boat and then placing the sample face up on top of this InP substrate. The remaining space around the sample and the six wells in the periphery are filled with pieces of crushed InP. When the sample is annealed, evaporation of phosphorous from the crushed InP will generate the overpressure required to preserve the sample surface. Annealing in the graphite boat also



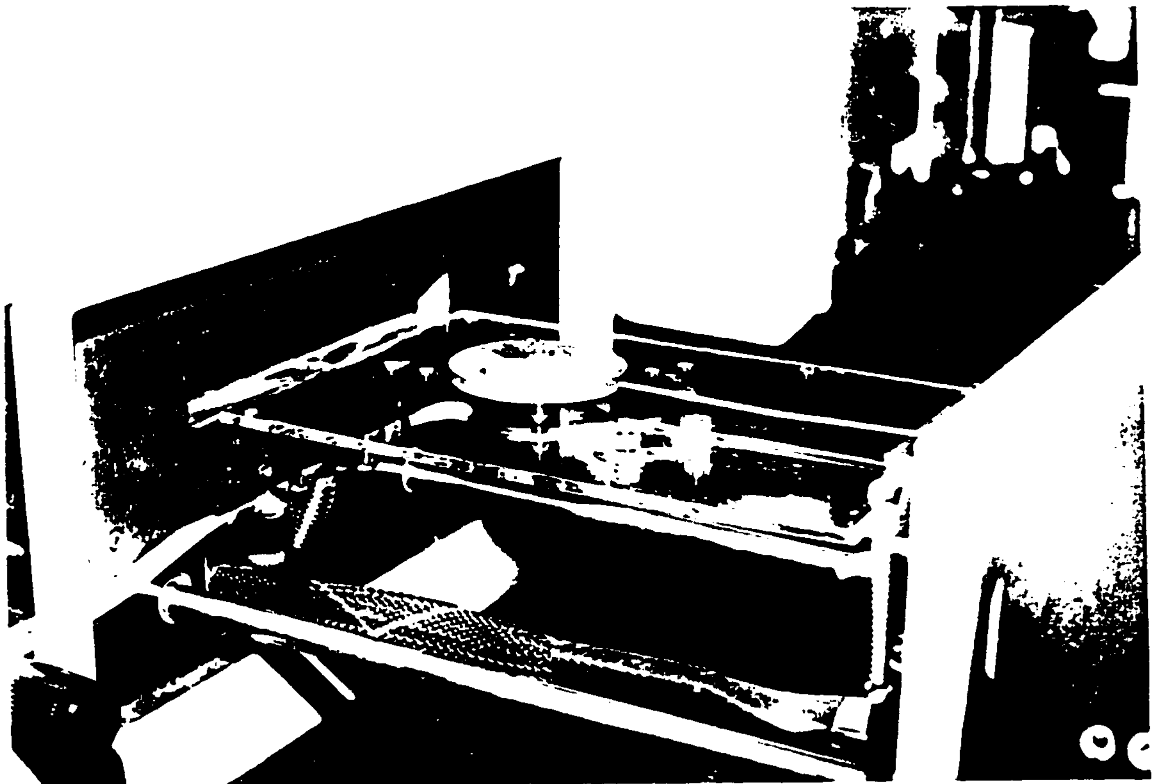


***Figure 5.23**: Photograph showing the graphite boat used for annealing. a) empty, b) with sample and crushed InP and c) in annealing chamber.*

minimizes slip formation on the wafer as a direct result of more even heating achieved with the high-emissivity character of graphite [27,28].

A commonly used method for annealing InP is the proximity cap method where the wafer of interest is placed face to face with another wafer of the same type. This method of annealing is not suitable for this application because the edges of the wafers are not protected and tend to pit. In addition, any movement of the wafers relative to each other during annealing and handling leads to microscratches which degrades device yield [27,28].

The samples are annealed in a HEATPULSE minipulse rapid thermal annealing oven by AG Associates. This form of annealing in an RTA is effective in achieving high activation and mobility from implants with anneal times of 1–60 seconds compared with 10–30 minutes for conventional oven annealing. This is advantageous for use with the ICT structure where diffusion of dopants out of the charge sheet must be minimized [29,30]. The temperature profile designed and used in annealing of the samples consists of a slow ramp up from room temperature to 250 °C before increasing rapidly to 700 °C (see Fig. 5.24). The annealing temperature is then held for 1 second before the heat lamps are shut off and the chamber is allowed to cool down at a rate which is limited by the thermal mass of the chamber and graphite boat. The graphite boat and rapid thermal anneal is able to preserve the surface of InP at temperatures up to 775 °C.

5.11.1 Annealing Results

Figure 5.25 illustrates the results of annealing semi-insulating Fe:In substrates which had been implanted with Se at 120 keV to doses of 1×10^{15}, 5×10^{14} and 1×10^{14} cm^{-2}. These substrates were implanted at a temperature of 190–

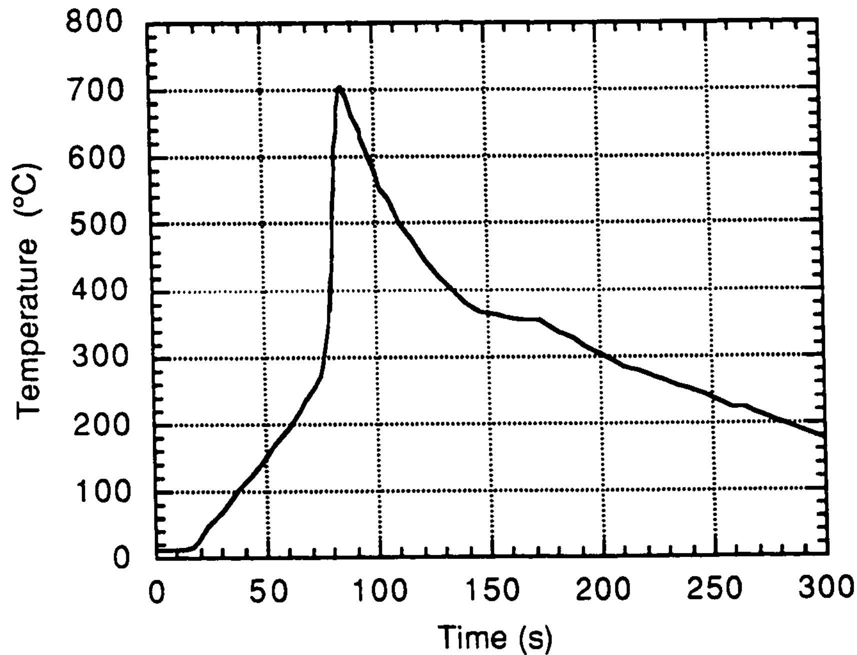


Figure 5.24: *Annealing temperature profile used for ion implant activation. The annealing was performed in a rapid thermal annealer (RTA).*

200 °C. All samples were annealed for 1 second at temperatures ranging from 550 °C to 750 °C. For high dose implants, the dopant activation is relatively constant over the range of annealing temperatures. For the lower dose implant, there is an increase in the activation which saturates at approximately 675 °C. These results indicate that the implantation at elevated temperatures provides the dopant ions with sufficient energy to migrate to lattice sites.

Figure 5.25(b) shows that, for all three dose levels, the mobility increases with temperature and saturates at temperatures above 700 °C. These results compare favourably with published results [30]. Based on the results of Fig. 5.25(a) and (b), the ICT devices were annealed at 700 °C for 1 sec with the temperature profile shown in Fig. 5.24.

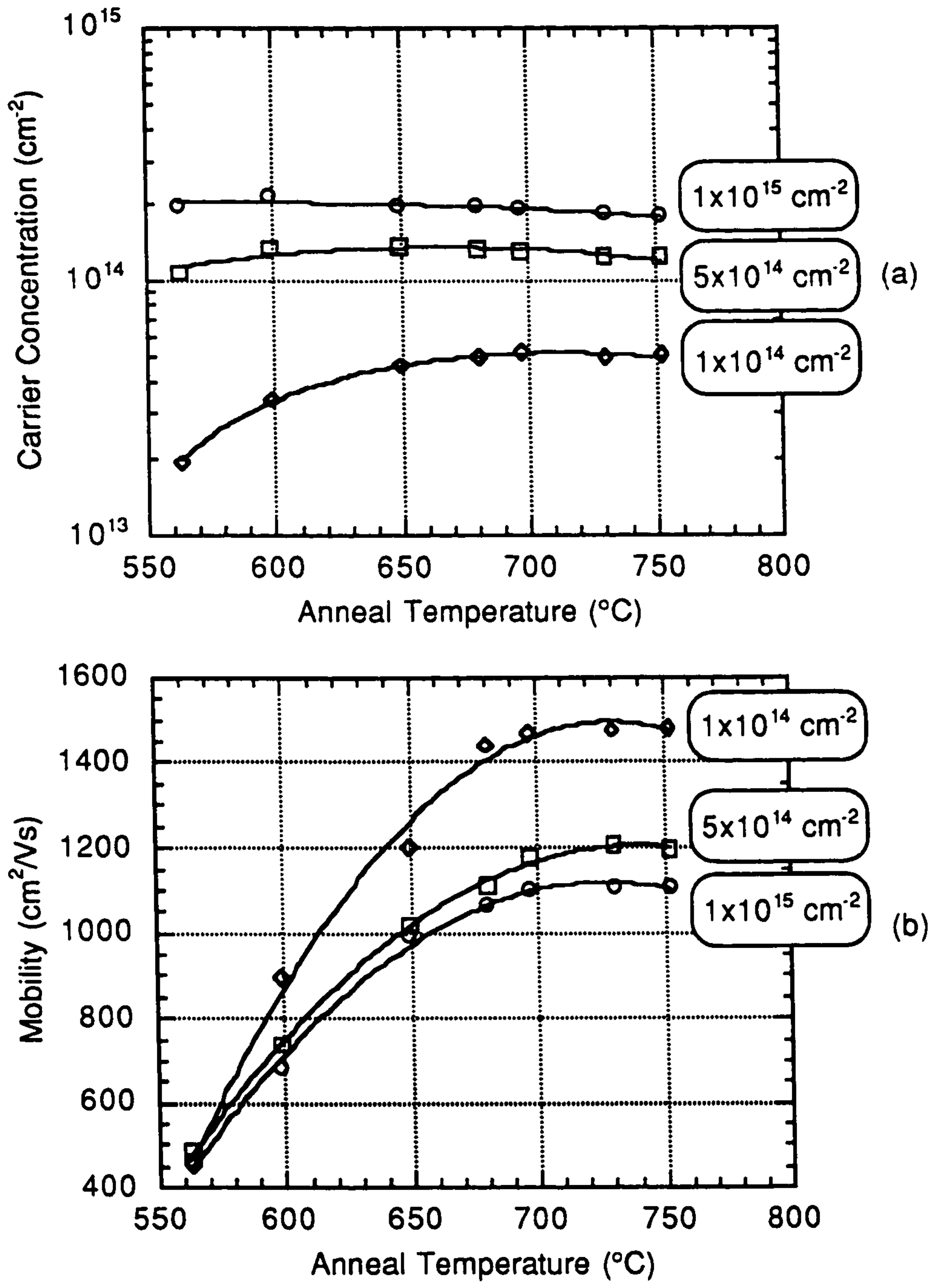


Figure 5.25: *a) carrier concentration and b) mobility as a function of annealing temperature for Se implanted SI:InP. Samples were subjected to a 1 second anneal.*

5.12 CONTACT METALLIZATION

Electrical access to the ICT devices is achieved by forming low-resistance, ohmic contacts to the emitter, inversion channel, active and collector layers. These contacts are formed by depositing a multi-layer metallic stack onto the sample and annealing the metal-semiconductor structure. The anneal forces the metal and semiconductor to intermix, forming an intermetallic transition layer at the interface which establishes the carrier-transport properties for the contacts [31–34].

The metal deposition system at McMaster consists of a deposition chamber, preparation chamber and a load-lock. Both the preparation and deposition chambers are evacuated by CTI-cryo pumps which maintains them at a pressure of 1×10^{-8} Torr. The metallization chamber has a 6-crucible e-beam source consisting of Ti, Pt, Ni, Ge, Au and Al. The deposition rate and total thickness is monitored by a crystal thickness monitor.

The samples for deposition are transferred to the preparation chamber through the load-lock and allowed to degas for 3 hours. Prior to deposition, the sources are degassed by melting each of the sources with the e-beam and evaporating them at a rate of 5 Å/sec for approximately 30 sec. The samples are then transferred to the deposition chamber for metal deposition. During the deposition, the samples are rotated at approximately 10 rpm. All layers are deposited at a rate of 2 Å/s.

5.12.1 Backside Metal

Contact metal, for the collector, made to the back-side of the sample consists of Ni-Ge-Au of thicknesses 300-500-2000 Å respectively. In this scheme, Ni is the first layer deposited and is in contact with the semiconductor. This metallization scheme achieves very low specific contact resistance, in the range of 10^{-6} to 10^{-8} $\Omega\cdot cm^2$ [35,36], to n-type InP after an anneal. Although this metallization scheme exhibits exceptionally low contact resistance, it exhibits deep penetration of the metal into the underlying semiconductor structure, lack of long-term metallurgical stability, non-uniform depth of interaction and spatial composition [37]. As a result of these deleterious effects, specifically, the large penetration depth of metal into the semiconductor, this metallization scheme is limited to forming contacts on the backside of the wafer.

5.12.2 Topside Metal with Tilt Stage

Topside metallization to the emitter, inversion channel and active layers is Ti-Pt-Au based. This system is used because it is thermodynamically more stable than Ni-Ge-Au and there is significantly less intermixing between the metal and semiconductor during the anneal. The penetration depth for this metal system into the underlying semiconductor is on the order of 300–500 Å [38–41]. This contact metallization is effective in forming ohmic contacts to both p- and n-type InP based materials, allowing it to be used for the p-type emitter and active contacts as well as the n-type inversion-channel contact [38,42,43].

The mesas for the devices on the ICT structure are all etched by RIE and exhibit very vertical sidewall profiles (see Fig. 5.17). This creates a problem as the metal deposits anisotropically and, thus, coverage of the metal along the

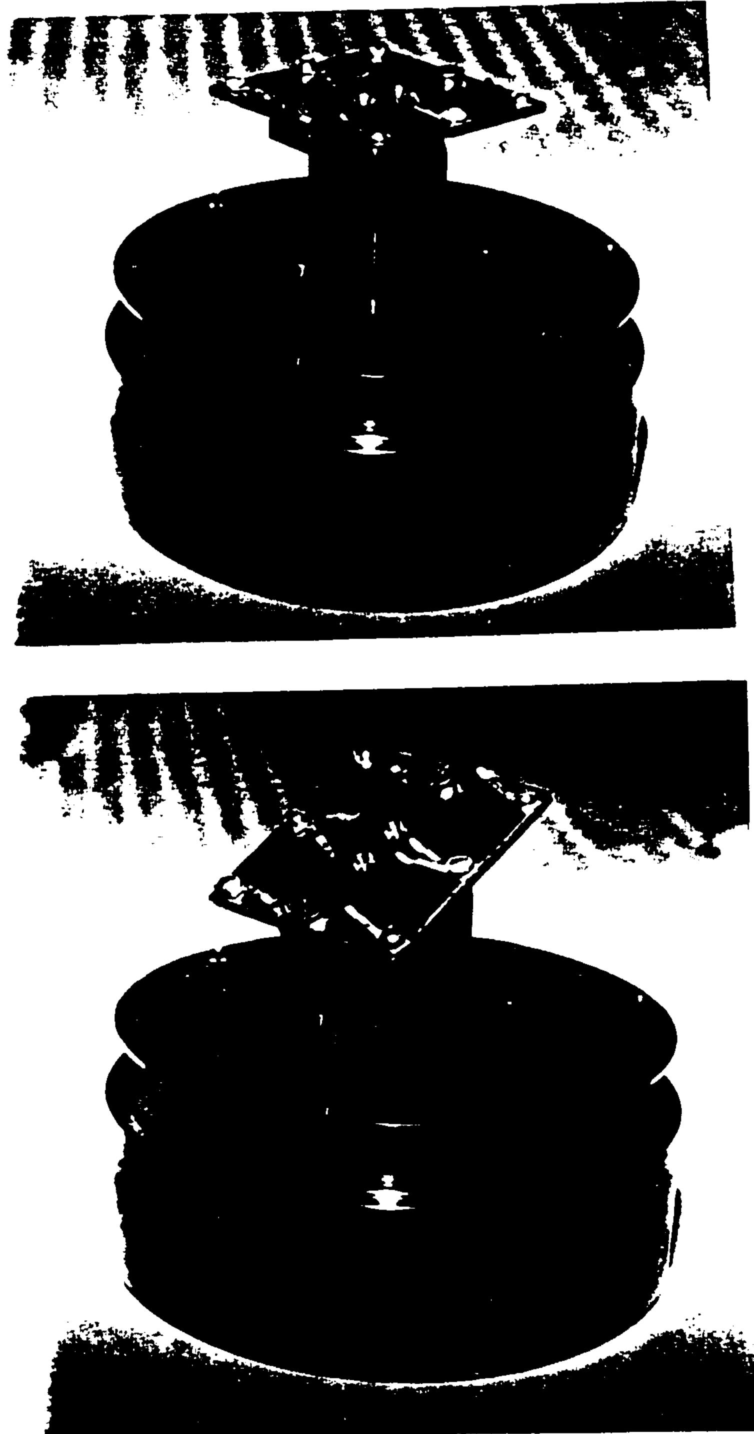


***Figure 5.26:** Photography of the tilt stage used for topside metallization of the samples. Stage set at a) at 0 degrees and b) tilted at 30 degrees.*

sidewalls of the mesa is very thin and discontinuous. A tilt stage was designed and constructed, for this project, to improve the coverage of metal along the sidewalls of the mesas. This stage allows the samples to be tilted at an angle ±30° to the plane of metallization (see Fig. 5.26). The angle of tilt can be changed during the metal deposition process with the substrate loading arm. To apply metal with the tilt stage, each layer of metal in the stack is divided into two halves so that one half is deposited with the stage tilted at -30° while the other half is deposited with the stage tilted at +30°. The topside metallization used for this project is 250-250-350-350-800-800 Å of Ti-Ti-Pt-Pt-Au-Au respectively. The metallization begins with the sample tilted at 30° for the first half of Ti metal. Then, the stage is tilted to -30° for deposition of the second Ti layer and the first Pt layer. The stage is tilted back to the 30° position again for the deposition of the second layer of Pt and the first layer of Au. Finally, the stage is tilted to -30° again and the second and final layer of Au is deposited.

Figure 5.27 illustrates an SEM micrograph of a 1.1 μm mesa metallized with the tilt-stage recipe. This figure clearly shows a relatively uniform and continuous film of metal along the sides of the mesa. The continuity of the metal layer along the sidewall is crucial to forming good contacts between the top of the mesa and the contact pads which lie on the base of the mesa. Thickness of the metal on top and at the base of the mesa is ~2200 Å while the sidewall metal thickness is ~750 Å. The small notch in the metal layer along the base of the mesa is a result of the shadow masking from the mesa itself. The metal in this notched area is approximately 1050 Å thick. The thickness of the metal on the top of the mesa is limited by the total thickness of metal that can be lifted-off successfully. This is limited by the thickness of the photoresist used in the lift-off patterning. A

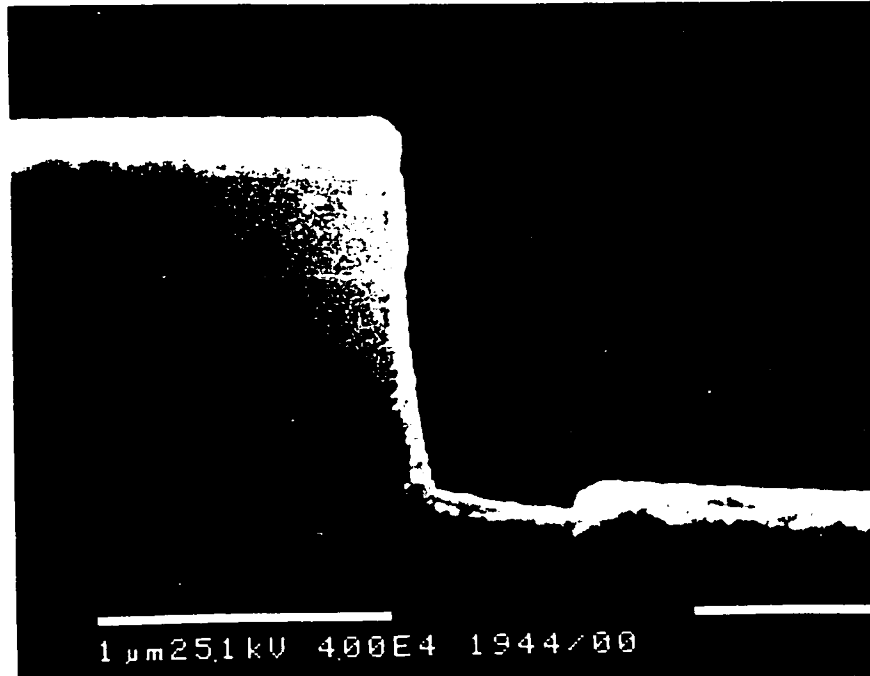


Figure 5.27: SEM photography showing the cross-sectional view of an RIE sample subject to topside metallization with a tilt stage.

conservative estimate of maximum metal to photoresist thickness ratio is 1:3. Since a 1 µm thick resist is used in the process, the total metal deposited is limited to a thickness of 3000 Å.

5.12.3 Contact Anneal Conditions

Contacts to the p- and n-type semiconductors must be annealed in order achieve low resistance ohmic behaviour. Although the multi-layered metallic stacks to the p- and n-type semiconductors have different optimal anneal cycles, a common alloying sequence which yields satisfactory results for both types was used. The annealing recipe requires subjecting the samples to 400 °C for 20 seconds in forming gas (5.5% H_2 in N_2). The samples are first sandwiched between two pieces of clean GaAs wafers and placed on the substrate holder of

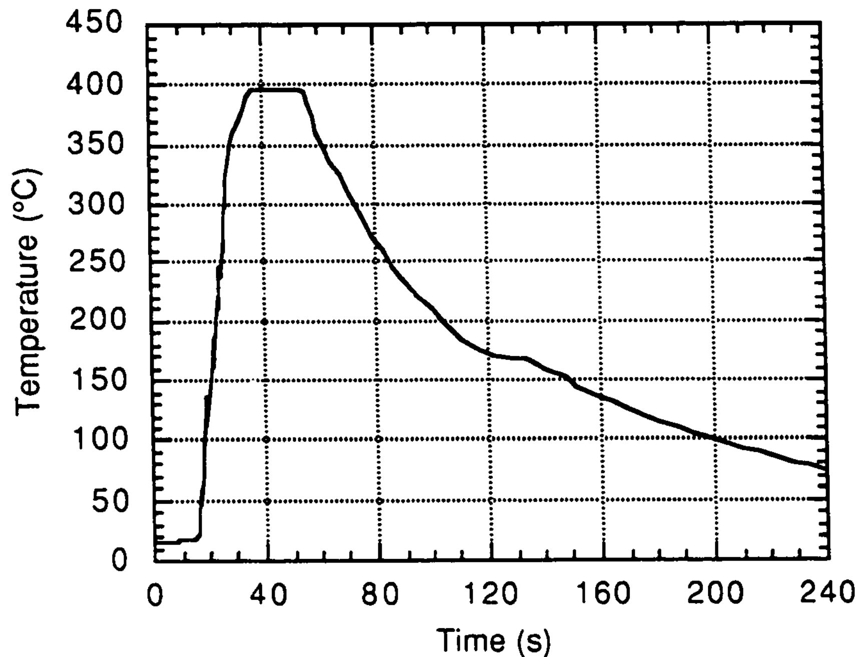


Figure 5.28: Annealing temperature profile used for ohmic contact formation. The annealing was performed in a rapid thermal annealer (RTA).

the rapid thermal annealer. The wafers were centered above the thermocouple that is mounted to the backside of the substrate holder. The primary purpose of the GaAs wafers is to serve as proximity caps to limit the outdiffusion of group V materials from the device structure. The samples are sealed in the annealing chamber which is flushed with a 5 slpm flow of forming gas for 5 minutes. Under the flowing forming gas ambient, the temperature of the chamber is ramped up at 50 °C/s ramp to 400 °C. When the chamber reaches 400 °C, the temperature is held constant at 400 °C for 20 seconds before the heating lamps are turned off. The chamber is allowed to cool as rapidly as possible. Figure 5.28 illustrates the temperature profile used in the annealing process.

Visible inspection of the Ti-Pt-Au contacts should show that they are gold in colour with no visible changes in colour or surface morphology. The Ni-Ge-Au

contact will appear silver with a salmon or pinkish tint. This colour change is a result of the In migrating to the surface to form $In_{1-x}Au_x$ compounds. This change in contact metallization emphasizes the alloy nature of this contact and the deep penetration of the metal into the semiconductor. A blanket metal of Ti-Pt-Au 400-600-1500 Å is applied to the backside of the wafer on top of the annealed Ni-Ge-Au contact to build up and passivate the backside metal.

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CHAPTER 6

EXPERIMENTAL CHARACTERIZATION OF THE DOES

This chapter demonstrates the operation of the 4-terminal n-channel InGaAsP-InP based DOES. It begins with a description of the experimental apparatus and biasing scheme used to electrically and optically characterize these devices. This is followed by detailed electrical and optical characterization of devices from wafer S1601 which includes 2-terminal current-voltage (I-V) and light-current (L-I) characteristics. The influence of device structure and size on the I-V characteristics of the device is then examined. Finally, the effects of carrier injection into the inversion channel and active layer, and optical injection on the I-V characteristics of the device are examined. In all cases, the I-V characteristics of the e-i, a-i and a-c junctions were measured as a function of the drive current to obtain further experimental insight into device operation. Comparisons between experimental and theoretical results are made throughout the chapter.

6.1. EXPERIMENTAL APPARATUS AND BIASING

The apparatus used to electrically characterize the DOES devices consists of a Hewlett-Packard Semiconductor Parameter Analyzer (HP4145B) and a probe

station (see Fig. 6.1). The HP4145B has four independent source-measure units (SMU), each capable of either sourcing a current and measuring voltage or sourcing a voltage and measuring current. The HP4145B also has two voltage measurement units (VMU) which are capable of measuring voltages over the range from -20 V to +20 V. The probe station includes a microscope and four xyz-manipulators with fine tungsten needles. With the aid of the microscope and the xyz-manipulators, the tungsten needles can be positioned very precisely on the contact pads of the devices to allow for connection between the SMU and the device under test (DUT). The entire probe station is enclosed in a metal box to minimize the amount of ambient light incident on the DUT.

In order to make optical measurements, an additional xyz-manipulator was modified to accommodate an optical fibre instead of the tungsten needle. This manipulator is used to position one end of the optical fibre directly above the device (see Fig. 6.2). To optically pump the device, the free-end of the fibre is coupled to a λ = 1.3 μm semiconductor diode laser through a fibre coupler. This laser is current driven with an ILX semiconductor laser diode driver. To collect light emitted from the device, the free-end of the optical fibre is coupled to an InGaAs photodetector through the fibre coupler. A mechanical chopper is placed in the path of the light between the fibre coupler and photodetector. The electrical signal from the photodetector is collected and processed by a Stanford Research SR810 lock-in amplifier. This signal is collected by the HP4145B by a connection between the external output of the lock-in amplifier and the VMU on the HP4145B. The experimental setup described allows each of the four contacts on the DOES device and the optical window to be accessed simultaneously.

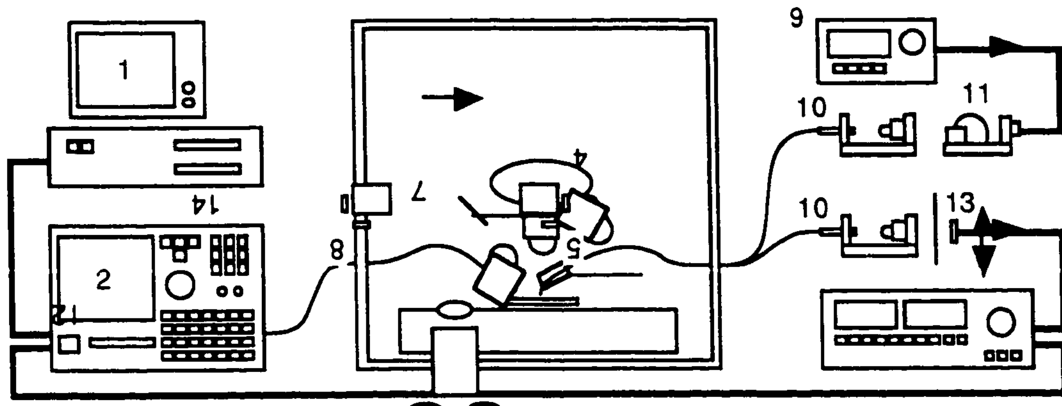


Figure 6.1: Schematic representation of the experimental apparatus for electrical and optical characterization of ICT devices. 1) Microcomputer, 2) Semiconductor parameter analyzer, 3) Probe station enclosure, 4) Sample stage, 5) Electrical probe with co-axial cable connection, 6) Microscope, 7) Device under test, 8) Optical probe with optical fibre connection, 9) Laser diode driver, 10) Optical fibre coupler, 11) Laser diode and mounting, 12) Mechanical chopper, 13) InGaAs photodetector, and 14) Lock-in amplifier.

The HP4145B serves as the coordinator for all the electrical and optical measurements. All data is collected and stored by the instrument in HP4145B format. This data can be transferred to a PC and converted to DOS compatible ASCII format via the IEEE-GPIB interface. The IEEE-GPIB connection also allows for computer control of the HP4145B and, thus, for automated testing of the devices.

The 4-terminal n-channel DOES device is biased by grounding the collector and injecting current into the emitter contact. This biasing scheme is required for devices which exhibit S-type negative differential resistance, as voltage is a function of current and therefore, there is a unique voltage for each current level; the converse is not true. The inversion channel and active layer contacts allow for external control of the I-V characteristics through injection or

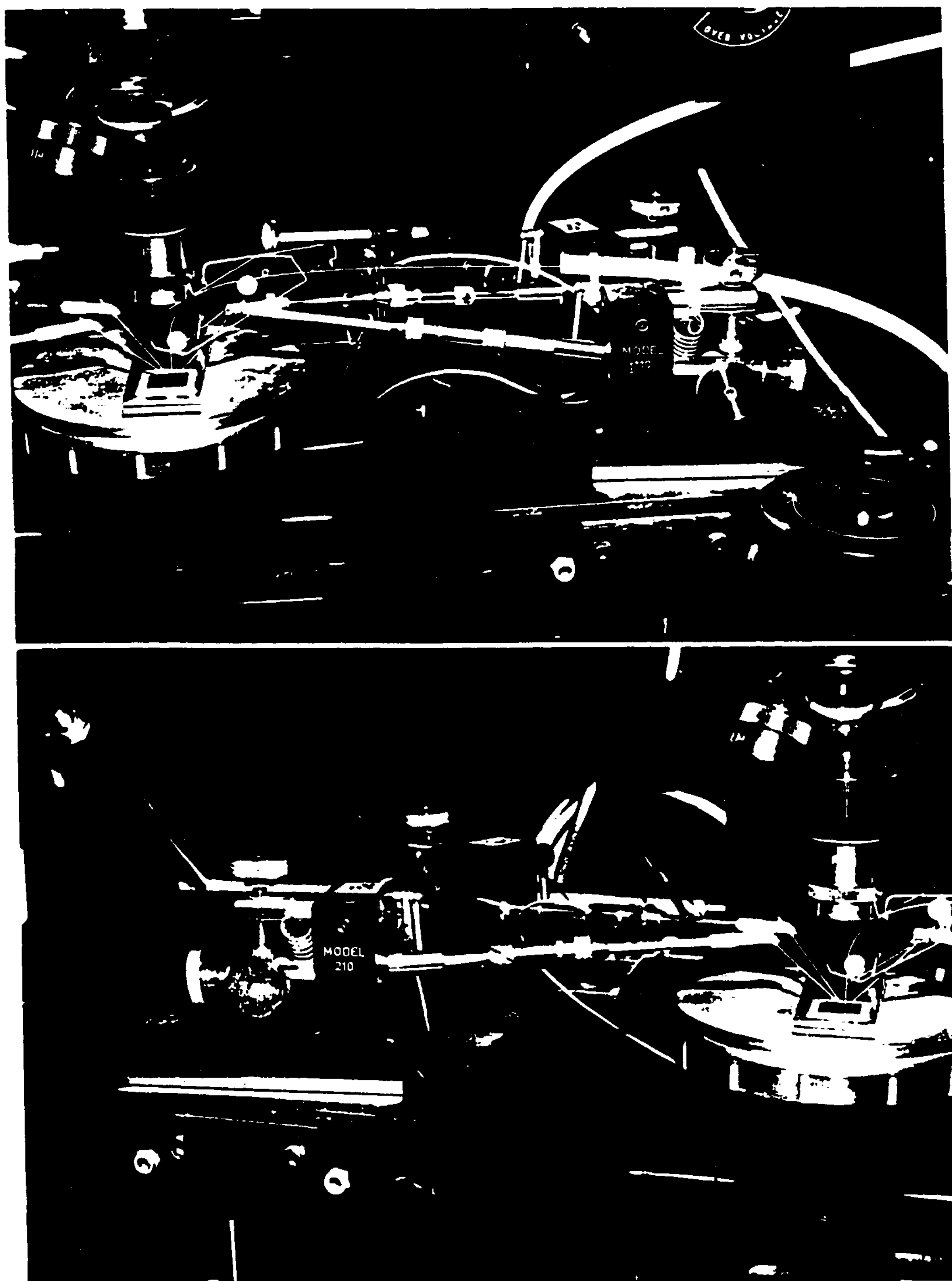


***Figure 6.2:** Photograph of a) an xyz-manipulator modified to accommodate an optical fibre and b) a standard xyz manipulator with tungsten probe.*

extraction of current from the structure. Optical injection through the contact window also allows for optical control of the switching condition. The SMUs are configured to inject current into and measure voltage at each of the contacts. This allows the device and voltage across the e-i, a-i and a-c junctions to be measured as a function of injection current.

6.2. TWO-TERMINAL DEVICE OPERATION

In the following sections, results from a detailed electrical characterization of an 80 x 80 μm^2 DOES device on S1601 are presented. The characteristics demonstrated by this device are representative of other DOES devices on S1601 with emitter mesa length (L) ≥ 80 μm and width (W) ≥ 80 μm.

6.2.1. DC I-V Characteristics

Figure 6.3(a) shows the dark two-terminal I-V characteristic of the DOES. The switching voltage (V_{sw}) and current (I_{sw}) are 3.19 V and 200 μA respectively, while the holding voltage (V_h) and current (I_h) are 1.92 V and 2 mA respectively. In the OFF state defined by the region of operation where $I_e < I_{sw}$, the device exhibits a high resistance (R) of approximately 10 KΩ. In the ON state defined by the region of operation where $I_e > I_h$, the device exhibits a resistance of less than 10 Ω. The region of operation where $I_h < I_e < I_{sw}$ is defined as the NDR region and represents a region of unstable device operation.

Figure 6.3(b) illustrates the dark two-terminal I-V characteristic measured with a logarithmic sweep of I_e. In the operating range marked by points A and B, recombination-generation dominates current transport through the device. In the region between points B and C, the contribution from diffusion current transport

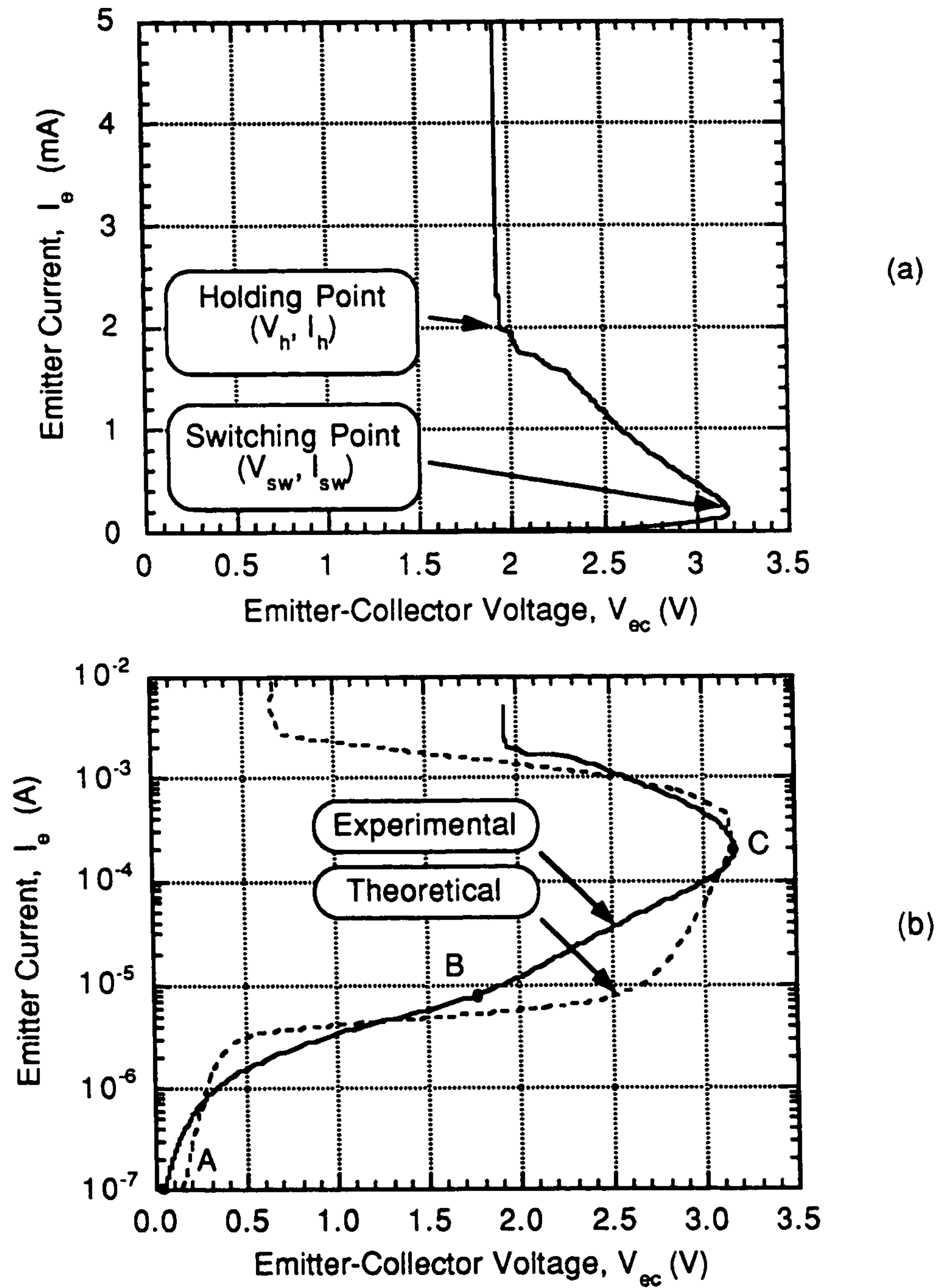


Figure 6.3: *Dark current-voltage (I-V) characteristic of an 80 x 80 μm^2 DOES device measured with a a) linear and b) logarithmic sweep of I_e. Dotted I-V characteristic was generated by the model of Chap. 2 (see Fig. 2.7).*

becomes increasingly significant. A comparison of the experimental I-V characteristics with the theoretical results of Chap. 2 show reasonably good agreement in the characteristic shapes of the curves (see Fig. 2.7). The switching voltage and currents are comparable in magnitudes; however, the experimental V_h is approximately 1.2 V higher than the theoretical V_h. This discrepancy in the experimental and theoretical V_h will be discussed in latter sections.

A distinct advantage of a 4-terminal DOES device is the ability to electrically access each of the four operational layers of the device. This allows the voltages across the emitter-inversion channel (V_{ei}), active layer-inversion channel (V_{ai}) and active layer-collector junctions (V_{ac}) to be measured over the entire range of I_e (see Fig. 6.4). These junction voltages are related to the device voltage (V_{ec}) by

$$V_{ec} = V_{ei} - V_{ai} + V_{ac} \tag{6.1}$$

The junction voltages are defined to be positive when the junction is forward biased, negative when reversed biased and zero under thermal equilibrium. As I_e increases, V_{ac} begins at approximately 0 V and increases over the entire range of I_e. Conversely, V_{ai} decreases as I_e increases and reaches a maximum reverse-bias voltage of -0.73 V. This corresponds with the switching point of the device where $I_e = I_{sw}$. When $I_e > I_{sw}$, V_{ai} begins to increase until a forward bias potential is established across the a-i junction. The operation of the a-i and a-c junctions resemble that predicted by the model of Chap. 2 (compare with Fig. 2.8).

The I-V characteristic measured across the emitter and inversion-channel contacts shown in Fig. 6.4, exhibits a behaviour that is different from the model of Chap. 2. As I_e increases, V_{ei} increases and reaches a maximum voltage of 2.34 V at $I_e \approx I_{sw}$. For further increases in I_e, where $I_{sw} < I_e < I_h$, V_{ei} decreases. Finally,

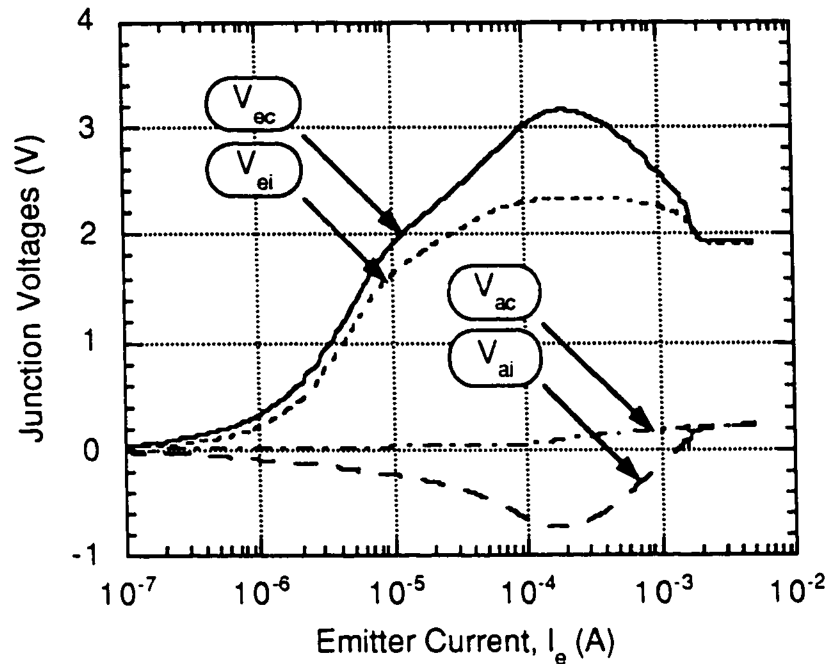


Figure 6.4: Voltage across e-i, a-i and a-c junctions as a function of the emitter current.

for $I_e > I_h$, V_{ei} remains essentially constant at V_{ei} = 1.93 V. The general shape of the I_e-V_{ei} curve resembles the I_e-V_{ec} characteristic of the DOES device. This behaviour results because of parallel conduction paths which exist between the emitter and inversion-channel contacts. In the schematic cross-section of Fig. 6.5, path A illustrates the current path associated with the p-n junction diode formed by the inversion channel and the emitter layers. Path B illustrates the current path through the active layer which forms a p-n$^+$-p-n structure that gives rise to the switching characteristic that is similar to the I_e-V_{ei} characteristic of the DOES.

The existence of parallel conduction paths between the emitter and inversion-channel contacts sets V_{ei} in the ON state of 1.93 V as opposed to approximately 0.7 V predicted by the model (see Fig. 2.8). As a result, the experimental V_h is 1.2 V higher than that predicted by the model.

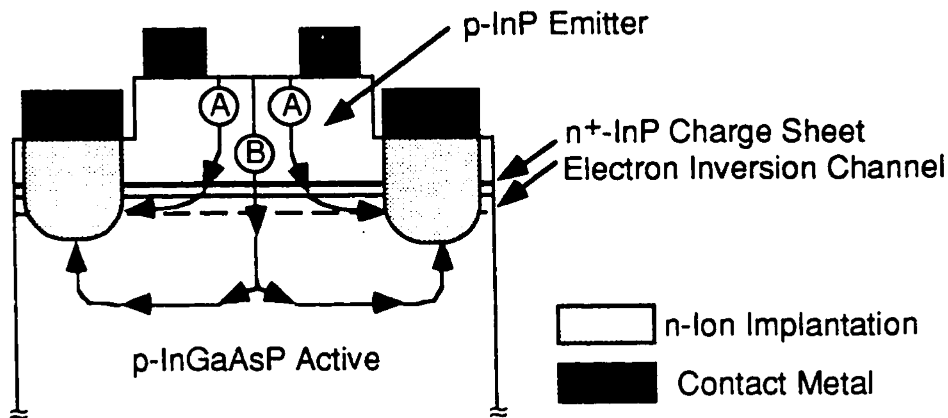


Figure 6.5: Schematic cross-section of the DOES device highlighting the parallel conduction paths which exist between the emitter and inversion-channel contacts. Path A: pn-junction device characteristic, path B: pnpn-device characteristic.

6.2.1. Time-Dependent I-V Characteristics

Figures 6.6(a) and (b) show the oscillations in the device voltage and current when it is biased in the NDR region. The device is biased by applying a DC current of 1.50 mA to the emitter with the SMU. Under this bias condition, a collector-emitter voltage of 2.24 V is measured by the SMU. The time-dependent voltage was measured directly across the device with an oscilloscope while the time-dependent current was obtained by measuring the voltage across a 1 Ω resistor that was connected in series with the device. The current and voltage waveforms oscillate at 550 kHz with a peak voltage of 2.65 V and a peak current of 13 mA. There is a π radians phase shift between the voltage and current which confirms the existence of NDR*. The time-average current and voltage of the oscillation waveforms are 2.16 V and 1.48 mA respectively, and are in agreement

* When the current and voltage waveforms are π radians out of phase with each other, the voltage increases as the current decreases or the voltage increases as the current decreases, the differential resistance $dR = dV/dI$ will be negative; giving rise to the NDR.

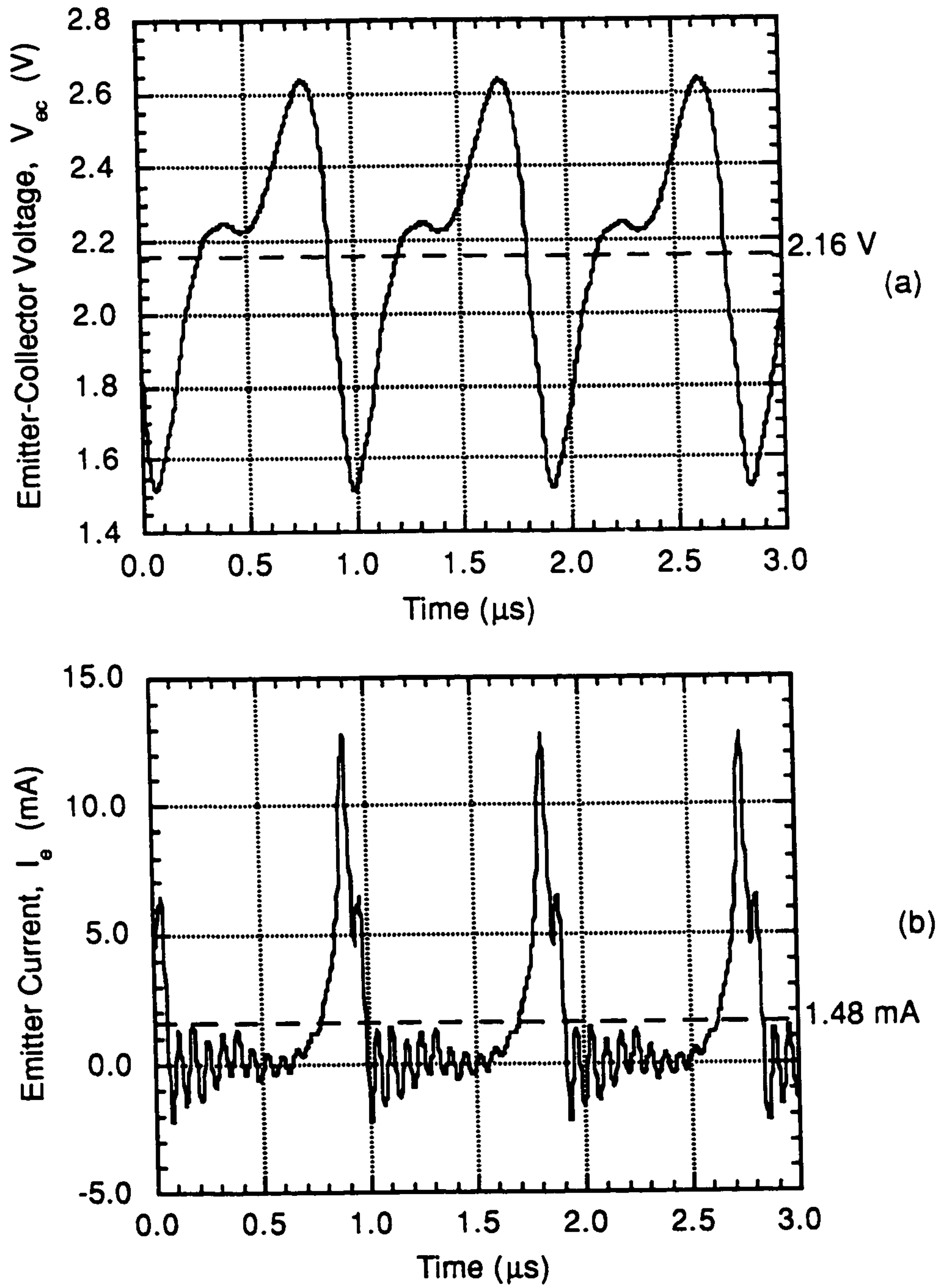


***Figure 6.6:** Time dependent a) voltage and b) current waveforms of the DOES device biased in the NDR regime of operation. (DC bias applied: $I_e = 1.50$ mA, $V_{ce} = 2.24$ V)*

with the DC voltage and currents measured by the SMU. Since the duty cycle for the current pulses is small, the device is subjected to current spikes with magnitudes in excess of 13 mA. Exposure of the device to these large current spikes stresses the device and may cause it to degrade with time. As I_e increases through the NDR region, the shape and magnitudes of the voltage and current waveforms remain the same. However, the oscillation frequency increases in a manner that allows the time averaged I-V of Fig. 6.3 to be swept out.

6.3. EFFECT OF STRUCTURAL PARAMETERS AND SIZE

Table 6.1 presents the layer description of the operational layers within the devices structures. It is a condensed version of the detailed structural parameters listed in Table 5.1. The effect of device structure on V_{sw} and I_{sw} of 80 x 80 μm^2 DOES devices is presented in Table 6.2. Each result represents an average of four 80 x 80 μm^2 devices. Structures S1602, S1603 and S1604 show the V_{sw} increasing with decreasing active layer doping and is in agreement with the modeling results of Chap. 2. The trend between S1601 and S1604 indicates that the switching voltage decreases as the emitter doping decreases, which is in contradiction with the modeling results. As discussed in Chap. 2, the operation of the device, especially the switching point is established by a delicate balance between the net recombination current components and the diffusion-thermionic current components. The relative magnitudes of these current components can be affected by material quality during the structure growth, as well as changes to the material during the fabrication process. It is conceivable that this anomaly is related to material growth or fabrication.

***Table 6.1:** Simplified device structures used in this project. See Table 5.1 for complete device structures.*

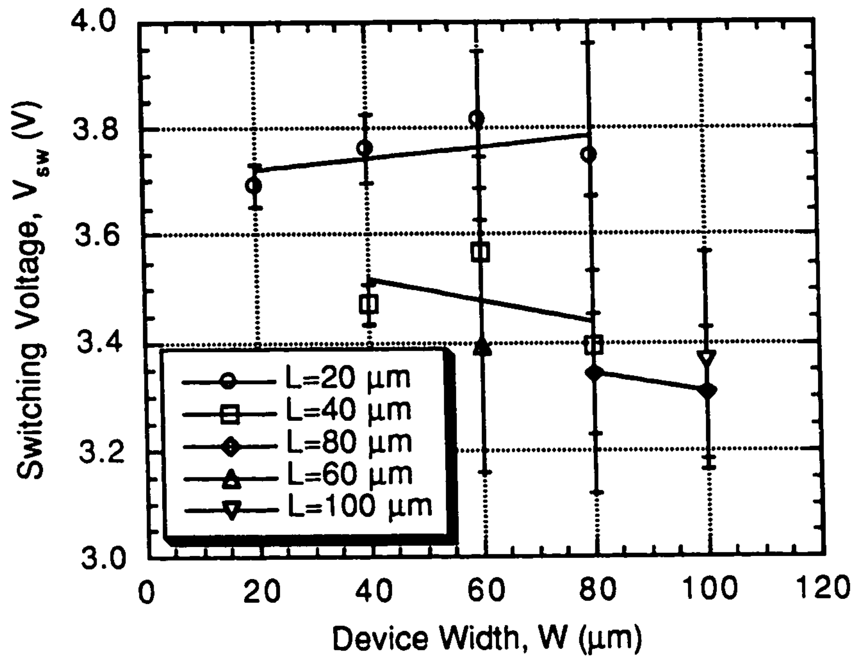
Layer Description & Composition	Layer Thickness (Å)	Device Structure Doping Concentration (cm^{-3})			
		S1601	S1602	S1603	S1604
Emitter InP	2000	Zn: $1x10^{17}$	Zn: $5x10^{17}$	Zn: $5x10^{17}$	Zn: $5x10^{17}$
Charge Sheet InP	100	Si: $5x10^{18}$	Si: $5x10^{18}$	Si: $5x10^{18}$	Si: $5x10^{18}$
Voltage Drop InGaAsP (λ=1.3μm)	2000	N/A	N/A	Zn: $6x10^{15}$	N/A
Active InGaAsP (λ=1.3μm)	5000	Zn: $1x10^{17}$	Zn: $5x10^{17}$	Zn: $1x10^{17}$	Zn: $1x10^{17}$
Collector InP	2000	Si: $2x10^{17}$	Si: $2x10^{17}$	Si: $2x10^{17}$	Si: $2x10^{17}$

***Table 6.2:** Influence of device structure on the switching voltage and switching current.*

Device Structure	Switching Point	
	Voltage (V)	Current (μA)
S1601	3.36 ± 0.15	187 ± 48
S1602	3.86 ± 0.11	550 ± 62
S1603	7.39 ± 0.46	216 ± 27
S1604	5.02 ± 0.21	488 ± 36

Figures 6.7(a) and (b) show the switching voltage and current as a function of the device size. Each result is an average from four similar-sized devices on S1601. The results indicate that V_{sw} and switching current density (J_{sw}) decreases as L increases. Furthermore, among devices with equal lengths, J_{sw} decreases as W increases. These results indicate for devices with L < 80 µm or W < 80 µm, recombination associated with the edges of the mesa is a dominating influence on the switching characteristic. In this case, the surface recombination removes carriers which are close to the edge of the mesa eliminating them from participation in DOES device conduction. This effect is deleterious to device performance and must be reduced by further examination and optimization of the device fabrication process. Possible device fabrication processes which could be responsible for the generation of the surface states include the high-temperature implant-activation annealing, reactive-ion etching, CVD oxide growth and O_2 plasma treatments.

For devices with dimensions L ≥ 80 µm and W ≥ 80 µm, the bulk effect dominates and establishes the switching character of the device. In this case, the switching point is relatively independent of size with $V_{sw} \approx 3.35$ V and $J_{sw} \approx 2$ A/cm^2.



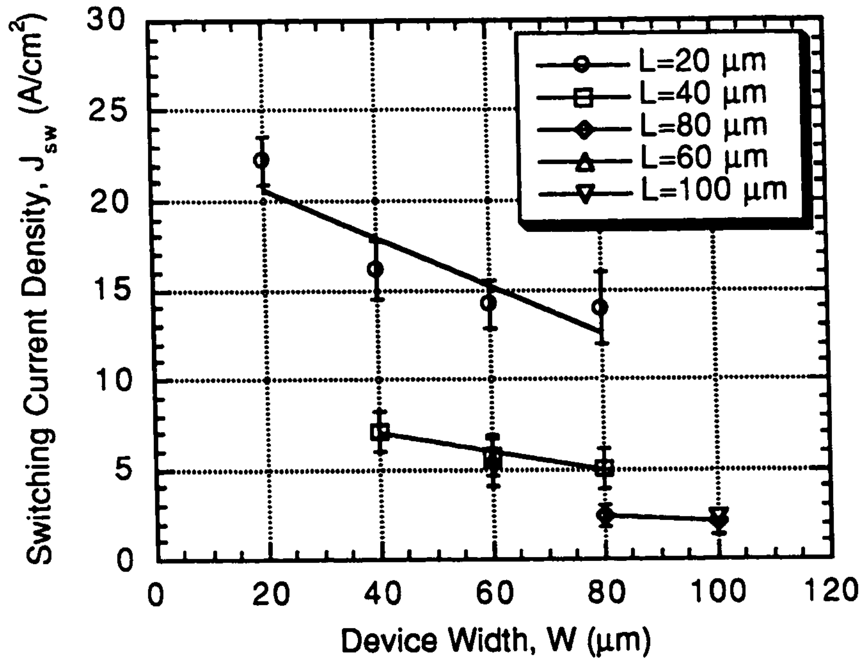


***Figure 6.7:** a) Switching voltage and b) switching current density of the DOES as a function of device width (W) and device length (L).*

6.4. FOUR-TERMINAL DEVICE OPERATION

6.4.1. Effect of Inversion Channel Current

Figures 6.8(a) and (b) illustrate the I-V characteristics with the inversion channel contact current (I_i) as the parametric variable. In this figure, I_i is negative because electrons are being injected into the inversion-channel contact and therefore, current flow is directed out of the contact. This figure shows that I_i strongly influences the operation of the device in the OFF and NDR states where $J_e < J_h$. This is demonstrated by an increase in the OFF state current, and a decrease in V_{sw}, as I_i decreases: V_{sw} = 3.16, 2.86, 2.60 and 2.40 V for I_i = 0, -0.18, -0.44 and -1.00 mA. I_i does not significantly influence the operation of the device in the ON state, where $J_e > J_h$, as there is no change in V_h, and in the ON state characteristics, with I_i. These experimental results are in agreement with the modeling results of Fig. 2.10.

The series of plots Figs. 6.9(a–c) illustrate the effect of I_i on V_{ei}, V_{ai} and V_{ac}. In the region of operation where $I_e > -I_i$, I_i does not change the I-V character of the e-i and a-c junctions. However, I_i does significantly affect the operation of the a-i junction. As I_i decreases, there is a reduction in the maximum reversed bias voltage across the a-i junction ($\hat{V}_{ai}$): $\hat{V}_{ai}$ = -0.73, -0.39 and -0.10 V for I_i = 0, -0.18 and -0.44 mA. This results in the reduction of V_{sw} with decreasing I_i. These experimental results are in agreement with the modeling results of Fig. 2.11. Figures 6.9(b) and (c) also show that when $I_e < -I_i$, the a-i junction is forward bias and the a-c junction is reversed bias. As I_i increases, V_{ai} increases and V_{ac} decreases. When $I_e < -I_i$, the barrier to electrons flowing towards the emitter is

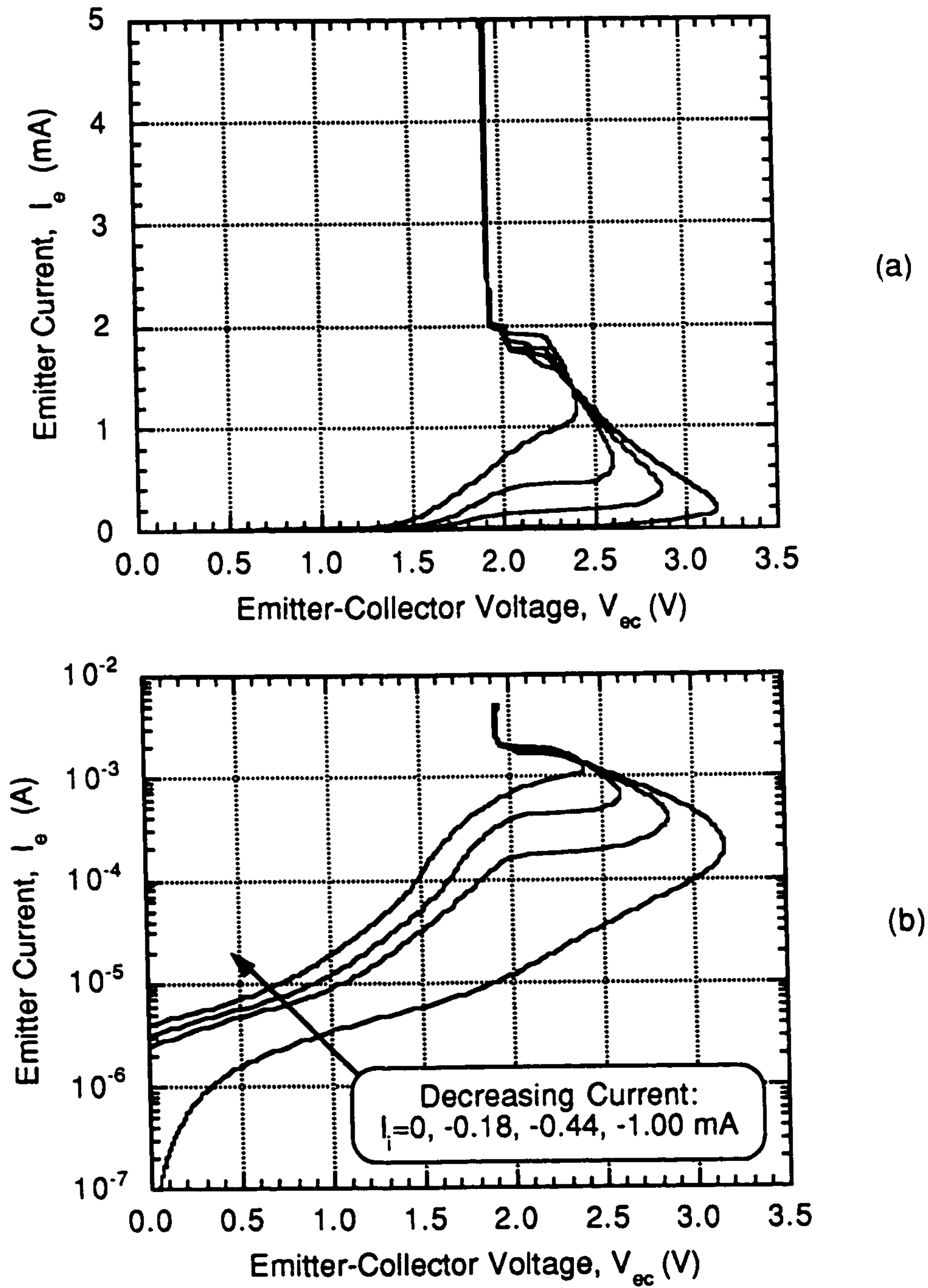
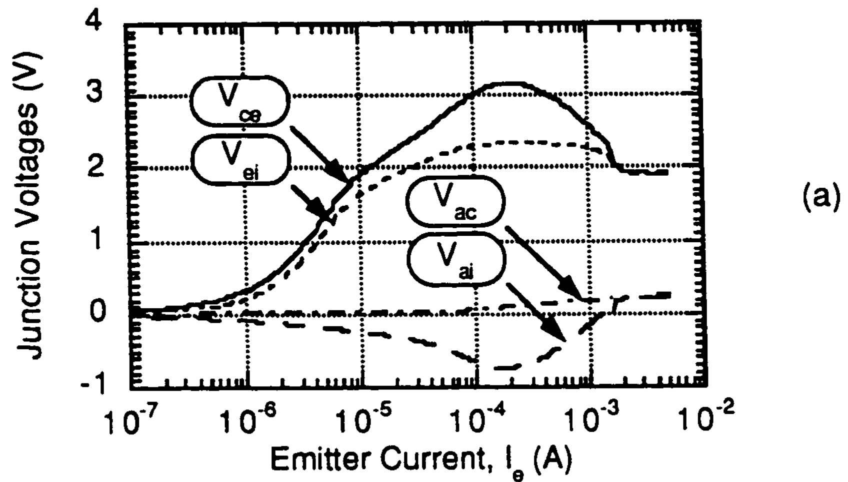
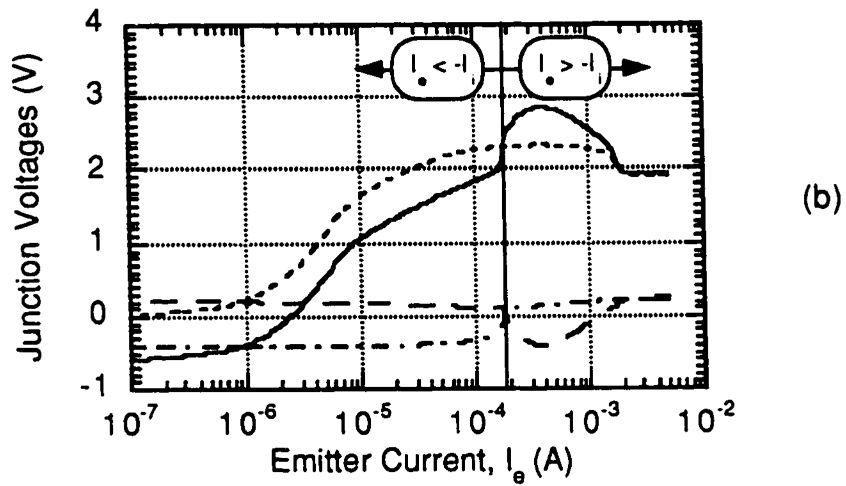


***Figure 6.8:** a) Linear and b) logarithmic I-V characteristics of the DOES device with the inversion channel current as the parametric variable.*





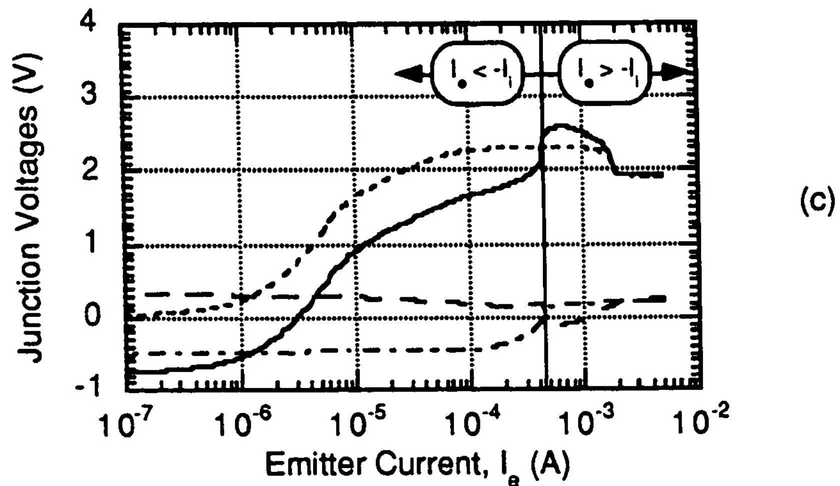


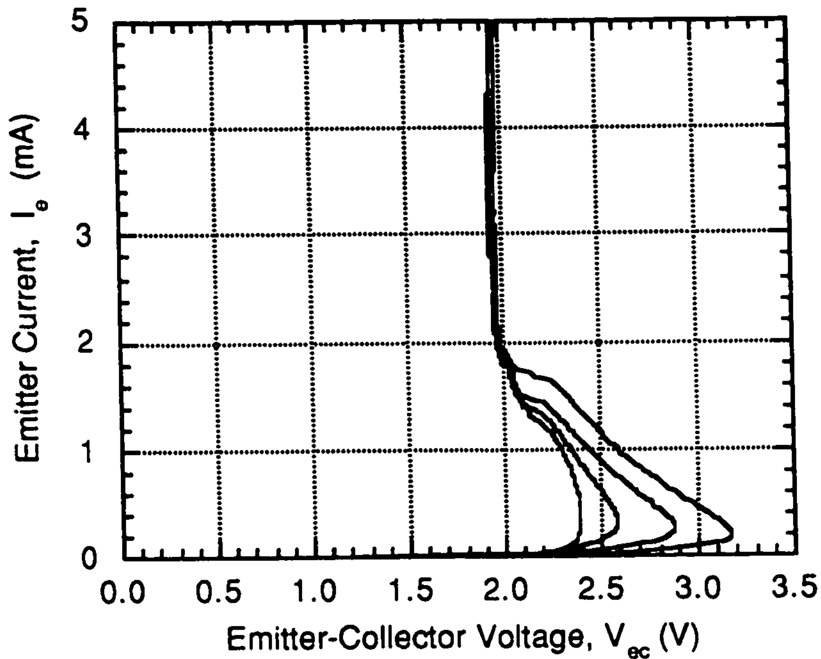
Figure 6.9: *Voltage across the e-i, a-i and a-c junctions as a function of I_e for a) $I_i = 0$ μA, b) $I_i = -180$ μA and c) $I_i = -440$ μA.*

greater than that for electrons flowing towards the collector. As a result, the majority of injected electrons flow from the inversion channel, across the active layer to the collector. This carrier flow forward biases the a-i junction and reverse biases the a-c junction.

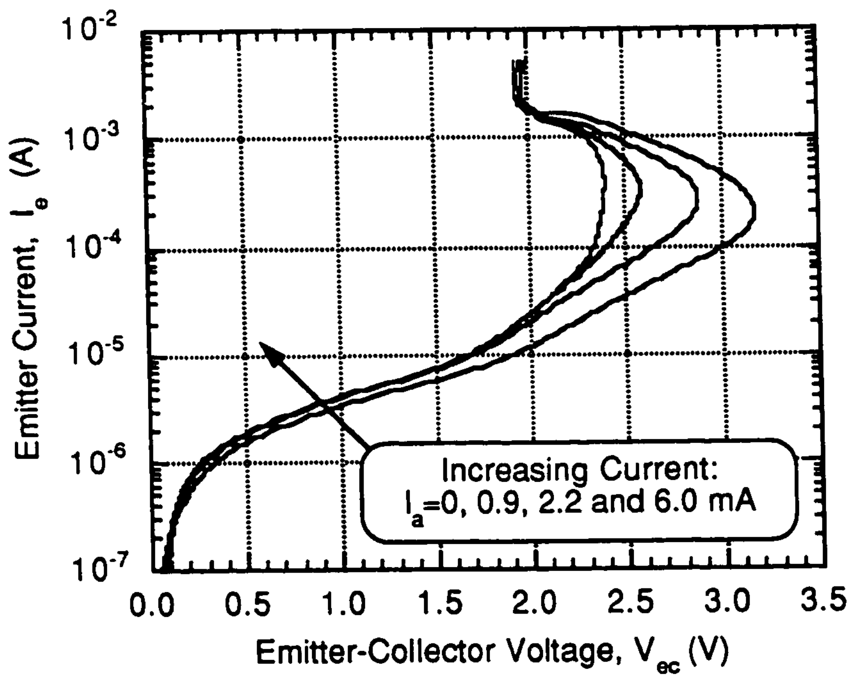
6.4.2. Effect of Active Layer Current

Figures 6.10(a) and (b) show a family of J-V curves with the active layer contact current (I_a) as the parametric variable. A positive value of I_a indicates that holes are being injected into the neutral portion of the active layer. The figure shows that I_a significantly influences the device in the OFF and NDR states, where $I_e < I_h$. As I_a increases, the OFF state current density increases and V_{sw} decreases: V_{sw} = 3.17, 2.88, 2.58 and 2.40 V for I_a =0, 0.9, 2.2 and 6.0 mA. I_a has little influence on the operation of the device in the ON state, where $I_e > I_h$, as there is no significant change in V_h, and in the ON state characteristics, with I_a. These experimental results are in agreement with the modeling results of Fig. 2.12.

The series of plots Figs. 6.11(a–c) illustrate the effect of I_a on V_{ei}, V_{ai} and V_{ac}. I_i does not affect the I-V character of the e-i junction but significantly affects the operation of the a-i and a-c junctions. The figures show that I_a forward biases the a-c junction and that V_{ac} increases as I_a increases. As I_a increases, there is a reduction in $\hat{V}_{ai}$: $\hat{V}_{ai}$ = -0.73, -0.13 and 0.49 V for I_i = 0, 0.5 and -3.0 mA. This results in the reduction of V_{sw} with increasing I_a. These experimental results are in agreement with the modeling results of Fig. 2.13.



(a)



(b)

***Figure 6.10:** a) Linear and b) logarithmic I-V characteristic the DOES device with active layer current as the parametric variable.*

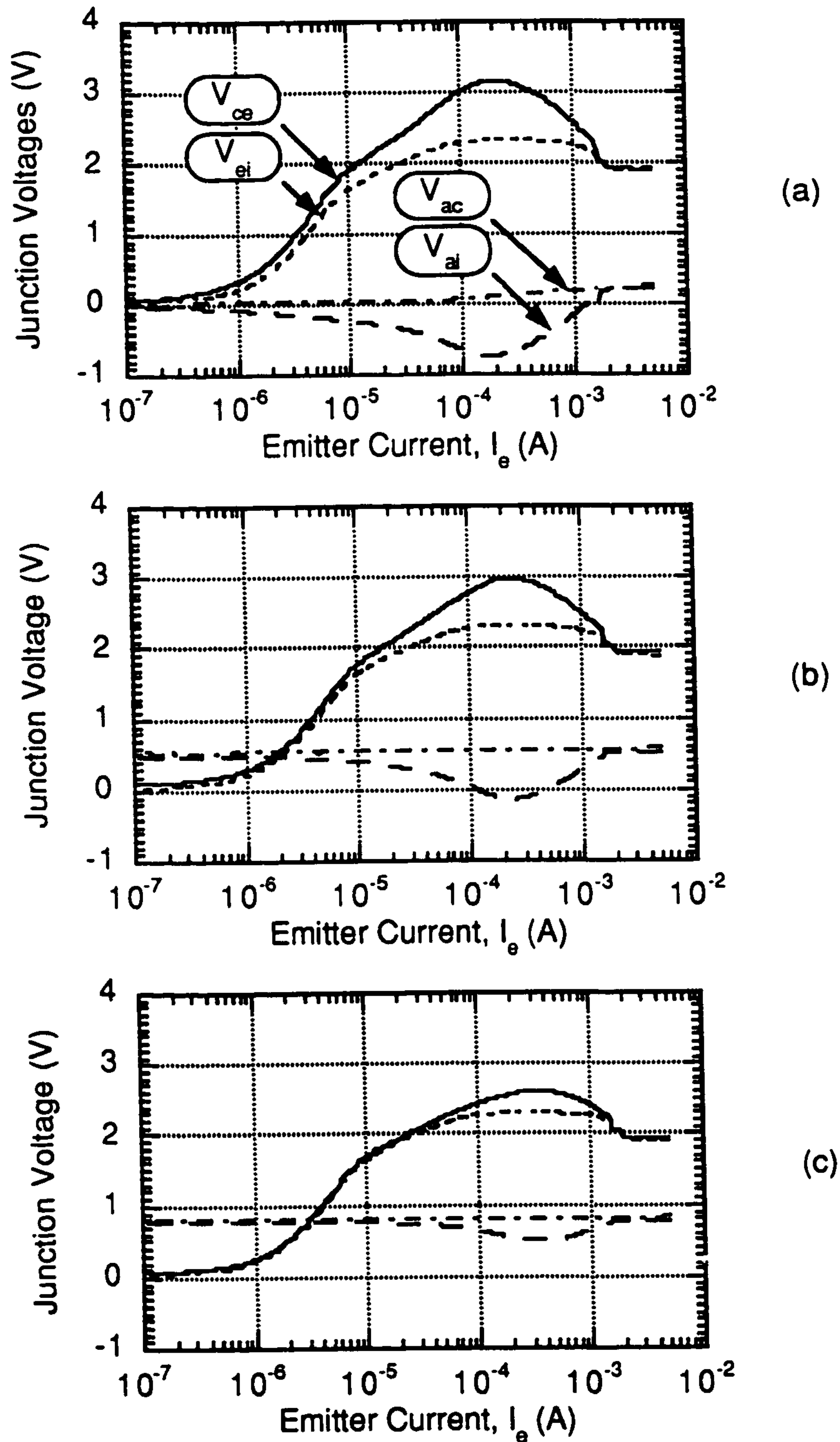


***Figure 6.11:** Voltage across the e-i, a-i and a-c junction as a function of I_e for a) $I_a = 0$ μA, b) $I_a = 0.5$ mA and c) $I_a = 3.0$ mA.*

6.4.3. Summary of Current Injection

Figure 6.12 shows the effect of I_i and I_a on V_{sw}. This figure shows that V_{sw} decreases when I_a increases or as I_i decreases. The figure also shows that I_i is more effective at reducing V_{sw} than is I_a. This is in agreement with the predictions made by the model in Chap. 2, see Fig. 2.14. Aside for the reasons cited in Chap. 2, the higher efficiency of the inversion channel injection over active layer injection in changing V_{sw} is further enhanced by the relative placements of the inversion channel and active layer contacts to the emitter mesa. In the device configuration used, the distance between the edge of the inversion channel contact to the edge of the emitter mesa is about 2000 Å. The separation between the active layer contact to the edge of the emitter mesa is approximately 20 µm. This separation represents the distance over which carriers must diffuse

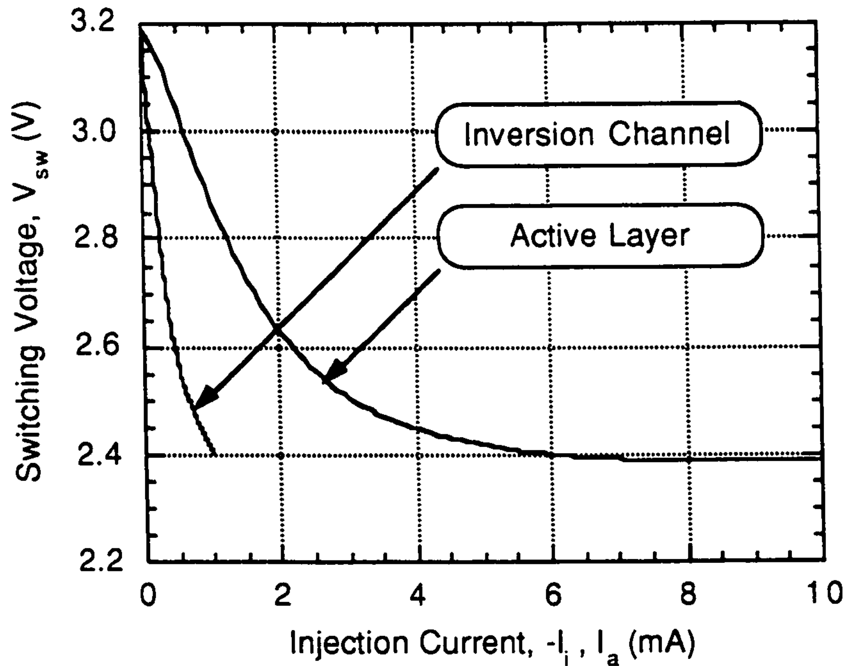


Figure 6.12: Switching voltage as a function of inversion channel and active layer current. Summary of Figs. 6.8 and 6.10.

before they arrive under the mesa and begin contributing to the current-feedback loop. Since the carriers injected into the active contact must diffuse over a larger distance, more of them will be lost to recombination before arriving under the mesa.

6.5. OPTICAL CHARACTERISTICS

The electrical and optical measurements reported in this section were performed on DOES devices with a window in the emitter contact metal. The devices used in this experiment had a 40 x 100 μm^2 emitter mesa and a window in the emitter contact metal of 20 x 80 μm^2. These devices were fabricated on wafer S1601.

6.5.1. L-I Characteristics

Figure 6.13 illustrates the normalized light-voltage (L-V) characteristics for the DOES device. In the OFF state, there is very little optical emission from the device and the optical signal collected in this regime of operation is dominated by noise. In the ON state, the optical emission from the device increases essentially linearly with I_e. High levels of optical emission from the DOES are measured while the device is biased in the NDR region of operation. The apparent enhancement of the optical emission within the NDR region of operation is a result of the voltage and current oscillations as discussed in Sect. 6.4.

From the I-V characteristic of Fig. 6.13 it is seen that $V_{SW} = 3.6$ V, $I_{SW} = 2.2$ mA and $J_{SW} = 55$ mA/cm^2. These voltages and currents are abnormally high because the thin highly doped InGaAs-emitter layer was unintentionally

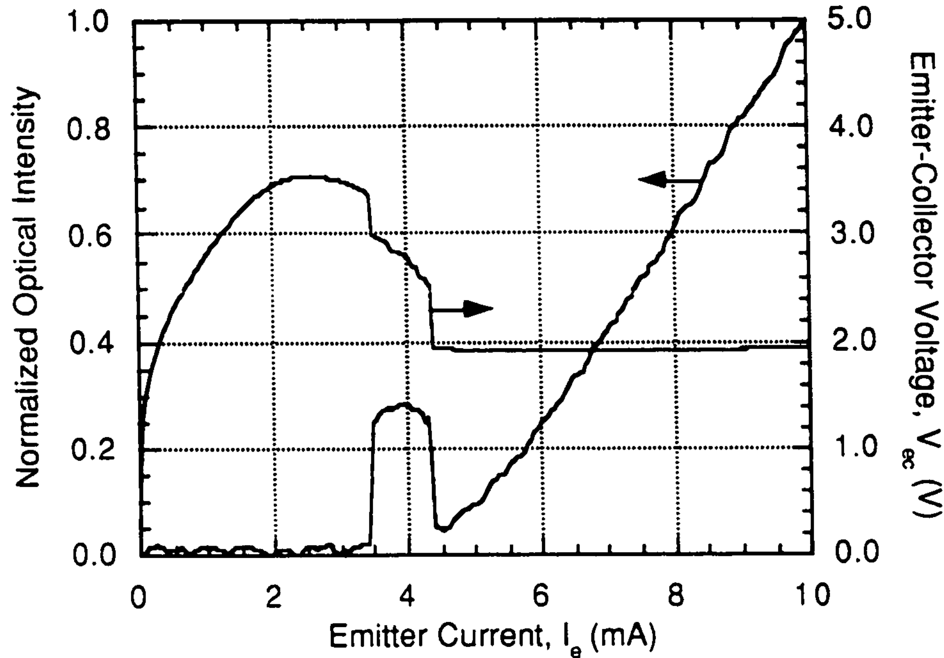


Figure 6.13: Light-current (L-I) characteristic of the DOES. Superimposed is the I-V characteristic of the device.

removed during device processing. Thus, contact to the emitter is made primarily about the ring contact and, consequently, higher currents must be used to achieve the switching condition. Future device designs should incorporate a thicker InGaAs emitter contact layer. The tradeoff when using a thicker InGaAs emitter contact layer is that a larger fraction of light will be absorbed by this layer.

Figure 6.14 shows V_{ei}, V_{ai} and V_{ac} as a function of I_e. These characteristics are similar to those presented in Fig. 6.4. In the OFF state, when $I_e < 2.2$ mA, the e-i and a-c junctions are in forward bias, and the a-i junction is in reverse bias. Optical emission from the device is negligible in this state of operation, indicating that emissions from the e-i and a-c junctions are negligible. In the ON state, the a-i junction is in forward bias and the optical emission increases

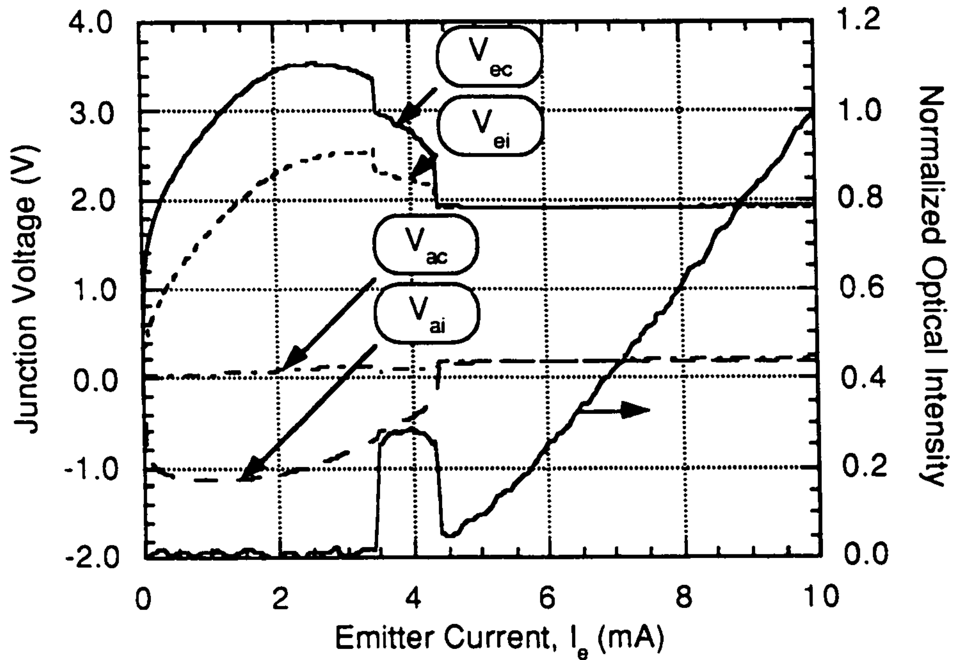


Figure 6.14: Voltage across the e-i, a-i and a-c junctions and the optical emission from the device as a function of I_e.

linearly. This suggests that the optical emission is generated primarily from electron-hole pair recombination in the forward biased a-i junction. These recombination events occur across the InGaAsP active layer and generate optical emissions that are centered about $\lambda = 1.3$ μm. The general trends of the L-I curve exhibited by the device match those predicted by the device model of Chap. 2, as shown in Fig. 2.9.

6.5.2. Effect of Optical Injection

Figure 6.15 illustrates a family of I-V curves with the incident optical flux (Φ), at $\lambda = 1.3$ μm, as the parametric variable. The figure shows that Φ significantly influences the device in the OFF and NDR states, where $I_e < I_h$. As Φ increases, the OFF state current increases and V_{SW} decreases: V_{SW} = 3.47, 3.27,

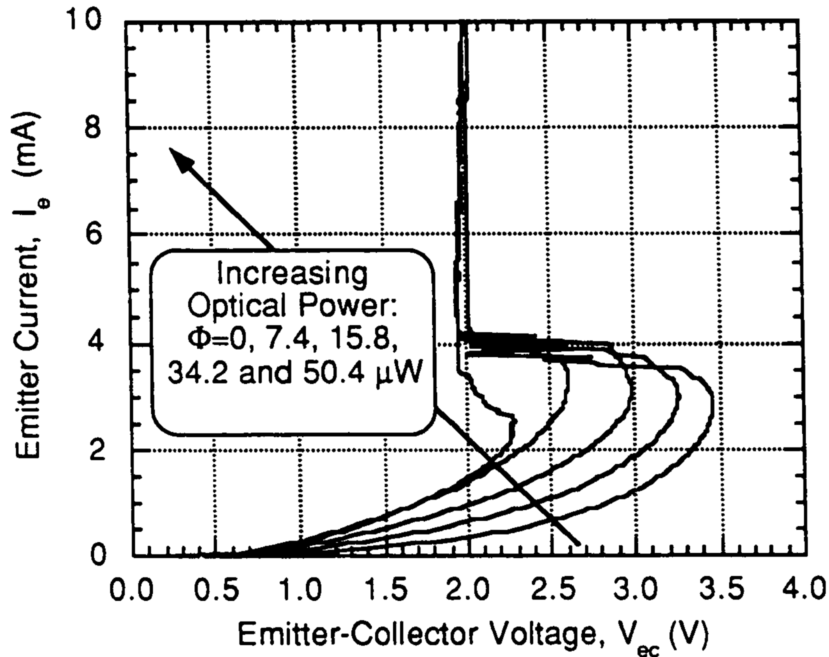


Figure 6.15: *Linear I-V characteristic of the DOES device with incident optical power (Φ)at λ = 1.3 μm as the parametric variable.*

2.99, 2.61 and 2.28 V for Φ = 0, 7.4, 15.8, 34.2 and 50.4 μW respectively. Φ has little influence on the operation of the device in the ON state, where $I_e > I_h$, as there is no significant change in the ON state characteristic, and in V_h, with Φ. These experimental results are in agreement with the modeling results of Fig. 2.15.

Figure 6.16 summarizes the results of Fig. 6.15 by showing the influence of Φ on V_{sw}. This figure shows that V_{sw} decreases rapidly with Φ, for Φ < 50 μW, but tends to saturate at 2.2 V for Φ > 50 μW.

The series of plots Figs. 6.17(a–c) illustrate the effect of Φ on the voltages across the e-i, a-i and a-c junctions of the device. It shows that Φ does not change the J-V character of the e-i and a-c junctions but significantly affects the operation of the a-i junction. Light of λ = 1.3 μm incident on the device results in the photo-generation of electron and hole pairs in the InGaAsP active layer of the DOES.

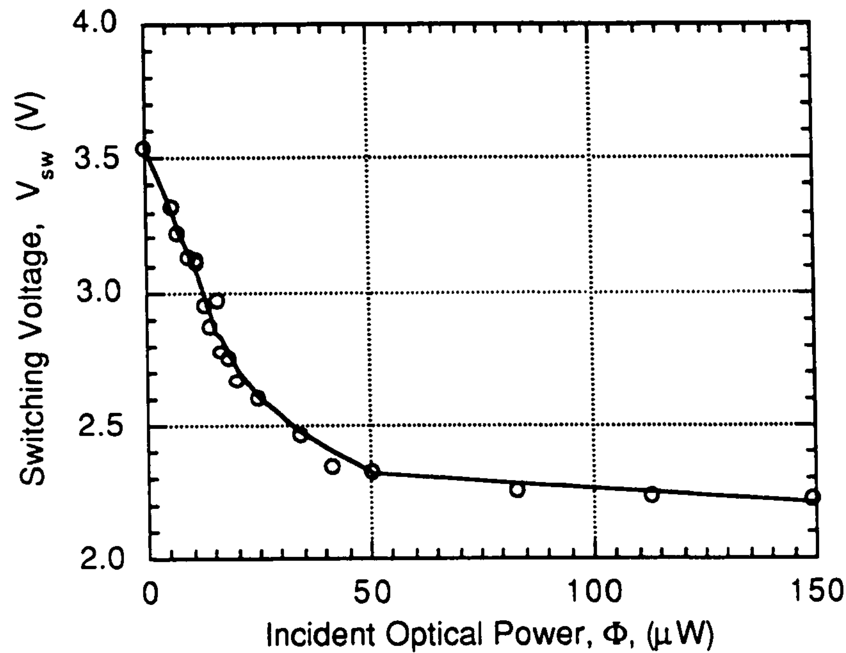


Figure 6.16: Switching voltage as a function of the incident optical power, Φ (λ = 1.3 μm).

The holes and electrons which are generated within the depletion region of the e-i junction are swept out by the field and adds to the internal current flows by supplementing the thermal generation of current in the a-i junction. As Φ increases the maximum of reverse bias across the a-i junction ($\hat{V}_{ai}$) decreases: $\hat{V}_{ai}$ = -1.049, -0.38 and 0.05 V for $\hat{V}_{ai}$ = 0, 7.4 and 34.2 μW. This in turn results in a reduction in the switching voltage of the device. These experimental results are in agreement with the modeling results of Fig. 2.17.

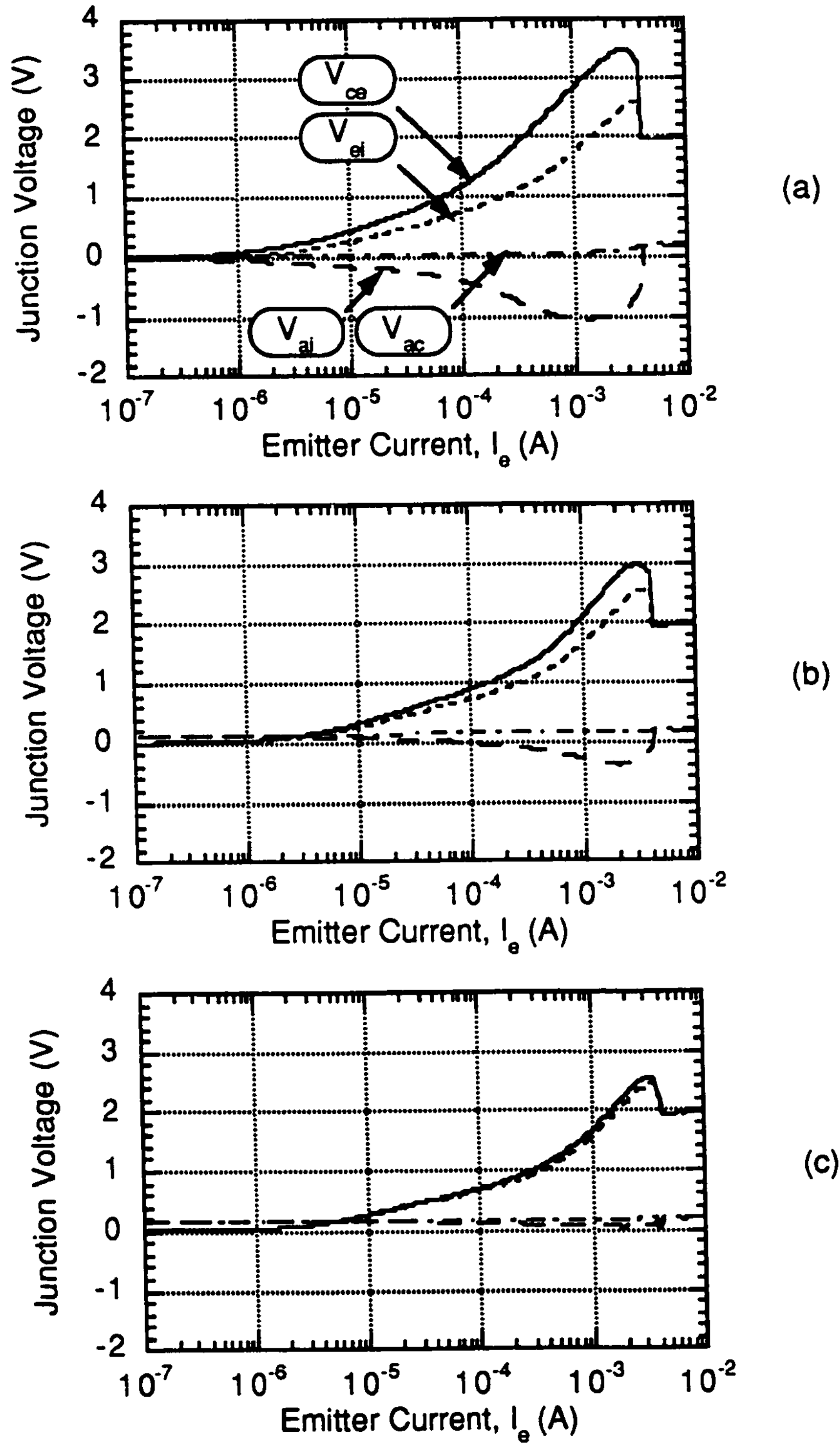


***Figure 6.17:** Voltages across the e-i, a-i and a-c junctions as a function of I_e with a) $\Phi = 0$ μW, b) $\Phi = 7.4$ μW and c) $\Phi = 34.2$ μW.*

CHAPTER 7

EXPERIMENTAL CHARACTERIZATION OF THE HFET

This chapter demonstrates the operation of the n-channel InGaAsP-InP based heterojunction field-effect transistor (HFET). The chapter begins with a detail characterization of the input, output and transfer characteristics of HFETs from wafer S1603. The influence of device structure and size on the output and transfer characteristics of the HFETs is then presented and examined. Throughout the chapter, comparisons are made between the experimental and theoretical results.

7.1 EXPERIMENTAL SETUP AND BIASING

Electrical characterization of the HFET was performed with the Hewlett-Packard Parameter Analyzer (HP4145B) and the probe station described in Chap. 6, Sect. 6.1. In all measurements, the probe station was covered to minimize the amount of ambient light incident on the devices. The HFET was biased by connecting source-measure units (SMU) to the gate, source and drain contacts; and configuring the SMUs to source voltage to the contacts and measure current flows from the contacts. The HFET was biased in the common-source circuit

configuration by connecting the input circuit across the gate-source contacts and the output circuit across the drain-source contacts. In this configuration, the source contact was biased at ground potential and the drain was positively biased relative to the source. This bias establishes a reversed bias condition at the p-n junction formed by the n-type implanted drain contact and the active layer, forcing electrons from the source to flow through the inversion-channel towards the drain and not through the active layer. The gate was biased both positively and negatively relative to the source, but limited to voltages where the magnitude of the gate current was below 100 μA. The biasing condition used in this experiment is typical for characterizing common-source field-effect transistor devices (MOSFET's, HEMT's and MESFET's) [1].

7.2 INPUT CHARACTERISTICS

Figure 7.1 shows the input current-voltage characteristics (I_{gs}-V_{gs}) of a 6 x 100 μm^2 HFET on S1603. This measurement examines the operation of the p-n junction formed by the gate and inversion channel, and is performed by grounding both the source and drain contacts, and biasing the gate contact. The g-s junction is forward biased when $V_{gs} > 0$ and reversed biased when $V_{gs} < 0$. In reverse bias, I_{gs} increases slowly as V_{gs} decreases: I_{gs} = -1 μA at V_{gs} = -2 V and increases to -2.8 μA at V_{gs} = -10 V. The forward bias characteristics of the HFET between the source and gate resembles the OFF state of the DOES I-V characteristic (see Fig. 6.3). This high resistance behaviour results from the existence of parallel conduction paths between the gate and source contacts, as discussed in Sect. 6.2.2. As a result of the high resistance in the forward bias

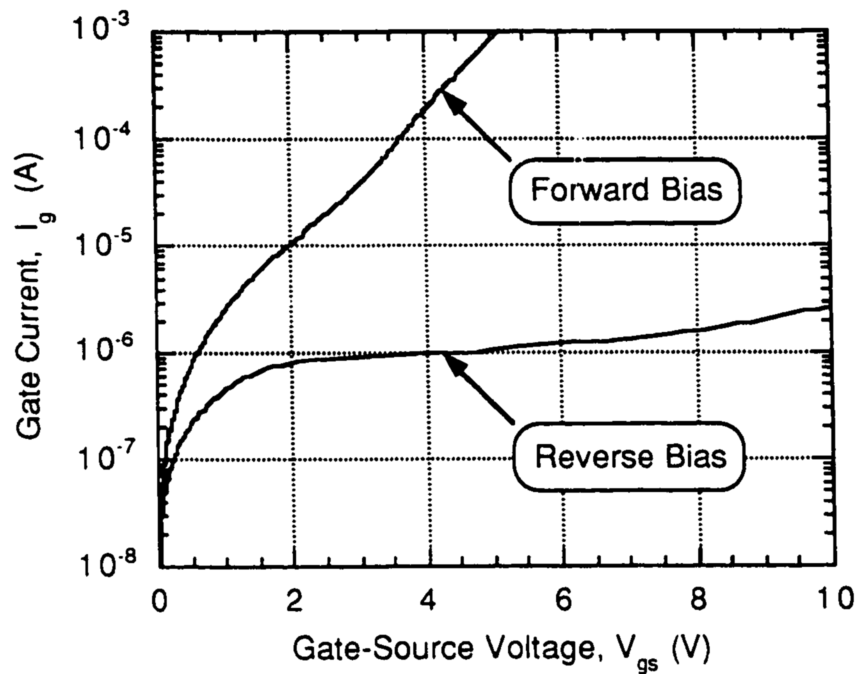


Figure 7.1: The input characteristics (I_g-V_{gs}) of the 6 x 100 μm^2 HFET.

region, relatively large positive biases can be applied across the gate and source contact with little resulting gate current flow.

7.3 OUTPUT CHARACTERISTICS

In the following sections, the output characteristic of a 6 x 100 μm^2 HFET on wafer S1603 is presented. These results are representative of other HFETs on S1603.

7.3.1 Drain Current Characteristics (I_d-V_{ds})

Figure 7.2 shows the I_d-V_{ds} characteristics of the HFET with V_{gs} as the parametric variable. The I_d-V_{ds} characteristic is divided into the sub-threshold, linear and saturation region of operation by the threshold voltage (V_t) and the

saturation drain-source voltage ($V_{ds,sat}$): V_t = -1 V and $V_{ds,sat}$ = 1.5, 1.3, 1.1, 0.8 and 0.5 V for V_{gs} = 4, 3, 2, 1 and 0 V. The negative V_t indicates that this HFET is a depletion mode device and that there is an accumulation of electrons in the inversion channel when $V_{gs} = 0$.

In the linear region of operation, for $V_{gs} > V_t$ and $0 < V_{ds} < V_{ds,sat}$, I_d increases relatively linear with V_{ds}. This is expected as the channel is not pinched off and therefore, behaves as a resistor. In the saturation region of operation, for $V_{gs} > V_t$ and $V_{ds} \geq V_{ds,sat}$, I_d essentially saturates: I_d = 3.07, 2.39, 1.76, 1.10 and 0.49 mA for V_{gs} = 4, 3, 2, 1 and 0 V. In this case, the inversion channel is pinched off and most of the incremental V_{ds} drops across the pinched-off or depleted portion of the channel. The voltage drop across the inverted portion of the inversion channel remains essentially constant and hence, I_d saturates. In typical circuit applications, the HFET is biased in the saturation region of operation. For $V_{ds} > 7$ V, I_d begins to increase exponentially with V_{ds} as avalanche breakdown of the pinched-off inversion channel occurs. The output resistance associated with this device, biased in the saturation region, is characterized by the Early voltage*. The Early voltage for this HFET is 24.2, 11.9, 7.6, 3.6, and 2.0 V for V_{gs} = 4, 3, 2, 1 and 0 V respectively.

The sub-threshold region exists for $V_{gs} < V_t$. In this region of operation, the inversion channel is void of electrons, $Q_{ni} = 0$. As V_{ds} increases, electrons which are injected into the source contact must overcome the active layer-n^+ implant barrier, diffuse across the active layer to the drain contact. In this region of operation, carrier transport between the source and drain contacts closely resembles that between the emitter and collector of a long-base bipolar transistor.

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* The Early voltage is defined as the x-intercept of a linear fit to the saturated portion of the I_d-V_{ds} characteristic.

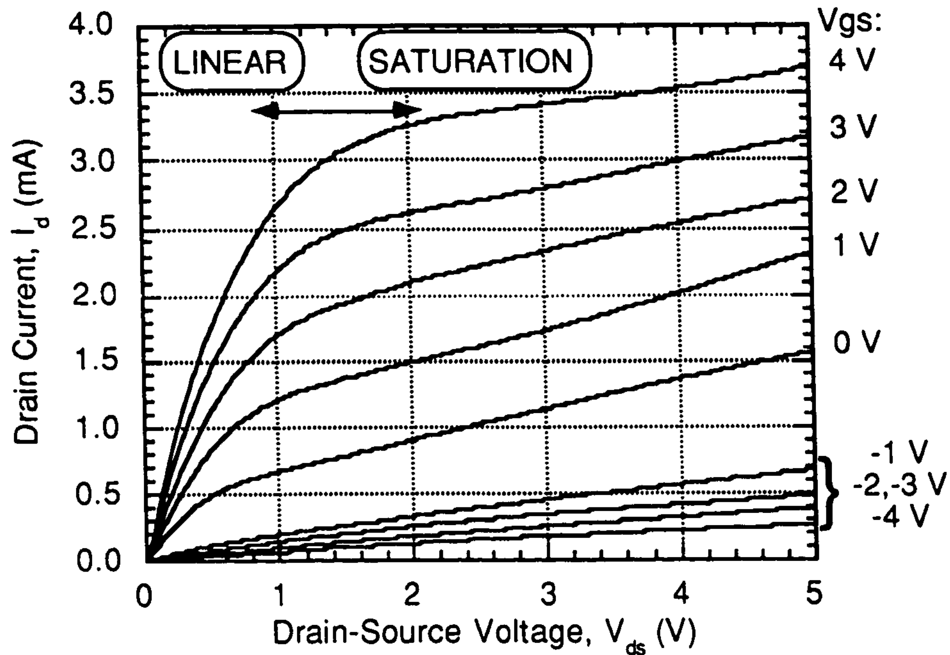


Figure 7.2: The output characteristics (I_d-V_{ds}) of the HFET with V_{gs} as the parametric variable.

The experimental I_d-V_{ds} characteristics closely match those predicted by the model of Chap. 3 which demonstrates the sub-threshold, linear and saturation regions of operation (see Fig. 3.7). The limitations of the model begins to show for $V_{gs} > V_t$ and $V_{ds} \geq V_{ds,sat}$ as the model assumes that I_d is constant but, experimentally, I_d increases with V_{ds}.

7.3.2 Gate Current Characteristics (I_g-V_{ds})

Figure 7.3 illustrates I_g as a function of V_{ds}. I_g is at a maximum when V_{ds} = 0 V and decreases to a saturation value of 3 µA for $V_{ds} \geq 1.5$ V. The V_{ds} which is applied is distributed along the length of the inversion-channel. At any point along the channel, the voltage drop across the gate to the inversion channel is defined as the channel voltage (V_c) where V_c = V_{gs} at the source end of the

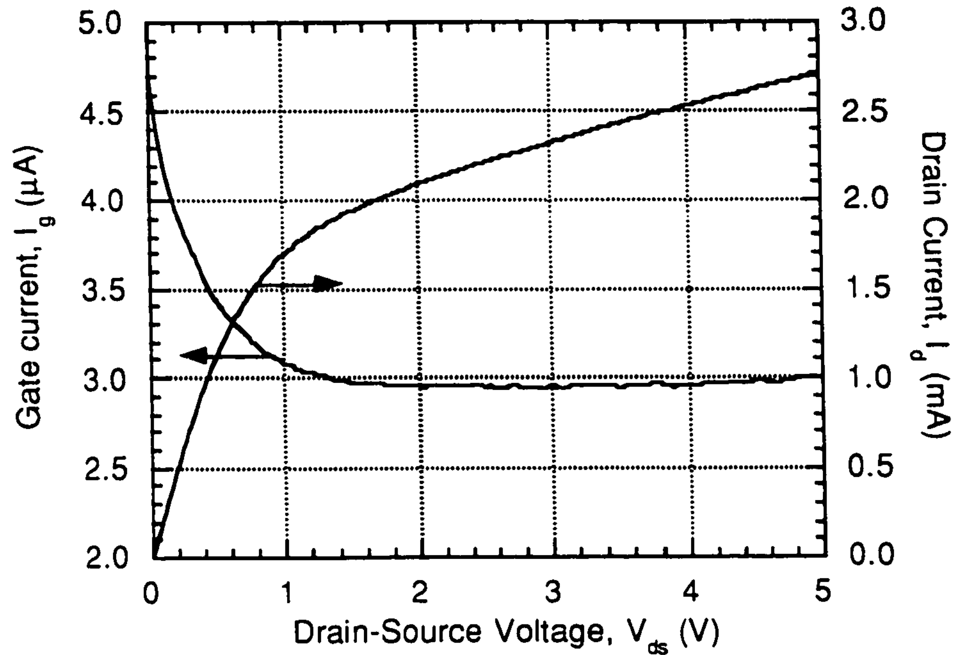


Figure 7.3: Gate leakage current (I_g) as a function of V_{ds} for $V_{gs} = 2$ V.

channel and $V_c = V_{gs} - V_{ds}$ at the drain end of the channel. As a result, the differential gate current which is a function of V_c is higher at the source end of the channel and lower at the drain end of the channel. The total gate current is the sum of all the gate current flows across the length of the channel. For $V_{ds} = 0$, V_{gs} is dropped across the entire channel and I_g is at a maximum. As V_{ds} increases V_c across the channel decreases. This in turn reduces the differential gate current flow and therefore, the total gate current. When $V_{ds} = V_{ds,sat}$, the channel is pinched off and most of the incremental V_{ds} drops across the pinched-off or depleted section of the channel. The voltage drop across the inverted portion of the inversion channel remains essentially constant for $V_{ds} \geq V_{ds,sat}$ and hence, I_g

saturates. This gate current, which represents a loss of electrons from the inversion channel, is small and represents between 0.1–0.2% of I_d.

7.3.3 Drain-Source Resistance Characteristics (R_{ds}-V_{ds})

Figure 7.4 shows the output resistance characteristics (R_{ds}-V_{ds}) for the HFET with V_{gs} as the parametric variable. In the sub-threshold region of operation, for $V_{gs} \leq V_t$, the channel is void of electrons and therefore, R_{ds} is relatively constant over V_{ds}: R_{ds} = 20, 15 and 12 kΩ for V_{gs} = -4, -3 and -2 V. The resistance across the source and drain contacts represents the resistance across the bulk active layer. In the linear region, for $V_{ds} < V_{ds,sat}$ and $V_{gs} \geq V_t$, the resistance increases exponentially with V_{ds}. This results because the application of V_{ds}, negates the biasing effect of V_{gs} on the inversion channel, results in a reduction of Q_{ni} across the channel. This decrease in channel conductance results in an increase in R_{ds} with V_{ds}. In the saturation region, for $V_{gs} \geq V_{ds,sat}$ and $V_{gs} \geq V_t$, R_{ds} is constant and is approximately 5 kΩ. In this region of operation, the inversion channel is pinched off at the drain end and R_{ds} is primarily the resistance of the pinched-off region. The resistance in the saturated region of operation is important as the device is typically biased to operate in this region.

7.4 TRANSFER CHARACTERISTICS

In the following sections, the output characteristic of a 6 x 100 μm^2 HFET on wafer S1603 will be presented. The results presented are representative of other HFETs on S1603.

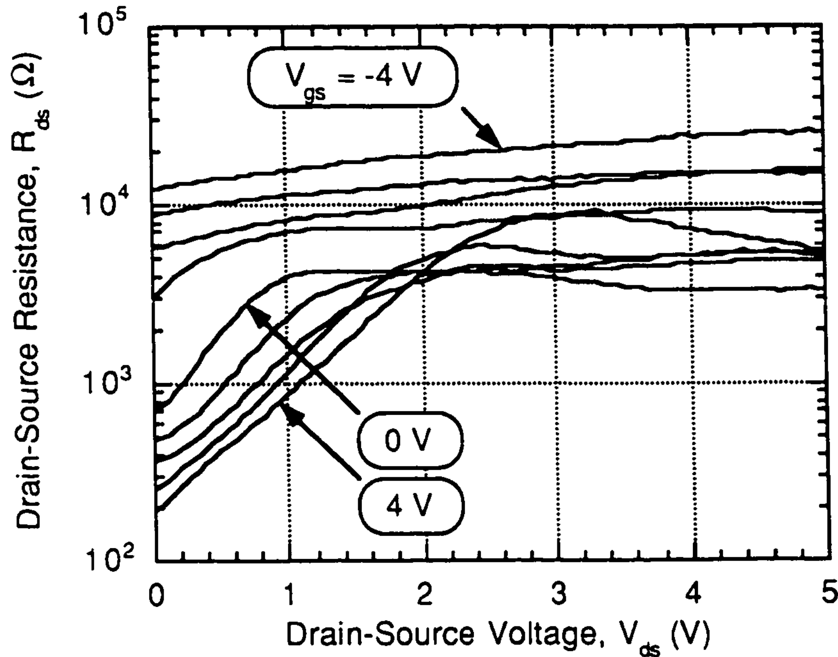


Figure 7.4: Output resistance of the HFET as a function of V_{ds} with V_{gs} as the parametric variable.

7.4.1 Drain Current Characteristics (I_d-V_{gs})

Figure 7.5 shows the I_d-V_{gs} characteristics of the HFET with V_{ds} as the parametric variable. When V_{ds} = 0 there is no applied electric field across the channel to direct electron flow and hence, I_d = 0. The small negative drain current, for V_{gs} > 2.5 V, results because V_{gs} causes electrons to flow from the inversion channel across the e-i junction to the gate contact.

The remaining transfer curves were all measured for $V_{ds} \geq 2$ V where the device biased in saturation region of operation. All these curves exhibit sub-threshold and saturation regions which are separated by the threshold voltage: V_t = -1.5, -1.4, -1.3 and -1.2 for V_{ds} = 5, 4, 3, and 2 V respectively. In the sub-threshold region, for $V_{gs} \leq V_t$, the are no electrons in the channel and current

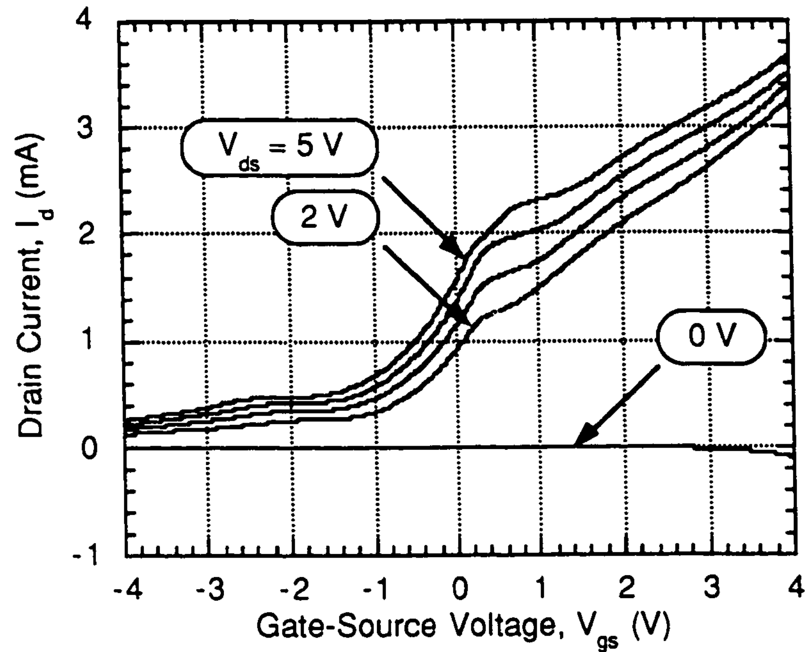


Figure 7.5: Transfer characteristic (I_d-V_{gs}) with V_{ds} as the parametric variable.

flow results from diffusion of electrons from the source to the drain. In this region, I_d is small and is independent of V_{gs}. For $V_{gs} > V_t$, there is an accumulation of electrons in the inversion channel which forms a low resistance path for current flow between the source and drain contacts. For $-1.3 < V_{gs} < 1$ V, I_d increases superlinearly with V_{gs} and represents the largest change in I_d with V_{gs}. For $V_{gs} > 1$ V, the I_d increases essentially linearly with V_{gs}. The transfer characteristics illustrate the effect of V_{gs} on I_d and also electron density in the channel.

7.4.2 Gate Current Characteristics (I_g-V_{gs})

Figure 7.6 shows I_g as a function of V_{gs} for V_{ds} = 2 V. The gate-source junction is reversed biased for $V_{gs} < 0$ and hence, I_g is small and negative. For V_{gs}

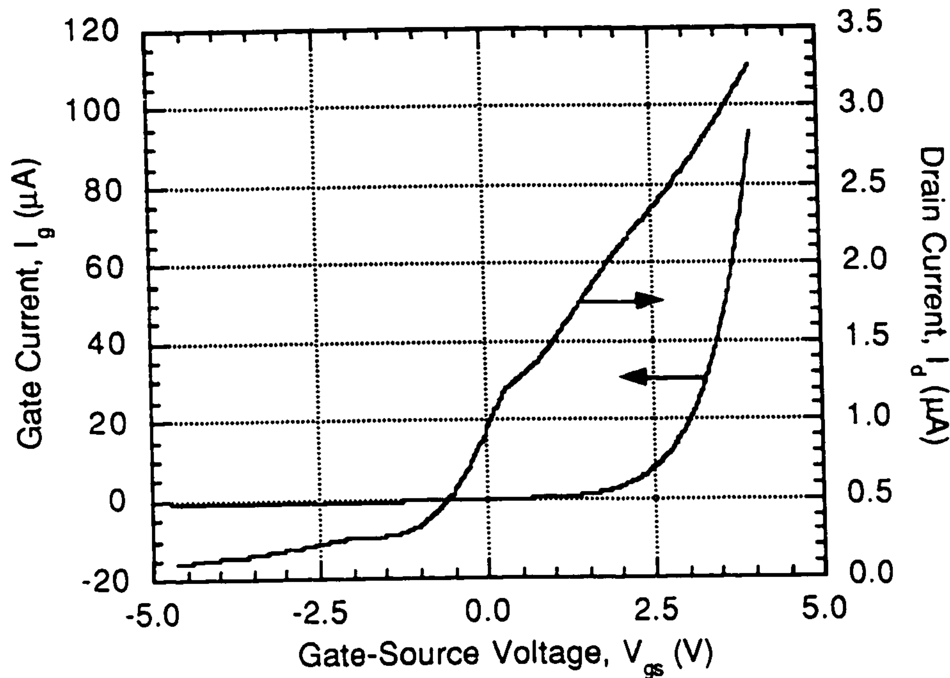


Figure 7.6: Gate leakage current of the HFET as a function of V_{gs} for V_{ds} = 2 V.

> 0 V, the e-i junction is forward bias and I_g increases exponentially with V_{gs}. The point of transition for I_d from increasing superlinearly to linearly with V_{gs} correspond approximately with the rapid increase in the I_g. The flow of I_g into the inversion channel reduces the electron density in the channel required to support the applied V_{gs} which in turn reduces the efficiency of V_{gs} in modulating the electron population within the inversion channel.

The model of Chap. 3, see Fig. 3.8, is only capable of predicting the transfer characteristic of the HFET in the region where gate leakage current does not play a significant role, $V_{gs} < 1$ V. In this region, the general shapes of the experimental and theoretical transfer characteristics are in good agreement. Since the model does not account for the effects of gate leakage current, it predicts that I_d continues to increase superlinearly with increasing V_{gs} for $V_{gs} > 1$ V.

7.4.3 Transconductance Characteristics (g_m-V_{gs})

Figure 7.7 illustrates the normalized transconductance of the HFETs. This characteristic is obtained by differentiating the transfer characteristics of the HFET and dividing by the width of the device (W)

$$g_m = \frac{1}{W}\frac{\partial I_d}{\partial V_{gs}} \tag{7.1}$$

The normalized transconductance quantifies the efficiency of V_{gs} in modulating I_{ds}. For V_{gs} < -2.0 V, where $V_{gs} < V_t$, g_m = 0 mS/mm. The transconductance increases superlinearly with V_{gs} for -2 V < V_{gs} < 0.2 V and peaks at the maximum transconductance ($g_{m,max}$) at V_{gs} ≈ 0.2V. With these devices, $g_{m,max}$ = 33.0, 30.0, 24.5 and 20.0 mS/mm for V_{ds} = 5, 4, 3 and 2 V respectively. In the voltage range for 0.2 V < V_{gs} < 0.8 V, g_m decreases sharply and then saturates at approximately 10 mS/mm, for V_{gs} > 1 V. The model of Chap. 3 is only capable of predicting the transfer characteristic of the HFET in the region where gate leakage current does not play a significant role, V_{gs} < 1 V (see Fig. 3.8). In this region, the general shapes of the experimental and theoretical transfer characteristics are in good agreement.

7.5 EFFECT OF STRUCTURAL PARAMETERS

A summary of the device structures listing only the operational layers of the HFET is presented in Table 7.21. Table 7.2 presents the effect of structural parameters on V_t maximum normalized transconductance ($g_{m,max}$) and saturation drain current ($I_{d,sat}$) of the HFETs. Each result represents the average and standard deviation from four different HFETs with gate length of L = 6 µm and W = 100 µm. The devices were biased in the saturation region of operation,

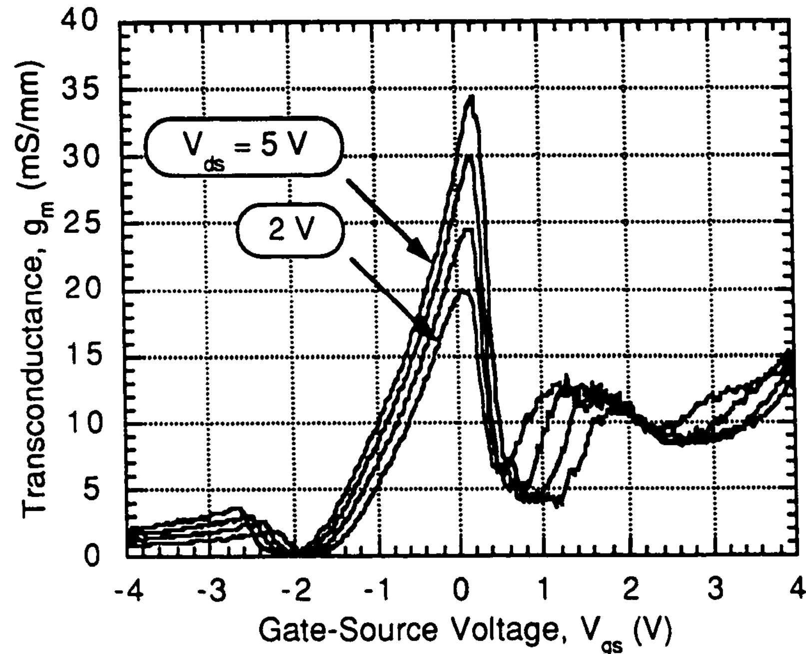


***Figure** 7.7: Normalized transconductance of the HFET as a function of V_{gs} with V_{ds} as the parametric variable.*

where $V_{ds} \geq V_{ds,sat}$, with V_{ds} = 1.5 V and 2.5 V. Results for structure S1602 are not available because contact to the inversion channel was not achieved and so, the HFETs were non-functional. V_t for all the structures were negative indicating that the HFETs fabricated were depletion mode devices.

A comparison of S1601 and S1604 shows that decreasing the emitter doping concentration results in a reduction in V_t and an increase in $g_{m,max}$ and I_d. A comparison of S1604 and S1603 shows that having an undoped layer results in a decrease in V_t, and an increase in $g_{m,max}$ and I_d. The effect of placing an undoped layer is equivalent to having a lightly doped active layer, which promotes a greater accumulation of electrons in the inversion channel and a higher effective channel mobility. These trends are in agreement with the predictions made by the model Chap. 3. These results indicate that decreasing

***Table 7.1:** Simplified device structural parameters of the four HFET devices. See Table 5.1 for complete device structural parameters.*

Layer Description & Composition	Layer Thickness (Å)	Device Structure Doping Concentration (cm^{-3})			
		S1601	S1602	S1603	S1604
Emitter InP	2000	Zn: $1x10^{17}$	Zn: $5x10^{17}$	Zn: $5x10^{17}$	Zn: $5x10^{17}$
Charge Sheet InP	100	Si: $5x10^{18}$	Si: $5x10^{18}$	Si: $5x10^{18}$	Si: $5x10^{18}$
Undoped InGaAsP (λ=1.3μm)	2000	N/A	N/A	Zn: $6x10^{15}$	N/A
Active InGaAsP (λ=1.3μm)	5000	Zn: $1x10^{17}$	Zn: $5x10^{17}$	Zn: $1x10^{17}$	Zn: $1x10^{17}$

***Table 7.2:** Influence of device structure on the threshold voltage (V_t), maximum transconductance ($g_{m,max}$) and saturation drain-source current (I_{ds}) of the HFETs.*

Structure	V_t (V)	V_{ds} = 1.5 V		V_{ds}= 2.5 V	
		g_m (max) mS/mm	I_d (V_{gs}=0) mA	g_m (max) mS/mm	I_d (V_{gs}=0) mA
S1601	-3.95 ± 0.49	20.3 ± 2.4	4.80 ± 0.33	26.8 ± 2.2	6.80 ± 0.41
S1603	-1.31 ± 0.34	25.8 ± 4.8	1.43 ± 0.05	28.8 ± 5.3	1.69 ± 0.07
S1604	-0.43 ± 0.09	18.4 ± 1.2	0.22 ± 0.02	19.3 ± 1.1	0.25 ± 0.02

N_e, N_a or adding a voltage drop layer will result in an increase in $g_{m,max}$ and I_d. However, the trade-off to the increases in $g_{m,max}$ and I_d is a more negative V_t.

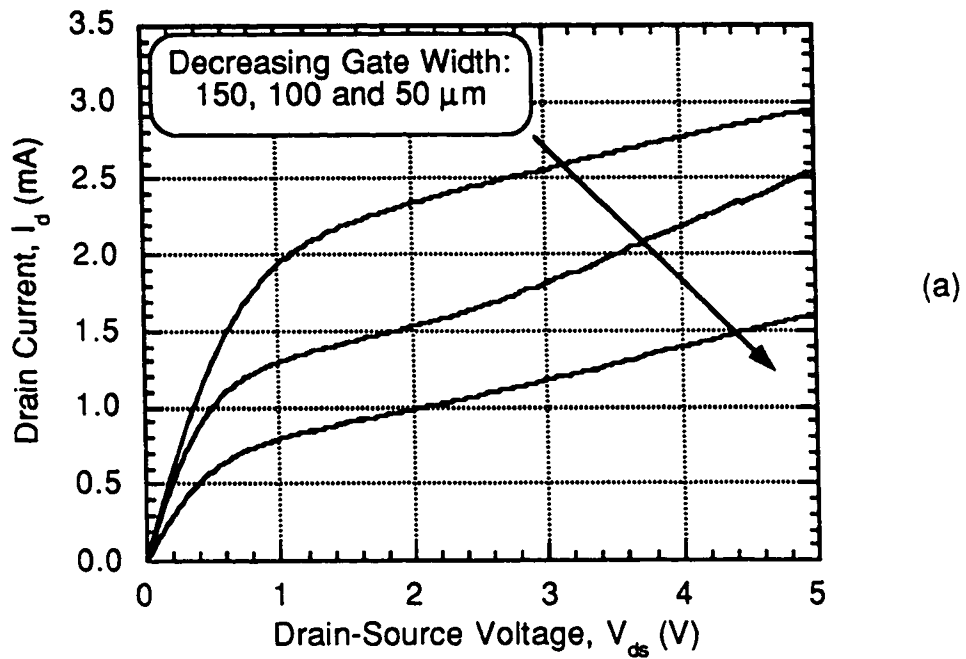
7.6 EFFECT OF SIZE

Figure 7.8(a) and (b) illustrates the effect of W and L on the output current-voltage characteristics (I_d-V_{ds}) of the HFET on S1603. Changes in W and L do not change the shape of the I_d-V_{ds} characteristics, scales the magnitudes of I_d. The results show that $I_{d,sat}$ and $V_{ds,sat}$ decreases as W decreases or as L increases. This is in agreement with the theory of Chap. 3, which shows that

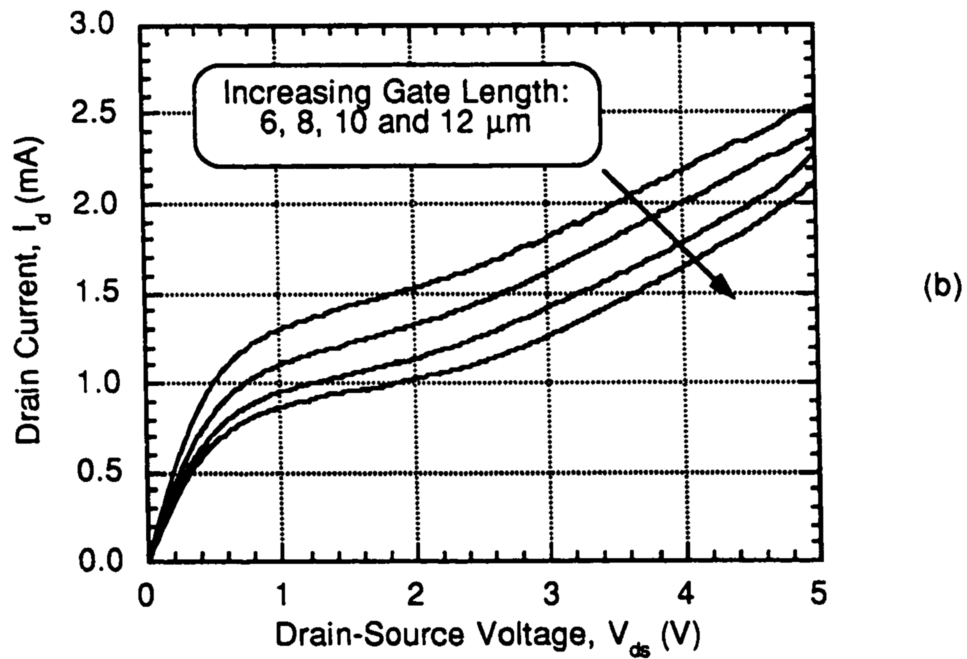
$$I_d = -\frac{W}{L}\overline{\mu}_n \int_0^{V_{ds}} Q_{ni} dV_c \qquad (4.1)$$

In all cases, saturation of I_d was achieved for $V_{ds} \geq 1.5$ V. Figure 7.9 summarizes the effect of device size on the I_d for devices biased at $V_{ds} = 1.5$ V and $V_{gs} = 0$ V. These results represent the average and standard deviations of four different devices on the same wafer. The figure shows I_d increasing linearly with W and increasing linearly with L^{-1}. These results are in agreement with the theory of Chap. 3.

Figure 7.10 shows the maximum normalized transconductance increases linearly with L^{-1}. The normalized transconductance is independent of W because I_d scales linearly with W. The results of Figs 7.9 and 7.10 clearly show that I_d and $g_{m,max}$, for a given structure, can be significantly improved by reducing L. Other studies on size effects of AlGaAs-InGaAs-GaAs based HFETs also reveal similar trends in the transconductance with size [2].

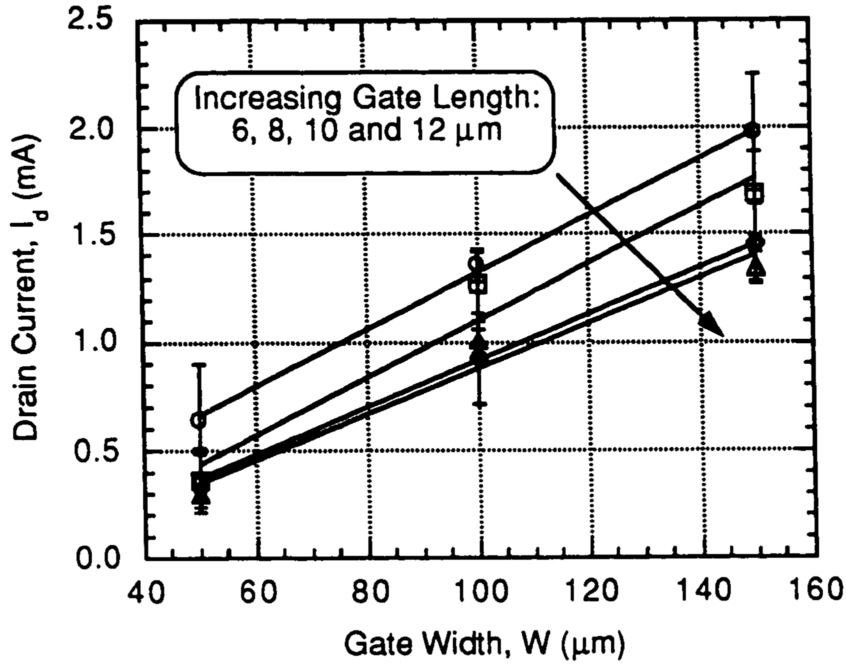


(a)



(b)

Figure 7.8: *Output characteristics I_d-V_{ds} of the HFET with a) gate width and b) gate length as the parametric variable. The HFETs were biased at $V_{gs} = 0$ V.*



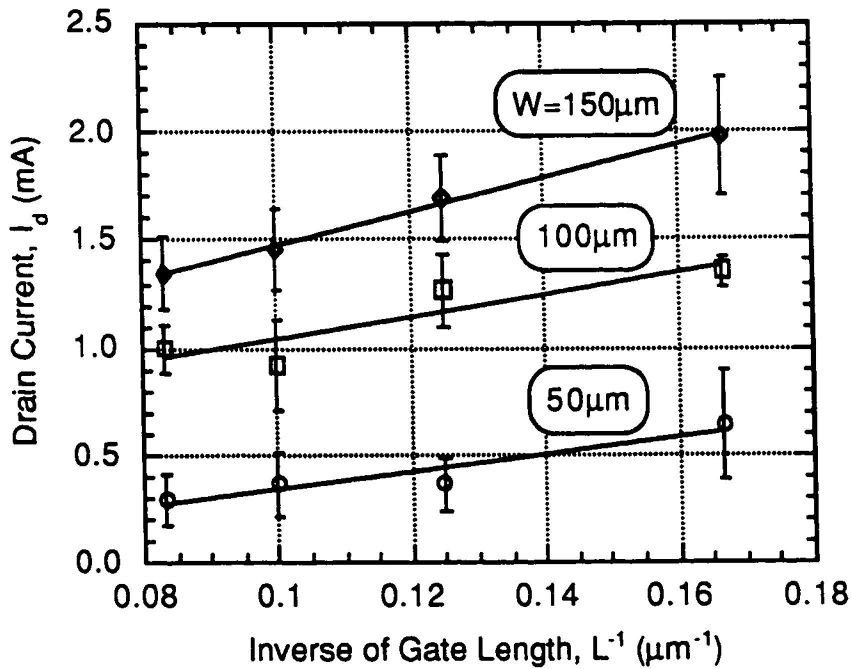


Figure 7.9: a) Saturation drain current as a function of gate width with gate length as the parametric variable; b) Saturation drain current as a function of inverse gate length with gate width as the parametric variable. The HFET's were biased at V_{ds} = 1.5 V and V_{gs} = 0 V.

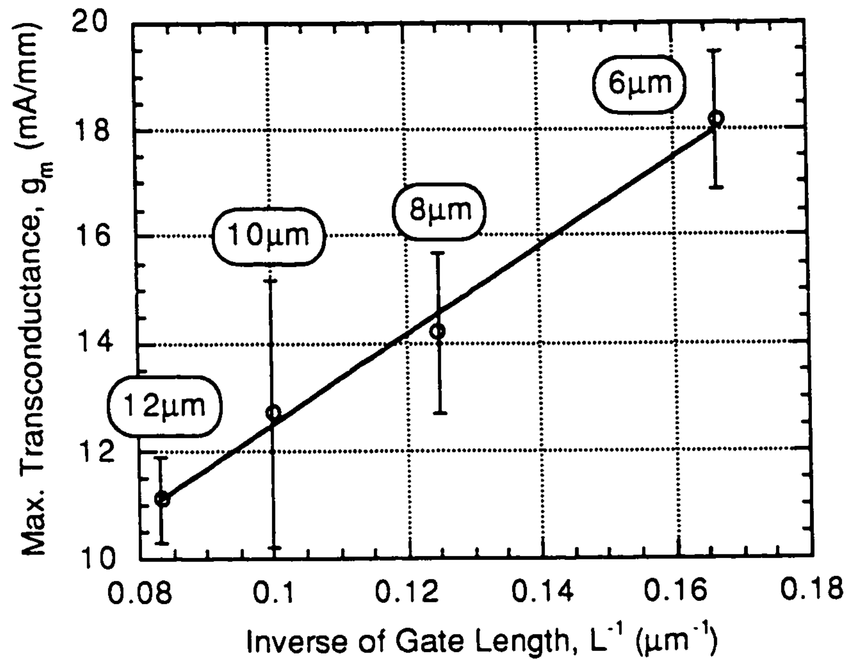


Figure 7.10: Effect of gate length (L) on the maximum normalized transconductance of the HFET. The devices were biased with $V_{ds} = 1.5$ V.

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CHAPTER 8

EXPERIMENTAL CHARACTERIZATION OF THE BICFET AND BICPT

This chapter demonstrates the operation of the n-channel InGaAsP-InP based bipolar inversion channel field-effect transistor (BICFET) and the n-channel InGaAsP-InP based bipolar inversion channel photo-transistor (BICPT). The chapter begins with a detailed experimental analysis of the BICFET which includes the input and output I-V characteristics of the device. This followed by a detailed experimental characterization of the input and output I-V characteristics of the BICPT. For each set of I-V characteristics, the behaviour of the p-n junctions within the BICFET and BICPT are measured. These results show that operationally, the BICFET and BICPT behave in a fashion that agrees with the predictions of Chap. 5. Unfortunately, in spite of this agreement with theory, the BICFET and BICPT did not demonstrate any current gain. The reasons for this absence of current gain in the BICPT and BICFET is presented along with recommendations for the future design and fabrication to remedy this problem.

8.1 BICFET

All electrical and optical characterization of the BICFET was performed with the parameter analyzer and probe station described in Sect. 6.1. Each of the emitter, inversion channel and active contacts were connected to an SMU. The devices were biased in the common-emitter circuit configuration by biasing the emitter at ground potential and the active layer at a negative bias relative to the emitter. The inversion channel was biased by injecting electrons into the inversion-channel, which results in a negative current flow at the inversion-channel contact. The I-V characteristics presented were of an 80 x 80 μm^2 device from wafer S1604. The characteristics exhibited by this device is typical of other devices from S1604.

The forward-biased current-voltage (I-V) characteristic across the emitter-inversion channel contacts of the BICFET is illustrated in Fig. 8.1. This I-V characteristic exhibits a high resistance characteristic which results from the parallel conduction paths between the emitter and inversion-channel contacts, as discussed in Sect. 6.4.1. This high-resistance characteristic, which exists over the operating range of the BICFET, restricts current flow across the e-i junction and limits the BICFET's ability to provide current amplification.

Figure 8.2(a) illustrates the I-V characteristic of the e-i and a-i junctions as a function of V_{ae} for I_i = -100 μA. At V_{ae} = 0, the a-i and e-i junctions are forward biased with $V_{ei} = V_{ai}$. Under this condition, the potential barrier for electrons in the inversion channel flowing out the active layer (ϕ_{ai}) is significantly smaller than the potential barrier for electrons in the inversion channel flowing out the emitter (ϕ_{ei}), see Fig. 8.3(a). As a result, most of the

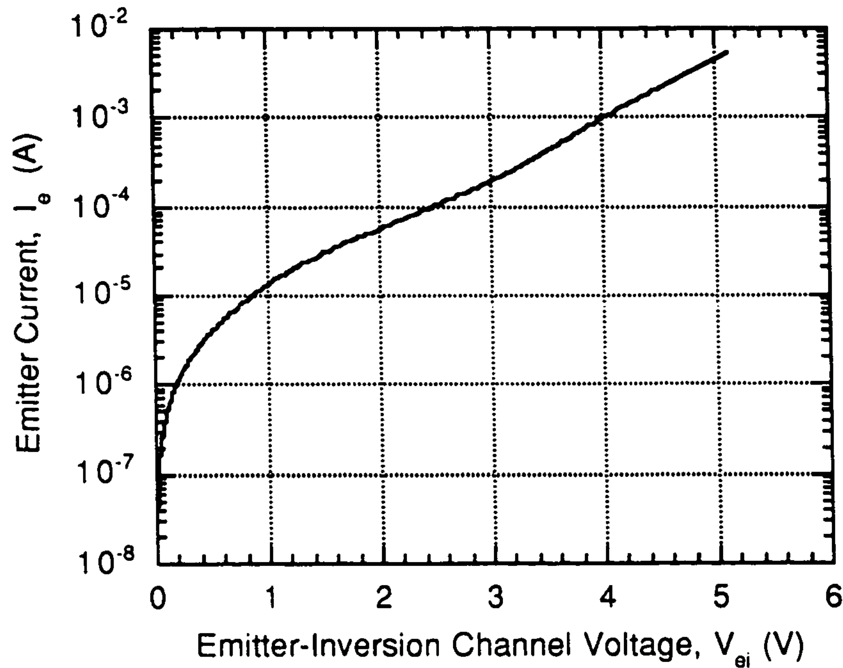
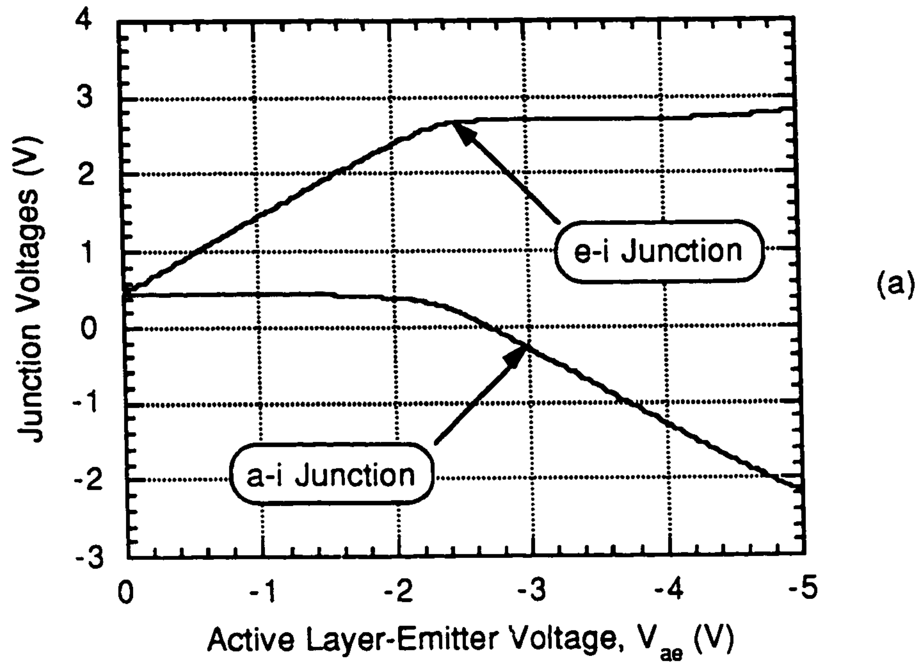


Figure 8.1: *Input current-voltage characteristics (I_e-V_{ei}) characteristics of the BICFET.*

injected electrons flow out of the active layer and thus, $I_a = -I_i$ and $I_e = 0$ (see Fig 8.2(b)). As V_{ae} decreases, in the region where $0 > V_{ae} > -1$ V, V_{ei} moves towards increasing forward bias and thus, ϕ_{ei} decreases. V_{ai} on the other hand is pinned at approximately 0.23 V, a bias that will support the flow of electrons from the inversion channel and out the active layer.

In the voltage range where $-1\ V > V_{ae} > -2.5$ V, the barriers ϕ_{ei} and ϕ_{ai} become comparable in magnitude and as a result I_i flows out both the emitter and the active layer contacts (see Fig. 8.3(b)). At $V_{ae} = -1$ V, a large fraction of the injected electrons flow out the active layer, as $\phi_{ei} > \phi_{ai}$; however, at $V_{ae} = -2.5$ V, a large fraction of the injected electrons flow out the emitter, as $\phi_{ei} > \phi_{ai}$. The condition when the flow of injected electrons out the emitter is equal to the flow out the active layer exists at $V_{ae} = -2.0$ V when $I_a \approx I_e$. For $V_{ae} < -2.5$



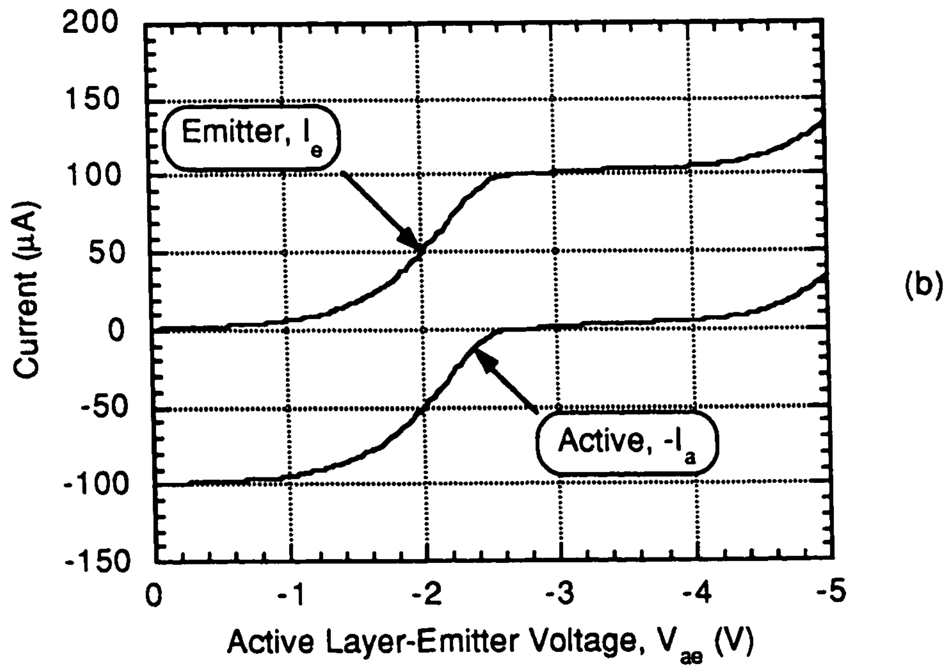


Figure 8.2: a) V_{ei} and V_{ai}, and b) I_e and I_a as a function of V_{ae} for $I_i = -100$ μA.

V, ϕ_{ei} << ϕ_{ai} and all the injected electrons flow across the e-i junction (see Fig. 8.3 (c)). V_{ei} is pinned at $V_{ei} \approx 2.7$ V, a voltage which will support the flow of all injected electrons across the e-i junction. The V_{ae} at which this condition exists is referred to as the turn-on voltage (V_{th}). For further decreases in V_{ae} for $V_{ae} < V_{th}$, V_{ei} is pinned at $V_{ei} \approx 2.7$ V while V_{ai} begins to decrease, eventually going into reverse bias, to support the applied V_{ae}.

Figure 8.2(a) and (b) shows that the a-i and e-i junctions behave in a fashion that is consistent with the predictions made by the BICFET model of Chap. 4 (see Fig. 4.7). However, the experimental results show the V_{th} = -2.5 V instead of the -0.5 V predicted by the model. This shift in V_{th} results because the e-i junction is in the high resistance state, therefore, the voltage required to sustain I_i is high. Another consequence of the e-i junction being in the high resistance state is that the induced hole current flow from the emitter to the active layer is also small and as a result the device does not exhibit any current amplification. With the absence of any current amplification, this device can only redirect the flow of I_i from the active layer contact to the emitter contact and act as a voltage controlled current divider.

Figure 8.4 shows the output current-voltage (I_a-V_{ae}) characteristics of the BICFET with the inversion-channel current as the parametric variable. The threshold voltage of the device, V_{th} = -2.5 V, separates the OFF and SATURATION states of operation. For $V_{ae} > V_{th}$, the device is in the OFF state and electrons which are injected into the inversion channel flow out of the active layer contact, $I_a = -I_i$. The operation of the BICFET in this region agrees with theory of Chap. 4, see Sect. 4.3. As V_{ae} decreases, ϕ_{ai} increases while ϕ_{ei} decreases (see Fig. 8.3), more of the injected electrons begin to flow

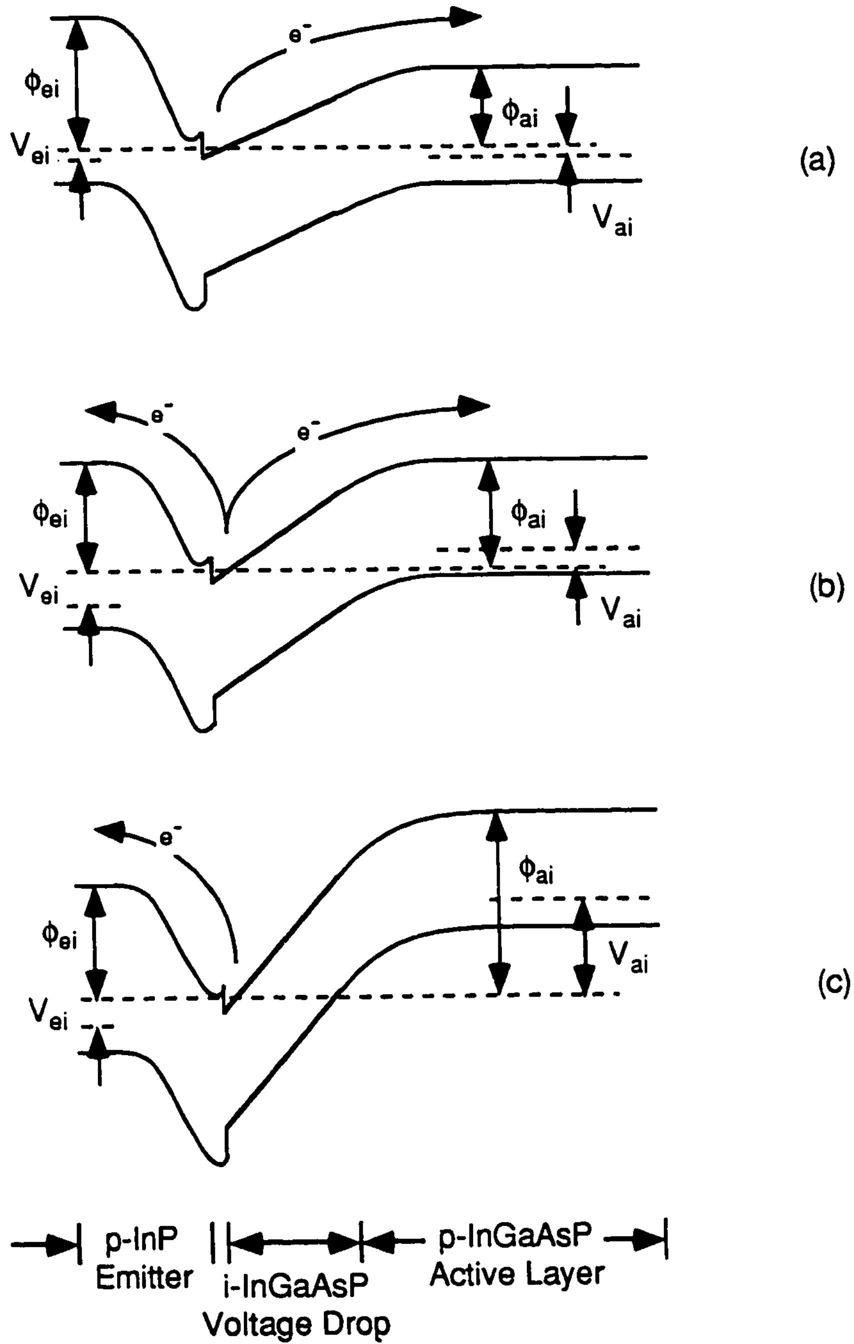


Figure 8.3: Energy band representation of the BICFET under a) low V_{ae} bias, b) moderate V_{ae} bias and c) high V_{ae} bias.

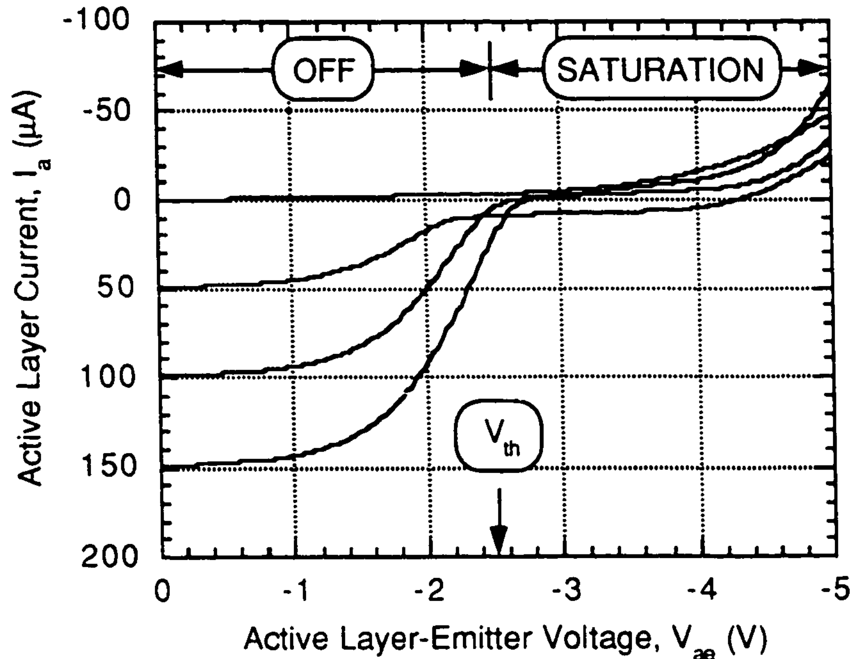


Figure 8.4: Output I_a-V_{ae} characteristic of the BICFET with I_i as the parametric variable.

out of the emitter. This continues until ϕ_{ei} is significantly smaller than ϕ_{ai}, and all electrons flow out through the emitter. This results in the decrease in the magnitude of I_a as V_{ae} decreases.

For $V_{ae} < V_{th}$, the device is in the SATURATION state and most of the injected electrons flow out the emitter. Ideally, the injected electrons flow across the e-i junction and forward biases the junction. This in turn will result in the flow of holes across this junction towards the active layer. These holes, which flow from the emitter and out the active layer contact, are the primary contribution to I_a in the SATURATION state. Since the emitter doping concentration for wafer S1604 is extremely low at $5x10^{17}$ cm^{-3}, relative to the doping concentration of the inversion channel, the inducted hole flow across the e-i junction is negligible. Furthermore, the parallel conduction

paths and the e-i junction being in the high resistance state further limits the already small hole flow across the junction. As a result, there is negligible active layer current flow in the ON state.

8.2 BICPT

BICPT characterization was also performed with the parameter analyzer and probe station described in Chap. 6, see Sect. 6.1. The devices were biased in the common-emitter circuit configuration with the emitter biased at ground potential and the active layer at a negative bias relative to the emitter. Each of the emitter, active contacts were connected to an SMU. An optical fibre was used to couple light (λ = 1.3 μm) into the device through a window in the emitter metal. All characterization was performed with devices from structure S1604. The devices had an emitter mesa that was 100 x 100 μm^2 and a window in the emitter contact that was 80 x 80 μm^2.

Figure 8.5 illustrates the effect of optical illumination from a λ = 1.3 μm optical source on the output I-V characteristics of the device. The λ = 1.3 μm light is not absorbed by the InP emitter but is strongly absorbed by the InGaAsP (λ=1.3 μm) active layer. Light which is absorbed in the active layer generates electron-hole pairs which will recombine unless they are separated from each other by an electric field. Thus, only the electron-hole pairs which are generated within the depletion regions of the active layer contribute to the internal current flows. For small V_{ae}, $V_{ae} > -0.5$ V, $\phi_{ei} > \phi_{ai}$ and thus, the photogenerated electrons flow towards the active layer contact. These electrons recombine with the photogenerated holes which also flow towards

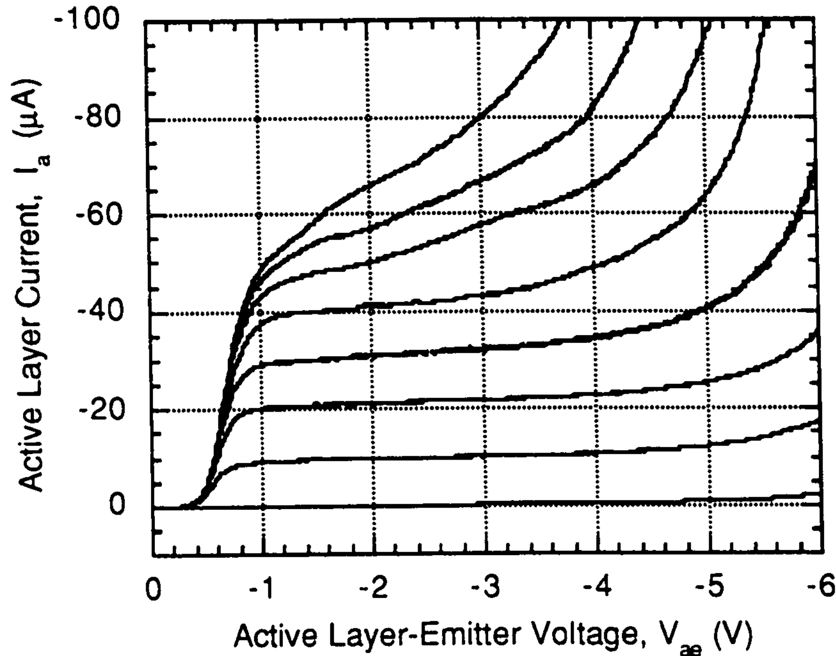


Figure 8.5: Output I_a-V_{ae} characteristic of the BICPT with optical injection (ϕ) as the parametric variable.

the active layer contact. As a result, there is negligible active current flow $V_{ae} \geq -0.5$ V.

As V_{ae} decreases, The e-i junction becomes more forward biased, and ϕ_{ei} decreases, while the a-i junction becomes more reverse biased, and ϕ_{ai} increases. For $V_{ae} < -0.5$ V, $\phi_{ei} << \phi_{ai}$ and thus, the photogenerated electrons flow from the a-i junction depletion layer across the e-i junction and out the emitter contact. The photogenerated holes are now able to flow out the active layer contact, before recombining, to generate I_a.

Ideally, the photogenerated electrons which flow across the e-i junction will induce a hole flow across the e-i junction and out the active layer contact. This hole flow will add to the photogenerated holes to form the total active contact current. This is the primary contribution to the current amplification

in the BICPT. Since the relative doping of the emitter and inversion channel is not suitable for generating current gain, this induced hole flow is negligible. As a result, I_a is composed entirely of the photogenerated hole current. These results show that with proper design of the device structure, there is potential for using this device as a photodetector with internal current gain.

The experimental characteristics of the BICPT resembles the modeling results of Chap. 4, see Fig. 4.10. The experimental threshold voltage of the BICPT also matches that of the model. This good agreement in the theoretical and experimental data results because the BICPT does not possess the n-type implantation which makes contact to the inversion channel and therefore, does not suffer from the existence of parallel current paths between the emitter an inversion-channel contacts.

Figure 8.6 shows the response of the BICPT to light at λ = 1.3 µm. The dark current of this device is extremely low at 97 nA for a 100 x 100 μm^2 device. The responsivity of this device at λ = 1.3 µm is approximately 0.2 A/W. The response of the device to the incident light is relatively linear.

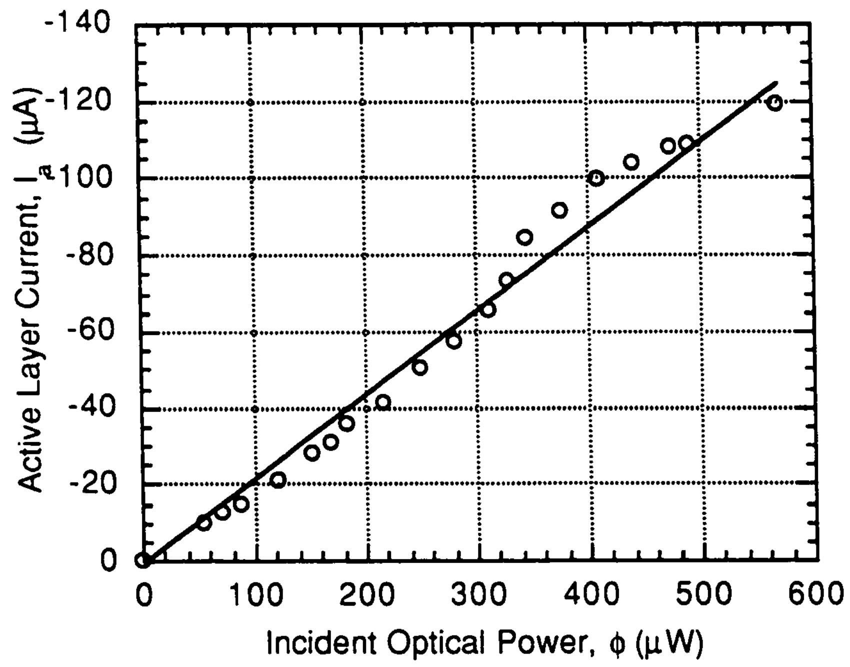


Figure 8.6: I_a *as a function of* ϕ (λ = 1.3 μm) *for the BICPT.*

CHAPTER 9

CONCLUSIONS

In this work, n-type inversion channel technology in the InGaAsP-InP based material system, for monolithic optoelectronic integrated circuits, has been developed and demonstrated. This is accomplished by demonstrating successful device structure design, device fabrication and operation of the DOES, HFET, BICFET and BICPT on a common substrate with a common fabrication sequence.

Device models for the DOES, HFET, BICFET and BICPT were developed and used to design structures S1601, S1602, S1603 and S1604. This was accomplished by identifying the relationship between device structure and device performance. These models also provide the internal potentials, current densities and flows, charge, junction voltages and terminal currents, for each set of external bias conditions. This detailed description of device performance also provides the device physics and operation necessary to experimentally evaluate device performance.

Fabrication recipes and sequences were developed for fabricating 4-terminal self-aligned InGaAsP-InP DOES, HFET, BICFET and BICPT devices on wafers S1601, S1602, S1603 and S1604. These recipes include the fabrication

sequence, photomask set, self-alignment with the use of an SiO_2 mask, SiO_2 sidewall passivation, high accuracy etching with an in-situ QMS, ion implantation, implant activation and metallization over high aspect ration structures. Successful integration of each individual recipe into the fabrication sequence demonstrates use of a common substrate and a common fabrication sequence for ICT.

Electrical and optical characterization of the DOES, HFET, BICFET and BICPT were performed. The DOES devices exhibited the OFF, NDR and ON states with the switching and holding points of V_{sw} = 3.19 V, I_{sw} = 200 μA, V_h = 1.92 V and I_h = 2 mA. Device resistance in the OFF and ON states were R = 10 kΩ and less than 10 Ω respectively. In the ON state, the DOES emits light at λ = 1.3 μm. It was shown that the switching point can be adjusted by applying current to the inversion channel contact, the active layer contact and by shining light into the device. These results are in agreement with the modeling results. Furthermore, detailed examination of the dc input, output characteristics, along with the insight provided by measuring the e-i, a-i and a-c junctions of the device, over the entire range of device bias confirms successful realization of the n-channel InGaAsP-InP based DOES device.

The HFETs were depletion mode devices with V_t = -1 V. These devices exhibit the sub-threshold, linear and saturation states of operation with I_d = 3,1, 2.4, 1.8, 1.1 and 0.5 mA for V_{gs} = 4, 3, 2, 1 and 0 V (at V_{ds} = $V_{ds,sat}$). In the saturation state of operation, the device exhibits a resistance of 5 kΩ. The maximum normalized transconductance exhibited by these devices are 33.0, 30.0, 24.5, and 20.0 mS/mm for V_{ds} = 5, 4, 3, and 2 V respectively. These results are in good agreement with the modeling results. Furthermore, examination

and comparisons of the input, output, transfer and leakage characteristics of the device with theory confirm successful realization of the n-channel InGaAsP-InP based HFET device.

The BICFET exhibited the Off and Saturation state of operation, with the turn-on voltage of V_{th} = -2.5 V. The BICFET did not exhibit any output current and hence, did not exhibit any current gain. In spite of the poor current gain performance of this device, examination of the e-i and a-i junction voltages over the operating range show that the internal potentials, internal charge distributions, current flows and voltages were behaving in a fashion that was predicted by theory. The cause of this poor current gain performance was identified as a low emitter doping level and the existence of parallel conduction paths between the emitter and inversion channel contacts. Recommendations on alternative designs and processes for overcoming these issues are presented.

The BICPT exhibited the Off and Saturation states of operation with a turn-on voltage of V_{th} = -0.5 V. The responsivity of the device for light with λ = 1.3 μm was 0.2 A/W, while the dark current was 97 nA (for a 100 x 100 μm^2 device). Examination of the e-i and a-i junction voltages over the operating range show that the internal potentials, internal charge distributions, current flows and voltages were behaving in a fashion that was predicted by theory. These results are in agreement with the modeling results confirming successful realization of the BICPT.

There are many avenues of research and development which can be pursued as a continuation to this work. These include OEIC circuit design and

optimization, device optimization, improvements to the device fabrication technology, and realization other ICT based devices.