BURST MODE CLOCK RECOVERY

FOR PASSIVE OPTICAL NETWORK

BURST MODE CLOCK RECOVERY

FOR PASSIVE OPTICAL NETWORK

By

MINHUI YAN, B. Eng., M. Eng.

A Thesis

Submitted to the School of Graduate Studies

in Partial Fulfillment of the Requirements

for the Degree of

Doctor of Philosophy

McMaster University

DOCTOR OF PHILOSOPHY (2007) McMaster University

(Electrical and Computer Engineering) Hamilton, Ontario

TITLE: Burst Mode Clock Recovery for Passive Optical Network

AUTHOR: Minhui Yan,

B. Eng. (Electrical Engineering)

M. Eng. (Electrical Engineering)

Shanghai Jiao Tong University,

China

SUPERVISORS: Dr. Wei-Ping Huang, Professor

Dr. Chih-Hung Chen, Assistant Professor

NUMBER OF PAGES: xx, 138

ABSTRACT

The emerging passive optical network (PON) requires the burst mode clock and data recovery (BM-CDR) for the successful data detection, with a strict requirement in the locking time. Two innovative BM-CDR schemes are proposed, modeled, simulated, and analyzed. They simplify the circuit design and reduce the chip size and the power consumption by utilizing the characteristics of the optical components in the upstream fiber link. One scheme utilizes the phenomenon of the clock tone generation by the fiber dispersion. The other scheme utilizes the nonlinear relaxation oscillation of the directly modulated laser (DML) to generate the clock tone. The phenomenon of the clock tone generation by the DML relaxation oscillation is discovered for the first time. Both schemes do not incur extra cost, additional optical components or electrical circuit blocks.

In both schemes, the BM clock recovery (CR) circuitry is based on the injection locked oscillator (ILO). Its behavior in the BM-CR application with the input of the distorted non-return-to-zero (NRZ) data is simulated at the system level for the first time. The BM-CR circuitry is designed and fabricated in a standard 0.18 μm CMOS technology to experimentally demonstrate the two schemes operating at the bit rate close to 10 Gbps.

ACKNOWLEDGEMENTS

First of all, I would like to express my sincere acknowledgment to Prof. Wei-Ping Huang, my principle supervisor, for providing me the chance to work in the projects, letting me freely think on innovative ideas, offering me the design/simulation and measurement environment with various tools and equipment to confirm my ideas, and his indispensable technical guidance, constant encouragement and careful publications reviews and revisions throughout this work, as well as the financial support through research assistantship.

I am also indebted to Prof. Chih-Hung Chen, my co-supervisor, for his support and encouragement, as well as the financial support. He took plenty of time discussing with me during the processes from ideas inspiration, detailed analysis methodologies, to paper drafting, revision and submission. He also taught me to focus on the "big picture" at first and the importance of innovations in conceptual level.

I want to express my sincere acknowledgement to two of the other members (besides Prof. Huang and Prof. Chen) in my PhD supervisory committee. Prof. Shiva Kumar and Prof. Nicola Nicolici spent their valuable time for me not only at the usually overtime committee meetings but also when I asked their advices and suggestions.

I am also grateful to all the members of Prof. Huang/Li/Kumar's photonic research group and Prof. Deen/Chen's microelectronics research group, both in department of Electrical and Computer Engineering, and Prof. Chang-Qing Xu's research

group in department of Engineering Physics, all in McMaster University, for the great learning and working environment they create and support.

I would also like to acknowledge the Canadian Microelectronics Corporation (CMC) is also acknowledged for providing the great design and simulation environment, the fabrication opportunities, and the measurement equipment. Thanks are also given to Ontario Graduate Scholarships (OGS) committee, Electrical and Computer Engineering department at McMaster University, and McMaster University graduate school for financially supporting this work through scholarships, teaching assistantships and bursaries.

Then I would like to thank my parents who have supported me financially and spiritually and encouraged me through my life. Finally, I would like to express my love and thanks to my wife, Dan Shan, for her constant love, understanding and patience throughout my PhD studies and research. I also want to thank her parents.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF SYMBOLS

A	Nonradiative recombination coefficient of directly modulated laser
B	Radiative recombination coefficient of directly modulated laser
b_k	Binary bit
c	Velocity of the light in vacuum
C	Auger recombination coefficient of laser, or capacitance of the capacitor
C_{gd}	Small-signal gate-drain capacitance
C_{gs}	Small-signal gate-source capacitance
C_{ox}	Capacitance between spiral inductor and substrate
C_{sb}	Small-signal source-body capacitance
C_{sub}	Substrate capacitance of spiral inductor
D	Dispersion parameter of the fiber
$\widetilde{E}_{Tx}(f)$	Transmitted optical signal in frequency domain
$E_{Tx}(t)$	Transmitted optical signal in time domain
$\widetilde{E}_{Rx}(f)$	Received optical signal in frequency domain
$E_{Rx}(t)$	Received optical signal in time domain
f	Frequency
f_o	Internal or natural frequency of injection locked oscillator
G_0	Gain constant of directly modulated laser
G_p	Absolute value of gain derivative to photon number in laser

g_m	Transconductance
i_d	Small signal drain current of transistor
I_D	DC drain current of transistor, or threshold decision current in data decision circuit
i_n	Internal noise of oscillator
I_{sink}	Current sink biasing for LC oscillator
i_{inj}	Small-signal injection current
j	Imaginary unit
L	MOSFET's gate (channel) length, or inductance of the inductor
n	Carrier density in directly modulated laser
n_t	Threshold carrier density in directly modulated laser
p	Photon density in directly modulated laser
$p_s(t)$	Electrical driving pulse shape
q	Charge of one electron
Q	Quality factor of inductor
Q_S	Signal quality factor
R	Absolute value of negative resistance represented in oscillator
R_s	Series resistance of spiral inductor
R_p	Equivalent parallel resistance of inductor
t	Time
T	Bit interval
t_D	Decision timing position

V	Active waveguide volume of laser
V_{freq}	Frequency controlling voltage for LC oscillator
V_{gs}	Large-signal gate-source voltage
v_{gs}	Small-signal gate-source voltage
V_{inj}	Large-signal injection voltage
v_{inj}	Small-signal injection voltage
$V_{inj,p}$	Amplitude of injected sinusoidal waveform to injection locked oscillator
$V_{osc,p}$	Amplitude of sinusoidal oscillation output from injection locked oscillator
V_{th}	Threshold voltage of transistor
W	MOSFET's gate (channel) width
Z	Fiber length
α	Linewidth enhancement factor, or fiber attenuation
β	Spontaneous emission factor in laser
β_2	GVD dispersion parameter (2nd order dispersion) of the fiber
ϕ	Instantaneous phase
$\phi(t)$	Normalized binary modulation signal in EML
λ	Wavelength of the optical signal
μ	Carrier mobility
ω	Angular frequency
θ	Instantaneous phase
τ_p	Photon lifetime in laser

LIST OF ACRONYMS

3D	Three-Dimension
ADC	Analog to Digital Conversion
AlGaAs	Aluminum Gallium Arsenide
APON	ATM PON
BiCMOS	Bipolar-CMOS
BER	Bit Error Rate
BM	Burst Mode
BPON	Broadband PON
BPF	Band-Pass Dilter
B-to-B	Back-to-Back
C	Capacitor, or Capacitance
CDR	Clock and Data Recovery
CLM	Channel Length Modulation
CM	Continuous Mode
CMC	Canadian Microelectronics Corporation
CP	Charge Pump
CR	Clock Recovery
DCF	Dispersion Compensation Fiber
DEMUX	De-Multiplexer
DFF	D-Flip-Flop

DML	Directly Modulated Laser
DPSK	Differential Phase Shift Keying
DUT	Device Under Test
EDC	Electrical Dispersion Compensation
EDFA	Erbium-Doped Fiber Amplifier
EML	Externally Modulated Laser
EPON	Ethernet PON
FBG	Fiber Brag Grating
FET	Field Effect Transistor
FD	Frequency Detector
FDL	Fiber Delay Line
GaAs	Gallium-Arsenide
GO	Gated Oscillator
GPON	Gigabit PON
GVD	Group Velocity Dispersion
HEMT	High Electron Mobility Transistor
IEEE	Institute of Electrical and Electronic Engineers
ILO	Injection Locked Oscillator
ITU-T	International Telecommunication Union – Telecommunication Standardization Sector
InP	Indium-phosphide
IPTV	Internet Protocol Television

L	Inductor
LA	Limiting Amplifier
LAN	Local Area Network
LD	Laser Diode
LPF	Low-Pass Filter
MAC	Media Access Control
MCM	Multi-Chip Module
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
MUX	Multiplexer
NMOS	N-channel MOSFET
NRZ	Non-Return-to-Zero
OLT	Optical Line Terminal
ONU	Optical Network Unit
OPS	Optical Packet Switching
P2P	Point To Point
P2MP	Point To Multiple Points
PD	Photo-Detector, or Phase Detector in PLL
PFD	Phase/Frequency Detector
PLC	Planar Lightwave Circuit
PLL	Phase-Locked Loop
PMOS	P-channel MOSFET
PON	Passive Optical Network

PPG	Pulse Pattern Generator
PRBS	Pseudo-Random Bit Sequence
PRZ	Pseudo-Return-to-Zero
PS	Power Splitter
PSD	Power Spectral Density
R	Resistor or Resistance
RBW	Resolution Bandwidth
RF	Radio Frequency
RLC	Resistor-Inductor-Capacitor
RMS	Root-Mean-Squared
RO	Ring Oscillator
Rx	Receiver
RZ	Return-to-Zero
SAW	Standing Acoustic Wave
SA	Spectrum Analyzer
SC	Star Coupler
SCR	Space Charge Region
SCM	Sub-Carrier Multiplexing
SDH	Synchronous Digital Hierarchy
SOA	Semiconductor Optical Amplifier
SPM	Self-Phase Modulation
Si	Silicon

SiGe	Silicon-Germanium
SG	Signal Generator
SMF	Single Mode Fiber
TDM	Time Division Multiplexing
TDMA	Time Domain Multiple Access
TIA	Transimpedance Amplifier
Tx	Transmitter
VBS	Video Bandwidth
VCO	Voltage Controlled Oscillator
WDM	Wavelength Division Multiplexer

Chapter 1
INTRODUCTION

1.1 Overview of PON

The conventional optical network uses point-to-point (P2P) continuous mode (CM) transmission, in which the optical data signal always exists in the fiber link. One example is the optical synchronous digital hierarchy (SDH) system [1]. Nowadays, the passive optical networks (PONs) are emerging and being deployed. The PONs can support various network applications by providing huge bandwidth directly to the premises of the users homes and the offices [2]. Depending on the different specifications, the PON networks can be categorized into the ATM PON (APON), the broadband PON (BPON), the Gigabit PON (GPON) recommended by the International Telecommunication Union – Telecommunication Standardization Sector (ITU-T), or the Ethernet PON (EPON) by the Institute of Electrical and Electronic Engineers (IEEE) [3, 4]. Their differences reside mainly on the data bit rate, framing and communication protocols, while their network physical architectures are similar, as shown in Figure 1.1 [5]. The network topology is point-to-multi-point (P2MP). The optical line terminal (OLT) resides at the service provider end. The optical network units (ONUs) reside at the user end. Both of them possess the laser diode (LD) and the photo-detector (PD) with different wavelengths. The wavelength of the ONU LD is the same as that of the OLT PD. It is the similar case between the ONU PD and

the OLT LD. Between the OLT and the ONU, the optical passive power splitter forms the tree-like network topology. The power splitter can broadcast the optical signal from the OLT to all the ONUs, and can pass the optical signal from the ONU to the OLT. The optical power splitter with multiple ports facing the ONUs can be implemented by utilizing several 1x2 power splitter in a cascaded way [6]. Other implementations of larger size power splitter include the planar lightwave circuit (PLC) technology [7] or the multimode interference scheme [8]. The wavelength division multiplexer (WDM) components used in both the OLT and the ONU are to separate the upstream and downstream wavelengths paths (e.g., 1310 nm and 1490 nm) from a single fiber to the different optical components.

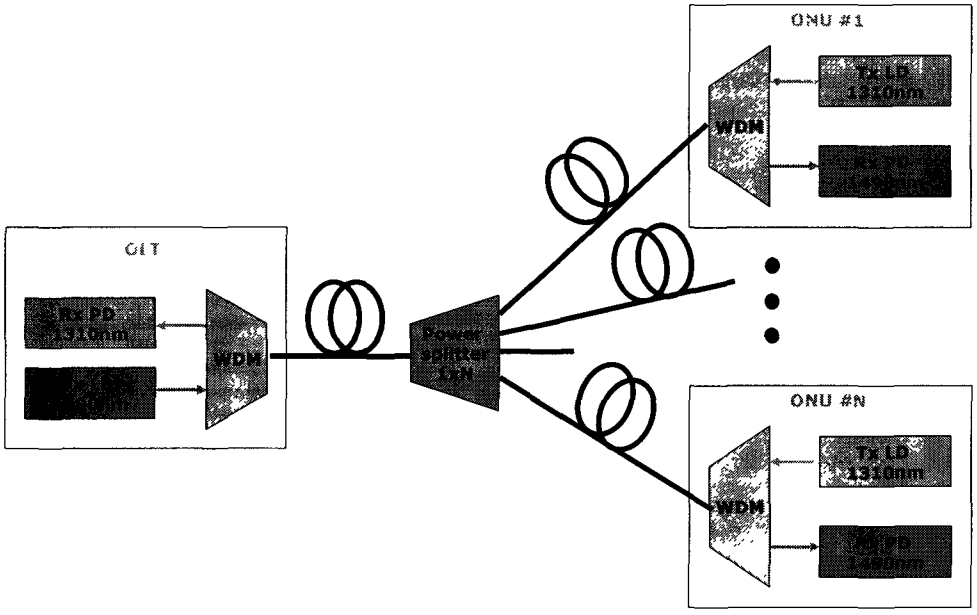


Figure 1.1 The network physical architecture of PON [5].

The operation procedure of the PON can be described in the following example. When the user requests the Internet content, for example, by clicking on the hyperlink on a webpage, the ONU at the user's side sends an optical packet to the OLT in one wavelength (e.g., 1310 nm) through the power splitter. The OLT then retrieves the content from the Internet and broadcasts to all ONUs in another wavelength (e.g., 1490 nm) through the power splitter. The broadcasting optical packet has the header to indicate which ONU shall receive the content. The ONU requested for the content then extracts the content from the optical data signal received. The PON can provide various applications to the access network, directly to the users' homes or offices, due to the huge bandwidth it can offer [2]. Larger communication bandwidth is always demanded by the users. Optical communication can well support this growing demand due to the wide bandwidth the optical fiber can support. However, the costs for the optical transceivers and the fibers are higher than the electrical transceivers and the phone wires used in the current widely used digital subscriber line (DSL) technology. To offset the large cost, different from the P2P topology used in DSL, the PON network architecture uses the P2MP topology to share the costs of the fibers and the OLT among the users.

Due to the topology of the PON, the transmission modes for the downstream (i.e., from the OLT to the ONU) and the upstream (i.e., from the ONU to the OLT) are different. For the downstream transmission, the OLT broadcasts optical signal to all the ONUs in CM, i.e., the downstream channel

always has the optical data signal. One given ONU can find which frame in the CM stream is for it by reading the header of the frame. However, in the upstream channel, the ONUs can not transmit optical data signal in CM. Otherwise, all the signals transmitted from the ONUs converge (with attenuation) into one fiber by the power splitter (serving as power coupler), and overlap among themselves if CM is used. To solve this problem, the BM transmission is adopted for the upstream channel. Each ONU only transmits optical packet when it is allocated a time slot and it needs to transmit, and all the ONUs share the upstream channel in the time domain multiple access (TDMA) mode [5]. The phases of the BM optical packets received by the OLT are different from packet to packet, since the ONUs are not synchronized to transmit optical packet in the same phase. Even if the packets are in phase when transmitted at the ONU sides, the packets reach the OLT at random phases because the distance between the OLT and the given ONU are random. Besides the characteristics of random phases in the burst mode packets, the other issue is regarding the amplitudes of the received packets. Since the distance between the OLT and the ONUs are not fixed, the optical packets received by the OLT have different amplitudes, supposing that the transmitted optical powers of the packets at the ONU sides are similar. In order to compensate the phase variation and the amplitude variation, the burst mode clock and data recovery (BM-CDR) and the burst mode amplifier need to be employed, respectively.

The PON network discussed so far is called the time-division-multiplexing (TDM) PON, for the users at the ONU side share the total bandwidth by different time slots, in both of the down-stream and the up-stream. The other kind of PON, namely the WDM-PON, allows the users to share the total bandwidths by the different wavelength channels [9]. The WDM-PON can provide larger bandwidth than the TDM-PON if their equipped transceivers have the same bit rate, because every user can solely possess one channel all the time in the WDM-PON. However, in the WDM-PON, every ONU shall have a transmitter with different wavelength. The wavelength of the ONU transmitter shall be precise in order not to overlap with the wavelengths of other transmitters. This leads to higher fabrication cost. Furthermore, the number of the ONUs in one WDM-PON is limited, due to the following two facts. One is that the wavelengths of different ONUs cannot be put too close because of the interference consideration, and the other is that the total wavelength range available for fiber transmission is limited according to the fiber attenuation profile. On the contrary, ONU transmitter in the TDM-PON is less expensive for looser requirement of the wavelength precision. The TDM-PON can also accommodate large amount of ONUs if the output powers of the ONU transmitters and the OLT ones are large enough to compensate the attenuations of the fiber and the large size power splitters. The WDM-PON is suitable for the users who access the network all the time with large uploading and downloading needs. The TDM-PON, however, can accommodate needs of the general users, who only access the network

occasionally. In this way, the pure WDM-PON may not be economical for the general public, and the hybrid WDM/TDM-PON (e.g., [10]) was proposed to balance the trade-off between the cost and the accessed bandwidth per user. In the hybrid WDM/TDM-PON, every wavelength channel is shared by a group of ONUs in the similar manner as in TDM-PON. In this work, we are focused on the designs for TDM-PON, which are also helpful for the hybrid WDM/TDM-PON.

In the TDM-PON, the wavelength of the upstream channel is specified as 1310 nm by the current PON recommendations (e.g., [5]). This is to reduce the ONU transmitter cost. At this wavelength, the G. 652 single mode fiber (SMF) [11] used in the PON does not exhibit dispersion, so the ONUs can use the low cost directly modulated lasers (DMLs) which usually possess large chirping effect. The chirping in the DML optical signal can dramatically damage the transmitted signal by the fiber dispersion effect. At zero dispersion, however, the chirping does not affect the transmitted optical signal. The disadvantage of using 1310 nm wavelength is that the G.652 SMF usually exhibits larger attenuation at 1310 nm than that at 1550 nm wavelength.

The academia and the industry has began the research to use the upstream wavelength at around 1550 nm [10, 12-14], to take the advantage of the low attenuation of the fiber at this wavelength [11], and the easy optical amplification from the Erbium doped fiber amplifier (EDFA) [15]. Correspondingly, the DML transmitter originally used at the ONU side shall be replaced by the transmitter based on the zero-chirping externally modulated laser (EML) [16] to

accommodate the 1550 nm wavelength. Though the cost of the EML is usually higher than that of the DML, the EML based transmitter can enable longer fiber transmission length [16]. This is because the zero-chirping optical signal produced by such EML can transmit farther distance than that from the DML with 1550 nm in the dispersive fiber (the G.652 SMF exhibits the dispersion at 1550 nm wavelength). Comparing between the configuration using the 1310 nm DML and that using the 1550 nm EML in the P2P optical fiber link, the latter can transmit farther distance than the former on the G.652 SMF without optical amplification [17, 18], and have the potential to transmit even more distance if the EDFA is equipped [14, 19]. By employing the EML, the ONUs can be deployed far beyond the 20 km limitation of distance from the OLT, specified in the current PON recommendations (e.g., [5]), and/or more ONUs can be deployed in one PON than the number specified (e.g., maximum 64 in [5]). As an example, by deploying the 1550 nm wavelength EML together with the EDFA, the resulting PON is able to support 1024 ONUs with an 100 km reach [14]. In this way, the OLTs supporting a large area can be put in one facility site. Conventionally, the OLTs have to be deployed sparsely to support the whole large area, for the ONUs have to be deployed within 20 km range of the corresponding OLT. The costs of building and maintaining those sparse facility sites are high. On the other hand, by using the new configuration, fewer OLTs are required to support such large area than the case when the DML transmitters are used at the ONU side. This is because the supported ONU number by one OLT increases. This makes the

central OLT site smaller and easier to maintain. Furthermore, migration from the 1310 nm DML to the 1550 nm EML of the upstream transmitter enables the possibility to deploy the hybrid WDM/TDM-PON (e.g., [10]). In the hybrid WDM/TDM-PON, the upstream channel has several wavelengths, and each wavelength is shared by several ONUs. In this way, the upstream bandwidth can be boosted and/or the ONUs number in one PON can be increased.

Besides the migration of the wavelength and the transmitter type, another trend is the quest for the bandwidth, both for the downstream and the upstream. We all know that the download bandwidth is always increasing to meet the demand of the emerging wide-band applications, like the high-definition Internet protocol television (IPTV) [20], etc. On the other hand, the Internet users nowadays do not restrict their access to the Internet as the pure downloads, but also upload their own contents to the Internet. The Youtube [21] is one example where users are fond of uploading their videos to the websites. The current video resolutions of the uploaded videos are low due to the limitations of both uploading and downloading bandwidths. Gradually, the users will not be satisfied with such low resolution and demand for larger uploading bandwidth (i.e., upstream bit rate). Other examples of the upstream bandwidth hungry applications include: 1) the immediate and fast online backup services like the data center; 2) the next generation online gaming with the immersive virtual reality system [22] uploading the large amount of the detailed actions of the user in three-dimension (3D); 3) the video conferences in which both the high definition sound and the

video contents are transmitted upstream; and 4) the 3D telemedicine [23] in which a huge amount of instantaneous data about the patients need to be transmitted to the remote hospital from the homes of the patients. In the PON architecture, the users at the ONU side share the total upload bandwidth determined by the upstream bit rate. For a large PON network holding large amount of ONUs to reduce the shared cost, the uploading bandwidth shared by every user is dramatically reduced. To tackle this bandwidth sharing problem and accommodate the current and future Internet applications, the BM transmitters and receivers operating at the high bit rate (e.g., 10 Gbps or beyond) are essential to boost the upstream bandwidth.

1.2 Design Challenge of BM-CDR

The structure of the optical receiver is illustrated in Figure 1.2 [24-27]. The received optical data signal is firstly converted into the photo-current (as the electrical current) by the photo-detector (PD), and then converted with amplification into the electrical voltage by the transimpedance amplifier (TIA). After that, the electrical voltage is further amplified by the limiting amplifier (LA) to reshape the pulses. Finally, the reshaped voltage data signal is fed into the clock and data recovery (CDR) circuit, and the CDR circuit extracts the clock from the data and performs the data decision. The optical data signal is usually transmitted in binary format, e.g., the non-return-to-zero (NRZ) format. However, after fiber transmission and photo-detection, the data signal is usually distorted

and added with noise. The CDR is used to decide whether the bits are logical ONE or ZERO, and the following digital circuits after the CDR can treat the recovered data as the digital signals.

Figure 1.2 Illustration of optical receiver structure [24-27].

Because of the point-to-multipoint network topology, the OLT Rx shall work in the burst mode. Here "Burst mode" for the OLT Rx has two aspects. One aspect is that the received optical packet amplitude has large dynamic range [5, 25]. This is because the distances between the OLT and the ONU are not fixed. Furthermore, the optical packets transmitted from different ONUs experience different attenuations from different power splitters if distributed power splitters are used [4, 5].

The other aspect of "burst mode" is that the phases of the received optical packets are different from one to another. This is again due to the different distances between the OLT and the ONUs, so the optical packets from different ONUs are not in phase when arriving at the OLT. Above all, the BM receiver needs to recover the amplitude dynamic range and the phase variation. Furthermore, both the amplitude recovery and the clock recovery shall be accomplished in a short time, namely, the preamble time [25]. The preamble time

defined in the GPON recommendation is different for different bit rates [5, 25]. The preamble bits keep increasing when the bit rate increases, however, the equivalent preamble time is kept within the range between 35 ns and 64 ns.

The strict specifications of the preamble times require the burst mode receiver to be equipped with both the burst mode amplifier (TIA and LA) and the burst mode CDR. The burst mode amplifier is to compensate the huge dynamic range, while the BM-CDR is to generate the clock to lock to the phase of the received packet in a short time.

In the current GPON recommendation [5], the data patterns of the preamble bits for the amplitude recovery and the clock recovery are the long consecutive ONEs and ZEROs, and the alternative ONEs and ZEROs, respectively. The long consecutive ONEs and ZEROs used for the amplitude recovery can help the BM amplifier easily find the maximum and minimum of the received packet amplitude. The alternative ONEs and ZEROs for the clock recovery can speed up the locking process by providing more bit transitions between bits ONEs and ZEROs. However, such data patterns are not necessarily the only patterns to be used. For example, the alternative ONEs and ZEROs pattern can also be used in the amplitude recovery preamble, and the amplitude recovery circuit can still recognize the maximum and minimum of the received packets [28]. In this way, the equivalent preamble time for the clock recovery can be prolonged and it would be a lot easier for the CDR to fully lock to the data packet at the end of the preamble time. On the other hand, the preamble bit

pattern for the clock recovery is not necessarily alternative ONEs and ZEROs. As demonstrated in this work, even if the preamble bits are replaced by the random bits, there are still schemes to perform BM-CDR (e.g., [29]). In this manner, if the architectures of the amplitude and clock recovery schemes are designed properly, the choices of the preamble bits are very flexible.

Regarding the BM-CDR, its output clock needs to lock to the random phase when the new packet arrives. Its frequency is fixed according to the recommendations [5]. Because the BM-CDR has stricter requirement of the locking time, the CDR schemes designed for CM situation may not be used for BM application without modification. For example, the phase-locked-loop (PLL) based CDR can not be easily used for the BM case since its locking time is usually more than several hundred nanoseconds or even several microseconds [30]. One attempt was made to achieve the fast locking in the PLL-based CDR by increasing its loop bandwidth [31]. However, it suffers from a large clock phase variation (10%) after the defined locking time. Furthermore, the designed voltage controlled oscillator (VCO) inside the CDR has a relatively large gain (K_{VCO} = 2 GHz/V) [31]. Such large VCO gain can amplify the noise from the frequency-control-voltage and results in large phase variation in the recovered clock.

To meet the challenge of short locking time, many BM-CDR schemes have been proposed, which can be categorized into three main categories, namely, the all-optical schemes, the all-electrical schemes (including the digital and the analog approaches) and the combined electrical and optical schemes. All the

existing schemes possess their drawbacks, which will be discussed in the following paragraphs.

The all-optical clock recovery schemes use advanced optical or optoelectronic components and devices to recover the clock and retime the optical data packet purely in optical domain [32-36]. They can achieve a very high bit rate (e.g., 40 Gbps) and/or very short locking time (e.g., 1 ns) [32]. However, in order to fit into the PON network, the recovered optical clock needs to be converted into electrical signal for the following electrical circuits to perform data processing. Therefore, for low-cost applications, it is preferred to reduce the number of expensive optical devices and directly recover the clock in the electrical domain. Another concern of the all-optical schemes is that most of them require the return-to-zero (RZ) data format [32-35], instead of the NRZ format which is widely used in the modern PON network. There are some all-optical schemes accepting the NRZ format, however, they usually require additional components or sub-systems to convert the NRZ format to the pseudo return-to-zero (PRZ) format [36]. This adds complexity to the system. Finally, the discrete optical or optoelectronic components used in the existing all-optical schemes [32-36] make the overall CDR sub-systems expensive and difficult in system integration. Therefore, all-optical schemes are not favored in the low-cost PON applications.

The digital approaches in the all-electrical schemes, e.g., using gated oscillators [37, 38] or phase alignment techniques with multiple-phase clocks [39]

are usually not suitable for high speed applications. This is due to the fact that the delay resulted from the transmission between the multiple cascaded gates in the digital circuits can not be reduced easily. The bimodal eyes due to the mismatched clock paths also degrade the eye diagram of the recovered clock and data using gated oscillators [37]. Other approaches are to use the digital processing algorithms after the analog to digital conversion (ADC) on the data [40, 41]. It suffers from the huge power consumption because many gates need to be used to perform the ADC and the digital computation, and/or the limited bit rate of operation because the sampling frequency of the ADC circuit needs to be very fast [40] in order to deal with the fast transition in the high bit rate data.

The analog approaches of the all-electrical schemes can usually work at higher bit rate than the digital approaches. They usually need to re-construct the clock information at the receiver. The logical circuit blocks (e.g., the one using the delay and XOR gates [42]) to convert the NRZ signal to the PRZ one or a differentiator to create the pulses at the rising and falling edges of the incoming NRZ signal [43] may be used. However, the former has a speed limitation restrained by the logical circuits (e.g., the delay gate), and the latter suffers from the false locking due to the pulses resulted from the receiver noise passing through the differentiator. Furthermore, the circuit blocks needed to re-construct the clock information increase the power consumption.

The combined optical-electrical schemes are the modifications of the all-analog schemes. They include the clock (or its harmonics) or create the clock

information in the optical manner, which releases the burdens on the electrical circuitry to generate such clock information. One approach utilizes an additional optical modulator to add the sub-harmonic of the clock into the data at the transmitter, and the receiver uses a simple band-pass filter (BPF) to extract the clock sub-harmonic and restore the clock via frequency multiplier [44]. The drawback of such method is the high cost due to the high-level circuit complexity at the transmitter. Another approach is to use an optical filter at the front-end of the optical receiver to select a portion of the optical spectrum. This results in the clock information exhibited in the converted electrical spectrum [45]. However, to incorporate a high-precision and narrow-band optical filter gives rise to optical assembly complexity and cost.

The BM-CDR designs for the low bit rate operation cannot be directly used or easily modified for the high bit rate operation even if the required locking time keeps similar. This is because most of the BM-CDR schemes control the locking process by the clock generation circuit, in an integrated manner. When the bit rate increases, the clock generation method may need to change, and the locking control manner has to change accordingly. The designs of the BM-CDR are more challenging for the higher bit rate than the lower one, including three aspects. One is that it is challenging to generate the high frequency oscillation used as the clock. The second challenge is to force the generated clock to lock to the new phase of every arriving packet in a quick manner. The third one is to keep the generated clock locked to the data within only small phase variation after

being locked. Generally, it is more difficult to design a CDR with higher bit rate than the one with lower bit rate. Adding the fast locking ability into the high bit-rate CDR would be even more difficult. On the other hand, the demand for higher bandwidth of the access networks, as discussed in Section 1.1, will further push the bi-directional transmission to 10 Gbps bit rates and beyond. This demands for the high bit-rate BM-CDR.

The data modulation format affects the choice and performance of the CDR architectures. Two modulation formats are commonly used. One is the return-to-zero (RZ) format, which uses short pulses (rising to high level and returning to low level within one bit) to represent bit ONE and low level to represent bit ZERO [24]. The other is the non-return-to-zero (NRZ) format, which uses consistent high level for bit ONE and low level for bit ZERO. The NRZ format possesses a big challenge for clock recovery, for it does not contain the clock component along with the transmitted data signal [24]. In contrast, the RZ format contains the clock component in the data signal, which means that it is much easier to recover the clock from the RZ format than from the NRZ one [24, 46]. However, the industry widely uses the NRZ format in the optical communications including the PON [5]. This is mainly because the NRZ format is used in the digital processing circuits, and there would be no need of special circuits to convert the data formats if the NRZ format is used in the optical transmission. The industry has used such format in the metro and long-haul optical communications with the data bit rate up to 10 Gbps. The research and the

industrial field trial using the NRZ format for 40 Gbps and beyond have also been carried out (e.g., [19, 47]). Assuming that the NRZ format would be continuously employed in the high-speed PON of 10 Gbps and beyond, the effective clock recovery schemes for such data format with high bit rate and the burst mode shall be studied and proposed to accommodate this tradition and the quest for low-cost system.

We can reduce the cost of the BM-CDR schemes in several ways, and the costs include the design, the fabrication and the operation ones. The first way is to use the least expensive fabrication process which can still achieve the targeted bit rate through clever designs. The expensive fabrication processes, like the AlGaAs/GaAs high electron mobility transistor (HEMT) [48], the InP hetero-junction bipolar (HBT) [49, 50] or the SiGe bipolar [51-53], are able to realize high frequency CDR circuits (including CM and BM ones). However, the academia and the industry are more in favor of using low cost fabrication process (e.g., complementary metal-oxide-semiconductor, i.e., CMOS) to realize the CDR function with the same high frequency achievable by the expensive fabrication processes. Among all the CMOS technologies, the one with longer gate length (e.g., 0.18 μm) is much less expensive than the one with shorter gate length (e.g., 0.13 μm or 90 nm) which is more advanced and more expensive. Normally, it is much easier to design the high bit rate CDR circuits using the CMOS technology with shorter gate length (e.g., 90 nm in [54], 0.13 μm in [55]); however, this incurs high cost. The 10 Gbps CM CDR circuits have been reported in 0.18 μm

low-cost CMOS technology [30, 56], indicating that the 0.18 μm CMOS technology can be a good choice to realize a 10 Gbps BM-CDR circuit. So far, the reported bit rates in the BM-CDR realized in this technology are usually low even at the recent journals or conferences (e.g., 2.5 Gbps at 2006 and 2007 [31, 57, 58]). One published work of the BM-CDR which can achieve 10 Gbps or higher using this technology requires the complicated digital control circuit and uses half-rate configuration [59]. The digital circuit block increases the chip area and the power consumption, and the half-rate configuration is not preferred for it is sensitive to fabrication mismatch. This situation provides the opportunity to design a better 10 Gbps BM-CDR circuits in 0.18 μm CMOS technology using innovative schemes.

The second way to reduce the cost is to reduce the size of the circuit chip. The fabrication cost is approximately proportional to the chip size in the same fabrication technology. The size reduction can be realized by eliminating some circuit blocks on the chip. Usually, every circuit block provides certain function. If one circuit block is eliminated, the function originally performed by it shall be done by the other manners.

The third way on cost reduction is to reduce the complexity of the circuit and the system, so that the design efforts can be reduced. It is desired that the changes to the components and the system can be kept minimum. The forth way to reduce the cost is to decrease the operation cost, mainly the power consumption.

According to the characteristics and requirements of the future PON networks, the proposed BM-CDR schemes used for such networks should have the following advantages: 1) working at the high bit rate (preferable 10 Gbps for the increasing Internet communication demand), 2) suitable for the widely used NRZ data format, 3) simplified in the design, 4) no requirements of the additional components, 5) using low cost fabrication technology (e.g., 0.18 μm CMOS technology), 6) reduction of chip area and power consumption, 7) easy integration with the following digital processing circuits on the same chip, 8) less sensitive to the fabrication mismatch.

1.3 Major Contributions

There are six major contributions in this thesis, which are listed as follows.

1. A BM-CDR scheme based on the clock tone generated by the fiber dispersion [29].
2. A discovery of the clock tone generation caused by the nonlinear relaxation oscillation in the DML [60].
3. A BM-CDR scheme based on the clock tone generated by the DML relaxation oscillation [60].
4. A systematic approach using the behavioral level simulation to analyze the BM-CR process performed by the ILO [29, 60].

5. An application of an ILO-based circuit topology employing a single switching transistor for the clock recovery.
6. An experimental demonstration of a BM-CDR circuitry with the bit rate close to 10 Gbps in a standard, low-cost 0.18 μm CMOS technology.

1.4 Thesis Organization

This thesis consists of five chapters. Chapter 1 provides the introduction to the PON and describes the design challenges of the BM-CDR. It also summarizes the major contribution of the work and the thesis organization.

Chapter 2 proposes a BM-CDR scheme utilizing the characteristics of the fiber dispersion. The theory and the modeling of the ILO are firstly discussed. Then the phenomenon of the clock tone generation by the fiber dispersion is illustrated through the simulations of the fiber link. The BM-CDR scheme utilizing this phenomenon is also proposed. The behavioural level simulations are performed to demonstrate the scheme and discuss the effects of the system parameters.

Chapter 3 proposes another BM-CDR scheme utilizing the relaxation oscillation in the DML. The clock tone generated by the nonlinear relaxation oscillation is discovered. By utilizing this phenomenon, the corresponding BM-CDR scheme is proposed. Simulations and discussions are followed to analyze the parameters of the devices and the system.

In Chapter 4, the corresponding BM-CR circuit for the two schemes described in Chapters 2 and 3 is designed and manufactured. The experiments are performed to demonstrate the two BM-CR schemes.

Chapter 5 summarizes the whole thesis and provides the recommendations for the future work.

Chapter 2
BM-CDR USING FIBER DISPERSION

According to the category definition of the BM-CDR schemes discussed in Section 1.2, our proposed BM-CDR schemes can be categorized into the combined electrical and optical schemes. However, compared with the existing combined electrical and optical schemes, our proposed schemes do not need to employ extra optical components. Instead, we utilize the characteristics of the fiber dispersion (this chapter) and the DML relaxation oscillation (next chapter), respectively, to generate the clock tone. Then we choose to use the ILO to restore the continuous (sinusoidal) clock from the clock tone.

In this chapter, the analytical theory and the numerical model of the ILO is described at first. Then we discuss on the proposed scheme using fiber dispersion in detail. After that, we perform the simulations by employing the 10 Gbps data bit rate and the 10 GHz clock oscillation frequency.

2.1 Theory of ILO

The ILO can be modeled as a feedback system with external input [61]. The parallel RLC tank in the feedback system serves as a frequency selection network, with the L as the inductor, the C as the capacitor and the R is the equivalent parallel resistance of the parasitic resistance of the inductor and the

capacitor. Usually, the parasitic resistance of the inductor dominates the overall parasitic resistance of the tank, and the parasitic resistance from the capacitor can be ignored. Assuming that both the input and the output are sinusoidal, the derivative equation describing the evolution of the output signal phase θ relatively to the injection signal is as follows [61]:

$$\frac{d\theta}{dt} = \omega_0 - \omega_{inj} - \frac{\omega_0}{2Q} \cdot \frac{V_{inj,p}}{V_{osc,p}} \sin\theta, \tag{2.1}$$

where Q is the quality factor of the inductor. Eq. (2.1) is valid when the injection signal amplitude $V_{inj,p}$ is infinitely small compared to the oscillation output amplitude $V_{osc,p}$. By assuming the injection frequency same as the internal frequency ($\omega_{inj} = \omega_0$) which is approximately the case in the BM-CDR, we can obtain:

$$\frac{d\theta}{dt} = -\frac{\omega_0}{2Q} \cdot \frac{V_{inj,p}}{V_{osc,p}} \sin\theta. \tag{2.2}$$

If the original phase θ = 0, i.e., the output signal has the same phase as the injection signal, Eq. (2.2) makes sure that θ is always 0, i.e., the ILO output is always locked to the input. If θ is not 0 initially, we need to solve Eq. (2.2).

After re-arranging Eq. (2.2), we can obtain:

$$\frac{d\theta}{\sin\theta} = -\frac{\omega_0}{2Q}\cdot\frac{V_{inj,p}}{V_{osc,p}}dt\,. \tag{2.3}$$

Then we can do integration to both sides of Eq. (2.3), and obtain:

$$\int\frac{d\theta}{\sin\theta} = \ln\left(\tan\frac{\theta(t)}{2}\right) - \ln\left(\tan\frac{\theta_i}{2}\right) = \int -\frac{\omega_0}{2Q}\cdot\frac{V_{inj,p}}{V_{osc,p}}dt = -\frac{\omega_0}{2Q}\cdot\frac{V_{inj,p}}{V_{osc,p}}t\,, \tag{2.4}$$

where $\theta(t)$ and θ_i are the final phase and initial phase of the ILO output, respectively. We can re-write Eq. (2.4) as:

$$\theta(t) = 2\tan^{-1}\left[\exp\left(-\frac{\omega_0}{2Q}\cdot\frac{V_{inj,p}}{V_{osc,p}}t\right)\cdot\tan\left(\frac{\theta_i}{2}\right)\right]. \tag{2.5}$$

Here Eq. (2.5) implies the physical meanings of the ILO phase evolution. For any given initial relative phase θ_i, the relative phase $\theta(t)$ approaches to 0 as t approaches to infinity in a monotonic way. This means that the phase evolution in the ILO never oscillates like that in the case of the PLL-based CDR [30, 31]. On the other hand, from Eq. (2.5), $\theta(t)$ never becomes exactly 0, indicating that the ILO never "exactly" locks to the injected signal, and some small phase difference always exists. So we need to set a threshold of relative phase to define the locking time. We can define that the ILO is locked when its absolute relative phase is

smaller than a pre-defined value. The time required to reach that state can be defined as the locking time. We can also re-write Eq. (2.5) as follows,

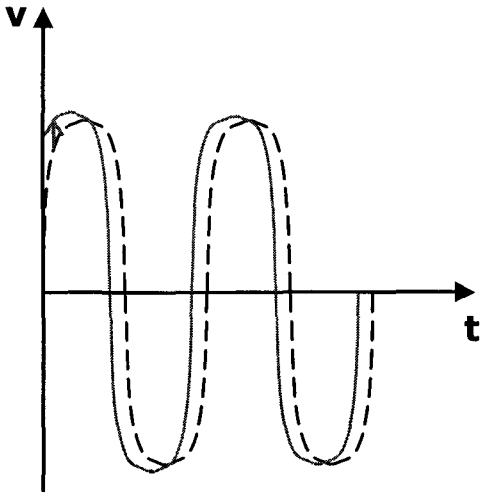
$$t = \frac{2Q}{\omega_0} \cdot \frac{V_{osc,p}}{V_{inj,p}} \left[\ln\left(\tan\frac{\theta_i}{2} \right) - \ln\left(\tan\frac{\theta(t)}{2} \right) \right]. \tag{2.6}$$

Eq. (2.6) provides a simple and intuitive guideline to improve the locking time for arbitrary initial and final phase (i.e., θ_i and $\theta(t)$), for the ILO with fixed frequency as ω_0. In order to reduce the locking time, we need to increase the ratio between the injection amplitude to the oscillation amplitude. This can be understood intuitively by assuming an ultimate case when the injection amplitude approaches to 0 while the oscillation amplitude keeps finite. In this time, there would be effectively no injection, or the ILO can not "sense" the injection. We can also find that in order to reduce the locking time, we need to decrease Q. When Q is smaller, there is more energy dissipated. Then the external injection has the chance to change the phase of the ILO. More energy loss in one oscillation cycle means injection signal has more chance to change the ILO phase.

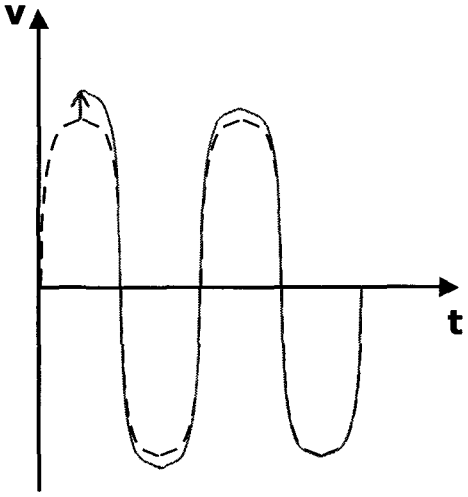
Though Eq. (2.1) provides an insight to the behavior of the ILO, it has some limitations [61], which prevent it from practical application in the analysis for the real ILO circuit. For example, the model assumes a sinusoidal injection. However, depending on the application of the ILO, other kinds of signal formats may be employed, e.g., the clock tone embedded NRZ data signal used in our proposed schemes.

Furthermore, the guidelines indicated by Eq. (2.6) should not be regarded as the only rules in designing the ILO, because other effects are not considered in the model. Eq. (2.6) indicates smaller oscillation amplitude of the ILO, larger injection amplitude and smaller Q can reduce the locking time, for the fixed oscillation frequency. However, improper choices of those parameters would bring problems. When the ILO output amplitude is small, it is more likely to be affected by the circuit noise, and results in large phase variation. When the injection amplitude is too large, it would interfere with the stable oscillation in the tank, especially when the injection is not pure sinusoidal but with random data pattern. When the Q factor is small, the large loss in the tank needs to be compensated by the transistors gain, which in turn consumes large value of power.

We can also understand the injection locking phenomenon intuitively through Figure 2.1, the impulse response of the LC oscillator [62-64]. Though the original intention of such analysis was targeted on the phase noise description and calculation [62-64], we find such an analysis technique is also valid for the case of injection locking. In Figure 2.1, the injection current signal is assumed to be an impulse, and the current impulse is translated into the voltage shift due to the capacitance in the tank [62-64].



(a)



(b)

Figure 2.1 Intuitive understanding of injection locking to oscillator through impulse response of the LC oscillator [62, 63] when (a) oscillator is not yet locked to the injection signal, and (b) oscillator is locked to the injection signal.

In Figure 2.1 (a), the voltage shift due to the impulse current injection changes the instantaneous oscillation voltage. After that, the instantaneous voltage will be pulled back to zero within half oscillation cycle because of the nonlinear oscillator characteristics [63]. After the injection of the impulse, the ILO continues oscillation, however, with the new phase.

In Figure 2.1 (b), if the impulse is injected at the maximum (or minimum) of the oscillation waveform, only the amplitude is changed and the phase is kept unchanged. In both cases, the changed amplitude would return back to its original value due to the nonlinearity attenuating the amplitude variance in the oscillator [61, 63]. If the phase is not locked as in Figure 2.1 (a), the periodic injection of impulses (or the impulses injection from time to time) with a fixed frequency same as the oscillator internal frequency (i.e., the RLC tank frequency) would change the phase in every injection cycle, and finally forces the ILO to reach the state close to Figure 2.1 (b), though it can never reach the perfect locked state.

The ILO is constructed based on the LC oscillator, so we can first discuss on the LC oscillator. Figure 2.2 represents the general topology of the LC oscillator, with the nodes Out+ and Out- forming the differential output. The power supply is provided by the node V_{dd}. The inductors L_1, L_2 and the capacitors C_1, C_2 form the frequency selection tank, with the internal central frequency as follows [65]:

$$f_0 = 1 \Big/ 2\pi \sqrt{(L_1 + L_2)\frac{C_1 \cdot C_2}{C_1 + C_2}} \,. \tag{2.7}$$

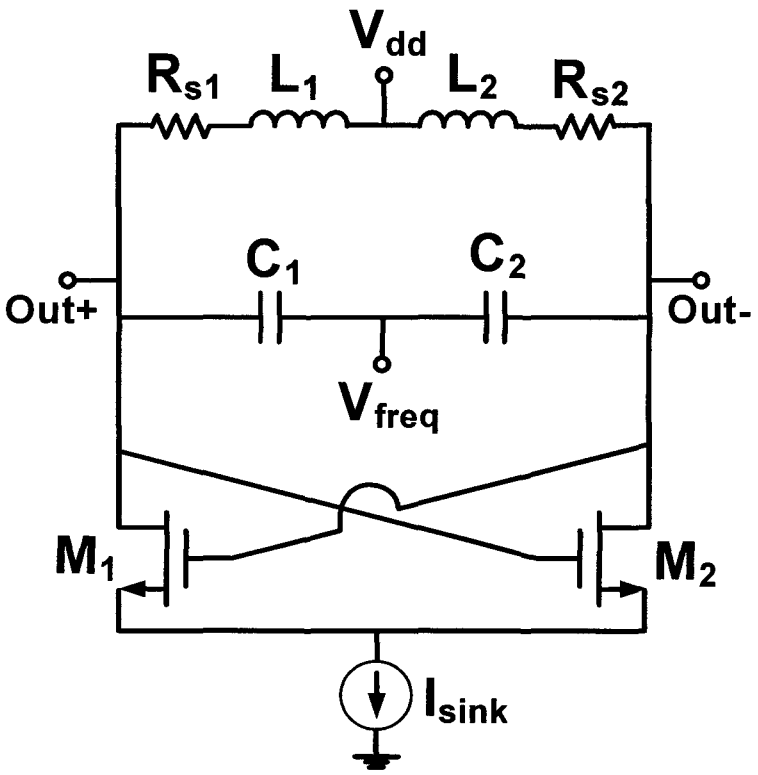


Figure 2.2 The general topology of the LC oscillator [65].

Usually, $L_1 = L_2$ and $C_1 = C_2$. Here C_1 and C_2 are called the varactors for their capacitance values are controlled by the voltages across them [65]. For example, the voltage difference between node V_{freq} and node Out+ decides the capacitance of C_1.

It shall be noted that because of the oscillation at the output nodes Out+ and Out-, the capacitances of C_1 and C_2 always change during every oscillation cycle even when V_{freq} is fixed. This makes the calculation of the precise internal frequency much difficult. The common practice, though not precise, is to

approximate their values by averaging the maximum and minimum values during one oscillation cycle [65]. If the precise internal frequency is to be obtained, the detailed large signal analysis of the oscillation shall be performed to model the transient capacitances of the varactors [66]. This is because in this case the oscillation can not be modeled as a sinusoidal waveform and the internal frequency cannot be calculated by Eq. (2.7).

In order to sustain the oscillation with fixed amplitude, transistors M_1 and M_2 are used to provide gain and compensate for the loss in R_{s1} and R_{s2}, which are the parasitic serial resistances of L_1 and L_2, respectively. The current source I_{sink} is used to control the output swing.

The general circuit topology of the ILO is shown in Figure 2.3 [67]. It is basically an LC oscillator with two injection currents to and from the nodes Out+ and Out- of the oscillator. The injection currents can be converted from the voltage injections [67]. By letting the injection current flow through the RLC tank, the current oscillation phase in the tank can be changed, thus fulfilling the injection locking. The current injection I_{inj1} and I_{inj2} are preferably symmetric with the same value but opposite polarity, to ensure that the injection current does not flow through the current source I_{sink}. Otherwise, the output swing is modulated by the injection current through I_{sink}, which is not preferred.

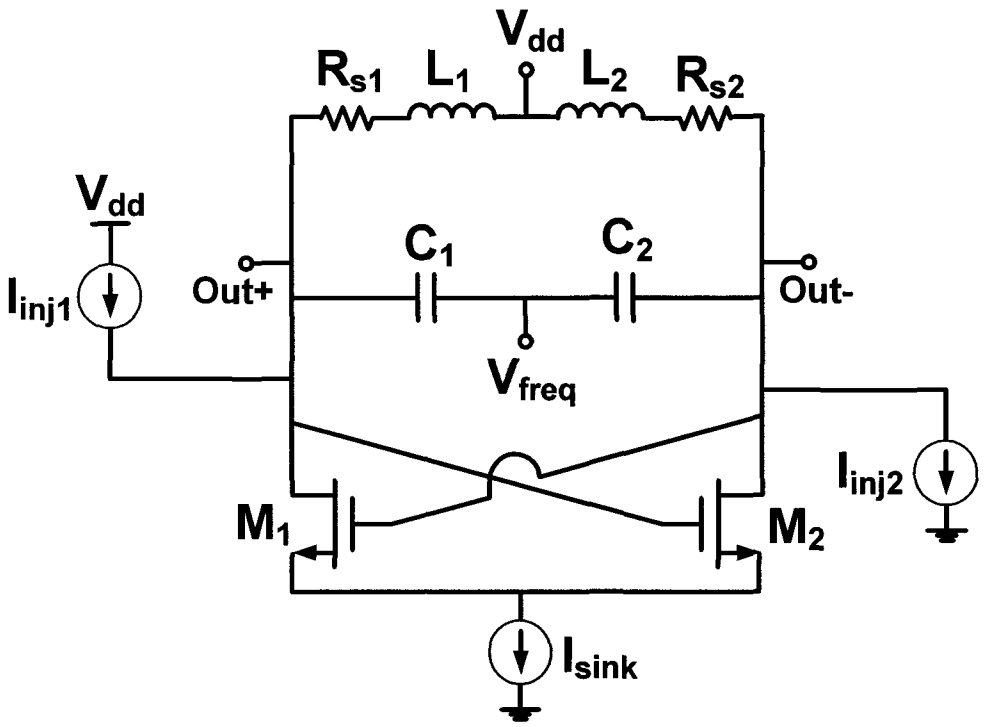


Figure 2.3 General topology of ILO [67].

We are now going to study the numerical model [68] which can provide the clear link to the circuit for an easy and practical parameter setup, at the same time, the numerical model is suitable for any arbitrary injection waveform. We can analyze the operation of the ILO as shown in Figure 2.3, by using the AC small signal analysis, illustrated in Figure 2.4.

In the AC analysis, we only care about the differential signals, and ground every common mode sources. Let us assume that at one moment, the AC current i_{inj} is injected into the ILO at the node Out+, and the LC tank AC current flows from the node Out+ to the node Out-. Since the current flowing into the tank is

positive in AC, then the voltage at node Out+ is positive in AC, i.e., gate (G) voltage of M_2 is larger than that of its DC value in quiescent mode. In this way, I_{ds2} is larger than its DC value, so that its AC component i_{ds2} flows from the drain (D) to the source (S) of M_2. Due to the symmetric characteristics of the ILO, AC current i_{ds1} flows from S to D of M_1, and adds to i_{tank}. We can re-draw the relationship at the Out+ node as in Figure 2.5.

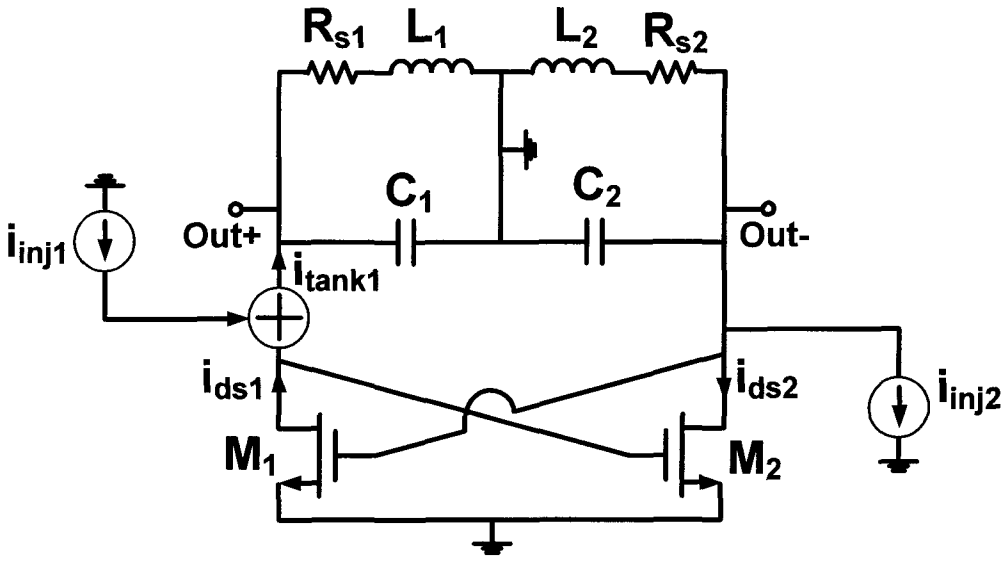
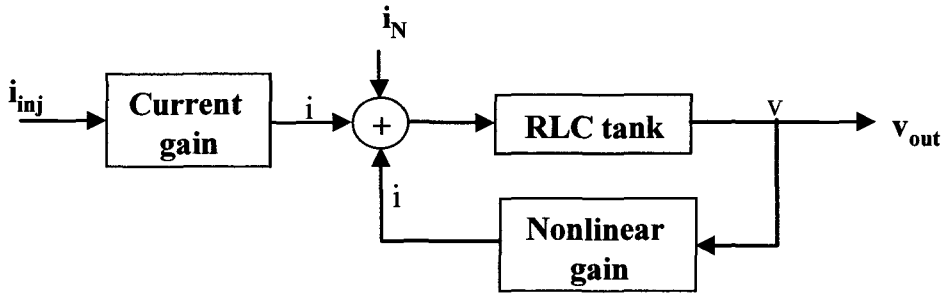
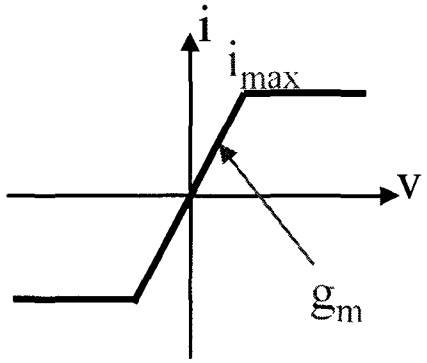


Figure 2.4 Analysis and modeling of ILO operation using small signal analysis.



(a)



(b)

Figure 2.5 Modeling of (a) the ILO, and (b) the nonlinear gain model. The model is modified from [68].

Figure 2.5 (a) represents the left half of the circuit in Figure 2.4, and the summation node in Figure 2.5 (a) represents the summation node at drain of M_1 in Figure 2.4. From Figure 2.5 (a), we can calculate the AC oscillation output of one port (i.e., the node Out+ in Figure 2.4) of the oscillator. If the differential oscillation output signal is to be calculated, a multiplication of 2 on the amplitude

is needed. The RLC tank in Figure 2.5 (a) is the left half of the RLC tank in Figure 2.4, and its transfer function can be calculated as [69]:

$$H(j\omega) = \frac{jL{\omega_0}^2\omega}{-\omega^2 + j\omega\frac{\omega_0}{Q} + {\omega_0}^2}. \tag{2.8}$$

where Q and L are the quality factor and the inductance value of the tank inductor, respectively. Here ω_0 is the internal angular velocity of the ILO, and the internal frequency of ILO is $\omega_0/2\pi$.

The nonlinear gain block in Figure 2.5 (a) represents the transconductance gain provided by M_1 (or M_2 in the other half circuit), and the relationship between the its input AC voltage (v) and its output AC current (i) is illustrated in Figure 2.5 (b). By assuming that M_1 is always working in the saturation region, transconductance gain g_m is constant, as shown in Figure 2.5 (b). However, the current output of M_1 cannot exceed the total current of M_1 and M_2, which is the current value of I_{sink}. Here i_{max} is used in the AC model to represent the upper bound, and $-i_{max}$ is the lower bound, of the AC current of M_1, where $i_{max} = \frac{1}{2} I_{sink}$. Such saturation effects are included in Figure 2.5 (b). The abrupt transition of the slope in Figure 2.5 (b) is an approximation. In reality, such transition would be smoothed if more detailed transistor operations are considered. However, the linear and saturation representation of the transistor in Figure 2.5 (b) provides an accurate and computationally efficient way in the simulation.

The current gain block in Figure 2.5 (a) provides an easy way to adjust the injection strength, which can emulate the function of a current amplifier (CA). The noise source i_N in Figure 2.5 (a) represents the device noises existing within the ILO. Such noise source is essential to trigger the ILO or a general oscillator to start the oscillation even when no external injection signal is applied. The noise source can be modeled as Gaussian noise with zero average and variance of $\sqrt{N_0}$. We can implement the model of Figure 2.5 in the numerical simulation platform MATLAB/Simulink [70].

Above all, a numerical model is demanded to simulate the details of the locking process for arbitrary injection signal, especially when the injection signal contains noise or interference. The numerical model in Figure 2.5 is a good choice, which not only abstracts the behavior of the ILO from the circuit transistor level and speeds up the simulation, but also incorporates nonlinear device characteristics and can simulate arbitrary signal injection.

So far, the analyses and the simulations of the ILO were limited to the sinusoidal injection for the frequency division purpose in the literature (e.g., see [71]). Though the ILO has been used in the CM-CDR schemes, most of the publications on that only presented the experimental results as proof-of-concept (e.g., [72]). The BM-CDR scheme utilizing the ILO with the injection from the converted data signal has been recently published, again in the experimental demonstration without the proper behavior modeling (e.g., [73]). To our best knowledge, no one has studied the ILO behavior through high-level behavioral

simulation in the application of clock recovery, especially in the case of being injected by NRZ data with embedded clock tone. The numerical model adopted here is a powerful tool to simulate the ILO behavior in such situation and will be used in the extensive simulation and analysis later.

2.2 Effect of Fiber Dispersion

We will now discuss on the effect of the fiber dispersion on the optical modulated data signal generated by the externally modulated laser (EML) based transmitter. In our analysis, the EML in the transmitter is the Mach-Zehnder amplitude modulator, and it is assumed to be ideal with zero chirping. The normalized baseband representation of the output optical field is [6, 74]:

$$E(t) = \frac{1}{2}\left[\exp\left(\frac{j\pi}{4}\phi(t)\right) + j\exp\left(-\frac{j\pi}{4}\phi(t)\right)\right], \tag{2.9}$$

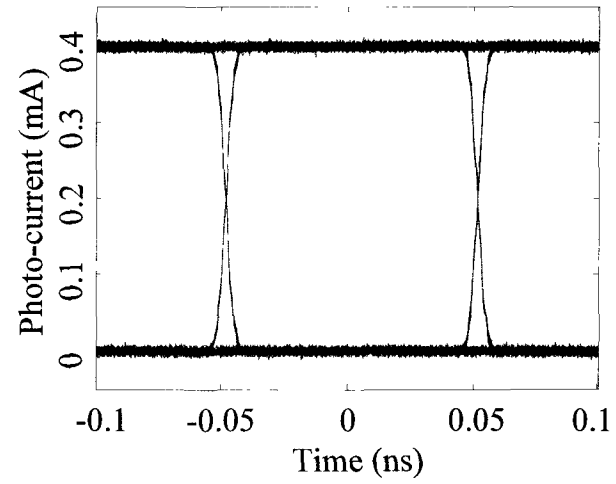
where $\phi(t) = \sum_{k=-\infty}^{+\infty} b_k p_s(t-kT)$ is the normalized binary modulation signal. Here $b_k = 1$ for binary ONE and $b_k = -1$ for binary ZERO. Here $p_s(t)$ is the electrical driving pulse shape, and T is the bit interval. The $p_s(t)$ is usually the raised cosine pulse with rolling factor as, e.g., 0.17, to soften the signal pulse shape [75], which can emulate the actual signal pulse.

To observe the performance of the EML, we can numerically modulate the EML by the $2^{31} - 1$ pseudo-random bit sequence (PRBS) data pattern at 10 Gbps, and feed the generated optical signal directly into the photo-detector. This

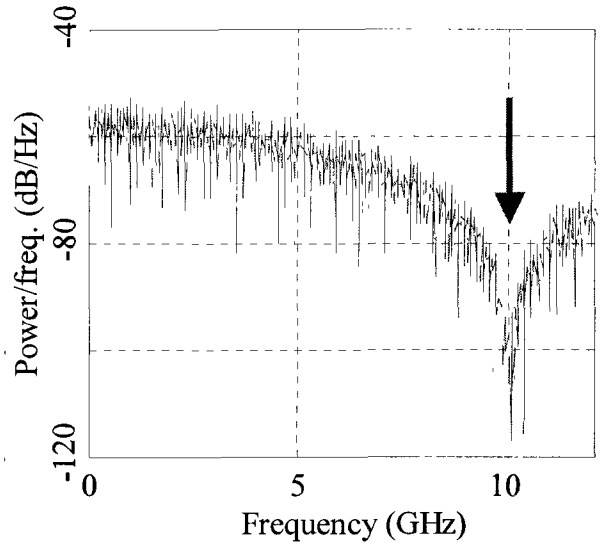
configuration is called back-to-back (B-to-B). The EML output optical power for binary ONE is 0.4 mW, and its power for ZERO is 0 mW. The electrical noise in the photodetector and the receiver circuit is also included with the power density as 10^{-20} A^2/Hz as indicated in [76].

In Figure 2.6, we plotted the eye diagram and the power spectral density (PSD) of the photo-current from the B-to-B configuration. The photo-current is still in the NRZ format. The PSD shown in Figure 2.6 (b) has very little power density at 10 GHz, indicated by the arrow. This is expected since the PRBS signal has zero power density at the bit rate theoretically [24]. Since the clock recovery circuit usually needs the clock tone at the bit rate to provide the frequency reference, the B-to-B data current cannot be used directly. We will see that the fiber dispersion can change the PSD of the received current in favor of the clock recovery.

In our simulation to demonstrate the fiber dispersion, the optical fiber is a standard single mode fiber (SMF) specified in G. 652 [11], and only the attenuation and the group velocity dispersion (GVD) of the fiber are considered in the fiber model. The higher order dispersions, the nonlinearity and the polarization model dispersion (PMD) are not considered. Such assumptions are valid for the situation with a data bit rate up to 10 Gbps, a moderate fiber span, a low optical power at the transmitter side and a relative large GVD value [77]. Furthermore, such assumptions are necessary to prove that the GVD in the fiber is the only cause to the clock tone generation phenomenon to be presented later.



(a)



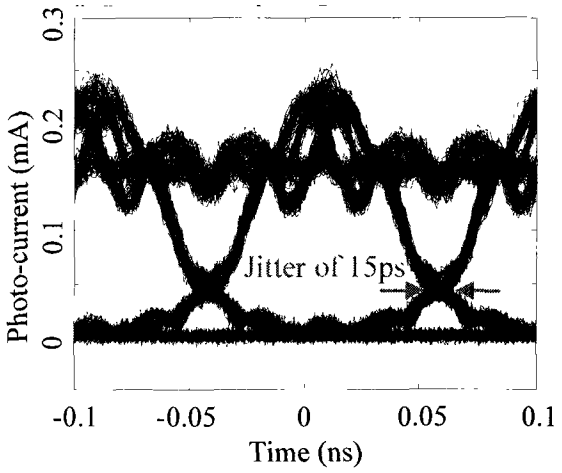
(b)

Figure 2.6 (a) The eye diagram and (b) the power spectral density of the back-to-back received electrical current from EML outputsity.

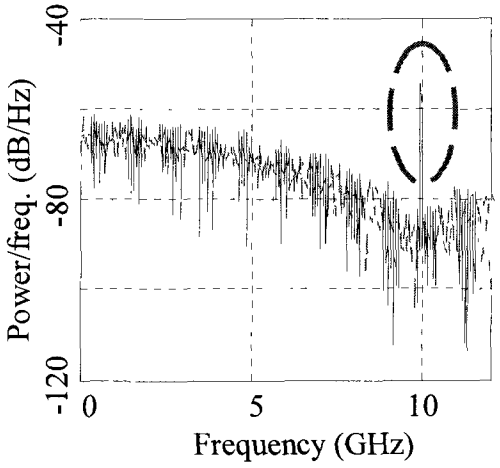
The effect of the GVD on the optical signal can be calculated as follows. For any optical signal generated from the modulator, we can first perform the Fourier transform to convert the transmitted normalized baseband time-domain optical signal $E_{Tx}(t)$ to the frequency-domain optical signal $\widetilde{E}_{Tx}(f)$. Then the received optical signal $\widetilde{E}_{Rx}(f)$ with the effect of the attenuation and the GVD in the fiber is calculated by [77]:

$$\widetilde{E}_{Rx}(f) = \exp\left[\frac{1}{2}\left(-\alpha + j\beta_2(2\pi f)^2\right)Z\right]\widetilde{E}_{Tx}(f), \tag{2.10}$$

where α is the fiber attenuation, β_2 is the GVD dispersion parameter, and Z is the fiber length the signal is transmitted over. Then the received optical signal $E_{Rx}(t)$ in the time domain is calculated by performing the inverse Fourier transform on $\widetilde{E}_{Rx}(f)$. We assume that the EML optical signal has the wavelength at 1550 nm, which is for the future long-distance PON [10, 12-14]. The attenuation of the G. 652 SMF is 0.2 dB/km, and the GVD dispersion can be calculated by the parameters and formula in [11], to be -20.4 ps^2/km. The fiber length is assumed to be 20 km. The same photodetector for the previous B-to-B case is used to convert the optical data signal to the electrical current. The simulated eye diagram and the PSD of the resulting photo-current after fiber transmission are shown in Figure 2.7. As shown in Figure 2.7 (a), the data signal is distorted by the fiber dispersion. The distorted waveform demonstrates the signal component with frequency at bit



(a)



(b)

Figure 2.7 (a) The eye diagram and (b) the power spectral density of full-fiber received electrical current from the EML output.

rate (i.e., the clock frequency), namely the clock tone, as shown in Figure 2.7 (b).

We have learned that without the fiber, there is no clock tone generated at the bit rate (see Figure 2.6). By inserting the fiber, the clock tone is generated, so the cause of such phenomenon is the fiber. Furthermore, we turned off the attenuation effect (setting the attenuation as zero), and observed that such phenomenon still exists. In this way, we can conclude that the clock tone generation phenomenon is solely from the fiber GVD, since we only considered the GVD and the attenuation in the fiber model.

Such clock generation phenomenon is a nonlinear phenomenon. In a purely linear system, there would be no signal with new frequency generated. As is well known, the fiber dispersion and the attenuation are linear effects, and the fiber with only the two effects can be regarded as a linear system. The NRZ data has a null at the bit rate in its spectrum. If the NRZ optical data is passed through the fiber, the resulting signal in optical domain would not have a signal at the bit rate, otherwise, there would be a new signal with a new frequency generated. However, the MZI modulator and the photo-detector (with square-law characteristics) are the nonlinear components. They generate the new frequency signal at bit rate through a complex way [78]. Such nonlinear phenomenon is preferred to be demonstrated through the extensive large signal numerical simulation, rather than the analytical analysis. In fact, the analytical analysis part in [78] does not represent the actual case due to its simplification of the EML

driving signal as a pure sinusoidal waveform. This simplification is far away from the practical driving signal waveform. Though the whole clock tone generation phenomenon is nonlinear, it shall be noted that such process happens with the aid of the linear fiber dispersion. In the simulation, if the dispersion is zero, no clock tone is generated.

Let us see how the dispersion generated clock tone can help in the clock recovery process from Figure 2.8, which is the waveform of the data photo-current. In the figure, we can observe that the oscillations appear on top of the original NRZ data pulses, and the most significant oscillations are observed as overshoots at the rising and falling edges of the original NRZ data. These overshoots can be deemed as the added PRZ pulses to the original NRZ data signal, and the overall waveform can be intuitively decomposed into the NRZ data and the PRZ pulses. These PRZ pulses inherit the frequency and the phase of the original NRZ data. It is known that the PRZ pulses can exhibit the frequency component at the bit rate, which can be used as the reference for the clock recovery (e.g., [73]). The spectrum of the resulting waveform in Figure 2.7 (b) demonstrates this phenomenon by exhibiting a precise frequency component at exactly 10 GHz. We learned that there were several other methods to generate such PRZ pulses from the NRZ data, however, they have the main drawback because they have to add an additional electrical circuit block to perform such pulse generation. In our proposed scheme later, we can prevent such drawback by utilizing the existing fiber dispersion in the transmission link to perform the clock

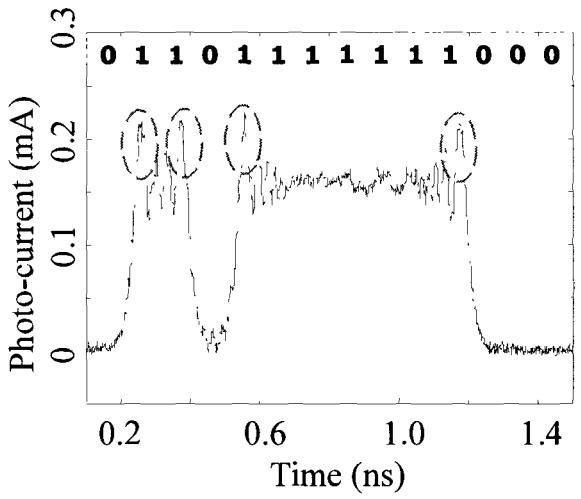


Figure 2.8 Waveform of received photo-current.

tone generation, which does not need to add any additional optical or electrical component.

It shall be noted that the clock tone cannot be directly used as the clock for following two reasons. One is that the clock tone is not continuous (i.e., sinusoidal) and with stable amplitude. It is strongest when the corresponding data signal makes transitions between ONE and ZERO (i.e., transition from ZERO to ONE, or vice versa), as shown in Figure 2.8, marked by circles. However, it is weaker when there is no level transition in the data signal, and it even disappears in the long consecutive bits (i.e., long ONE or long ZERO). The other reason is that the clock tone is embedded in the data signal. The data signal which is not at

the bit rate frequency serves as noise or interference for the clock. In order to use the clock tone for data decision, the data signal needs to be removed.

This phenomenon of clock tone generation by the fiber dispersion has been discovered in year 2001 [79]. However, it has never been used to assist the burst mode clock recovery. Recently, it has been used to do CM clock recovery, however, using the all-optical scheme in the complex optical differential phase shift keying (DPSK) transmission system [80]. In this work, we use this phenomenon for the BM-CDR employing an electrical ILO circuit.

The dispersion and the receiver noise add phase variation (i.e., jitter) of 15 ps in the received data signal, as shown in Figure 2.7 (a), compared to the B-to-B case, as shown in Figure 2.6 (a), which is jitter free. We will use this phase variation value later to demonstrate the capability of phase variation reduction of our proposed BM-CDR.

2.3 Proposed Scheme

Figure 2.9 shows the detailed system configuration for a BM optical link utilizing the dispersion generated clock tone. The transmitter (Tx) is a conventional EML transmitter which employs an external optical modulator (MOD) to modulate the optical signal generated from the laser diode (LD) operating at 1550 nm range. The PRBS data from the pulse pattern generator (PPG) working at 10 Gbps is fed into the modulator. The modulated optical signal is then transmitted through a span of G.652 SMF.

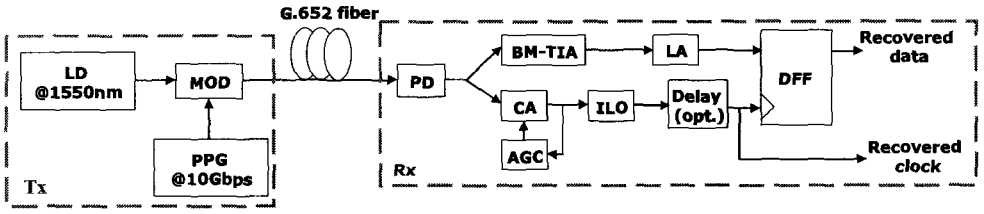


Figure 2.9 The proposed system configuration for a BM optical link (Tx: transmitter, LD: laser diode, MOD: optical external modulator, PPG: pulse pattern generator, PD: photodetector, TIA: transimpedance amplifier, LA: limiting amplifier, CA: current amplifier, ILO: injection locking oscillator, AGC: automatic gain controller, and DFF: D-flip-flop).

At the receiver (Rx), the optical signal is first converted into the electrical current through a photodetector (PD), and then the current is fed into two paths, namely the data recovery path and the clock recovery path. In the data recovery path, the data is converted from current to voltage by a burst mode transimpedance amplifier (BM-TIA) (e.g., [39]), and then further amplified and reshaped by a limiting amplifier (LA). The BM-TIA used here is to compensate the huge dynamic range of the received packet amplitudes from various transmitters with different distances with the Rx and/or after experiencing different optical power splitter loss. The BM-TIA has been extensively researched and one of its key components is the burst mode automatic gain controller (AGC) (e.g., [39]). The AGC can enable the TIA gain tunable within a short time [5].

In the clock recovery path, the photo-current is amplified by a current amplifier (CA) controlled by the AGC similar to that for the BM-TIA [39] and the amplified current is injected into the ILO. It is assumed that the AGC can adjust the CA gain to its desired value in a negligibly short time. The ILO recovers the embedded clock information (i.e., the clock tone) from the injected current, and then outputs the clock in voltage. An electrical delay block could be inserted after the ILO, if necessary, to compensate the fabrication mismatch between the clock and data recovery circuitries. Finally, the amplified data and recovered clock tone are fed into the data decision circuit, e.g., a D-flip-flop (DFF), to obtain the data message. This scheme is suitable for the situation when the upstream transmitters located at the ONUs employ the EML with the 1550 nm wavelength range, which is the trend for the future PON network as discussed in Section 1.1.

We set the CA gain in Figure 2.9 as a negative value. Such negative value can be realized by reversing the polarity of current injection in the corresponding actual circuit. The reason of doing so is elaborated as follows. As we learned in Section 2.1 , the locked ILO would have the same phase as the injected clock tone. In Section 2.2 , we also learned that the dispersion generated clock tone has the same phase as the original NRZ data. If the injection data current in the clock recovery path does not changes its polarity, the recovered clock would have the same phase as the NRZ data in the data recovery path. However, the decision circuit (i.e., the DFF in Figure 2.9) prefers to have the phase of its clock input 180 degree different from that of its data input, in order to align the rising edge of the

recovered clock in the clock recovery path to the center of the data eye in the data recovery path. The decision circuit usually performs the data decision at the time when the clock rises and reaches its average value. By changing the polarity of the injection current to the ILO, the decision circuit can perform the correct data decision. The above analysis assumes that the transmission delays through the BM-TIA, the CA, and the LA are ignored, as well as the delays in the interconnection lines between them. If the transmission delays between the clock recovery path and the data recovery path have some mismatch, the optional delay element in Figure 2.9 can be used to compensate such mismatch.

There are two main contributions in this proposed clock recovery scheme. Firstly, the clock tone resulted from the fiber dispersion is utilized for the first time in the electrical ILO based clock recovery circuitry. Secondly, this is the first design to directly inject the signal in current (instead of injecting voltage as in [81] and using some circuit block to convert it into the current injection) to the ILO. This reduces the design complexity by eliminating the circuits used in the current-to-voltage and voltage-to-current conversions.

2.4 Simulation and Discussion

We have simulated the eye diagram, waveform and spectrum of the received photo-current, as shown in Figure 2.7 and Figure 2.8. We then need to specify the parameters of the following circuit blocks along the clock recovery path. The internal (natural) frequency f_0 of the ILO is 10 GHz to match the bit rate

of the received data. For the RLC tank, the inductor is designed to be 0.8 nH with its Q value at 10. Transconductance gain g_m is set as 10 mS, and i_{max} is set as 16.5 mA. For the CA, the magnitude of gain as 50 achieved by the single- or multi-stage amplification is used in our simulation. For the burst mode operation, because the data are received at different times, the first thing we need to confirm is that the ILO can always lock to the data, and the relative phase of the recovered clock compared to the incoming data is always the same.

For simulation and illustration purpose to demonstrate the phase difference between the injected data and the recovered clock, instead of injecting the data signal to the ILO at different times, the data signal injection is fixed at 5 ns but the ILO is turned on at different times, namely at 0 ps, 25 ps, 50 ps and 75 ps, respectively. In this case, for the injection at a fixed time, under the locked conditions the recovered clocks should not depend on when the ILO is turned on, because the relative phases between the locked clocks and the incoming data should be the same for all cases.

The method of starting the ILO at different times can also emulate the different original clock phases which should have been locked to the phases of previous optical packets. Therefore the burst mode locking capability can be verified by checking if the waveforms of the locked clocks are overlapped with each other for the cases of different original phases. Such method to use limited but sparsely distributed cases of different original clock phases to estimate the locking time is a common practice in the published papers (e.g., [31]).

The data signal used is the $2^{31} - 1$ PRBS instead of the alternative ONEs and ZEROs defined in [82]. The PRBS data provide fewer bit transitions (between ONE and ZERO) than the alternative ONEs and ZEROs (simplified as "1010"), and is expected to reduce the averaged clock tone strength and prolong the locking time. In the following simulation, we will demonstrate that even using the PRBS, the locking time can still be short.

Furthermore, if the PRBS data can be used to perform the clock locking, then there is possibility to design the receiver architecture to enable the preamble-free clock locking. For example, we can feed the arriving optical data signal into two fibers. One fiber without delay is for the purpose of the clock recovery, the other one with proper delay using a fiber delay line (FDL) is for the data recovery. Then the recovered clock and the recovered data are fed into the DFF for data decision. This architecture is similar to the technique in the optical header processing for optical label switching [83]. In this way, when the unlocked clock arrives at the DFF, the data is still in the FDL, so no incorrect data decision would be made; when the fully locked clock reaches the DFF, the delayed recovered data reaches the DFF at the similar time, and the data decision can be done correctly.

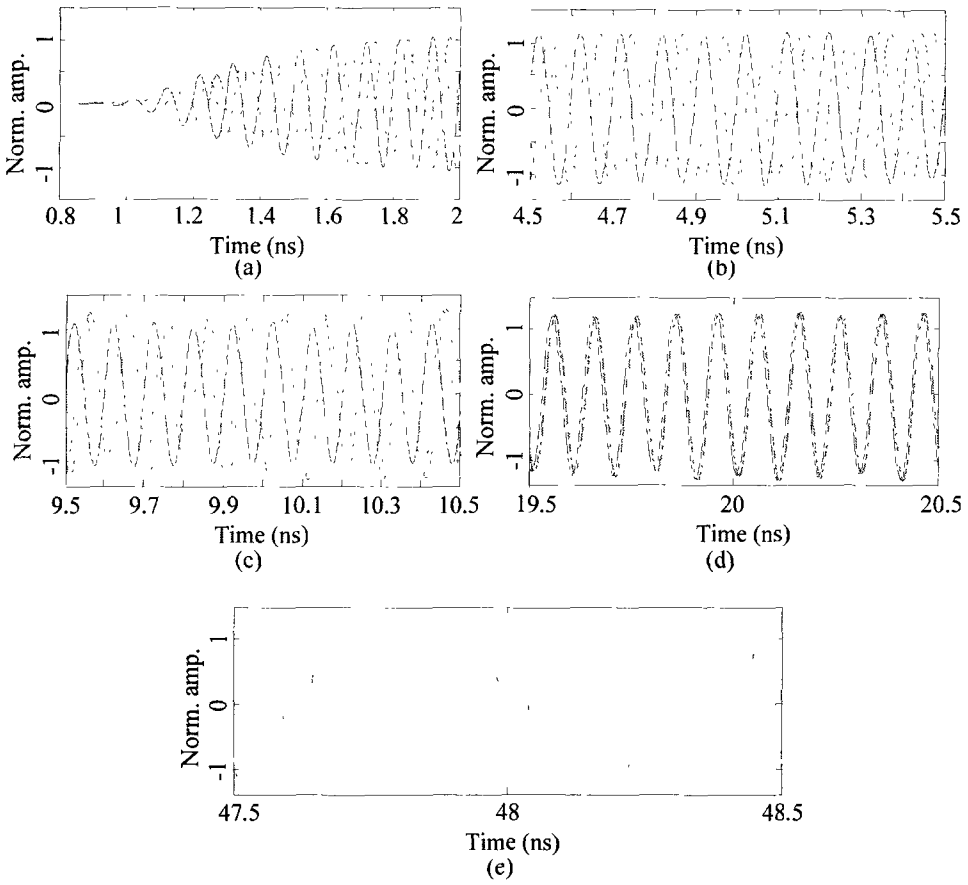


Figure 2.10 Evolution of the recovered clocks in normalized amplitude (norm. amp.) as a function of time at around (a) 1.4 ns, (b) 5 ns, (c) 10 ns, (d) 20 ns, and (e) 48 ns, respectively. Different sinusoidal-like waveforms represent different injection cases at 10 Gbps.

The PRBS data signal is injected to the ILO at 5 ns to ensure that the ILO reaches its stable oscillation state before performing the clock locking. Figure 2.10 shows the waveforms of the output clock as a function of time at around 1.4

ns, 5 ns, 10 ns, 20 ns, and 48 ns, respectively, for different cases. When the ILO just oscillates (see Figure 2.10 (a)), the phases are all different because the ILO is turned on at different times. Before the data is injected into the ILO at 5 ns, the clock phases are different as shown in Figure 2.10 (b). After the data is injected at 5 ns, as shown in Figure 2.10 (c), (d), and (e), all the waveforms gradually overlap with each other and this confirms the locking capability of the proposed scheme.

The evolution of the clock waveforms provides the insight on how the ILO locks to the incoming data. To analyze the locking time for different injection cases, we can plot the normalized relative phase as a function of time. Before we do so, we choose the ideal data bit at the input of the receiver as the reference and define the normalized relative phase as:

$$\text{Normalized relative phase} = \frac{\Delta T_p}{T_{bit}}, \tag{2.11}$$

where T_{bit} is the period of the ideal data bit, and ΔT_p is the time duration between the zero-crossing position of the signal of interest and that of the ideal data bit. The signal of interest in ΔT_p could be the data injected at the ILO input or the recovered clock at the output of the ILO. The ideal data bit used in (2.11) is the data bit at the input of the receiver without any distortion. Figure 2.11 shows the timing diagram to illustrate the definition of the normalized relative phase. The zero-crossing position, where the waveform crosses the 0 volt, is defined at the rising edge of the signal.

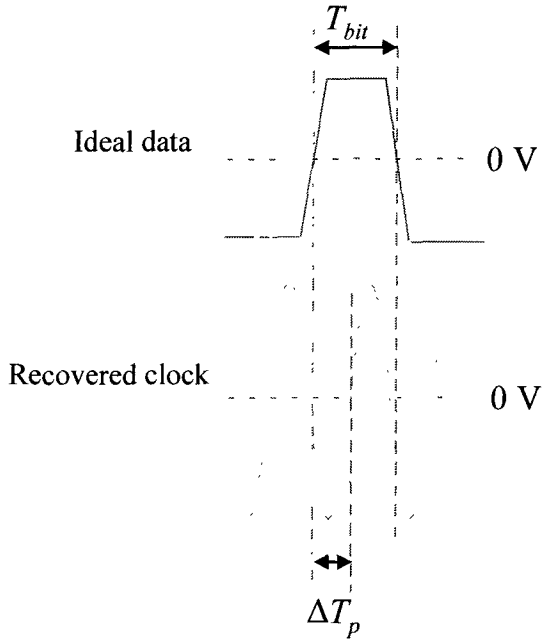


Figure 2.11 Timing diagram showing the definition of the relative phase for the recovered clock.

In Figure 2.12, different lines are used to differentiate different injection cases. As observed, four lines with different initial phases converge at around 35 ns, which can be regarded as the coarse locking. We can observe that after sufficient long time (e.g., after 80 ns), the phase variation is within 2% of the average phase. So that we can define the fine locking time as the time at which the phase variation is less than 2%. This is how we determine the fine locking happens at 58 ns as shown in Figure 2.12 and the locking time is 53 ns (i.e., 58 ns – 5 ns). In addition, the received data before the clock recovery circuitry has the peak-to-peak jitter of 15% (see Figure 2.7 (a)) and our clock recovery scheme

improves the jitter performance of the received data by 87%. Jitter may also be alternatively reduced by the data dependant jitter equalizer before the clock recovery [84] or the jitter reduction circuit after the clock recovery [85]. However, such added circuit blocks increase the total power consumption and the design complexity. In this work, we chose to use a much stricter criterion of phase variation (e.g., 2%) to define the locked state than most of the published papers (e.g., 10% in [31]).

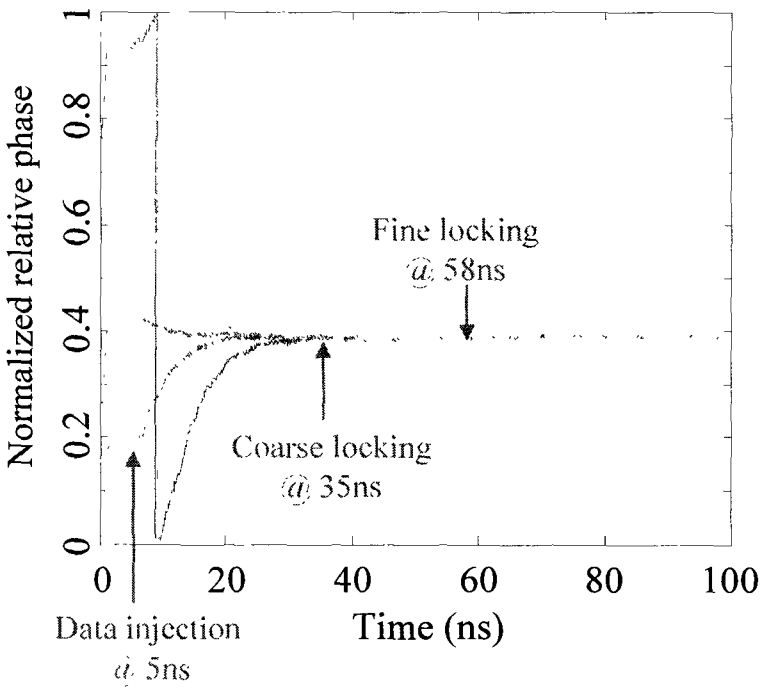


Figure 2.12 Phase evolutions of the recovered clock as a function of time for different injection cases at 10 Gbps.

From Figure 2.12, we can also observe the characteristics of the ILO locking process. The instantaneous clock phases for all the cases monotonically approach their final value, without oscillation as in the PLL phase or frequency locking process [30]. The small noise in the phase evolution is due to the effect of the random data pattern, which is the interference to the locking process.

The CA gain can change the locking time, but it does not change the final clock phase under the locked condition. This is because at that time the clock is always locked to the phase of the injected data, independent from the magnitude of the data. To study the impact of the CA gain on the locking time, Figure 2.13 shows the locking time as a function of the CA gain for different fiber spans. It is shown that for each fiber span, there exists an optimal current gain for the shortest locking time. If the gain is smaller than the optimal value, the resulting clock tone is not strong enough for an efficient locking, leading to longer locking time. If the gain is larger than the optimal value, the NRZ data signal is also amplified to a level to saturate the nonlinear gain block in the ILO and interfere with the locking process. This increases the locking time. In addition, when the fiber span increases, the optimal current gain also increases as expected. This is due to the higher fiber attenuation to be compensated. On the other hand, for longer fiber span, the resulting optimal locking time is shorter. This benefits from the stronger clock tone due to the additional accumulated fiber dispersion.

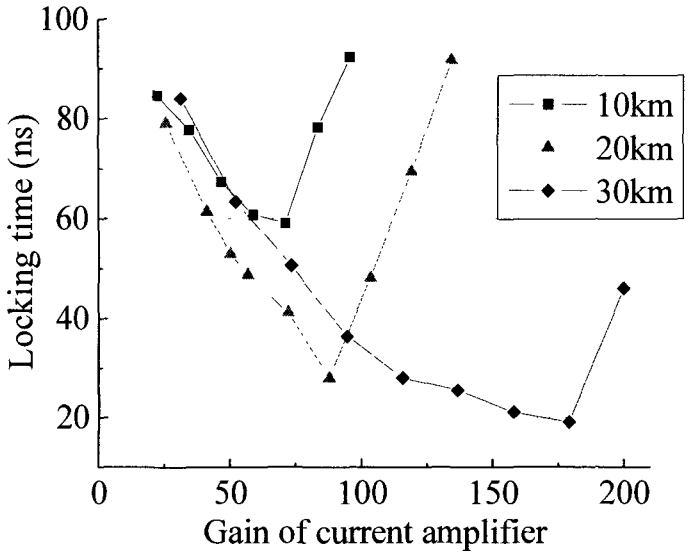


Figure 2.13 Locking time vs. current gain characteristics for different fiber spans at 10 Gbps.

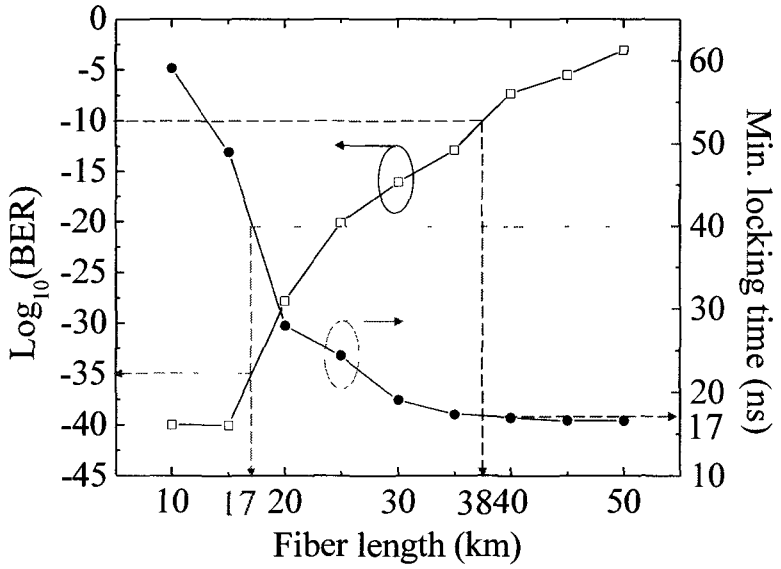


Figure 2.14 BER and optimal locking time vs. fiber length at 10 Gbps.

On the other hand, the BER might stop us from using long span fiber because of the accumulated dispersion and the attenuation along the fiber. Figure 2.14 demonstrates the optimal BER calculated by the model in [86], and the shortest locking time (corresponding to each optimal current gain) as a function of fiber length. Because of the dispersion caused distortion, the BER is worse than that when only receiver noise is considered. When the fiber length increases, the BER becomes worse as expected, since the dispersion is accumulated, leading to more data signal distortion. On the other hand, the optimal locking time decreases when increasing the fiber length from 10 km to around 40 km. The improved locking time for a fiber span shorter than 40 km is due to the enhanced clock tone by the accumulated fiber dispersion [79, 80].

As seen in Figure 2.14, the locking time reduction starts to saturate when the fiber length is about 40 km, this is due to the saturation of the clock tone strength [79, 80]. The decrease of the clock tone and the corresponding increase of the locking time would happen when fiber length is longer than 50 km, for the NRZ 10 Gbps data and G.652 SMF. A fiber span longer than 50 km would not be directly used in a practical system for 10 Gbps transmission since the corresponding BER is larger than 10^{-5}. If a dispersion compensation fiber (DCF) [86] is inserted before the receiver to compensate the accumulative dispersion in order to improve the BER, the equivalent dispersive fiber length will be reduced to within 50 km, and the total generated clock tone will be still strong enough to aid the BM-CDR. Here the equivalent dispersive fiber length is calculated as the

sum of the accumulated dispersion from the original fiber and the opposite polarity dispersion provided by the DCF, divided by the dispersion parameter of the G. 652 SMF. The above discussion on the equivalent dispersive fiber length and its affect on a generated clock tone is valid when the optical power is low and the fiber transmission link is approximately linear, which is the case for the practical system [77].

Figure 2.14 provides the very useful information in the determination of the feasible fiber length or equivalent fiber length if DCF is used, to perform the BM-CDR scheme. For example, if we choose the commonly used 40 ns as the maximum clock recovery preamble time as suggested in [5, 31], this determines the shortest fiber length to be 17 km with BER of 10^{-35}. On the other hand, an acceptable BER in an optical link should be lower than 10^{-9} [86, 87]. We put a stricter requirement of BER to be 10^{-10}. This determines the longest fiber length to be 38 km with a minimum 17 ns locking time. The fiber length limitation for BER is mainly due to the fiber GVD. If only the attenuation is considered, by assuming a –27 dBm receiver sensitivity, the attenuation limited fiber length is 133 km. From the above analysis, our proposed scheme working at 10 Gbps is suitable for a wide range of fiber spans from 17 km to 38 km, and guarantees that the locking time is shorter than 40 ns and the BER is smaller than 10^{-10} without specific preamble bit patterns. If the proposed scheme is used in the optical transmission link with a fiber span shorter than 17 km, an additional highly dispersive fiber or a discrete dispersive element can be inserted before a burst mode receiver or after

the transmitter to enhance the dispersion to meet the required locking time. On the other hand, the fiber length can exceed the 38 km limitation if DCF is inserted before the receiver or after the transmitter, while keeping the accumulated dispersion sufficient to achieve the specified locking time. Above all, the fiber span reach can be further explored to either shorter or longer length, while keeping the BER and locking time within specification. In addition, the DCF may not be required to improve the BER. The electrical dispersion compensation (EDC) circuit [88] can be used to compensate the distortion of the dispersion in the data signal, performed in the electrical circuits after the clock recovery, without decreasing the clock tone strength for the clock recovery.

In the simulation, the PD and the CA are assumed to have the infinite large bandwidth and flat gain profile, which is to simplify the simulation and analyze the key phenomenon and the key parameter effect. In the practical designs, it is preferred to have the bandwidths of the PD and the CA larger than the bit rate, so that the clock tone embedded in the received data is not filtered out. On the other hand, even if the PD and the CA have slightly smaller 3-dB bandwidth than the bit rate, the filtered clock tone could be still strong enough for the clock recovery, since the cut-off shapes of the circuits transfer functions (usually low-pass) are not infinitely sharp. Furthermore, the attenuation due to the circuit transfer functions can be compensated by increasing the CA gain.

The wideband amplification can also be easily achieved optically. For example, a semiconductor optical amplifier (SOA) with AGC can be put in front

of the PD to provide the wideband amplification to the optical data signal [41]. Such SOA can be used to provide the gain to compensate the dynamic range of the optical packets amplitudes, and to strengthen the clock tone at the same time. In this way, the BM-TIA as well as the CA and its associated AGC in Figure 2.9 can be eliminated, simplifying the design and reducing the total chip area. Furthermore, the SOA can be integrated with the photo-detector [89], reducing the receiver size and the packaging costs. If the gain-controlled SOA is used to replace the CA and its associated AGC originally used in the clock recovery path, the gain of the SOA provides the equivalent CA gain originally used in the simulation, and the above simulation and analysis is still valid.

Chapter 3
BM-CDR USING DML RELAXATION OSCILLATION

In the conventional PON, the BM upstream data link uses the wavelength at around 1310 nm, which does not provide dispersion when the general G.652 fiber is used. In this case, the directly modulated laser (DML) is usually employed at the ONU transmitter, to transmit the BM data signal. In this chapter, the photo-detected spectrum of the DML output is analyzed to illustrate the clock tone generation by the relaxation oscillation. The corresponding application in the BM-CDR is then demonstrated through extensive simulation.

3.5 Effect of DML Relaxation Oscillation

The semiconductor laser can be modulated directly by injecting the modulating current into the laser, which can change the instantaneous photon density inside the laser cavity, and the corresponding output optical power. The dynamics of the DML laser can be described by the following rate equations [90]:

$$\frac{dp(t)}{dt} = G(n,p,t)\,p(t) - \frac{p(t)}{\tau_p} + R_{sp}(n,t), \text{ and} \tag{3.1}$$

$$\frac{dn(t)}{dt} = \frac{I(t)}{qV} - \frac{n(t)}{\tau_n(n,t)} - G(n,p,t)p(t), \tag{3.2}$$

where $p(t)$ is the photon density (defined by photon number in unity volume), $n(t)$ is the carrier density, which is either the density of electrons or holes (they are of the same density). They evolve with time t. Here τ_p is the photon lifetime, defined by one over photon decay rate. Photon density is reduced (decayed) inside the cavity because the photon is either absorbed by the materials in the cavity, or ejected through the cavity facet. The transmitted optical power is proportional to the ejected photons, which is again proportional to the photon density in the laser cavity [90, 91]. Here $I(t)$ is the driving current into the laser, and q and V are the electrical quantity of one electron and the volume of the active cavity of the laser, respectively. Here $\tau_n(n,t)$ is the carrier life time, and it accounts for the recombination effect of the carriers, except the effect of stimulated radiative recombination. Here $\tau_n(n,t)$ can be obtained by [90]:

$$\tau_n(n,t) = \left(A + Bn(t) + Cn^2(t)\right)^{-1}, \tag{3.3}$$

where parameter A is due to the surface recombination or trap mechanism, namely non-radiative recombination, B is due to the spontaneous radiative recombination, and C is due to the Auger recombination. More details of their physical meanings can be obtained in [90]. Here $G(n,p,t)$ is used to link the carrier density and the photon density. Here $-G(n,p,t)p(t)$ in Eq. (3.2) is due to the stimulated radiative recombination, describing the rate of the carriers consumption to recombine and generate photons, based on the instantaneous photon density. Here $G(n,p,t)$ can be obtained by [90]:

$$G(n,p,t) = \Gamma G_0 \left(n(t) - n_t\right) - G_p p(t), \tag{3.4}$$

where G_0 is the gain constant to describe the linear relationship (with offset n_t) between the gain and the carrier density, and n_t is the threshold carrier density. Here G_p is used to account for the saturation effect on the gain $G(n,p,t)$, for the gain is decreased if the photon density increases. Γ is the optical confinement factor of the active layer.

In Eq. (3.1), $R_{sp}(n,t)$ is used to consider the spontaneous emitted photons, and can be obtained by [90]:

$$R_{sp}(n,t) = \frac{\beta_{sp} n(t)}{\tau_r(n,t)}, \tag{3.5}$$

where β_{sp} is the spontaneous-emission factor. Here $\tau_r(n,t)$ is the spontaneous radiative recombination lifetime, equivalent to $1/(Bn)$. Here $R_{sp}(n,t)$ is indispensable in describing the dynamics of the DML laser. Suppose there is no photon in the laser initially, if Eq. (3.1) does not have the term of $R_{sp}(n,t)$, photons can not be generated whatever the $G(n,p,t)$ is.

The DML also has the chirping effect in the output optical signal during modulation [90]. Chirping $(d\phi(t)/dt)$ is dependant on the carrier density as shown below:

$$\frac{d\phi(t)}{dt} = \frac{\alpha}{2} G(n,p,t), \tag{3.6}$$

where α is the linewidth enhancement factor [90]. The constant frequency shift is not considered in (3.6), since it does not affect signal shape when propagating along the fiber. As we learned, Eqs. (3.1) and (3.2) do not contain $\phi(t)$, so the evolutions of photon and carrier densities in the DML are not affected by $\phi(t)$. Chirping does affect the pulse evolution in dispersive fiber [77]. However, in the case we study, there is zero fiber dispersion exhibited at DML output wavelength, 1310 nm. In this case, chirping effect can be ignored.

Above all, Eqs. (3.1) and (3.2) can be used to describe the dynamics of the DML laser and calculate its resulting waveform at the receiver side without considering Eq. (3.6), in the case of zero fiber dispersion. Under the small signal approximations of Eqs. (3.1) and (3.2), the DML laser can be modeled as an RLC equivalent circuit model [92]. It is well known that RLC tank can generate relaxation oscillation with damping for a step input. Similarly, when a step input current (i.e., input current rise from ZERO to ONE) is fed into the DML laser, relaxation oscillation also happens. The detailed explanation through theoretical formula derivation can be seen in [90, 92]. The relaxation oscillation discussed above, however, is a linear process. To demonstrate the clock tone generation phenomenon to be discussed later, the above linear approximation as an RLC tank can not be used, and nonlinear large signal simulation strictly using Eqs. (3.1) and (3.2) has to be adopted.

We use the parameters of an Agere D1861C DML in the following simulation. It is suitable for the 10 Gbps modulation, and its parameters are

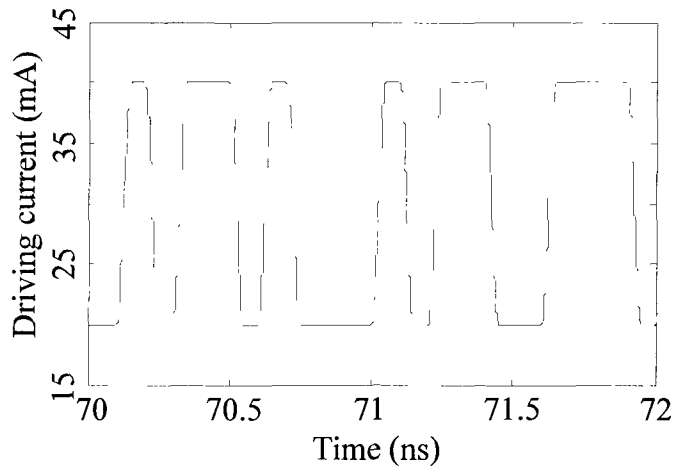
provided in OptSim [93] and listed in TABLE III. I. Except those parameters discussed above, the fiber coupling coefficient is used to account for the coupling loss when the ejected optical power from laser is coupled into the fiber connecting to the laser.

TABLE III. I Parameters Used for the DML in the Simulation [93].

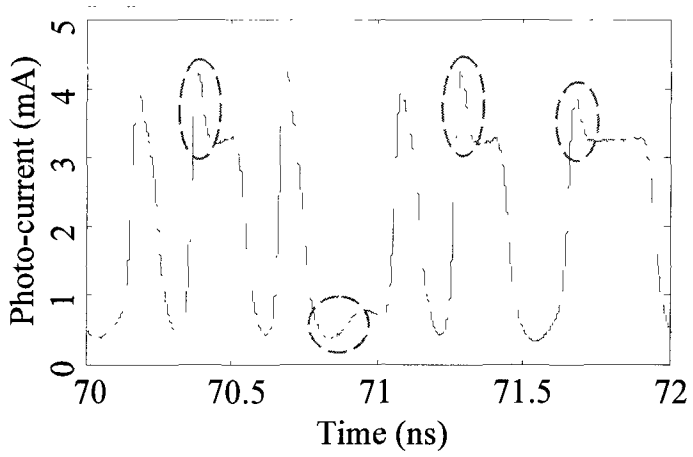
Parameters	Value
Active waveguide volume (V)	$1.73 \cdot 10^{-16}$ m^3
Photon lifetime (τ_p)	4.5 ps
Threshold carrier density (n_t)	$1.13 \cdot 10^{24}$ m^{-3}
Gain constant (G_0)	$6 \cdot 10^{-20}$ m^2
Gain derivative to photon number ($-G_p$)	$-8.6 \cdot 10^{4}$ m^{-1}
Auger recombination coefficient (C)	$9.8 \cdot 10^{-41}$ m^2/s
Radiative recombination coefficient (B)	$1.9 \cdot 10^{-16}$ m^3/s
Nonradiative recombination rate (A)	$1.02 \cdot 10^{8}$ s^{-1}
Spontaneous emission factor (β)	$3.5 \cdot 10^{-5}$
Field confinement factor (Γ)	0.78
Fiber coupling coefficient	0.22

As we learned, the fiber exhibits zero dispersion at the DML wavelength in the upstream channel in the PON. In this case, we can model the fiber as a pure

attenuator. Attenuation of G.652 SMF at 1310 nm is around 0.35 dB/km [11]. The length of the fiber in the simulation is 20 km. The threshold current of the laser with the parameters in TABLE III. I is around 15 mA. The raised-cosine driving current has 20 mA for logical ZERO and 40 mA for logical ONE. After 20 km fiber transmission, the photo-detector with same parameters as in Chapter 2 is used to receive the optical signal and convert it into photo-current. Figure 3.1 shows the simulated driving current and the received photo-current, when a PRBS data signal is used. The simulation on DML modulation is performed in large signal to consider its nonlinearity, through Eqs. (3.1) and (3.2). As can be observed by comparing between Figure 3.1 (a) and (b), the relaxation oscillations happen at the transitions between ZERO and ONE, some apparent incidents are marked by circles in Figure 3.1 (b). For the others unclear appearances such as when the data pattern is alternative ONEs and ZEROs ("1010"), relaxation oscillation still exists, and will be analyzed later in the electrical spectrum. Intuitively speaking, such relaxation oscillation generated overshoot can be regarded as PRZ pulses on top of the original NRZ data. Such PRZ pulses have the same frequency and phase of the NRZ data, and furthermore, exhibit the frequency component at the bit rate, which can be used as a frequency reference for the circuit performing full clock restoration. This is the similar case as in Section 2.2 , where the dispersion generated clock tone is used.



(a)



(b)

Figure 3.1 (a) The driving current and (b) the received photo-current for the PRBS data signal.

Though the relaxation oscillation phenomenon in the DML is well known, however, the phenomenon of the clock tone generation by the relaxation oscillation was never published to our best knowledge. Furthermore, such

phenomenon has never been utilized for clock recovery, especially for the BM-CDR. In this work, we utilize such phenomenon for the clock recovery by directly injecting the clock tone embedded data into the ILO.

3.6 Proposed Scheme

Figure 3.2 illustrates the detailed system configuration for a BM optical link utilizing DML relaxation oscillation generated clock tone.

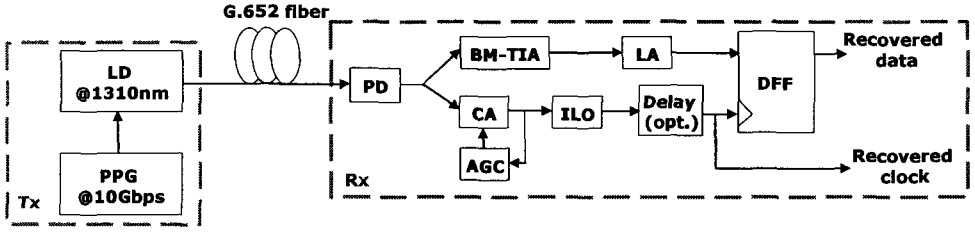


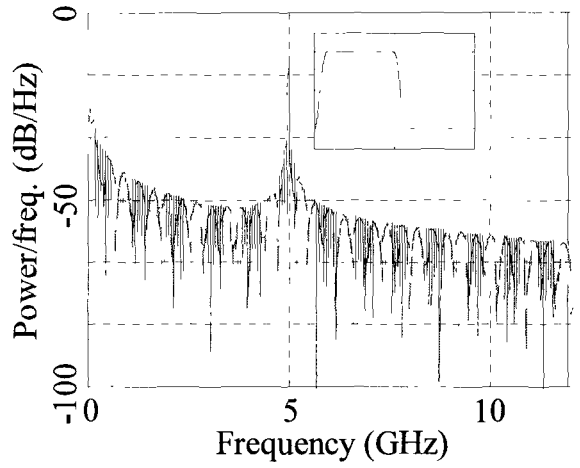
Figure 3.2 Proposed DML-based system configuration for a BM optical link (Tx: transmitter, LD: laser diode, PPG: pulse pattern generator, PD: photodetector, TIA: transimpedance amplifier, LA: limiting amplifier, CA: current amplifier, ILO: injection locking oscillator, AGC: automatic gain controller, and DFF: D flip-flop).

In Figure 3.2, the DML-based transmitter (Tx) employs a pulse pattern generator (PPG) operating at 10 Gbps to generate the data sequence which is directly fed into a conventional 1310 nm DML. The DML output optical signal is then transmitted through a span of G.652 fiber. The receiver (Rx) part is the same as the case for utilizing a dispersion generated clock tone. The detailed

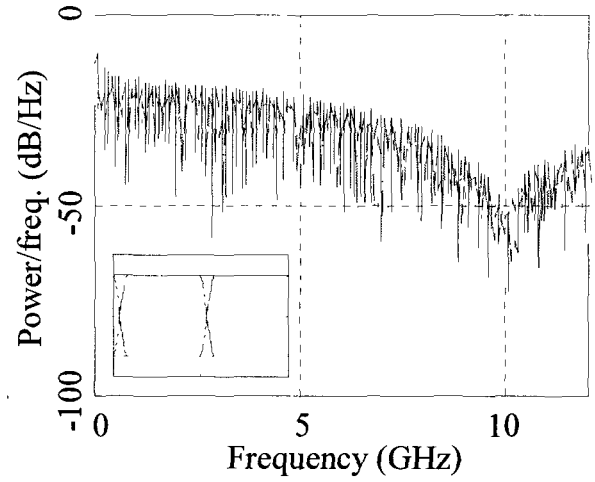
description of the Rx can be seen in Section 2.3 . This scheme is suitable for the case when the upstream transmitters are resided in ONUs use DMLs with 1310 nm wavelength window. This is the case of current PON networks recommended in specifications (e.g., GPON in [5]). Similar to Figure 2.9, CA gain has negative value to align the recovered clock at the clock recovery path to the center of the data eye at the data recovery path.

3.7 Simulation and Discussion

In the simulation, we use the system and device parameters discussed in the BM-CDR scheme utilizing fiber dispersion. The data signal is composed of "1010" repetitive sequence in the 40 ns preamble time as defined in [5], followed by the PRBS data, both at 10 Gbps bit rate. Figure 3.3 shows the simulated power spectrums and the eye diagrams of the modulation data signal at the PPG output, and the PD output photo-current, all at 10 Gbps. Figure 3.3 (a) and (b) are for the "1010" repetitive and the PRBS sequence of DML driving current, respectively. It can be seen that the driving data sequence do not contain clock tone at 10 GHz, in both cases of "1010" and PRBS sequence. In contrast, after the DML modulation and the photo-detection, the clock tone at 10 GHz appears in the received electrical spectrum for both data sequence, as shown in Figure 3.3 (c) and (d). Note that the clock tone embedded in the PRBS sequence is not continuous due to the randomness of the PRBS data sequence. The discontinuous clock tone has to be further processed by the ILO to restore it into a continuous clock. On the other

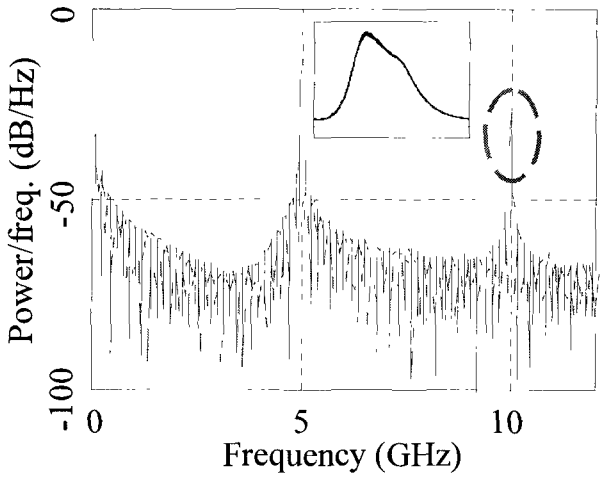


(a)

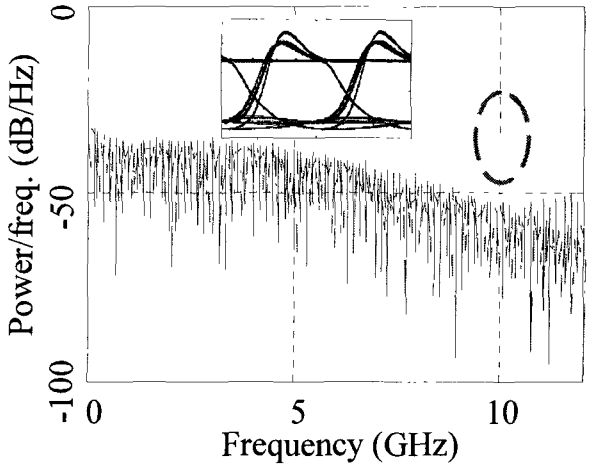


(b)

Figure 3.3 (a) (b) Power spectrums and eye diagrams of the PPG output operated at 10 Gbps. Here (a) is for the "1010" data pattern, and (b) is for the PRBS data pattern.



(c)



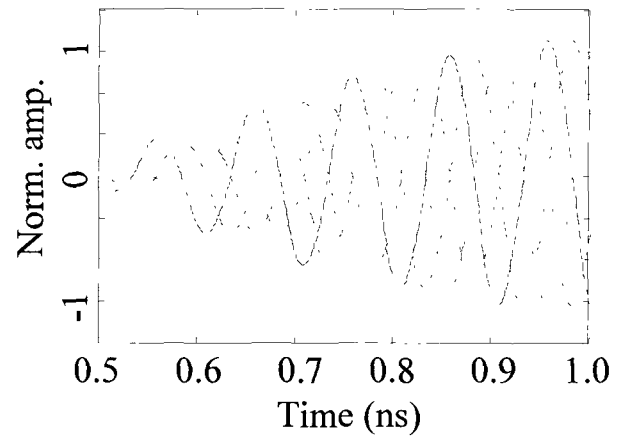
(d)

Figure 3.3 (c) (d) Power spectrums and eye diagrams of the detected DML output operated at 10 Gbps. Here (c) is for the "1010" data pattern, and (d) is for the PRBS data pattern.

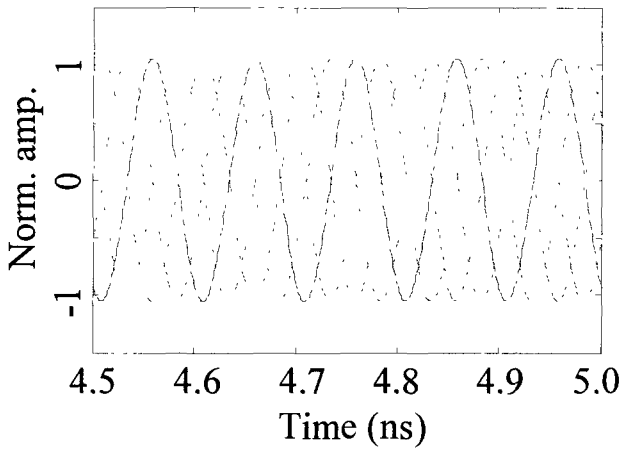
hand, the resulting clock tone corresponding to the first 40 ns "1010" sequence is continuous; however, the ILO is still needed to remove the unwanted data components.

The relaxation oscillation phenomenon is usually analyzed by the small-signal analysis [90]. However, the clock generation phenomenon has to be discovered through the large signal analysis by including the nonlinear effect. Such clock generation phenomenon, as shown in Figure 3.3, has never been published. It is noted that the frequency of the clock tone demonstrated in Figure 3.3 does not depend on the relaxation oscillation frequency of the DML. In fact, the DML relaxation oscillation frequency is obtained in small-signal linear analysis, and such frequency changes depending on the biasing for the small-signal analysis [90]. For the large signal modulation, there is no demonstrated relaxation oscillation frequency tone in the resulting spectrum, as shown in Figure 3.3. In another word, the DML does not need to be designed to have its relaxation oscillation frequency at the bit rate for this scheme. For example, the relaxation oscillation frequency of the simulated DML is at 8.6 GHz when biased at 40 mA, different from the bit rate of 10 Gbps.

In the following clock recovery circuit, the natural frequency f_0 of the ILO is 10 GHz to match the bit rate of the incoming data. For the RLC tank, the inductor is designed to be 0.8 nH with its Q value at 10, the same values as the ones used for dispersion generated clock tone case. Transconductance gain g_m is set as 20 mS, and i_{max} is set as 33 mA. For the CA, the gain magnitude of 125 is

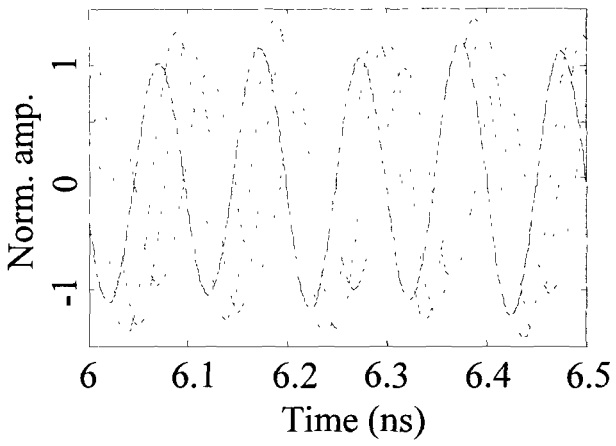


(a)

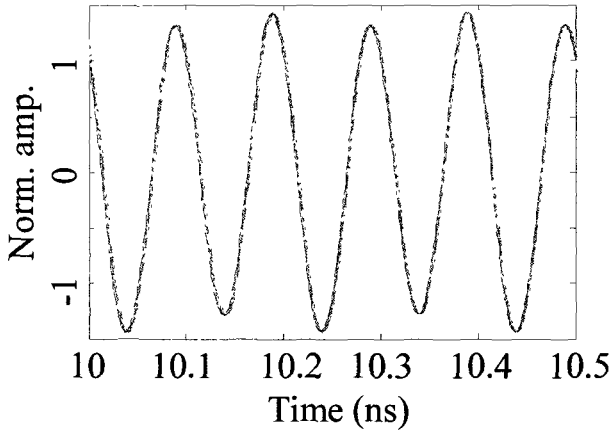


(b)

Figure 3.4 Evolution of the recovered clocks in normalized amplitude (norm. amp.) as a function of time at around (a) 0.75 ns and (b) 4.75 ns.



(c)



(d)

Figure 3.4 Evolution of the recovered clocks in normalized amplitude (norm. amp.) as a function of time at around (c) 6.25 ns and (d) 10.25 ns.

chosen in our simulation which can be achieved by a single- or multi-stage amplification. Similarly, we need to confirm that the ILO can always lock the data received at different times, and the relative phase of the recovered clock compared to the incoming data is always the same under the locked condition.

For the simulation purpose to emulate the burst mode operation, we turn on ILO at different times, namely at 0 ps, 25 ps, 50 ps and 75 ps, respectively, while injecting data signal at fixed 5 ns. Figure 3.4 shows the waveforms of the recovered clock as a function of time at around 0.75 ns, 4.75 ns, 6.25 ns, and 10.25 ns, respectively for different cases. When the ILO just oscillates (see Figure 3.4 (a)), the phases are all different because the ILO is turned on at different times. Before the data is injected into the ILO at 5 ns, the phases are different for different cases, as shown in Figure 3.4 (b). After the data injected at 5 ns, as shown in Figure 3.4 (c) and (d), all the clock waveforms gradually overlap with each other and this confirms the locking capability of the proposed scheme.

We then can observe the phase evolutions of the ILO for different turn-on conditions and plot the normalized relative phases to the received data (according to Eq. (2.11)) as a function of time in Figure 3.5. Different lines in Figure 3.5 are used to represent different injection cases. Four curves with different initial phases converge at around 11 ns and vary only within a small range after. Here we define the locking condition as when the phase variation is within 5% of the final average value. When the PRBS sequence arrives after the clock is locked to the repetitive "1010" sequence, the clock phase variation becomes a little bit

larger and demonstrates randomness. However, the variation is still within 5%. Compared to the case of dispersion assisted clock recovery, large jitter target of 5% is used. This is because the DML output data has larger jitter due to the pattern dependency problem inherent in the DML modulation method, and the embedded clock tone also has larger jitter. Though the ILO can reduce the clock jitter from the clock tone, the resulting jitter is still larger than the dispersion assisted clock recovery case. The jitter target has to be increased to accommodate this situation. However, such jitter target is still much smaller than that in the literature (e.g., [31]).

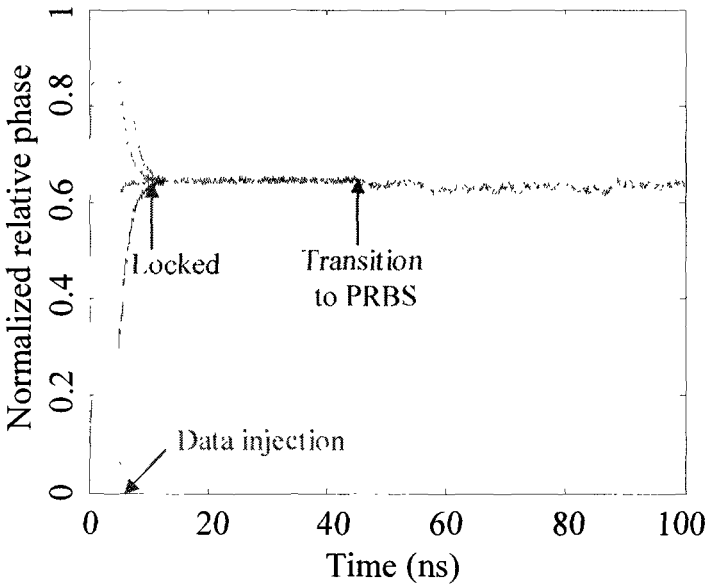


Figure 3.5 Phase evolutions as a function of time for different injection cases at 10 Gbps.

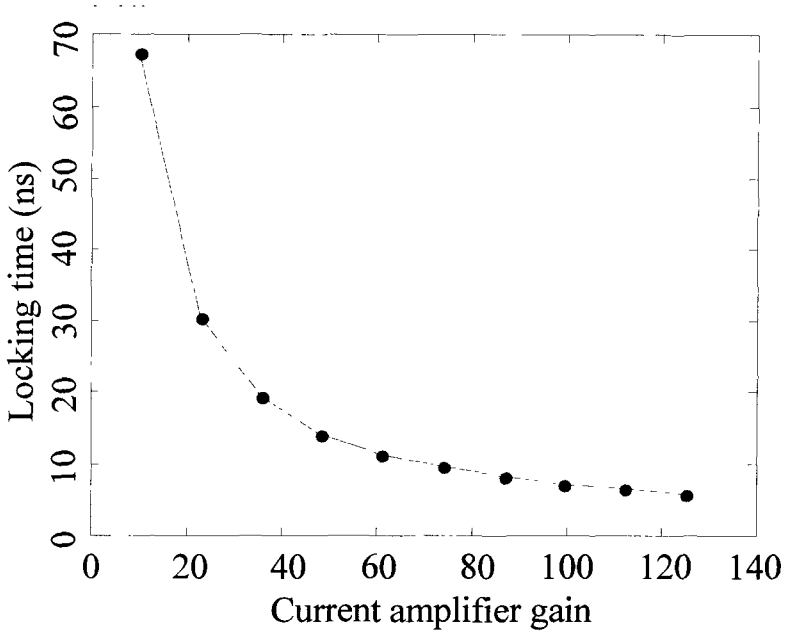


Figure 3.6 Effect of different current amplifier gains on the locking time.

Similar to the previous scheme, the CA gain in this scheme does not change the final average phase, but only the locking time and jitter. To study the impact of the CA gain on the locking time, Figure 3.6 shows the locking time as a function of the current gain. It is shown that when the current gain increases, the locking time reduces. This is because a larger injection current assists the ILO to reach the locked condition earlier. However, it is observed that when current gain is higher than 125, the phase variation is larger than 5%, which we consider the ILO is not locked. The larger phase variation is due to the fact that when the gain increases, the data component is also amplified. The data component is treated as an unwanted signal (like noise) in the clock recovery path and it interferes with

the locking process. In this case (with the DML driving currents of 40 mA for ONE and 20 mA for ZERO), current gain of 125 is the optimal value.

Figure 3.7 shows the probability density functions (PDFs) of the normalized relative phases of the injected data to the ILO and the recovered clock. The PDF of the injected data has three discrete local maximums with some probability distributions, which demonstrates that the deterministic and random jitters co-exist in the injected data [94]. On the other hand, the PDF of the recovered clock demonstrates a single local maximum, which indicates that the random jitter is dominant in the recovered clock [94].

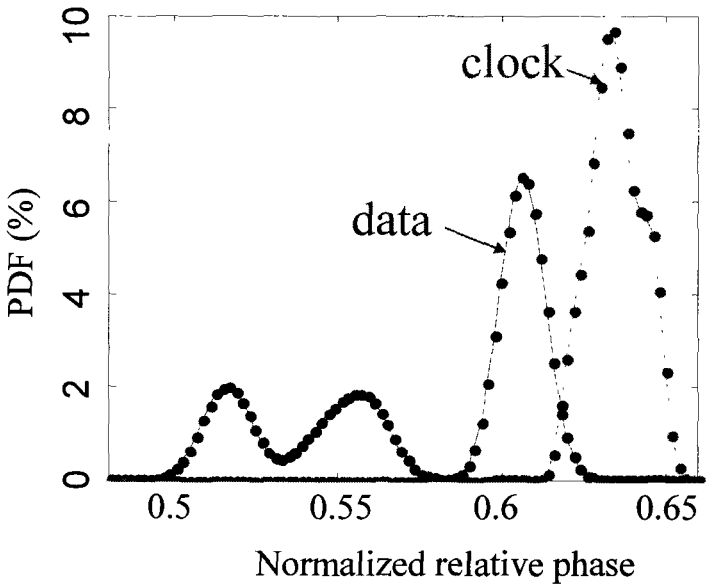


Figure 3.7 The PDFs of the normalized relative phases of the injected data at the ILO input and the recovered clock at the ILO output.

Figure 3.8 shows the jitter transfer function of our proposed clock recovery scheme, and the jitter transfer bandwidth is around 400 MHz. Such relatively wide bandwidth for the clock recovery circuit is not favored in the conventional long-haul optical communication, where multiple cascaded repeaters along the optical link are used. However, this wide bandwidth is preferred in the burst mode receiver [31]. This is because a CDR with narrow bandwidth cannot trace to the fast phase transition between packets and slow down the clock locking process.

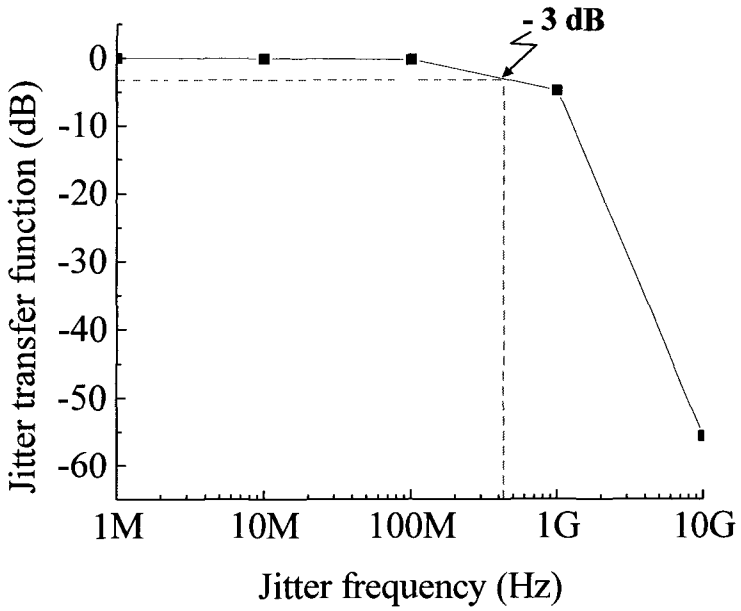
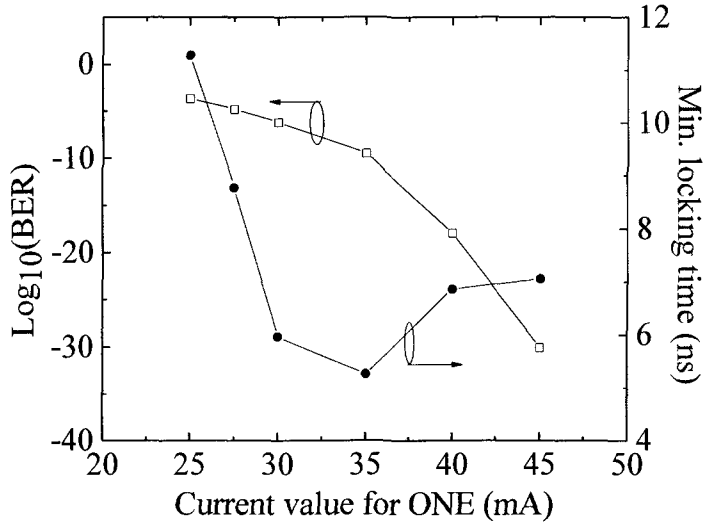


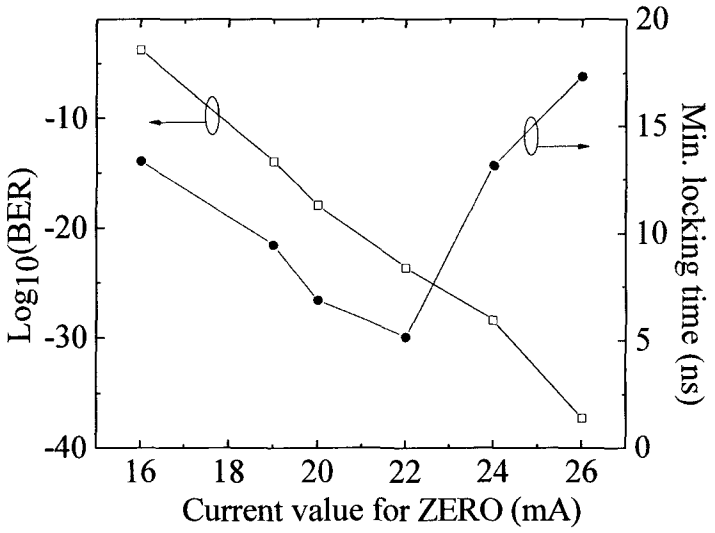
Figure 3.8 Jitter transfer function.

It is interesting to see how the proposed scheme functions under different modulation conditions by changing the current levels for ZERO and ONE of the digital data signal. Furthermore, the BER of the received data needs to be monitored to ensure the proper information transmission. Figure 3.9 demonstrates the calculated BER based on the model in [86], and the minimum locking time (under each optimal current gain according to each setting of DML driving current values) as a function of current levels for ONE and ZERO.

In Figure 3.9 (a), when changing the current level for ONE, the current for ZERO is fixed at 20 mA. On the other hand, in Figure 3.9 (b), when changing the current level for ZERO, the data amplitude between ONE and ZERO is fixed at 20 mA. It is found that when the data amplitude increases, the ratio between the overshoot amplitude and the data amplitude increases when the data amplitude is low, and decreases when data amplitude is high. Since the NRZ data is regarded as the noise or interference in the clock recovery path, a high overshoot-to-data ratio leads to a stronger normalized clock tone and faster synchronization, and vice versa. So in Figure 3.9 (a) there exists an optimal value for current value for ONE.



(a)

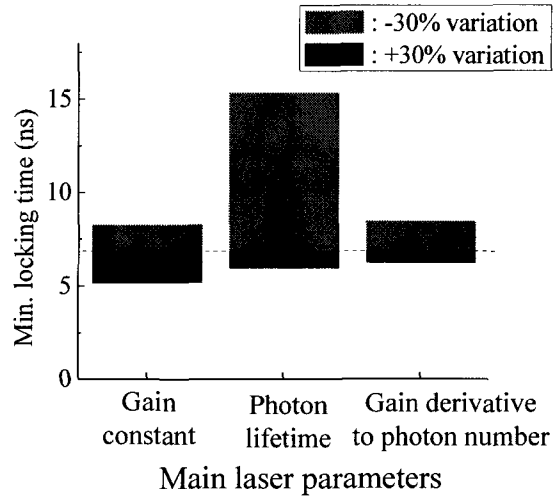


(b)

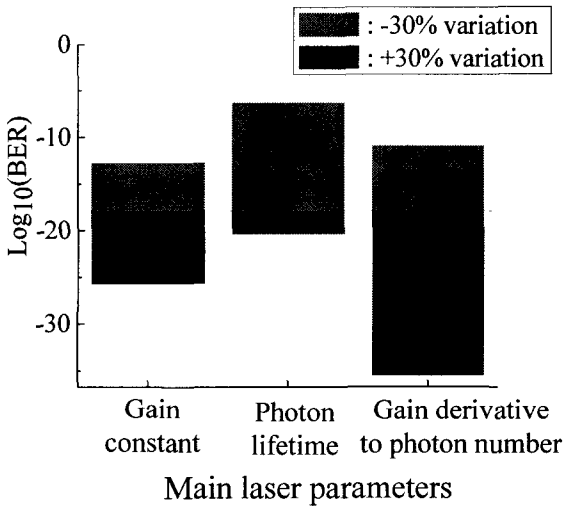
Figure 3.9 Variation of the BER and the minimum locking time as a function of the modulation current for (a) ONE with current value for ZERO fixed at 20 mA, and for (b) ZERO with the current amplitude fixed at 20 mA.

In Figure 3.9 (b), there exists an optimal current value for ZERO due to another reason different from the overshoot-to-data ratio variation. For the modulation bias more than 22 mA, a higher current makes the overshoot phenomenon less pronounced, which results in a weaker clock tone and a longer locking time. On the other hand, for the modulation current less than 22 mA, a lower current makes the pattern dependency more severe, which results in a larger jitter in the clock tone so that the locking process is jeopardized. As far as the BER is concerned, it is improved in both cases due to a better eye diagram when the current value for ZERO or pulse amplitude increases. In Figure 3.9 (a), a bigger eye is obtained because of the larger amplitude. In Figure 3.9 (b), the eye diagram is improved because the pattern dependency and the overshoot are less pronounced when the modulation bias moves away from the threshold.

Due to the process and design variations, there always exist some differences in the laser performance and four physical modeling parameters (i.e., the linewidth enhancement factor, the gain constant, the photon lifetime, and the gain derivative to photon number) are deemed important in determining the laser performance [95]. Among them, the linewidth enhancement factor does not affect our simulation because the fiber dispersion is ignored. We varied the remaining three parameters by ±30%, and showed their effects on the minimum locking time and the BER in Figure 3.10. As observed, if these parameters are tuned in the +30% range, both the minimum locking time and the BER are further improved. On the other hand, when the laser parameters variations move towards the -30%



(a)



(b)

Figure 3.10 Sensitivity analysis for (a) the minimum locking time and (b) the BER with respect to three main laser parameters.

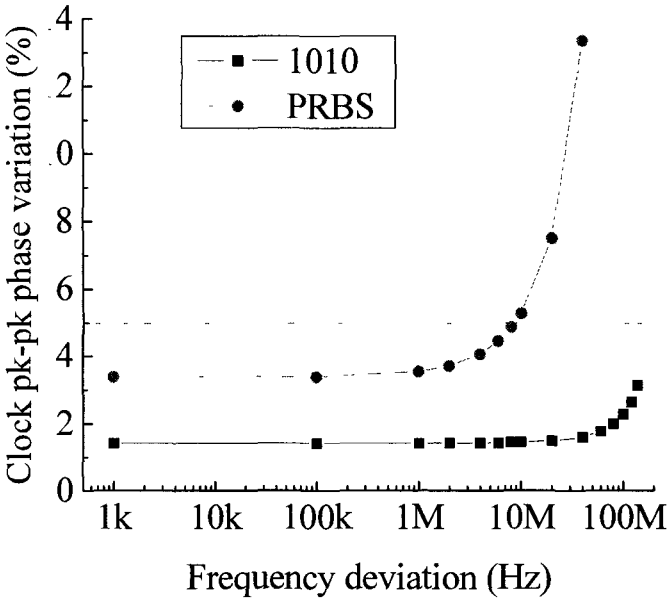


Figure 3.11 Peak-to-peak jitter of the recovered clock for the "1010" and PRBS patterns as a function of the frequency mismatch between the natural frequency of the ILO and the data bit rate.

range, the minimum locking time is longer, however, it is still confined within 15 ns.

In the discussions so far, we assumed that the natural frequency of the ILO matches the bit rate of the received data. If there exists a frequency deviation due to the fabrication mismatch, it can be corrected by tuning the capacitance of the varactor (see Figure 2.2) to change the natural frequency of the ILO to match the data rate. If we don't tune the natural frequency via the varactors, Figure 3.11 shows the peak to peak jitter of the locked clock as a function of frequency deviation between the natural frequency of the ILO and the data bit rate. Both the

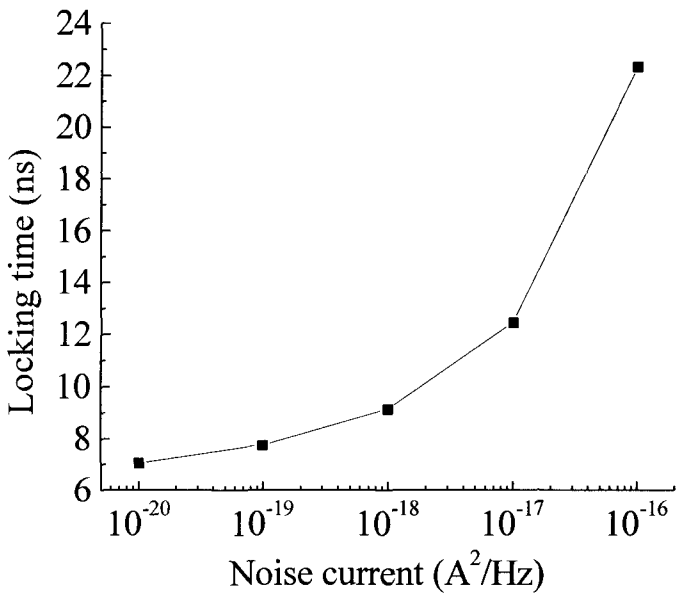


Figure 3.12 Relationship between the locking time and the noise current in the receiver.

"1010" sequence and the PRBS are used in the simulation and demonstrated in Figure 3.11. The clock jitter of the PRBS is larger than that of the "1010" sequence as expected. This is because the "1010" sequence provides more transitions between bit ONE and bit ZERO, which causes a stronger average clock tone. Following the 5% locking criteria, the frequency locking range for the PRBS is around 10 MHz, while the locking range for the "1010" sequence exceeds several hundreds of MHz.

In the previous simulation, the noise power density of the receiver in our simulation was assumed to be 10^{-20} A^2/Hz as indicated in [76]. Improper receiver design, however, may result in higher noise and degrade the clock recovery

process. Figure 3.12 shows the locking time as a function of noise power density for our proposed clock recovery scheme. Twenty simulations with randomly generated noise are conducted to find the longest locking time among them in order to demonstrate the worst case scenario. We observed that, in general, the higher receiver noise (or lower signal-to-noise ratio, SNR) results in longer locking time. This is because the receiver noise momentarily generates false tones close to the frequency of the clock tone. If these noise tones become stronger, the ILO has higher chance to mistakenly lock to such noise tones during the locking phase and results in longer locking time. Our proposed clock recovery scheme demonstrates a good SNR tolerance, and it keeps the locking time within 25 ns when the noise power increases from 10^{-20} to 10^{-16} A^2/Hz.

In a communication protocol, the maximum length of consecutive identical bits (ZEROs or ONEs) is defined to ensure the existence of reliable timing information (e.g., clock tone). In our proposed scheme, we take consecutive ZEROs to study this maximum length. In an ideal case, if the receiver noise is negligible, and the natural frequency of the ILO and the data bit rate matches to each other, the relative phase between the ILO and that of the ideal data can be maintained, even when the data bits have infinite number of consecutive ZEROs. This means that the tolerable ZERO length is infinity under the ideal case. However, because of the noise in the receiver and the finite difference between the ILO frequency and the data bit rate, the maximum length

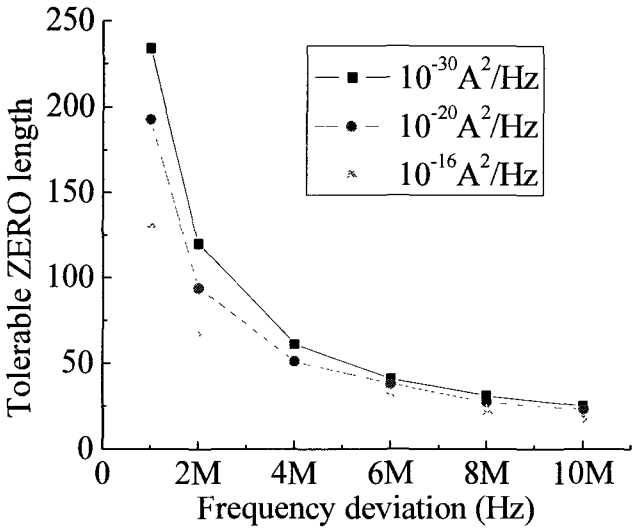


Figure 3.13 Tolerable ZERO length for different frequency deviation at different receiver noise power densities (A^2/Hz).

for the consecutive identical bits is finite. Figure 3.13 shows the relationship between the tolerable ZERO length and the frequency deviation at different receiver noise power densities (in A^2/Hz). Twenty simulations with random noise injections are conducted to find the maximum lengths of consecutive ZEROs at which the ILO is out of lock. The shortest length from these twenty simulations is chosen to demonstrate the worst case scenario. Larger frequency deviation leads to shorter tolerable ZERO length, as seen in Figure 3.13. On the other hand, the receiver noise also plays an important role. When the noise power density increases (e.g., from 10^{-30} to 10^{-16} A^2/Hz), the resulting tolerable ZERO length reduces. This is because the receiver noise causes the ILO phase to exceed the locking criteria easier. It should be noted that the values in Figure 3.13 are

obtained according to the 5% locking criteria. Relaxed criteria will lead to longer tolerable ZERO length.

Chapter 4
EXPERIMENTAL VERIFICATION

Though the BM-CDR schemes we proposed use the optical characteristics of either the fiber dispersion or the DML relaxation oscillation, those two optical characteristics already exist in the future or current burst mode optical communication link, respectively, and generally we do not need to engineer them. So the design task is focused on the circuit implementation of the BM-CDR in the receiver end. In this work, we are focused on the design for burst mode clock recovery (CR) circuitry, without the data decision circuit. This strategy helps ensure the tape-out quality and easy debugging.

4.1 Design of BM-CR Circuitry

The designed BM-CR in this work uses the ILO as the core circuit, as shown in shown in Figure 4.1. The ILO is based on the VCO. The designed circuit combines the circuit design techniques of both transistor body biasing frequency tuning scheme [96] and the voltage injection scheme by the single switching transistor [71]. The former technique tunes the oscillation frequency by changing the body bias of the transistors and corresponding parasitic capacitances. It can eliminate the varactor utilized in the conventional VCO design and can boost the oscillation frequency dramatically compared to the

conventional design. The latter circuit design technique employs the NMOS transistor M_{inj} in Figure 4.1 to equivalently create current injection by applying the voltage injection applied on M_{inj}. Such technique was originally used in the frequency division application, and this work is the first time to utilize it for the clock recovery purpose.

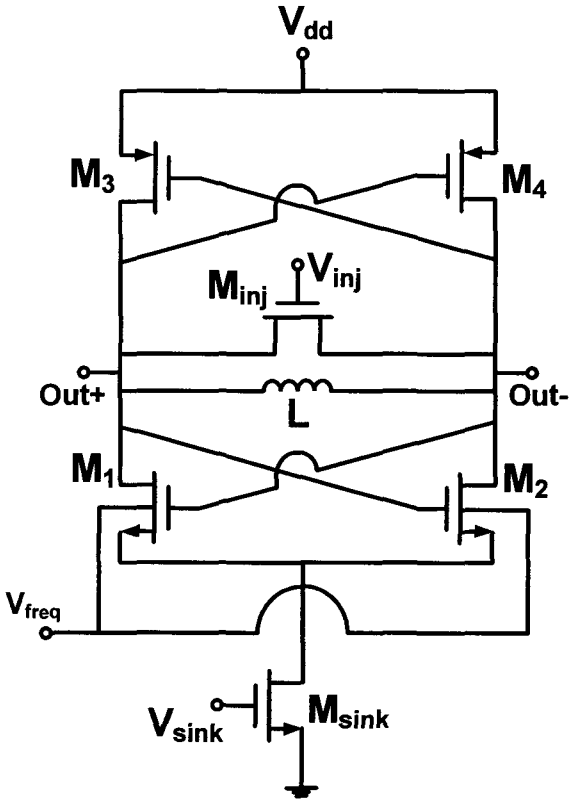


Figure 4.1 The BM-CR circuit design using both techniques of the switching transistor for the injection and body biasing for frequency tuning.

Besides the core circuit of the ILO, the total circuit chip of BM-CR needs to include the buffer circuit block to provide impedance matching. The input impedance of the measurement equipment is usually 50 Ω. However, the ILO is able to output larger oscillation amplitude if the load of the ILO has larger impedance. In order to provide large loading impedance for the ILO, a properly designed buffer is necessary to be inserted between the ILO and the measuring equipment. The buffer circuit in our circuit is an inverter with proper sizing of the NMOS and PMOS transistor, to provide symmetric rising and falling time of the oscillation swing at the buffer output.

Another reason we choose to use voltage injection instead of direct current injection because the commercial photo-detector or photo-receiver usually has voltage output instead of current one. If we are to fully implement our schemes by using direct current injection, we have to attach the photo-detector chip with the BM-CR circuit chip in a multi-chip module (MCM) [97] to access the photo-current. Furthermore, in the measurement, we have to align and apply optical signal onto the photo-detector. The overall packaging and measurement procedure would be much more complicated. This work is focused on proposing and verifying the BM-CR schemes without divergence on packaging and multi-chip mounting, so we choose to simplify our chip packaging and measurement by designing an ILO with voltage injection. Among the various voltage injection schemes, we choose to use the one utilizing single switching transistor, for its

robust design in eliminating the mismatch existed in the balanced voltage injection schemes.

There are two main challenges worth consideration regarding employment of the switching transistor M_{inj} (see Figure 4.1). One is related to the value of the current injection. The value of the current passing through M_{inj} depends on two voltages, V_{inj} and V_{DS} of M_{inj}, where drain (D) and source (S) of M_{inj} are interchangeable depending on which ports have higher potential. For any given V_{DS}, larger V_{inj} attracts more electrons in the channel under the gate oxide, and thus more current can be equivalently injected. The current also depends on the V_{DS}. Here V_{DS} always changes since it is the difference between Out+ and Out-, which always oscillate. Smaller V_{DS} leads to smaller current injection. At the moments $V_{DS} = 0$, even V_{inj} is large, there is no current injection. In this manner, this scheme may not be as efficient as balanced current or voltage injection, in which the injection is independent from the tank voltage drop.

The other challenge resides on that putting M_{inj} in parallel with RLC tank introduces its own parasitic capacitance into the tank, which leads to two problems. One is that the increased capacitance reduces the oscillation frequency. Care needs to be taken in deciding the width (W) of M_{inj} (supposing its length is 0.18 μm). Large W introduces large capacitance and decrease oscillation frequency. On the other hand, to obtain enough injection current, too small W is not preferred. The other problem is that the added parasitic capacitance by M_{inj} always changes for V_{inj} and V_{DS} of M_{inj} are not fixed, leading to variation of the

internal frequency depending on V_{inj} and V_{DS}. The problem of internal frequency variation affects little in the case of sinusoidal waveform injection by V_{inj} when performing the frequency division [71]. Since the internal frequency variation is also sinusoidal, the resulting oscillation waveform is still approximately sinusoidal. In our case of random data signal injection by V_{inj}, the frequency variation has some randomness, and the oscillation output waveform may be different from cycle to cycle. To reduce such effect, W of the M_{inj} shall not be too large.

It is also a challenge to add body biasing frequency tuning scheme (V_{freq}) in the ILO circuit and such combination with the usage of single switching transistor has never been published. External injection changes the equivalent tank current and voltage drop (between nodes Out+ and Out-) over the tank instantaneously, and adds the randomness to the equivalent parasitic capacitances of the transistors (M_1 and M_2), since such parasitic capacitances are dependant on the gate and drain voltages (i.e., nodes Out+ and Out-). This would further add additional randomness to the internal frequency beyond the one added by the M_{inj} itself. Through simulations and experiments, we find that such randomness problems of the internal frequency does not affect the ILO locking process much, under proper circuit design. This is because the injection locking phenomenon can change the oscillation frequency from the internal one to the external injection frequency, in the case the difference between the internal frequency and the external injection frequency is within the frequency locking range [61]. The

variation of the internal frequency directly and indirectly caused by switching transistor M_{inj} is limited within a range supposing the width of M_{inj} is not too large. The actual design of width of M_{inj} has to be done through extensive parameter sweeping and simulation.

The decision of the signal amplitude on V_{freq} also needs careful consideration. The internal frequency can be increased by letting V_{freq} be more negative, due to the larger SCR depth of the PN junctions of the drain and body in the NMOS transistors and the resulting smaller parasitic capacitance value. However, the output swing of the ILO would decrease at the same time. This is because when the body bias is more negative, the voltage-drop between the source and the body of the gain-providing transistors (M_1 and M_2) increases, which in turn increases the threshold voltage due to the body effect. Increased threshold decreases the transconductance gain the transistors can provide, leading to decreasing of the oscillation amplitude.

We can also insert a DC blocking capacitor before the ILO to reduce the strength of the interfering NRZ data, especially its low frequency component. However, to block only the low frequency portion but not the high frequency one which contains the clock tone, we need to design the capacitor with large capacitance. That would translate into a large size for the capacitor, consuming chip space. In order to keep small chip size, we do not use DC blocking capacitors in this work, and we will find that the BM-CR circuit can still perform well without such capacitor.

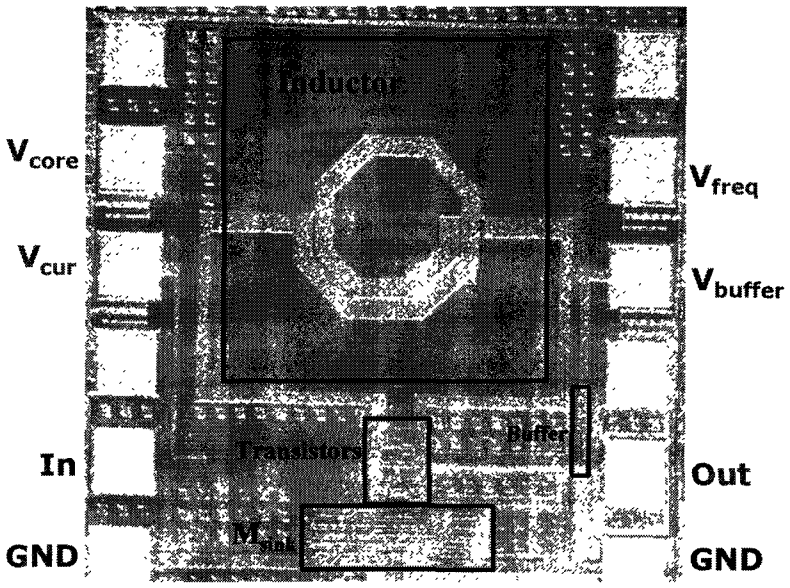


Figure 4.2 Photograph of the fabricated BM-CR circuit.

Figure 4.2 shows the layout of the BM-CR chip in microphotograph. The total size (including the PADs) of the chip is 910 μm x 880 μm.

4.2 Experimental Setup

The experimental setup is shown in Figure 4.3. The signal generator (SG) provides the frequency reference for the PPG, which generates the electrical data either in continuous or burst mode, in either NRZ format or "1010" pattern. The generated electrical data is then fed into the transmitter (Tx) which outputs corresponding optical data signal. The Tx can be either an EML or a DML. The EML transmitter has its operation bit rate around 10 Gbps. The DML is provided

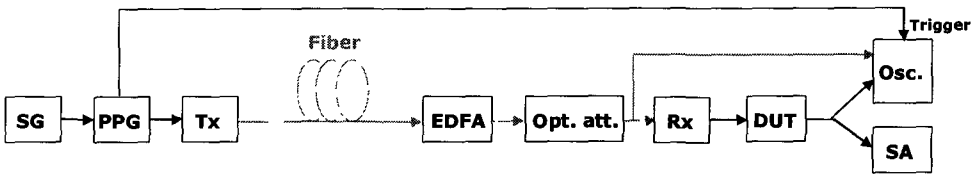


Figure 4.3 Measurement setup for burst mode clock recovery scheme using fiber dispersion or DML spectrum (SG – signal generator, PPG – pulse pattern generator, Tx – optical transmitter, EDFA – Erbium doped fiber amplifier, opt. att. – optical attenuator, Rx – optical receiver, DUT – device under test, referring to the BM-CR circuit chip, Osc. – oscilloscope, SA – spectrum analyzer).

by the Department of Engineering Physics, and it was originally designed for operation of bit rate up to 2 Gbps. Both of them have output wavelength at around 1550 nm.

After the Tx, the transmission fiber type is G. 652 SMF with a length of around 20 km. The EDFA and the following optical attenuator (opt. att.) are employed to fine tune the optical power of the signal arriving at the optical receiver (Rx). The EDFA and the optical attenuator is to provide a fixed gain throughout the experiment. The receiver (Rx) converts the received optical data signal into the electrical voltage signal, which is then fed into the BM-CR (i.e., the device under test, DUT), and the BM-CR is expected to output the clock locked to the input data signal. The output of the DUT is fed into the oscilloscope (Osc.) and the spectrum analyzer (SA) through a power divider. The optical signal

after the optical attenuator is also fed into the oscilloscope through an optical power splitter, to display the waveform or the eye diagram of the received data. The bandwidths of both the photo-detector inside the oscilloscope and the Rx are greater than 10 GHz. The oscilloscope receives the trigger signal from the PPG synchronization output, which can be either the pattern synchronization signal or the 1/64 clock. When the pattern synchronization signal is chosen, the full waveform can be displayed. If the 1/64 clock is chosen, an eye diagram can be displayed. By feeding the waveforms (or eye diagrams) of the received data and the recovered clock to the oscilloscope at the same time, we can display both of the waveforms (or eye diagrams) on the oscilloscope screen and clearly demonstrate the locking phenomenon.

In the initial measurement of the BM-CR, it was noticed that the internal frequency of the ILO could be tuned (through V_{freq}) up to around 9 GHz, 1 GHz less than the designed target. There are several possible reasons causing this. It may be due to the parasitic capacitance existing in the layout, which can not be fully extracted and considered during the design stage, since the design tools used are for university education purpose and the model files for the parasitic post-layout extraction tool are not complete. Another possible reason is due to the parasitic capacitances existing in the cables connected to the chip, and the contacts between the chip PADs and probe tips. The cables used in the measurement are somehow low quality to save the experimental costs (high quality cables with nearly ideal 50 Ω impedance and zero parasitic capacitances

would cost several thousand dollars per cable). The contacts between the chip PADs and probe tips also add parasitic capacitances, which depend on the actual contacting positions and the pressure applied on the probe tips. The third reason for frequency reduction may be due to the fabrication mismatch. The parasitics of the chip are different from one fabrication run (on one wafer) to another and from one chip to another in the same run (wafer). There is no way to fully control the fabrication mismatch especially in the low cost fabrication technology. The only way is to design the circuit to compensate the mismatch. For the ILO, we can increase the frequency tuning range to compensate the frequency dropping in future tape-outs.

Measures have been taken to tune the frequency controlling voltage to be more negative, to move the internal frequency toward 10 GHz. However, the closer the internal frequency approaches 10 GHz, the lower the output oscillation amplitude of the ILO, due to the increased threshold voltage caused by more negative body biasing. We chose to tune the frequency controlling voltage to balance the trade-off between the demands for high frequency and large oscillation amplitude, and the resulting internal frequency is at around 8.9 GHz.

In the following measurement, the testing data bit rate is tuned to be around 8.9 Gbps, depending on the actual internal frequency of the ILO under test, controlled by the external frequency controlling voltage and the actual contact parasitics. We first tune V_{freq} to change the internal frequency of the ILO to our desired value, usually close to 8.9 GHz, and we measure this frequency

through a SA reading. We then tune the PPG bit rate to be similar to the internal frequency of ILO. It should be noted that due to the precision limitation of both the frequency measured by the SA and the frequency reference generated by the SG, the bit rate of data and the internal frequency of ILO may not match exactly. However, injection locking phenomenon can force the ILO to have the same frequency as the data bit rate if the internal frequency of ILO is within the frequency locking rage (around +/- 2 MHz in our measurement) from the data bit rate [98].

4.3 Components Performance

We measured the spectrum of the PPG output, as shown in Figure 4.4, when its output is $2^{31} - 1$ PRBS at 8.9 Gbps. Theoretically, the spectrum in this case should not contain power at the bit rate. However, in the measurement, the PPG output exhibits a clock tone at the bit rate. We set the resolution bandwidth (RBW) and video bandwidth (VBS) both as 3 MHz for the oscilloscope, when displaying the spectrum of the data signal in the full frequency span.

This phenomenon of clock tone generation from PPG is due to the clock feed-through existing within the PPG equipment, or impedance mismatch between the PPG output port and connection cables. Better PPG and/or cables should be able to reduce the clock tone strength. For example, in [79], the clock tone strength in a back-to-back configuration is nearly unnoticeable.

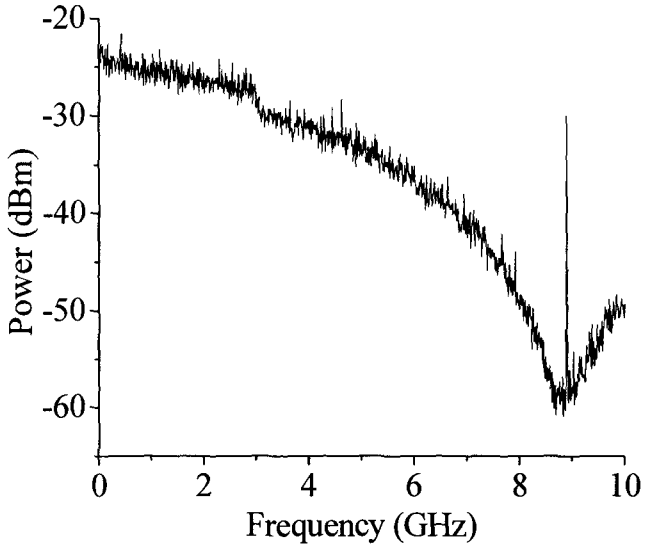


Figure 4.4 Measured spectrum of the PPG output at 8.9 Gbps with $2^{31} - 1$ PRBS pattern.

The clock tone generated by the PPG nonideality has been used for the CM-CR [81, 99]. However, the clock tone generated through transmitter nonideality is so weak, and may only be suitable for CM-CR due to its loose requirement of locking time. To enable a fast locking in BM-CR, the embedded clock tone must be strong enough. It is noted that the clock tone as shown in Figure 4.4 is less than the DC level of the spectrum. We will see in Figure 4.6 that the clock tone is strengthened and higher than the DC value of the spectrum after experiencing fiber dispersion.

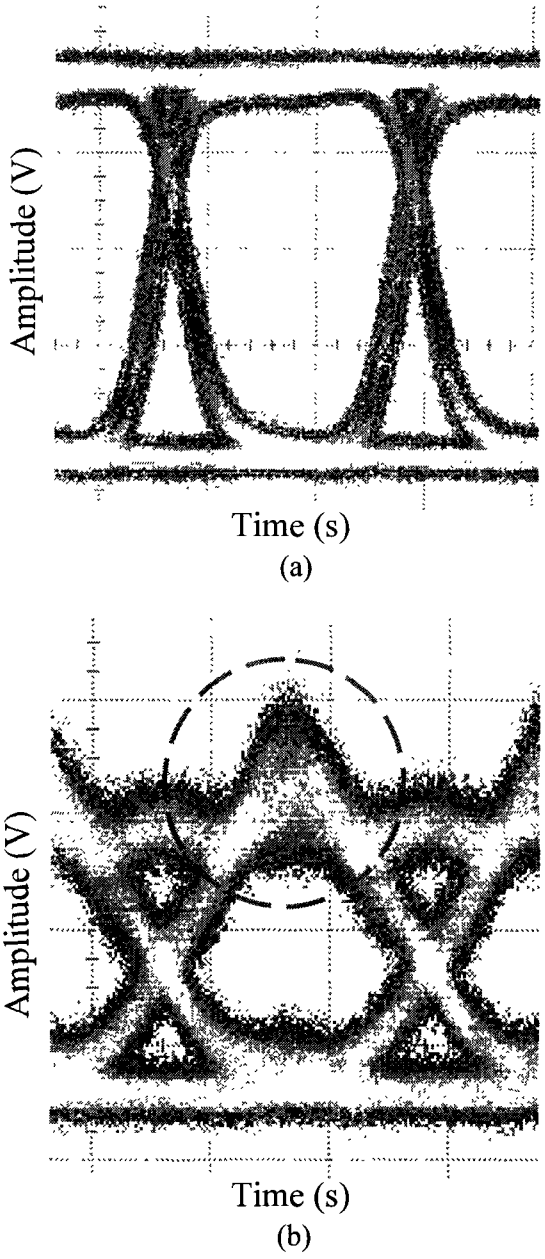


Figure 4.5 Measured eye diagrams of data in the configuration of (a) back-to-back (i.e., EML Tx directly to Rx) and (b) after fiber link (i.e., EML Tx – fiber – Rx).

To demonstrate the effect of fiber dispersion, the eye diagrams of back-to-back (i.e., EML Tx directly connects to Rx) and after fiber link (i.e., EML Tx – fiber – Rx) are shown in Figure 4.5. The bit rate used is 8.9 Gbps. The EML output is distortionless, as shown in Figure 4.5 (a), while after the fiber dispersion, the signal is distorted, as shown in Figure 4.5 (b). The distortion behaves as ripples at ZERO and ONE levels, which is similar to the simulation results of Figure 2.7 (a).

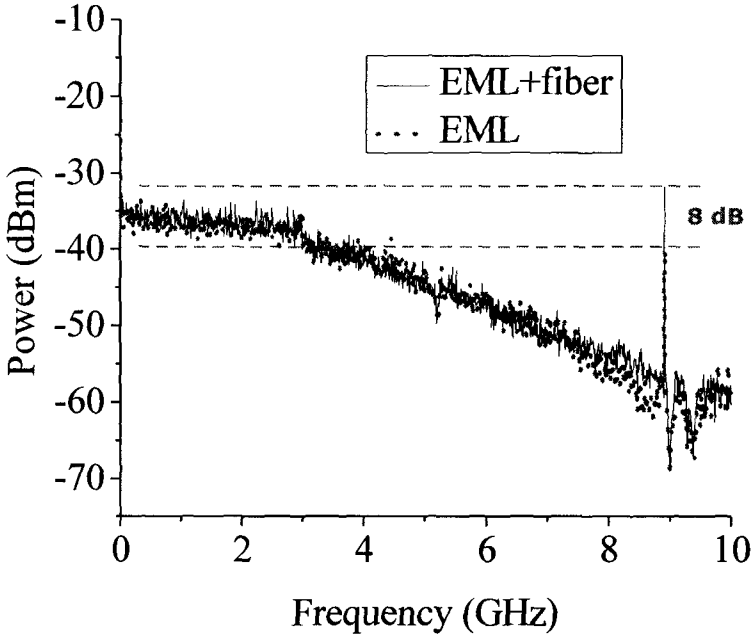
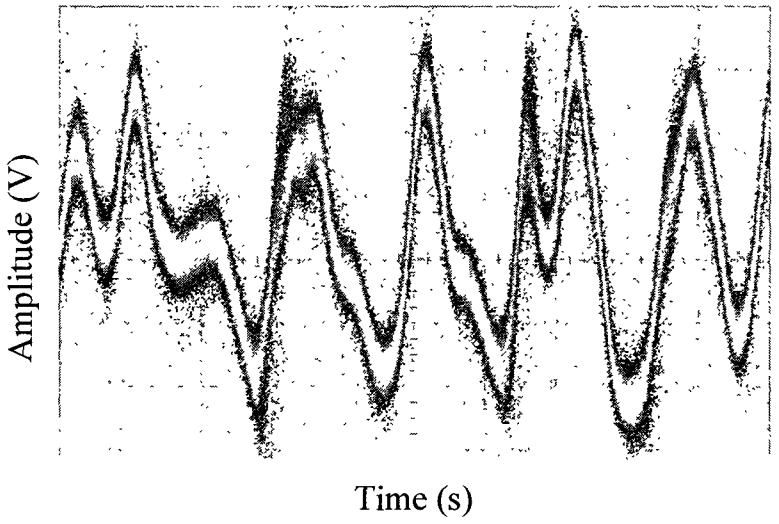


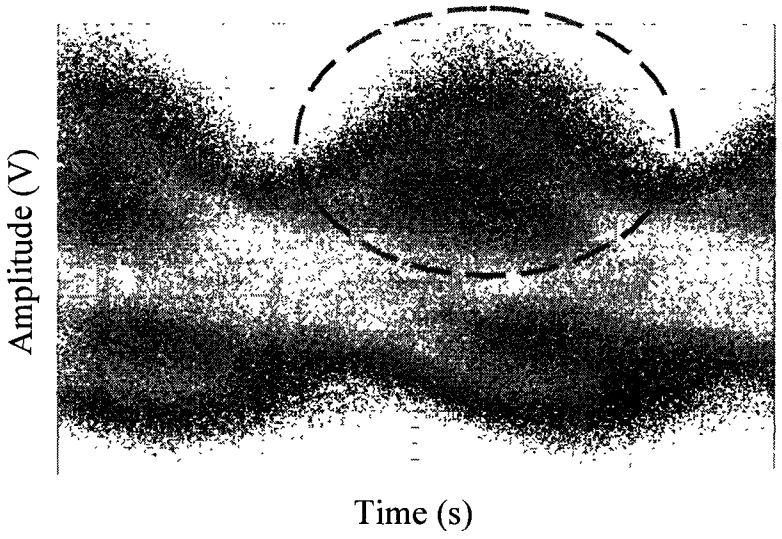
Figure 4.6 Comparison between the measured spectrums of back-to-back (i.e., EML Tx directly to Rx) and after fiber link (i.e., EML Tx – fiber – Rx). The solid line is spectrum after fiber transmission, and the dotted line is the spectrum in back-to-back.

In the power spectrum, the dispersion caused distortion demonstrates a strengthened clock tone at the bit rate, as shown in Figure 4.6. The dotted line represents the spectrum of the back-to-back transmission without passing through the fiber, and the solid line represents the spectrum after fiber transmission. The optical attenuator is tuned in both cases to compensate the link loss difference introduced by the fiber transmission, and to align the frequency components of the data (e.g., DC components, and the frequency components around but not at the clock tone) in the spectra. It could be seen that fiber dispersion strengthens the clock tone at the bit rate by 8 dB (more than 6 times amplification).

The DML used in the experiment has the output wavelength of around 1550 nm. As our intention is to emulate a DML working at 1310 nm range, the optical fiber is replaced by an optical attenuator to emulate the fiber attenuation, while not introducing dispersion by the fiber. The DML is designed to operate below 2 Gbps. However, in the experiment, the 8.9 Gbps electrical data signal is used to directly modulate the DML, and the output is highly distorted. In Figure 4.7 (a), it is barely recognized that the waveform represents "1110101011010", and in Figure 4.7 (b), the corresponding eye diagram is closed. On the other hand, the distorted waveform still contains the clock tone, as circled, shown in Figure 4.7 (b).



(a)



(b)

Figure 4.7 Measured (a) waveform and (b) eye diagram of DML output with $(2^7 - 1)$ PRBS data pattern.

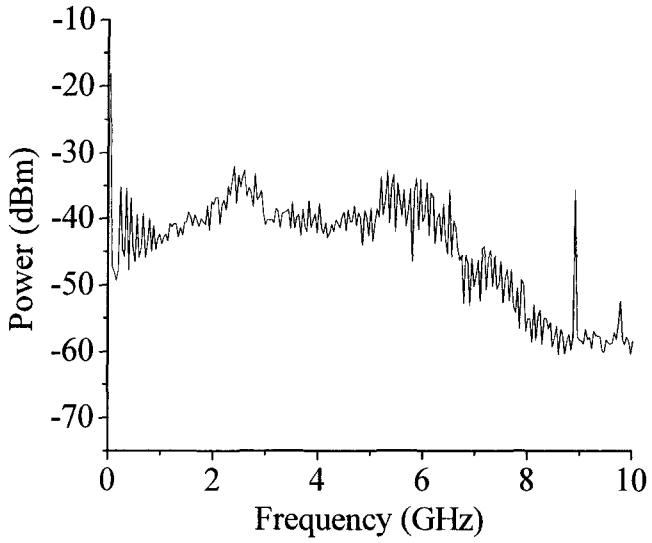


Figure 4.8 Measured spectrum of received data from the DML.

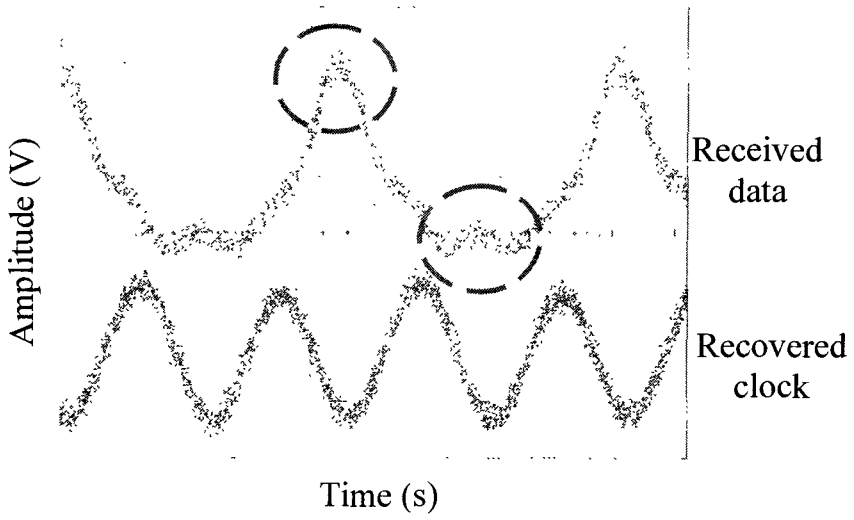
The corresponding spectrum of received data signal generated from DML and after optical attenuation is shown in Figure 4.8. As can be seen, at 8.9 GHz, clock tone is clearly exhibited.

Regarding the BM-CR circuit, there are two power supplies to the circuit. One is for the core circuit, the ILO, and the other is for the output buffer. Both of them have the values of 1.8 V. The BM-CR is usually integrated with other circuit blocks in the practical designs, and the buffer circuit block is not necessary. In this manner, we only need to monitor the current and calculate the power supply of the core circuit. The currents flowing out from the power supply for the core circuit is 3.64 mA and the consumed power is calculated as 6.552 mW. The

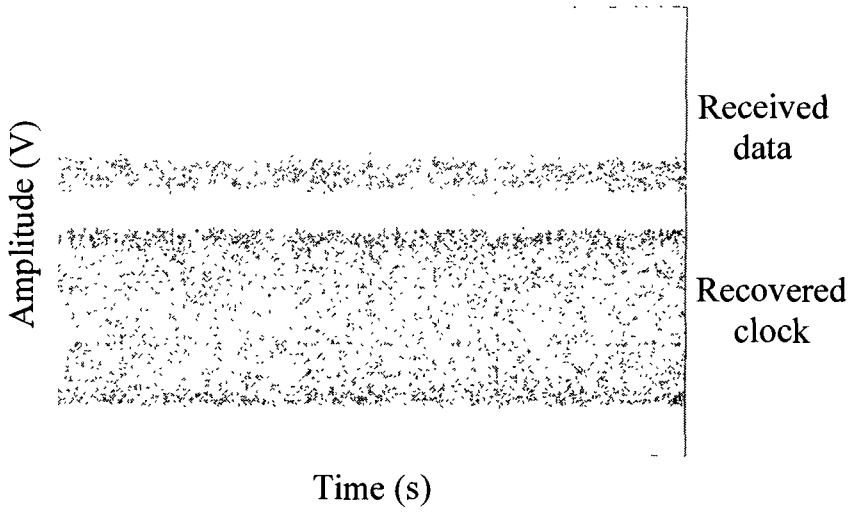
measurement shows that there is not much difference between the power consumptions whenever there is data injection or not. This is because in both cases the ILO keeps oscillating and outputs sinusoidal waveform.

4.4 Data Locking

Data pattern as alternative ONEs and ZEROs (i.e., "1010") is firstly used to test the locking behaviour of the chip. The trigger signal provided from the PPG to the oscilloscope is the pattern synchronization signal. The measured results in both cases when the Tx is on and off are shown in Figure 4.9. In Figure 4.9 (a), the upper eye diagram is the received data and the lower eye diagram is the output clock from the BM-CR circuit. A clear eye for the clock is shown. Since the trigger to the oscilloscope is synchronized with the PPG, a clear eye for the clock means that the clock has the same frequency as the data bit rate, and keeps a fixed phase relative to the data. It is noted that the recovered clock shifts its amplitude and offset (i.e., average value) between two values. This is because the interferences from the data are different for different data levels (i.e., bit ONE or ZERO). The clock tone injection from bit ONE is larger than that from bit ZERO (see circle marking in Figure 4.9 (a)). It shall be noted that the phases of the data and the clock are not aligned on the oscilloscope, because they propagate through different lengths, due to the measurement setup.



(a)



(b)

Figure 4.9 Measured eye diagram of the received data and the recovered clock when the received data is continuous, when (a) Tx is turned on, and (b) Tx is turned off.

In Figure 4.9 (b), the Tx is turned off, and the upper eye for the received data only shows noise around ZERO level. The lower eye diagram for the recovered clock does not show an eye, indicating that the output clock from the BM-CR does not have exactly the same frequency as the data bit rate. However, it still demonstrates the peak-to-peak amplitude, indicating that the oscillator of the BM-CR is still oscillating. Such state is called free-running.

The spectrum of the BM-CR output can also indicate the locking phenomenon. Figure 4.10 shows the spectra of the BM-CR output when the Tx is off and on, with the same conditions as in Figure 4.9. The x-axis is the offset frequency from the frequency of the bit rate. When displaying the spectrum of the recovered clock, the RBW and VBS are both set as 10 kHz. When the Tx is off, the clock spectrum distribution is wider and asymmetric, compared to the case when the Tx is on. Furthermore, the clock spectrum is not stable during the measurement. Although the internal central frequency is close to 0 Hz offset frequency, it always shifts around the central point, due to the noise. When the Tx is on, the main band of the output spectrum is stable, and the central offset frequency is exactly 0 Hz. The bandwidth reduction of the output during external data injection is benefited from the injection locking phenomenon [100].

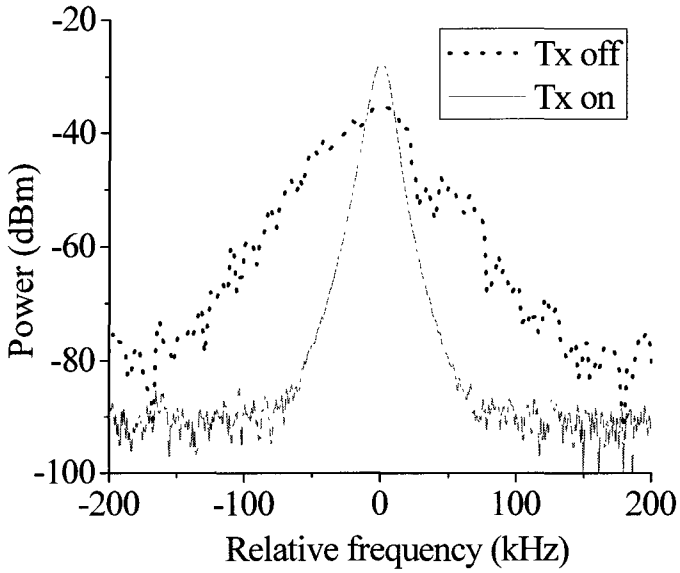
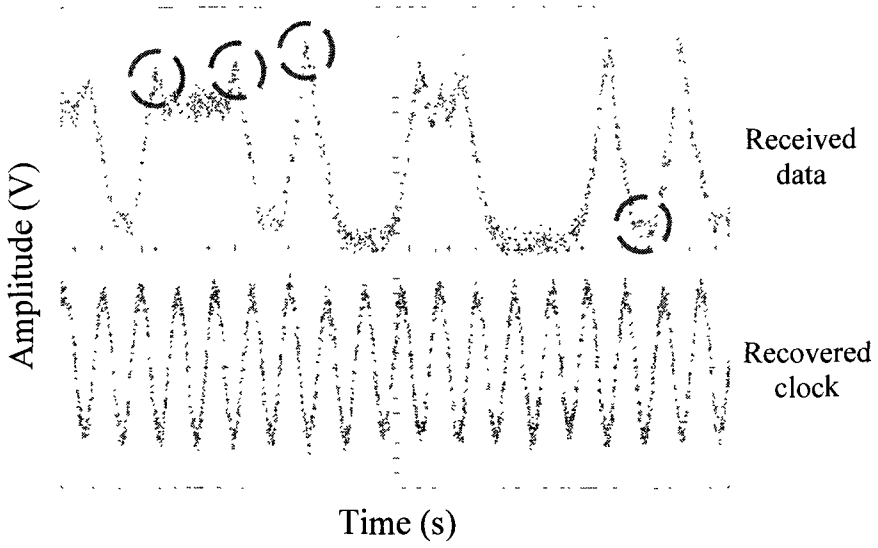
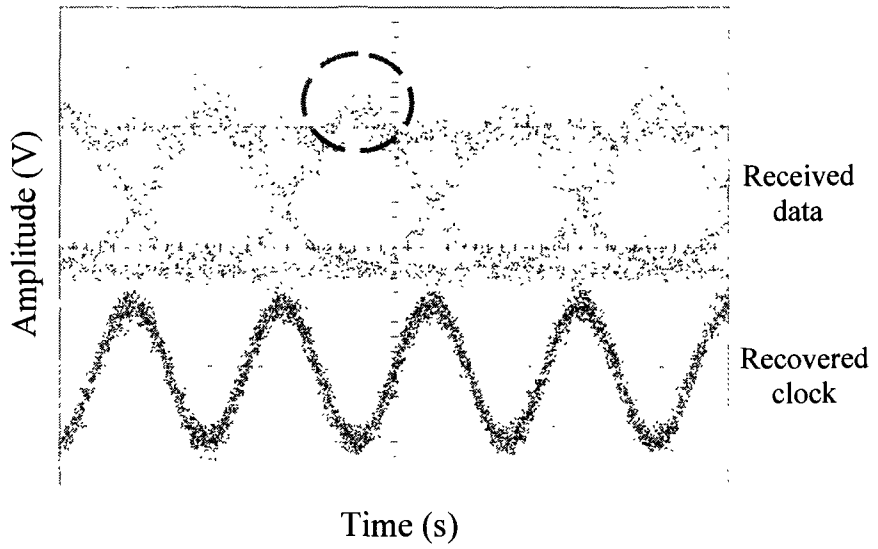


Figure 4.10 Measured spectrum of BM-CR output when Tx is turned off and on.

We can also test the BM-CR performance when it is locked to a $2^7 - 1$ PRBS data signal. Figure 4.11 shows the captured waveforms and eye diagrams of the received data and the recovered clock. The received data is distorted by the dispersion as expected, and the overshoot-like distortion enhances the clock tone. The recovered clock has a clear eye, showing it is locked to the received data. In Figure 4.11 (a), we can observe that the instantaneous clock amplitude and average value (i.e., offset) are shifted randomly, although such shifting is very slightly and even unnoticeable. This is due to the interference from the random data pattern.

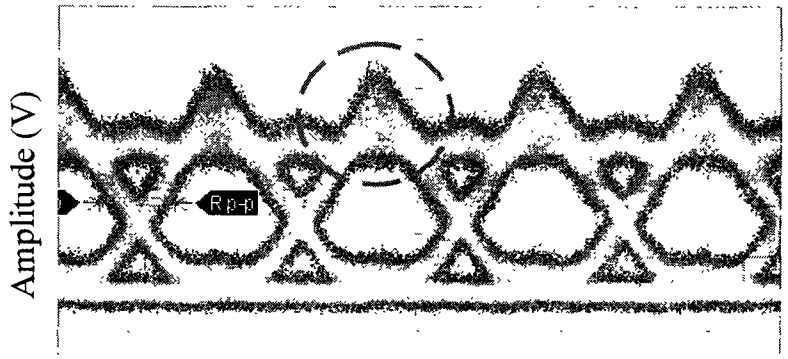


(a)

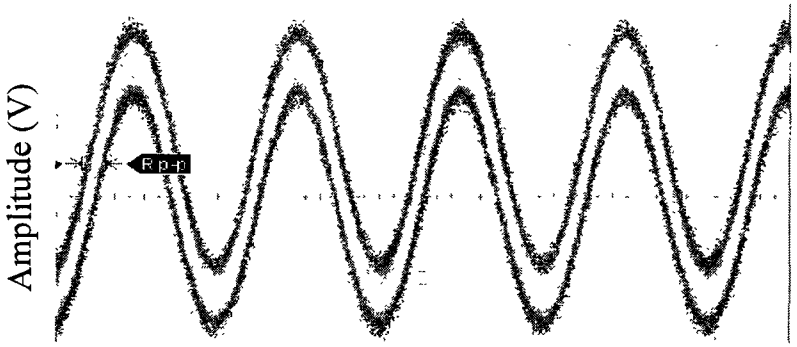


(b)

Figure 4.11 Measured (a) waveforms and (b) eye diagrams of received data and recovered clock.



(a)



(b)

Figure 4.12 Measured eye diagrams of (a) received data and (b) recovered clock.

In Figure 4.11 (b), the eye diagrams of the received data and the recovered clock are displayed by setting the PPG synchronization output as the 1/64 clock. It is observed that the variation of the clock amplitude and offset discussed above is not severe, although it adds to the jitter of the recovered clock. To further analyze the jitter performance, the eye diagrams and the jitters are shown in Figure 4.12,

using the eye diagram mode on the oscilloscope (the usual mode used, as in Figure 4.11, is the oscilloscope mode). Now the data pattern is set as 2^{31}-1 PRBS. The maximum root-mean-squared (RMS) jitter of the received data is 10.9 ps, and the recovered clock has an RMS jitter of 2.9 ps. It demonstrates the jitter reduction effect by the clock recovery circuit. Such phenomenon has been demonstrated in the simulations.

During the locked state, the recovered clock maintains a good performance in the jitter, even though the noise within the ILO exists and affects the oscillation. The clock recovery benefits from the bit transitions from time to time in the PRBS data sequence. If there is a long time during which the bits are identical and do not contain a bit transition, the ILO does not have the proper clock tone injection as the reference, and it would grow into free-running status. During the free-running, the ILO can accumulate a large value of phase variation (jitter) generated from its internal noise. In the practical optical communication systems, the protocols usually define the coding schemes, such as 8B/10B [24, 101]. Such coding schemes are used to convert the arbitrary random data into the encoded data before transmission. They are designed to ensure that the length of the consecutive identical bits (e.g., long ONEs) is limited in the converted data.

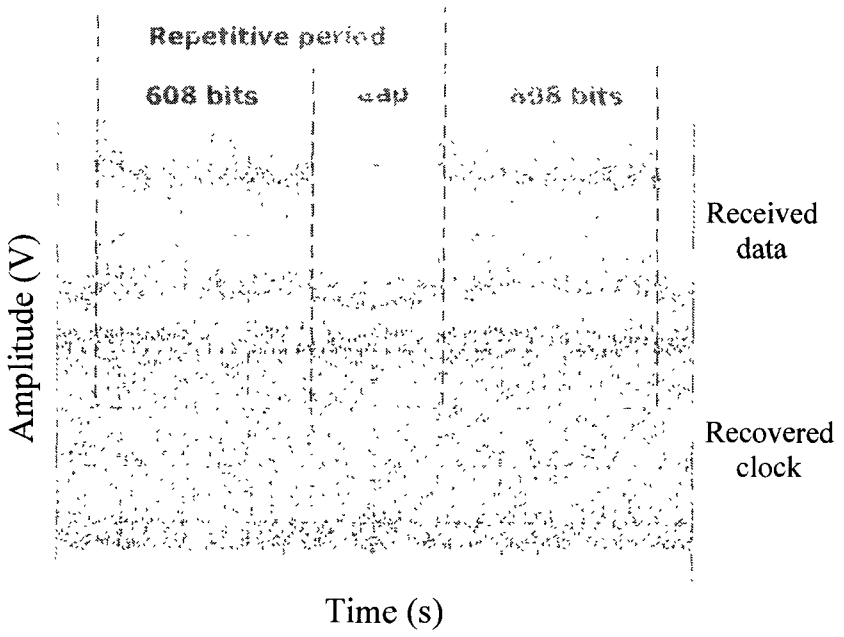


Figure 4.13 Measured waveform of received data packets and recovered clock (upper waveform is received data packets, and lower waveform is recovered clock).

We can program the PPG to generate the burst mode packets, as shown in Figure 4.13 (see the upper waveform). The data pattern length (i.e., the repetitive period) is the sum of 608 bits and the length of the gap period. The 608 bits can be either PRBS or alternative ONEs and ZEROs ("1010"), depending on the different testing we perform. In the gap period, the PPG output is all ZEROs. The PPG output repeats such combined data pattern (i.e., the 608 bits and the gap bits). In this way, we can generate burst mode data packets. In the following paragraphs, we will demonstrate the case of burst mode "1010" data. The PRBS data case has the similar phenomenon.

The recovered clock waveform is shown in the bottom waveform in Figure 4.13. Though it is hard to judge the jitter performance from the waveform, it can demonstrate the stability of the clock amplitude, and shows that the ILO is always oscillating, whether there is data input or not.

We can increase the gap period between the packets from zero gap bit (i.e., continuous mode case) to a larger value, to observe the effect on the locking performance of the BM-CR in the burst mode. Since the pattern length is very long, it is more convenient for one to obtain the eye diagram which is the overlay of all the clock waveforms, including when the data pattern contains the bit transitions or all ZEROs. By comparing among the jitters or observing the background noise of the recovered clock for different repetitive periods, we can observe how the jitter accumulates during the gap period.

We tried to record the clock waveform by using the pattern synchronization signal from the PPG as the oscilloscope trigger. However, when the pattern length is very long (e.g., 4208 bits), the trigger signal frequency is very low, and the oscilloscope cannot perform the measurement correctly and reports the error of slow triggering signal. In order to compare the measurement results conveniently, we chose to only measure the clock eye diagrams.

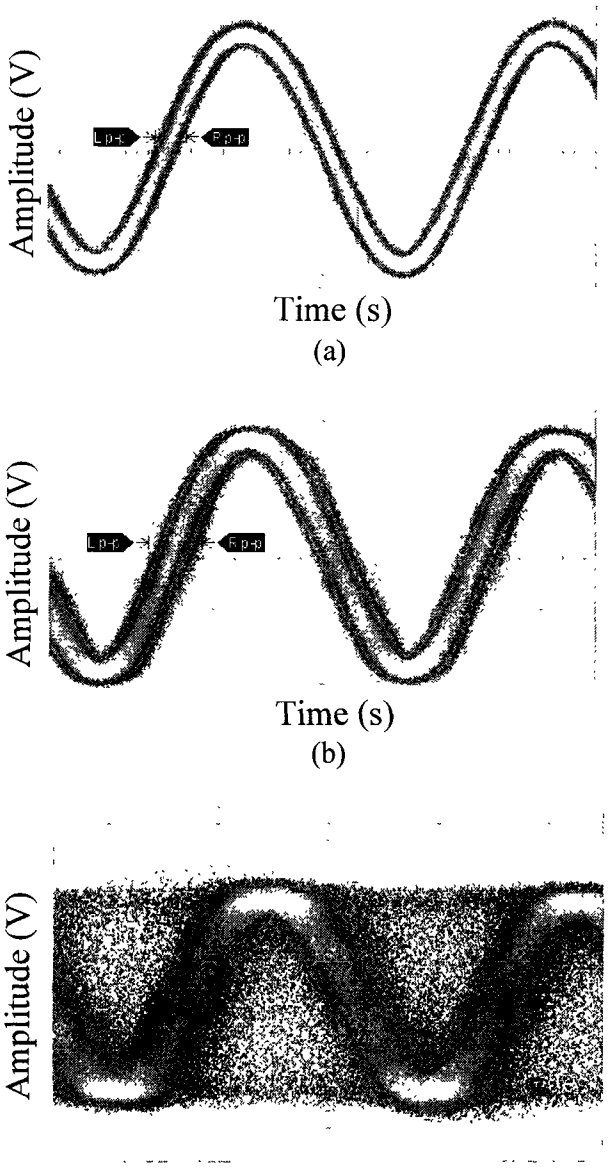


Figure 4.14 Measured eye diagrams of recovered clock, and the repetitive period is (a) 608 bits, (b) 1008 bits, and (c) 4208 bits.

We change the repetitive periods in the measurements. Figure 4.14 (a), (b), and (c) show the resulting eye diagrams of recovered clock for the repetitive period as the length of 608 bits, 1008 bits, and 4208 bits, respectively. We observed that when the number of gap bits increase, the jitter increases. This is because during the gap period, the ILO in the BM-CR goes into free-running state, and accumulates jitter over the time. The jitters of the ILO are usually from two sources. One is the internal noise of the ILO which universally exists for all kinds of oscillators [102]. The other is the noise from the frequency control voltage which is biased externally, due to the equipment noise. Longer gap period leads to larger accumulated jitter. In Figure 4.14 (c), the BM-CR reaches a state when its phase and frequency have no link to those of the data signal, namely pure free-running, during the gap period. However, we can observe a clear eye displayed with the background noise. By linking to Figure 4.11, we can understand that the eye diagram as shown in Figure 4.14 (c) is actually the combination of eye diagram in locked mode (i.e., Tx is on in Figure 4.14 (a)) and that in pure free-running mode (i.e., Tx is off in Figure 4.14 (b)), and indicate that the BM-CR locks to the data packets when they arrive, and goes to free-running during the gap period. This figure can prove that the locking time for the burst mode packet is well within 608 bits (equivalently around 68 ns), since clear eye of clock in locked state is shown. It is noted that such method is not precise in determination of locking time. Such method and corresponding eye diagram are very similar to the case in [103] (see Fig. 2 (c) inside), which also uses this kind

of overlapped clock eye diagram (including the clock eye diagrams at both data packet and gap periods) to confirm locking to burst mode packets.

We have demonstrated the burst mode clock recovery capability when the injected data signal is embedded with the clock tone due to the fiber dispersion. We are now going to demonstrate the BM CR capability when the data signal is generated by DML transmitter. It is noted that the obtained DML in the experiment is not stable at high bit-rate modulation (e.g., 10 Gbps) beyond its designed operation bit rate (i.e., less than 2 Gbps), especially when this DML is modulated by burst mode data. So we have to only use continuous mode data modulation.

In our measurement, the fiber length connecting various optical components (e.g., optical attenuator, DML transmitter) is kept as short as possible, to reduce the effects from fiber dispersion. In our simulation, we assumed that the DML laser has wavelength of 1310 nm, so we ignored the fiber dispersion. However, in the measurement, the DML laser we obtained has wavelength of 1550 nm. So we have to use an optical attenuator to emulate the fiber attenuation which does not introduce fiber dispersion.

We will test both the cases when the data pattern are "1010" and $2^7 - 1$ PRBS, respectively. The result for the "1010" data pattern is shown in the waveforms in Figure 4.15. The recovered clock waveform is clear, indicating that the clock is locked to the "1010" data.

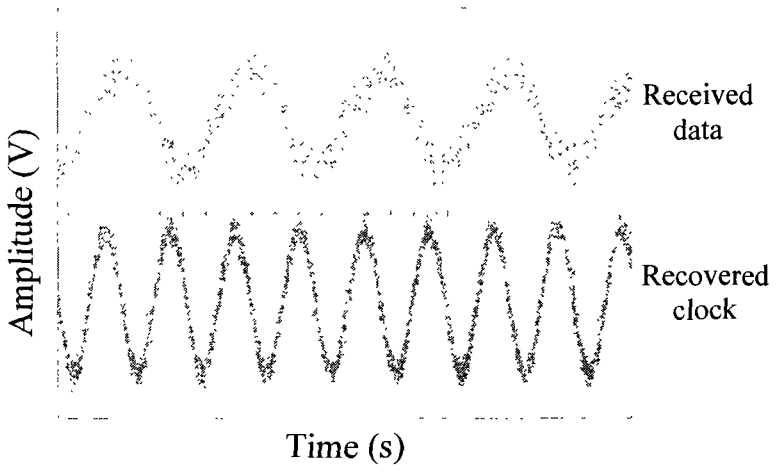
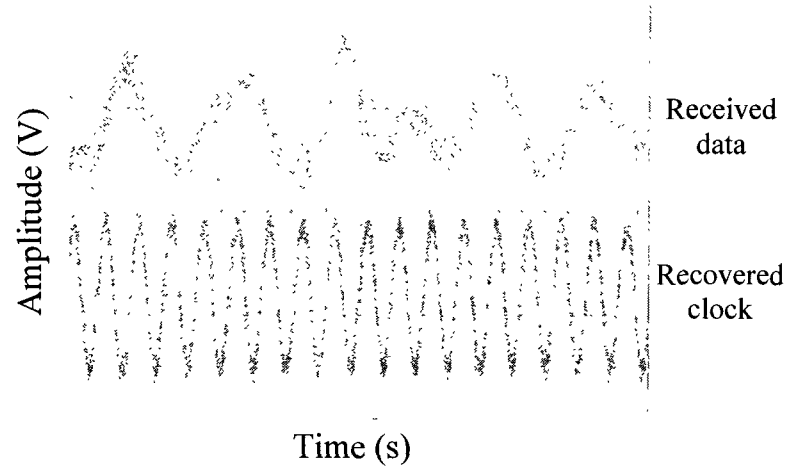
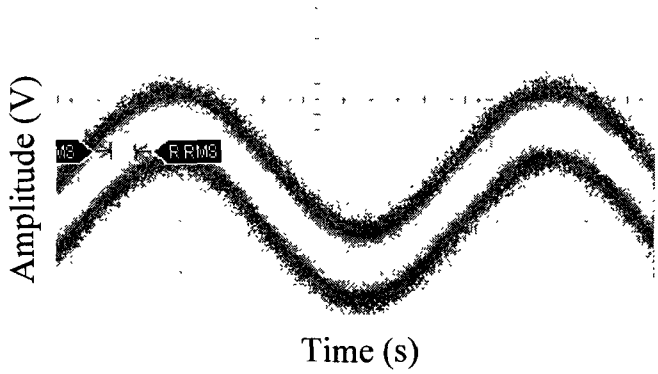


Figure 4.15 Measured waveforms of received data and recovered clock when the data pattern is "1010" (upper waveform is the received data, and the lower waveform is the recovered clock).

The measurement results for the PRBS data are shown in Figure 4.16. In Figure 4.16 (a), the upper waveform is the received data from DML transmitter. It is hard to tell the corresponding logic bits from the waveform, which demonstrates huge distortion because the DML is modulated at the frequency (8.9 GHz) much higher than its designed specification (less than 2 GHz). The lower waveform in Figure 4.16 (a) is the recovered clock, which is still clear, showing that the BM-CR can still lock to the data even when the data is highly distorted. To further analyze the performance, the eye diagram of the recovered clock is shown in Figure 4.16 (b).



(a)



(b)

Figure 4.16 Measured waveforms and eye diagrams of received data and recovered clock when the data pattern is PRBS. (a) The waveforms of received data and recovered clock, and (b) the eye diagram of the recovered clock.

We can recall that the data eye from the DML is almost closed, in Figure 4.7 (b). However, the clock tone due to the relaxation oscillation can still provide the clock information for the locking process. In Figure 4.16 (b), the jitter RMS of the recovered clock is 9.4 ps, demonstrating excellent jitter reduction capability. The measurement results demonstrate the usefulness of our designed BM-CR to be able to work in the situation the data is not well modulated due to poor DML performance.

3) Simplification in design – these schemes are simpler than the existing schemes by eliminating the clock tone generation circuit blocks or extra optical components;

4) No need of additional components – these schemes does not need to add additional electrical or optical components, but utilize the characteristics of the optical components already in the optical link, existing in either currently deployed or future PON;

5) Using low cost fabrication technology – 0.18 μm CMOS technology is used to tape out the BM CR circuit for its low cost;

6) Reduction of the chip area, the fabrication cost and the power consumption – since the circuit block to generate the clock tone is eliminated, the chip area, the fabrication cost and the power originally consumed by that circuit block are saved;

7) Easy integration with the following digital processing circuits on single chip – the choice of CMOS technology for fabrication allows the designed BM CR to serve as one circuit block to be integrated into the following digital circuits; and

8) Less sensitive to the fabrication mismatch – this is achieved by two ways, one is by allowing external frequency tuning, and the other is by using full-rate clock recovery architecture.

5.2 Recommendations

In Chapter 4, we designed and taped out the circuit using low cost CMOS technology, and the obtained BM-CDR bit rate is slightly less than 10 Gbps. In future work, we can use more advanced technologies, and design BM-CDR with higher bit rate, e.g., 40 Gbps or even 100 Gbps. Those high bit rate BM-CDR chips are very useful for the far future optical networks using burst packet transmission mode.

The burst mode clock recovery chip designed does not contain the function of data decision, mostly because the design for high bit rate data decision circuit (e.g., DFF) in low cost CMOS technology is very challenging and need much extra endeavour. Since it is not the focus of this work, it is not designed and included on chip. The future work could be including such circuit block on chip by exploring the published circuit topology and/or inventing new one.

Finally, the designed clock recovery chip used voltage injection instead of current injection. As explained, this option is chosen because the commercial photo-detector outputs voltage instead of photo-current, so the voltage injection scheme has to be employed if we need to use commercial photo-detector to simplify the experiment. However, using voltage injection induces less efficient injection for the current injection strength is dependant on the current oscillation in the RLC tank. The future work could be implementing the direct current injection scheme into the circuit chip, and attaching the photo-detector chip onto the circuit chip using MCM technology.

REFERENCES

[1] H. G. Perros, *Connection-Oriented Networks: SONET/SDH, ATM, MPLS, and Optical Networks*: John Wiley and Sons, 2005.

[2] X. Hong, M. Yan, and W.-P. Huang, "System demo for optical access networks," in *OPC (Ontario Photonic Consortium) Annual Meeting*. Hamilton, 2005.

[3] D. Nowak and J. Murphy, "FTTH: the overview of existing technologies," in *Proceedings SPIE*, vol. 5825, pp. 500-509, 2005.

[4] G. Keiser, *FTTX Concepts and Applications*: John Wiley & Sons, 2006.

[5] Rec. G.984: *Gigabit-capable Passive Optical Networks (GPON)*, ITU-T, 2003.

[6] M. Bass and E. W. V. Stryland, *Fiber Optics Handbook: Fiber, Devices, and Systems for Optical Communications*, 1 ed: McGraw-Hill Professional, 2001.

[7] M. Kawachi, "Recent progress in silica-based planar lightwave circuits on silicon," *IEE Proceedings Optoelectronics*, vol. 143, pp. 257-262, 1996.

[8] Y.-L. Sun, X.-Q. Jiang, J.-Y. Yang, Y. Tang, and M.-H. Wang, "Experimental demonstration of two-dimensional multimode-interference optical power splitter," *Chinese Physics Letters*, vol. 20, pp. 2182-2184, 2003.

[9] A. Banerjee, Y. Park, F. Clarke, H. Song, S. Yang, G. Kramer, K. Kim, and

B. Mukherjee, "A review of wavelength-division multiplexed passive optical network (WDM-PON) technologies for broadband access," *OSA Journal of Optical Networking*, pp. 737-758, 2005.

[10] D. J. Shin, D. K. Jung, H. S. Shin, J. W. Kwon, S. Hwang, Y. Oh, and C. Shim, "Hybrid WDM/TDM-PON with wavelength-selection-free transmitters," *Journal of Lightwave Technology*, vol. 23, pp. 187-195, 2005.

[11] Rec. G. 652: *Characteristics of a single-mode optical fibre cable*, ITU-T, 1997.

[12] S. Appathurai, D. Nesset, and R. Davey, "Measurement of tolerance to non-uniform burst powers in SOA amplified GPON systems," in *Optical Fiber Communication (OFC)*, 2007.

[13] F. T. An, D. Gutierrez, K. S. Kim, J. W. Lee, and L. G. Kazovsky, "SUCCESS-HPON: A next-generation optical access architecture for smooth migration from TDM-PON to WDM-PON," *IEEE Communications Magazine*, vol. 43, pp. S40-S47, 2005.

[14] R. P. Davey, D. Nesset, A. Rafel, D. B. Payne, and A. Hill, "Designing long reach optical access networks," *BT Technology Journal*, vol. 24, pp. 13-19, 2006.

[15] P. C. Becker and N. A. Olsson, *Erbium-Doped Fiber Amplifiers: Fundamentals and Technology*: Academic Press, 1999.

[16] I. P. K. Kaminow and T. Li, *Optical Fiber Telecommunications IV-A:*

Components: Academic Press, 2002.

[17] R. A. Salvatore, R. T. Sahara, M. A. Bock, I. Libenzon, C. Lasertron, and M. A. Bedford, "Electroabsorption modulated laser for long transmission spans," *IEEE Journal of Quantum Electronics*, vol. 38, pp. 464-476, 2002.

[18] Y. Kang, B. Young, H. Mun, and K. Jang, "Operation of 1550-nm electroabsorption-modulated laser at 40°C for 10-Gb/s, 40-km transmission," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 11, pp. 135-140, 2005.

[19] J. S. Han, M. J. Chu, J. S. Ko, K. M. Yoon, and Y. G. Lee, "Field trial of the 40 Gb/s ETDM prototype over 219 km of the installed single-mode fiber," *International Journal of Infrared Millimeter Waves*, vol. 16, pp. 231-236, 1995.

[20] B. Alfonsi, "I want my IPTV: Internet protocol television predicted a winner," *IEEE Distributed Systems Online*, vol. 6, pp. 4, 2005.

[21] YouTube, LLC, <http://www.youtube.com>.

[22] G. C. Burdea and P. Coiffet, *Virtual Reality Technology*: Wiley-IEEE, 2003.

[23] R. Wootton and V. Patterson, *Introduction to Telemedicine*: RSM Press, 2006.

[24] B. Razavi, *Design of Integrated Circuits for Optical Communications*: McGraw Hill, 2005.

[25] X. Z. Qiu, P. Ossieur, J. Bauwelinck, Y. Yi, D. Verhulst, J. Vandewege, B.

De Vos, and P. Solina, "Development of GPON upstream physical-media-dependent prototypes," *Journal of Lightwave Technology*, vol. 22, pp. 2498-2508, 2004.

[26] B. Razavi, "Prospects of CMOS technology for high-speed optical communication circuits," *IEEE Journal of Solid-State Circuits*, vol. 37, pp. 1135-1145, 2002.

[27] J. Savoj and B. Razavi, *High-Speed CMOS Circuits for Optical Receivers*: Springer, 2001.

[28] C. Su, L. K. Chen, and K. W. Cheung, "Theory of burst-mode receiver and its applications in optical multi-access networks," *Journal of Lightwave Technology*, vol. 15, pp. 590-606, 1997.

[29] M. Yan, C.-H. Chen, and W.-P. Huang, "A clock recovery scheme utilizing fiber dispersion for burst mode transmission," submitted to *Journal of Optical Communications*.

[30] J. Savoj and B. Razavi, "A 10-Gb/s CMOS clock and data recovery circuit with a half-rate binary phase/frequency detector," *IEEE Journal of Solid-State Circuits*, vol. 38, pp. 13-21, 2003.

[31] A. Li, J. Faucher, and D. V. Plant, "Burst-mode clock and data recovery in optical multiaccess networks using broad-band PLLs," *IEEE Photonics Technology Letters*, vol. 18, pp. 73-75, 2006.

[32] B. Sartorius, C. Bornholdt, S. Bauer, and M. Mohrle, "40 GHz optical clock recovery for application in asynchronous networks," in *European*

Conference on Optical Communication (ECOC), vol. 3, 2001.

[33] N. Pleros, K. Vyrsokinos, C. Bintjas, K. Yiannopoulos, K. Vlachos, H. Avramopoulos, and G. Guekos, "All-optical clock recovery from short asynchronous data packets at 10 Gb/s," *IEEE Photonics Technology Letters*, vol. 15, pp. 1291-1293, 2003.

[34] C. Bintjas, K. Yiannopoulos, N. Pleros, G. Theophilopoulos, M. Kalyvas, H. Avramopoulos, and G. Guekos, "Clock recovery circuit for optical packets," *IEEE Photonics Technology Letters*, vol. 14, pp. 1363-1365, 2002.

[35] D. Petrantonakis, G. T. Kanellos, P. Zakynthinos, D. Apostolopoulos, N. Pleros, and H. Avramopoulos, "40-Gb/s 3R burst mode regenerator using four integrated MZI switches," *IEEE Photonics Technology Letters*, vol. 19, pp. 288, 2007.

[36] J. Slovak, C. Bornholdt, S. Bauer, J. Kreissl, M. Schlak, and B. Sartorius, "Novel concept for all-optical clock recovery from NRZ format PRBS data streams," *Optical Fiber Communication Conference, 2006 and the 2006 National Fiber Optic Engineers Conference*, pp. 3, 2006.

[37] Y. Ota, R. G. Swartz, V. D. Archer, S. K. Korotky, M. Banu, and A. E. Dunlop, "High-speed, burst-mode, packet-capable optical receiver and instantaneous clock recovery for optical bus operation," *Journal of Lightwave Technology*, vol. 12, pp. 325-331, 1994.

[38] M. Yan, X. Hong, W.-P. Huang, and J. Hong, "Design of high-speed burst

mode clock and recovery IC for passive optical network," in *Photonic North (SPIE sponsored)*, 2005.

[39] J. Nakagawa, "Key technologies of GE-PON burst-mode receivers and future PON systems," in *Optical Fiber Communication (OFC)*, 2007.

[40] H. Lee, C. H. Yue, S. Palermo, K. W. Mai, and M. Horowitz, "Burst mode packet receiver using a second order DLL," *2004 Symposium on VLSI Circuits*, pp. 264-267, 2004.

[41] B. C. Thomsen, B. J. Puttnam, and P. Bayvel, "Optically equalized 10 Gb/s NRZ digital burst mode receiver for dynamic optical networks," *Optics Express*, vol. 15, pp. 9520-9526, 2007.

[42] T. Finateu, J.-B. Begueret, Y. Deval, and F. Badets, "GMSK modulation of subharmonic injection locked oscillators," in *European Solid-State Circuits Conference*, 2005, pp. 101 - 104.

[43] R. R. E. Hugues-Salas, T. J. Quinlan, M. P. Thakur, and S. D. Walker, "A 2.5 Gb/s edge-detecting burst-mode receiver for GPON access networks," in *Optical Fiber Communication (OFC) Conference*, 2007, pp. OThK6.

[44] S. B. Jun, P. K. J. Park, H. Kim, and Y. C. Chung, "Ultra-fast clock recovery based on pre-embedded sub-harmonic clock in optical burst/packet networks," in *Optical Fiber Communication (OFC)*, 2007, pp. JThA55.

[45] B. Franz, "Optical signal processing for very high speed (>40 Gbit/s) ETDM binary NRZ clock recovery," in *Optical Fiber Communication*

(OFC), 2001.

[46] A. H. Gnauck, X. Liu, X. Wei, D. M. Gill, and E. C. Burrows, "Comparison of modulation formats for 42.7-Gb/s single-channel transmission through 1980 km of SSMF," *IEEE Photonics Technology Letters*, vol. 16, pp. 909-911, 2004.

[47] W. Bogner, E. Gottwald, A. Schopflin, and C. J. Weiske, "40 Gbit/s unrepeatered optical transmission over 148 km by electrical time division multiplexing and demultiplexing," *Electronics Letters*, vol. 33, pp. 2136-2137, 1997.

[48] Z. Wang, A. Thiede, and M. Schlechtweg, "40Gbit/s/GHz clock recovery and frequency multiplying AlGaAs/GaAs-HEMT-IC using injection-synchronised narrowband ring-VCOs and auxiliary PLLs," *Electoronics Letters*, vol. 35, pp. 1151, 1999.

[49] G. Georgiou, Y. Baeyens, Y. K. Chen, C. Groepper, P. Paschke, R. Pullela, M. Reinhold, C. Dorschky, J. P. Mattia, and T. W. von Mohrenfels, "Clock and data recovery IC for 40 Gb/s fiber-optic receiver," *Gallium Arsenide Integrated Circuit (GaAs IC) Symposium,* pp. 93-96, 2001.

[50] Y. G. Baeyens, G. Weiner, J. S. Leven, A. Houtsma, V. Paschke, P. Lee, Q. Kopf, R. Chua, L. Chen, and C. Liu, "InP D-HBT ICs for 40-Gb/s and higher bitrate lightwave transceivers," *IEEE Journal of Solid-State Circuits*, vol. 37, pp. 1152-1159, 2002.

[51] M. Wurzer, J. Bock, H. Knapp, W. Zirwas, F. Schumann, and A. Felder, "A

40-Gb/s integrated clock and data recovery circuit in a 50-GHz f_T silicon bipolar technology," *IEEE Journal of Solid-State Circuits*, vol. 34, pp. 1320-1324, 1999.

[52] M. Reinhold, C. Dorschky, E. Rose, R. Pullela, P. Mayer, F. Kunz, Y. Baeyens, T. Link, and J. P. Mattia, "A fully integrated 40-Gb/s clock and data recovery IC with 1:4 DEMUX in SiGe technology," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 1937-1945, 2001.

[53] A. B. Ong, S. Cancio, J. Condito, V. Labrie, T. Q. L. Mattia, J. P. Shaeffer, D. K. Shahani, A. Tarsia, M. Wong, and W. M. Xu, "A 40-43-Gb/s clock and data recovery IC with integrated SFI-5 1:16 demultiplexer in SiGe technology," *IEEE Journal of Solid-State Circuits*, vol. 38, pp. 2155-2168, 2003.

[54] H. S. Muthali, T. P. Thomas, and I. A. Young, "A CMOS 10-Gb/s SONET transceiver," *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 1026-1033, 2004.

[55] S. Kimura, M. Nogawa, K. Nishimura, T. Yoshida, K. Kumozaki, S. Nishihara, and Y. Ohtomo, "A 10-Gbit/s CMOS burst-mode clock and data recovery IC for a WDM/TDM-PON access network," *The 17th Annual Meeting of the IEEE Lasers and Electro-Optics Society (LEOS 2004)*, vol. 1, 2004.

[56] Z. Gu and A. Thiede, "10 GHz full-rate clock and data recovery circuit in 0.18 μm CMOS without external reference clock," *Electronics Letters*,

vol. 40, pp. 1572-1574, 2004.

[57] P. S. Han and W. Y. Choi, "1.25/2.5-Gb/s burst-mode clock recovery circuit with a novel dual bit-rate structure in 0.18-μm CMOS," in *Proceedings of 2006 IEEE International Symposium on Circuits and Systems (ISCAS 2006)*, pp. 4, 2006.

[58] P. S. Han and W. Y. Choi, "1.25/2.5-Gb/s dual bit-rate burst-mode clock recovery circuits in 0.18-μm CMOS Technology," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 54, pp. 38-42, 2007.

[59] C. F. Liang, S. C. Hwu, and S. I. Liu, "A 10 Gbps burst-mode CDR circuit in 0.18 μm CMOS," in *IEEE Custom Integrated Circuits Conference 2006*, pp. 599-602.

[60] M. Yan, C.-H. Chen, and W.-P. Huang, "Burst-mode clock recovery utilizing relaxation oscillation in directly modulated lasers," submitted to *IEEE Journal of Lightwave Technology*, revised and under second review.

[61] B. Razavi, "A study of injection locking and pulling in oscillators," *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 1415-1424, 2004.

[62] T. H. Lee and A. Hajimiri, "Oscillator phase noise: a tutorial," *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 326-336, 2000.

[63] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 179-194, 1998.

[64] C. Toumazou, *Trade-Offs in Analog Circuit Design: the designer's*

companion: Kluwer Academic Publishers, 2002.

[65] B. Razavi, *RF microelectronics*: Prentice-Hall, Inc., 1998.

[66] R. L. Bunch and S. Raman, "Large-signal analysis of MOS varactors in CMOS-G_m-LC VCOs," *IEEE Journal of Solid-State Circuits*, vol. 38, pp. 1325-1332, 2003.

[67] Y. Deval, J. Begueret, A. Spataro, P. Fouillat, D. Belot, F. Badets, and B. I. Ixl, "HiperLAN 5.4-GHz low-power CMOS synchronous oscillator," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, pp. 1525-1530, 2001.

[68] Y. Wan, X. Lai, and J. Roychowdhury, "Understanding injection locking in negative-resistance LC oscillators intuitively using nonlinear feedback analysis," in *Proceedings of the IEEE Custom Integrated Circuits Conference*, 2005, pp. 729- 732.

[69] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*: Cambridge University Press, 1998.

[70] The MathWorks, Inc., <http://www.mathworks.com>.

[71] M. Tiebout, "A CMOS direct injection-locked oscillator topology as high-frequency low-power frequency divider," *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 1170-1174, 2004.

[72] M. De Matos, J. B. Begueret, H. Lapuyade, D. Belot, L. Escotte, and Y. Deval, "A 0.25um SiGe receiver front-end for 5GHz applications," *SBMO/IEEE MTT-S International Conference on Microwave and*

Optoelectronics 2005, pp. 213-217.

[73] J. Lee and M. Liu, "A 20Gb/s burst-mode CDR circuit using injection-locking technique," in *IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 46-586, 2007.

[74] K. P. Ho and J. M. Kahn, "Spectrum of externally modulated optical signals," *Journal of Lightwave Technology*, vol. 22, pp. 658-663, 2004.

[75] J. G. Proakis, *Digital Communication*: McGraw-Hill, 2001.

[76] C. Kromer, G. Sialm, T. Morf, M. L. Schmatz, F. Ellinger, D. Erni, and H. Jackel, "A low-power 20-GHz 52-dBΩ transimpedance amplifier in 80-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 885-894, 2004.

[77] G. Agrawal, *Nonlinear Fiber Optics*, 3rd ed: Academic Press, 2001.

[78] F. Heismann, "Origin of clock-frequency components in NRZ-formatted optical signals," *IEEE Photonics Technology Letters*, vol. 15, pp. 912-914, 2003.

[79] Z. Y. Pan, Q. Xie, Y. Havstad, S.A. Willner, A.E. Starodubov, and D.S. Feinberg, J., "Chromatic dispersion monitoring and automated compensation for NRZ and RZ data using clock regeneration and fading without adding signaling," in *Optical Fiber Communication (OFC) Conference*, vol. 3, pp. WH5-1- WH5-3, 2001.

[80] S. Fu, M. Tang, W. D. Zhong, Y. J. Wen, and P. Shum, "All-optical NRZ-DPSK clock recovery using chromatic-dispersion-induced clock tone," *IEEE Photonics Technology Letters*, vol. 19, pp. 925-927, 2007.

[81] T. Gabara, "An 0.25 μm CMOS injection locked 5.6 Gb/s clock and data recovery cell," in *Symposium on Integrated Circuits and Systems Design* 1999, pp. 84 - 87.

[82] Recommendation G. 983.1: *Broadband optical access systems based on passive optical networks*, ITU-T, 1998.

[83] B. Meagher, G. K. Chang, G. Ellinas, Y. M. Lin, W. Xin, T. F. Chen, X. Yang, A. Chowdhury, J. Young, and S. J. Yoo, "Design and implementation of ultra-low latency optical label switching for packet-switched WDM networks," *Journal of Lightwave Technology*, vol. 18, pp. 1978-1987, 2000.

[84] J. Buckwalter and A. Hajimiri, "A 10Gb/s data-dependent jitter equalizer," in *Proceedings of the IEEE 2004 Custom Integrated Circuits Conference*, pp. 39-42.

[85] J. S. Hwang, C. S. Park, and C. S. Park, "155-Mb/s burst-mode clock recovery circuit using the jitter reduction technique," *IEICE Transactions on Communications*, vol. 86, pp. 1423-1426, 2003.

[86] G. P. Agrawal, *Fiber-Optic Communication Systems*, 3rd ed.: John Wiley & Sons, 2002.

[87] G. P. Agrawal, *Lightwave Technology Telecommunication Systems*: Wiley-Interscience, 2005.

[88] J. D. Downie, M. Sauer, and J. Hurley, "Flexible 10.7 Gb/s DWDM transmission over up to 1200 km without optical in-line or post-

compensation of dispersion using MLSE-EDC," in *Optical Fiber Communication (OFC) Conference,* 2006.

[89] J. W. Raring, L. A. Johansson, E. J. Skogen, M. N. Sysak, H. N. Poulsen, S. P. DenBaars, and L. A. Coldren, "40 Gbit/s photonic receivers integrating UTC photodiodes with high-and low-confinement SOAs using quantum well intermixing and MOCVD regrowth," *Electronics Letters*, vol. 42, pp. 942-943, 2006.

[90] G. P. Agrawal and N. K. Dutta, *Semiconductor Lasers*: 2nd ed. New York: Van Nostrand Reinhold, 1993.

[91] J. C. Cartledge and R. C. Srinivasan, "Extraction of DFB laser rate equation parameters for system simulation purposes," *Journal of Lightwave Technology*, vol. 15, pp. 852-860, 1997.

[92] J. Katz, S. Margalit, C. Harder, D. Wilt, and A. Yariv, "The intrinsic electrical equivalent circuit of a laser diode," *IEEE Journal of Quantum Electronics*, vol. 17, pp. 4-7, 1981.

[93] RSoft Design Group, Inc. <http://www.rsoftdesign.com>.

[94] M. A. Kossel and M. L. Schmatz, "Jitter measurements of high-speed serial links," *IEEE Design & Test of Computers*, vol. 21, pp. 536-543, 2004.

[95] J. A. P. Morgado and A. V. T. Cartaxo, "Directly modulated laser parameters optimization for metropolitan area networks utilizing negative dispersion fibers," *IEEE Journal of Selected Topics in Quantum*

Electronics, vol. 9, pp. 1315-1324, 2003.

[96] R. Murji and M. J. Deen, "A low-power, 10 GHz back-gated tuned voltage controlled oscillator with automatic amplitude and temperature compensation," in *International Symposium on Circuits and Systems 2004 (ISCAS'04)*, vol. 4, 2004.

[97] Y. Nakasuga, T. Hashimoto, Y. Yamada, H. Terui, M. Yanagisawa, K. Moriwaki, Y. Akahori, Y. Tohmori, K. Kato, and S. Sekine, "Multi-chip hybrid integration on PLC platform using passive alignment technique," *Proceedings of 46th Electronic Components and Technology Conference,* 1996, pp. 20-25.

[98] J. Zhan, J. Duster, and K. Komegay, "A full-rate injection-locked 10.3 Gb/s clock and data recovery circuit in a 45GHz-f_T SiGe process," *Proceedings of the IEEE Custom Integrated Circuits Conference*, vol. 2005, pp. 557, 2005.

[99] T. Gabara, "A 3.25 Gb/s injection locked CMOS clock recovery cell," in *Proceedings of the IEEE Custom Integrated Circuits*, pp. 521-524, 1999.

[100] H. C. Chang, "Phase noise in self-injection-locked oscillators-theory and experiment," *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, pp. 1994-1999, 2003.

[101] A. X. Widmer and P. A. Franaszek, "A DC-balanced, partitioned-block, 8B/10B transmission code," *IBM Journal of Research and Development*, vol. 27, pp. 440-451, 1983.

[102] B. Razavi, *Design of Analog CMOS Integrated Circuits*: McGraw-Hill, Boston, MA, 2001.

[103] Z. Hu, B. R. Koch, J. E. Bowers, and D. J. Blumenthal, "Integrated photonic/RF 40-Gb/s burst-mode optical clock recovery for asynchronous optical packet switching," in *Optical Fiber Communication (OFC) Conference*, 2006.