Advancing Ultra-Wideband Technology: High-Throughput Low-Cost Compact Pulsed Radars for Portable and Mobile Platforms

ADVANCING ULTRA-WIDEBAND TECHNOLOGY: HIGH-THROUGHPUT LOW-COST COMPACT PULSED RADARS FOR PORTABLE AND MOBILE PLATFORMS

BY

AARON D. PITCHER, M.A.Sc.

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AUTHOR:	Aaron D. Pitcher M.A.Sc., (Electrical Engineering) McMaster University, Hamilton, Canada
SUPERVISOR:	Dr. Natalia K. Nikolova Ph.D. (Electrical Engineering) University of Electro-Communications, Tokyo, Japan P. Eng. (Ontario)
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To my family

ABSTRACT

Emerging ultra-wideband (UWB) imaging and sensing applications in the low-gigahertz electromagnetic spectrum demand high-throughput, low-cost, and compact radar solutions for portable and mobile sensing. This work introduces a novel UWB pulse radar system capable of capturing thousands of polarimetric radar measurements per second, enabling advanced target detection and identification techniques, including those based on statistical signal processing, machine learning, and artificial intelligence. The realized system achieves a 1:10 fractional bandwidth (FBW) ratio, spanning 500 MHz to beyond 5 GHz at the -10 dB level. The first key contribution is the development of a picosecond pulse generator producing an ultra-stable monocycle-like waveform. This contribution also includes developing a set of rigorous metrics and measurement procedures to evaluate UWB pulse generators, filling a substantial gap in the emerging UWB technology. The second key contribution is the development of a field-programmable gate array (FPGA) controlled dual-channel equivalent-time sampling receiver (ETSR) based on a novel system architecture. The receiver's unprecedented accuracy and stability is achieved due to the proposed simple but effective calibration method. The method quantifies and corrects the systematic timebase distortion due to the programmable delay chip (PDC). Also, a set of rigorous performance metrics and measurement procedures are proposed to evaluate and compare time-sampling receivers. Similar to the metrics developed for the UWB

generators, the receiver metrics have provided the much-needed means of evaluating UWB time-sampling receivers. Finally, a parallelized FPGA architecture is proposed to resolve the main shortcoming of current FPGA-based radars, namely, the low processing throughput. The novel FPGA architecture allows the receiver to achieve a remarkable speed of over 9 000 waveforms per second on each channel. As the radar data rate far exceeds the Ethernet link capacity, the FPGA-based processing is leveraged to reduce offloaded data while fully utilizing the radar output with minimal data loss.

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AC	Alternating current
ADC	Analog-to-digital converter
AWG	Arbitrary waveform generator
AXI	Advanced extensible interface
BIST	Built-in self-test
BJT	Bipolar junction transistor
CDC	Clock domain crossing
CMOS	Complementary metal-oxide-semiconductor
CPU	Central processing unit
CPW	Co-planar waveguide
CW	Continuous wave
CWD	Concealed weapon detection
DARPA	Defense Advanced Research Program Agency
DC	Direct current
DMAC	Direct memory access control
DSP	Digital signal processing
DSPPL	Digital signal processing pipeline
DUT	Device under test
EMI	Electromagnetic interference
ET	Equivalent-time
ETSR	Equivalent-time sampling receiver
FBW	Fractional bandwidth
FCC	Federal Communications Commission
FFT	Fast Fourier transform
FIFO	First-in first-out
FMC	FPGA mezzanine card
FMCW	Frequency-modulated continuous-wave
FPGA	Field-programmable gate array
FOM	Figure of merit
FPGA	Field-programmable gate array
FPS	Frames per second
FSM	Finite state machine
FWHM	Full-width half maximum
Gbps	Gigabit per second
GPR	Ground penetrating radar
GSa/s	Giga-samples per second

HDL	Hardware description language
HPBW	Half-power beamwidth
IC	Integrated circuit
LDO	Low-dropout
LNA	Low noise amplifier
LVDS	Low voltage differential signaling
LwIP	Light-weight internet protocol
MAC	Multiplier-accumulator
MCU	Microcontroller
MSa/s	Mega-samples per second
NDT	Non-destructive testing
NLTL	Nonlinear transmission line
NPN	Negative-positive-negative
PCB	Printed circuit board
PDC	Programmable delay chip
PDF	Probability distribution function
PLL	Phase-locked loop
PRF	Pulse repetition frequency
PRI	Pulse repetition interval
PSD	Power spectrum density
RF	Radio frequency
RMS	Root-mean-square
RT	Real-time
RTOS	Real-time operating system
Rx	Receiving
SAR	Synthetic Aperture Radar
SD	Schottky diode
SMP	Symmetric multiprocessing
SFCW	Stepped-frequency continuous wave
SFDR	Spurious free dynamic range
SNR	Signal-to-noise ratio
SoC	System on a chip
SR	Slew rate
SRD	Step recovery diode
T&H	Track and hold
TTL	Transistor-transistor logic
Tx	Transmitting
UAV	Unmanned aerial vehicle
UWB	Ultra-wideband
VCO	Voltage controlled oscillator
VNA	Vector network analyzer
Wfm/s	Waveforms per second

CHAPTER 1:

INTRODUCTION

1.1 Historical Perspective of UWB Radar

The history of ultra-wideband (UWB) radar systems goes all the way back to the first man-made electromagnetic wave generation by sparks in Heinrich Hertz's groundbreaking experiments. Using a spark-gap generator and a loop antenna, Hertz demonstrated the existence of radio waves in 1880s, validating Maxwell's theoretical predictions [1]–[3]. These experiments employed the excitation and detection of short-duration electromagnetic pulses, generated by sparks, effectively pioneering the concept of wideband signals. His work laid the groundwork for technologies that would later apply these principles to radar and communication systems.

Following Hertz's experiments, spark-gap generators became widely adopted for proof-of-concept radars and wireless communication, i.e., telegraphy [4]–[7]. However, spark-gap generators were power inefficient and costly, and they caused difficulty in controlling interference with their broad spectral emissions. Thus, they were eventually supplanted by continuous wave (CW) technologies. At the same time, researchers

recognized the potential of the short-pulse waves for radar applications, where temporal resolution and the ability to penetrate obstacles were critical [8]. CW single-frequency radars could only provide Doppler information, i.e., the target's speed. Therefore, the exploration of pulsed signals for target detection and localization continued unabated, setting the stage for modern UWB pulsed radars for sensing and imaging.

The advent of radar during the Second World War marked a significant milestone in electromagnetic technology. While most radar systems employed narrowband CW signals, some pulsed radars were developed with enhanced resolution capabilities for military applications [8]–[10]. The development during this time period demonstrated how short pulses could be leveraged to detect, localize and characterize objects [11]. The first radar applications of this kind were for detecting and tracking large objects in the far zone of the antennas, such as planes, ships and submarines. However, ultra-short pulses that could excite a UWB spectrum by today's standards would remain out of reach for some time due to inadequate electronics technologies [3], [12].

During the 1950s and 1960s, military scientists and researchers returned to civilian life, exploring new radar applications in high-resolution imaging and target detection [8], [13]. In the decades following the war, advances in high-frequency electronics, computing technologies, and signal processing paved the way for more sophisticated radar systems. The heightened security around the Cold War and the innovation prompted by the Space Race pushed radar systems to new heights. Radar detection advanced beyond simple detection and localization toward target recognition by extracting features and information from the echo signal. The first airborne Synthetic Aperture Radar (SAR) was introduced to provide high-resolution mapping of ground scenes [13], [14]. Doppler radar systems were harnessed by meteorology, enabling weather monitoring and warning systems around the globe [15]. Chirp radars, i.e.,

linear frequency-modulated continuous-wave (FMCW) radars, were introduced to enable the detection of very small targets at greater ranges with higher range and angular resolutions than the traditional CW radars [16]. These advancements prompted the development of technology for generating ultra-short pulses with instantaneous bandwidths of unprecedented spectral coverage [12], [17]–[19].

Nearly a century after Hertz's pioneering experiments, advances in semiconductor technology at the end of the 20th century facilitated not only the efficient generation but also the reception and the processing of wideband signals [18]–[21]. In 1990, the first definition of UWB signals was introduced by the United States Defense Advanced Research Program Agency (DARPA) [22] supporting numerous projects aimed at developing UWB radar for ground penetrating radar (GPR), through-wall imaging, and covert communication. The advent of fast-switching electronics and digital signal processing made it possible to generate and analyze ultra-short pulses with unprecedented precision. During this period, the first commercial applications of UWB radar emerged in automotive collision avoidance and non-destructive testing (NDT). However, the lack of regulatory standards for UWB technology posed challenges as its broad spectral emissions could interfere with existing systems in the already over-crowded electromagnetic spectrum.

The turning point for UWB technology came in 2002, when the United States Federal Communications Commission (FCC) established regulations [23] that allocated unlicensed frequency bands for UWB devices under strict emission limits. The regulations define the UWB systems as those operating within the frequency range from 100 MHz to 10.6 GHz, and with an absolute bandwidth exceeding 500 MHz or a factional bandwidth[1] greater than 20% [3], [12], [23]. This regulatory milestone

[1]The fractional bandwidth is defined as $B_{\mathrm{f}} = (f_{\mathrm{h}} - f_{\mathrm{l}})/f_{\mathrm{c}}$ where the lower (f_{l}) and upper (f_{h}) frequencies indicate the -10-dB bandwidth, and $f_{\mathrm{c}} = 0.5(f_{\mathrm{h}} + f_{\mathrm{l}})$.

enabled the commercialization of UWB technology, spurring innovation in modern UWB radar and communication systems.

1.2 Emerging UWB Radar Applications

In recent decades, emerging UWB systems have enabled new applications in imaging and detection. These applications are growing rapidly, driven by advancements in semiconductor technology, increased computational power, and supportive regulatory environments. These new research efforts explore mostly short-range applications. The term "short range" is not to be confused with the near-field zones of the employed antennas. So far, the radar range has remained a somewhat ambiguous concept, i.e., no agreed-upon quantitative limit separates long-range from short-range radar applications. Here, the definition is adopted, which states that long-range applications involve distances to target greater than one of the following: (i) the target size, (ii) the largest antenna dimension, or (iii) the wavelength [24]. Meanwhile, short-range applications are at distances comparable to or shorter than at least one of the three items listed above.

Some of the high-impact emerging applications are listed below:

- **Security and Surveillance**: Non-imaging detection methods are employed to detect threat objects (e.g. guns, knives, grenades or explosive vests) hidden under clothing or in baggage, based on analyzing the early-time and late-time responses of back-scattered signals or by feature extraction based on estimated radar-cross section and polarization ratios [25]–[32]. Imaging methods are used for threat or fault detection behind barriers such as the proposed through-wall or see-through-wall systems [33]–[36].

- **Ground Penetration, Search and Rescue, and NDT**: There is a great need for radar systems to image and detect objects visually obscured by mediums opaque to visible light. For instance, GPR has been around for decades [37]–[39]. However, new emerging GPR systems employ lightweight and compact radar systems mounted on unmanned aerial vehicles (UAVs) or drones for landmine, metal and object detection [40]–[42]. The same technology can also aid search and rescue efforts by detecting people trapped under rubble, snow, or lost outdoors [43], [44]. Mobile NDT systems enable the inspection of defects in building foundations, roadways, and tunnels, or with localizing pipes and wires behind walls [37].

- **Indoor Positioning and Navigation**: The precise ranging and localization with UWB radar provides superior positional information necessary for robotic navigation [45], [46]. The boom of autonomous robotics for aerial- and ground-based transportation necessitates accurate and lightweight solutions. UWB radar is also employed for asset tracking and precise localization of items, devices and people [3], [47]–[49]

- **Automotive Safety Systems**: UWB radar has found applications in adaptive cruise control, automatic emergency brake, blind spot detection, lane change assist, pedestrian and cyclist detection, front and read cross-traffic alert, and parking assist systems [50]–[53].

- **Smart Agriculture**: In addition to enhanced ranging and localization solutions for autonomous agricultural machines [46], the application of UWB technology is being explored for biomass measurements, vegetation water content, and soil moisture estimation [54]–[57]. Frequently, the deployment is on UAVs and surveillance drones [54], [57].

- **Medical Imaging and Diagnostics**: Microwave imaging and detection methods are being developed for affordable alternatives to breast-cancer screening, water accumulation, and stroke detection [3], [24], [58]–[60]. Several prototypes have been developed for routine health monitoring of vital signs, non-invasive glucose monitoring, wearable sweat monitoring, gait monitoring, and fall detection [3], [35], [61], [62].

1.3 Modern Developments in UWB Radar Technologies

UWB applications have benefited from state-of-the-art hardware and modern signal-processing techniques. This section highlights the key technology developments that made the presented novel UWB radar system possible. An extensive and recent overview can be found in [63].

A major development is the miniaturization and the cost reduction of microelectronics operating within the UWB spectrum. Meanwhile, it must be acknowledged that the counterpart stepped-frequency continuous wave (SFCW) and FMCW technologies have seen remarkable advancement toward compact on-chip radar solutions [64], [65]. Generating and digitizing large instantaneous bandwidths requires multi-giga-samples per second (GSa/s) rates to sample the signals with sufficient density. To this end, proof-of-concept developments often use benchtop instrumentation (e.g., arbitrary waveform generators and high-speed real-time (RT) oscilloscopes). These systems are versatile, highly accurate, and convenient for early-stage prototype testing. However, they are impractical for real-world applications, where low cost and small size/weight are required, especially in mobile and large-scale network deployments. Recent advancements in equivalent-time (ET) sampling oscilloscopes [66], [67],

which can function as UWB receivers, have led to more compact designs. However, these systems remain expensive compared to the approach presented here and lack transmitter control capabilities for UWB radar applications. A key limitation is their offload speed, which is restricted to approximately 480 MB/s [66], [67], significantly constraining the amount of data transferred to an external signal-processing computer. For instance, the RT analog-to-digital converter (ADC) in [67] generates 12 bits per sample per channel at 500 mega-samples per second (MSa/s). When both channels are utilized, this results in a 1.5 GB/s data stream from the ADC, yet less than one-third of this can be offloaded for processing. Thus, the transition to a commercially viable radar system for the particular application involves a lengthy and expensive hardware development stage, which seriously impedes the growth of modern UWB radar technology. Therefore, there is a great need for well-characterized, versatile, accurate and compact UWB radar systems and/or modules (generators and time-sampling receivers).

At the same time, only a few commercial pulsed radar systems are available, as shown in Table 1.1, all of which are extremely band-limited with bandwidths ranging from 2 GHz to 2.5 GHz at the most. This makes them incapable of taking full advantage of the allocated UWB spectrum (3.1 GHz to 10.6 GHz) and makes them less versatile than what designers need. Also, the limited system bandwidth translates into poor temporal and spatial resolutions, which is detrimental to the expansion into new sensing and imaging applications. Table 1.1 lists the commercial UWB radar chips and devices, their release year, operating frequencies and production status. Additionally, the compact ET oscilloscopes [66], [67] have been added for comparison. It is evident that most commercial developments in this space emerged circa 2020s. Note that none of these products cover frequencies below 3.1 GHz and down to 100 MHz, where applications must resort to custom hardware development. To date, the

custom radar architectures which can excite lower frequencies are still at the discrete circuit and chip layout stages [33], [34], [43], [64], [68]–[78].

At the current stage, several challenges still exist from a hardware perspective. For instance, UWB signals require very high sampling rates, which in turn demand fast processing and data transfer in the receiver system, so that full waveform utilization is achieved without data loss. But ADCs with sampling rates in the GSa/s range are very expensive, and so is the digital circuitry that can process and transfer such ADC output. Alternatively, methods that extend the pulse timebase [68], [69] or perform ET sampling (or sub-sampling) [33], [34], [43], [64], [70]–[78] have been proposed, enabling sampling with a lower sampling rate ADCs. These methods exploit the periodic nature of the pulse train to reconstruct one pulse waveform from a measurement over multiple periods. But this comes at the expense of an extended measurement time, which hinders applications in detecting and tracking fast-moving objects. Also, high measurement speed with matching data throughput to the signal processing unit is crucial for emerging applications that rely on statistically large datasets collected over very short time periods.

The advent of machine learning, artificial intelligence, and statistical modelling have revolutionized the UWB radar's ability to operate in complex dynamic environments and deal with fast-moving targets. Advanced learning models process complex, high-dimensional radar data to detect subtle patterns, improve clutter reduction, and enhance target classification [32], [63], [65], [79]. These algorithms open countless opportunities for autonomous adaptation to dynamic environments, improve system intelligence, and reduce false alarms. However, UWB radars are not yet equipped to support these large dataset requirements as they must achieve significantly higher measurement speed and data throughput.

Lastly, as UWB radar technology advances toward compact low-cost solutions with

Table 1.1: Overview of commercial UWB radar chips and devices.

Manufacturer	**Chip**	**Device**	**Year**	**Freq. (GHz)**	**Status**
Aria Sensing	LTM103OEM	LTM103OEM UWB Radar Module	2020	7.3 - 8.5	Released
	AHM2D/AHM3D	NA	2024	7.3 - 9	Pre-Production/ New Release
Novelda	X4	X4M02	2017	7.29 - 8.75	Released
	X7	X7 Direct Radar Module	2024	7.5 - 8.25	Pre-Production/ New Release
NXP Trimension	SR250	Murata Type 2HQ	2024	NA	Pre-Production/ New Release
	SR150	Murata Type 2BP EVK	2021	6.24 - 8.24	Released
	SR040	Murata Type 2DK EVK	2021	6 - 8.5	Released
	NCJ29D6	NA	2023	6 - 8.5	Released
	NCJ29D5	OrangeBox, NCJ29D5 Eval Board	2019	6 - 8.5	Released
Time Domain Systems Inc. / Humatic / TDSR	P400	PulsON 400	2011	3.1 - 5.3	Obsolete
	P410	PulsON 410	2012	3.1 - 5.3	Obsolete
	P440	PulsON 440	2015	3.1 - 4.8	Obsolete
	P452	TSDR P452	2024	3.1 - 5.3	Pre-Production/ New Release
Qorvo	DW1000	DWM1001-DEV	2013	3.5 - 6.5	Released
	DW3110	DWM3000EVB	2020	6.5 - 8	Released
ST	B-UWB-MOD1	B-UWB-MEK1	2021	3.25 - 4.75	Proposed
Microchip	ATA8350	ATA8350-EB1	2021	6.2 - 7.8	Proposed
	ATA8352	ATA8352-EB1	2021	6.2 - 8.3	Proposed
Eltesta	NA	FemtoScope 2052	2020	DC - 5 GHz	Released
Pico Technology	NA	PicoScope 9402-05	2021	DC - 5 GHz	Released

NA stands for "Not Available".

larger bandwidths and higher data throughput, it becomes imperative to evaluate and compare the emerging systems quantitatively. Yet, standardized or widely agreed upon metrics are lacking, and so are the measurement procedures for these metrics. Too often, the literature focuses on showcasing radar systems with their application-specific performance metrics. While this is promoting the specific applications, it does not support the progress of the UWB hardware technology. The versatility of the new radar systems proposed in the scientific literature appears to be very limited since they are always tailored to particular applications. This may not always be the case, but the lack of clarity about the limitations of the hardware obscures their broader applicability. Often, performance metrics such as jitter and noise are overlooked, but these are essential in determining the noise floor along with the system's dynamic range and stability. Another example of a lacking metric is the receiver bandwidth. The customary practice is to report only the input impedance-match bandwidth of the radio frequency (RF) front-end in the receiver. However, this is only one of many factors determining the frequency-dependent input-to-output performance of a UWB time-sampling receiver.

1.4 Research Objectives

This research aims to develop a versatile UWB radar system to enable and support a wide range of emerging sensing and imaging applications. The proposed system provides time-domain measurements at GSa/s sampling rates with remarkable accuracy and versatility (on par with a benchtop high-speed oscilloscope), but at a much lower cost and in a very compact size in order to support deployment on portable and/or vehicular platforms.

Proof-of-concept development of new custom UWB-radar applications often employs bench-top instrumentation, which is, by design, versatile and highly accurate. However, these instruments are prohibitively expensive, large, and heavy. Thus, advancing to a practical, low-cost, small-form-factor system requires lengthy and expensive custom hardware development. Here, we propose an accurate FPGA-based low-cost, compact, and versatile UWB radar system, which is not application specific or even excitation specific. The proposed radar system features a UWB receiver, which works with various types of transmitters (pulsed or continuous wave), provided a synchronization method is available and the transmitted spectrum is within the receiver bandwidth.

This research also targets ultra-fast measurements with high-throughput capability to support a novel non-imaging method for unattended and unobtrusive radar surveillance detecting concealed weapons under clothing or in bags [25], [31]. Current security checkpoints at public venues rely on technologies with limited throughput capabilities and require trained personnel to be close to the inspected individual, who must comply with instructions and remain still. These limitations preclude continuous automated surveillance. The non-imaging methods detect concealed objects by analyzing the radar return through early-time and late-time responses or extracting features such as radar cross-section and polarization ratios [25]–[32]. The approach in [31] leverages the resonant signatures of weapons (e.g., handguns, knives, grenades, explosive vests) in the 400 MHz to 5 GHz range [26], [30]. Since UWB radars operating in this frequency band are unavailable, the new system architecture and pulse generator proposed here are implemented into prototypes operating in this frequency band.

1.5 Contributions

The author has contributed to the development of novel UWB pulsed-radar technology in the following ways:

1. Developed and demonstrated an ultra-stable picosecond pulse generator [80], which features higher center frequency, bandwidth, and peak-to-peak voltage compared to prior art. For the first time, a design approach is delineated allowing for modifying the pulse parameters by tuning key circuit components. This work also highlights the importance of jitter and noise characterization for pulse generators. Including a jitter cleaner demonstrates the trigger's impact on the pulse stability. This work also provides a rigorous set of performance metrics and measurement procedures to evaluate and compare pulse generators.

2. Proposed an accurate high-speed equivalent-time sampling receiver (ETSR) architecture and performance metrics for time-sampling receivers [81]. The architecture employs a programmable delay chip (PDC) to achieve an ultra-high measurement speed of over 9 000 waveforms per second with 20-GSa/s ET sampling rate. Importantly, PDC timebase distortion is identified and quantified. A calibration method is proposed to correct the PDC systematic errors, which is critical for realizing highly accurate sampling at picosecond intervals [81], [82]. Time-sampling receiver performance metrics are proposed and used to evaluate and compare the new UWB receiver with previously reported prototypes and bench-top oscilloscopes.

3. Proposed and implemented a new parallelized architecture for field-programmable gate array (FPGA) firmware design to achieve ultra-fast processing and data

throughput for the low-cost dual-channel UWB pulsed-radar system [83]. Implemented a hardware description language (HDL) design, which minimizes the data loss and maximizes the throughput efficiency of the radar's receiver. For the first time, this work demonstrates how electromagnetic interference suppression can be implemented in the FPGA-based signal pre-processing and how it improves the resilience of the UWB radar to common interference sources, e.g., Wi-Fi transmissions. Since the radar data rate exceeds the offload capability, this work demonstrates how the FPGA-based processing can be leveraged to reduce the offload burden.

1.6 Outline of the Thesis

This thesis presents the research results toward realizing new high-throughput, low-cost, and versatile UWB radar systems. The thesis focuses on the necessary hardware improvements required to enable the emerging applications outlined above.

Chapter 2 introduces a picosecond pulse generator for a stable differentiated Gaussian (monocycle) waveform generation. It presents design approaches that increase the center frequency, bandwidth and peak-to-peak voltage compared to previously reported UWB generators. The 280 ps wide pulse achieves a 1:10 fractional bandwidth (FBW) ratio extending from 500 MHz to beyond 5 GHz at the -10 dB level. A measurement procedure is proposed for evaluating the jitter and noise performance, and the impact of the input trigger on the pulse stability is demonstrated. This chapter is a reproduction from a published journal paper in the IEEE Transactions on Instrumentation and Measurement [80].

Chapter 3 proposes an ultra-high throughput UWB ET sampling dual-channel receiver which is controlled by a FPGA. The architecture employs a PDC to achieve

over 9 000 waveforms per second for a typical 1 μs repetition period. For the first time, the problem of a systematic timebase distortion due to the PDC is identified. It is shown that the PDC delay inaccuracies are the main signal-degradation factor in the high-speed ET receivers realizing picosecond sampling intervals. A simple yet effective calibration method and metrics for quantitative comparison are proposed. This chapter duplicates the journal paper manuscript submitted to the IEEE Transactions on Instrumentation and Measurement [81]. Additionally, Appendix A is a reprint of a conference paper published and presented at the IEEE European Radar Conference on the calibration procedure [82].

Chapter 4 demonstrates a parallelized FPGA architecture for realizing a compact low-cost dual-channel UWB pulsed-radar system with ultra-fast processing capabilities. This architecture resolves the main shortcoming of current FPGA-based radars, namely, the low processing throughput, which leads to significant loss of the data provided by the radar receiver. The proposed system achieves an impressive speed of over 9 000 waveforms per second per channel, demonstrating that the FPGA processing speed can match the radar output, effectively eliminating data loss. This chapter duplicates a journal paper published in MDPI Sensors [83].

Chapter 5 summarizes the achieved hardware advancements and their benefits for the future portable and mobile applications of the UWB radars. It also suggests future work towards further enhancement of the proposed UWB system and its uses in unobtrusive surveillance for concealed weapon detection and UAV borne radars.

References

[1] H. Hertz, *Electric Waves: Being Researches on the Propagation of Electric Action with Finite Velocity Through Space*, 1st. New York, NY, USA: Dover Publications, Inc., 1962.

[2] M. Z. Win, D. Dardari, A. F. Molisch, W. Wiesbeck, and J. Zhang, "History and applications in UWB," *Proceedings of the IEEE*, vol. 97, no. 2, pp. 198–204, Feb. 2009.

[3] T. Zwick, W. Wiesbeck, J. Timmermann, and G. Adamiuk, *Ultra-Wideband RF System Engineering* (EuMA High Frequency Technologies Series), 1st. Cambridge, UK: Cambridge University Press, 2013.

[4] C. Hülsmeyer, *Hertzian-wave projecting and receiving apparatus to indicate or give warning of the presence of a metallic body, such as a ship or a train, in the line of projection of such waves*, UK Patent No. 13,170, Sep. 1904.

[5] J. Ender, "98 years of the radar principle: The inventor Christian Hülsmeyer," in *Proceedings of the 4th European Conference on Synthetic Aperture Radar (EUSAR)*, Cologne, Germany, Jun. 2002, pp. 1–9.

[6] S. G. Marconi, "Radio telegraphy," *Proceedings of the Institute of Radio Engineers (IRE)*, vol. 10, no. 4, pp. 215–238, Aug. 1922.

[7] D. Parry, *NRL history - November 1930*, News Release from the U.S. Naval Research Laboratory, Nov. 2010. [Online]. Available: https://www.nrl.navy.mil/Media/News/Article/2577147/nrl-history-radar/.

[8] M. I. Skolnik, *Introduction to Radar Systems*, 3rd. New York, NY, USA: McGraw-Hill, 2001.

[9] R. M. Page, "The early history of radar," *Proceedings of the Institute of Radio Engineers (IRE)*, vol. 50, no. 5, pp. 1232–1236, Jan. 1962.

[10] R. J. James, "A history of radar," *IEE Review*, vol. 35, no. 9, pp. 343–349, Oct. 1989.

[11] M. A. Richards, *Fundamentals of Radar Signal Processing*, 2nd. New York, NY, USA: McGraw-Hill Education, 2014.

[12] J. Sachs, *Handbook of Ultra-Wideband Short-Range Sensing*, 1st. Weinheim, Germany: Wiley-VCH Verlag & Co., 2013.

[13] W. M. Brown and L. J. Porcello, "An introduction to synthetic-aperture radar," *IEEE Spectrum*, vol. 6, no. 9, pp. 52–62, Aug. 1969.

[14] S. W. Lasswell, "History of SAR at Lockheed Martin (previously Goodyear Aerospace)," *Radar Sensor Technology IX, SPIE Digital Library*, vol. 5788, pp. 1–12, May 2005.

[15] D. Atlas, *Radar in Meteorology: Battan Memorial and 40th Anniversary Radar Meteorology Conference*. Boston, MA, USA: American Meteorological Society, 1990.

[16] J. R. Klauder, A. C. Price, S. Darlington, and W. J. Albersheim, "The theory and design of chirp radars," *Bell System Technical Journal*, vol. 39, no. 4, pp. 745–808, Jul. 1960.

[17] T. W. Barrett, "History of ultrawideband (UWB) radar and communications: Pioneers and innovators," in *Progress in Progress In Electromagnetics Symposium (PIERS)*, Cambridge, MA, USA, Jul. 2000, pp. 1–42.

[18] J. D. Taylor, *Ultrawideband Radar: Applications and Design*, 1st. Boca Raton, FL, USA: CRC Press, Taylor & Francis Group, 2016.

[19] J. D. Taylor, *Advanced Ultrawideband Radar: Signals, Targets, and Applications*, 1st. Boca Raton, FL, USA: CRC Press, Taylor & Francis Group, 2017.

[20] I. I. Immoreev and D. V. Fedotov, "Ultra wideband radar systems: Advantages and disadvantages," in *2002 IEEE Conference on Ultra Wideband Systems and Technologies*, IEEE, Baltimore, MD, USA, May 2002, pp. 201–205.

[21] I. Y. Immoreev, "Ultrawideband radars: Features and capabilities," *Journal of Communications Technology and Electronics*, vol. 54, no. 1, pp. 1–26, Jan. 2009.

[22] OSD/DARPA Ultra-Wideband Radar Review Panel, "Assessment of ultra-wideband (UWB) technology," Defense Advanced Research Project Agency (DARPA), Arlington, VA, USA, Tech. Rep. R-6280, Jul. 1990. [Online]. Available: https://apps.dtic.mil/sti/citations/tr/ADB146160.

[23] "First report and order, revision of part 15 of commission's rule regarding UWB transmission system FCC 02-48," Federal Communications Commission (FCC), Washington, DC, USA, Tech. Rep. FCC 02-48, Apr. 2002.

[24] N. K. Nikolova, *Introduction to Microwave Imaging* (EuMA High Frequency Technologies Series), 1st. Cambridge, United Kingdom: Cambridge University Press, 2017.

[25] J. J. McCombe, N. K. Nikolova, M. S. Georgiev, and T. Thayaparan, "Clutter removal in the automatic detection of concealed weapons with late time responses," in *2013 European Radar Conference (EuRAD)*, IEEE, Nuremberg, Germany, Oct. 2013, pp. 53–56.

[26] AKELA, "Final report - demonstration of a concealed weapons detection system using electromagnetic resonances," *US Department of Justice*, Jan. 2001.

[27] A. Agurto, Y. Li, G. Y. Tian, N. Bowring, and S. Lockwood, "A review of concealed weapon detection and research in perspective," in *2007 IEEE International Conference on Networking, Sensing and Control*, London, UK: IEEE, Apr. 2007, pp. 443–448.

[28] A. Vasalos, "Late time response analysis in UWB radar for concealed weapon detection: Feasibility study," Ph.D. dissertation, Dept. of Electronic, Electrical & Computer Engineering, Univ. of Birmingham, Birmingham, UK, Sep. 2010.

[29] S. W. Harmer, S. E. Cole, N. J. Bowring, N. D. Rezgui, and D. Andrews, "On body concealed weapon detection using a phased antenna array," *Progress In Electromagnetics Research*, vol. 124, pp. 187–210, Jan. 2012.

[30] N. K. Nikolova and T. Thayaparan, "Ultra-wideband (UWB) high-resolution noise radar for concealed weapon detection," Defence Research and Development Canada, Tech. Rep. TR 2013-160, Feb. 2014.

[31] N. K. Nikolova and J. J. McCombe, *On-body concealed weapon detection system*, U.S. Patent No. 10,229,328, Mar. 2019.

[32] A. D. Pitcher, M. S. Georgiev, J. Nguyen, and N. K. Nikolova, "Unobtrusive inspection for on-body threats concealed under clothing: Concealed weapons detection using polarization energy ratios," Electromagnetic Vision (EMVi) Research Laboratory, McMaster University, Hamilton, ON, Canada, Tech. Rep. EMVi-R-110, Sep. 2021.

[33] Y. Yang and A. Fathy, "Near-real-time data acquisition and beamforming for UWB see-through-wall system," in *2007 IEEE Workshop on Signal Processing Applications for Public Security and Forensics*, Washington, DC, USA: IEEE, Apr. 2007, pp. 1–4.

[34] Q. Liu, Y. Wang, and A. Fathy, "Towards low cost, high speed data sampling module for multifunctional real-time UWB radar," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 49, no. 2, pp. 1301–1316, Apr. 2013.

[35] D. Yang, Z. Zhu, J. Zhang, and B. Liang, "The overview of human localization and vital sign signal measurement using handheld IR-UWB through-wall radar," *MDPI Sensors*, vol. 21, no. 402, pp. 1–31, Jan. 2021.

[36] J. Yousaf, S. Yakoub, S. Karkanawi, *et al.*, "Through-the-wall human activity recognition using radar technologies: A review," *IEEE Open Journal of Antennas and Propagation*, vol. 5, no. 6, pp. 1815–1837, Sep. 2024.

[37] D. J. Daniels, *Ground Penetrating Radar*, 2nd. London, UK: The Intitution of Engineering and Technology (IET), 2007.

[38] H. M. Jol, *Ground Penetrating Radar: Theory and Application*, 1st. Amsterdam, The Netherlands: Elsevier Science, 2009.

[39] R. Persico, *Introduction to Ground Penetrating Radar: Inverse Scattering and Data Processing*, 1st. Hoboken, NJ, USA: John Wiley & Sons, Inc., 2014.

[40] Y. López, M. García-Fernández, G. Álvarez-Narciandi, and F. Las-Heras, "Unmanned aerial vehicle-based ground-penetrating radar systems: A review," *IEEE Geosci. Remote Sens. Mag.*, vol. 10, no. 2, pp. 66–86, Apr. 2022.

[41] C. Noviello, G. Gennarelli, G. Esposito, *et al.*, "An overview on down-looking UAV-based GPR systems," *MDPI Remote Sensing*, vol. 14, no. 3245, pp. 1–28, Jul. 2022.

[42] M. García-Fernández, G. Álvarez-Narciandi, Y. López, and F. Las-Heras, "Array-based ground penetrating synthetic aperture radar on board an unmanned aerial

vehicle for enhanced buried threats detection," *IEEE Trans. Geosci. Remote Sens.*, vol. 61, pp. 1–18, May 2023.

[43] L. Tantiparimongkol and P. Phasukkit, "IR-UWB pulse generation using FPGA scheme for through obstacle human detection," *MDPI Sensors*, vol. 20, no. 3750, pp. 1–21, Jul. 2020.

[44] E. N. Paliodimos, F. G. Papadopoulos, D. Uzunidis, C. Z. Patrikakis, and S. A. Mitilineos, "A UWB radar and machine learning-based tool for detecting victims through foliage in search and rescue operations," in *2024 13th International Conference on Modern Circuits and Systems Technologies (MOCAST)*, Sofia, Bulgaria: IEEE, Jun. 2024, pp. 1–5.

[45] Y. Xianjia, L. Qingqing, J. P. Queralta, J. Heikkonen, and T. Westerlund, "Applications of UWB networks and positioning to autonomous robots and industrial systems," in *2021 10th Mediterranean Conference on Embedded Computing (MECO)*, Budva, Montenegro: IEEE, Jun. 2021, pp. 1–6.

[46] R. Wang, L. Chen, Z. Huang, W. Zhang, and S. Wu, "A review on the high-efficiency detection and precision positioning technology application of agricultural robots," *MDPI Processes*, vol. 12, no. 1833, pp. 1–34, Aug. 2024.

[47] *Airtag - apple (ca): Airtag tech specs*, Apple (Canada). [Online]. Available: https://www.apple.com/ca/airtag/.

[48] A. R. Jiménez and F. Seco, "Finding objects using UWB or BLE localization technology: A museum-like use case," in *2017 International Conference on Indoor Positioning and Indoor Navigation (IPIN)*, IEEE, Sapporo, Japan, Sep. 2017, pp. 1–8.

[49] M. Elsanhoury, P. Mäkelä, J. Koljonen, *et al.*, "Precision positioning for smart logistics using ultra-wideband technology-based indoor navigation: A review," *IEEE Access*, vol. 10, pp. 44 413–44 445, Apr. 2022.

[50] W. Wiesbeck, *Lecture script: Radar systems engineering*, Institut für Hochfrequenztechnik und Elektronik, Karlsruhe Institute of Technology, 2009. [Online]. Available: https://www.ihe.kit.edu/download/RSE_script__2009.pdf.

[51] W. Wiesbeck, *Radar history (Rad 01.1)*, Lecture Notes from Radar 2020 - Future Radar Systems, European School of Antennas (ESoA), Apr. 2018.

[52] R. Sadli, "Study and development of a road collision avoidance system based on ultra wide-band radar for obstacles detection and identification dedicated to vulnerable road users," Ph.D. dissertation, Doctoral School of Engineering Science, Polytechnique Hauts-de-France Univ., Valenciesnnes, France, Mar. 2019.

[53] C. Waldschmidt, J. Hasch, and W. Menzel, "Automotive radar - from first efforts to future systems," *IEEE Journal of Microwaves*, vol. 1, no. 1, pp. 135–148, Jan. 2021.

[54] C. D. Simpson, S. Kolpuke, A. K. Awasthi, *et al.*, "Development of a UAS-based ultra-wideband radar for fine-resolution soil moisture measurements," in *2021 IEEE Radar Conference (RadarConf21)*, Atlanta, GA, USA, May 2021, pp. 1–4.

[55] K. Muzalevskiy, S. Fomin, and M. Mikhaylov, "UWB reflectometric method for the measuring of vegetation biometric parameters and soil moisture," in *2023 IEEE Ural-Siberian Conference on Biomedical Engineering, Radioelectronics and Information Technology (USBEREIT)*, Yekaterinburg, Russian Federation, May 2023, pp. 166–169.

[56] D. Gomez-Garcia, F. Rodriguez-Morales, S. Welch, and C. Leuschen, "High-throughput phenotyping of wheat canopy height using ultrawideband radar: First results," *IEEE Geoscience and Remote Sensing Letters*, vol. 19, pp. 1–5, Dec. 2022.

[57] A. A. Pramudita, Y. Wahyu, S. Rizal, *et al.*, "Soil water content estimation with the presence of vegetation using ultra wideband radar-drone," *IEEE Access*, vol. 10, pp. 85 213–85 227, Aug. 2022.

[58] E. C. Fear, J. Bourqui, C. Curtis, D. Mew, B. Docktor, and C. Romano, "Microwave breast imaging with a monostatic radar-based system: A study of application to patients," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 5, pp. 2119–2128, May 2013.

[59] N. K. Nikolova, "Microwave biomedical imaging," *Wiley Encyclopedia of Electrical and Electronics Engineering*, pp. 1–22, Apr. 2014.

[60] M. Pastorino, *Microwave Imaging*, 1st. Hoboken, NJ, USA: John Wiley & Sons, Inc., 2010.

[61] A. Kandwal, L. W. Liu, M. J. Deen, R. Jasrotia, B. K. Kanaujia, and Z. Nie, "Electromagnetic wave sensors for noninvasive blood glucose monitoring: Review and recent developments," *IEEE Trans. Instrum. Meas.*, vol. 72, pp. 1–15, Oct. 2023.

[62] Q. Li, J. Liu, R. Gravina, W. Zang, Y. Li, and G. Fortino, "A UWB radar-based adaptive method for in-home monitoring of elderly," *IEEE Internet of Things Journal*, vol. 11, no. 4, Feb. 2024.

[63] M. Cheraghinia, A. Shahid, S. Luchie, *et al.*, "A comprehensive overview on UWB radar: Applications, standards, signal processing techniques, datasets,

radio chips, trends and future research directions," *IEEE Communications Surveys & Tutorials*, pp. 1–42, Oct. 2024, early access.

[64] D. Oloumi, A. Bevilacqua, and M. Bassi, "UWB radar for high resolution breast cancer scanning: System, architectures, and challenges," in *2019 IEEE International Conference on Microwaves, Antennas, Communications and Electronic Systems (COMCAS)*, Tel-Aviv, Israel: IEEE, Nov. 2019, pp. 1–4.

[65] Z. Fang, W. Wang, J. Wang, *et al.*, "Integrated wideband chip-scale RF transceivers for radar sensing and UWB communications: A survey," *IEEE Circuits Syst. Mag.*, vol. 22, no. 1, pp. 40–76, Feb. 2022.

[66] "PicoScope 9400 series: Sampler-extended real-time oscilloscopes," Pico Technology Ltd., User's Guide ps9400ug-7, 2024.

[67] "FemtoScope 1000/2000/3000 series: 5 GHz and 16 GHz USB wide-bandwidth oscilloscope," Eltesta, Datasheet v1.2, 2020.

[68] H. G. Han, B. G. Yu, and T. W. Kim, "A 1.9-mm-precision 20-GHz direct-sampling receiver using time-extension method for indoor localization," *IEEE J. Solid-State Circuits*, vol. 52, no. 6, pp. 1509–1520, Jun. 2017.

[69] R. Feghhi, R. Winter, F. Sabzevari, and K. Rambabu, "Design of a low-cost UWB time-domain radar system for subcentimeter image resolution," *IEEE Trans. Microw. Theory Techn.*, vol. 70, no. 7, pp. 3617–3628, Jul. 2022.

[70] Y. Masui, A. Toya, M. Sugawara, *et al.*, "Differential equivalent time sampling receiver for breast cancer detection," in *2017 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, Turin, Italy: IEEE, Oct. 2017, pp. 1–4.

[71] Y. Yang and A. Fathy, "Development and implementation of a real-time see-through-wall radar system based on FPGA," *IEEE Trans. Geosci. Remote Sens.*, vol. 47, no. 5, pp. 1270–1280, May 2009.

[72] C. Chen, S. Wu, S. Meng, J. Chen, G. Fang, and H. Yin, "Application of equivalent-time sampling combined with real-time sampling in UWB through-wall imaging radar," in *2011 International Conference on Instrumentation, Measurement, Computer, Communication and Control*, Beijing, China: IEEE, Oct. 2011, pp. 721–724.

[73] Q. Liu, Y. Wang, and A. Fathy, "A compact integrated 100 GS/s sampling module for UWB see through wall radar with fast refresh rate for dynamic real time imaging," in *2012 IEEE Radio and Wireless Symposium*, Santa Clara, CA, USA: IEEE, Jan. 2012, pp. 59–62.

[74] A. D. Pitcher, "Compact low-cost ultra-wideband pulsed-radar system," M.A.Sc. thesis, Department of Electrical and Computer Engineering, McMaster University, Hamilton, ON, Canada, Aug. 2019.

[75] M. Saad, A. Maali, M. S. Azzaz, A. Bouaraba, and M. Benssalah, "Development of an IR-UWB radar system for high-resolution through-wall imaging," *Progress in Electromagnetic Research (PIER) C*, vol. 124, pp. 81–96, Sep. 2022.

[76] M. Saad, A. Maali, M. S. Azzaz, and M. Benssalah, "An efficient FPGA-based implementation of UWB radar system for through-wall imaging," *International Journal of Communication Systems*, e5510, May 2023.

[77] A. D. Pitcher, C. W. Baard, M. Georgiev, and N. K. Nikolova, "Equivalent-time sampling ultra-wideband pulsed-radar receiver: RF front-end design," Electromagnetic Vision (EMVi) Research Laboratory, McMaster University, Hamilton, ON, Canada, Tech. Rep. EMVi-R-122, Sep. 2024.

[78] A. Srivastav, D. Ariando, and S. Mandal, "An FPGA-based flexible and MIMO-capable GPR system," in *2018 17th International Conference on Ground Penetrating Radar (GPR)*, Rapperswil, Switzerland: IEEE, Jun. 2018, pp. 1–6.

[79] T. Pardhu, V. Kumar, P. Kumar, and N. Deevi, "Advancements in UWB based human motion detection through wall: A comprehensive analysis," *IEEE Access*, vol. 12, May 2024.

[80] A. D. Pitcher, C. W. Baard, and N. K. Nikolova, "Design and performance analysis of a picosecond pulse generator," *IEEE Trans. Instrum. Meas.*, vol. 71, pp. 1–14, Aug. 2022.

[81] A. D. Pitcher, C. W. Baard, M. Georgiev, and N. K. Nikolova, "Accurate high-speed equivalent-time sampling receiver: Architecture and performance metrics," *IEEE Trans. Instrum. Meas.*, pp. 1–15, Mar. 2025.

[82] A. D. Pitcher, M. Georgiev, and N. K. Nikolova, "Correcting timebase errors in ultra-wideband equivalent-time sampling receivers," in *2024 21st European Radar Conference (EuRAD)*, Paris, France: IEEE, Nov. 2024, pp. 47–50.

[83] A. D. Pitcher, M. Georgiev, N. K. Nikolova, and N. Nicolici, "Parallelized field-programmable gate array data processing for high-throughput pulsed-radar systems," *MDPI Sensors*, vol. 25, no. 239, pp. 1–25, Jan. 2025.

CHAPTER 2:

DESIGN AND PERFORMANCE ANALYSIS OF A PICOSECOND PULSE GENERATOR

Preface

This chapter is a reproduction of the following published article:

A. D. Pitcher, C. W. Baard, and N. K. Nikolova, "Design and performance analysis of a picosecond pulse generator," *IEEE Transactions on Instrumentation and Measurement*, vol. 71, pp. 1–14, Aug. 2022. DOI: 10.1109/TIM.2022.3195265.

I led the development, design, and validation of the proposed picosecond pulse generator, established the experimental framework and measurement methodology, investigated and formalized the results, created the visualizations, and authored and edited the manuscript. Charl W. Baard contributed to the prototype development, manufacturing of the printed circuit boards, and manuscript review. Natalia K. Nikolova supervised the project, supported design reviews and testing, and assisted with manuscript editing.

2.1 Introduction

Ultra-wideband (UWB) technology is growing at an unprecedented rate due to the development of new sensing and imaging systems. These systems operate in various frequency bands from 100 MHz to 10.6 GHz designated by the Federal Communications Commission (FCC) [1] and other spectrum management bodies [2], [3]. Applications in ground penetrating radar (GPR) and non-destructive testing (NDT) [4]–[6], security and surveillance [6]–[8], and microwave imaging [9]–[11] favour this technology due to its harmless non-ionizing radiation and low-power emissions spread over wide bandwidths. The broad bandwidth provides many advantages over traditional narrowband systems such as frequency diversity, spread spectrum, improved spatial resolution, penetration depth, and relatively high peak power [12]. The generation of a clean and stable pulse that accurately represents the desired waveform continues to be a major challenge in designing these UWB systems.

A common approach to the generation of an UWB signal is to use a train of Gaussian-like (and higher-order Gaussian derivative) waveforms produced by analog discrete circuits [6]–[8], [13]–[21] or complementary metal-oxide-semiconductor (CMOS) integrated circuits (ICs) [22]–[24]. The design requirements involve pulse shaping characteristics such as full-width half maximum (FWHM) pulse width, frequency range and bandwidth, peak-to-peak voltage, peak power, and late-time ringing. The CMOS designs provide low power consumption and a single-chip compact form factor but are limited by low output power and relatively narrow bandwidths [17]. The discrete analog designs perform pulse manipulation on an input rectangular or sinusoidal trigger to achieve the desired broadband waveform. They use a combination of avalanche transistors, tunnel diodes, step recovery diodes (SRDs), and linear or

nonlinear transmission lines (NLTLs) [12]. They can provide large peak-to-peak voltages and picosecond pulse widths, but they occupy large surface areas and consume significantly more power. The most common design for Gaussian pulse generation uses SRDs, which provides a compromise between the large breakdown voltage and slow switching of the avalanche transistor, and the small breakdown voltage and fast switching of the tunnel diode.

Here, we propose an SRD-based picosecond UWB pulse generator that produces a differentiated Gaussian (monocycle) waveform with a 1:10 fractional bandwidth (FBW) ratio within the low-GHz spectrum. It incorporates a jitter cleaner to remove jitter due to the input trigger. The design builds upon circuits reported in [7], [8], [13]–[15]. Critical design steps are discussed, which enable significant bandwidth increase without compromising the peak output power and the peak-to-peak voltage. Strategies are also discussed to tune the pulse bandwidth and shape along with the respective limitations.

In addition to the new pulse-generator design, this work offers two main contributions. First, a systematic investigation is carried out regarding the limitations of the design concerning FBW, the upper and lower frequency limits, FWHM pulse width, the peak-to-peak voltage, and the late-time ringing. Second, a rigorous methodology is developed for the noise and jitter analysis of a UWB pulse generator, which is applied to evaluate the proposed design. Both investigations are based on a statistical evaluation of the generator's performance using thousands of captured waveforms. The proposed methodology for evaluating the jitter and noise performance of the UWB generator exploits definitions from high-speed digital electronics, originally developed for periodic signals in digital clocks and data buses [25]–[27]. We discuss the challenges associated with adapting these definitions and the respective measurement strategies to the case of UWB generators at microwave frequencies.

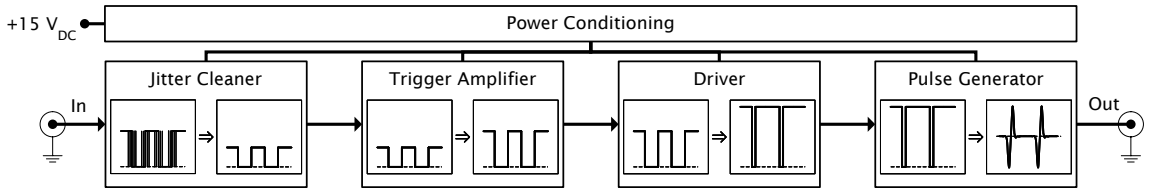


Figure 2.1: Block diagram of the picosecond pulse generator.

This paper is organized as follows. In Section 2.2, we describe the proposed pulse generator design along with the key tuning strategies. The UWB pulse performance metrics are introduced in Section 2.3 along with the respective performance analysis of the proposed generator. We formulate the jitter and noise performance metrics in Section 2.4 and apply them to evaluate the jitter and noise performance of the generator. The results are discussed in Section 2.5 followed by conclusions in Section 2.6.

2.2 Picosecond Pulse Generator Design

The proposed design is based on circuits reported in [7], [8], [13]–[15]. The principles of operation are briefly described, followed by a discussion of the critical design steps toward larger bandwidth and peak-to-peak voltage along with the key tuning parameters.

2.2.1 Design Principles

As shown in Fig. 2.1, the picosecond pulse generator consists of five major sections: (i) jitter cleaner, (ii) trigger amplifier, (iii) driver circuit, (iv) pulse generator circuit, and (v) power conditioning circuit. Fig. 2.2 to Fig. 2.5 show the circuit schematics of the generator's sections. The respective component values are listed in Table 2.1.

Table 2.1: Pulse generator components.

Component	Type	Value	Part
R1-3, R5*	Discrete	49.9 Ω	–
R4	Discrete	10 Ω	–
R6†	Discrete	205 Ω	–
R7†	Discrete	33 Ω	–
R8, R9	Discrete	100 Ω	–
R10	Potentiometer	0 – 1 kΩ	3313J-1-102E [28]
R11	Potentiometer	0 – 20 kΩ	3313J-1-203E [28]
R12	Discrete	1 kΩ	–
R13	Discrete	150 Ω	–
R14	Potentiometer	0 – 20 Ω	3313J-1-200E [28]
R15	Discrete	2 Ω	–
R16‡	Discrete	49.9 kΩ	–
C1	Discrete	10 nF	–
C2	Discrete	100 nF	–
C3	Discrete	47 pF	–
C4	Discrete	10 pF	–
C5	Discrete	1 nF	–
C6§	Discrete	5.1 pF	–
Q1, Q2	Transistor	–	BFP196W [29]
SD1, SD2	Discrete	–	BAT15-03W [30]
SRD	Discrete	–	MMD830-0805-2 [31]

* The closest E96 standard resistor value to 50 Ω, which is needed for impedance matching.
† Following [32], R6 and R7 are chosen based on the closest E96 standard resistor to achieve the closed-loop gain of 7.6.
‡ The closest E96 resistor chosen based on recommendations in [33].
§ E24 standard capacitance value.

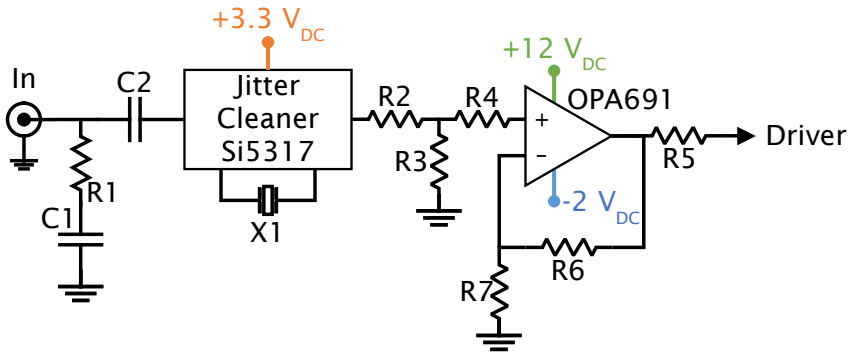


Figure 2.2: Jitter cleaner and trigger amplifier circuit schematic.

2.2.1.1 Jitter Cleaner

The performance and stability of the pulse generator are dependent on the input trigger. The jitter cleaner is critically important to the pulse stability in terms of the pulse repetition interval (PRI), or inversely, the pulse repetition frequency (PRF). This circuit is shown in Fig. 2.2 along with the trigger amplifier. The employed jitter cleaner [34] performs jitter attenuation for any transistor-transistor logic (TTL) square-wave input trigger (0 V low, 5 V high) to produce a stable trigger source. Ultra-low root-mean-square (RMS) output jitter values are expected in the range of 300 fs to 400 fs [34]. The IC incorporates a dual-loop phase-locked loop (PLL) which integrates digital signal processing (DSP) circuitry and an ultra-low phase noise voltage controlled oscillator (VCO) [35]. The IC is pin-controlled to set the PRF and PLL bandwidth to phase-lock onto a 1 MHz to 20 MHz signal. R1 and C1 are chosen to present the input as a 50 Ω load. C2 is an input direct current (DC) block. X1 is a high-quality 114.285 MHz crystal clock.

2.2.1.2 Trigger Amplifier

The trigger amplifier translates the output square wave from the jitter cleaner back to the 5 V TTL-level signal. The operational amplifier [32] is DC coupled and designed for a 50 Ω source and 50 Ω load. The non-inverting closed-loop gain is set to 7.6 to yield the correct voltage at the input of the driver circuit. It is important to select a wideband operational amplifier with a sufficient slew rate (SR) to meet the output voltage swing and frequency demands. A minimum SR of 628.3 V/μs is required for a 5 V, 20 MHz square-wave signal.[1]

2.2.1.3 Driver Circuit

The driver circuit (Fig. 2.3) accepts the square-wave trigger from the jitter cleaner and the operational amplifier circuit. The inverter [36] inverts the input ensuring constant rise and fall times. The subsequent circuit amplifies the trigger pulse while reducing its duty cycle and increasing the falling-edge's slope. The RC integrator (R11 and C4) is responsible for delaying the switching of Q2 with respect to Q1, which reduces the trigger's duty cycle. The delay is controlled by the integrator's time constant as determined by R11 and C4. As described in [14], R13 limits the bias current of Q1, which is switched off (non-conducting) in the absence of a trigger pulse. The trigger leads to the discharge of C3, thus accelerating the switching of Q1 to an on-state (conducting). At this instant, Q2 is still in an off state until the trigger passes through the RC integrator. At this point, Q2 is switched on, whereas the base of Q1 is shorted to ground, thus switching Q1 off. As the trigger falls to 0 V, Q1 and Q2 return to their original off states until the next trigger arrives. R10 and R12 limit the output current from the inverter to the base of Q1 and Q2. C5 is an output DC

[1] A slew rate (SR) was chosen using SR $\geq 2\pi fV/10^6$ [V/μs] where f is the desired PRF in Hz and V is the desired voltage swing in volts.

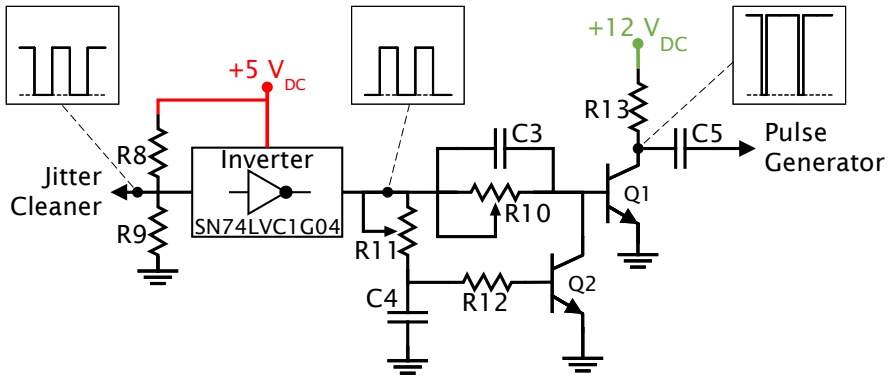


Figure 2.3: Driver circuit schematic.

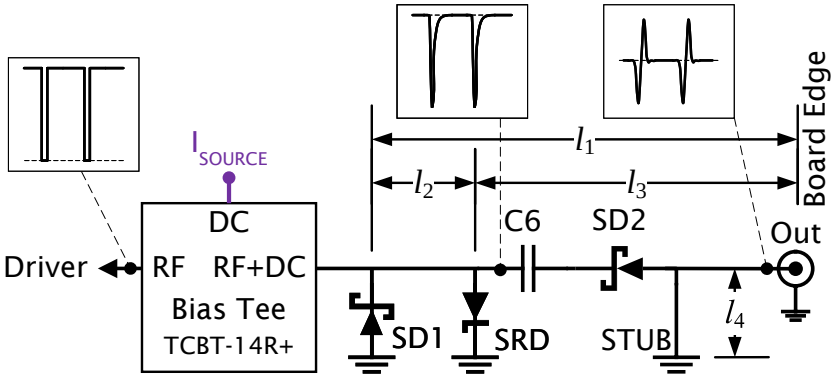


Figure 2.4: Pulse generator circuit schematic.

block.

2.2.1.4 Pulse-Generator Circuit

The pulse-generator circuit produces the monocycle pulse from the reduced-duty-cycle trigger at the output of the driver circuit. It is shown in Fig. 2.4. The circuit consists of two pulse forming networks: (i) SRD-based falling edge sharpener, and (ii) monocycle forming network [14].

The SRD-based falling edge sharpener consists of a bias tee [37] for the Schottky

diode (SD), SD1, and for the SRD. C6 is a DC blocking capacitor needed to forward-bias the SRD (low impedance) and reverse-bias the SD1 (high impedance). The role of the falling edge sharpener is to further reduce the duty cycle by using the SRD as a charge-controlled rapid switch [38]. The SRD is forward-biased so that the trigger switches the diode from forward conduction to reverse cut-off. As the stored charge within the SRD is removed, the diode remains open for a brief moment before it snaps off. The SRD briefly produces a reverse current at the moment of switching as the stored charge dissipates, producing the Gaussian-like pulse. This pulse then propagates in both directions down the co-planar waveguide (CPW) transmission line. As the waveform travels back toward the driver circuit, SD1 switches from reverse bias to forward bias presenting a short circuit. This wave is then inverted and reflected back toward the output SD, SD2. This second SD traps subsequent internal reflections while allowing through only the initial Gaussian-like pulse produced by the SRD. The delay line of length l_2, which lies between SD1 and SRD, plays a crucial role in further sharpening the Gaussian pulse [8]. The distances l_1 and l_3 indicate the SD1 and SRD diode positions in the prototypes, and their difference is the respective l_2 length.

The Gaussian pulse is then submitted to the monocycle forming network, i.e., to the junction with the shorted stub (STUB in Fig. 2.4). Here, it splits so that one part passes onto the output directly, whereas the other part enters the shorted stub and forms an inverted time-delayed version of the original Gaussian pulse. The direct and reflected portions superimpose to form the monocycle waveform.

2.2.1.5 Power Conditioning Circuit

The power conditioning circuit is presented as a block diagram in Fig. 2.5. It is designed to supply the necessary DC voltage rails (+12, +5, +3.3 and −2 V_{DC}) and one current source to the generator's components. The circuit utilizes DC/DC

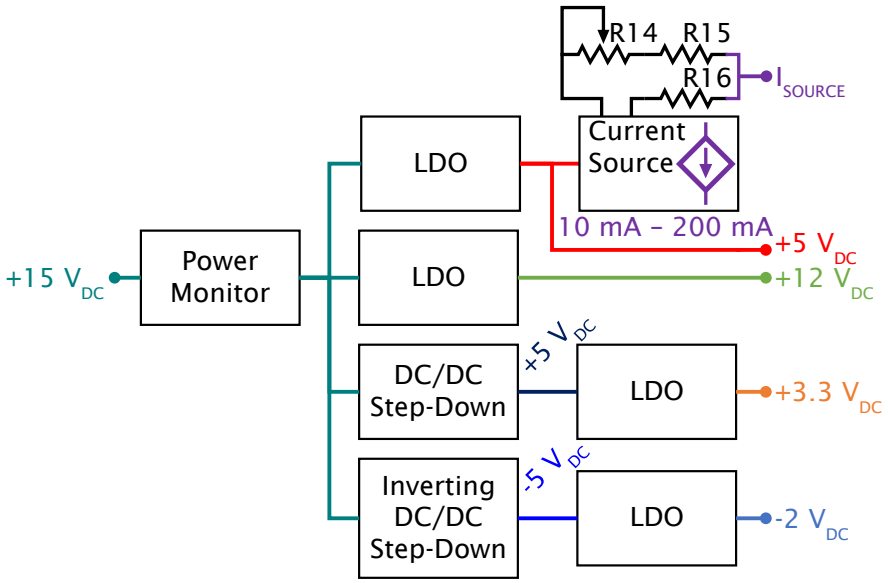


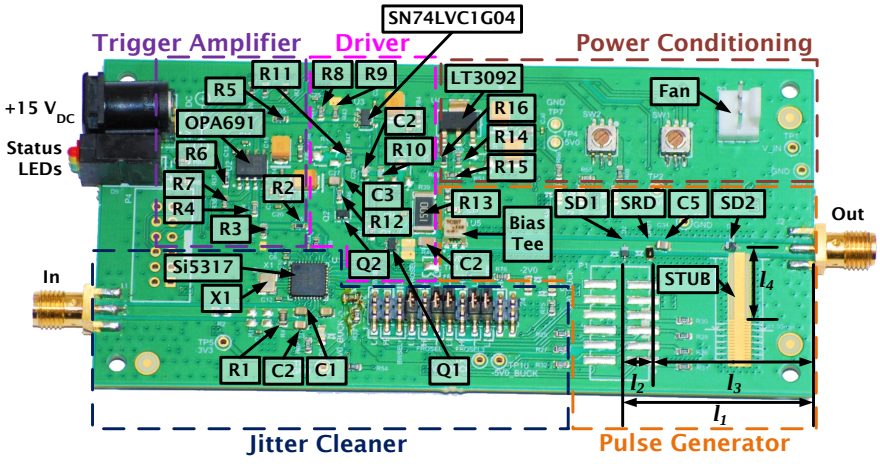
Figure 2.5: Power conditioning block diagram. LDO stand for low-dropout linear regulator.

converters [39], [40] to reduce power dissipation along with low-noise low-dropouts (LDOs) linear regulators [41], [42] to regulate the +15 V_{DC} input supply. Low-noise LDOs are chosen to reduce the supply noise on the microwave circuitry. A power monitoring IC [43] is added to measure the power consumption.

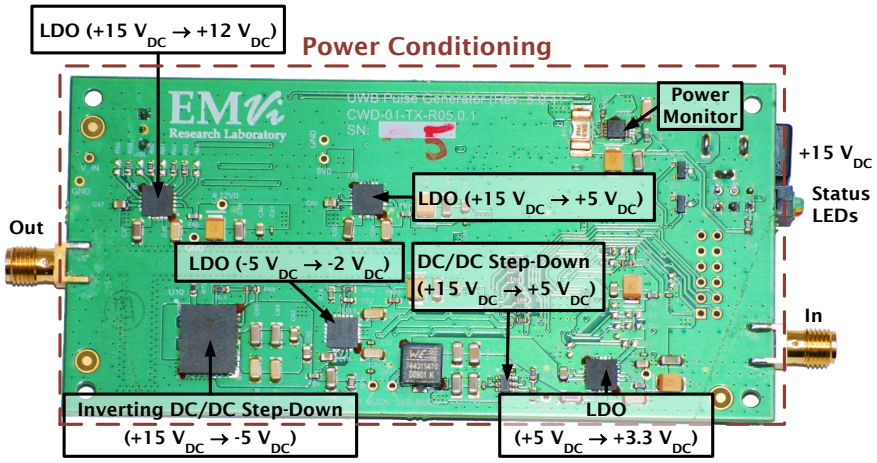
The 200 mA programmable current source [33] supplies the current, I_{SOURCE}, to the pulse-generator circuit. The current supply value is a critical tuning parameter (discussed later), and this tuning is achieved with the R14 potentiometer.

2.2.2 Fabricated Prototype

The picosecond pulse generator is fabricated on a four-layer, 1.622 mm (63.9 mil) thick printed circuit board (PCB). Annotated photos of the PCB top and bottom are shown in Fig. 2.6. The PCB stackup (shown in Fig. 2.7) contains a 0.813 mm (32.0 mil) thick high-frequency RO4003C [44] substrate core stacked on two layers of FR-4



(a)



(b)

Figure 2.6: Manufactured PCB board: (a) top and (b) bottom.

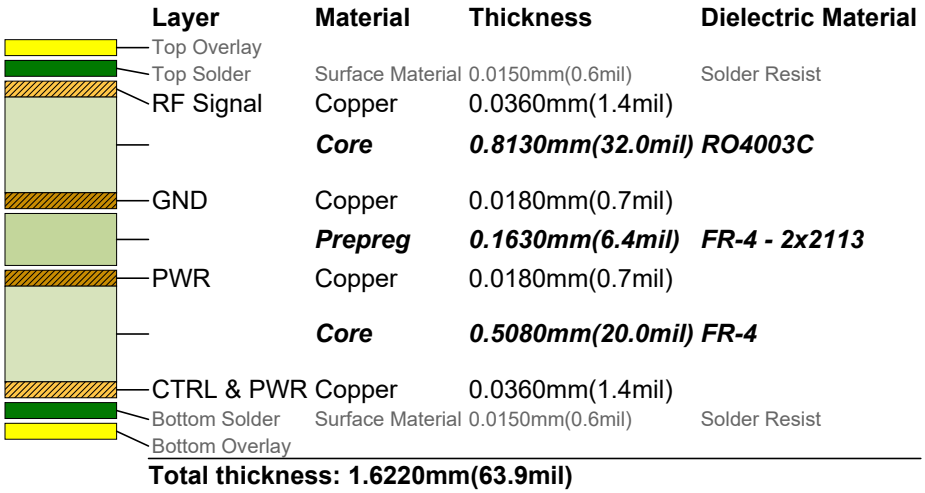


Figure 2.7: PCB stackup.

pre-preg and cores. The high-frequency substrate contains all radio frequency (RF) signal paths backed by a ground plane since it has a low dielectric loss, unlike FR-4. The FR-4 layers supply the RF components with power and control paths. CPW transmission lines (of 50 Ω characteristic impedance) are used because they allow for easy shunt-element mounting and the tuning of the shorted stub.

2.2.3 Design Tuning and Critical Components

The critical components that lead to significant improvement over the previously reported designs [7], [8], [13]–[15] with the realization of the 1:10 FBW ratio are: (i) high-quality UWB on-chip bias tee, (ii) fast-switching wideband negative-positive-negative (NPN) transistors, (iii) optimizing the length l_2 between SD1 and SRD, (iv) optimizing the length l_4 of the stub, and (v) tuning of the current source supply. The significance of these components is discussed next, along with the tuning strategies.

2.2.3.1 On-chip Bias Tee

In [7], [13]–[15], the bias tee to the pulse-generator circuits uses discrete components. Through [8] and this work, it has been found that despite careful component selection, a bias tee based on discrete components adversely affects the UWB performance of the generator due to insufficient decoupling between the RF and DC signal paths. A commercially available on-chip bias tee [37] has been selected as a replacement, and it has been found to provide lower insertion loss and higher port isolation in the desired bandwidth, and well beyond 5 GHz [8].

2.2.3.2 Choice of RF Transistors

The choice of RF transistors for the driver circuit (Q1 and Q2) is also critical. To ensure that the transition of the square wave is sharp, the transition frequency of the transistor must be greater than that of the maximum frequency expected in the picosecond pulse spectrum. Here, this frequency is 5 GHz. In addition, the collector-emitter voltage ratings must meet the 12 V_{DC} supply. A suitable component is the RF NPN bipolar junction transistor (BJT) [29], which is used in the fabricated prototypes. R13 limits its collector current (see Fig. 2.3), and its resistance is based on the maximum collector current for the device. Note that R13 must be sized to handle the power dissipation. The resistors R10 and R11 have been tuned by hand, and their optimal setting is shown in Table 2.2. The driver is also tuned to achieve the shortest duty cycle with a square waveform shape extending from 0 V to 12 V.

2.2.3.3 Length between SD1 and SRD

The placement of SD1 and SRD in relation to each other plays a critical role in the FWHM pulse width of the Gaussian pulse. Several prototypes have been developed

Table 2.2: Discrete component replacements for potentiometers based on measured resistance of tuned generator.

Component	Type	Value	Part
R10	Discrete	249 Ω	–
R11	Discrete	15 kΩ	–
R14	Discrete	12 Ω	–

[8] with values of the length l_2 from 4 mm to 10 mm in 2 mm increments. The position of the SRD is kept constant while SD1 is shifted. As l_2 decreases, the temporal pulse width also decreases. Thus, the best performance is achieved at 4 mm [8]. Distances below 4 mm have not been investigated because the physical mounting of the diodes becomes problematic.

2.2.3.4 Stub Length

The tuning of the stub length impacts the higher frequency components of the picosecond pulse. Its tuning results in an impressive increase in the upper-frequency limit within the 3 GHz to 5 GHz with little to no trade-offs at the lower frequency end. In [14], the stub is viewed as a series capacitance in an RC differentiator, where the resistance is the 50 Ω output load. However, this model is valid for a relatively narrow frequency band. In our case, with a FBW ratio on the order of 1:10, the stub can be better represented by a transmission-line model. At the stub junction, about half the incident pulse proceeds directly toward the output port, whereas the other half travels down the stub's shorted end. The shorted end reverses the pulse polarity upon reflection. The pulse in the stub travels two times its length l_4, resulting in a time delay with respect to the incident pulse. The waveform is a superposition of the direct pulse and the inverse-polarity reflected pulse at the output port. The delay introduced by the stub depends on l_4 and the phase velocity of the CPW forming

the stub. Therefore, the optimal time delay corresponds to half of the incident pulse width. The incident pulse peak must align at the junction with the beginning of the inverse-polarity reflected pulse to create the sharpest transition between the two pulse peaks without loss in peak voltage.

2.2.3.5 Tuning of the Current Source Supply

The current supply ensures that the SRD is forward biased in the absence of the trigger. The trigger introduces a short-time reversed bias, which leads to the diode producing the Gaussian pulse. In [14], a 30 mA current supply is suggested, but no justification is provided. Here, we demonstrate that the current-supply value is critically important for the pulse bandwidth and must be tuned according to the desired specifications. Our prototypes include the R14 resistance (see Fig. 2.5), which is varied for values between 0 Ω and 21 Ω. This resistance maps into current values from 10 mA to 200 mA through

$$I_{\text{SOURCE}} = 10\mu\text{A} \cdot \frac{\text{R16}}{\text{R14} + \text{R15}} + 10\mu\text{A} \tag{2.1}$$

where R16 = 49.9 kΩ and R15 = 2 Ω. It is found that a minimum resistance of R14 = 8.5 Ω is required to see substantial improvement at higher frequencies with minimal change at lower frequencies. This resistance maps into a 47.5 mA current-source supply. The impact of the respective parameter tuning is illustrated in Section 2.3 in terms of the pulse performance metrics defined.

2.3 Pulse Performance Metrics of the UWB Generator

2.3.1 Definitions of Pulse Metrics

The signal measured by the high-speed sampling oscilloscope [45] in the temporal domain is denoted as $x[n]$. Assuming $x[n]$ is sufficiently densely sampled to represent the real analog signal, $x(t)$, a complex analytical signal can be approximated through the Hilbert transform[2][46]. The analytical signal [46]–[48], $\hat{x}(t)$, is defined as

$$\hat{x}(t) = x(t) + j\mathcal{H}\{x(t)\} \tag{2.2}$$

where the analytical Hilbert envelope,

$$|\hat{x}(t)| = \sqrt{x(t)^2 + \mathcal{H}\{x(t)\}^2} \tag{2.3}$$

estimates accurately the envelope of $x(t)$. Both $x(t)$ and $|\hat{x}(t)|$ are used to evaluate the picosecond pulse generator. Here, the *hilbert* MATLAB function [49] is used.

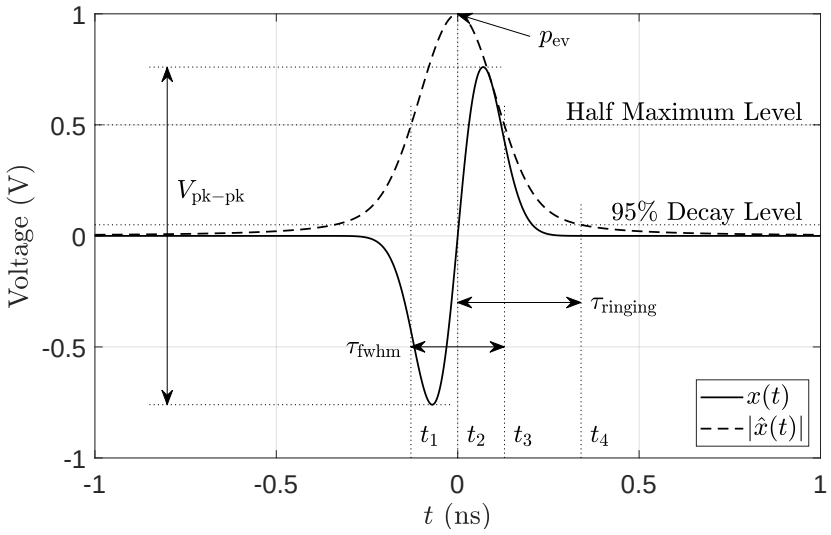
Fig. 2.8 illustrates the following pulse metrics.

2.3.1.1 Peak-to-Peak Voltage

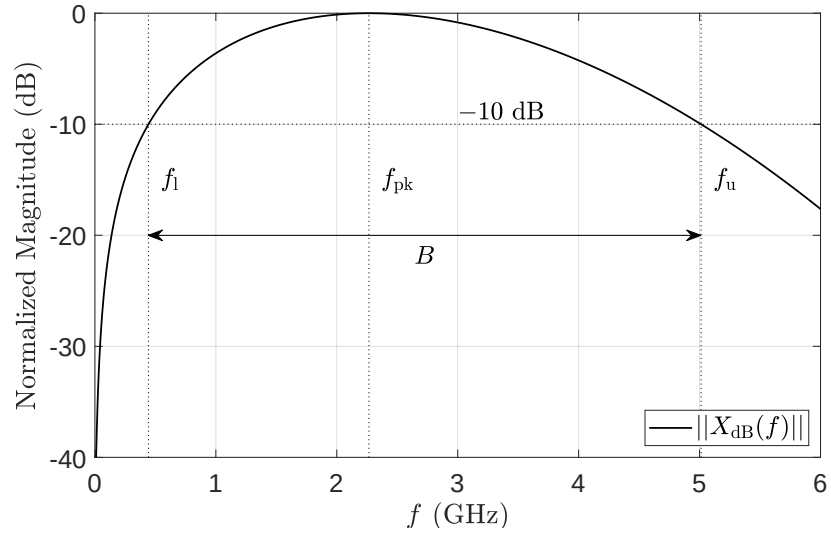
The peak-to-peak voltage is a measure of the pulse strength:

$$V_{\text{pk-pk}} = \left|\max\{x(t)\} - \min\{x(t)\}\right|. \tag{2.4}$$

[2]The Hilbert transform $\mathcal{H}\{\cdot\}$ of a time-domain signal $x(t)$ is $\mathcal{H}\{x(t)\} = x(t) * 1/\pi t$ where $*$ is convolution, whereas, in the Fourier domain, $\mathcal{H}\{X(f)\} = -j\text{sgn}(f)X(f)$, where $\text{sgn}(f)$ is the signum function [47].



(a)



(b)

Figure 2.8: Pulse metrics: (a) temporal domain and (b) spectral domain.

2.3.1.2 Full-Width Half Maximum (FWHM)

The FWHM is defined by the width at half maximum of the analytical Hilbert envelope $|\hat{x}(t)|$ [48]. It is a measure of the temporal impulse width but also relates to the spectral bandwidth. The peak (or maximum) of the analytical envelope is defined as $p_{\text{ev}} = \max\{|\hat{x}(t)|\}$ whereas the FWHM is

$$\tau_{\text{FWHM}} = t_3\big|_{|\hat{x}(t_3)|=p_{\text{ev}}/2} - t_1\big|_{|\hat{x}(t_1)|=p_{\text{ev}}/2}\,. \tag{2.5}$$

2.3.1.3 Late-Time Ringing

Ringing within a pulse waveform is undesirable. It is a result of component resonances and multiple reflections in interconnects [48]. The duration of the ringing, τ_{ringing}, is defined as the time required for the Hilbert envelope peak to decay below a given level α:

$$\tau_{\text{ringing}} = t_4\big|_{|\hat{x}(t_4)|=\alpha p_{\text{ev}}} - t_2\big|_{|\hat{x}(t_2)|=p_{\text{ev}}} \tag{2.6}$$

where $0 \leq \alpha \leq 1$. We use $\alpha = 0.05$ corresponding to a 95% decay level. It is desirable to shorten the ringing time to ensure that most of the energy is contained within the main pulse.

2.3.1.4 10 dB Bandwidth

The 10 dB bandwidth, B, is defined through the spectral magnitude $|X(f)|$, where $X(f)$ is the fast Fourier transform (FFT) of the measured signal $x(t)$. Note that $x(t)$ is passed through a Hamming window prior to the FFT. The normalized spectral magnitude in the logarithmic scale is

$$||X_{\text{dB}}(f)|| = 20\log_{10}(|X(f)|) - \max\{20\log_{10}(|X(f)|)\}. \tag{2.7}$$

The 10 dB Bandwidth is then defined as

$$B = f_{\mathrm{u}} - f_{\mathrm{l}} \text{ s.t. } ||X_{\mathrm{dB}}(f|_{f_{\mathrm{l}} \leq f \leq f_{\mathrm{u}}})|| \geq -10 \text{ dB} \tag{2.8}$$

where f_{l} and f_{u} define the lower and upper frequency bounds.

The bandwidth computed with (2.8) is also confirmed using the power spectrum density (PSD) estimation based on *Welch's* method [50]. The *pwelch* MATLAB function [51] is used to return the PSD estimate of $x(t)$. The function divides $x(t)$ into the longest possible segments to obtain 8 segments with 50 % overlap. A Hamming window is also applied to each segment.

2.3.1.5 Fractional Bandwidth (FBW)

The FBW, b_{f}, is a common figure of merit for UWB devices defined as the ratio of the absolute bandwidth B and the center frequency f_{c}:

$$b_{\mathrm{f}} = \frac{B}{f_{\mathrm{c}}} = 2\left(\frac{f_{\mathrm{u}} - f_{\mathrm{l}}}{f_{\mathrm{u}} + f_{\mathrm{l}}}\right) = 2\left(\frac{b_{\mathrm{fr}} - 1}{b_{\mathrm{fr}} + 1}\right) , \tag{2.9}$$

where $b_{\mathrm{fr}} = f_{\mathrm{u}}/f_{\mathrm{l}}$ is the FBW ratio.

2.3.2 Measurement Procedures

The measurement setup used for the generator evaluation is shown in Fig. 2.9. A 10 MHz rubidium standard [52] is used as a frequency standard for the 50 giga-samples per second (GSa/s) real-time sampling oscilloscope [45], which has a 50 Ω input and a built-in analog front-end filter with 16 GHz bandwidth. The rubidium standard is an accurate frequency reference for the oscilloscope's internal sampling logic. A 10-dB direction coupler [53] is used to measure the picosecond pulse while

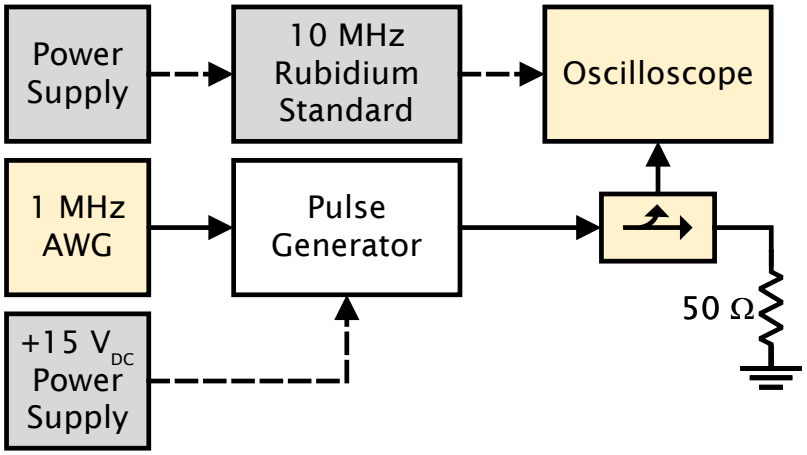


Figure 2.9: General measurement test setup for pulse metric evaluation.

protecting the measurement instrument front-end. The coupler's through port is loaded with a 50 Ω load while the coupled port is connected to the oscilloscope. A 1 MHz square-wave trigger is generated from the arbitrary waveform generator (AWG) built in the oscilloscope [54]. The pulse metrics (see Subsection 2.3.3) are extracted from a waveform, which is the average of 1024 pulses.

2.3.3 Evaluation of the UWB Generator Pulse Metrics

As discussed in Section 2.2, the critical factors impacting the generator's performance are the current supplied by the current source and the stub length l_4. The current-source resistance (R14) regulates the supplied current. Thus, the generator's output has been evaluated for R14 values between 0 Ω and 21 Ω along with two stub lengths, $l_4 = 10.45$, 11.95 mm.

Fig. 2.10 shows the peak-to-peak voltage *versus* the R14 values for the two stub lengths. The circle points indicate the measurement samples. It is observed that the longer stub length results in a marginal increase in the peak-to-peak voltage. However,

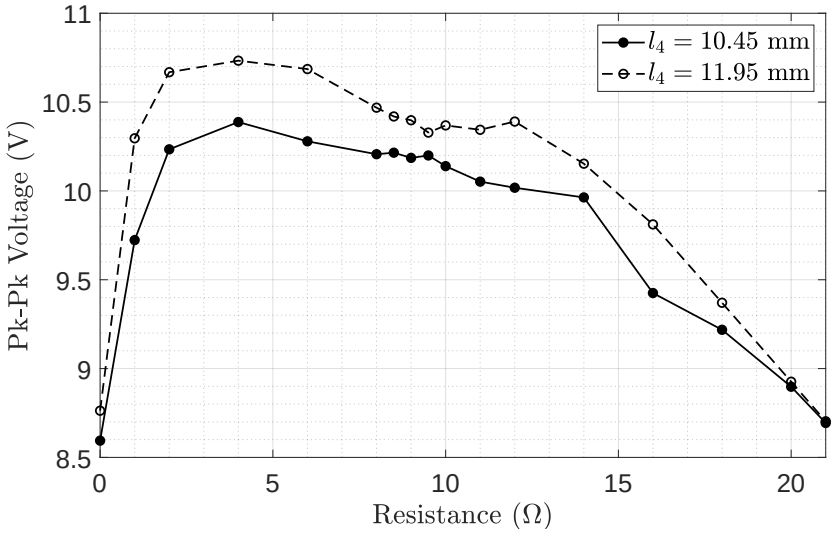


Figure 2.10: Peak-to-peak voltage *versus* current-source resistance (R14) and two stub lengths.

the current-source resistance has a marked impact. The R14 values between 2 Ω and 14 Ω provide the largest peak-to-peak voltage (exceeding 10 V).

Fig. 2.11 reports the FWHM pulse width dependence on the R14 value and the stub length. The strong impact of the current supply is again observed. A larger R14 setting (smaller supply current, I_{SOURCE}) decreases the FWHM from 340 ps to 260 ps. Since a narrow pulse width leads to the UWB performance, an R14 setting of 10 Ω or larger is desirable. Also, it is evident that the stub length plays little to no role in the FWHM pulse width. This is expected since the difference in the two stub lengths leads to reflection delays, which are well below the oscilloscope's 20 ps real-time sampling step.

The late-time ringing dependence on R14 and the stub length is shown in Fig. 2.12. At low current-source resistance settings, the stub length does not play a vital role in reducing the late-time ringing. However, at higher resistance settings, the longer stub length reduces the ringing by almost 100 ps. Also, at an R14 setting of 14 Ω, a substantial improvement in the late-time ringing for a 10.45 mm stub length

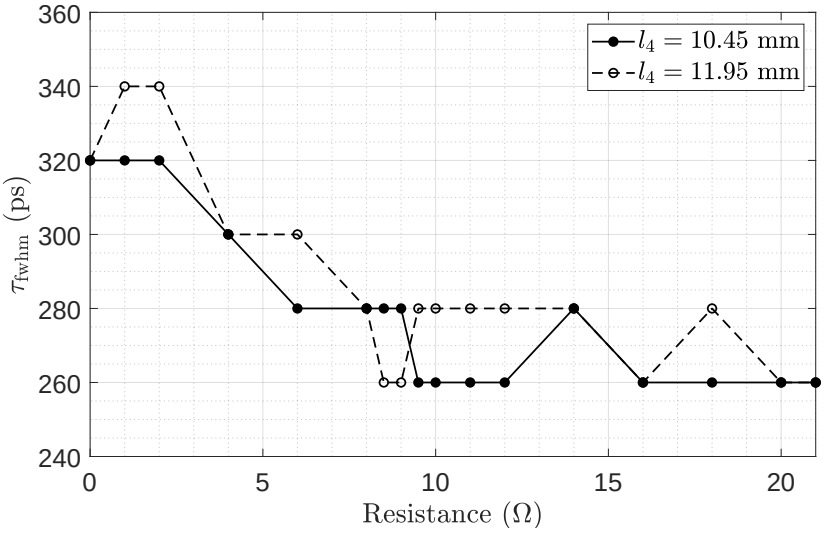


Figure 2.11: Full-width half maximum (FWHM) *versus* current-source resistance (R14) and two stub lengths.

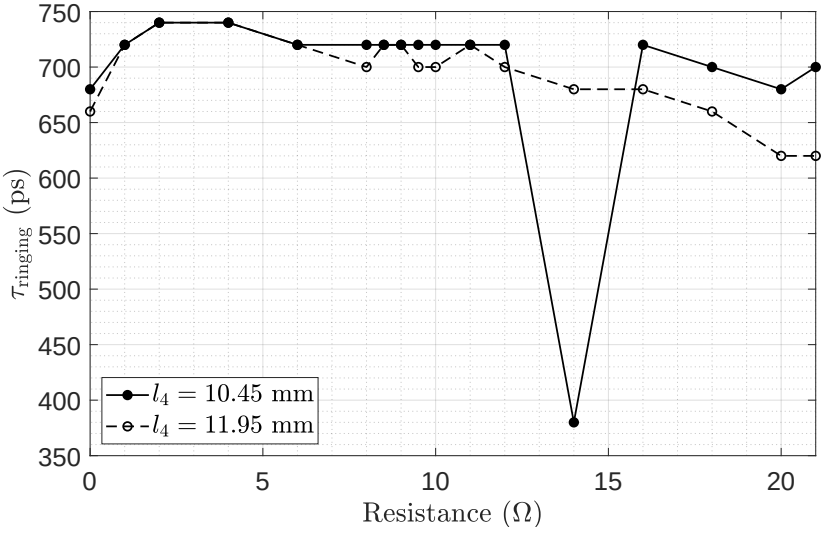
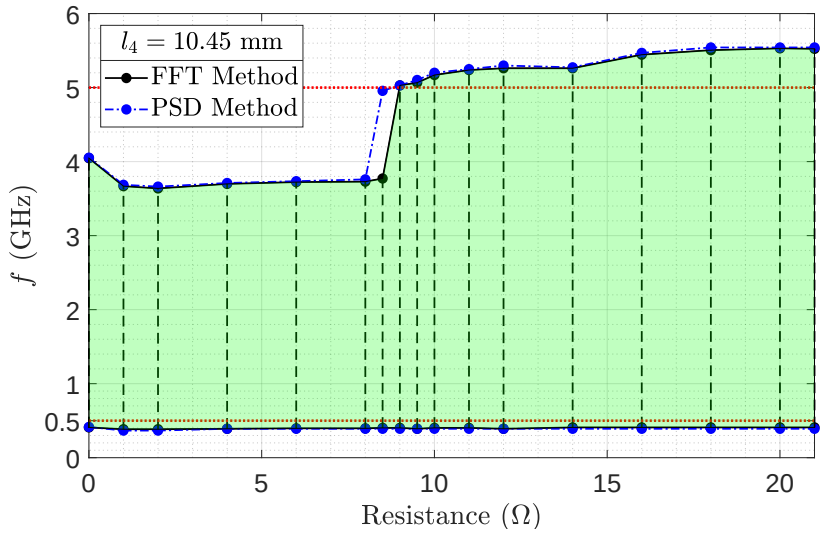


Figure 2.12: Ringing *versus* current-source resistance (R14) and the stub lengths ($\alpha = 0.05$).

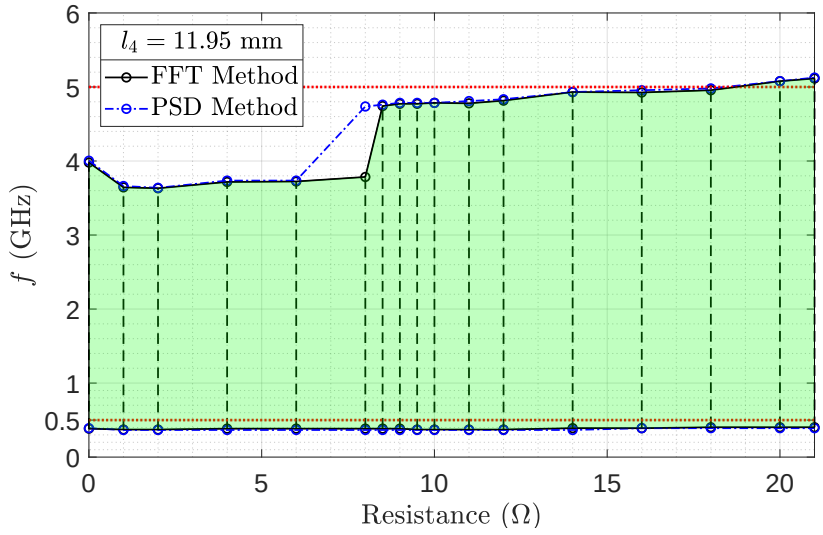
seems to occur. However, this is an outlier due to the choice of α in (2.6) where the Hilbert envelope quickly dips below that threshold for a single sample and quickly returns above it. By varying the decay level (α), it was seen that the current-source resistance and stub length only marginally improve the late-time ringing.

Fig. 2.13 and Fig. 2.14 show the results of the 10 dB bandwidth and FBW analysis. These figures are divided into two sub-figures, (a) and (b), which show the metrics for the 10.45 mm and 11.95 mm stub length, respectively. Fig. 2.13 shows the upper and lower frequency bounds resulting from the FFT method in black-solid lines, with the 10 dB bandwidth shaded in light green. The PSD method is also plotted for reference using the blue-dotted-dash lines. These metrics were plotted against various current-source resistance values similar to the temporal metrics. The vertical black-dashed lines show the occupied bandwidth per resistance setting. The horizontal red-dotted lines show our desired lower and upper-frequency limits of 500 MHz and 5 GHz. We observe an increase in the 10 dB bandwidth for a current-source resistance setting above 8.5 Ω (at least 47.5 mA current supply). A larger resistance setting results in a broader 10 dB bandwidth which aligns with Fig. 2.11 showing that the pulse width decreases. It can be seen that by varying the stub length, only the upper-frequency limits are changed. In our case, a shorter stub length is preferred as it easily covers the desired bandwidth for various current-source settings.

Fig. 2.14 shows an alternative way of visualizing the picosecond pulse generator's bandwidth through the FBW ratio. Again, the FFT results are shown as the black-solid line while the blue-dotted-dash line shows the PSD method results. The red-dotted line shows the desired 1:10 FBW ratio. These sub-figures show that the design easily achieves a 1:9 FBW for any current-source setting at both stub lengths. However, if a 1:10 FBW is desirable, a minimum current-source resistance value of 8.5 Ω is required no matter the stub length. It is important to note that, with proper

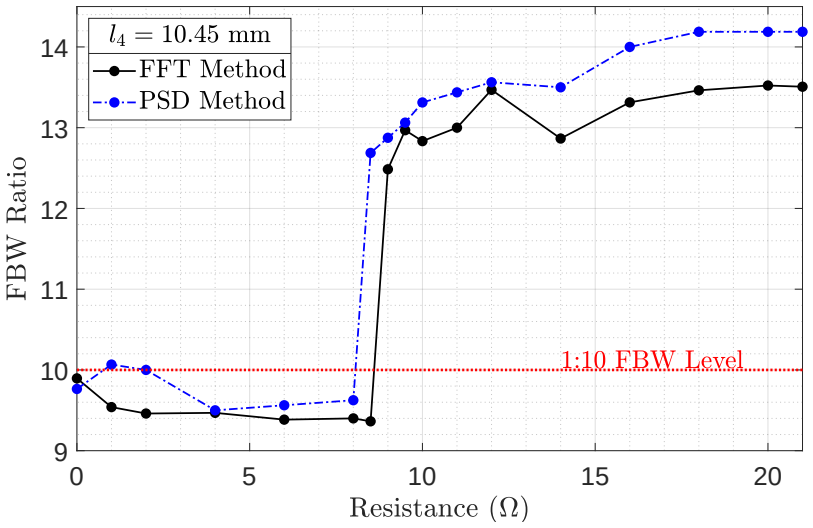


(a)

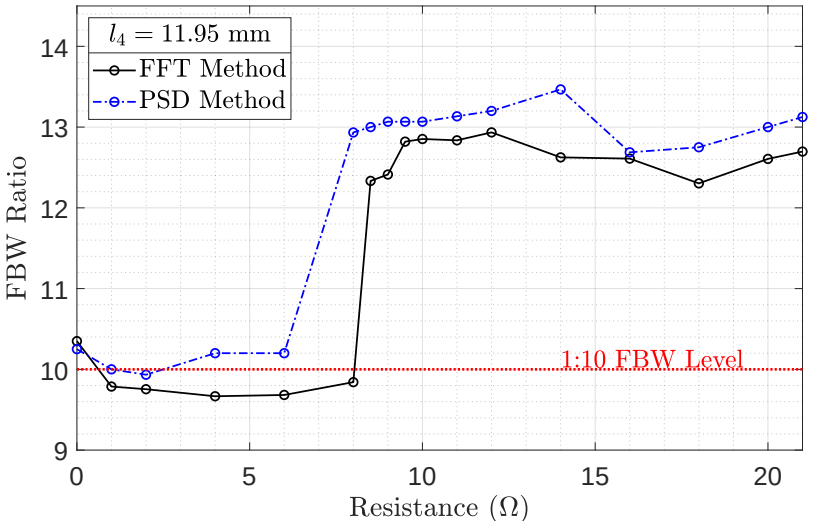


(b)

Figure 2.13: 10 dB bandwidth *versus* current source resistance (R14) settings for two stub lengths: (a) 10.45 mm and (b) 11.95 mm.



(a)



(b)

Figure 2.14: Fractional bandwidth (FBW) *versus* current source resistance (R14) settings for two stub lengths: (a) 10.45 mm and (b) 11.95 mm.

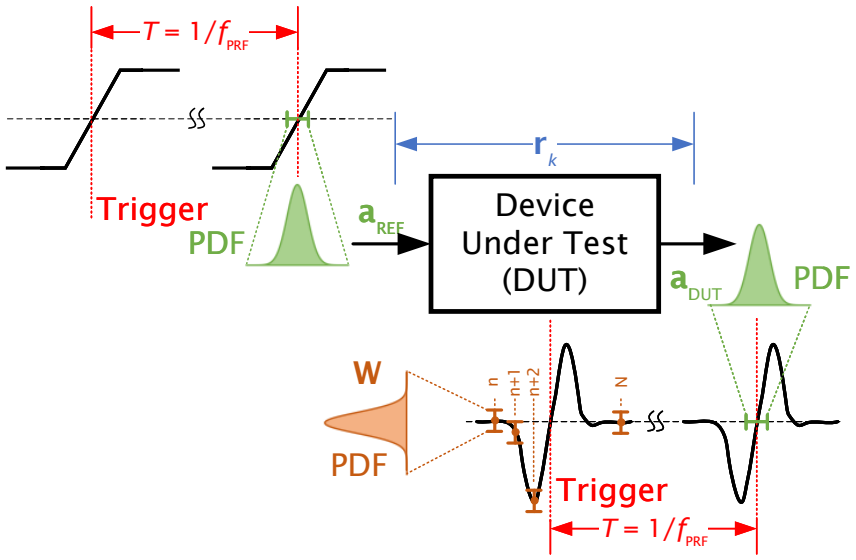


Figure 2.15: Jitter (green for **a** and blue for **r**) and noise (orange for **w**) metrics used for evaluation.

tuning, it is possible to achieve FBW ratio as high as 1:13.

2.4 Jitter and Noise Performance Metrics of the UWB Generator

2.4.1 Definitions of Jitter Metrics

Jitter metrics characterize a signal's timing variation for a set of edges from their ideal location, i.e., they measure the signal's phase stability. Here, we introduce the analysis of a pulse jitter at the generator's output using the known input trigger jitter as shown in Fig. 2.15. Both absolute and relative jitter [25]–[27] are evaluated with the available input and are then used in the pulse jitter metric.

2.4.1.1 Absolute Trigger Jitter

The absolute jitter of the generator's input (trigger jitter) is evaluated using standard definitions [25]–[27]. The trigger input is a periodic clock signal with an ideal

period of T. The absolute jitter is defined as a discrete-time random sequence, $\mathbf{a}$, where the k-th element is denoted as a_k. The trigger jitter is the time displacement between the k-th edge of the real clock with respect to the corresponding edge of the ideal clock [25]. The k-th edge of the ideal clock can be determined assuming the edges do not change with time and are spaced by exactly T. Therefore, the absolute jitter at the k-th sample, a_k, is defined as:

$$a_k = t_k - kT\,. \tag{2.10}$$

Here, t_k denotes the time instance where the real clock edge reaches half of its full amplitude. The trigger jitter is used as our reference and is denoted as $\mathbf{a}_{\mathrm{REF}}$ hereafter.

A probability distribution function (PDF) histogram for the rising edge of the trigger input is constructed from 10 000 waveforms to produce a statistical model over multiple clock periods. This histogram, which describes the absolute trigger jitter, provides three possible jitter metrics. The first metric is the standard deviation jitter (also known as RMS jitter) which is the standard deviation σ of the histogram. The second metric is the peak-to-peak jitter which is the maximum timing error defined by the minimum and maximum values on the abscissa of the histogram. However, since jitter noise is theoretically an unbounded Gaussian PDF, the length of the taken measurements drives the result. Due to this unbounded nature, it is better to bound the histogram by 6σ representing 99.6 % of the statistical distribution. Therefore, the third and final metric is the 6-sigma (6σ) jitter which is the $\pm 3\sigma$ standard deviation.

2.4.1.2 Absolute Pulse Jitter

Although the output of the picosecond pulse generator does not contain clock-like rising and falling edges, it does produce a periodic waveform which allows for

phase-stability evaluation. Here, we propose to use the temporal point where the pulse voltage crosses the 0 V reading while swinging between minimum-to-maximum peaks. The ideal pulse period is determined by the period, T, of the input trigger. Thus, we can use (2.10) to define the pulse jitter as $\mathbf{a}_{\mathrm{DUT}}$ where t_k is the k-th pulse zero-crossing point.

2.4.1.3 Relative Jitter

In contrast to absolute jitter, which compares a real clock to an ideal one, the relative-jitter metric compares two real clocks with the same average period T. One of these real clocks serves as a reference. Similarly to absolute jitter, the relative jitter is viewed as a discrete-time random process $\mathbf{r}$, where the element r_k is the time displacement of the k-th edge of the device under test (DUT) with respect to that of the reference clock [25]. The relative jitter can be expressed in terms of the two signals' absolute jitter:

$$\mathbf{r} = \mathbf{a}_{\mathrm{DUT}} - \mathbf{a}_{\mathrm{REF}}. \tag{2.11}$$

Here, the same σ, 6σ, and peak-to-peak jitter metrics apply. Note that a negative relative jitter result means that the DUT decreases the output jitter compared to the reference.

2.4.1.4 Jitter Measurements

Fig. 2.16 depicts the jitter measurement setup for each section of the picosecond pulse generator. During development, the generator has been broken down into separate hardware modules: the jitter cleaner, the trigger amplifier, and the driver along with the pulse generator circuit. The modules are accessed through SMA connectors. Note that these modules are amalgamated into a single PCB prototype, which has

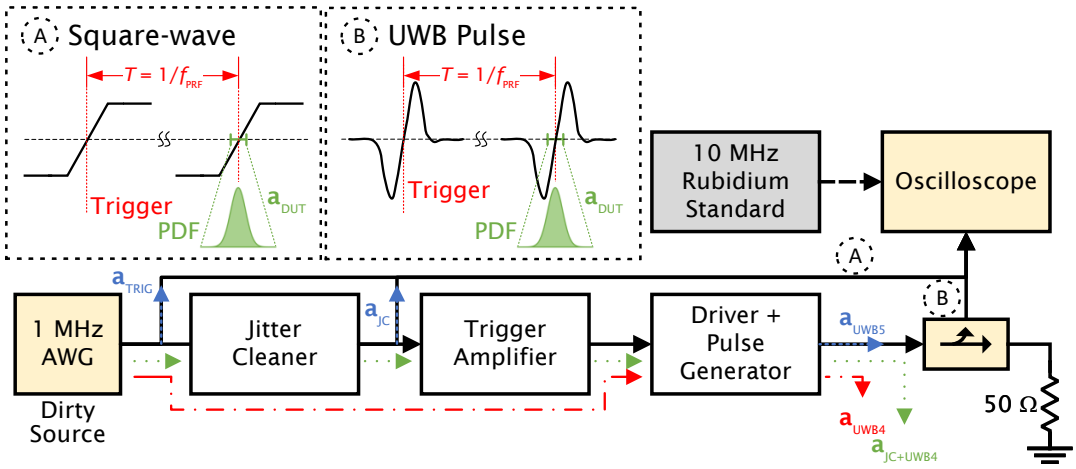


Figure 2.16: Measurement setup used for the jitter metric evaluation.

been presented in Section 2.2.

As indicated in Fig. 2.16, the absolute jitter values are denoted as $\mathbf{a}_{\mathrm{DUT}}$, where DUT designates the measured module. The blue-dashed, green-dotted and red-dash-dotted arrows indicate the output signals fed to the oscilloscope port. The blue arrows are associated with $\mathbf{a}_{\mathrm{TRIG}}$, $\mathbf{a}_{\mathrm{JC}}$, and $\mathbf{a}_{\mathrm{UWB5}}$, i.e., the absolute jitter at the outputs of the input trigger, the jitter cleaner, and the whole generator (shown in Fig. 2.6). The green arrow is associated with the total absolute jitter $\mathbf{a}_{\mathrm{JC+UWB4}}$ of the cascaded prototype. The $\mathbf{a}_{\mathrm{JC+UWB4}}$ measurement, as compared to $\mathbf{a}_{\mathrm{UWB5}}$, is a verification that the integrated and the cascaded prototypes are comparable. The red arrow corresponds to the absolute jitter $\mathbf{a}_{\mathrm{UWB4}}$ of the driver and pulse generator circuit, which bypasses the jitter cleaner and the trigger amplifier. Note that the oscilloscope is directly connected to the outputs of the AWG trigger and the jitter cleaner, whereas, in the measurements of the generated pulse, it requires the directional coupler for protection. The AWG is used to generate the input trigger, and is considered a dirty (not stable) source for this work since its jitter is significant enough to be measured.

The insets A and B in Fig. 2.16 illustrate the type of waveform measured by the oscilloscope at the outputs of the AWG trigger and the jitter cleaner (A) and the

UWB pulse generator (B). The oscilloscope is configured to trigger on the positive slope (first edge). We then delay the signal on the oscilloscope view to capture the next edge following the trigger edge. Ten thousand waveforms are obtained and saved for processing offline. A temporal histogram is created from the 10 000 waveforms by finding the closest discrete-time sample to a threshold crossing using a sinc $(\sin(t)/t)$ interpolation. The threshold is half the waveforms amplitude for the square-wave trigger signals whereas, for the UWB pulse, the threshold is 0 V. The σ, 6σ, and peak-to-peak absolute jitter are obtained from the histogram.

2.4.2 Jitter Evaluation of the UWB Generator

Table 2.3 and Table 2.4 show the absolute and relative jitter results for the prototype with R14 = 14 Ω and $l_4 = 10.45$ mm. Each table contains the standard deviation (σ), 6σ and pk-pk jitter results. Referring back to Fig. 2.16, the relationship between the circuits and measurement location of Table 2.3 can be understood. The absolute jitter of the trigger source ($\mathbf{a}_{\mathrm{TRIG,3.3V}}$ or $\mathbf{a}_{\mathrm{TRIG,5.0V}}$) has a standard deviation on the orders of 150 ps. When this trigger is applied to the proposed generator without the jitter cleaners we see a relative (REF = $\mathbf{a}_{\mathrm{TRIG,5.0V}}$, DUT = $\mathbf{a}_{\mathrm{UWB4}}$) jitter decrease in the standard deviation by 95.17 ps. The resulting standard deviation of the output jitter for the driver and pulse generator circuit is 52.83 ps ($\mathbf{a}_{\mathrm{UWB4}}$). This means that the pulse jitter standard deviation is on the order of 10 GSa/s (or 10 GHz), which is the Nyquist sampling rate required to reconstruct the 5 GHz frequency components. In this case, the total arrival time uncertainty of the pulse can vary as much as the 6σ or pk-pk jitter, which is on the order of 300 – 400 ps. This is 6 to 8 times the Nyquist sampling rate and is not desirable.

The introduction of the jitter cleaner provides a substantial improvement on the

Table 2.3: Results of the absolute jitter analysis.

Measurement	Std. Dev. (σ), (ps)	6-Sigma (6σ), (ps)	Pk-Pk (ps)
$\mathbf{a}_{\text{TRIG,3.3V}}$ [$\mathbf{a}_{\text{TRIG,5.0V}}$]	154.2 [148.0]	925.2 [888.0]	1240.0 [1200.0]
$\mathbf{a}_{\text{JC}}$	3.07	18.42	23.75
$\mathbf{a}_{\text{UWB4}}$	52.83	317.0	388.0
$\mathbf{a}_{\text{JC+UWB4}}$	1.658	9.948	12.5
$\mathbf{a}_{\text{UWB5}}$	1.653	9.918	11.25

Table 2.4: Results of the relative jitter analysis.

Measurement				
REF	DUT	Std. Dev. (σ), (ps)	6-Sigma (6σ), (ps)	Pk-Pk (ps)
$\mathbf{a}_{\text{TRIG,3.3V}}$	$\mathbf{a}_{\text{JC}}$	-151.13	-906.78	-1216.25
$\mathbf{a}_{\text{TRIG,5.0V}}$	$\mathbf{a}_{\text{UWB4}}$	-95.17	-571.02	-812.0
$\mathbf{a}_{\text{JC}}$	$\mathbf{a}_{\text{JC+UWB4}}$	-1.412	-8.472	-11.25
$\mathbf{a}_{\text{JC}}$	$\mathbf{a}_{\text{UWB5}}$	-1.417	-8.502	-12.5
$\mathbf{a}_{\text{TRIG,3.3V}}$	$\mathbf{a}_{\text{JC+UWB4}}$	-152.542	-915.252	-1227.5
$\mathbf{a}_{\text{TRIG,3.3V}}$	$\mathbf{a}_{\text{UWB5}}$	-152.547	-915.282	-1228.75

pulse jitter of the picosecond pulse generator. In measurements of generators that contain a jitter cleaner ($\mathbf{a}_{\text{JC+UWB4}}$, and $\mathbf{a}_{\text{UWB5}}$), either as an evaluation board or embedded on the PCB, we see a standard deviation of approximately 1.6 ps, and 6σ or pk-pk jitter on the orders of 10 ps. Therefore, there is 50 times reduction due to the jitter cleaner ($\mathbf{a}_{\text{TRIG,3.3V}}$ *versus* $\mathbf{a}_{\text{JC}}$) and two times reduction due to the generator circuit design ($\mathbf{a}_{\text{JC}}$ *versus* $\mathbf{a}_{\text{JC+UWB4}}$, $\mathbf{a}_{\text{UWB5}}$). It should be mentioned that these results include the oscilloscope's typical RMS (standard deviation) trigger jitter of 1 ps [45]. The inclusion of the jitter cleaner enables the generator to maintain stability to within the Nyquist sampling rate necessary for reconstruction.

2.4.3 Definitions of Noise Metrics

We propose a method to evaluate the generator's voltage noise so that it excludes a noise contribution from the measurement setup. Here, we are primarily concerned with voltage amplitude uncertainty due to internal noise produced within the generator. This noise is usually measured through the RMS (one σ) of the PDF since it is considered random and modelled by a Gaussian distribution [55].

In order to evaluate the generator's performance, it is crucial to de-embed the noise produced by the measurement setup. This is indeed possible assuming that: (i) the measurement setup for the DUT and that for the inherent setup noise are the same, and (ii) the DUT noise is greater than that in the measurement reference. It is also necessary to assume that the noise sources of the setup and the DUT are uncorrelated and that their statistical models are available. Therefore, two noise models are developed and used for this analysis: (i) for the measurement setup (system noise), and (ii) for the DUT (pulse generator noise). As explained next, these models are based on histograms of the PDF generated at each temporal sample for $M = 10\,000$ pulse waveforms.

Here, we propose to define noise as a function of the temporal sample n since the noise is expected to increase within the pulse duration. Thus, the *voltage noise* is quantified by the discrete-time random process, $\mathbf{w}$, where the element w_n is the variance σ_n^2 of the set of M pulse waveforms at the n-th time sample. In all results presented hereafter, the waveforms contain $N = 200$ samples, i.e., $n = [1, \ldots, 200]$.

2.4.3.1 System Noise Measurement

A directional coupler [53] is required to protect the input of the oscilloscope while measuring the pulse generator (the DUT). Therefore, to evaluate the system noise,

the oscilloscope is connected directly to the coupled port, which incurs a 10 dB loss. Two 50 Ω loads terminate the input and through ports. The voltage deviation is set to 400 mV/div. Note that the voltage-deviation setting affects the oscilloscope voltage resolution. Also, the 10 dB external attenuation due to the direction coupler affects the noise measurements. We assume that this attenuation affects the noise similarly in the system and the DUT measurements. This measurement provides the system noise $(\sigma_n^2)_{\mathrm{SYS}}$.

2.4.3.2 Pulse Generator (DUT) Noise Measurement

This time, the generator's output is connected to the directional coupler's input port while the through port is terminated with a 50 Ω load. The oscilloscope is still connected directly to the coupled port. The voltage deviation of the oscilloscope remains the same as in the system-noise measurement setup. A time window is captured before and after the pulse to characterize the change in the noise metrics between pulse and no-pulse periods. This measurement provides the noise $(\sigma_n^2)_{\mathrm{M}}$, which includes the system noise $(\sigma_n^2)_{\mathrm{SYS}}$ and the noise due to the DUT $(\sigma_n^2)_{\mathrm{DUT}}$, which is to be extracted.

2.4.3.3 System Noise De-embedding Process

The noise of the pulse generator is defined by $(\sigma_n^2)_{\mathrm{DUT}}$ whereas the system measurement noise is $(\sigma_n^2)_{\mathrm{SYS}}$. The total measured noise $(\sigma_n^2)_{\mathrm{M}}$ includes both, which is modelled as

$$(\sigma_n^2)_{\mathrm{M}} = (\sigma_n^2)_{\mathrm{DUT}} + (\sigma_n^2)_{\mathrm{SYS}} + \Sigma_{\mathrm{DUT,SYS}}, \tag{2.12}$$

where $\Sigma_{\mathrm{DUT,SYS}}$ is the covariance between the two signals. Provided that the noise in the DUT signal that in the SYS signal are uncorrelated and that they are both with

zero mean, $\Sigma_{\mathrm{DUT,SYS}} = 0$ and (2.12) simplifies to

$$(\sigma_n^2)_{\mathrm{M}} = (\sigma_n^2)_{\mathrm{DUT}} + (\sigma_n^2)_{\mathrm{SYS}}. \tag{2.13}$$

Since the system noise is estimated separately under the same test conditions as the DUT, the DUT variance is obtained as

$$(\sigma_n^2)_{\mathrm{DUT}} = (\sigma_n^2)_{\mathrm{M}} - (\sigma_n^2)_{\mathrm{SYS}}, \tag{2.14}$$

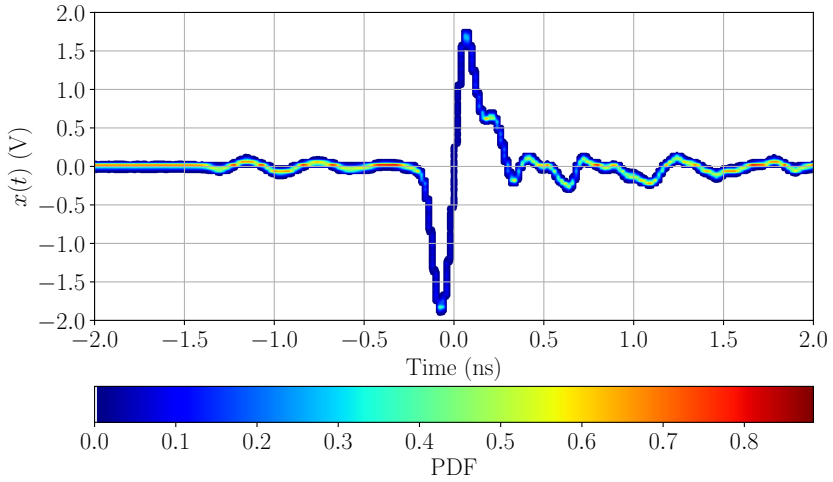
and the standard deviation is

$$(\sigma_n)_{\mathrm{DUT}} = \sqrt{(\sigma_n^2)_{\mathrm{M}} - (\sigma_n^2)_{\mathrm{SYS}}}\,. \tag{2.15}$$

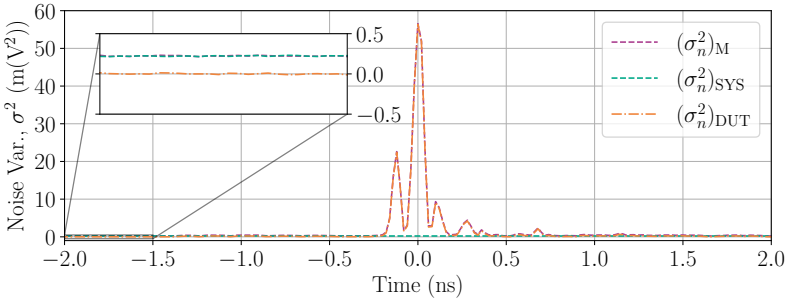
Note that (2.15) implies that $(\sigma_n^2)_{\mathrm{M}} \geq (\sigma_n^2)_{\mathrm{SYS}}$. If $(\sigma_n^2)_{\mathrm{M}} < (\sigma_n^2)_{\mathrm{SYS}}$, then the generator does not produce measurable additive noise.

2.4.4 Noise Evaluation of the UWB Generator

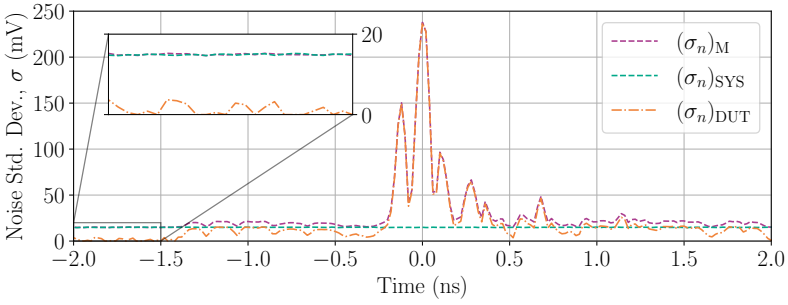
The results of the voltage noise analysis are presented in Fig. 2.17. Shown in Fig. 2.17a is a histogram heatmap generated by the 10 000 waveforms. The red and blue colours indicate high and low probabilities of the waveform values, respectively. Note that these waveforms are obtained with the 10 dB directional coupler, and the 10 dB voltage decrease has not been compensated in the plot. Fig. 2.17b and Fig. 2.17c shows the variance and standard deviation describing the total measured noise, the system noise, and the de-embedded DUT noise *versus* time. As expected, within the pulse duration, additive Gaussian noise is present. The mean of the reference noise variance is 0.22 m(V^2) whereas its standard deviation is 14.93 mV. We observe that



(a)



(b)



(c)

Figure 2.17: Noise analysis with 10 dB external attenuation and an oscilloscope voltage division of 400 mV/div: (a) A picosecond pulse generator waveform histogram heatmap of 10 000 waveforms overlaid. (b) The noise variance of the histogram of the measured signal ($(\sigma_n^2)_{\mathrm{M}}$), system noise measurement ($(\sigma_n^2)_{\mathrm{SYS}}$), and DUT ($(\sigma_n^2)_{\mathrm{SYS}}$). (c) The noise standard deviation of the histogram for the same respective measurements.

during the main pulse transition, the DUT noise increases, e.g., its standard deviation becomes about 16 times greater than the mean of the system-noise standard deviation. Their largest values are seen at the time of the largest voltage swings. However, at the pulse minima and maxima, the voltage is stable to within a standard deviation of 55 mV.

In the timeframe from -2.0 ns to -1.5 ns, the generator does not produce additive noise, resulting in the presence of system noise only. There are instances within this timeframe where $(\sigma_n^2)_{\mathrm{M}} < (\sigma_n^2)_{\mathrm{SYS}}$ and (2.15) produces a small imaginary number ($(\sigma_n^2)_{\mathrm{DUT}}$ not exceeding -0.016 m(V^2)). In such instances, we enforce a hard zero floor. An intuitive explanation is that while the transmitter is in an off or standby state, its additive noise is not measurable with this setup. Mathematically, the negative DUT noise variance values can be explained through the existence of nonzero positive covariance $\Sigma_{\mathrm{DUT,SYS}}$ in (2.12), resulting in corrected forms of (2.14) and (2.15):

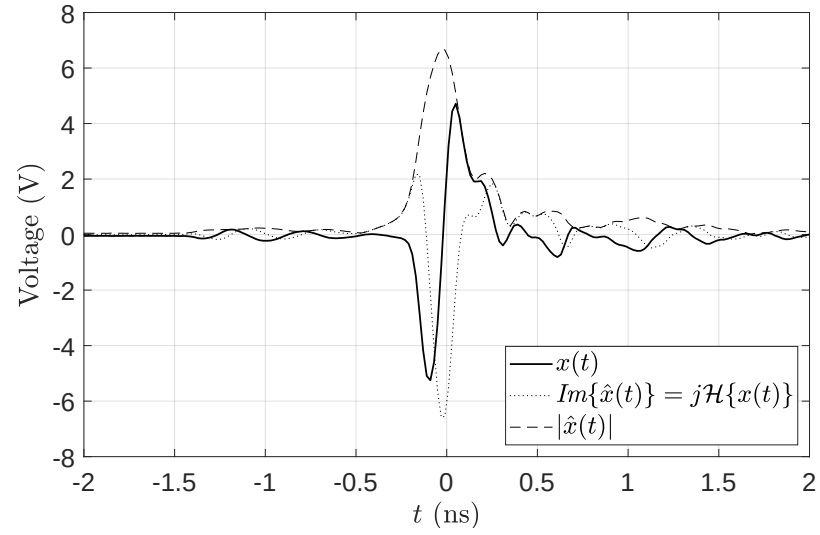
$$(\sigma_n^2)_{\mathrm{DUT}} = (\sigma_n^2)_{\mathrm{M}} - (\sigma_n^2)_{\mathrm{SYS}} - \Sigma_{\mathrm{DUT,SYS}} \tag{2.16}$$

$$(\sigma_n)_{\mathrm{DUT}} = \sqrt{(\sigma_n^2)_{\mathrm{M}} - (\sigma_n^2)_{\mathrm{SYS}} - \Sigma_{\mathrm{DUT,SYS}}}. \tag{2.17}$$

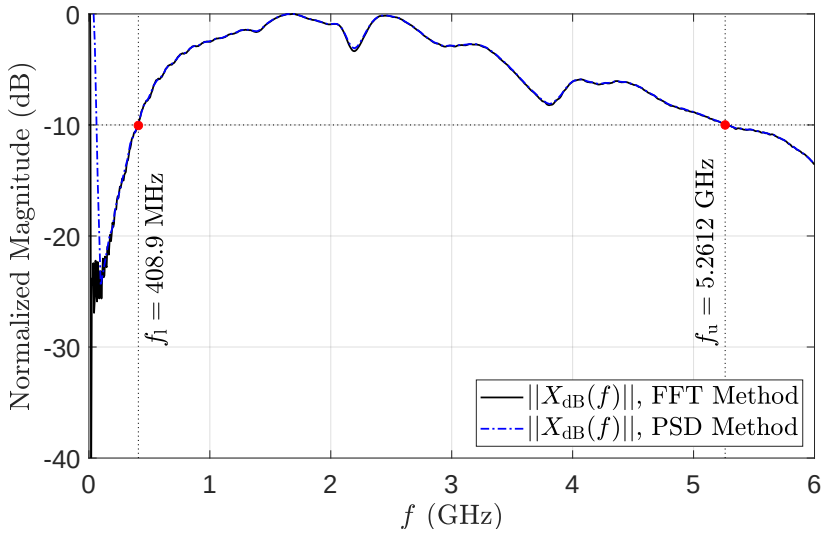
This covariance term, however, cannot be obtained as it is inherent to the measurement setup.

2.5 Discussion

It is evident that the proposed generator design has to strike a balance between maximum peak-to-peak voltage and maximum spectral bandwidth. The choices of the current-source supply current and the stub length are crucial. A smaller current supply (larger R14 resistance) results in a shorter pulse containing higher frequency



(a)



(b)

Figure 2.18: Sample of a pulse generated by the picosecond pulse generator (R14 = 14 Ω, l_4 = 10.45 mm). (a) Time-domain plot of the measured pulse ($x(t)$), the imaginary part of the analytical waveform obtained with the Hilbert transform, and the Hilbert envelope. (b) Frequency-domain plot of the measured pulse calculated using the FFT and PSD methods. The −10 dB lower and upper frequency bounds are shown by the red dots.

Table 2.5: Comparison with prior literature.

Metric	This work	[13]	[14]	[22]	[17]	[23]	[16]	[18]	[19]	[20]	[6]	[21]
Pulse Type	MC	MC	G/MC	G^n	G/MC	G^n	G	G	G	G	MC	G/MC
Technology	SRD	SRD	SRD	CMOS	SRD	CMOS	SRD	SRD	SRD	SRD	SRD	SRD
PRF (MHz)	1	1	3.125 kHz – 20	10 – 50	10 – 100	33	NA	10	10	0.1	1000	10
$V_{\text{pk-pk}}$ (V)	9.9633	9.477	27 / 25	0.425	6.8 / 4.6, 1.2 / 0.7	2.12	3.95, 4.1, 3.9, 3.92	1.67 / 0.83	1.586	6.4	0.3	1.3 / 1.6
p_{ev} (V)	6.677	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
τ_{FWHM} (ps)	280	NA	180*/ 500†	600†	220, 60*	500†	34, 24, 24, 34*	214, 153*	286*	620*	330 – 380	300 – 1000†
τ_{ringing} (ps)	380	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
f_l (GHz)	0.4089	0.4395	NA	3.8	0.5 / 1	3.6§	NA	NA	NA	NA	2.5, 2§	NA
f_u (GHz)	5.2612	3.5889	NA	8.8	3 / 13	11.1§	NA	NA	NA	NA	11, 10.6§	NA
f_c (GHz)	2.8351	3.8087	NA	6.3§	1.75 / 7§	7.35§	NA	NA	NA	NA	6.75, 6.3§	NA
B (GHz)	4.8523	3.1494	NA	5	2.5 / 12§	7.5	NA	NA	NA	NA	8.5, 8.6§	NA
b_{f}	1.712	0.8269§	NA	0.7937§	1.429 / 1.714§	1.020§	NA	NA	NA	NA	1.259, 1.365§	NA
b_{fr}	12.8657	8.166§	NA	2.316§	6 / 13§	3.083§	NA	NA	NA	NA	4.4, 5.3§	NA
$\mathbf{a}_k$ (ps)	1.653	1.32¶	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
$(\sigma_n^2)_{\text{DUT}}$ (m(V)^2)	46.42	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
$(\sigma_n)_{\text{DUT}}$ (mV)	215.45	324.0¶	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA

* Gaussian pulse FWHM value reported. † Full pulse width value reported, calculation criterion unknown.
§ Estimated based on reported figures but not explicitly stated in cited text. ¶ Different calculation criterion was used.
NA stands for "Not Available".

components. On the other hand, a larger current supply (smaller R14 resistance) is required to produce a larger peak-to-peak voltage. Similarly, a longer stub length (l_4) produces a larger peak-to-peak voltage, whereas a shorter length results in the higher frequency components. Based on these observations, a picosecond pulse generator has been tuned to meet our design criteria of a 1:10 FBW ranging from 500 MHz to 5 GHz with 10 V peak-to-peak voltage.

Fig. 2.18 presents the output pulse of the tuned prototype, where the current-source resistance (R14) is 14 Ω and the stub length (l_4) is 10.45 mm. Fig. 2.18a shows the picosecond pulse in the time domain with a black-solid line. The imaginary part (see (2.2)) is also plotted along with the resulting Hilbert envelope. Fig. 2.18b shows the normalized FFT and PSD pulse spectra along with the −10 dB bandwidth limits.

All performance metrics, as defined and proposed in this work, are presented in the first column of Table 2.5. The tuned generator has a band extending from 408.9 MHz to 5.2612 GHz with FBW (b_{f}) of 1.7 and FBW ratio (b_{fr}) of 1:12.9. At the same time, it achieves 10 V peak-to-peak voltage.

The inclusion of the jitter cleaner dramatically reduces the generator's jitter to only a few picoseconds. With an output absolute jitter standard deviation of 1.6 ps, the design shows a 100× improvement compared to the input trigger. The voltage noise of the generator is consistent while a pulse is being generated. When the generator is in an off or standby state, before and after a pulse generation, the internal circuitry generates no additive noise. At the minima and maxima of the pulse, the waveform is consistent within a standard deviation of 55 mV, thus, ensuring reproducible peak-to-peak voltage and peak power. Overall, the proposed generator circuit has been shown to produce a stable, jitter-free monocycle pulse.

Table 2.5 compares the proposed design with similar designs reported in the literature. The pulse types are designated as Gaussian (G), Monocycle (MC), and

high-order Gaussian derivatives (G^n). The "/" in the table helps separate metrics when multiple pulse types are reported whereas "," indicates multiple results per pulse type. "NA" indicates that the metric has not been reported.

Table 2.5 illustrates the superior performance of the proposed generator. It also shows the lack of complete performance evaluation in previous work, especially in terms of jitter and voltage noise. This is due to the lack of an agreed-upon set of metrics in the UWB community. The metrics proposed here aim to fill this gap. The pulse stability (jitter and noise) has never been reported in the prior publications, yet these are crucial metrics of a generator's performance. It is our hope that the complete set of metrics proposed here will lead to an all-inclusive figure of merit (FOM) which could be used in the future to compare the various pulse-generator designs.

2.6 Conclusion

An SRD-based picosecond pulse generator is designed to generate a stable differentiated Gaussian waveform with 1:10 FBW ratio, bandwidth from 500 MHz to beyond 5 GHz at the -10 dB level, and 10 V peak-to-peak voltage. The tuning strategies are discussed, which lead to a significant improvement in pulse bandwidth without loss of peak-to-peak voltage compared to the designs reported in the literature. It is found that the critical factors impacting the pulse metrics are the amount of current supplied to the pulse generating circuit by the DC current source as well as the length of the stub responsible for the pulse differentiation. A complete set of metrics is defined for the performance analysis of the UWB pulse generator with the introduction of new metrics for jitter and noise analysis. It is determined that the major contribution to the generator's jitter is due to the input trigger source. The inclusion of a jitter cleaner is shown to result in a dramatic improvement in pulse stability.

References

[1] "First report and order, revision of part 15 of commission's rule regarding UWB transmission system FCC 02-48," Federal Communications Commission (FCC), Washington, DC, USA, Tech. Rep. FCC 02-48, Apr. 2002.

[2] "Devices using ultra-wideband (UWB) technology," Industry Canada, Spectrum Management and Telecommunications, Canada, Tech. Rep. RSS-220, Apr. 2009.

[3] "ECC decision (06)04: The harmonised conditions for devices using ultra-wideband (UWB) technology in the bands below 10.6 GHz," Electronic Communications Committee (ECC), The European Conference of Postal and Telecommunications Administration (CEPT), Copenhagen, Denmark, Tech. Rep. ECC Decision (06)04, Mar. 2006.

[4] J. Lee, C. Nguyen, and T. Scullion, "A novel, compact, low-cost, impulse ground-penetrating radar for nondestructive evaluation of pavements," *IEEE Trans. Instrum. Meas.*, vol. 53, no. 6, pp. 1502–1509, Dec. 2004.

[5] F. Rodriguez-Morales, C. Leuschen, C. L. Carabajal, *et al.*, "An improved UWB microwave radar for very long-range measurements of snow cover," *IEEE Trans. Instrum. Meas.*, vol. 69, no. 10, pp. 7761–7772, Oct. 2020.

[6] R. Thai-Singama, F. Du-Burck, and M. Piette, "A low-cost UWB pulse generator for medical imaging, through-wall imaging and surveillance systems," in *2012 IEEE Asia-Pacific Conference on Applied Electromagnetics (APACE)*, Melaka, Malaysia: IEEE, Feb. 2012, pp. 45–50.

[7] A. D. Pitcher, J. J. McCombe, E. A. Eveleigh, and N. K. Nikolova, "Compact transmitter for pulsed-radar detection of on-body concealed weapons," in *2018*

IEEE/MTT-S International Microwave Symposium (IMS), Philadelphia, PA, USA: IEEE, Jun. 2018, pp. 919–922.

[8] E. A. Eveleigh, "Development of an ultra-wideband (UWB) pulse generator and printed antenna for concealed weapons detection radar," M.A.Sc. thesis, Department of Electrical and Computer Engineering, McMaster University, Hamilton, ON, Canada, Jul. 2020.

[9] N. K. Nikolova, "Microwave biomedical imaging," *Wiley Encyclopedia of Electrical and Electronics Engineering*, pp. 1–22, Apr. 2014.

[10] E. C. Fear, J. Bourqui, C. Curtis, D. Mew, B. Docktor, and C. Romano, "Microwave breast imaging with a monostatic radar-based system: A study of application to patients," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 5, pp. 2119–2128, May 2013.

[11] E. Porter, E. Kirshin, A. Santorelli, M. Coates, and M. Popović, "Time-domain multistatic radar system for microwave breast screening," *IEEE Antennas Wireless Propag. Lett.*, vol. 12, pp. 229–232, Feb. 2013.

[12] J. Sachs, *Handbook of Ultra-Wideband Short-Range Sensing*, 1st. Weinheim, Germany: Wiley-VCH Verlag & Co., 2013.

[13] A. D. Pitcher, "Compact low-cost ultra-wideband pulsed-radar system," M.A.Sc. thesis, Department of Electrical and Computer Engineering, McMaster University, Hamilton, ON, Canada, Aug. 2019.

[14] P. Protiva, J. Mrkvica, and J. Macháč, "Universal generator of ultra-wideband pulses," *Radioengineering*, vol. 17, no. 4, pp. 74–78, Dec. 2008.

[15] J. McCombe, "Cognitive microwave radar for the stand-off detection of on-body concealed weapons," Computational Electromagnetics Laboratory, McMaster University, Hamilton, ON, Canada, Tech. Rep. CEM-R-70, Mar. 2015.

[16] M. Rahman and K. Wu, "A nonlinear transmission approach to compressing rise and fall time in picosecond pulse generation," *IEEE Trans. Instrum. Meas.*, vol. 70, pp. 1–13, Apr. 2021.

[17] R. Feghhi, D. Oloumi, and K. Rambabu, "Tunable subnanosecond gaussian pulse radar transmitter: Theory and analysis," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 9, pp. 3823–3833, Apr. 2020.

[18] R. Feghhi, D. Oloumi, and K. Rambabu, "Design and development of an inexpensive sub-nanosecond gaussian pulse transmitter," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 9, pp. 3773–3782, Sep. 2019.

[19] D. Oloumi and E. Fear, "A picosecond pulse generator using SRD diodes: Design, analysis, and measurements," in *2018 USNC-URSI Radio Science Meeting (Joint with AP-S Symposium)*, Boston, MA, USA: IEEE, Jul. 2018, pp. 159–160.

[20] Y. Ahajjam, O. Aghzout, J. M. Catalá-Civera, F. Peñaranda-Foix, and A. Driouach, "A compact UWB sub-nanosecond pulse generator for microwave radar sensor with ringing miniaturization," in *2016 5th International Conference on Multimedia Computing and Systems (ICMCS)*, Marrakech, Morocco: IEEE, 2016, pp. 497–501.

[21] C. Zhang and A. E. Fathy, "Reconfigurable pico-pulse generator for UWB applications," in *2006 IEEE Int. Microw. Symp. Digest*, San Francisco, CA, USA: IEEE, Jun. 2006, pp. 407–410.

[22] X. An, J. Wagner, and F. Ellinger, "An efficient ultrawideband pulse transmitter with automatic ON–OFF functionality for primary radar systems," *IEEE Microw. Wireless Compon. Lett.*, vol. 30, no. 4, pp. 449–452, Apr. 2020.

[23] S. Gao and K. Moez, "A 2.12-V V_{pp} 11.67-pJ/pulse fully integrated uwb pulse generator in 65-nm CMOS technology," *IEEE Trans. Circuits Syst. I*, vol. 67, no. 3, pp. 1058–1068, Mar. 2020.

[24] E. Kaya and K. Entesari, "A broadband CMOS pulse generator for UWB systems," in *2020 IEEE Radio and Wireless Symposium (RWS)*, IEEE, San Antonio, Texas, USA, Jan. 2020, pp. 9–11.

[25] N. Da Dalt and A. Sheikholeslami, *Understanding Jitter and Phase Noise: A Circuits and Systems Perspective*, 1st. Cambridge, UK: Cambridge University Press, 2018.

[26] "Definitions and terminology for synchronization networks," Telecommunication Standardization Sector of International Telecommunication Union (ITU-T), Recommendation G.810, Aug. 1996.

[27] "Jitter specifications for timing signals," Integrated Device Technology, Inc., San Jose, CA, USA, Application Note AN-840 Revision A, May 2014.

[28] "3313 - 3 mm trimpot triming potentiometer," Bourns, Inc., Riverside, CA, USA, Datasheet 3313, Aug. 2019.

[29] "Low noise silicon bipolar RF transistor," Infineon Technologies, Munich, Germany, Datasheet BFP196W, Apr. 2014.

[30] "Single silicon RF Schottky diode," Infineon Technologies, Munich, Germany, Datasheet BAT15-03W, v1.0, Jun. 2018.

[31] "Silicon step recovery diode," MACOM Technology Solutions Inc., Lowell, MA, USA, Datasheet MMDx & SMMDx Series, Rev. V4.

[32] "Wideband, current feedback operational amplifier with disable," Texas Instruments, Dallas, TX, USA, Datasheet SBOS226D, Rev. D, Jul. 2008.

[33] "LT3092: 200mA 2-terminal programmable current source," Linear Technology, Milpitas, CA, USA, Datasheet LT0217 Rev. C, Feb. 2009.

[34] "Si5317 pin-controlled 1 – 711 MHz jitter cleaning clock," Silicon Laboratories Inc., Austin, TX, USA, Datasheet Si5317 Rev. 1.1, Apr. 2011.

[35] "Innovative DSPPL and MultiSynth clock architecture enables high-density 10/40/100G line card designs," Silicon Laboratories Inc., Austin, TX, USA, White Paper, 2013.

[36] "SN74LVC1G04 single inverter gate," Texas Instruments, Dallas, TX, USA, Datasheet SCES214AD, Rev. AD, Oct. 2014.

[37] "Surface mount bias-tee TCBT-14R+," Mini-Circuits, Brookyn, NY, USA, Datasheet TCBT-14R+, Rev. D, Apr. 2018.

[38] "Pulse and waveform generation with step recovery diodes," Hewlett Packard, Palo Alto, CA, USA, Application Note 918, 1986.

[39] "TPS56220x 4.5-V to 17-V input, 2-A synchronous step-down voltage regulator in 6-pin SOT-23," Texas Instruments, Dallas, TX, USA, Datasheet SLVSD91B, Rev. B, Sep. 2020.

[40] "LMZ34002 15-W negative output power module with 4.5-V to 40-V input in QFN package," Texas Instruments, Dallas, TX, USA, Datasheet SNVS989C, Rev. C, Apr. 2018.

[41] "TPS7A470x 36-V, 1-A, 4-μV_{RMS}, RF LDO voltage regulator," Texas Instruments, Dallas, TX, USA, Datasheet SBVS204F, Rev. F, Sep. 2014.

[42] "TPS7A33 -36-V, 1-A, ultralow-noise negative voltage regulator," Texas Instruments, Dallas, TX, USA, Datasheet SBVS169D, Rev. D, Apr. 2015.

[43] "INA233 high-side or low-side measurement, bidirectional current and power monitoring with i^2c-, smbus-, and pmbus-compatible interface," Texas Instruments, Dallas, TX, USA, Datasheet SBOS790, Apr. 2017.

[44] "RO4000 series - high frequency circuit materials," Rogers Corporation, Chandler, AZ, USA, Datasheet PUB# 92-004, 2018.

[45] "Digital phosphor oscilloscopes / digital serial analyzers," Tektronix, Inc., Datasheet 4HW-19377-15, Mar. 2009.

[46] L. Marple, "Computing the discrete-time "analytic" signal via FFT," *IEEE Trans. Signal Process.*, vol. 47, no. 9, pp. 2600–2603, Sep. 1999.

[47] F. R. Kschischang, *The hilbert transform*, Lecture Notes from the Edward S. Rogers Sr. Department of Electrical and Computer Engineering, University of Toronto, Canada, Mar. 2015. [Online]. Available: https://www.comm.utoronto.ca/frank/notes/hilbert.pdf.

[48] T. Zwick, W. Wiesbeck, J. Timmermann, and G. Adamiuk, *Ultra-Wideband RF System Engineering* (EuMA High Frequency Technologies Series), 1st. Cambridge, UK: Cambridge University Press, 2013.

[49] *Hilbert: Discrete-time analytical signal using hilbert transform*, MathWorks MATLAB Help Center, 2022. [Online]. Available: https://www.mathworks.com/help/signal/ref/hilbert.html.

[50] P. D. Welch, "The use of fast fourier transform for the estimation of power spectra: A method based on time averaging over short, modified periodograms," *IEEE Trans. Audio Electroacoust.*, vol. 15, no. 2, pp. 70–73, Jun. 1967.

[51] *Pwelch: Welch's power spectral density estimate*, MathWorks MATLAB Help Center, 2022. [Online]. Available: https://www.mathworks.com/help/signal/ref/pwelch.html.

[52] "Rubidium frequency standard model FE-5680A series: Operation and maintenance instructions," Frequency Electronics, Inc., Mitchel Field, NY, USA, Tech. Manual TM 5680-0211, Nov. 2002.

[53] "Coaxial 50W 10 dB directional coupler 0.5 – 6 GHz," RF-Lambda, Datasheet RFDC5M06G10, Rev. 5.0, Jun. 2022.

[54] "Keysight technologies InfiniiVision 6000 X-series oscilloscope," Keysight Technologies, Inc., Datasheet 5991-4087EN, Dec. 2024.

[55] "Evaluating oscilloscope vertical noise characteristics," Keysight Technologies, Tech. Rep. 5989-3020EN, Aug. 2019.

CHAPTER 3:

ACCURATE HIGH-SPEED EQUIVALENT-TIME SAMPLING RECEIVER: ARCHITECTURE AND PERFORMANCE METRICS

Preface

This chapter is a reproduction of a manuscript submitted to the IEEE Transactions on Instrumentation and Measurement on March, 25th 2025:

A. D. Pitcher, C. W. Baard, M. Georgiev, and N. K. Nikolova, "Accurate high-speed equivalent-time sampling receiver: Architecture and performance metrics," *IEEE Transactions on Instrumentation and Measurement*, pp. 1–15, Mar. 2025.

I was responsible for the development, design, and validation of the proposed equivalent-time sampling receiver (ETSR), as well as the establishment of the experimental framework and measurement methodology. I conducted the investigation and formal analysis of the results, created the visualizations, and took the lead in authoring and editing the manuscript. Charl W. Baard contributed to the prototype

development, the manufacturing of printed circuit boards, and the manuscript review. Mihail Georgiev supported the development of the proposed calibration method and contributed to reviewing the manuscript. Natalia K. Nikolova supervised the project, provided guidance during design reviews and testing, and assisted with manuscript editing.

3.1 Introduction

The use of ultra-wideband (UWB) technology in new sensing and imaging systems is expanding rapidly. Emerging UWB systems are employed in medical sensing and diagnostics [1]–[4], security and surveillance [5]–[10], non-destructive testing [11], and ground penetrating radar (GPR) [12]–[15] applications, operating in various frequency bands from 100 MHz to 10.6 GHz [16]. These applications favor the safe non-ionizing radiation in the low-GHz electromagnetic spectrum, along with its good penetration and the UWB emissions spread over a large bandwidth [17].

Here, we focus on the direct time-domain UWB receivers, which aim to capture the time-dependent signal directly, i.e., without down-conversion. This functionality, similar to that of high-speed oscilloscopes, is needed in pulsed radars developed for sensing and imaging applications. Its advantage is the fast measurement, while providing instantaneous broadband magnitude and phase information. These receivers employ architectures fundamentally different from the frequency-domain continuous wave (CW) systems (e.g., based on vector network analyzers (VNAs) and software-defined radios) or the frequency-modulated continuous-wave (FMCW) radar receivers [2], [17]–[22]. The CW and FMCW technologies have matured sufficiently to allow for numerous system on a chip implementations. In contrast, the adoption of UWB direct time-domain receivers for on-chip or low-cost compact systems remains limited.

The likely reasons are the challenges of their miniaturization and the lower accuracy compared to the more mature frequency-domain systems.

Direct sampling UWB receivers require multi-giga-samples per second (GSa/s) rates to sample picosecond-pulse signals. Although bench-top oscilloscopes [23]–[27] and off-the-shelf high-speed analog-to-digital converters (ADCs) [28]–[30] meet the sampling requirements, they are too expensive for low-cost solutions. Bench-top oscilloscopes are also impractical for portable or vehicle-mounted systems, due to their size and weight [31]. As they are general-purpose measurement instruments, they do not support custom radar signal processing, necessitating the measurements' offload to external computing platforms. This offload is prohibitively slow. For compact system realizations, an alternative to the high-cost GSa/s ADCs is provided by the equivalent-time (ET) sampling (or sub-sampling) methods [1], [2], [4]–[9], [31]–[34]. These methods exploit the periodic nature of the pulse train to reconstruct one pulse waveform from a measurement over multiple periods. Nonetheless, the measurement time remains much faster than that in the frequency-domain systems over a wide bandwidth. At the same time, the required sampling rates are lowered by an order of magnitude or more, simplifying the data interfaces and lowering the cost of the employed ADCs.

Direct sampling ET architectures use two types of delay-control circuits to provide a repeatable sequence of precise delays to the ADC clocks: phase-locked loops (PLLs) [1], [4], [6], or programmable delay chips (PDCs) [7], [8]. When re-setting a delay value, the delay-control circuit requires time to adjust and stabilize (or settle). This time must be minimal, ideally orders of magnitude shorter than a pulse period. Otherwise, the pulses during which the circuit settles are missed, leading to longer measurement time. PLL-based networks have superior delay accuracy, but they require a long settling time (on the order of a microsecond [35], [36]) to lock on the clock

signal and adjust the delay. This results in more than 50% of the generated pulses not being utilized [5], [6]. Thus, the PLL-based ET architectures are not preferred in high-speed applications aiming at thousands of measurements per second. On the other hand, the PDC circuits [7], [8] settle very fast (within picoseconds). However, PDCs exhibit deviations from the expected (tabulated) delay values, which depend on the device temperature and can exceed 10 ps [37]–[39]. This is very significant for UWB ET receivers, which realize sampling steps in the range of 10 ps to 50 ps [40].

Here, we propose a reconfigurable, dual-channel, low-cost UWB equivalent-time sampling receiver (ETSR), controlled by a field-programmable gate array (FPGA). It realizes a simultaneous ET sampling rate of 20 GSa/s on both channels, and an instantaneous bandwidth from below 1 MHz to 6 GHz without down-conversion. Prior architectures [3], [5]–[8], [11], [12] can not realize this bandwidth, leading to the need for homodyne or heterodyne down-conversion with basebands up to ∼2 GHz. Direct ET sampling has been implemented in integrated-circuit prototypes [1], [4] with higher upper-frequency limits of 9 - 10 GHz, but they are limited in their lower frequencies to ~ 2 GHz. The direct time-expansion method has been proposed [34] to extend the instantaneous bandwidth beyond ~ 2 GHz with ET sampling rate of 20 GSa/s. The limitation of this approach is the limited time window of about 2 ns, where the pulse is captured, while the entire repetition period is as large as 1 μs. Therefore, the method is limited to pulse trains of low duty cycle. In contrast, the proposed ETSR can capture any waveform extending over multiple repetition periods, including sinusoidal waveforms.

Secondly, the proposed ETSR employs a PDC-based architecture to achieve near 100% utilization of the pulse train. For the first time, we investigate and identify drawbacks to the PDC-based architecture and provide a simple yet effective method to correct for PDC-based errors. Specifically, we demonstrate two PDC drawbacks: (i)

the non-uniform sampling timebase, and (ii) the substantial temperature-dependent time-delay inaccuracies, which lead to very significant timebase distortion and errors in the reconstructed signal spectrum. To our knowledge, this investigation has not been carried out before despite its serious implications for the accuracy of the fast PDC-based UWB receivers. We then propose methods to address these drawbacks: (i) the development of a calibration procedure to obtain accurate estimates of the actual PDC delays and, subsequently, an accurate uniform timebase, and (ii) metrics and procedures to assess the system's overall jitter and signal reconstruction accuracy. The calibration procedure exploits the systematic nature of the PDC inaccuracies and employs harmonic signal measurements with the realized receiver system. The method produces highly accurate values for the delays actually realized by the PDC.

The proposed ETSR is paired with a recently developed picosecond pulse generator [41] to demonstrate its operation as a UWB pulsed radar receiver. However, any other pulse generator [42]–[47] or waveform source (sinusoidal or frequency-modulated) can be used, provided it allows for synchronization. This is because the proposed ETSR functions as an accurate high-speed oscilloscope that can be employed in various UWB detection and imaging systems using different excitations. None of the prior systems [3], [5]–[8], [11], [12] have shown the versatility to handle continuous signals (sinusoidal or frequency-modulated). Such capabilities depend on the accuracy of the digitized timebase to ensure the signal continuity from one repetition period to the next. When integrated into a UWB radar system, the proposed dual-channel architecture demonstrates high-speed simultaneous data collection on 4 radar channels (with two transmitting and two receiving antennas), realizing a low-cost compact polarimetric radar. With a unique and efficient data offload strategy [48], the system provides unprecedented speed of over 8 900 4-channel measurements every second. The importance of this advancement is that it enables powerful real-time target detection

and identification based on statistical signal processing techniques, machine learning, and artificial intelligence, all of which require statistically large data sets.

Third, we propose a framework of rigorous performance metrics to evaluate the UWB pulsed-radar receivers. Respective measurement procedures are also proposed. The metrics include receiver bandwidth, spurious free dynamic range (SFDR), time-base distortion, voltage pulse metrics, jitter and noise. The procedure is applied to the proposed ETSR, which is compared with bench-top high-speed oscilloscopes (the golden standard in time-domain receivers). The proposed common framework for the quantitative assessment of time-domain UWB receivers aims to facilitate the system-level UWB radar design, which is dictated not only by the specifics of the application but also by the limitations of the employed hardware. The impact of the limitations of the used electronic components on the receiver performance is also discussed.

The paper is organized as follows. Section 3.2 provides a brief overview of UWB receiver architectures and the types of sampling commonly employed for analog-to-digital conversion. The proposed ETSR architecture, along with the critical improvements in the radio frequency (RF) front-end design, are described in Section 3.3. The performance metrics and the ETSR evaluation are discussed in Section 3.4. Discussion and conclusions are provided in Section 3.5 and Section 3.6.

3.2 PDC-Based Equivalent Time Sampling

3.2.1 Signal Sampling and Reconstruction

The desired 20 GSa/s sampling rate requires a sampling step of $\Delta t = 50$ ps. In ET sampling, the short Δt is achieved by interleaving K sub-sampled waveforms, each containing N samples acquired by an ADC with a sampling period T_{ADC}. The k-th

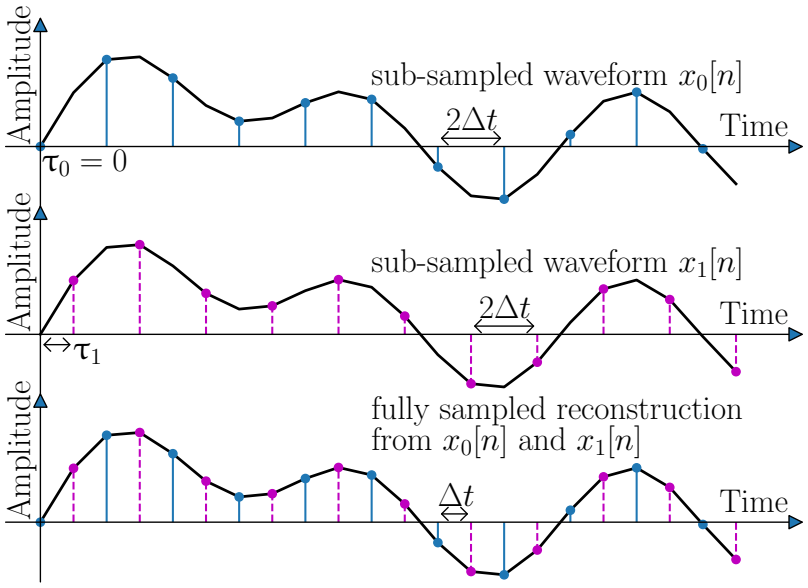


Figure 3.1: Illustration of interleaving two sub-sampled waveforms to produce a single fully sampled waveform reconstruction.

sub-sampled waveform of a signal $x(t)$ is

$$x_k[n] = x(\tau_k + nT_{\text{ADC}}), n = 0, \ldots, N-1, \tag{3.1}$$

where τ_k $(k = 0, \ldots, K-1)$ is the delay determining its start. An example of interleaving two $(K = 2)$ sub-sampled waveforms to produce a waveform with an ET sampling step of Δt is shown in Fig. 3.1.

The PDC (a cascaded network of delay circuits) time-shifts the k-th sub-sampled waveform by the delay τ_k. The PDC is critical for the accuracy of the temporal digitization as it controls the ADC's clocking network. Each delay circuit (referred to as *tap*) is individually enabled or disabled by a binary input. The proposed ETSR PDC [38] provides 10 tap delays (in ps) as shown by the delay vector

$$\mathbf{d} = [4610, 2300, 1150, 575, 290, 145, 70, 35, 15, 10]^{\text{T}}. \tag{3.2}$$

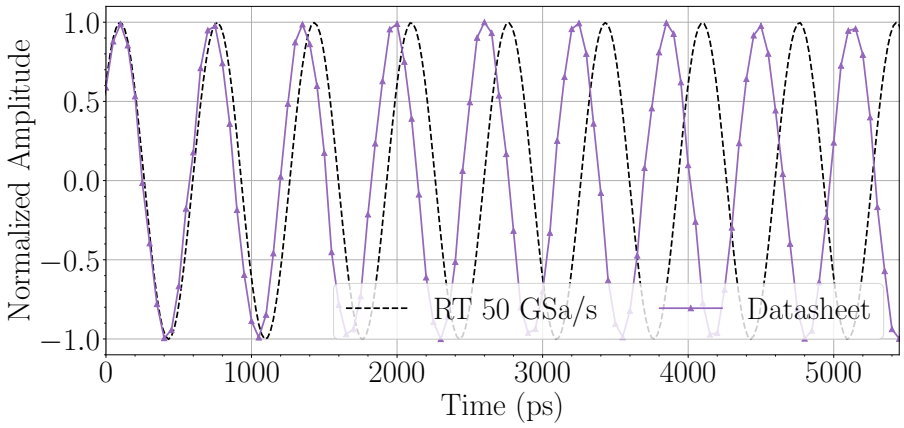
The PDC realizes the delay $\tau_k = \mathbf{c}_k^{\mathrm{T}}\mathbf{d}$, where $\mathbf{c}_k \in \{0,1\}^{10}$ defines the binary inputs controlling the taps. For example, if $\mathbf{c}_k = [0,0,0,0,0,0,0,1,1,0]^{\mathrm{T}}$, then $\tau_k = 50$ ps.

If the delays were all equispaced and the ADC sampled at $T_{\mathrm{ADC}} = 5$ ns, exactly $K = 100$ sub-sampled $x_k[n]$ waveforms are needed to reconstruct $x(t)$, since $K = T_{\mathrm{ADC}}/\Delta t$. However, it is evident from (3.2) that the PDC cannot provide delays equispaced by $\Delta t = \tau_{k+1} - \tau_k = 50$ ps (the desired ET sampling step). For this reason, $K = 110$ sub-sampled waveforms are used to provide a temporal overlap between the samples $\{x_{100}[n] \cdots x_{109}[n]\}$ and the samples $\{x_0[n+1] \cdots x_9[n+1]\}$. The overlap aids the signal interpolation onto an equispaced 50-ps timebase and its smooth transition from one repetition period to the next. The PDC delays are configured to cover tap delays from $\tau_0 = 0$ ps to $\tau_{109} = 5\,450$ ps with increments as close to 50 ps as possible under the constraints of those available in (3.2). In all presented measurements, the system is configured for a repetition period $T_{\mathrm{p}} = 1$ µs, where the waveform in one repetition period is reconstructed from $K = 110$ sub-sampled waveforms, and each sub-sampled waveform contains $N = T_{\mathrm{p}}/T_{\mathrm{ADC}} = 200$ samples.

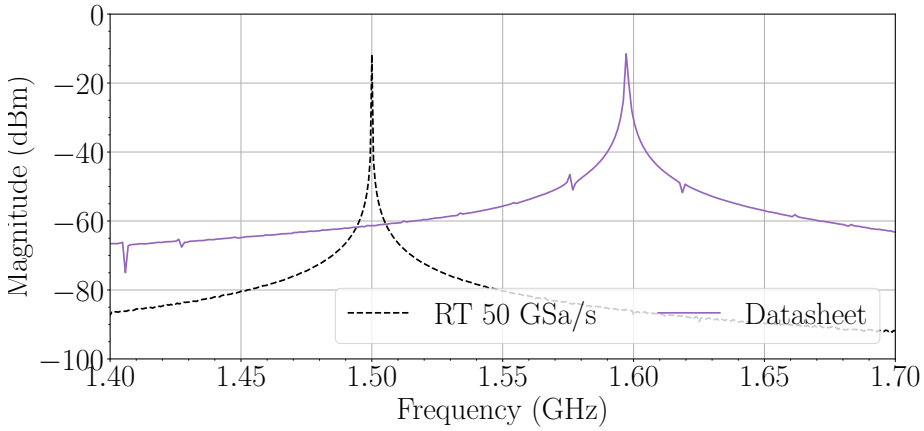
3.2.2 Timebase Distortions in PDC-based Receivers

The delays from (3.2) are used to form the digitized timebase $t_k[n] = \tau_k + nT_{\mathrm{ADC}}$ for the ET-sampled waveform. When the PDC-controlled delays τ_k deviate from their nominal (or tabulated) values, the samples' actual temporal positions differ from the expected ones. The deviation is mostly systematic, i.e., all realized delays are either longer or shorter than the nominal ones, depending on the device temperature [37]–[39]. This results in the timebase stretching or shrinking, leading to unacceptable errors in the spectrum of the recovered signal.

For illustrative purposes, we feed a 1.5-GHz sinusoidal signal from a precision RF



(a)



(b)

Figure 3.2: A 1.5-GHz sinusoidal waveform sampled by the proposed ETSR and a 50-GSa/s real-time (RT) oscilloscope: (a) time-domain plot, (b) magnitude-spectrum plot. Here, the proposed ETSR uses the timebase generated from the PDC nominal (datasheet) delay values.

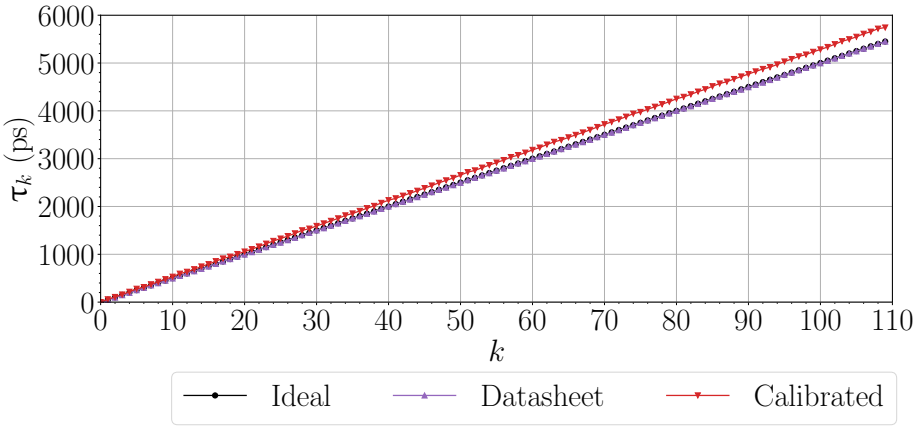
generator [49] to the proposed ETSR to produce the waveform labeled "Datasheet" in Fig. 3.2a. For reference, we also plot the same signal when sampled by a 50-GSa/s RT oscilloscope [50]. The ETSR output appears "shrunk" compared to the reference—a result of longer than expected delays. Fig. 3.2b shows the magnitude spectrum of the sampled 1.5-GHz waveforms. The incorrect timebase of the ETSR output leads to an error in the estimated waveform frequency of almost 100 MHz. Such errors are unacceptable in radar sensing relying on spectral analysis. It is thus imperative to quantify and correct the timebase distortion in PDC-based ET sampling receivers.

3.2.3 Calibration of the Timebase

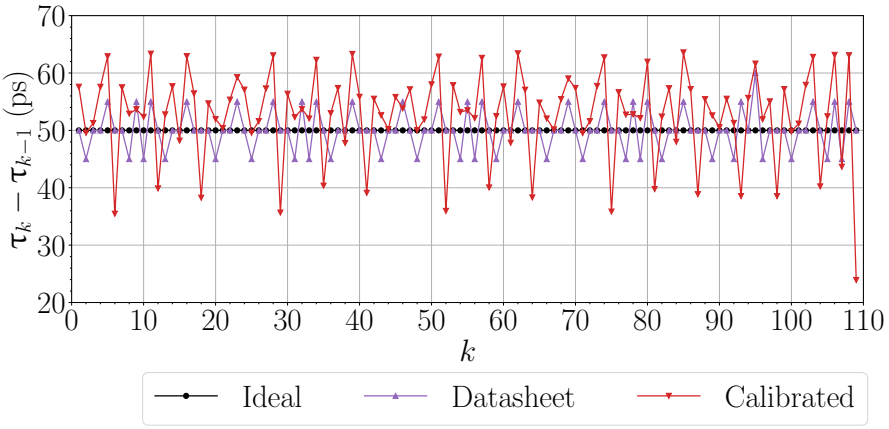
Here, we propose a simple yet effective calibration method to determine the actual tap delays τ_k $(k = 0, \ldots, K-1)$ provided by the PDC to the ETSR. The actual (nonuniform) timebase $t = \tau_k + nT_{\mathrm{ADC}}$ is then calculated using the actual tap delays instead of their nominal (datasheet) values, followed by the signal interpolation onto a uniform 50-ps timebase.

The calibration employs the measurement of a harmonic signal with the ETSR at any frequency below $0.5f_{\mathrm{s}}$, where $f_{\mathrm{s}} = 1/T_{\mathrm{ADC}}$. The input signal must be provided by a precise RF generator so that the frequency is known accurately. The procedure and the algorithm [40] extracting the actual τ_k values are described in detail in Section 3.A.

Fig. 3.3a illustrates the ideal τ_k delays for a uniform $\Delta t = 50$ ps timebase, the delays provided by the PDC according to the datasheet values, and the actual delays extracted by the proposed calibration method. It is observed that the nominal PDC delays are properly selected to closely match the ideal delays. However, the actual delays provided by the PDC are longer than the nominal ones, leading to the "shrinking" effect observed in the sinusoidal signal in Fig. 3.2a. Fig. 3.3b shows the step sizes



(a)



(b)

Figure 3.3: PDC timebase error in terms of: (a) tap delays, (b) step sizes between consecutive tap delays. In (a), the "Ideal" slope is 50 ps per k. The "Ideal" and "Datasheet" traces overlap visually but are not identical.

between consecutive delay settings. Compared to Fig. 3.3a, it shows better that the nominal PDC delays are spaced by nonuniform steps not always equal to 50 ps, but on average providing the desired 50 ps interval. The actual delays clearly exhibit an averaged tendency toward larger than 50 ps interval from one tap delay to the next.

As mentioned earlier, the PDC delay deviations are temperature dependent. To capture this dependence, the ETSR was set in a calibration mode with a sinusoidal signal for over 350 consecutive hours without interruption, where the PDC delays were estimated every minute. At each delay estimation, the temperature was also collected through an onboard temperature sensor. A total of 20 694 actual-delay estimates were obtained. Scatter plots of all delays τ_k *versus* the board temperature have been generated to provide insight into the temperature dependence of the PDC deviations. Fig. 3.4 presents the results for τ_1 (Fig. 3.4a) and τ_{109} (Fig. 3.4b). The dotted line is a first-degree polynomial fit to the data. It is observed that the PDC's delay deviations from the nominal values grow as the delays get longer (more enabled tap delays). Also, the longer delays exhibit near-linear dependence on temperature. Overall, the delay deviations may be as small as 7.4 ps for a nominal 50 ps delay, and as large as 290 ps for a nominal 5450 ps delay. This is significant, as the proposed ETSR employs an ET sampling step of 50 ps.

The beneficial effect of the timebase calibration is illustrated in Fig. 3.5, which shows the same 1.5-GHz sinusoidal waveform of Fig. 3.2 after the calibration. Now, the temporal and spectral plots show excellent agreement between the ETSR output and that of the 50-GSa/s RT oscilloscope.

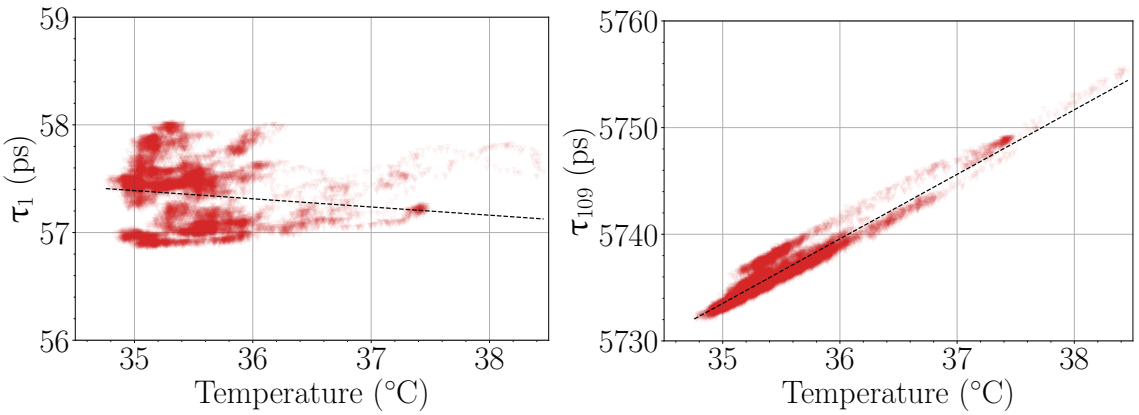
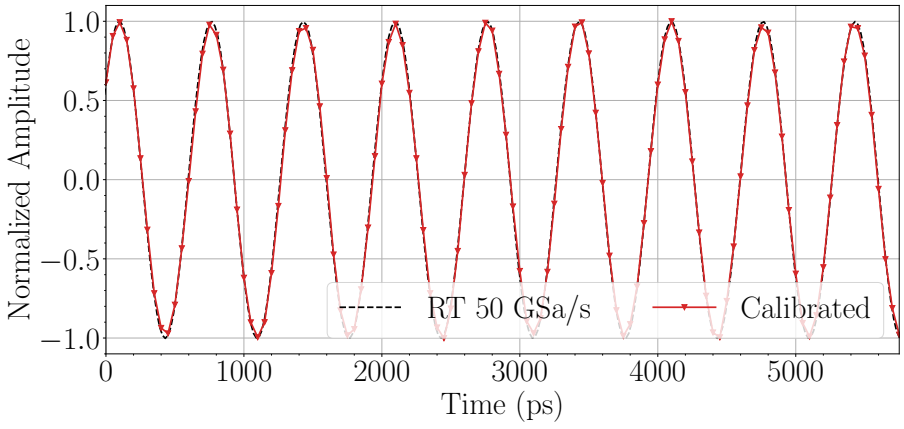
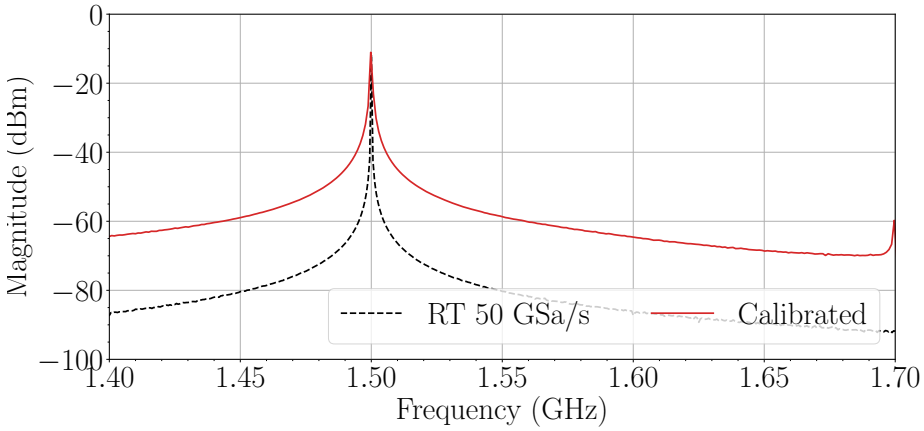


Figure 3.4: Scatter plots of tap delays *versus* board temperature: (a) τ_1 (nominal value of 50 ps), (b) τ_{109} (nominal value of 5 450 ps). The black dotted line is a first-degree polynomial fit.



(a)



(b)

Figure 3.5: A 1.5 GHz sinusoidal waveform sampled by the proposed ETSR with the timebase calibration enabled and a 50-GSa/s RT oscilloscope: (a) time-domain plot, (b) spectral plot.

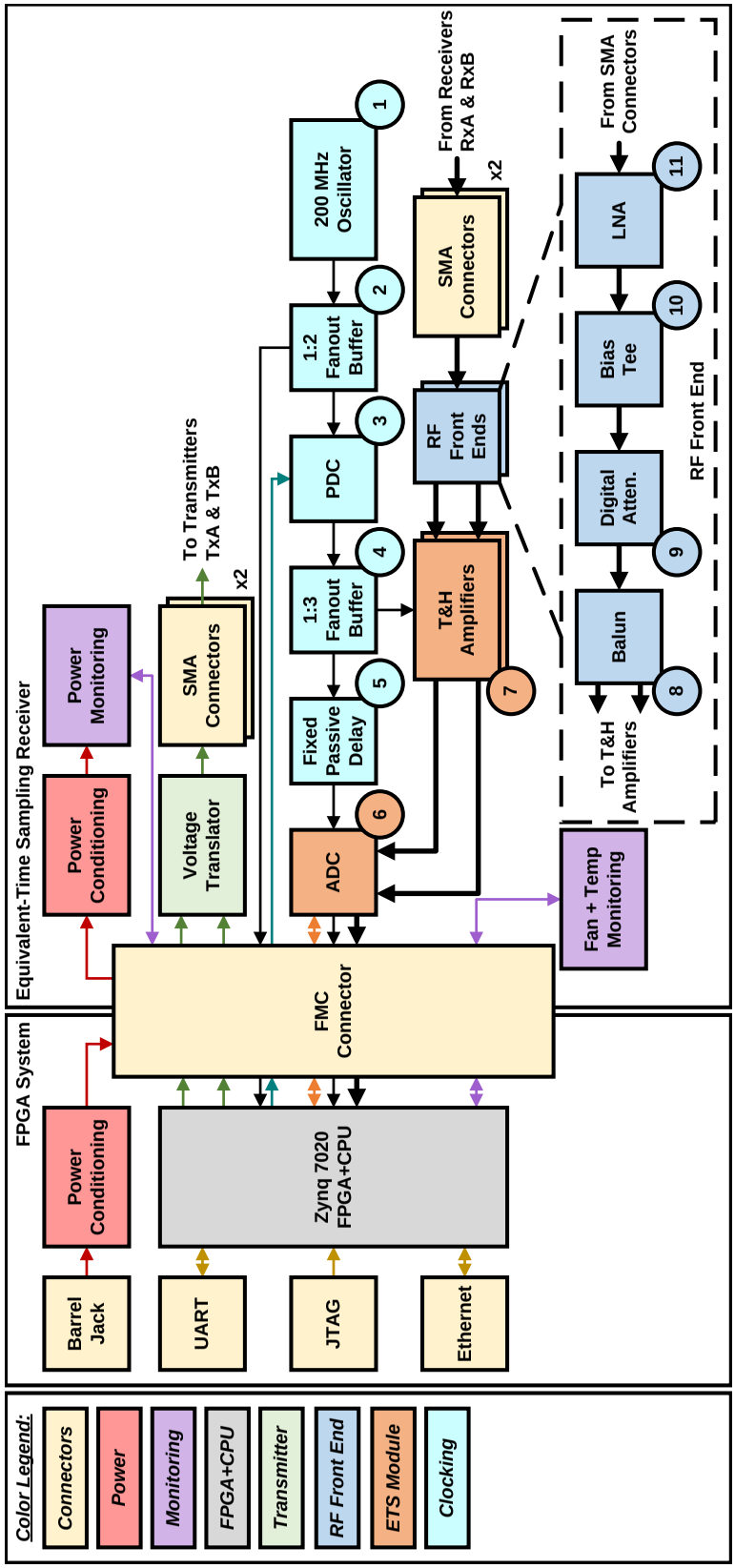


Figure 3.6: High-level UWB equivalent-time sampling receiver (ETSR) block diagram. The colour legend located on the left side helps to identify the functionality of the ETSR. The numbered item corresponds to the chips in Fig. 3.7.

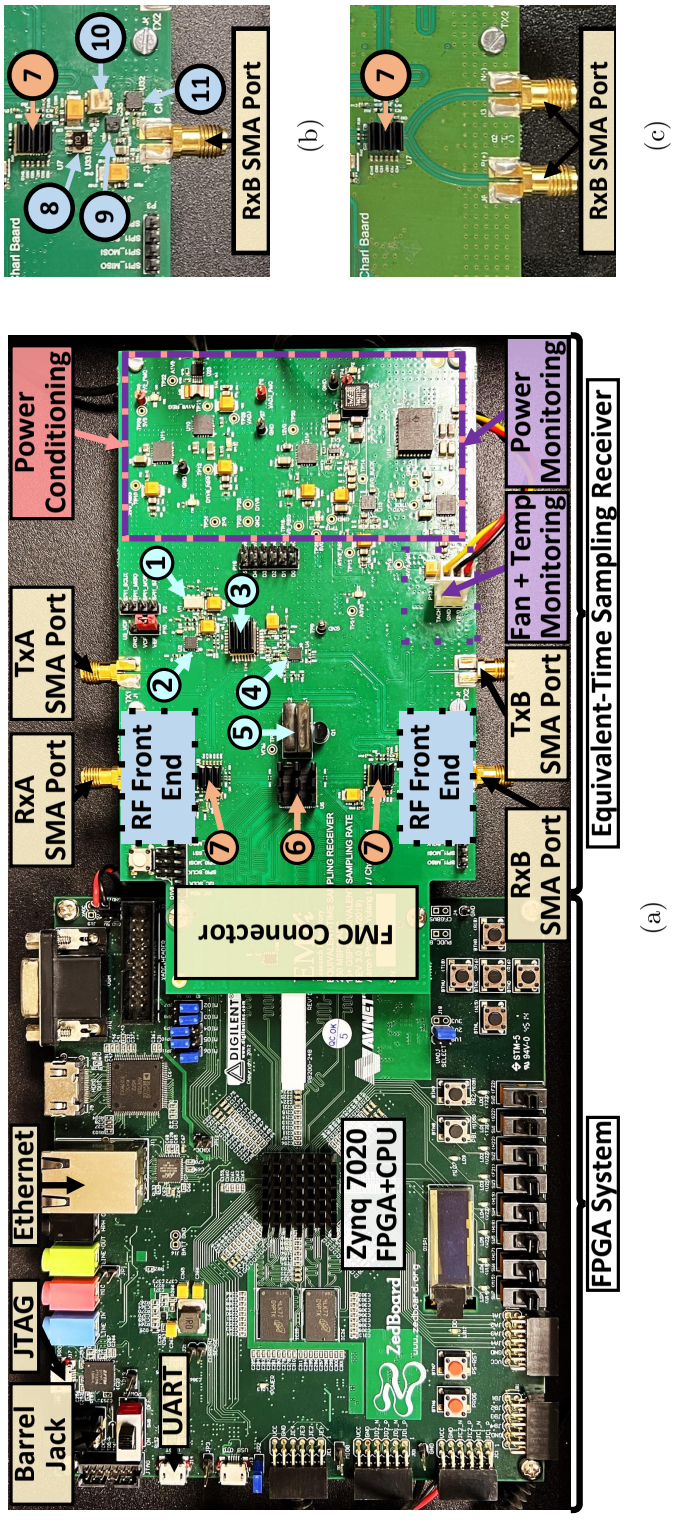


Figure 3.7: ETSR prototype in the enclosure with the FPGA (left) and ETSR (right) boards interfaced through the FMC connector. The numbered items correspond to those in Fig. 3.6. (b) Front-end prototype with RF circuitry. (c) Front-end prototype containing only a track and hold (T&H) amplifier chip and two coaxial (SMA) connectors leading to an external balun and the antenna.

3.3 Dual-Channel ETSR System Design

A high-level system block diagram and the fabricated prototype of the proposed dual-channel receiver are shown in Fig. 3.6 and Fig. 3.7a, respectively. The circled item numbers in Fig. 3.6 correspond to those in Fig. 3.7. The custom ETSR (right side in Fig. 3.6) is integrated with an FPGA board [51] (left side in Fig. 3.6) through an FPGA mezzanine card (FMC) 160-pin connector. The programmable logic of the FPGA configures and controls the ETSR [48]. A single 12 VDC source powers the FPGA board, which has its own power-conditioning circuitry to power the ETSR board through the FMC connector. The ETSR has its own circuitry to monitor and regulate the onboard voltage rails, along with temperature monitoring and control. A voltage translator provides a reference trigger from the FPGA to two transmitting (Tx) modules (through the TxA and TxB ports) for synchronization with the dual-channel receiver inputs (RxA and RxB ports).

In the following, we focus on the design of the two main modules: (i) time-sampling module and (ii) RF front-end.

3.3.1 Equivalent-Time Sampling Module

With reference to Fig. 3.6, the RF front-ends of the two channels (items 8 to 11) provide the input signals to the respective T&H amplifiers [52] (item 7), whose output signals are submitted to the dual-channel 16-bit ADC [53] (item 6). The T&H amplifiers play a critical role in the proposed architecture. They extend the ADC's 900 MHz analog bandwidth [53], thus enabling the reception of GHz-range signals. Here, the selected T&H amplifier has a bandwidth of 5 GHz at the 3-dB level, which ensures accurate sampling at and below this frequency limit. It also provides the

required differential (balanced) signal input to the ADC. The two channels (RxA and RxB) are identical and mirrored symmetrically across the circuit board; see Fig. 3.7a. The ADC submits the digitized signals to the FPGA through a high-speed differential data bus and the FMC connector.

A 200-MHz ultra-low-jitter oscillator [54] (item 1) provides the reference for the entire clocking network. It features 80 femtoseconds of root-mean-square (RMS) jitter and is critical for achieving: (i) the sampling temporal stability and (ii) the timebase accuracy for high-frequency signal reconstruction. In an early prototype [9], a voltage-controlled oscillator [55] proved inadequate with 0.85 picoseconds of RMS jitter for the required sampling stability. The overall sampling circuitry must accurately place a voltage sample within the proper ET temporal bin (here 50 ps wide). To achieve this, the total system peak-to-peak jitter must be smaller than the ET sampling step, as this jitter measures the maximum timing error for each temporal sample. Prior work on ET sampling architectures accounts only for the RMS jitter of the employed clocks, which, for off-the-shelf components, is provided by the manufacturer. However, the peak-to-peak jitter is significantly larger. It can be estimated by applying the "crest factor" of ~ 14 to the RMS jitter value [56]. Additionally, the compounded jitter of the entire sampling circuit is always higher than the jitter of the individual clocks it employs. This is why selecting a reference clock for ET sampling circuit with an RMS jitter at least two orders of magnitude lower than the ET sampling step, is critical.

A 1:2 fan-out buffer [57] (item 2) distributes the reference clock to the FPGA and the PDC. The FPGA uses the reference clock for Tx synchronization and for the internal logic. The PDC (item 3) controls the delays applied to the ADC clock. Another 1:3 fan-out buffer [58] (item 4) distributes the delayed clock to the two T&H amplifiers (item 7) and, through a fixed 500-ps passive delay [59] (item 5), to the ADC (item 6). The arrival times of the clock signals must ensure that the ADC sampling

occurs during the hold stage of the T&H amplifiers [9]. All clocking traces are 100-Ω differential microstrip transmission lines. Their design must be precise to ensure the desired delays while accounting for the internal chip delays in the T&H amplifiers and the ADC.

3.3.2 RF Front-End Design

The RF front-ends of the dual-channel ETSR ensure the reception of weak scattered signals and transform the unbalanced antenna outputs to the T&H amplifier differential (balanced) inputs. The RF front-end (items 8 to 11) is shown in the dash-box inset of Fig. 3.6. The RF circuit with a low noise amplifier (LNA) is shown in Fig. 3.7b. The RF interconnects are 50-Ω co-planar waveguides (CPWs), which feed a wideband LNA [60] (item 11) with an approximate 20-dB gain from 0.5 GHz to 8.0 GHz. The bias tee [61] (item 10) supplies power to the LNA. A digitally controlled attenuator [62] (item 9) prevents T&H amplifier saturation, which is limited to an input peak-to-peak voltage of 1 V (about 4 dBm for a sinusoidal input on a 50-Ω load). The attenuation control is necessary because the LNA's 1-dB compression point is 16 dBm, which exceeds the T&H amplifier saturation limit. A chip balun [63] (item 8) connects the attenuator's output to the T&H amplifier.

To evaluate the receiver's performance without the bandwidth limitations imposed by the LNA, a second front-end prototype is fabricated (see Fig. 3.7c) without an LNA, chip balun and digital attenuator. In this case, the input (equipped with an external balun [64]) connects to the T&H amplifier 100-Ω CPW differential input through two coaxial connectors.

3.4 Proposed UWB Receiver Performance Metrics and ETSR Evaluation

The proposed performance metrics are based on two types of input signals: (i) sinusoidal, and (ii) UWB pulse. The sinusoidal waveforms must be generated by a high-fidelity RF generator [49]. Similarly, the UWB pulsed source must feature low voltage and jitter noise. It also must have a pulse spectrum within the receiver bandwidth, it must provide a sharp transition in the main voltage swing, and its jitter and noise [41] must be known. Here, a high-performance picosecond pulse generator [41] is used, which provides a highly stable approximation of a monocycle pulse often used in compact radar modules [42]–[47].

The performance of the proposed ETSR is compared with two bench-top RT sampling oscilloscopes: a 20-GSa/s oscilloscope [23] and a 50-GSa/s oscilloscope [50].

3.4.1 UWB Receiver Bandwidth: Definition and Evaluation

In current time-sampling receiver research, it is common practice to report the input impedance-match bandwidth [1], [2], [4]–[9], [31]–[34], which is based on measurements of the reflection coefficient $|S_{11}|$. However, this bandwidth reflects only the adequacy of the RF front-end input circuitry, and it does not capture the performance of the sampling circuitry, which, too, has an impact on the bandwidth of the output signal. Here, we propose a receiver-bandwidth metric, which captures the overall system performance.

The bandwidth of the system under test must be evaluated with a sinusoidal input at discrete frequencies f_i, $i = 1, \ldots, N_f$, covering the range of the measured bandwidth. The expected output at the i-th frequency is then of the form

$$\tilde{x}_i[n] = 0.5A_i \cos(2\pi f_i n\Delta t + \phi_i), \tag{3.3}$$

where n is the temporal sample, Δt is the sampling step, A_i is the peak-to-peak voltage, and ϕ_i is the initial phase. The input must ensure that A_i is as large as possible without saturating the RF front-end or the ADC. The receiver bandwidth depends on the extraction of A_i. Similarly to the evaluation of ADCs [65], the results must be averaged over a large number M of measurements. Here, we average the extracted A_i values from $M = 256$ measurements at each i-th frequency.

The bandwidth is determined from the estimated A_i values of the output signal across the measurement bandwidth. To this end, a non-linear least-squares curve fitting [66] algorithm is used, which minimizes the residual error

$$r_i = \sum_{n=1}^{N} \left(\tilde{x}_i[n] - y_i[n]\right)^2, \tag{3.4}$$

where $y_i[n]$ is a four-parameter function defined similarly to a model recommended in [65]:

$$y_i[n] = \alpha_i \cos(2\pi\nu_i n\Delta t) + \beta_i \sin(2\pi\nu_i n\Delta t) + \gamma_i. \tag{3.5}$$

The optimizable parameters are $\alpha_i, \beta_i, \gamma_i$ and ν_i. With these found, the peak-to-peak voltages are computed as

$$A_i = \max_n(y_i[n]) - \min_n(y_i[n])\,. \tag{3.6}$$

Then, they are normalized and converted to decibels:

$$A_i^{\mathrm{dB}} = 20\log_{10}\left(\frac{A_i}{\max_i(A_i)}\right). \tag{3.7}$$

The receiver bandwidth B is determined at the frequencies where A_i^{dB} drops below a specific threshold α_{dB}:

$$B = f_{\mathrm{u}} - f_{\mathrm{l}} \ \text{ s.t. } A_i^{\mathrm{dB}}|_{f_{\mathrm{l}} \le f_i \le f_{\mathrm{u}}} \ge -\alpha_{\mathrm{dB}}\,, \tag{3.8}$$

where f_{l} and f_{u} are the lower and upper cut-off frequencies. Here, we employ the 10-dB threshold, which is common in UWB technology. Note that the bandwidth of test instruments may need to be characterized with a 3-dB threshold.

In the bandwidth measurements carried out here, the RF generator is connected to one of the ETSR inputs (RxA or RxB port in Fig. 3.7a), or to the oscilloscope input. The RF generator produces a pure sinusoidal tone with -10 dBm power. A total of 43 discrete frequencies ($N_f = 43$) are used between 1 MHz and 10 GHz. Similarly to the procedures for evaluating ADCs [65], these frequencies, f_i, must be chosen such that they are not multiples of the ADCs sampling rate ($f_{\mathrm{s}} = 200$ MHz). The ETSR trigger port (TxA or TxB port in Fig. 3.7a) is configured by the FPGA as a synchronized 10-MHz reference. When the ETSR equipped with an LNA is measured, its digital attenuator is set to 12 dB of attenuation to offset the LNA gain. When measuring the bench-top oscilloscopes, a 10-MHz rubidium standard [67] provides the synchronized 10-MHz reference to the oscilloscopes and the RF generator. Note that the 3-dB cut-off frequencies of the 20-GSa/s and 50-GSa/s oscilloscopes are stated as 6 GHz and 16 GHz, respectively [23], [50].

Fig. 3.8 shows the plot of A_i^{dB} *versus* frequency for the two ETSR prototypes (with and without an LNA). The bandwidth B is determined at the 3-dB and 10-dB levels, along with the lower and upper cut-off frequencies. These are listed in Table 3.1. For comparison, the results for the RT oscilloscopes are also presented in Fig. 3.8 and Table 3.1. The estimates of their respective 3-dB bandwidths agree

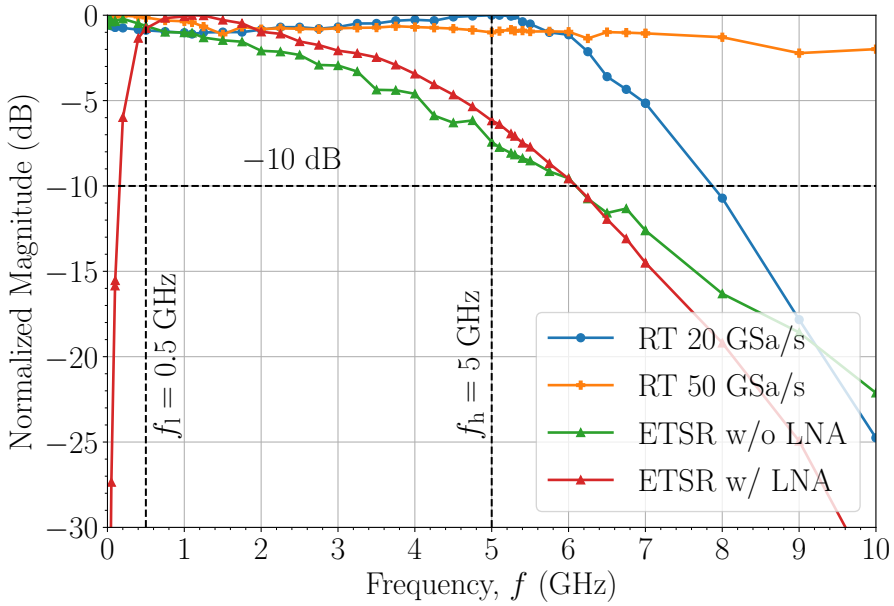


Figure 3.8: ETSR receiver bandwidth results along with the results for the bench-top RT oscilloscopes.

with the manufacturers' specifications (∼6 GHz for [23] and ∼16 GHz for [50]). The 10-dB bandwidth of the ETSR without an LNA ranges from $<$ 1 MHz to about 6.1 GHz, whereas with an LNA it ranges from 159 MHz to about 6.1 GHz. Both designs successfully cover the desired 10-dB bandwidth from 500 MHz to 5 GHz, with the lower cut-off frequency of the ETSR without an LNA being well below 1 MHz.

It is worth noting that the input-impedance bandwidths of the measured ETSR prototypes are entirely determined by the employed RF front-end components. Specifically, the input-impedance bandwidth of the ETSR without LNA (dictated by the balun [64]) is from 200 kHz to 10 GHz, whereas that of the ETSR with LNA (dictated by the balun [63] and the LNA [60]) is from 0.5 MHz to 6.0 GHz. Yet, the receiver bandwidths of both prototypes, when evaluated in accordance with the proposed metric, is limited to $\sim$ 6 GHz.

Table 3.1: Sinusoidal metrics for the ETSR with and without the LNA *versus* the RT oscilloscopes.

Metric	ETSR w/o LNA	ETSR w/ LNA	20 GSa/s scope [23]	50 GSa/s scope [50]
$f_{\mathrm{l,3dB}}$ (MHz)	< 1	330	< 1	< 1
$f_{\mathrm{h,3dB}}$ (GHz)	3.039	3.795	6.399	> 10
B_{3dB} (GHz)	3.038	3.465	6.398	> 10
$f_{\mathrm{l,10dB}}$ (MHz)	< 1	159	< 1	< 1
$f_{\mathrm{h,10dB}}$ (GHz)	6.095	6.096	7.873	> 10
B_{10dB} (GHz)	6.094	5.937	7.872	> 10

3.4.2 SFDR Definition and Evaluation

Similarly to the definition in [65] for ADCs, the spurious free dynamic range (SFDR) of a time-sampling receiver can be defined as the difference in strength between the output spectral component at the input frequency and the next largest spurious or harmonic output component. Harmonics are spectral components at multiples of the input frequency, whereas spurious components are persistent sinusoids at frequencies other than the input frequency and its harmonics. The SFDR defines the receiver's dynamic range where a signal can be distinguished from the receiver's noise and spurious output.

The SFDR at each frequency f_i, SFDR_i, is determined from the (discrete-time) Fourier transform of the signal $\tilde{x}_i[n]$ at the receiver's output when the input is:

$$X_i(f) = \sum_{n=0}^{N-1} \tilde{x}_i[n] e^{-j2\pi f n \Delta t}. \tag{3.9}$$

In practice, $X_i(f)$ is obtained via the fast Fourier transform (FFT). The calculation of SFDR_i needs only the magnitude spectrum $|X_i(f)|$. However, this magnitude spectrum must be averaged over M measurements [65], i.e., $\bar{X}_i(f) = (1/M) \sum_{m=1}^{M} |X_{i,m}(f)|$.

Here, $M = 1024$. The SFDR is then determined in dBc (dB relative to carrier) as [65]:

$$\mathrm{SFDR}_i = 20\log_{10}\left(\frac{\bar{X}_i(f_i)}{\max\left(\bar{X}_i(\mathbf{f}_{\mathrm{h},i}), \bar{X}_i(\mathbf{f}_{\mathrm{s}})\right)}\right). \tag{3.10}$$

Here, $\mathbf{f}_{\mathrm{h},i}$ is the vector of all frequencies harmonic in f_i, and $\mathbf{f}_{\mathrm{s}}$ is the vector of all frequencies excluding f_i and $\mathbf{f}_{\mathrm{h},i}$.

This evaluation uses the same measurement setup as described for the receiver bandwidth. It is performed on both versions of the ETSR (with and without an LNA) and the two RT oscilloscopes for comparison.

The SFDR results are shown in Fig. 3.9. The two vertical dash lines delineate the 0.5 GHz to 5 GHz band of interest. The ETSR without an LNA aligns well with the RT sampling oscilloscopes up to 2 GHz, where the SFDR measures at or above 40 dBc. Beyond 2 GHz, the SFDR begins to linearly decrease to 20 dBc at 5 GHz. The ETSR with an LNA circuitry shows worse SFDR performance over the entire band of interest. An investigation has identified the cause to be the imperfect linearity of the LNA. As we decrease the input power (initially set at -10 dBm), while maintaining the same attenuator and ADC settings, the SFDR performance improves and tends to that of the ETSR without the LNA circuitry.

3.4.3 Evaluation of UWB Receiver Pulse Metrics

UWB pulse metrics have been proposed in [41] to evaluate picosecond pulse generators. This methodology is also applicable to the evaluation of the received pulses reconstructed by time-domain measurement systems, namely: peak-to-peak voltage V_{pp}, full-width half maximum (FWHM) pulse width τ_{FWHM}, lower f_{l} and upper f_{u} cut-off frequencies at the -10 dB level, pulse bandwidth B_{p}, and fractional bandwidth ratio b_{fr}. The receiver pulse metrics for different systems can be used to compare their

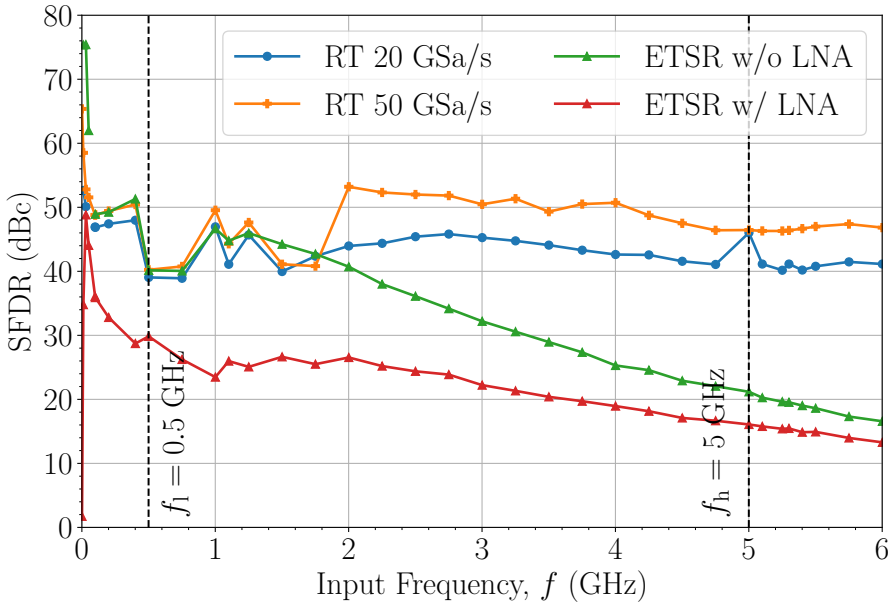


Figure 3.9: SFDR *versus* frequency of the proposed ETSR with and without the LNA, alongside the SFDR of the bench-top high-speed oscilloscopes.

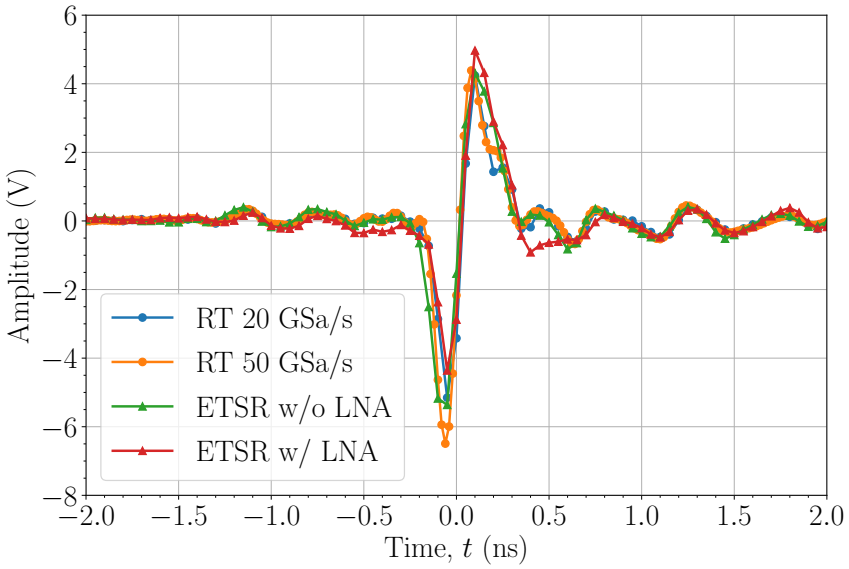
time-domain accuracy. Here, we apply these metrics to compare the performance of the proposed ETSRs and the RT oscilloscopes. The 50-GSa/s oscilloscope serves as the reference due to its highest sampling rate.

The measurement procedure must employ a pulse input approximating a mono-cycle waveform whose bandwidth is within the receiver's bandwidth. Here, we use the pulse generator in [41] since its pulse spectrum is confined between 500 MHz and 5 GHz at the -10 dB level. In this measurement, directional couplers are needed to connect the Tx output to the receiving systems because the Tx peak-to-peak voltage is high ($\sim$10 V). The ETSR without an LNA and the RT oscilloscope measurements employ a 10-dB directional coupler [68], where the receivers are connected to the coupled port while the through port is terminated with a 50-Ω load. The ETSR with LNA measurement employs two cascaded directional couplers [68], [69] with 30-dB overall attenuation. The additional 20-dB attenuation counteracts the LNA gain,

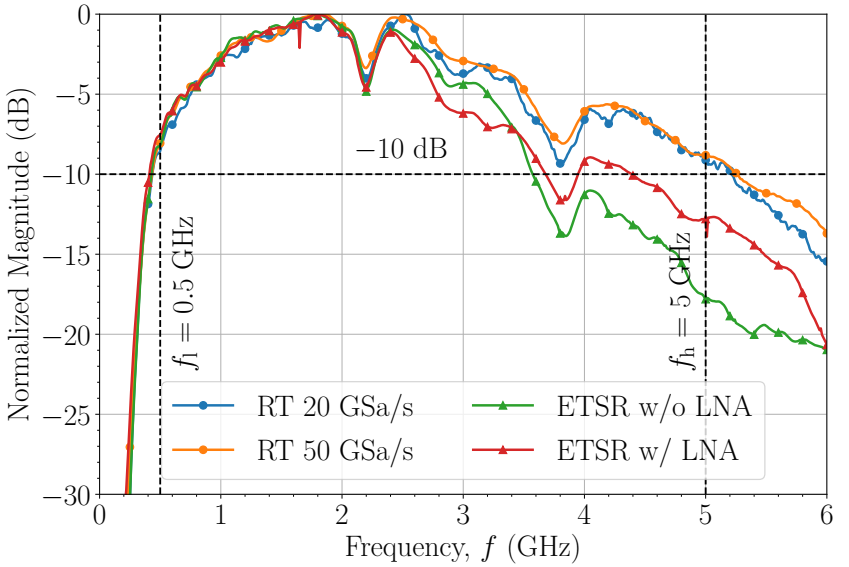
thus providing approximately the same signal strength at the ADC input as that in the ETSR without an LNA. In the oscilloscope measurements, the 1-MHz trigger for the pulse generator is provided by the arbitrary waveform generator built in the oscilloscope [23]. In the ETSR measurements, the FPGA produces the 1-MHz trigger. The pulses are averaged over $M = 256$ measurements.

The impact of the directional couplers on the measured waveforms is de-embedded using their measured scattering (S) parameters. These are measured with a VNA [70]. The de-embedding procedure employs the $ABCD$ matrix of a two-port device [71]. It is summarized in Section 3.B. To de-embed the impact of the on-board digital attenuator from the measurements with the ETSR with an LNA, its 12-dB attenuation is converted to the scaling factor $10^{12/20}$ applied to the voltage. Note that this attenuation is guaranteed to be constant across the band [62].

Fig. 3.10 presents the de-embedded temporal and spectral plots of the pulse sampled by the ETSRs and the oscilloscopes. The pulse metrics are listed in Table 3.2. It is evident that the ETSR performance yields similar results to the 20-GSa/s RT oscilloscope. The 50-GSa/s RT oscilloscope produces the most accurate result, which is best observed in Fig. 3.10a. Therein, the peak-to-peak voltage in the waveform sampled at 50 GSa/s is visibly larger than that registered by the ETSRs and the 20-GSa/s oscilloscope. The spectral plots in Fig. 3.10b indicate that the ETSRs do not capture well the pulse energy above 3.5 GHz, resulting in a narrower pulse bandwidth compared to that obtained with the 20- and 50-GSa/s RT oscilloscopes. This high-frequency roll-off is expected given the higher power loss above 3.5 GHz observed in the ETSR's receiver bandwidth discussed in Subsection 3.4.1 and plotted in Fig. 3.8. The suboptimal high-frequency performance of the ETSR is not due to deficiencies in the architecture but the bandwidth limitations of the chosen components. For example, it is evident from the response of the ETSR without an LNA, shown in Fig. 3.8,



(a)



(b)

Figure 3.10: Pulse comparison between ETSR and RT oscilloscopes. (a) Time-domain plot of the measured plot when acquired using the 20-GSa/s (blue-circle) and 50-GSa/s (orange-circle) oscilloscope along with the ETSR with the LNA (red-triangle) and without (green-triangle). (b) The respective frequency-domain plot of the acquired pulse.

Table 3.2: Pulse metrics obtained with the ETSR with and without the LNA *versus* the RT oscilloscopes.

Metric	ETSR w/o LNA	ETSR w/ LNA	20 GSa/s scope [23]	50 GSa/s scope [50]
V_{pp} (V)	9.674	9.329	9.390	10.878
τ_{FWHM} (ps)	350	250	250	240
f_{l} (GHz)	0.403	0.420	0.440	0.438
f_{u} (GHz)	3.580	3.680	5.220	5.263
B_{p} (GHz)	3.150	3.260	4.780	4.825
b_{fr}	8.326	8.762	11.864	12.029

that the culprit is the T&H amplifier (analog 3-dB bandwidth of 5 GHz) and the interconnect circuit between the T&H amplifier and the ADC. By swapping the T&H amplifier with a pin compatible alternative with an 18 GHz analog 3-dB bandwidth [72], our preliminary findings indicate the ETSR receiver bandwidth improves by $\sim$3 dB at 5 GHz. Therefore, it is recommended that these components' choices feature analog bandwidths exceeding significantly the desired ETSR bandwidth.

In order to evaluate the measurement similarity between the 20-GSa/s oscilloscope and the ETSR, the cross-correlation between their captured waveforms is calculated. The cross-correlation values for the ETSR with and without an LNA are 93.6% and 91.0%, respectively, indicating very good reconstruction accuracy relative to the 20-GSa/s oscilloscope.

In summary, while the received pulse metrics are related to the frequency-domain performance metrics of the receiver (receiver bandwidth and SFDR), they provide important additional information about the instantaneous power and the output-pulse spectral characteristics actually available for detection and sensing. The proposed comparative evaluation is imperative when pairing a UWB receiver with a pulse generator for a UWB radar system. For example, in the presented evaluation, it is

evident that the spectral bandwidths for both the generator's pulse (see the last column of Table 3.2) and the ETSR's input (see Fig. 3.8) cover well the 500 MHz to 5 GHz bandwidth. However, when paired together, the received pulse spectrum has an upper-frequency limit of ~ 3.6 GHz.

3.4.4 Jitter Definition and Evaluation

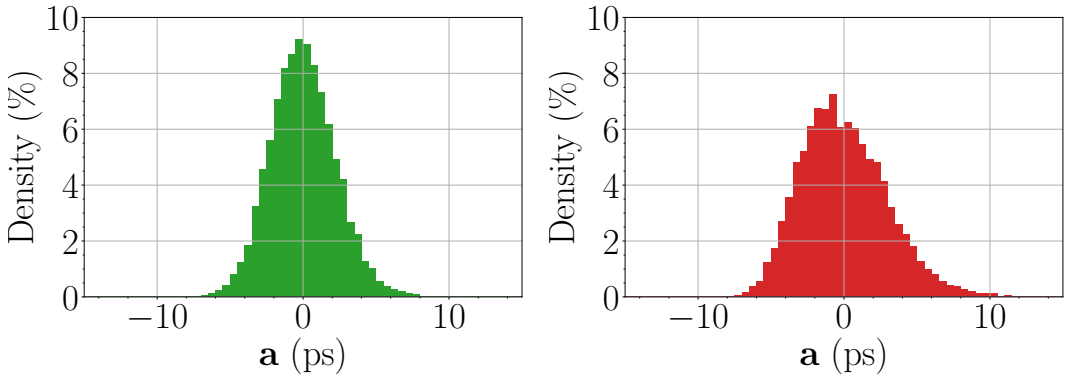
The output of a UWB pulse generator does not have clock-like rising and falling edges. Nonetheless, the jitter of a received monocycle pulse can be evaluated using the approach proposed in [41]. The jitter definition employs the ideal pulse period, here determined by the FPGA output trigger, $T_{\mathrm{p}} = 1$ µs. The absolute pulse jitter is a discrete-time random sequence $\mathbf{a}$, the m-th element of which, a_m, is defined as:

$$a_m = t_m - mT_{\mathrm{p}}\,,\ m = 0, \ldots, M-1, \tag{3.11}$$

where t_m is the time instance where the pulse voltage crosses the 0-V reading while swinging from the minimum to maximum peaks. Since $\mathbf{a}$ describes a random process, a large number of waveforms is needed to perform the analysis. Here, $M = 10\,000$ waveforms are collected.

Additionally, the temporal position of the zero crossing must be determined accurately. Let $n_{\min}$ and $n_{\max}$ denote the time samples where the minimum and maximum peaks, $x_{\min} = \tilde{x}[n_{\min}]$ and $x_{\max} = \tilde{x}[n_{\max}]$, occur. A search in the interval $[n_{\min}, n_{\max}]$ finds the two samples, $\tilde{x}[n_{0_-}]$ and $\tilde{x}[n_{0_+}]$, between which the zero-crossing occurs. A line-segment intersection algorithm [73] uses linear interpolation between these samples to locate the zero-crossing t_m. A probability distribution function (PDF) histogram of the random sequence $\mathbf{a}$ is then created from the M waveforms.

This histogram provides three jitter metrics. (i) The *standard deviation jitter* σ_j



(a) (b)

Figure 3.11: Histograms of the ETSR absolute jitter measured with UWB pulse generator: (a) ETSR without LNA, and (b) ETSR with LNA.

Table 3.3: Evaluation of ETSR absolute jitter with UWB pulse.

a	ETSR w/o LNA	ETSR w/ LNA	20 GSa/s scope [23]	50 GSa/s scope [50]	UWB Pulse [41]
σ_j (ps)	3.110	3.876	1.729	2.062	1.653
$6\sigma_j$ (ps)	18.662	23.258	10.373	12.373	9.918
$\sigma_{j,\text{pp}}$ (ps)	21.918	23.258	12.978	15.256	11.25

is the histogram's standard deviation. Provided the jitter histogram conforms to a normal (Gaussian) distribution, this is also its RMS value. (ii) The *$6\sigma_j$ jitter* is the histogram's bounded statistical representation at $\pm 3\sigma_j$. (ii) The *peak-to-peak jitter* $\sigma_{j,\text{pp}}$ is the maximum timing error defined by the difference between the maximum and minimum values on the histogram's abscissa.

The jitter measurements employ the same pulse generator and directional-coupler setups explained in Subsection 3.4.3. Averaging must not be used.

The histograms and the metrics generated from the 10 000 waveforms for both ETSRs are presented in Fig. 3.11 and Table 3.3. The two ETSRs exhibit similar jitter, although the system without an LNA is marginally better; see columns 2 and 3 in Table 3.3. Both systems are sufficiently stable to ensure that the samples arrive within

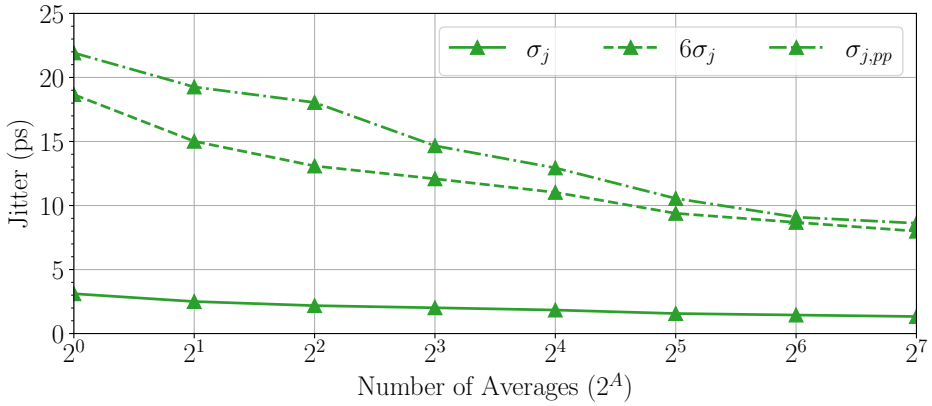


Figure 3.12: Absolute jitter of the ETSR without an LNA *versus* number of averages.

the proper 50-ps temporal bin since the peak-to-peak jitter is 23.258 ps and 21.918 ps for the ETSR with and without an LNA, respectively. Note that the jitter metrics of the generator itself (last column of Table 3.3, taken from [41]), have been obtained with a 50-GSa/s oscilloscope and a 10-MHz rubidium standard, which guarantees very precise synchronization and jitter evaluation.

To make a fair comparison between the proposed ETSRs and the RT oscilloscopes, the measurements with these oscilloscopes (see columns 4 and 5 in Table 3.3) use their own internal clocks. The proposed ET sampling architecture provides excellent jitter performance, which is comparable to the oscilloscopes. The slightly better performance of the RT architecture (which comes at a premium cost) is expected, bearing in mind the impact of the PDC delay uncertainties, the use of multiple pulse periods for waveform reconstruction, and the need for interpolation to recover a uniform 50-ps timebase in the ETSR system. To exemplify the above factors, jitter measurements are performed with the two ETSRs at various 2^A, $A = 1, \ldots, 7$, averaging values. Fig. 3.12 presents the results for the case of the ETSR without an LNA. As the averaging increases, the ETSR jitter decreases. With $2^3 = 8$ and higher averaging, the ETSR jitter becomes equivalent or lower than that of the RT oscilloscopes (without

averaging).

3.4.5 Voltage Noise Definition and Evaluation

The voltage noise is the measure of amplitude uncertainty due to internal noise. As in the case of jitter, a receiver system is expected to add voltage noise to that which is inherently present in the output of the picosecond pulse generator [41]. This noise is stochastic, and it resembles a Gaussian distribution, which can be derived from a large number of measurements (M). Here, $M = 10\,000$.

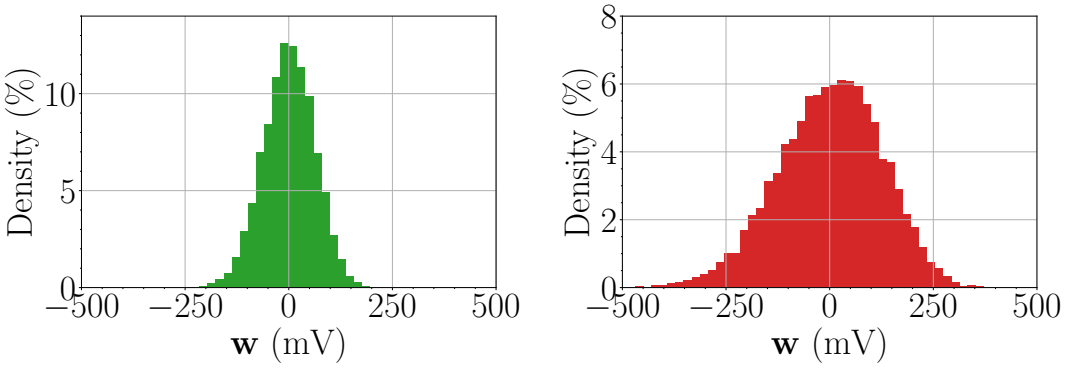
The voltage noise is a discrete-time random sequence $\mathbf{w}$, the m-th element of which, $w_m[n]$, is defined as:

$$w_m[n] = \tilde{x}_m[n] - \bar{x}[n]\,,\ m = 0, \ldots, M-1, \tag{3.12}$$

where $\tilde{x}_m[n]$ is the n-th temporal sample of the m-th measurement, and $\bar{x}[n]$ is the n-th sample in the mean of all M measurements. A PDF histogram of the random sequence $\mathbf{w}$ is then created at the n-th temporal sample. This histogram provides two voltage-noise metrics: (i) *voltage-noise standard deviation* $\sigma_{\mathrm{v},n}$, and (ii) *voltage-noise variance* $\sigma^2_{\mathrm{v},n}$.

The noise measurements are performed with the same pulse generator and directional-coupler setups explained in Subsection 3.4.3. Again, averaging must not be used.

Fig. 3.13 presents the ETSRs worst-case histograms obtained from the voltage values at the time samples where the voltage swings between the pulse minimum and maximum. The distributions of both ETSRs are similar, although the system without an LNA exhibits lower deviation σ_{v}. This is expected because the ETSR with an LNA amplifies the inherent noise in the input pulse, i.e., the voltage noise of the pulse generator itself. The voltage-noise metrics of the two ETSRs and the RT



(a) (b)

Figure 3.13: Histograms of the voltage-noise metric measured with: (a) ETSR without LNA, and (b) ETSR with LNA.

Table 3.4: Worst-case voltage-noise metrics with UWB pulse.

w	ETSR w/o LNA	ETSR w/ LNA	20 GSa/s scope [23]	50 GSa/s scope [50]
σ_{v} (mV)	61.31	124.38	279.09	229.06
σ_{v}^2 ($\mathrm{V}^2 \times 10^{-3}$)	3.76	15.47	77.89	52.470

oscilloscopes are listed in Table 3.4. It is evident that, with this UWB pulse input, the voltage noise of ETSRs is much better than the RT oscilloscopes. This is expected bearing in mind the higher (16-bit) resolution of the employed ADC in our systems compared to the 8-bit ADCs in the RT oscilloscopes.

3.5 Discussion

3.5.1 Design Versatility

We have proposed an accurate high-performance dual-channel ETSR architecture employing T&H amplifiers, a PDC, a dual-channel ADC, and an FPGA control, which synchronizes the ETSR with two UWB transmitters. With two transmitters, the

dual-channel receiver collects data on 4 radar channels, allowing for full polarimetric measurements. The fast PDC settling time enables high pulse repetition rates and very fast measurements. The design of the FPGA-based control and signal processing is beyond the scope of this contribution but is presented in [48]. Importantly, it realizes efficient data offload, which matches the radar speed. Thus, it fully utilizes the available ADC data stream to provide an unprecedented measurement speed of over 8 900 waveforms per second on each of the 4 radar channels, offloaded to a computer for custom signal processing [48].

The architecture has been implemented in two designs, with and without an LNA in the RF front-end. Both prototypes achieve a 1:10 receiver bandwidth at the -10 dB level, where this bandwidth refers to the definition proposed in Subsection 3.4.1, not the RF front-end input impedance bandwidth. A digital attenuation control in the ETSR with an LNA allows for operation with varying input signal strength.

The ETSR's versatility has already been demonstrated by measuring two different types of signals (sinusoidal for calibration and an UWB radar pulse). To exemplify this further, a unit step function from 0 V to 1 V with a fast ~ 100 ps rise time is measured. The unit step function is generated by a 10-GSa/s arbitrary waveform generator (AWG) [74]. Fig. 3.14 presents the measured responses obtained with the ETSR (without LNA) and the two RT oscilloscopes. Note that the ETSR input is alternating current (AC) coupled to the AWG as there is no need for direct current (DC) coupling when connecting to an antenna. The RT oscilloscopes have also been AC coupled. This is why the unit step function responses are symmetric about 0 V. The result in Fig. 3.14 validates the architecture's ability to capture rapidly changing signal portions. It is evident that the ETSR prototype captures well the fast rise of the unit step function with a slope equivalent to that in the response of the 20-GSa/s RT oscilloscope but with reduced rippling effect. As expected, the slope is captured

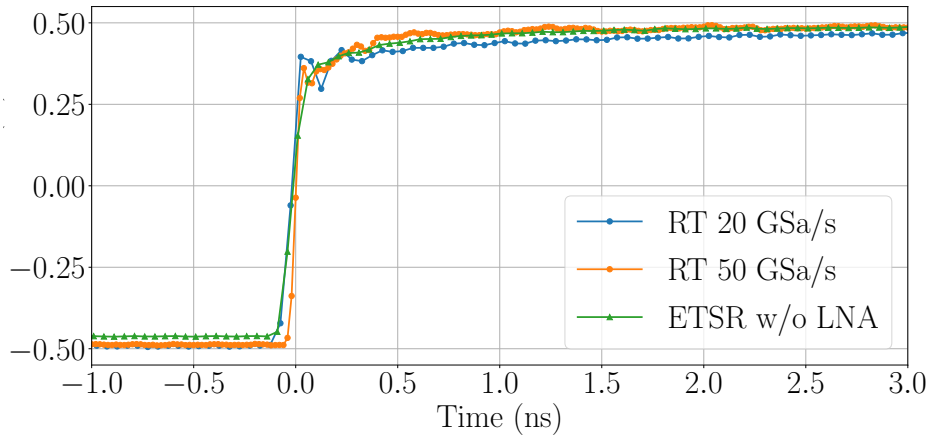


Figure 3.14: The AC coupled unit step function responses of the proposed ETSR and the two RT oscilloscopes.

best by the 50-GSa/s RT oscilloscope.

3.5.2 PDC Timebase Distortion

An important finding of this work is the significant impact of the PDC delay errors, i.e., the deviations of the actual delays realized by the PDC compared to their nominal values. Thus, jitter is not the only factor impacting the digitized timebase. It is demonstrated that these deviations cause timebase distortions, which in turn lead to errors in the spectral characteristics of the received signal. The deviations depend on the device temperature but they are systematic and, therefore, amenable to correction, provided a method is devised to estimate accurately the actual delays provided by the PDC. We have proposed such a method and have demonstrated its ability to effectively provide an accurate timebase for the received signals.

The timebase calibration is the key to achieving highly accurate time-domain measurements, demonstrated by over 93% cross-correlation between the ET-sampled pulse waveforms and those obtained with bench-top RT oscilloscopes. The careful clocking network design, employing an ultra-low jitter oscillator, ensures excellent

Table 3.5: Comparison of the proposed ETSR with prior ET receiver designs and with bench-top RT oscilloscopes.

	ETSR w/o LNA	ETSR w/ LNA	[1]	[4]	[34]	20 GSa/s Scope [23]	50 GSa/s Scope [50]
Sampling Rate (GSa/s)	20	20	102	NA	20	20	50
Resolution (bits)	16	16	8	NA	6	8	8
Input Impedance-Match Bandwidth (GHz)	0.0002-10	0.5-6	1.87-9.47	2-9.75	1-7 (8 dB)	NA	NA
Receiver Bandwidth, $B_{10\text{dB}}$ (GHz)	0.001-6.095	0.159-6.096	NA	NA	NA	DC[‡]-7.873	DC[‡]-10+
Std. Dev. Jitter, σ_j (ps)	3.110	3.876	0.9[§]	NA	NA	1.729	2.062
6σ Jitter, $6\sigma_j$ (ps)	18.662	23.258	NA	NA	NA	10.373	12.373
Peak-to-Peak Jitter, $\sigma_{j,\text{pp}}$ (ps)	21.918	23.258	NA	NA	NA	12.978	15.256
Voltage-Noise Std. Dev., σ_v (mV)	61.31	124.38	NA	NA	NA	279.09	229.06
Voltage-Noise Variance, σ_v^2 ($\text{V}^2 \times 10^{-3}$)	3.76	15.47	NA	NA	NA	77.89	52.470
Gain (dB)	NA	21	16-26	NA	NA	NA	NA
Gain Control	No	Yes	Yes	Yes	No	No	No

[‡] Taken from oscilloscope datasheet. [§] Calculated as RMS jitter integrated from 1 kHz to 10 MHz. NA stands for "Not Available".

system stability with jitter and voltage noise on par with those of the highly accurate 20-GSa/s and 50-GSa/s RT oscilloscopes. The addition of an LNA and a digital attenuator for dynamic gain control is shown to have marginal impact on the jitter and noise system metrics.

3.5.3 Comparison with Literature

Table 3.5 provides a partial comparison of the proposed design with similar direct ET sampling receivers reported in the literature. As a reference, the Table also provides the measured performance metrics of the two bench-top RT oscilloscopes in the last two columns.

We note that very few direct ET sampling receiver designs exist, which can directly sample from $\sim$1 MHz to beyond 5 GHz, and none report the receiver bandwidth, the timebase accuracy, the receiver's dynamic range in terms of the SFDR, the jitter, and the voltage noise. In [1], [4] and [34], the impedance-match bandwidths are provided based on reflection coefficient $|S_{11}|$ measurements. The impedance-bandwidth lower frequency cutoffs (f_l) of these on-chip systems are limited to 1-2 GHz, but this reflects the limits of the RF front-end impedance match. The input impedance-match bandwidths of the ETSR prototypes realized here are determined by the employed RF front-end components: 200 kHz to 10 GHz for the ETSR without LNA, and 0.5 MHz to 6.0 GHz for the ETSR with LNA. As shown here, the receiver bandwidth depends not only on the impedance match at the input, but also on the bandwidth of the sampling circuitry. The definition of the receiver bandwidth of a time-sampling receiver and the method of its evaluation proposed in Subsection 3.4.1 employ the output of the receiver (not the reflection from its input), thus capturing the performance of the entire system. The Table illustrates that the comparison with prior

systems in terms of receiver bandwidth is not possible as this metric has not been reported. The receiver bandwidths of the proposed ETSR reported in Table 3.5 are limited to $\sim$6 GHz, which clearly differs from their impedance bandwidths.

The system in [34], based on the time-expansion method, also employs an RF front-end with LNA, and the reported impedance-match bandwidth is between 1 GHz and 7 GHz for a reflection loss better than 8 dB. As discussed earlier, this system does not sample in the entire repetition period. The sampled window is limited to 2 ns, leading to an output resolution bandwidth of 500 MHz.

Further, Table 3.5 does not include ETSRs employing down-conversion [3], [5]–[8], [11], [12]. It can be argued that these architectures could also be used as direct sampling receivers if the down-conversion modules are removed. Assuming that this is possible, they are all band-limited to a highest frequency of $\sim$2 GHz. Similarly to the prior direct ET sampling receivers included in the Table, they do not report the system jitter and voltage noise, or the dynamic range (e.g., in terms of the SFDR), or the timebase accuracy of the receiver.

The above comparison of the various ET sampling receivers highlights the lack of performance metrics and their respective measurement procedures, which would allow for an objective comparison in terms of bandwidth and the accuracy of the digitized voltage and timebase. This is a significant gap in the UWB technology, which impedes the system-level design for new sensing and imaging applications. The proposed framework of metrics has been demonstrated through the evaluation of the fabricated ETSR prototypes and two bench-top RT oscilloscopes. The ETSRs exhibit low jitter, on par with the RT oscilloscopes, whereas their voltage noise is lower, which is attributed to the higher (16-bit) resolution of the employed ADC compared to the 8-bit ADCs in the RT oscilloscopes.

Finally, the proposed metrics are directly applicable to ETSRs employing down-conversion. It is our hope that the proposed framework of metrics can lead to an all-inclusive figure of merit to enable the quantitative comparison of time-domain UWB receivers.

3.5.4 Scalability

It is worth discussing the scalability of the design toward higher frequencies of operation. First, such scaling requires the extension of the analog bandwidths of the RF front-end and the T&H amplifiers. The RF front-end impedance bandwidth can be easily extended by employing high-frequency capable baluns and low-noise amplifiers (if needed). These are available well into the millimeter-wave bands. On the other hand, off-the-shelf T&H and sample-and-hold amplifier chips are limited in their analog bandwidths to about 18 GHz [72].

Second, to satisfy Nyquist's criterion, the ET sampling rate must increase to accommodate higher-frequency spectral components. Here, the limitation is determined by the shortest delay that a PDC can provide. For off-the-self PDCs, this is on the order of 10 ps, which, in principle, allows for 100 GSa/s sampling rate. However, the sampling-circuit jitter and the timebase inaccuracy must also be lower, i.e., much lower than the temporal sampling step. In the described ETSR prototype, a highly accurate 50-ps timebase is realized, along with 3-4 ps RMS jitter. Since the system's RMS jitter is an order of magnitude smaller than the 50-ps sampling step, the placement of a sample in the correct temporal bin is ensured. For a similar performance with a 10-ps sampling step, the entire clocking network of the ETSR must ensure an RMS jitter of 1 ps or less. Here, the proposed jitter metric is critical in providing guidance for the highest possible ET sampling rate.

Finally, the FPGA architecture [48], is highly flexible. Its scalability for higher sampling rates is detailed in [48].

3.6 Conclusion

In summary, the proposed time-sampling receiver architecture, along with the timebase calibration method, provides a compact, low-cost and accurate solution for a wide variety of UWB technology applications. The realized receiver prototypes function as high-performance high-speed oscilloscopes, which can be paired with any external pulsed generator of similar bandwidth to configure fast and accurate pulsed radars. The cost of the entire ETSR system is less than $4 500 USD. The system weighs 260 g and fits a length of 305 mm, a width of 135 mm, and a height of 30 mm. When paired with two of our in-house high-performance Tx modules, a unique pulsed-radar system with two transmitting and two receiving antennas is realized. Through its FPGA control, the receivers achieve unprecedented measurement speed, providing thousands of waveforms per second in each of the four radar channels. Such speed is currently not feasible with stepped frequency continuous-wave receivers. The intended applications include portable sensors for concealed weapon detection (see, for example, [75]) and radar sensors deployed on autonomous aerial vehicles, both of which require ultra-fast measurements while maintaining low cost, small size and weight.

3.A PDC Delay Calibration Procedure

The ET sampling $\check{x}(t)$ of the continuous signal $x(t)$ is represented by the interleaving of the K sub-sampled waveforms $\check{x}_k(t)$ which are sampled at $t = \tau_k + nT_{\mathrm{ADC}}$,

i.e.,

$$\check{x}(t) = \sum_{k=0}^{K-1} \check{x}_k(t),\ \check{x}_k(t) = \sum_{n=0}^{N-1} x(t)\delta\left(t - (\tau_k + nT_{\mathrm{ADC}})\right), \tag{3.13}$$

where τ_k is the k-th tap delay, n is the ADC sample index, T_{ADC} is the ADC sampling period, and $\delta(t)$ is the delta function. The goal of the timebase calibration is to accurately determine the sampling instants $(\tau_k + nT_{\mathrm{ADC}})$. Since T_{ADC} is known, only the estimation of the tap delays τ_k is needed. The (discrete-time) Fourier transform is applied to $\check{x}_k(t)$ to obtain

$$\check{X}_k(f) = \int_{-\infty}^{\infty} \check{x}_k(t) e^{-j2\pi ft} \mathrm{d}t = \sum_{n=0}^{N-1} x_k[n] e^{-j2\pi f(\tau_k + nT)}, \tag{3.14}$$

where $x_k[n] = x(\tau_k + nT)$ are the samples. In practice, we approximate $\check{X}_k(f)$ with a discrete spectrum via the FFT. For periodic signals below the Nyquist limit of $1/(2T_{\mathrm{ADC}})$, the spectra $\check{X}_k(f)$ $(k = 0, \ldots, K-1)$ differ only by a phase shift. Thus, using $\check{X}_0(f)$ as a reference, where the first tap delay is set to $\tau_0 \equiv 0$, we obtain the relationship

$$\check{X}_k(f) = e^{-j2\pi\tau_k f} \check{X}_0(f). \tag{3.15}$$

Then, each tap delay is estimated as

$$\tau_k = -\frac{1}{j2\pi f} \log\left(\frac{\check{X}_k(f)}{\check{X}_0(f)}\right) = -\frac{\log \check{X}_k(f) - \log \check{X}_0(f)}{j2\pi f}. \tag{3.16}$$

The choice of $x(t) = \cos(2\pi f_c t + \phi)$, where $f_c < 1/(2T_{\mathrm{ADC}})$, is particularly attractive as a reference signal since the spectra $\check{X}_k(f)$ are concentrated at $f = f_c$, where they all have the same magnitude but distinct (unwrapped) phases ϕ_k. Thus, (3.16) need

only be evaluated at $f = f_c$, yielding

$$\tau_k = -\frac{\phi_k - \phi_0}{2\pi f_c}. \tag{3.17}$$

To account for noise and sampling jitter, (3.17) is evaluated for M signals $x_m(t) \approx \cos(2\pi f_{c,m} t + \phi_m)$ $(m = 0, \ldots, M-1)$ with samples $x_{k,m}[n]$, each yielding an estimate $\tau_{k,m}$ of the k-th tap delay. The delay estimates are then averaged as $\bar{\tau}_k = \frac{1}{M}\sum_{m=0}^{M-1} \tau_{k,m}$ (see Algorithm 1).

Algorithm 1 Algorithm for PDC tap delay estimation

Input: sampling period T, sinusoidal signal samples $x_{k,m}[n]$
Output: average tap delay estimates $\{\bar{\tau}_k\}$

for $k = 0$ to $K-1$ **do**
  for $m = 0$ to $M-1$ **do**
    approximate spectrum $\check{X}_{k,m}(f)$ as FFT of $x_{k,m}[n]$
    identify carrier frequency $f_{c,m} = \arg\max \left|\check{X}_k(f)\right|$
    identify phase $\phi_{k,m}$ of $\check{X}_{k,m}(f_{c,m})$
    if k = 0 **then**
      set $\tau_{0,m} = 0$ and store $\phi_{0,m}$
    else
      compute $\tau_{k,m} = -(\phi_{k,m} - \phi_{0,m})/(2\pi f_{c,m})$ per (3.17)
    end if
  end for
  compute $\bar{\tau}_k = \frac{1}{M}\sum_{m=0}^{M-1} \tau_{k,m}$
end for

3.B Procedure for De-embedding the Impact of the Directional Couplers

The directional coupler is viewed as a two-port RF device since only the *coupled* port is used as an output whereas the *through* and *isolation* ports are terminated with 50-Ω loads. The de-embedding procedure is based on the $ABCD$ matrix characterization of a two-port device [71] as shown in Fig. 3.15, which represents the network

Figure 3.15: The two-port device representing a directional coupler in the measurements with the time-sampling receivers.

of the measurement with the pulse generator as a source and the receiver as a load. With the S-parameters of the two-port device known from prior measurements with a VNA [70], the goal is to extract the voltage V_1 provided the voltage V_2 is measured by the receiver. The so obtained V_1 represents the pulse-generator output measured by the receiver if they were connected directly.

First, the coupler is set up as a two-port device as explained above, and its complex S-parameters are measured with a frequency sweep from 100 MHz to 10 GHz and a step of 10 MHz. A resolution bandwidth of 10 kHz and averaging over 16 measurements are employed.

The $ABCD$ parameters of a two-port network are defined with the relation

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix}, \tag{3.18}$$

where V_1 and I_1 are the input voltage and current, and V_2 and I_2 are the output voltage and current. Note that the upper-case variables represent frequency-domain complex phasors whereas, later, we use lower-case variables for the respective functions of time.

The $ABCD$ parameters of the two-port device are computed from its S-parameters

as [71]:

$$\begin{aligned} A &= \frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{2S_{21}}, \\ B &= Z_0\frac{(1+S_{11})(1+S_{22})-S_{12}S_{21}}{2S_{21}}, \\ C &= \frac{1}{Z_0}\frac{(1-S_{11})(1-S_{22})-S_{12}S_{21}}{2S_{21}}, \\ D &= \frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{2S_{21}}, \end{aligned} \tag{3.19}$$

where $Z_0 = 50\ \Omega$ is the system impedance.

From (3.18), it follows that V_1 can be expressed as

$$V_1 = AV_2 + BI_2 = V_2\Big(A + \frac{B}{Z_{\text{in}}^{\text{Rx}}}\Big), \tag{3.20}$$

where $I_2 = V_2/Z_{\text{in}}^{\text{Rx}}$ and $Z_{\text{in}}^{\text{Rx}}$ is the receiver's input impedance. $Z_{\text{in}}^{\text{Rx}}$ is obtained from a one-port S_{11}^{Rx} measurement with the same VNA and the same frequency sweep setup as the one used to obtain the two-port device S-parameters. The input impedance $Z_{\text{in}}^{\text{Rx}}$ is then computed using

$$Z_{\text{in}}^{\text{Rx}} = Z_0\Big(\frac{1+S_{11}^{\text{Rx}}}{1-S_{11}^{\text{Rx}}}\Big). \tag{3.21}$$

$V_2(f)$ is obtained using the discrete-time Fourier transform of the measured receiver response $\tilde{x}[n] \approx x(n\Delta t)$:

$$V_2(f) = \sum_{n=0}^{N-1} \tilde{x}[n]e^{-j2\pi f(n\Delta t)}, \tag{3.22}$$

which is implemented via the FFT algorithm.

Once $V_1(f)$ is computed using (3.20), the time-domain input voltage v_1 is found

by applying the inverse discrete-time Fourier transform

$$v_1 = \sum_{n=0}^{N-1} V_1[n] e^{j2\pi f(n\Delta t)}\,, \tag{3.23}$$

which is implemented with the inverse-FFT algorithm.

References

[1] Y. Masui, A. Toya, M. Sugawara, *et al.*, "Differential equivalent time sampling receiver for breast cancer detection," in *2017 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, Turin, Italy: IEEE, Oct. 2017, pp. 1–4.

[2] D. Oloumi, A. Bevilacqua, and M. Bassi, "UWB radar for high resolution breast cancer scanning: System, architectures, and challenges," in *2019 IEEE International Conference on Microwaves, Antennas, Communications and Electronic Systems (COMCAS)*, Tel-Aviv, Israel: IEEE, Nov. 2019, pp. 1–4.

[3] R. Feghhi, R. Winter, F. Sabzevari, and K. Rambabu, "Design of a low-cost UWB time-domain radar system for subcentimeter image resolution," *IEEE Trans. Microw. Theory Techn.*, vol. 70, no. 7, pp. 3617–3628, Jul. 2022.

[4] L. M. M. De Almeida, B. Sanches, and W. A. M. Van Noije, "High-speed sampler for UWB breast cancer detection system," in *2023 IEEE 14th Latin America Symposium on Circuits and Systems (LASCAS)*, Quito, Ecuador: IEEE, Feb. 2023, pp. 1–4.

[5] Y. Yang and A. Fathy, "Near-real-time data acquisition and beamforming for UWB see-through-wall system," in *2007 IEEE Workshop on Signal Processing Applications for Public Security and Forensics*, Washington, DC, USA: IEEE, Apr. 2007, pp. 1–4.

[6] Y. Yang and A. Fathy, "Development and implementation of a real-time see-through-wall radar system based on FPGA," *IEEE Trans. Geosci. Remote Sens.*, vol. 47, no. 5, pp. 1270–1280, May 2009.

[7] Q. Liu, Y. Wang, and A. Fathy, "A compact integrated 100 GS/s sampling module for UWB see through wall radar with fast refresh rate for dynamic real time imaging," in *2012 IEEE Radio and Wireless Symposium*, Santa Clara, CA, USA: IEEE, Jan. 2012, pp. 59–62.

[8] Q. Liu, Y. Wang, and A. Fathy, "Towards low cost, high speed data sampling module for multifunctional real-time UWB radar," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 49, no. 2, pp. 1301–1316, Apr. 2013.

[9] A. D. Pitcher, "Compact low-cost ultra-wideband pulsed-radar system," M.A.Sc. thesis, Department of Electrical and Computer Engineering, McMaster University, Hamilton, ON, Canada, Aug. 2019.

[10] M. Saad, A. Maali, M. S. Azzaz, and M. Benssalah, "An efficient FPGA-based implementation of UWB radar system for through-wall imaging," *International Journal of Communication Systems*, e5510, May 2023.

[11] A. Altieri, M. Bouza, J. A. Maya, and C. G. Galarza, "Design and evaluation of an impulsive ultrawideband system for estimating the moisture content of polyamide targets," *IEEE Trans. Instrum. Meas.*, vol. 70, pp. 1–9, Dec. 2020.

[12] J. Lee, C. Nguyen, and T. Scullion, "A novel, compact, low-cost, impulse ground-penetrating radar for nondestructive evaluation of pavements," *IEEE Trans. Instrum. Meas.*, vol. 53, no. 6, pp. 1502–1509, Dec. 2004.

[13] C. Noviello, G. Gennarelli, G. Esposito, *et al.*, "An overview on down-looking UAV-based GPR systems," *MDPI Remote Sensing*, vol. 14, no. 3245, pp. 1–28, Jul. 2022.

[14] Y. López, M. García-Fernández, G. Álvarez-Narciandi, and F. Las-Heras, "Unmanned aerial vehicle-based ground-penetrating radar systems: A review," *IEEE Geosci. Remote Sens. Mag.*, vol. 10, no. 2, pp. 66–86, Apr. 2022.

[15] M. García-Fernández, G. Álvarez-Narciandi, Y. López, and F. Las-Heras, "Array-based ground penetrating synthetic aperture radar on board an unmanned aerial vehicle for enhanced buried threats detection," *IEEE Trans. Geosci. Remote Sens.*, vol. 61, pp. 1–18, May 2023.

[16] "First report and order, revision of part 15 of commission's rule regarding UWB transmission system FCC 02-48," Federal Communications Commission (FCC), Washington, DC, USA, Tech. Rep. FCC 02-48, Apr. 2002.

[17] J. Sachs, *Handbook of Ultra-Wideband Short-Range Sensing*, 1st. Weinheim, Germany: Wiley-VCH Verlag & Co., 2013.

[18] T. Zwick, W. Wiesbeck, J. Timmermann, and G. Adamiuk, *Ultra-Wideband RF System Engineering* (EuMA High Frequency Technologies Series), 1st. Cambridge, UK: Cambridge University Press, 2013.

[19] C. Nguyen and J. Park, *Stepped-Frequency Radar Sensors: Theory, Analysis and Design*. Berlin/Heidelberg, Germany: Springer International Publishing, 2016.

[20] J.-M. Muñoz-Ferreras, Z. Peng, R. Gómez-García, and C. Li, "Review on advanced short-range multimode continuous-wave radar architectures for healthcare applications," *IEEE J. Electromagn. RF Microw. Med. Biol.*, vol. 1, no. 1, pp. 14–25, Aug. 2017.

[21] C. Li, Z. Peng, T.-Y. Huang, *et al.*, "A review on recent progress of portable short-range noncontact microwave radar systems," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 5, pp. 1692–1706, Jan. 2017.

[22] Z. Fang, W. Wang, J. Wang, *et al.*, "Integrated wideband chip-scale RF transceivers for radar sensing and UWB communications: A survey," *IEEE Circuits Syst. Mag.*, vol. 22, no. 1, pp. 40–76, Feb. 2022.

[23] "Keysight technologies InfiniiVision 6000 X-series oscilloscope," Keysight Technologies, Inc., Datasheet 5991-4087EN, Dec. 2024.

[24] "Infiniium Z-series oscilloscopes," Keysight Technologies, Inc., Datasheet 5991-3868EN, Oct. 2019.

[25] "Infiniium S-series oscilloscopes," Keysight Technologies, Inc., Datasheet 5991-3904EN, May 2022.

[26] "6 series B MSO: Mixed signal oscilloscope," Tektronix, Inc., Datasheet 48W-61716-09, May 2023.

[27] "Mixed signal and digital phosphor oscilloscopes: MSO/DPO70000DX series," Tektronix, Inc., Datasheet 55W-23446-40, Aug. 2023.

[28] "ADC12DJ5200RF 10.4-GSPS single-channel or 5.2-GSPS dual-channel, 12-bit RF-sampling analog-to-digital converter (ADC)," Texas Instruments, Inc., Datasheet SLVSEN9F, Rev. F, Apr. 2024.

[29] "ADC08DJ5200RF 10.4-GSPS single-channel or 5.2-GSPS dual-channel, 8-bit RF-sampling analog-to-digital converter (ADC)," Texas Instruments, Inc., Datasheet SLVSEO1A, Rev. A, Aug. 2022.

[30] "12-bit, 6 GSPS/10.25 GSPS, JESD204B RF analog-to-digital converter," Analog Devices, Inc., Datasheet AD9213, Rev. A, Mar. 2020.

[31] C. Nguyen and J. Han, *Time-Domain Ultra-Wideband Radar, Sensor and Components: Theory, Analysis and Design*. Berlin/Heidelberg, Germany: Springer International Publishing, 2014.

[32] I. Y. Immoreev, "Ultrawideband radars: Features and capabilities," *Journal of Communications Technology and Electronics*, vol. 54, no. 1, pp. 1–26, Jan. 2009.

[33] S. Kumar, A. Kumar, V. Singh, and A. Singh, "A review on impulse radar," *International Journal of Electronics and Telecommunications*, vol. 67, no. 4, pp. 579–587, Nov. 2021.

[34] H. G. Han, B. G. Yu, and T. W. Kim, "A 1.9-mm-precision 20-GHz direct-sampling receiver using time-extension method for indoor localization," *IEEE J. Solid-State Circuits*, vol. 52, no. 6, pp. 1509–1520, Jun. 2017.

[35] "AN1365: Si5361/62/63 lock time parameters," Skyworks Solutions, Inc., Application Note AN1365, Nov. 2022.

[36] I. Collins, "Phase alignment and control of the ADR4356/ADF5356 devices," Analog Devices, Inc., Technical Article, Aug. 2017.

[37] "3.3V ECL programmable delay chip," ON Semiconductor, Denver, CO, USA, Datasheet MC100EP195B/D, Rev. 4, Nov. 2024.

[38] "SY89295U 2.5V/3.3V 1.5GHz precision LVPECL programmable delay," Micrel, Inc., Datasheet SY89295U, Mar. 2011.

[39] "SY100EP195V 3.3V/5V 1.6GHz programmable delay," Microchip Technology, Inc., Datasheet DS20006194A, May 2019.

[40] A. D. Pitcher, M. Georgiev, and N. K. Nikolova, "Correcting timebase errors in ultra-wideband equivalent-time sampling receivers," in *2024 21st European Radar Conference (EuRAD)*, Paris, France: IEEE, Nov. 2024, pp. 47–50.

[41] A. D. Pitcher, C. W. Baard, and N. K. Nikolova, "Design and performance analysis of a picosecond pulse generator," *IEEE Trans. Instrum. Meas.*, vol. 71, pp. 1–14, Aug. 2022.

[42] P. Protiva, J. Mrkvica, and J. Macháč, "Universal generator of ultra-wideband pulses," *Radioengineering*, vol. 17, no. 4, pp. 74–78, Dec. 2008.

[43] M. Rahman and K. Wu, "A nonlinear transmission approach to compressing rise and fall time in picosecond pulse generation," *IEEE Trans. Instrum. Meas.*, vol. 70, pp. 1–13, Apr. 2021.

[44] R. Feghhi, D. Oloumi, and K. Rambabu, "Tunable subnanosecond gaussian pulse radar transmitter: Theory and analysis," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 9, pp. 3823–3833, Apr. 2020.

[45] R. Feghhi, D. Oloumi, and K. Rambabu, "Design and development of an inexpensive sub-nanosecond gaussian pulse transmitter," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 9, pp. 3773–3782, Sep. 2019.

[46] D. Oloumi and E. Fear, "A picosecond pulse generator using SRD diodes: Design, analysis, and measurements," in *2018 USNC-URSI Radio Science Meeting (Joint with AP-S Symposium)*, Boston, MA, USA: IEEE, Jul. 2018, pp. 159–160.

[47] A. D. Pitcher, J. J. McCombe, E. A. Eveleigh, and N. K. Nikolova, "Compact transmitter for pulsed-radar detection of on-body concealed weapons," in *2018 IEEE/MTT-S International Microwave Symposium (IMS)*, Philadelphia, PA, USA: IEEE, Jun. 2018, pp. 919–922.

[48] A. D. Pitcher, M. Georgiev, N. K. Nikolova, and N. Nicolici, "Parallelized field-programmable gate array data processing for high-throughput pulsed-radar systems," *MDPI Sensors*, vol. 25, no. 239, pp. 1–25, Jan. 2025.

[49] "EXG X-series signal generator N5173B microwave analog 9 KHz to 13, 20, 31.8, or 40 GHz," Keysight Technologies, Inc, Datasheet 5991-3132EN, Feb. 2023.

[50] "Digital phosphor oscilloscopes / digital serial analyzers," Tektronix, Inc., Datasheet 4HW-19377-15, Mar. 2009.

[51] "Zedboard," Digilent, Inc., Hardware User's Guide, v1.1, Aug. 2012.

[52] "HMC760LC4B wideband 4 GS/s track-and-hold amplifier DC - 5 GHz," Analog Devices, Inc., Datasheet HMC760LC4B, v01.0514.

[53] "ADS42LBx9 14- and 16-bit, 250-MSPS, analog-to-digital converters," Texas Instruments, Inc., Datasheet SLAS904F, Rev. F, May 2016.

[54] "Ultra series crystal oscillator Si545 data sheet," Skyworks Solutions, Inc., Datasheet Si545, Rev. 206613A, May 2023.

[55] "CDCM61001 one output, integrated VCO, low-jitter clock generator," Texas Instruments, Inc., Datasheet SCAS869F, Rev. F, Jun. 2011.

[56] J. Wilson, "Timing jitter tutorial and measurement guide," *Silicon Labs*, pp. 1–31, [Online]. Available: https://www.mouser.com/pdfdocs/timing-jitter-tutorial-and-measurement-guide-ebook.pdf?srsltid=AfmBOoqo_wIz7N_H_YpANNS0dCqBNT1iNAGrdXPXuESWvyDG0pQByoS2.

[57] "CDCLVP1102 two-LVPECL output, high-performance clock buffer," Texas Instruments, Inc., Datasheet SCAS884D, Rev. D, Dec. 2015.

[58] "CDCLVP1204 four LVPECL output, high-performance clock buffer," Texas Instruments, Inc., Datasheet SCAS880F, Rev. F, Sep. 2015.

[59] "Fixed SIP delay line T_R ¡ 1 ns (series 2020 & 2021)," Data Delay Devices, Datasheet #01009, Oct. 2001.

[60] "Low noise, wideband, high IP3 monolithic amplifier," Mini Circuits, Datasheet PMA3-83LN+, Rev. E, Apr. 2024.

[61] "Surface mount bias-tee," Mini Circuits, Datasheet TCBT-14R+, Rev. D, Apr. 2018.

[62] "2 dB LSB, 4-bit, silicon digital attenautor, 9 kHz to 40 GHz," Analog Devices, Inc., Datasheet ADRF5721, Rev. A, Mar. 2020.

[63] "Surface mount RF transformer," Mini Circuits, Datasheet TCM1-63AX+, Rev. A, 2015.

[64] "High power balun (200 kHz to 10 GHz)," Marki Microwave, Inc., Datasheet BALH-0010, Rev. D, Oct. 2020.

[65] "IEEE standard for terminology and test methods for analog-to-digital converters," IEEE Standard 1241-2023, May 2023.

[66] "Scipy.optimize.curve_fit," The SciPy Community, SciPy Manual v1.12.0, 2024.

[67] "Rubidium frequency standard model FE-5680A series: Operation and maintenance instructions," Frequency Electronics, Inc., Mitchel Field, NY, USA, Tech. Manual TM 5680-0211, Nov. 2002.

[68] "Coaxial 50W 10 dB directional coupler 0.5 – 6 GHz," RF-Lambda, Datasheet RFDC5M06G10, Rev. 5.0, Jun. 2022.

[69] "Coaxial 50W 20 dB directional coupler 0.5 – 6 GHz," RF-Lambda, Datasheet RFDC5M06G20, Rev. 5.0, Jan. 2025.

[70] "R3860A, R3770, R3768 operator manual," Advantest Corporation, Operator Manual FOE-8440128F01, Aug. 2003.

[71] D. Pozar, *Microwave Engineering*, 4th. Hoboken, NJ, USA: John Wiley & Sons, 2012.

[72] "HMC661LC4B wideband 4 GS/s track-and-hold amplifier DC - 18 GHz," Analog Devices, Inc., Datasheet HMC661LC4B, v03.0615.

[73] F. Antonio, "Graphics gems III," in D. Kirk, Ed. San Diego, CA, USA: Academic Press, Inc., 1992, ch. IV.6 Faster Line Segment Intersection, pp. 199–202.

[74] "Arbitrary waveform generator," Tektronix, Inc., Datasheet 76W-19779-3, 2009.

[75] N. K. Nikolova and J. J. McCombe, *On-body concealed weapon detection system*, U.S. Patent No. 10,229,328, Mar. 2019.

CHAPTER 4:

PARALLELIZED FIELD-PROGRAMMABLE GATE ARRAY DATA PROCESSING FOR HIGH-THROUGHPUT PULSED RADAR SYSTEMS

Preface

This chapter is a reproduction of the following published article:

A. D. Pitcher, M. Georgiev, N. K. Nikolova, and N. Nicolici, "Parallelized field-programmable gate array data processing for high-throughput pulsed-radar systems," *MDPI Sensors*, vol. 25, no. 239, pp. 1–25, Jan. 2025. DOI: 10.3390/s25010239.

I developed, designed, simulated, and validated all firmware and software, established the experimental framework and measurement methodology, conducted the system analysis, and authored and edited the manuscript. Mihail Georgiev contributed to the development of the proposed calibration method, supported the design of the Ethernet offload and digital signal processing pipeline (DSPPL) software suite, and reviewed the manuscript. Natalia K. Nikolova supervised the project, provided critical

resources, and contributed to manuscript editing. Nicola Nicolici provided valuable insights into the design and formulation of the field-programmable gate array (FPGA) data processing pipeline and reviewed the manuscript.

4.1 Introduction

The advent of ultra-wideband (UWB) technology has enabled a multitude of emerging sensing and imaging applications. It operates in various frequency bands between 100 MHz and 10.6 GHz [1]. Its main advantages are non-ionizing radiation, low-power emission spread over large bandwidths, and good penetration [2], especially in the low-GHz spectrum. Emerging applications include medical sensing and diagnostics [3]–[5], security and surveillance [6]–[10], through-the-wall imaging [11]–[17], and ground penetrating radar [18]–[22].

Sensing and imaging applications of UWB technology demand time-domain measurements with sampling rates on the order of tens of giga-samples per second (GSa/s), along with versatility, affordability, and compactness. Versatility greatly simplifies the system development for a new application, whereas the low cost and small size/weight enable mobile and large-scale network deployment. The proof-of-concept development of a new custom UWB radar application often employs bench-top instruments (e.g., high-speed oscilloscopes and waveform generators) as they are, by design, versatile, i.e., capable of generating and measuring a variety of radar waveforms. They are also highly accurate. However, they are large, heavy, and expensive, and advancing the prototype to a practical application often hinges on developing a custom UWB radar system. Here, we propose an accurate FPGA-based low-cost, compact, and versatile UWB receiver.

To date, a few compact UWB receiver prototypes have been reported in the literature, but they are application-specific [3]–[5], [9]–[19]. Also, important challenges have not been addressed. First, high sampling rates demand fast processing and high data-transfer rates that match the sampling speed and prevent data loss so that the radar capabilities are fully utilized. Second, fast data offloading to a computer is needed for application-specific signal processing and data storage. Finally, time-domain receivers are prone to noise and interference due to their large input bandwidths. While bench-top oscilloscopes [23]–[27] and off-the-shelf high-speed analog-to-digital converters (ADCs) [28]–[30] can meet the required sampling rates, their data transfer to an external device creates a bottleneck. Since they do not support custom signal processing, data offloading to an external computing platform is needed, which creates a major impediment. Also, the cost of bench-top oscilloscopes and GSa/s ADC chips is prohibitive when a low-cost solution is desired.

The reported compact custom UWB receivers [3]–[5], [9]–[19] employ various architectures. Here, we are interested in direct equivalent-time (ET) sampling receivers, i.e., those without down-conversion, that use lower ADC sampling rates, leading to simple data interfaces and reduced cost. It has been shown in [3], [9]–[16], [18], [19], [31] that ET sampling can be implemented on field-programmable gate arrays (FPGAs), but only a few of these sources [11]–[16], [31] describe aspects of the FPGA firmware architecture that performs the radar control and the ET waveform processing in the receivers. From the reported throughput performance, it is apparent that current architectures suffer from significant data loss in the data-processing pipeline. One reason is the time needed to adjust and stabilize (or settle) the clocks controlling the delays applied to the ADC sampling [11], [12]. This time is very significant when a phase-locked loop (PLL) delay-control network is employed since it requires approximately a microsecond [32], [33] to phase-lock on the clock signal and

create the sampling delay. In the case of PLLs, the settling time is greater than the ADC's sampling period and is of the same order of magnitude as the pulse repetition period (or pulse cycle). This results in less than 50% of the pulse cycles being utilized, thereby reducing the waveforms per second at the radar output [12]. An alternative is to employ a programmable delay chip (PDC) [14], [15], which has much shorter settling times (on the order of picoseconds [34]). PDCs offer an advantage because the settling time is orders of magnitude smaller than the ADC's sampling period. Therefore, there is no loss of pulses within the received pulse train. The FPGA-based radar receiver proposed here employs a PDC to eliminate the loss of pulse cycles due to clock settling and to highlight the importance of parallelizing the firmware architecture for fully utilizing the pulse train.

Another factor contributing to data loss in prior FPGA processing architectures is the use of a single memory bank to perform the waveform reconstruction, the waveform averaging, and the offloading [11]–[13], [15], [16], [31]. This sequential approach creates a data-throughput bottleneck. Memory bank offloading (reading) takes time comparable to waveform reconstruction (implemented as memory bank writing), slowing down processing by a factor of 2 if reading and writing occur at the same rate. In the absence of buffering, only reading or writing can occur at one time, leading to data loss within the FPGA pipeline. But FPGAs support multiple memory banks, enabling buffering so that reconstruction can be carried out in parallel with offloading, thereby completely eliminating data loss.

Here, we propose a parallelized FPGA architecture designed to control a generic receiver, which functions as a highly accurate, high-speed oscilloscope [10] and supports a wide range of UWB radar applications. The parallelized FPGA architecture maximizes the data throughput and efficiency, achieving 98.2% utilization of the received pulse train. The design features simultaneous data collection from two ADC

channels while optimizing parallelization for the per-channel computation. The proposed parallel processing minimizes data loss and maximizes data throughput. This implementation leverages eight memory banks, of which four are used for waveform reconstruction and interference monitoring (two per receiver channel) and another four for user-defined averaging (two per receiver channel).

The proposed architecture supports real-time radar applications requiring ultra-fast measurements, such as tracking moving objects. Capturing thousands of measurements per second enables advanced detection and identification tools, including those using statistical signal processing or machine learning, which require large datasets. This work does not focus on detection and imaging (radar signal processing) algorithms. For example, in our concealed weapon detection application, novel statistical algorithms are implemented on external computing platforms for research and development purposes, emphasizing the system's need for high data throughput and efficiency. Although introduced in the context of this application, the system is versatile and adaptable to various use cases. It can integrate with any transmitter module (e.g., pulse or continuous-wave generators) that supports synchronization, adding versatility.

The FPGA architecture leverages the multi-bank design to perform signal-processing tasks crucial for signal quality assurance: (i) user-defined waveform averaging to improve signal-to-noise ratio (SNR), and (ii) interference monitoring and suppression. To the best of our knowledge, FPGA-based processing for interference suppression has not previously been implemented. This is critically important since UWB radars share frequencies with cellular, Wi-Fi, and Bluetooth signals. These additional tasks do not affect the data throughput rate.

Finally, we introduce a systematic method, along with metrics, for evaluating data loss in the FPGA signal-processing chain, as well as that in the data offloading

from the UWB radar system to an external device (e.g., a computer). To the best of our knowledge, these rates have either not been investigated or not reported in published work. The throughput of image frames per second (FPS) was reported in [11], [12], [14], but this metric included image reconstruction. A waveform refresh rate at the FPGA output was reported in [31], but the data loss or efficiency of the FPGA processing is unknown. We demonstrate the proposed method and metrics with the new parallelized FPGA architecture on the dual-channel UWB receiver when this receiver is connected to an external computer through an Ethernet link. A 1 gigabit per second Ethernet link is used because it is the fastest interface on the employed FPGA board [35]. The radar output of over 9 000 waveforms per second (Wfm/s), generating 6.4 gigabit per second (Gbps), greatly exceeds the capacity of the Ethernet link. Therefore, we show how the FPGA-based functionality is leveraged to reduce the offloaded data while fully utilizing the radar output.

This paper is organized as follows. Section 4.2 discusses the requirements for the UWB radar system. Section 4.3 describes the proposed FPGA architecture. The results are discussed in Section 4.4, including throughput analysis and measurements involving moving people. Conclusions are provided in Section 4.5.

4.2 UWB Radar System Requirements

4.2.1 The Intended Application

The detection method proposed in [6]–[8] provides a non-imaging solution for unattended and unobtrusive radar surveillance to detect weapons concealed under clothing or in bags. The need for such surveillance arises from the limited efficacy of current screening technologies (e.g., walk-through detectors [36], X-ray and millimeter-wave

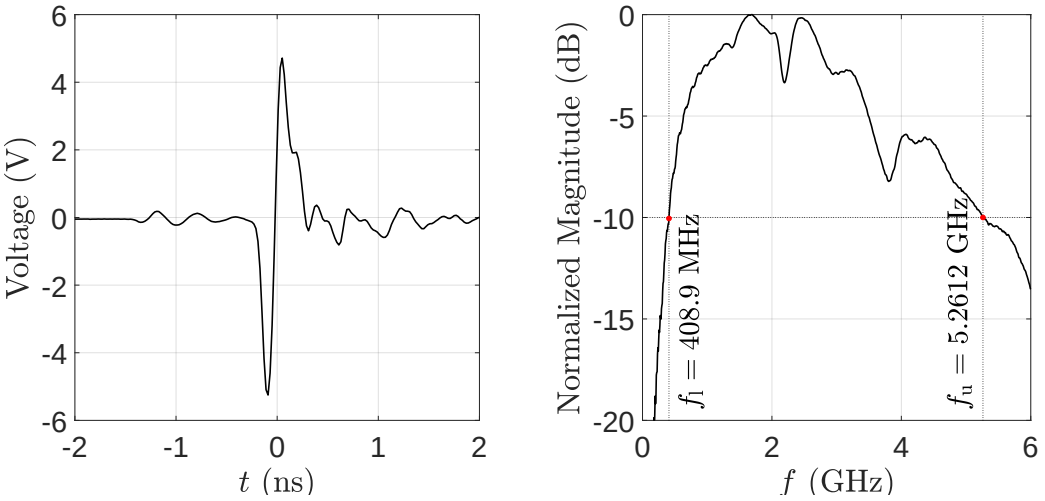
full-body scanners [37], portable scanners [38]), all of which require trained security personnel in proximity to the inspected person, who must comply with instructions and remain still. This results in low screening throughput and precludes around-the-clock automated surveillance.

To be effective, the method proposed in [8] requires a low-cost, compact radar system, which enables discrete deployment, preferably multiple units for wide-area coverage and various viewing angles of an object. Additionally, it benefits from polarization diversity. For this reason, our radar system is equipped with two transmitting (Tx) and two receiving (Rx) antennas. The antennas are linearly polarized, acquiring four back-scattered responses: VV, HH, VH, and HV. Here, H stands for horizontal and V stands for vertical; the first letter denotes reception, whereas the second denotes transmission.

4.2.2 Frequency Bandwidth and Pulse Excitation Requirements

Non-imaging detection methods distinguish an object of interest from the radar background and clutter by analyzing the early-time response and late-time response of the back-scattered radar signals or by extracting features based on estimated radar-cross section and polarization ratios [6]–[8], [39]–[42]. In particular, the method proposed in [8] relies on the resonant signatures of the various weapons of interest (handguns, knives, grenades, or explosive vests), which are typically found in the range of approximately 400 MHz to 5 GHz [6], [39]. Our UWB radar system is designed to operate from 500 MHz to 5 GHz.

The excitation is provided by a picosecond pulse generator, which produces a highly stable monocycle-like pulse [43]. The measured temporal and spectral plots of the pulse are shown in Fig. 4.1. The -10 dB bandwidth covers the spectrum from



(a) (b)

Figure 4.1: The UWB radar system monocycle-like pulse generated by a picosecond pulse generator [43]: (a) temporal plot, (b) spectral plot indicating the low (f_{l}) and upper (f_{u}) bounds with red dots for the -10 dB bandwidth.

500 MHz to 5 GHz.

4.2.3 Timing Requirements

The measurement speed must ensure multiple waveform acquisitions while the object remains within the radar's field of view. The signal-processing algorithms that issue the threat/non-threat decision and identify the threats must also perform in real time; however, they run on an external computer and are not discussed here. Here, we focus on data acquisition speed and signal preprocessing on the FPGA-based system. The main constraint is the time available while the radar interrogates a moving person.

The average velocity v of a person, walking or running, ranges from 0.75 m/s to 3.25 m/s [44]. Fig. 4.2 shows an example arrangement for the intended application, where the Tx and Rx antennas are placed apart at a distance of $d = 0.5$ m. The

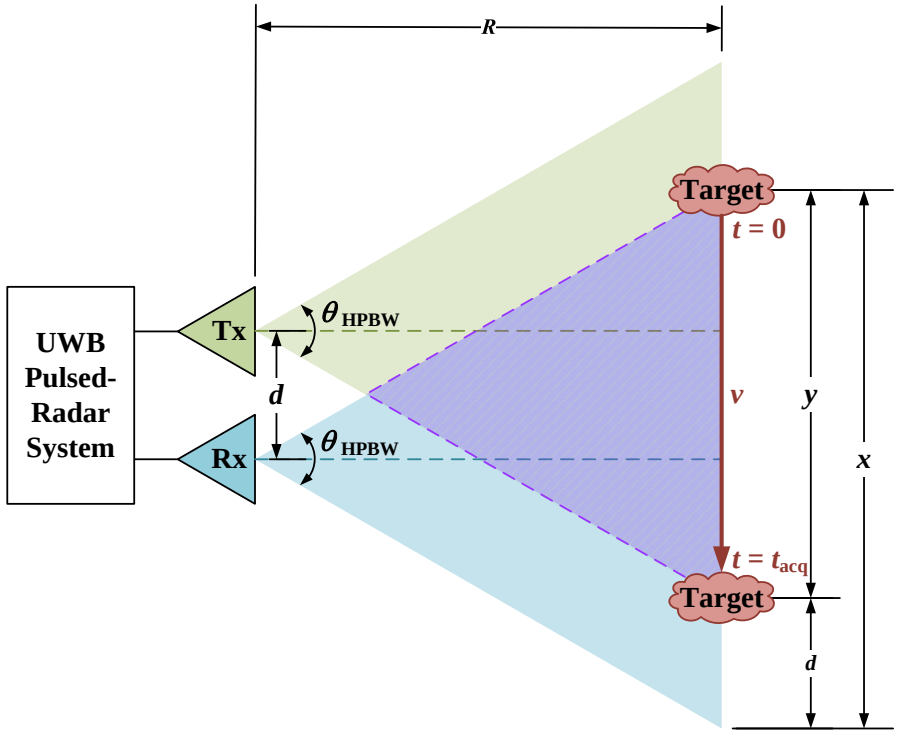


Figure 4.2: Data acquisition window of target.

object is at a distance R, which is smaller than the radar's unambiguous range, and moving perpendicularly to the radar's field of view, resulting in the shortest observation time. The maximum unambiguous range for a monostatic radar configuration is $R_{\max} = cT_{\mathrm{P}}/2$, where c is the speed of light and T_{P} is the inverse of the pulse repetition frequency (PRF).

The purple-shaded region, outlined by dashed lines, is where the object is within both the Tx and Rx antennas' field of view. Using the UWB antenna half-power beamwidth (HPBW) of $\theta_{\mathrm{HPBW}} = 51°$ [45], the distance traveled by the object while in this region is

$$y = x - d = 2R\tan(\theta_{\mathrm{HPBW}}/2) - d. \tag{4.1}$$

The acquisition time is $t_{\mathrm{acq}} = y/v$. The shortest acquisition time arises at the shortest range distance $R \approx 1$ m, for which 138 ms $\lesssim t_{\mathrm{acq}} \lesssim$ 605 ms if 0.75 m/s $\lesssim v \lesssim$ 3.25 m/s.

Within this short observation time, it is desirable to acquire more than a hundred measurements in each of the four available radar responses (VV, HH, VH, and HV). The range $R \geq 1$ m ensures operation beyond the reactive near-field zone of the antennas.

With the above requirement in mind, the chosen PRF for the monocycle-like pulse of each transmitter is $f_{\mathrm{PRF}} = 1$ MHz ($T_{\mathrm{P}} = 1$ µs). The two transmitters are triggered on the rising edges of their respective synchronized 1 MHz clock signals, which have a 50% duty cycle and are mutually shifted by 0.5 µs. Thus, the effective PRF of the system is $T_{\mathrm{P,eff}} = 0.5$ µs. Note that the unambiguous radar range with this $T_{\mathrm{P,eff}}$ is $\sim$75 m, which exceeds the targeted concealed weapon detection (CWD) application range ($\sim$1 m to 10 m).

The two pulse generators trigger about 276 000 pulses for the shortest observation time, 138 ms. On the other hand, as explained later, each of the two ET receiver channels sub-samples 110 waveforms to reconstruct a single, fully sampled waveform. We emphasize that each fully sampled waveform contains two back-scattered responses (co- and cross-polarized), spaced in time by 0.5 µs. Thus, the radar system, with its two Tx and two Rx antennas, can provide over 5 000 back-scattered responses within the shortest observation time. Such data abundance enables highly effective statistical detection and identification methods. This remarkable speed is conditional upon FPGA processing and offloading to the computer in real time without data loss.

4.2.4 Implementation of the Radar System

Fig. 4.3 presents a high-level block diagram of the proposed dual-channel UWB pulsed-radar system. Table 4.1 summarizes the key radar parameters. The system simultaneously receives on two Rx channels (RxA and RxB). With two sequentially

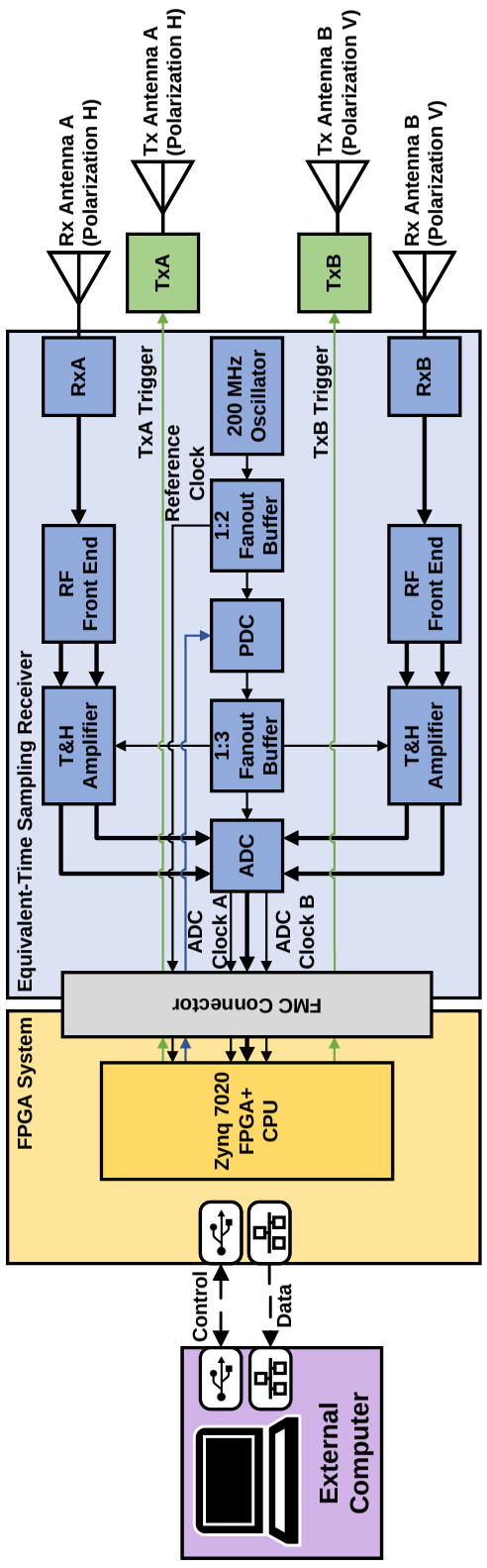


Figure 4.3: High-level block diagram of the UWB pulsed-radar system. RxA and RxB are the two ETSR Rx input channels. TxA and TxB are the two Tx modules.

excited Tx modules (TxA and TxB) and antennas, it performs full polarimetric measurement with four responses. It consists of two identical transmitter modules (the picosecond pulse generator described in [43]), the output of which is shown in Fig. 4.1. The custom dual-channel equivalent-time sampling receiver (ETSR) features an input bandwidth of 6.1 GHz at the −10 dB level and an ET sampling rate of 20 GSa/s [10]. The dual-channel ETSR receiver interfaces with a low-cost FPGA board [35] through two 200 MHz low voltage differential signaling (LVDS) data buses (one per ADC channel) across the FPGA mezzanine card (FMC) connector. The common off-the-shelf FPGA board controls the entire system. We emphasize that the proposed radar system is coherent, i.e., the ETSR is precisely synchronized with the employed Tx modules. Finally, the data are offloaded to the external computer for target feature extraction and classification. The radar has a programmable PRF, here set to f_{PRF}.

Table 4.1: UWB radar system parameters.

Parameters	Values
Lower Frequency, f_{l}	0.5 GHz
Upper Frequency, f_{h}	5.0 GHz
Bandwidth, B	4.5 GHz
Excitation	Monocycle Pulse
PRF, f_{PRF} (PRI, T_{P})	1 MHz (1 μs)
Effective PRF, $f_{\text{PRF,eff}}$ (Effective PRI, $T_{\text{P,eff}}$)	0.5 MHz (0.5 μs)
Approximate Maximum Unambiguous Range, R_{max}	75 m
Number of Transmitters	2
Number of Receivers	2
Reconstruction Method	ET Sampling
ET Sampling Rate, f_{ET} (Sampling Period, Δt)	20 GHz (50 ps)
ADC Sampling Rate, f_{s} (Sampling Period, T)	200 MHz (5 ns)
ADC Resolution	16 bits
Sub-Sampled Waveforms per Reconstruction, K	110
Samples per Sub-Sampled Waveform, N	200
Number of Averages	2^A, $A \leq 8$
Fully Sampled Waveform Reconstruction Time, T_{Wfm}	110 μs

Fig. 4.3 shows the key ETSR hardware components and their clock distribution network, which are essential for understanding the FPGA design. A detailed description of the ETSR is provided in [10]. A 200 MHz oscillator [46] generates the *reference clock*, distributed to the FPGA and PDC via a 1:2 fan-out buffer [47]. The FPGA uses this clock for internal logic and to synchronize the Tx modules with the waveform reconstruction. The 1 MHz TxA and TxB triggers (see Fig. 4.3) are derived from this reference clock within the FPGA and sent to the Tx modules. The PDC [34], discussed later, introduces delays to shift the ADC sampling points relative to the oscillator. A 1:3 fan-out buffer [48] distributes the delayed clock to the ADC and the two track and hold (T&H) amplifiers. Precise clock timing is crucial to account for internal delays in the T&H amplifiers and ADC [9], ensuring that the Rx signals are synchronized and sampled during the T&H amplifier's hold stage. The ADC digitizes samples into 16-bit values, sending them over the LVDS data buses along with an ADC clock (see *ADC clocks A and B* in Fig. 4.3). These clocks, synchronized with the PDC output, are a delayed version of the reference clock.

Next, we describe how the PDC is leveraged to perform ET sampling, the efficiency of which critically depends on the FPGA firmware architecture. The 20 GSa/s sampling rate requires an ET sampling interval $\Delta t = 50$ ps. The ET waveform reconstruction interleaves K sub-sampled waveforms ($K = 110$), each containing N samples ($N = 200$) acquired by the onboard 200 MHz ADC [49]. The k-th sub-sampled waveform of a signal $x(t)$ is

$$x_k[n] = x(\tau_k + nT_{\text{ADC}}),\ n = 0, \ldots, N-1 \tag{4.2}$$

where τ_k ($k = 0, ..., K-1$) is the delay determining its start and $T_{\text{ADC}} = 5$ ns is the ADC's sampling period. The delay τ_k, which time-shifts the k-th sub-sampled

waveform, is realized by the PDC, which is a cascaded network of delay circuits. Each delay circuit (referred to as a *tap*) is enabled or disabled by the FPGA. The 10 tap delays of the PDC are represented by the delay vector

$$\mathbf{d} = [4610, 2300, 1150, 575, 290, 145, 70, 35, 15, 10]^{\mathrm{T}}, \tag{4.3}$$

in ps. The overall delay is $\tau_k = \mathbf{c}_k^{\mathrm{T}}\mathbf{d}$, where $\mathbf{c}_k \in \{0,1\}^{10}$ is a sequence of tap-control bits. For example, if $\mathbf{c}_k = [0,0,0,0,0,0,0,1,1,0]^{\mathrm{T}}$, then $\tau_k = 50$ ps.

If the delays were equispaced, i.e., if $\Delta t = \tau_{k+1} - \tau_k = 50$ ps for all k, exactly $K = 100$ sub-sampled waveforms $x_k[n]$ are needed to reconstruct $x(t)$, since $K = T_{\mathrm{ADC}}/\Delta t$. However, it is evident from (4.3) that the PDC cannot provide equispaced delays. For this reason, $K = 110$ sub-sampled waveforms are used to provide a temporal overlap between the waveform samples $\{x_{100}[n] \cdots x_{109}[n]\}$ and $\{x_0[n+1] \cdots x_9[n+1]\}$. The PDC delays are optimally configured to provide tap-delay increments close to 50 ps, covering a tap-delay range from $\tau_0 = 0$ ps to $\tau_{109} = 5\,450$ ps.

It is worth mentioning that the actual PDC tap delays may differ significantly from the tabulated values in (4.3) [10], [50]. A calibration procedure has been developed to extract the true delay values [50]. This delay correction, along with interpolation to an equispaced 50 ps timebase (carried out on the external computer), results in an accurate uniformly sampled reconstructed signal with a temporal length of 1 μs.

Hereafter, we adopt the following terminology for the reconstructed signals. The term *waveform* refers to a full 1 μs single-channel reconstruction due to reception from one Rx antenna. The dual-channel radar receiver's simultaneous processing reconstructs two such waveforms. Further, a waveform contains two *responses* (HH and HV, or VH and VV), triggered 0.5 μs apart. Thus, a response is 0.5 μs long. Finally, the term *trace* refers to a user-defined portion of a response. Typically, the

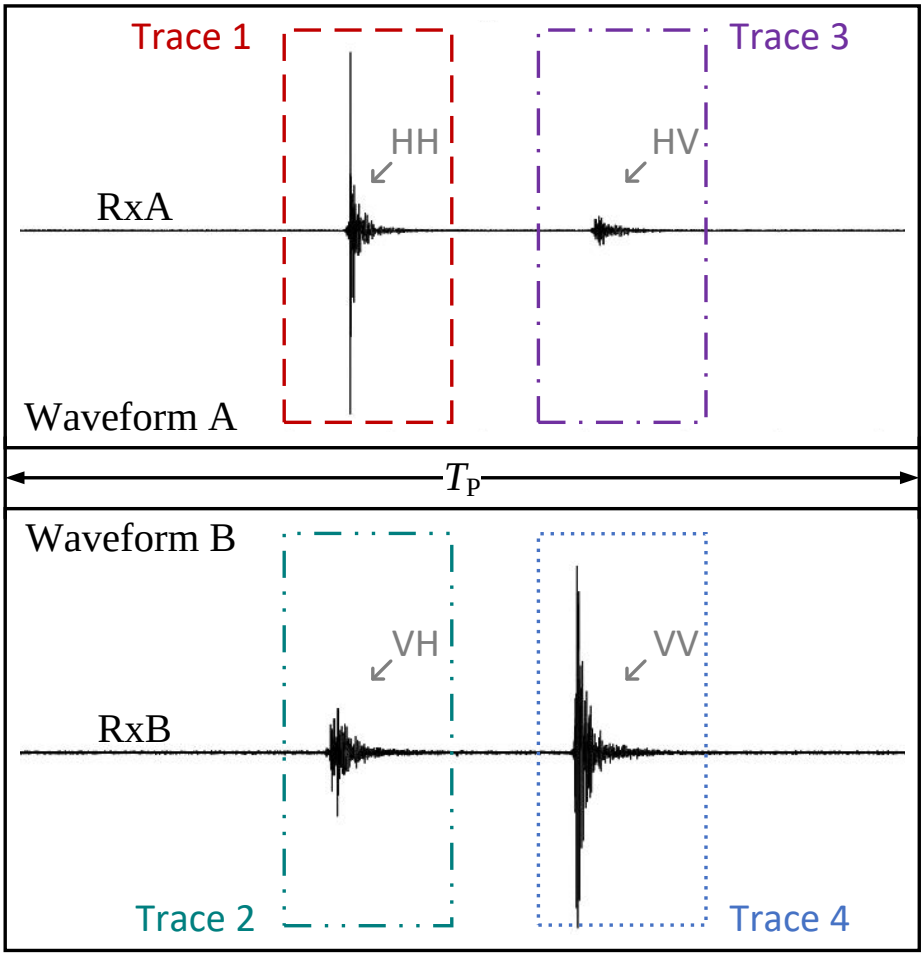


Figure 4.4: Visualization of the terms *waveform* and *trace* in relation to the four radar responses (VV, HH, VH, and HV). The plots are derived from actual measurements of a scattering object.

trace spans a time interval where the user expects to receive a back-scattered signal based on the radar range and/or the expected distance to the target. Thus, a trace has a length ≤ 0.5 µs. As shown later, the reduced trace size can significantly alleviate the burden of data offloading and effectively eliminate data loss. Fig. 4.4 provides a visualization of this terminology.

4.2.5 Data Offload Constraints

The speed requirement for data offloading is dictated by the speed at which data are generated by the dual-channel ETSR, whose dual-channel 200 MHz 16-bit ADC output data rate is 6.4 Gbps, or 800 MB/s. This data stream is then processed in the FPGA to produce the overall radar throughput, which is measured in terms of Wfm/s. In our case, the measurement time required to obtain a full waveform on each channel is $T_{\text{Wfm}} = KT_{\text{P}} = 110$ µs. Thus, ideally (no data loss), the waveform generation rate on each channel is $\text{INT}(T_{\text{Wfm}}^{-1}) = 9\,090$ Wfm/s, where $\text{INT}(x)$ rounds x down to an integer. A single waveform reconstructed in the FPGA contains $NK = 200 \times 110 = 22\,000$ samples (with 16-bit samples), or 44 kB of data. Provided the FPGA preprocessing keeps up with the ADC in reconstructing the two output waveforms simultaneously, the radar output data rate is 2×44 kB $\times$ 9 090 Wfm/s, or 799.92 MB/s, closely matching the ADC's data rate.

The proposed FPGA board features a 1 Gbps (125 MB/s) Ethernet link, which we use for data offloading. Our receiver far exceeds the data rate of the widely available Ethernet link. Thus, we perform real-time signal preprocessing, such as interference monitoring, averaging, and trace windowing, to reduce the amount of offloaded data, achieving nearly 100% data utilization over this interface. Higher-throughput solutions would enable us to offload more raw data, but this would be of little utility in our envisioned application, which targets the employment of low-cost solutions.

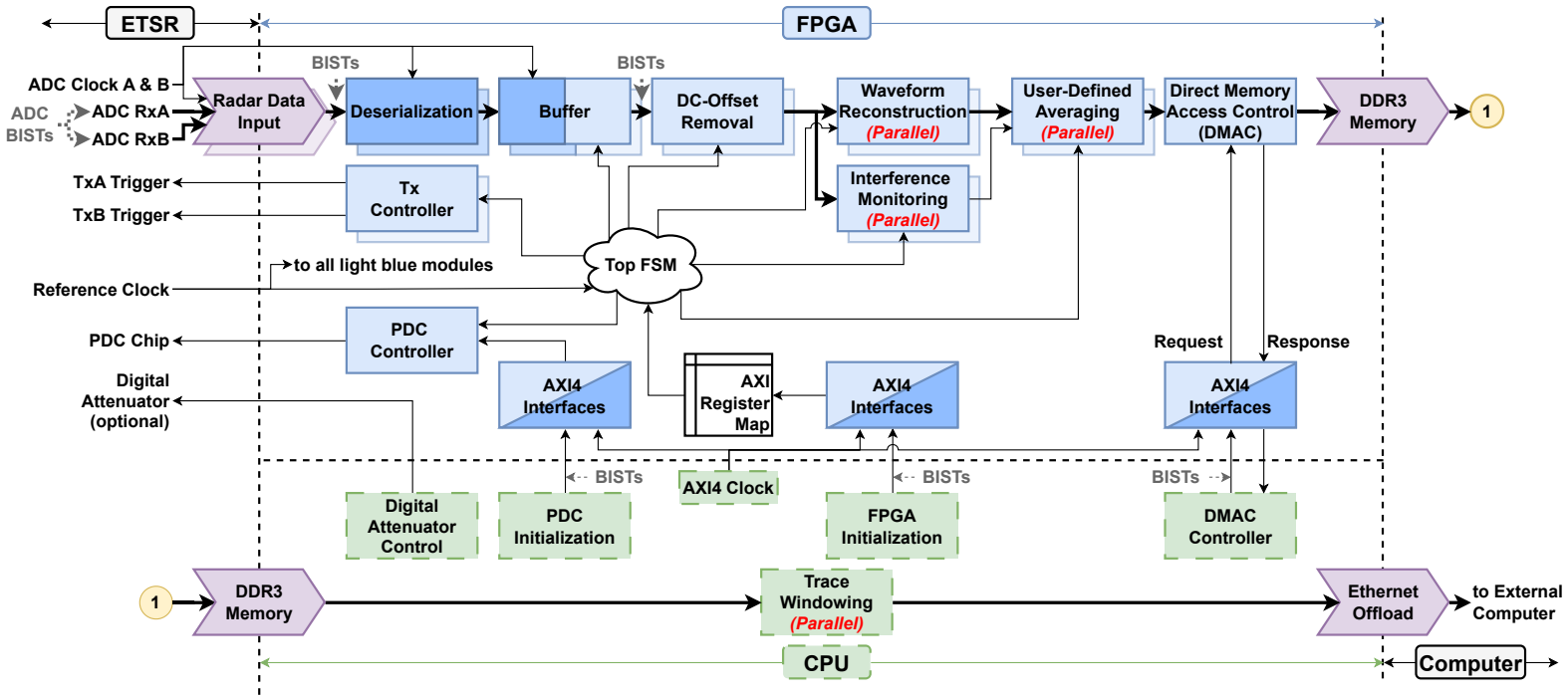


Figure 4.5: A high-level diagram of the data pipeline for waveform reconstruction and preprocessing on the FPGA and CPU SoC. The data pipeline is interrupted at the circle labeled 1 to wrap the image on the page. The blue blocks outlined by solid lines indicate processing occurring within the FPGA. The double-stacked blue blocks indicate simultaneous processing on two channels. The blocks labelled "Parallel" indicate where parallel processing is implemented. The green blocks outlined by dashed lines indicate processing on the CPU SoC. The purple chevron blocks represent interfaces for data transfer from/to the indicated source/destination. If a block is colored in two shades, it corresponds to a process involving clock domain crossings (CDCs).

4.3 Proposed FPGA System Design

Our design utilizes a Zynq 7020 system on a chip (SoC) [51], containing an Artix-7 FPGA and a dual-core ARM Cortex-A9 central processing unit (CPU) on a pre-built FPGA board [35]. Fig. 4.5 presents the proposed firmware architecture, which leverages the FPGA's high speed to perform real-time (RT) waveform reconstruction and embedded signal-preprocessing tasks. The preprocessing conditions the waveform before submitting it to the external computer for further processing. The dual-channel ADC data are simultaneously collected on both channels, while optimal parallelization is proposed for per-channel preprocessing. Here, we use the term "simultaneous processing" to refer to the concurrent data collection due to the dual-channel ADC (indicated by the stacked blue blocks in Fig. 4.5). Meanwhile, the terms "parallel processing" or "parallelization" refer only to the optimal parallel operations in each of the two channels (indicated by the "parallel" labels in Fig. 4.5), thus enabling the loss-free high throughput of data.

The FPGA implementation is written using hardware description languages, specifically *System Verilog*, *Verilog*, and *VHDL*, in AMD's Vivado Design Suite [52]. The custom CPU codebase uses the *C*-based Software Development Kit [53] provided with Vivado [52].

With reference to Fig. 4.5, the data flows from the ETSR ADC (top-left corner) through the FPGA data pipeline. Then, it is passed to the shared off-chip DDR3 memory (top-right corner) and the CPU (see circle 1). The CPU performs *trace windowing*, which reads the external DDR3 memory data and breaks the waveforms into traces. Then, the traces are offloaded by the CPU to the external computer through the 1 Gbps Ethernet link. As shown in the CPU section in Fig. 4.5, the other CPU functions are: (i) setting the attenuation level in the ETSR radio frequency (RF)

front end (*digital attenuator control*), (ii) start-up configuration of the PDC and the FPGA (*PDC initialization* and *FPGA initialization*), and (iii) requesting the last dual-channel reconstructed waveforms from the direct memory access control (DMAC) (*DMAC controller*).

We next focus on the FPGA section in Fig. 4.5. The *top FSM* (finite state machine) provides master-control sequences within the FPGA. These are initialized by a register map provided by the CPU. The ADC output data stream must first be deserialized. The *deserialization* module receives the ADC samples in a serialized format and converts each of them into a 16-bit parallel bit stream for the *buffer*. The *buffer* (one per channel) queues the 16-bit samples of the k-th sub-sampled waveform. The *DC-offset removal* module removes the mean (DC offset) from the sub-sampled waveform (a parasitic effect created by the ETSR circuitry). The sub-sampled waveform is then passed to both the *waveform reconstruction* and *interference-monitoring* modules, which are the first two parallel processing modules in the proposed architecture. The reconstructed waveform is then passed to the third parallel processing module, the *user-defined averaging* module, if no electromagnetic interference (EMI) is detected. If EMI corrupts the waveform, it is discarded. This concludes waveform preprocessing within the FPGA. The waveform is then passed to the DMAC, where it is stored in the DDR3 memory at an address allocated by the CPU. As indicated by the double blue blocks in Fig. 4.5, each module in the preprocessing chain is duplicated for simultaneous processing on both the RxA and RxB channels.

The key FPGA features that significantly enhance the per-channel data throughput through parallelization are explained next.

4.3.1 FPGA Synchronization

The proposed FPGA architecture operates in an asynchronous multi-clock system. First, the radar system has an external 200 MHz precision *reference clock* provided by the ETSR (refer to Fig. 4.3). This is the same reference clock shown in Fig. 4.5. All FPGA preprocessing must be synchronized with this clock (see the light-blue modules in Fig. 4.5). Second, a 100 MHz advanced extensible interface (AXI) clock (generated within the FPGA) synchronizes the commands between the CPU and the FPGA on the SoC through the AXI4 Interfaces (see the three interfaces in Fig. 4.5). Third, there are two 200 MHz ADC clocks (one per channel, labeled *ADC Clock A* and *ADC Clock B* in Fig. 4.3 and Fig. 4.5) provided by the ETSR ADC. These ADC clocks provide the timing reference for deserializing and buffering the ADC outputs into 16-bit parallel bit streams. We consider all four clocks to be mutually asynchronous, including the ADC clocks, which originate from the reference clock but pass through the PDC, introducing variable delays.

As a result, the FPGA architecture must accommodate domains synchronized by their respective clocks. These are referred to as *clock domains*, of which our architecture has four (reference clock, AXI clock, and two ADC clocks). When data are passed between clock domains, the metastability created by the clock domain crossing (CDC) must be addressed [54], [55]. A metastable state, referred to as metastability, occurs when the output of a flip-flop within the FPGA is unpredictable. At all CDCs, this is accomplished with asynchronous first-in first-out (FIFO) buffers [56], configured to use one clock reference for writing and another for reading. Provided the FIFO's status flags are monitored within their respective clock domains (which they are here), an error-free CDC is achievable. Here, CDCs occur in the two *buffer* modules (see

Fig. 4.5), which are implemented as FIFOs capable of holding a minimum of N samples. Here, the FIFO depth is 512 samples. When the FIFO *writes*, filling the *buffer*, it is synchronized with the ADC clock. But when it *reads*, emptying the *buffer*, it is synchronized with the reference clock. The FIFO CDC implementation was verified using built-in self-test (BIST) patterns, e.g., deterministic synthetic binary signals generated by either the ADC (referred to as test patterns in [49]) or custom-built pattern generators embedded within the FPGA processing (see the BIST labels in Fig. 4.5). These BIST patterns are used to emulate hardware and synthesize data buses to validate FPGA functionality in operational conditions. After verifying the BIST patterns through simulation and hardware, it was determined that no error correction and detection were needed. Similarly, the *AXI4 interfaces* use FIFOs, which can buffer 16 CPU commands. These FIFOs *write* to the AXI clock and *read* from the reference clock. Likewise, these CDCs were also verified using BIST patterns through FPGA simulations of the AXI interconnect and CPU commanding on the hardware, e.g., writing and then reading back known values to registers within the FPGA.

The synchronization of the two *buffers* with the *PDC controller* and the *Tx controller* is illustrated in Fig. 4.6. All transitions are synchronized with the rising edges of the 200 MHz reference clock, which is not shown due to its short temporal extent. The TxA and TxB 1 MHz triggers are clock-divided from the reference clock, and they trigger a pulse transmission on the rising edge. A 180° phase shift is applied to the TxB trigger to stagger the two transmitted pulses in time by 0.5 µs. A PDC delay setting is invoked on the rising edge of the TxA trigger, and the setting depends on the sub-sampled waveform index k, after which it resets to 0 ps (see the third row in Fig. 4.6). Each new delay setting is invoked by the PDC update sequence, which is a latch signal generated by the FPGA (see the fourth row in Fig. 4.6). The two *buffers* follow identical timing sequences, and only one is shown in rows five to nine.

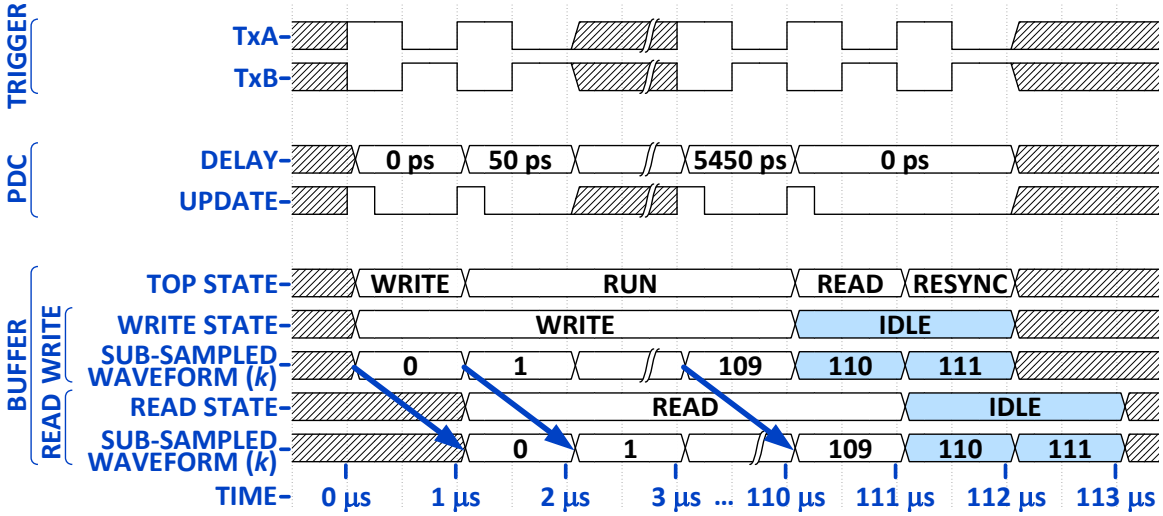


Figure 4.6: FPGA synchronization diagram for a single waveform reconstruction. The shaded regions are where the process repeats. The blue arrows indicate the data transfer of the k-th sub-sampled waveform through the *buffer*. The shaded 110 and 111 cells are two additional sub-sampled waveforms that cannot be received due to synchronization issues.

At the start of waveform reconstruction, the buffer's *top state* is a write-only state (WRITE), during which the buffer accepts the first sub-sampled waveform ($k = 0$), filling it with N samples. Then, it transitions to a RUN state, where it performs *write* and *read* operations for the sub-sampled waveforms $k = 1, \ldots, K-2$, and a *write* operation for the last sub-sampled waveforms $k = K - 1 = 109$. The FIFO remains filled around N samples as the write and read clocks operate at the same rate (200 MHz) but with different phases. Finally, it transitions to a read-only state (READ), emptying the last sub-sampled waveform (N samples) until the FIFO empty flag is raised. CDC sample counters are used on both clock domains to ensure that the NK samples required for waveform reconstruction are passed through the FIFO. The buffer then enters a re-synchronization state (RESYNC). The blue arrows in Fig. 4.6 represent the k-th sub-sampled waveform data transfer through the *buffer*. We can observe that two additional sub-sampled waveforms (shaded and labeled as 110 and

111 in rows seven and nine) are actually generated by the ADC while the *buffer* is in the READ and RESYNC top states when it cannot *write*. Since only 110 out of 112 waveforms are actually used, the data-throughput efficiency is 98.2% before the waveform reconstruction occurs.

Although the re-synchronization state causes minor data loss, it is necessary. In one period $T_{\mathrm{P}} = 1$ µs, the ADC provides $N = 200$ samples for each sub-sampled waveform. But the ET sampling scheme requires a delay τ_k of the ADC clock (controlled by the PDC) for each (k-th) sub-sampled waveform, thus pushing its end into the next 1 µs period. For example, the sampling of the last 109th waveform is delayed by $\tau_{109} = 5\,450$ ps, effectively extending the 1 µs waveform period to an ET waveform extent of 1 005.45 ns. To synchronize the acquisition of the next set of 110 waveforms with the Tx triggers, the system needs to skip *writing* one waveform period. It also must wait for the *buffer* to offload (or *read*) the last sub-sampled waveform.

4.3.2 FPGA Waveform Reconstruction

The *waveform reconstruction* process in each channel (see Fig. 4.5) interleaves the K sub-sampled waveforms, described by (4.2), into a single fully sampled waveform:

$$x[k + nK] = x_k[n] = x(\tau_k + nT_{\mathrm{ADC}})\,. \tag{4.4}$$

Fig. 4.7 illustrates the interleaving of $K = 2$ sub-sampled waveforms to produce a waveform with an ET sampling step of Δt.

Fig. 4.8 shows a block diagram of the hardware components within the FPGA used for parallelizing a single-channel waveform reconstruction and interference-monitoring preprocessing. In contrast with prior waveform reconstruction strategies [11], [12],

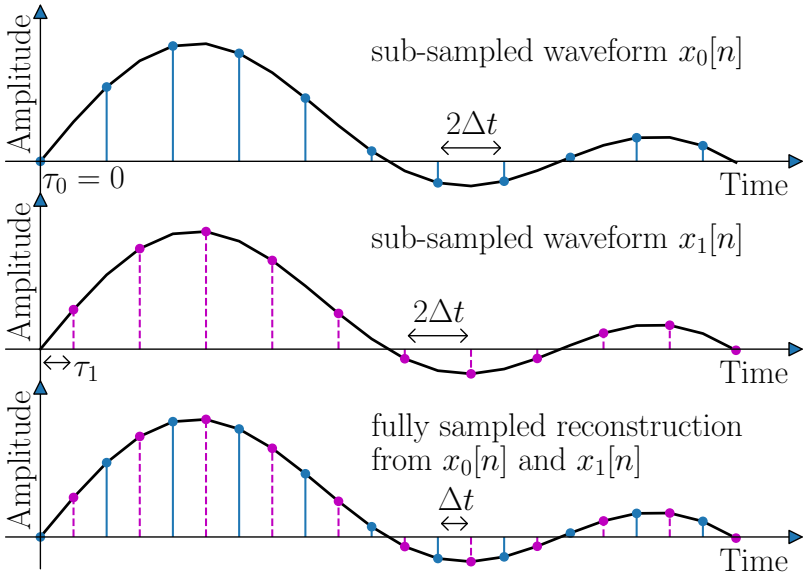


Figure 4.7: Illustration of waveform reconstruction by interleaving two sub-sampled waveforms.

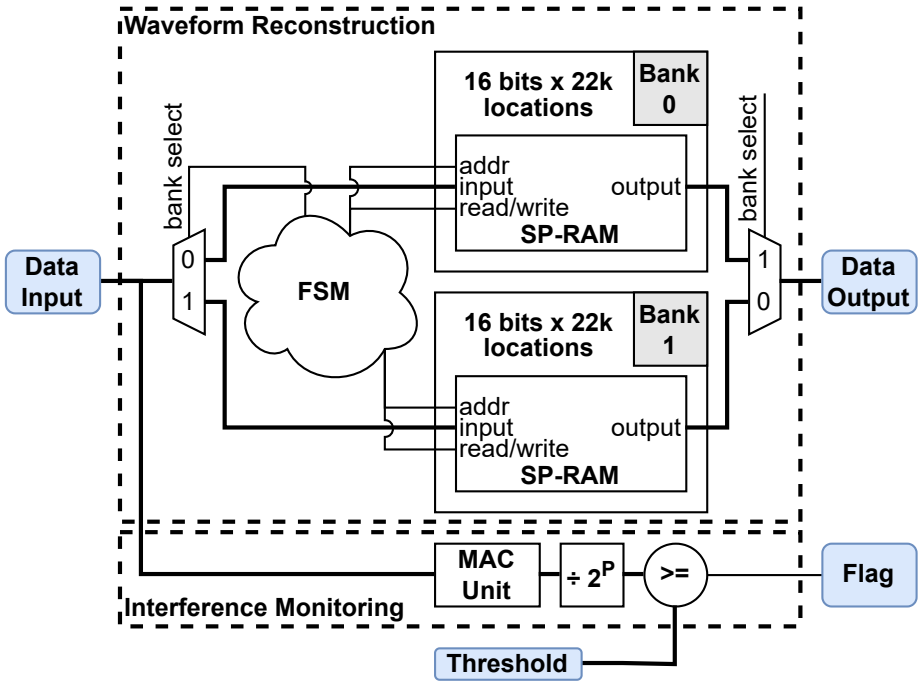


Figure 4.8: Block diagram of the hardware components within the FPGA used for waveform reconstruction and interference monitoring in one of the two channels. The two embedded processes run in parallel, and they are delineated with dashed-line boxes. The MAC unit is a multiplier-accumulator.

[15], [16], [31], two single-port memory banks (SP-RAM in Fig. 4.8) run in parallel. Each bank has 22 000 16-bit locations to store one fully sampled waveform. A local FSM controls the *bank select* signal to determine the bank in which the data are written (0 or 1). It also provides a memory address and read/write flag to the *addr* and *read/write* ports, respectively. While one bank is written to through the *input* port, the other is offloaded through the *output* port. This is the first parallelization approach, which achieves maximum throughput at the cost of a second memory resource.

The interleaving of the K sub-sampled waveforms is accomplished while writing to a bank by selecting the memory location (*addr* port in Fig. 4.8) as $addr = k + nK$. This realizes the digitized signal in (4.4). When reading from a bank, the *addr* port is driven by a sequential counter from 0 to $NK - 1 = 21\,999$. Since the number of locations written to equals those read from, and the *write* and *read* operations are both matched to the 200 MHz reference clock, the waveform reconstruction is 100% efficient (no data loss).

4.3.3 FPGA Signal Preprocessing

As shown in Fig. 4.5, preprocessing within the FPGA performs *DC-offset removal*, *interference monitoring*, and *user-defined averaging*.

4.3.3.1 DC-Offset Removal

A pre-determined DC offset is subtracted from all sub-samples. This value is ETSR-specific and is determined empirically. It is obtained by terminating the ETSR input ports with a 50 Ω load, resulting in the ETSR outputs being noise-only waveforms. For each channel, 1024 such waveforms are acquired and averaged, producing

$x_{\text{avg}}[i]$, $i = 0, \ldots, NK-1$. The DC offset is then computed as

$$\bar{x} = \frac{1}{NK} \sum_{i=0}^{NK-1} x_{\text{avg}}[i]. \tag{4.5}$$

The DC offset values used here are 5.49 mV and 0.99 mV for RxA and RxB, respectively.

4.3.3.2 Interference Monitoring

This preprocessing step mitigates the impact of EMI sources corrupting the received waveforms. It is the second parallel operation in the FPGA preprocessing stage. It runs in parallel with the waveform reconstruction (see Fig. 4.8) and produces a flag when EMI is detected. This flag is submitted to the *user-defined averaging* module to discard the corrupted waveform, i.e., not including it in the average.

When the radar operates indoors, the strongest EMI is usually due to Wi-Fi transmissions. This poses a problem for the radar system, as the Wi-Fi packets, depending on their size and bit rate, spread over much longer periods (well over 100 µs) than the pulse period of 1 µs. This causes incoherent interference over the entire reconstructed waveform period, masking the back-scattered radar signal from a target. However, the UWB pulse is very short (∼4 ns, see Fig. 4.1) compared to the 1 µs waveform. Thus, large portions of the reconstructed waveform carry only system noise (see Fig. 4.4). As a result, the interference is easily detected within a predetermined portion of the waveform where the pulse does not exist. We define a time period at the beginning of waveform reconstruction and denote it as $T_{\text{EMI}} = \tau_k + jT_{\text{ADC}}$, where $j = 0, \ldots, J-1$, and $J < N-1$. T_{EMI} is user-defined by the number of samples. Here, we use $KJ = 4\,096$, resulting in a temporal length of (J/N) µs ≈ 186.2 µs.

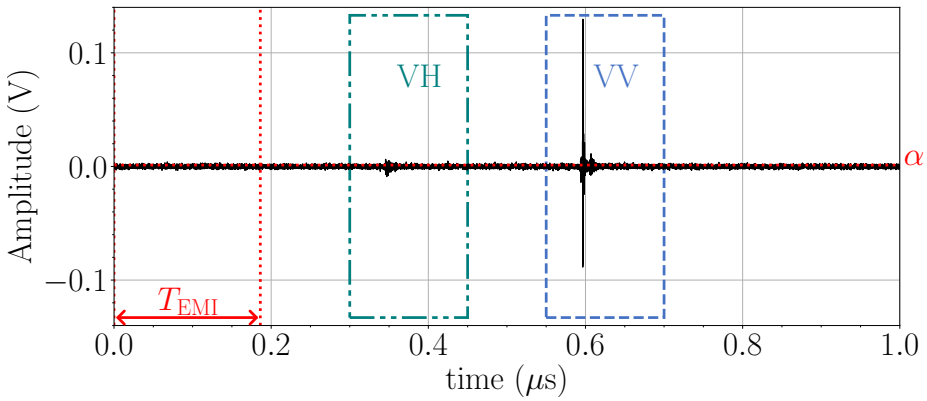
The detection of EMI employs the variance of the zero-mean signal within T_{EMI}:

$$\sigma^2 = \frac{1}{KJ} \sum_{k=0}^{K-1} \sum_{j=0}^{J-1} (x_k[j] - \bar{x})^2. \tag{4.6}$$

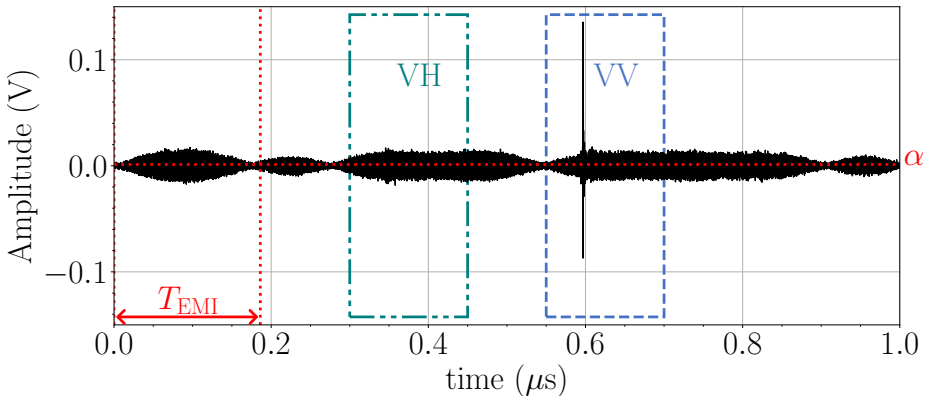
It is advantageous to have the sample length such that $KJ = 2^P$ (here, $P = 12$) since this allows for efficient fixed-point division. The FPGA hardware components implementing the variance computation (4.6) are the multiplier-accumulator (MAC) along with the division by 2^P (see Fig. 4.8). A user-defined threshold α^2 is then used to determine whether a waveform reconstruction is corrupted by checking $\alpha^2 \geq \sigma^2$.

The threshold α is dependent on the entire radar system. The threshold is determined by deploying the entire radar system in an electromagnetically quiet environment, such as an anechoic chamber. The system voltage noise standard deviation σ_{v} is computed, as described in [10], for the T_{EMI} portion of the reconstructed waveform. Here, the EMI detection threshold is empirically chosen to be $\alpha = 1.2 \times \sigma_{\text{v}}$ or 1.21 mV. It is also important to emphasize that, due to the parallelization, each reconstructed pulse on the simultaneous channel collection can be inspected for EMI. This enables us to discard corrupted waveforms on both channels before averaging. If the EMI signals are below the interference-monitoring threshold, their impact is nonetheless mitigated by the averaging.

Fig. 4.9 illustrates an example of an indoor measurement of a dihedral corner reflector (aligned with the V-polarized Tx and Rx antennas). Only the waveform received by the V-polarized Rx antenna is shown, which contains the VV and VH signals. Fig. 4.9a shows an example of a received waveform (without averaging) when EMI monitoring is enabled, whereas Fig. 4.9b shows the same measurement scenario when it is disabled. Intense Wi-Fi communication is realized through a video call from a tablet. In Fig. 4.9a, the VH and VV traces are clearly identified against the



(a)



(b)

Figure 4.9: Illustration of reconstructed waveforms (a) with EMI suppression enabled, and (b) with a Wi-Fi burst corrupting the signal while EMI suppression is disabled. The dashed-dotted and dashed-line windows show the VH and VV responses, respectively. The vertical dotted lines show the interference-monitoring window T_{EMI}. The horizontal dot line indicates the EMI threshold α.

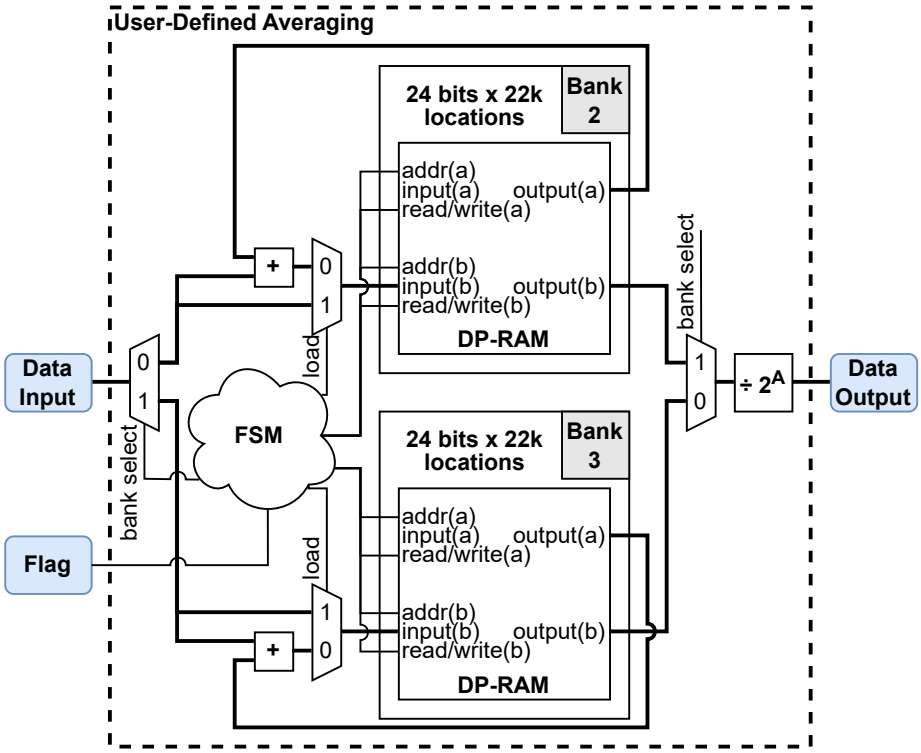


Figure 4.10: Block diagram illustrating the various hardware components in the FPGA used for user-defined averaging on a single channel.

noise, while in Fig. 4.9b, the weak VH signal is completely masked by the interference. We have determined empirically that this simple EMI mitigation strategy discards 3–6% of the reconstructed waveforms when the radar is deployed under the described scenario.

4.3.3.3 User-Defined Averaging

This process uses 2^A, $A = 0, 1, \ldots, 8$, fully sampled waveforms to deliver a single cumulative average. Averaging improves the SNR for random uncorrelated noise by a factor of A [2], and cumulative averaging reduces the amount of offloaded data by a factor of 2^A.

A block diagram of the involved FPGA hardware components is shown in Fig. 4.10.

Similar to the *waveform reconstruction* module, two memory banks (Bank 2 and Bank 3) perform parallel processing, each containing 22 000 locations. Again, while one bank is written to, the other is offloaded from, controlled by the "bank select" signal. However, here, the bank locations are extended from 16 bits to 24 bits to support an accumulated sum of up to 256 (2^8) waveforms. The additional 8-bit width is needed to maintain precision and avoid overflow. Additionally, each bank is implemented with a dual-port RAM (DP-RAM) in the FPGA, allowing for two input/output port pairs: (a) and (b) in Fig. 4.10. While the two port pairs share the same memory addresses, they allow for separate access to *write/read* operations. In particular, two output ports are needed in each dual-port RAM to implement averaging. The address ports, *addr* (a) and (b), for both *read* and *write* operations, are driven by sequential counters from 0 to $NK - 1 = 21\,999$.

To obtain the 2^A average, the first incoming waveform is written to a memory address through the input (b), which is controlled by the "load" signal from the local FSM. Subsequent waveforms are accumulated by reading the last accumulated result from the output (a), adding it to the incoming waveform on input (b) and writing it to the same memory address. Once 2^A waveforms are accumulated, the bank is emptied on output (b), while the second bank begins the process again. The sum is divided by 2^A before offloading to the DDR3 memory.

The dual-bank design of the averaging module is 100% efficient with zero data loss. With $A > 0$, the amount of data to be delivered to the external computer is also reduced. The data-reduction ratio resulting from the averaging (DR_{av}) is the input-to-output sample ratio, i.e., $DR_{\text{av}}(A) = 2^A$. As explained later, this aids data offloading in matching the radar speed of one waveform every 110 µs.

Table 4.2: Trace-windowing cases.

	Length in Sa/trace	DR_{win}
1	11 000	1
2	8 250	1.33
3	5 500	2
4	2 750	4
5	2 200	5

4.3.4 CPU Signal Preprocessing and Data Offload

4.3.4.1 Trace Windowing

This task is performed by the CPU and is the last parallel processing step in the preprocessing pipeline. While the FPGA is preparing the next pair of reconstructed waveforms, the CPU is offloading the current pair of reconstructed waveforms. Here, the two prepared waveforms are segmented into four traces (VV, VH, HV, and HH), offloaded in this order. This allows the user to set the trace windows (depending on the anticipated range to the target), which can provide substantial data reduction. Table 4.2 presents some windowing cases used later for throughput analysis. The second column lists the number of samples in each trace. Since a full waveform contains 22 000 samples and two responses (VV and VH, or HV and HH), the maximum trace length is 11 000 samples. The last column shows the windowing data-reduction ratio DR_{win}, i.e., the ratio of the maximum trace length to the actual one.

4.3.4.2 Data Offload

CPU-controlled data offloading is carried out via a 1 Gbps Ethernet link using the light-weight internet protocol (LwIP) library [53]. Broadcast datagrams [57] are employed, which is important for eliminating the latency and throughput overhead inherent in the more common connection-based communication protocols [58]. The

network spans only the radar and the external device, making it highly reliable, so most advantages of connection-based protocols are irrelevant. Note that broadcast datagrams are used in the connectionless user-datagram protocols. Each data packet sent includes a small header with sequence counters to enable data loss detection and proper data sequencing in the computer. The offloaded traces are then used for digital signal processing [59], system calibration [50], saving, or plotting in real time.

4.4 Results and Discussion

4.4.1 Firmware Throughput Efficiency, Data Reduction and End-to-End Latency

Table 4.3 illustrates the calculation of the FPGA firmware data-throughput efficiency, as well as the respective data reduction for the trace-windowing case 5, as described in Table 4.2. The modules listed in the first column correspond to the signal-processing chain in Fig. 4.5. The total efficiency is the product of all module efficiencies. When interference monitoring is disabled, a total efficiency of 98.2% is achieved. When interference monitoring is enabled, EMI-corrupt waveforms are discarded, thus reducing efficiency; however, this is not related to the firmware implementation. In summary, the proposed FPGA architecture can effectively match the radar measurement speed with minimal data loss.

The data reduction of each FPGA module is shown in the third column of Table 4.3. The *deserialization* and *DC-offset removal* modules have $DR = 1$ since they do not reduce the amount of data. The *buffer* and *interference-monitoring* modules incur marginal data loss, hence the values just above 1. The most significant data reduction in the considered case 5 occurs in the *user-defined averaging* module due to

Table 4.3: FPGA firmware efficiency and data reduction when averaging over 8 waveforms for trace-windowing case 5.

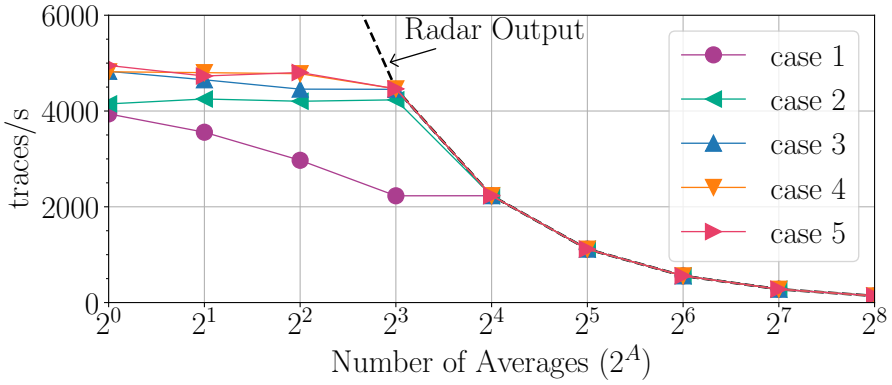
Module	Efficiency (%)	Data Reduction, DR
Deserialization	100	1
Buffer	98.2	1.018
DC-Offset Removal	100	1
Waveform Reconstruction	100	1
Interference Monitoring	(94.0)	(1.06)
User-Defined Averaging	100	8
DMAC	100	1
Waveform Segmentation	100	5
Total	98.2 (92.3)	40.72 (43.16)

averaging over eight waveforms and in the *trace-windowing* module due to windowing the traces to one-fifth of their full length. The total data reduction is the product of the DR values. As shown next, the minimum DR value necessary to offload the data without loss through the Ethernet link is about 40.

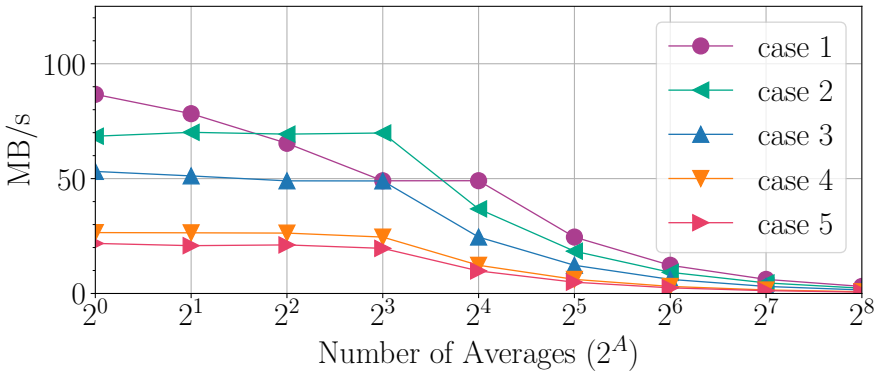
Finally, the FPGA end-to-end latency of the proposed FPGA design (provided that averaging is disabled) is measured at 224.07 µs since two reconstructed pulses (2×112 µs) are always in the pipeline, plus some registers (14 clocked at 5 ns) for data pipelining. Increasing the cumulative averaging by a factor of 2^A increases the latency by $2^{A-1} \times 112$ µs. Therefore, the worst-case end-to-end latency occurs for an average of 2^8, which is ~ 28.78 ms. This latency is reasonable and does not affect the application to real-time concealed weapon detection, as it remains below the worst-case acquisition time of 138 ms.

4.4.2 Data Offload Throughput Analysis

To evaluate the data offloading throughput, each trace is tagged with a unique identification number by the CPU. This allows for counting and tracking the traces



(a)



(b)

Figure 4.11: Data throughput analysis using 40 000 generated traces *versus* the number of averages: (a) traces per second received, (b) data throughput rate. The labels "case 1" to "case 5" refer to those described in Table 4.2.

received by the computer. The analysis employs the cases listed in Table 4.2 along with varying averaging.

Fig. 4.11 presents the data offloading throughput analysis results using 40 000 generated traces *versus* the number of averages. Fig. 4.11a shows the number of traces per second successfully offloaded to the computer. The dashed line shows the full number of traces generated by the radar (including the FPGA preprocessing chain), which is 98.2% of $4 \times 9\,090/2^A$ traces/s. It is evident that the Ethernet offload saturates at

about 4 000 to 5 000 traces/s depending on the trace length. When the number of averages is 8 or higher, there is no data loss, except in case 1 (full-length traces). For averaging below 8, the throughput improves as the traces become shorter, which is expected. For Ethernet offloading, it is advantageous to employ at least 8 averages, along with reducing the trace length by $DR_{\text{win}} = 1.33$ or more, since this fully utilizes the radar output and improves the SNR.

Fig. 4.11b shows the data throughput rate. It can be observed that the theoretical network speed of 125 MB/s is never reached, which is due to the networking overhead. Also, sending longer traces (see cases 1 or 2) results in higher data rates, which can be explained by larger data payloads requiring less networking overhead per second. This insight can be used to further increase throughput by packing shorter traces into larger network packets (not pursued here).

The proposed design approach and architecture are scalable as technology evolves, making the ADC and Ethernet data rates faster. For instance, doubling the Ethernet speed while keeping the same ADC sampling rate allows for reducing the averaging, thus leading to higher throughput (as seen in Fig. 4.11a). The enhanced throughput, currently constrained by today's commonplace technology, would provide higher trace rates, thus improving detectability. Of course, higher-bandwidth solutions are currently available, such as multi-gigabit links via Ethernet, PCIe, and USB3/4 interfaces. Provided that the employed FPGA board can support these higher-bandwidth solutions, replacing the 1 Gbps Ethernet link is straightforward.

Conversely, increasing the ADC's sampling rate would demand larger buffers and memory resources on the FPGA. For example, doubling the sampling rate or waveform period would require twice the number of memory locations per bank. The architecture would remain the same, provided that the FPGA has the memory resources to support the implementation. The FPGA throughput efficiency would not

be affected by these increases due to the proposed parallel processing approach. Certainly, a larger ADC sampling rate would also lead to challenges with data offloading.

4.4.3 Comparison to Prior Art

As shown in this work, highlighting and addressing FPGA-based design inefficiencies and throughput capabilities are of great importance for achieving a loss-free, high-throughput, and capable radar system. This is often not investigated or reported in published works, leaving a gap in these systems' performance metrics due to sub-optimal solutions. For example, the system proposed in [12] was shown to produce a reconstructed image every 0.748 ms (1 336 FPS), but the images are limited to a display refresh rate of 60 FPS. This effectively leads to 4.5% throughput efficiency. This result also includes image reconstruction, an application-specific solution not relevant to a generic receiver.

The designs proposed in [11]–[13], [15], [16], [31] use a single memory bank for channel waveform reconstruction, averaging, and offloading. Data loss occurs in these designs due to the serialized signal-processing approach, but the extent of the loss is unclear. In contrast, we present a system that can achieve high efficiency and high-throughput capabilities far exceeding the user-defined output.

The reported (or extracted from available data) waveform reconstruction times for the designs proposed in [11], [12], [14] show that they require more than 144 pulse periods to reconstruct a 100 ns waveform. Our solution constructs a 1 µs waveform in 112 pulse periods, representing a significant improvement. It is important to note that making quantifiable comparisons is difficult due to the various ET sampling rates reported, ranging from 5 GSa/s to 100 GSa/s. The ET sampling rate employed directly impacts the number of pulse periods used, the FPGA memory management,

and the temporal extent of the measurements. Comparisons are further inhibited by the lack of agreed-upon metrics for data loss and data throughput.

4.4.4 Experimental Validation with Walking People

Here, we demonstrate the ability of the proposed high-throughput radar system to capture thousands of responses from people walking across its field of view. Team members, one at a time with their consent, are asked to walk back and forth along the cross-range at a range distance of about 1 meter (similar to the scenario in Fig. 4.2). The radar system with antennas is placed outside a semi-anechoic chamber with the antennas pointing toward the chamber. In one experiment, the person walks slowly, and in another, the person walks at a normal pace. A video camera captures the person's motion, and each video frame is timestamped. This establishes the correspondence between the video capture and the radar measurement. The FPGA preprocessing employs an average of eight waveforms for trace-windowing case 5 (see Table 4.2). The measured traces are saved and plotted on a computer.

Examples of these experiments are shown in Fig. 4.12 and Fig. 4.13. In Fig. 4.12, the person walks slowly. The video captures the person's position at the start, midway, and end, along with the corresponding peaks and dips in the radargram in Fig. 4.12d. The radargram plots the slow time *versus* the fast time of 27 500 VV traces. The slow time corresponds to the time the pulse is received. The fast time corresponds to the temporal sample in the trace. Labels a, b, and c in Fig. 4.12d correspond to the video frame timestamps in Fig. 4.12a–c. A background response is obtained by averaging 27 500 traces without a person in the radar's field of view. The background signal is subtracted to enhance the back-scattered response. Fig. 4.13 is analogous to Fig. 4.12 but for measurements with a person walking at a normal pace.

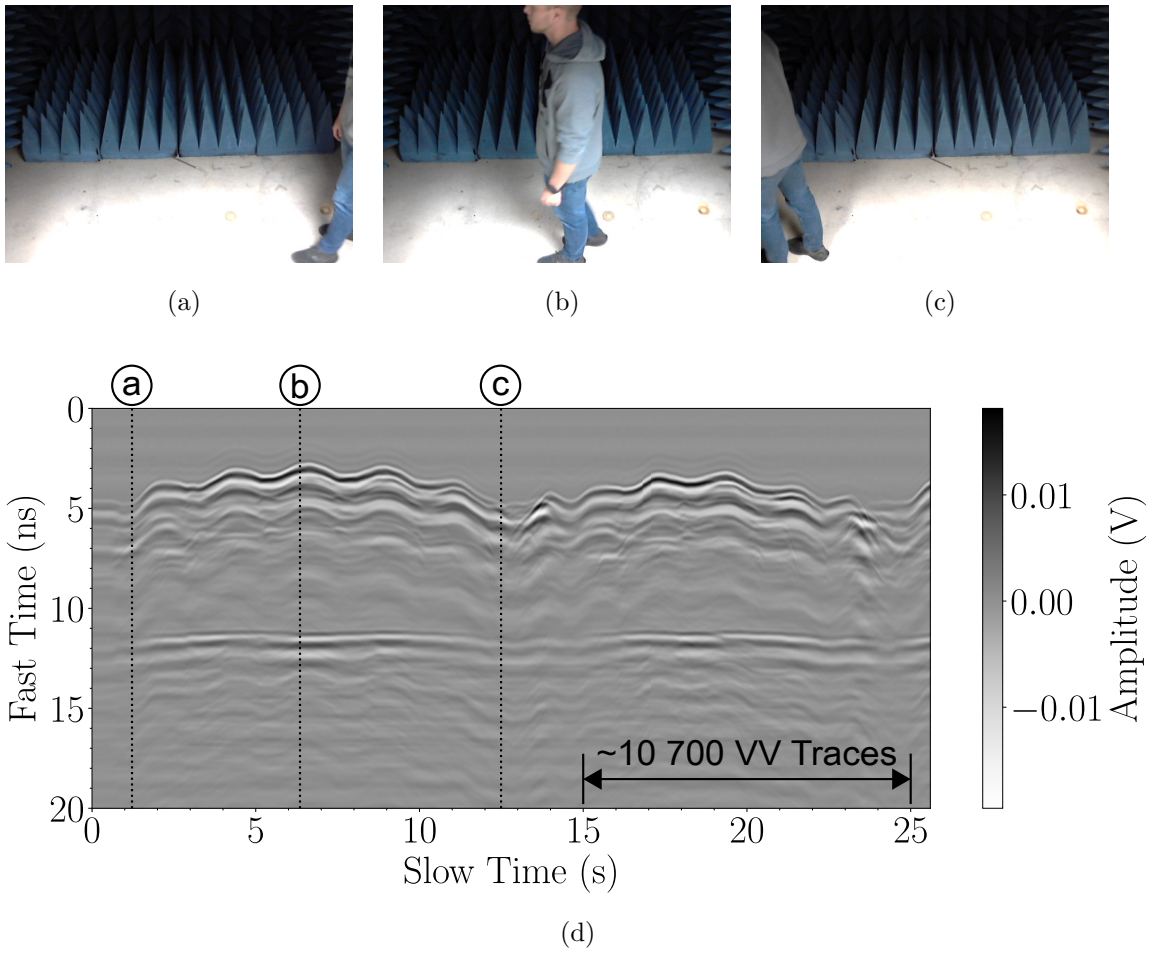


Figure 4.12: Measurements of a human walking slowly back and forth along the cross-range and at a range distance of about 1 meter from the antennas. The radar is positioned outside an open chamber with the antennas pointed toward the chamber. The person's speed is estimated to be 0.22 m/s. Video frames show the positions of the person at (a) the start, (b) midway between the Tx and Rx antennas, and (c) the end after turning around. (d) The radargram shows the slow time *versus* the fast time of the VV radar response (background signal subtracted).

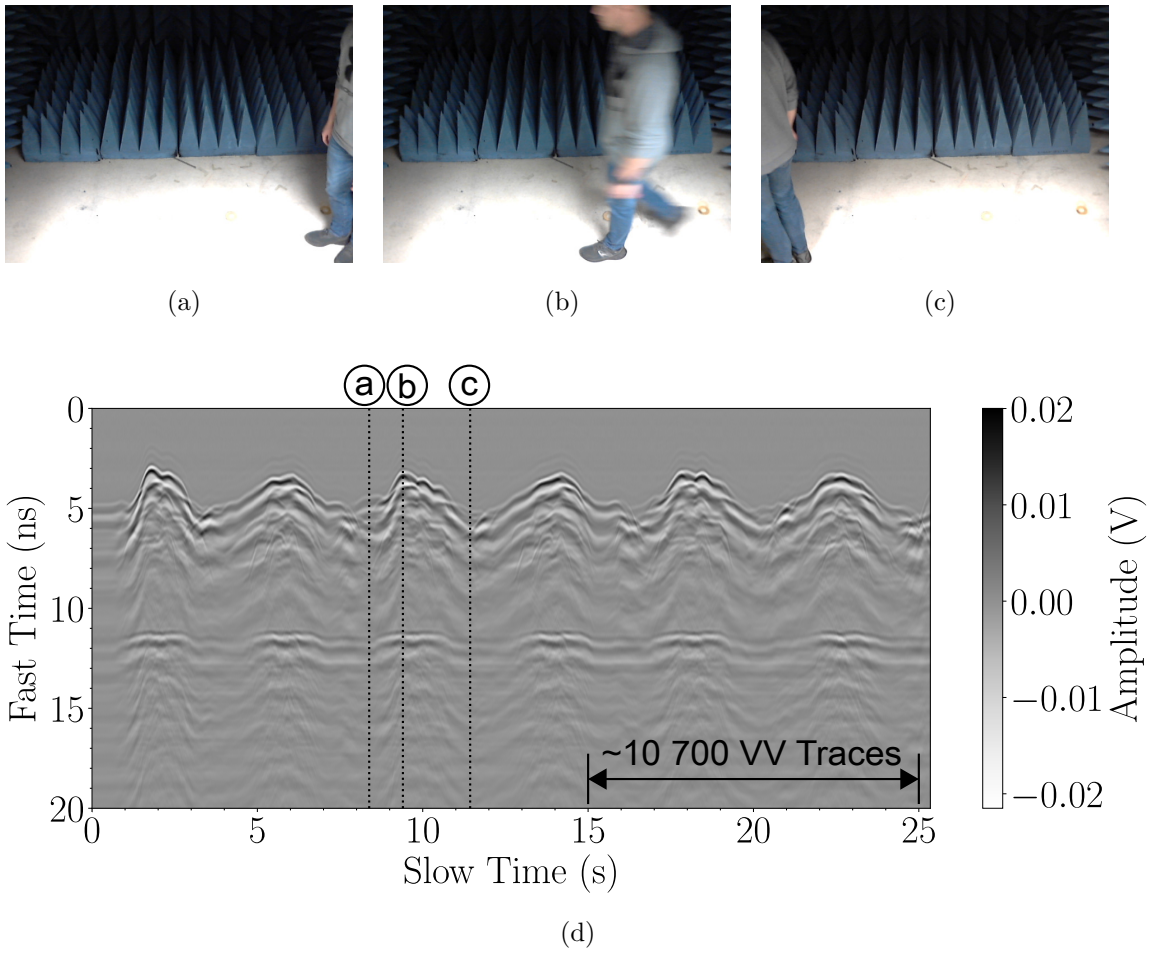


Figure 4.13: Measurements of a human walking normally back and forth along the cross-range and at a range distance of about 1 meter from the antennas. The setup is the same as that in Fig. 4.12. The person's speed is estimated to be 0.8 m/s. Video frames show the positions of the person at (a) the start, (b) midway between the Tx and Rx antennas, and (c) the end after turning around. (d) The radargram shows the slow time *versus* the fast time of the VV radar response (background signal subtracted).

The radargrams in Fig. 4.12 and Fig. 4.13 clearly show the human response at around 3.5 ns, corresponding to a range of about 1 m. The peaks and troughs seen along the slow-time axis indicate the person's movement. Peaks occur when the person is midway in the radar's field of view, whereas troughs occur when the person reaches the end of the chamber and has to turn around. The person's speed can be estimated using the timestamps of the radargram's slow-time index. Measuring from trough to trough in Fig. 4.12, the person's speed is estimated to be 0.22 m/s. Likewise, in Fig. 4.13, the person's speed is estimated to be 0.8 m/s. In both figures, late-time (on the fast-time axis) ripples are observed that are only weakly dependent on the slow time. These are associated with multi-path responses.

4.5 Conclusion

A dual-channel FPGA-based architecture is proposed for a high-throughput UWB pulsed-radar system, which leverages parallel processing within the FPGA firmware. Parallel signal preprocessing is realized through a multi-memory bank layout, drastically improving the FPGA throughput efficiency and practically eliminating the data loss provided by the radar ETSR. It is shown that the FPGA-based signal preprocessing utilizes 98.2% of the high-speed data stream from the ETSR, effectively matching its speed. The realized radar system is equipped with an Ethernet link to a computer, and it is demonstrated that it can handle a total of about 4 950 traces/s, with the limit dictated by the Ethernet capacity, not the radar system. Note that the FPGA-based design performs two simultaneous waveform reconstructions (each containing two responses) every 110 µs, thus generating over 35 000 responses per second if averaging is disabled. Even with offloading limited to 4 950 traces/s, the system still delivers 1 238 traces/s in each radar response (VV, HH, VH, and HV). This remarkable speed

makes the proposed radar system uniquely equipped for real-time radar applications targeting moving objects. Large datasets quickly become available for slowly moving objects such as people, making stochastic radar signal processing possible. Such processing provides powerful target detection and identification tools, which can successfully counteract environmental noise and radar clutter in emerging sensing and imaging UWB applications.

We also show how to leverage the speed of the proposed FPGA-based system to perform additional user-defined signal-preprocessing tasks besides ET waveform reconstruction, namely averaging, EMI suppression, and trace windowing. Averaging improves the SNR while reducing the amount of data to be offloaded to external devices. Trace windowing also greatly aids data reduction. EMI suppression allows for radar operation despite interference from wireless communications (e.g., Wi-Fi).

For the first time, FPGA firmware design strategies are delineated that are critical for improving the throughput efficiency of FPGA-controlled radar systems. The practical problem of data offloading is also discussed in the case of an Ethernet link since this offloading creates a bottleneck when additional signal processing is carried out on external devices. It is demonstrated that enabling data-reduction processing (averaging and trace windowing) within the FPGA firmware is critical for the optimal utilization of the high-speed radar output, i.e., achieving the best SNR for the given maximum data offloading rate.

References

[1] "First report and order, revision of part 15 of commission's rule regarding UWB transmission system FCC 02-48," Federal Communications Commission (FCC), Washington, DC, USA, Tech. Rep. FCC 02-48, Apr. 2002.

[2] J. Sachs, *Handbook of Ultra-Wideband Short-Range Sensing*, 1st. Weinheim, Germany: Wiley-VCH Verlag & Co., 2013.

[3] Y. Masui, A. Toya, M. Sugawara, *et al.*, "Differential equivalent time sampling receiver for breast cancer detection," in *2017 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, Turin, Italy: IEEE, Oct. 2017, pp. 1–4.

[4] D. Oloumi, A. Bevilacqua, and M. Bassi, "UWB radar for high resolution breast cancer scanning: System, architectures, and challenges," in *2019 IEEE International Conference on Microwaves, Antennas, Communications and Electronic Systems (COMCAS)*, Tel-Aviv, Israel: IEEE, Nov. 2019, pp. 1–4.

[5] R. Feghhi, R. Winter, F. Sabzevari, and K. Rambabu, "Design of a low-cost UWB time-domain radar system for subcentimeter image resolution," *IEEE Trans. Microw. Theory Techn.*, vol. 70, no. 7, pp. 3617–3628, Jul. 2022.

[6] N. K. Nikolova and T. Thayaparan, "Ultra-wideband (UWB) high-resolution noise radar for concealed weapon detection," Defence Research and Development Canada, Tech. Rep. TR 2013-160, Feb. 2014.

[7] J. J. McCombe, N. K. Nikolova, M. S. Georgiev, and T. Thayaparan, "Clutter removal in the automatic detection of concealed weapons with late time responses," in *2013 European Radar Conference (EuRAD)*, IEEE, Nuremberg, Germany, Oct. 2013, pp. 53–56.

[8] N. K. Nikolova and J. J. McCombe, *On-body concealed weapon detection system*, U.S. Patent No. 10,229,328, Mar. 2019.

[9] A. D. Pitcher, "Compact low-cost ultra-wideband pulsed-radar system," M.A.Sc. thesis, Department of Electrical and Computer Engineering, McMaster University, Hamilton, ON, Canada, Aug. 2019.

[10] A. D. Pitcher, C. W. Baard, M. Georgiev, and N. K. Nikolova, "Equivalent-time sampling ultra-wideband pulsed-radar receiver: RF front-end design," Electromagnetic Vision (EMVi) Research Laboratory, McMaster University, Hamilton, ON, Canada, Tech. Rep. EMVi-R-122, Sep. 2024.

[11] Y. Yang and A. Fathy, "Near-real-time data acquisition and beamforming for UWB see-through-wall system," in *2007 IEEE Workshop on Signal Processing Applications for Public Security and Forensics*, Washington, DC, USA: IEEE, Apr. 2007, pp. 1–4.

[12] Y. Yang and A. Fathy, "Development and implementation of a real-time see-through-wall radar system based on FPGA," *IEEE Trans. Geosci. Remote Sens.*, vol. 47, no. 5, pp. 1270–1280, May 2009.

[13] C. Chen, S. Wu, S. Meng, J. Chen, G. Fang, and H. Yin, "Application of equivalent-time sampling combined with real-time sampling in UWB through-wall imaging radar," in *2011 International Conference on Instrumentation, Measurement, Computer, Communication and Control*, Beijing, China: IEEE, Oct. 2011, pp. 721–724.

[14] Q. Liu, Y. Wang, and A. Fathy, "A compact integrated 100 GS/s sampling module for UWB see through wall radar with fast refresh rate for dynamic real time imaging," in *2012 IEEE Radio and Wireless Symposium*, Santa Clara, CA, USA: IEEE, Jan. 2012, pp. 59–62.

[15] Q. Liu, Y. Wang, and A. Fathy, "Towards low cost, high speed data sampling module for multifunctional real-time UWB radar," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 49, no. 2, pp. 1301–1316, Apr. 2013.

[16] M. Saad, A. Maali, M. S. Azzaz, and M. Benssalah, "An efficient FPGA-based implementation of UWB radar system for through-wall imaging," *International Journal of Communication Systems*, e5510, May 2023.

[17] M. Saad, A. Maali, M. S. Azzaz, A. Bouaraba, and M. Benssalah, "Development of an IR-UWB radar system for high-resolution through-wall imaging," *Progress in Electromagnetic Research (PIER) C*, vol. 124, pp. 81–96, Sep. 2022.

[18] A. Srivastav, D. Ariando, and S. Mandal, "An FPGA-based flexible and MIMO-capable GPR system," in *2018 17th International Conference on Ground Penetrating Radar (GPR)*, Rapperswil, Switzerland: IEEE, Jun. 2018, pp. 1–6.

[19] L. Tantiparimongkol and P. Phasukkit, "IR-UWB pulse generation using FPGA scheme for through obstacle human detection," *MDPI Sensors*, vol. 20, no. 3750, pp. 1–21, Jul. 2020.

[20] Y. López, M. García-Fernández, G. Álvarez-Narciandi, and F. Las-Heras, "Unmanned aerial vehicle-based ground-penetrating radar systems: A review," *IEEE Geosci. Remote Sens. Mag.*, vol. 10, no. 2, pp. 66–86, Apr. 2022.

[21] C. Noviello, G. Gennarelli, G. Esposito, *et al.*, "An overview on down-looking UAV-based GPR systems," *MDPI Remote Sensing*, vol. 14, no. 3245, pp. 1–28, Jul. 2022.

[22] M. García-Fernández, G. Álvarez-Narciandi, Y. López, and F. Las-Heras, "Array-based ground penetrating synthetic aperture radar on board an unmanned aerial vehicle for enhanced buried threats detection," *IEEE Trans. Geosci. Remote Sens.*, vol. 61, pp. 1–18, May 2023.

[23] "Keysight technologies InfiniiVision 6000 X-series oscilloscope," Keysight Technologies, Inc., Datasheet 5991-4087EN, Dec. 2024.

[24] "Infiniium Z-series oscilloscopes," Keysight Technologies, Inc., Datasheet 5991-3868EN, Oct. 2019.

[25] "Infiniium S-series oscilloscopes," Keysight Technologies, Inc., Datasheet 5991-3904EN, May 2022.

[26] "6 series B MSO: Mixed signal oscilloscope," Tektronix, Inc., Datasheet 48W-61716-09, May 2023.

[27] "Mixed signal and digital phosphor oscilloscopes: MSO/DPO70000DX series," Tektronix, Inc., Datasheet 55W-23446-40, Aug. 2023.

[28] "ADC12DJ5200RF 10.4-GSPS single-channel or 5.2-GSPS dual-channel, 12-bit RF-sampling analog-to-digital converter (ADC)," Texas Instruments, Inc., Datasheet SLVSEN9F, Rev. F, Apr. 2024.

[29] "ADC08DJ5200RF 10.4-GSPS single-channel or 5.2-GSPS dual-channel, 8-bit RF-sampling analog-to-digital converter (ADC)," Texas Instruments, Inc., Datasheet SLVSEO1A, Rev. A, Aug. 2022.

[30] "12-bit, 6 GSPS/10.25 GSPS, JESD204B RF analog-to-digital converter," Analog Devices, Inc., Datasheet AD9213, Rev. A, Mar. 2020.

[31] Y. Wanyu, Z. Yijiu, Y. Zhonghao, and L. Dan, "Design of random equivalent sampling control module based on FPGA," in *2019 14th IEEE International Conference on Electronic Measurement & Instruments (ICEMI)*, Changsha, China: IEEE, Nov. 2019, pp. 1027–1032.

[32] "AN1365: Si5361/62/63 lock time parameters," Skyworks Solutions, Inc., Application Note AN1365, Nov. 2022.

[33] I. Collins, "Phase alignment and control of the ADR4356/ADF5356 devices," Analog Devices, Inc., Technical Article, Aug. 2017.

[34] "SY89295U 2.5V/3.3V 1.5GHz precision LVPECL programmable delay," Micrel, Inc., Datasheet SY89295U, Mar. 2011.

[35] "Zedboard," Digilent, Inc., Hardware User's Guide, v1.1, Aug. 2012.

[36] *Garrett Paragon: Walk through metal detector*, Garrett Metal Detectors, Feb. 2024. [Online]. Available: https://garrett.com/security/walk-through/paragon-walk-through-metal-detector.

[37] *Pro:Vision 3: High performance advanced passenger screening*, Leidos Holdings, Inc., 2024. [Online]. Available: https://www.leidos.com/markets/aviation/security-detection/aviation-checkpoint/people-screening.

[38] *Mirtle 30: Metal & non metal detector*, CWT Aerospace Services Pte. Ltd., 2022. [Online]. Available: https://www.cwtaerospace.com/mirtle30.

[39] AKELA, "Final report - demonstration of a concealed weapons detection system using electromagnetic resonances," *US Department of Justice*, Jan. 2001.

[40] A. Agurto, Y. Li, G. Y. Tian, N. Bowring, and S. Lockwood, "A review of concealed weapon detection and research in perspective," in *2007 IEEE International Conference on Networking, Sensing and Control*, London, UK: IEEE, Apr. 2007, pp. 443–448.

[41] A. Vasalos, "Late time response analysis in UWB radar for concealed weapon detection: Feasibility study," Ph.D. dissertation, Dept. of Electronic, Electrical & Computer Engineering, Univ. of Birmingham, Birmingham, UK, Sep. 2010.

[42] S. W. Harmer, S. E. Cole, N. J. Bowring, N. D. Rezgui, and D. Andrews, "On body concealed weapon detection using a phased antenna array," *Progress In Electromagnetics Research*, vol. 124, pp. 187–210, Jan. 2012.

[43] A. D. Pitcher, C. W. Baard, and N. K. Nikolova, "Design and performance analysis of a picosecond pulse generator," *IEEE Trans. Instrum. Meas.*, vol. 71, pp. 1–14, Aug. 2022.

[44] D. J. Farris and G. S. Sawicki, "The mechanics and energetics of human walking and running: A joint level perspective," *Journal of The Royal Society Interface*, vol. 9, no. 66, pp. 110–118, Jan. 2012.

[45] "300MHz to 6GHz Type:08 lightweight open boundary quad-ridged broadband horn antenna," Fei Teng Wireless Technology (FT-RF) Co., Ltd., Datasheet HR-03M06G08-NF, 2021.

[46] "Ultra series crystal oscillator Si545 data sheet," Skyworks Solutions, Inc., Datasheet Si545, Rev. 206613A, May 2023.

[47] "CDCLVP1102 two-LVPECL output, high-performance clock buffer," Texas Instruments, Inc., Datasheet SCAS884D, Rev. D, Dec. 2015.

[48] "CDCLVP1204 four LVPECL output, high-performance clock buffer," Texas Instruments, Inc., Datasheet SCAS880F, Rev. F, Sep. 2015.

[49] "ADS42LBx9 14- and 16-bit, 250-MSPS, analog-to-digital converters," Texas Instruments, Inc., Datasheet SLAS904F, Rev. F, May 2016.

[50] A. D. Pitcher, M. Georgiev, and N. K. Nikolova, "Correcting timebase errors in ultra-wideband equivalent-time sampling receivers," in *2024 21st European Radar Conference (EuRAD)*, Paris, France: IEEE, Nov. 2024, pp. 47–50.

[51] *Zynq-7000 SoC data sheet: Overview*, Xilinx, Inc. Datasheet, Jul. 2018. [Online]. Available: https://docs.amd.com/v/u/en-US/ds190-Zynq-7000-Overview.

[52] *Vivado design suite 2018.3 - HLx editions*, AMD, Inc. Mar. 2019. [Online]. Available: https://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/vivado-design-tools/archive.html.

[53] "Xilinx standalone library documentation: OS and libraries document collection," AMD, Inc., Reference Manual UG643 v2018.3, Dec. 2018.

[54] C. E. Cummings, "Clock domain crossing (CDC) design & verification techniques using systemverilog," Sunburst Design, Inc., Tech. Rep., 2008. [Online]. Available: http://www.sunburst-design.com/papers/CummingsSNUG2008Boston_CDC.pdf.

[55] C. E. Cummings, "Simulation and synthesis techniques for asynchronous FIFO design," Sunburst Design, Inc., Tech. Rep., 2002. [Online]. Available: http://www.sunburst-design.com/papers/CummingsSNUG2002SJ_FIFO1.pdf.

[56] "FIFO generator v13.2: LogiCORE IP product guide," Xilinx, Inc., Datasheet PG057 (v13.2), Oct. 2017.

[57] J. Mogul, *RFC 0919: Broadcasting internet datagrams*, RFC Editor, Oct. 1984.

[58] W. Eddy, *RFC 9293: Transmission control protocol (TCP)*, RFC Editor, Aug. 2022.

[59] M. Georgiev, "The digital signal processing pipelines (DSPPL) suite," Electromagnetic Vision (EMVi) Research Laboratory, McMaster University, Hamilton, ON, Canada, Tech. Rep. EMVi-R-121, Sep. 2024.

CHAPTER 5:

CONCLUSIONS AND FUTURE WORK

5.1 Conclusion

A high-throughput ultra-wideband (UWB) pulsed radar system has been developed as a compact low-cost system, which achieves accuracy on par with bench-top high-grade instruments (e.g., waveform generators and high-speed oscilloscopes). New design approaches and system architectures have allowed for developing and demonstrating: (i) an ultra-stable picosecond pulse generator, (ii) an accurate high-speed equivalent-time sampling receiver (ETSR), and (iii) a parallelized field-programmable gate array (FPGA) architecture, which enables a low-cost dual-channel UWB pulsed-radar system with ultra-fast processing and data throughput [1]–[3]. All results are supported by fabricated and tested hardware (realized in printed circuit technology), making the system readily available for replication and use as a versatile UWB radar system.

The proposed designs are compact and cost-effective. For the 0.5 GHz to 5 GHz frequency range, where wavelengths vary from approximately 600 mm to 60 mm, the picosecond pulse generator printed circuit board (PCB) measures 114 mm by 55 mm by 16 mm, while the ETSR has dimensions of 305 mm by 135 mm by 30 mm. The

entire UWB system can be manufactured for $5,500$ USD, with each picosecond pulse generator board costing 500 USD and the ETSR priced at $4,500$ USD.

An important conclusion from the presented work is that modern UWB radar technology has been lacking metrics and measurement procedures for evaluating the performance of both the transmitters (the pulse generators) and the time-sampling receivers. The lack of complete and standardized information about a UWB radar system and/or its modules inhibits progress toward innovative applications. The hardware limitations remain unclear, and comparisons of existing designs or devices are incomplete due to missing evaluation metrics in the literature. Thus, the proposed rigorous system of quantitative UWB generator and receiver metrics fills a gap and will enable future sensing and imaging system designers to make optimal choices for their system components. Importantly, any radar system design must account for the noise and jitter in the generator and the time-sampling receiver, as these set the noise floor and the dynamic range of the overall system. In addition, more common metrics, such as frequency bandwidth and output power, must reflect the entire system's performance, not just one of its components.

5.2 Future Work

There are many opportunities to further improve the proposed ETSR and to use it in novel methods and systems for UWB target detection, classification and identification. The proposed UWB radar system can also be used in imaging applications when mounted on scanning or mobile platforms. Provided here are the short-term (1 – 2 years) improvements that can be made to the work presented here and the long-term (2 – 5 years) progress I wish to see in this area of research.

5.2.1 Short-Term Improvements

5.2.1.1 ETSR RF Front-End Improvements

The work in Chapter 3 demonstrates that the proposed ETSR can achieve a -10 dB receiver bandwidth over 6 GHz. However, when paired with the picosecond pulse generator proposed in Chapter 2 (pulse bandwidth of ≈ 4.85 GHz), the compounded radar bandwidth, i.e., the bandwidth of the pulse at the output of the receiver, is limited to approximately 3.5 GHz at the -10 dB level. This is attributed to the compounding of the high-frequency roll-offs in the generated pulse spectrum (Fig. 2.18b) and in the receiver input bandwidth (Fig. 3.8).

Another metric of the proposed ETSR that deserves further work for improvement is its spurious free dynamic range (SFDR). The current design matches the SFDR performance of the real-time bench-top high-speed oscilloscopes up to about 2 GHz (see Fig. 3.9), but as the frequency increases beyond 2 GHz, the SFDR of the proposed receiver starts to decline, and at 5 GHz, it is already more than 20 dBc below that of the real-time (RT) oscilloscopes. This is attributed to the significant harmonic generation by the equivalent-time sampling circuitry above 2 GHz.

The following work should be pursued to achieve the above improvements of the ETSR front-end.

1. An investigation should be carried out to identify the suboptimal circuit design or component choices which limit the ETSR's receiver bandwidth. For instance, pin-compatible track and hold (T&H) amplifiers with 18 GHz analog bandwidths [4] are available, which should mitigate the -3 dB loss at 5 GHz caused by the currently used T&H amplifier [5]. Preliminary comparisons of the two chipsets within the proposed ETSR are presented in Fig. 5.1. However, this addresses

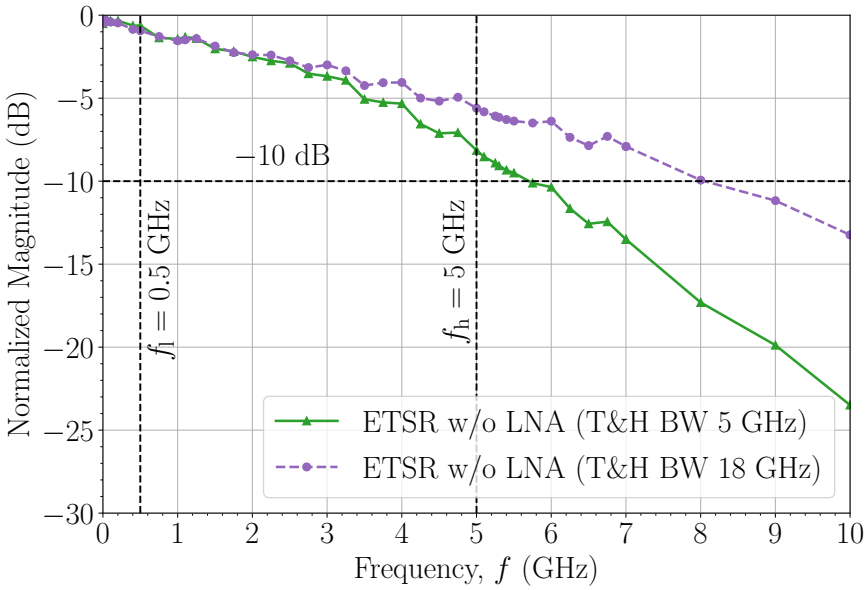


Figure 5.1: ETSR (without LNA) receiver bandwidth with 5 GHz and 18 GHz analog bandwidth T&H amplifiers.

only the −3 dB loss, whereas the ETSR prototype exhibits a total loss of −8 dB at 5 GHz.

2. Design enhancements should be implemented to reduce the spurious harmonic generation within the ETSR toward improving the receiver SFDR. To this end, the following design changes are promising upon further inspection of the employed components.

   - The T&H amplifier SFDR performance above 2 GHz depends on the input clock power [5]; therefore, this power level should be investigated and, if necessary, the clocking circuit should be re-designed to provide a sufficient power level.
   - The analog-to-digital converter (ADC) features a digital gain setting, which allows for trading signal-to-noise ratio (SNR) with SFDR (refer to Figures

15 and 16 in [6]); therefore, tuning this setting may be beneficial for the receiver's SFDR.

- To optimize the ADC even-harmonic performance at high input frequencies, the use of back-to-back transformers is recommended by the datasheet [6] but is not implemented in the current prototype.

5.2.1.2 ETSR Timebase Calibration

The results obtained using the calibration procedure described in Chapter 3 and Appendix A clearly indicate a nearly linear relationship between device temperature and the errors in the delays produced by the programmable delay chip (PDC). Currently, calibration is achieved using a bench-top radio frequency (RF) sinusoidal generator [7] to produce a single tone at 30 MHz. This means the radar must be brought off-line (disconnected from the antennas) to calibrate. Various improvements can be implemented to simplify calibration without disrupting the radar setup.

1. An RF switch can be incorporated in the receiver's RF front-end to select between the antenna inputs (RxA and RxB) and the input from the sinusoidal generator. Moreover, an on-chip sinusoidal generator can be embedded into the proposed ETSR (e.g., the direct digital synthesis chip [8]) to avoid the use of an external generator. Such an internally embedded single-tone generator must be switched off when not in use to avoid electromagnetic interference (EMI) with the ETSR. The jitter of the sinusoidal generator must be on par or better than the expected ETSR jitter. For example, as presented in Chapter 3, the root-mean-square (RMS) jitter of the ETSR is approximately 3.1 ps. At the same time, the RF generator's RMS jitter is less than a picosecond [7].

2. It would be very beneficial if the FPGA or central processing unit (CPU) could

perform the calibration calculations and provide the corrected timebase. Currently, this is done on an external computer.

3. Moreover, the proposed ETSR has been designed to carry two temperature sensors. These sensors are tied into the fan controller to monitor and control the temperature of the ETSR. The sensors are located close to the ADC and the fan controller chip, and their readings can be accessed by the CPU. Additionally, temperature sensors can be added to the FPGA board through peripheral modules [9], thus enabling real-time monitoring of the PDC chip. Note that temperature drift while the system operates is unavoidable and may be significant depending on the deployment environment. Our preliminary research has indicated that predictive models can be built based on statistically large datasets for the PDC actual delays *versus* temperature. These can be acquired before the radar is deployed. We emphasize that the delay errors and their temperature dependence are device-specific.

   We have already obtained an extensive dataset of the actual delays for all employed taps *versus* temperature for one of our ETSR prototypes. The measurement campaign involved calibrating the ETSR every minute for over 350 consecutive hours while reading out the device temperature at each calibration instance. A total of 20 694 actual-delay estimates have been obtained *versus* temperature. We have then built a simple linear regression model of the actual PDC delays as a function of temperature. Initial results are very promising, but future research is needed to evaluate the model predictions' accuracy further. Moreover, employing alternative models based on higher-order regression and machine learning should be explored for accuracy.

This research should be pursued further, and the delay-*versus*-temperature model

should be embedded within the embedded system to generate a correct timebase without interrupting the radar operation.

5.2.1.3 Hardware Miniaturization

Hardware development is evolving fast. Since developing our ETSR, newer compact FPGA boards have become available [10]–[13]. These can replace the FPGA board [14] used in this work with a fraction of the size. I envision a compact radar system that employs the architecture presented here but in a smaller form factor and with interchangeable modules (e.g. transmitters and FPGAs). I emphasize that the proposed ETSR architecture is not specific to pulse signals; it can sample any waveform (including continuous-wave signals) whose spectrum is within the receiver's bandwidth.

5.2.1.4 FPGA and CPU Firmware Enhancements

Currently, a few signal preprocessing operations take place on the external computer. These should be moved to the embedded hardware platform to run on either the FPGA or the CPU.

1. Building the calibrated timebase with the non-uniform sampling instants can be implemented on the CPU. This would require loading and storing the latest calibration with the actual PDC tap delays. Then, the CPU would rebuild the calibrated timebase whenever the temperature fluctuates and apply it to the reconstructed waveforms. Performing this within the FPGA is also possible, but its implementation would be more difficult.

2. Once the calibrated timebase with the non-uniform sampling instants is available in the system on a chip (SoC) CPU, the linear interpolation, which casts

the sampled waveforms from the non-uniform timebase to the uniform 50-ps timebase, should also be implemented on the CPU.

Migrating these to the embedded hardware platform will reduce the offloaded data and accelerate the overall signal-processing time.

Finally, the CPU firmware is supported by a bare-metal operating system provided with the Vivado Design Suite [15]. The codebase runs using only one of the two available CPUs and is limited to a superloop architecture due to its ease of implementation. For example, the high-throughput capabilities presented here were achieved by optimizing the serialized processing steps within the superloop's infinite loop. However, this approach has two main problems. First, any additional processing step, like gathering the ETSR board temperatures, slows down the time it takes the loop to complete. Second, if data is unavailable for the CPU, the current processing step halts all subsequent steps until the data becomes available. These impact the overall CPU throughput efficiency and effectively waste computational time. For example, gathering board temperatures has to be limited as it takes approximately 498 µs. Meanwhile, the radar data is available once every 112 µs.

The following is proposed for further firmware enhancement.

1. Transition to a thread-based architecture allowing the CPU to be freed while the processing steps wait for data. This will enable the CPU to perform other non-critical tasks, such as allowing the user to change parameters or gathering ETSR board temperatures while ensuring high-throughput capabilities. This will improve the efficiency of a single CPU processing pipeline.

2. Recent advancements in symmetric multiprocessing (SMP) real-time operating systems (RTOSs), such as FreeRTOS [16] and the Zephyr project [17], have enabled multiple embedded processors to share a unified memory and operating

system. Previously, such systems would have relied on an asymmetric multiprocessing architecture or required a hypervisor, allowing each CPU to execute its own RTOS kernel [18]. FreeRTOS is natively supported on the chosen Zynq SoC, while the Zephyr project provides development builds targeting the same chipset [19]. This makes it feasible to implement SMP features, enabling the use of the second CPU within the same operating system. This would allow the operating system to schedule parallel processing tasks and assign them to any of the two CPUs, thereby improving the overall CPU processing efficiency. For example, one CPU could be collecting the latest waveform reconstruction. Meanwhile, the second CPU would apply the calibrated timebase and interpolation on the previous waveform reconstruction.

5.2.1.5 Considerations for Mobile Deployments

Currently, the proposed UWB radar system is compact and lightweight for portable deployments. This means that the radar can be easily moved from one deployment site to another. However, the proposed prototype still assumes that an electrical outlet is available to provide power. This is not necessarily the case when the radar is to be deployed on a mobile platform. Therefore, as the prototype moves toward mobile applications that depend on batteries to supply power, a number of improvements can be made to the overall system.

First, the system's overall power consumption and efficiency must be evaluated. This has not yet been conducted, and improvements can be made to the overall system design in terms of power consumption and efficiency as described below.

1. Utilize the already integrated power monitoring circuitry for real-time power consumption monitoring of the picosecond pulse generator and ETSR with

FPGA system. This hardware capability currently exists; however, the firmware necessary for monitoring needs to be developed.

2. Improve the DC-to-DC voltage regulation, focusing on improving the overall system efficiency, i.e. minimizing power loss.

3. Improve the FPGA resource utilization and CPU efficiency. Minimizing the overall system power consumption can be improved by minimizing the FPGA resource utilization or by disabling unused FPGA logic.

   Additionally, the current firmware runs continuously with a 100% duty cycle. It may be beneficial to lower that duty cycle to decrease the overall power consumption of the system. This would require allowing the CPU and FPGA to go to a lower power state where measurements are not taken for a short period of time.

Finally, the current system does not rely on wireless data offload methods or long-term storage. In terms of data offload and storage, it has been designed for portable applications where a wired Ethernet network is assumed. Even for mobile applications, the initial vision is to provide an onboard signal-processing computer [20], which is lightweight, powerful and compact. In this case, only small data packets need to be transmitted wirelessly carrying the reconstructed scene images or the coordinates of detected objects of interest. This method is far more reliable than wireless transmission of large data streams of radar signals, as this would be prone to jamming and interference. If wireless connections are developed to handle gigabit per second (Gbps) data rates reliably, it is potentially possible to investigate this implementation. Additionally, to take full advantage of the radar data stream capabilities, the digital signal processing (DSP) algorithms should consider parallelization. Preliminary DSP modules within [21] cannot match the radar's speed.

5.2.2 Long-Term Improvements: Advancements Aiding Detection and Identification

Much of the future work will integrate the proposed UWB radar system with target detection, classification and identification algorithms. For example, in the concealed weapon detection (CWD) application, security personnel would appreciate not only the early warning of a potential threat but also the likelihood of the presence of a weapon class (e.g., rifle, handgun, knife, grenade) under a person's clothing or in a bag. Several hardware- and deployment-dependent signal-processing steps are necessary to achieve successful algorithm performance.

1. **Background De-embedding:** Background de-embedding is essential to suppress radar clutter. The deployment of CWD radar is likely to be indoors, where clutter is significant, masking the radar return from the target of interest. Moreover, the deployment environment may be dynamic due to the movement of people and/or vehicles. The background signal components are also due to the mutual coupling between the antennas. In summary, the background component of the received radar signal carries no information about the target; thus, its de-embedding is desirable since it greatly improves the detection outcome.

   A common technique employs background subtraction to eliminate stationary clutter. However, this requires regular background measurements of a static deployment scenario. This technique cannot deal with dynamic background environments. To overcome this limitation, machine-learning, artificial-intelligence, and deep-learning models are being developed to address dynamic and time-varying clutter [22]–[24]. These algorithms allow the radars to adapt to changing environments and learn from prior dynamic scenarios. Such *cognitive* radars are more likely to succeed in detection tasks indoors. Therefore, future research

should focus on this emerging signal-processing field and develop algorithms for effective and adaptive background de-embedding even in the most complex and cluttered deployment scenarios.

2. **Extracting System-Independent Target Features:** In order to detect and identify a target, certain features in its radar return must be defined and extracted. These features serve as inputs to the detection and classification algorithms. Various features can be extracted from the early-time and late-time portions of the back-scattered signals, e.g., radar-cross section, polarization ratios, complex resonant frequencies, early-to-late-time energy ratios [25]–[32]. It is critical that the features can be reliably extracted regardless of the deployment scenario. They must also be independent of the employed antennas and the specific radar system. Satisfying the first requirement depends mainly on the effectiveness of the background de-embedding. The second requirement, however, requires a different signal processing step, namely *system transfer-function de-embedding*. This de-embedding step is important for employing target detection and identification based on feature libraries for the objects of interest. These libraries must be system-independent to be applicable across multiple radar systems and all antennas chosen for the specific deployment. Thus, future work must develop effective methods to remove the impact of the antenna and radar hardware transfer functions on the objects' features.

3. **Development of Object Feature Libraries:** As radar hardware and signal-processing algorithms evolve, it is important to focus on defining system-independent sets of features that uniquely characterize the back-scattering from objects of interest. This research area is in its infancy, so rigorous theory, measurement approaches, and feature extraction algorithms still need to be developed. A recent

study highlighted that only nine publicly available datasets use UWB radar and are available for download [22]. Most of these target motion detection, gesture recognition and localization applications of UWB radar. However, numerous other applications of UWB radar are emerging. For example, in CWD applications, feature sets are needed for various *threat* (e.g., handguns, knives, explosive vests, grenades) and *non-threat* (e.g., water bottles, wallets, keys) objects. The radar features of handheld devices (e.g. mobile phones, tablets) and laptops are also of interest as those may be considered a *threat* in certain establishments (e.g., data centers).

The proposed UWB radar system has the unique advantage of unmatched measurement speed, generating over 9 000 waveforms per second on each of the four radar channels. Thus, it can be leveraged to generate enormous amounts of data. This should be exploited to benefit the emerging field of target feature extraction for radar detection and identification.

References

[1] A. D. Pitcher, C. W. Baard, and N. K. Nikolova, "Design and performance analysis of a picosecond pulse generator," *IEEE Trans. Instrum. Meas.*, vol. 71, pp. 1–14, Aug. 2022.

[2] A. D. Pitcher, C. W. Baard, M. Georgiev, and N. K. Nikolova, "Accurate high-speed equivalent-time sampling receiver: Architecture and performance metrics," *IEEE Trans. Instrum. Meas.*, pp. 1–15, Mar. 2025.

[3] A. D. Pitcher, M. Georgiev, N. K. Nikolova, and N. Nicolici, "Parallelized field-programmable gate array data processing for high-throughput pulsed-radar systems," *MDPI Sensors*, vol. 25, no. 239, pp. 1–25, Jan. 2025.

[4] "HMC661LC4B wideband 4 GS/s track-and-hold amplifier DC - 18 GHz," Analog Devices, Inc., Datasheet HMC661LC4B, v03.0615.

[5] "HMC760LC4B wideband 4 GS/s track-and-hold amplifier DC - 5 GHz," Analog Devices, Inc., Datasheet HMC760LC4B, v01.0514.

[6] "ADS42LBx9 14- and 16-bit, 250-MSPS, analog-to-digital converters," Texas Instruments, Inc., Datasheet SLAS904F, Rev. F, May 2016.

[7] "EXG X-series signal generator N5173B microwave analog 9 KHz to 13, 20, 31.8, or 40 GHz," Keysight Technologies, Inc, Datasheet 5991-3132EN, Feb. 2023.

[8] "20 mW power, 2.3 V to 5.5 V 75 MHz complete DDS," Analog Devices, Inc., Datasheet AD9834, Rev. D, Mar. 2014.

[9] "PmodTC1: Board reference manual," Digilent, Inc., Reference Manual, Rev. A, Apr. 2016. [Online]. Available: https://digilent.com/reference/_media/reference/pmod/pmodtc1/pmodtc1_rm.pdf.

[10] "Mars ZX2 SoC module," Enclustra FPGA Solutions, User Manual, version 08, Feb. 2021. [Online]. Available: https://www.enclustra.com/en/products/system-on-chip-modules/mars-zx2/.

[11] "Mars ZX3 SoC module," Enclustra FPGA Solutions, User Manual, version 09, Sep. 2022. [Online]. Available: https://www.enclustra.com/en/products/system-on-chip-modules/mars-zx3/.

[12] "Mercury ZX1 SoC module," Enclustra FPGA Solutions, User Manual, version 07, Jan. 2022. [Online]. Available: https://www.enclustra.com/en/products/system-on-chip-modules/mercury-zx1/.

[13] "Mercury ZX5 SoC module," Enclustra FPGA Solutions, User Manual, version 06, Feb. 2021. [Online]. Available: https://www.enclustra.com/en/products/system-on-chip-modules/mercury-zx5/.

[14] "Zedboard," Digilent, Inc., Hardware User's Guide, v1.1, Aug. 2012.

[15] *Vivado design suite 2018.3 - HLx editions*, AMD, Inc. Mar. 2019. [Online]. Available: https://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/vivado-design-tools/archive.html.

[16] "Symmetric multiprocessing (SMP) with FreeRTOS," Amazon Web Services, Tech. Rep., Jan. 2025. [Online]. Available: https://www.freertos.org/Documentation/02-Kernel/02-Kernel-features/13-Symmetric-multiprocessing-introduction.

[17] "Zephyr Project," Zephyr Project, a Linux Foundation Project, Tech. Rep., 2025. [Online]. Available: https://zephyrproject.org/.

[18] T. O'Neal, "Multi-OS support (AMP & hypervisor)," Xilinx Wiki, Tech. Rep., Jan. 2021. [Online]. Available: https://xilinx-wiki.atlassian.net/wiki/spaces/A/pages/18841668/Multi-OS+Support+AMP+Hypervisor.

[19] "Digilent zybo," Zephyr Project, a Linux Foundation Project, Tech. Rep., Sep. 2024. [Online]. Available: https://docs.zephyrproject.org/latest/boards/digilent/zybo/doc/index.html.

[20] "NVIDIA Jetson Orin NX series," NVIDIA Corporation, Datasheet DS-10712-001, v1.5, Dec. 2024. [Online]. Available: https://developer.nvidia.com/embedded/downloads#?search=Data%20Sheet.

[21] M. Georgiev, "The digital signal processing pipelines (DSPPL) suite," Electromagnetic Vision (EMVi) Research Laboratory, McMaster University, Hamilton, ON, Canada, Tech. Rep. EMVi-R-121, Sep. 2024.

[22] M. Cheraghinia, A. Shahid, S. Luchie, *et al.*, "A comprehensive overview on UWB radar: Applications, standards, signal processing techniques, datasets, radio chips, trends and future research directions," *IEEE Communications Surveys & Tutorials*, pp. 1–42, Oct. 2024, early access.

[23] Z. Fang, W. Wang, J. Wang, *et al.*, "Integrated wideband chip-scale RF transceivers for radar sensing and UWB communications: A survey," *IEEE Circuits Syst. Mag.*, vol. 22, no. 1, pp. 40–76, Feb. 2022.

[24] T. Pardhu, V. Kumar, P. Kumar, and N. Deevi, "Advancements in UWB based human motion detection through wall: A comprehensive analysis," *IEEE Access*, vol. 12, May 2024.

[25] J. J. McCombe, N. K. Nikolova, M. S. Georgiev, and T. Thayaparan, "Clutter removal in the automatic detection of concealed weapons with late time responses," in *2013 European Radar Conference (EuRAD)*, IEEE, Nuremberg, Germany, Oct. 2013, pp. 53–56.

[26] AKELA, "Final report - demonstration of a concealed weapons detection system using electromagnetic resonances," *US Department of Justice*, Jan. 2001.

[27] A. Agurto, Y. Li, G. Y. Tian, N. Bowring, and S. Lockwood, "A review of concealed weapon detection and research in perspective," in *2007 IEEE International Conference on Networking, Sensing and Control*, London, UK: IEEE, Apr. 2007, pp. 443–448.

[28] A. Vasalos, "Late time response analysis in UWB radar for concealed weapon detection: Feasibility study," Ph.D. dissertation, Dept. of Electronic, Electrical & Computer Engineering, Univ. of Birmingham, Birmingham, UK, Sep. 2010.

[29] S. W. Harmer, S. E. Cole, N. J. Bowring, N. D. Rezgui, and D. Andrews, "On body concealed weapon detection using a phased antenna array," *Progress In Electromagnetics Research*, vol. 124, pp. 187–210, Jan. 2012.

[30] N. K. Nikolova and T. Thayaparan, "Ultra-wideband (UWB) high-resolution noise radar for concealed weapon detection," Defence Research and Development Canada, Tech. Rep. TR 2013-160, Feb. 2014.

[31] N. K. Nikolova and J. J. McCombe, *On-body concealed weapon detection system*, U.S. Patent No. 10,229,328, Mar. 2019.

[32] A. D. Pitcher, M. S. Georgiev, J. Nguyen, and N. K. Nikolova, "Unobtrusive inspection for on-body threats concealed under clothing: Concealed weapons detection using polarization energy ratios," Electromagnetic Vision (EMVi) Research Laboratory, McMaster University, Hamilton, ON, Canada, Tech. Rep. EMVi-R-110, Sep. 2021.

APPENDIX A:

CORRECTING TIMEBASE ERRORS IN ULTRA-WIDEBAND EQUIVALENT-TIME SAMPLING RECEIVERS

Preface

This chapter is a reproduction of the following published conference manuscript:

A. D. Pitcher, M. Georgiev, and N. K. Nikolova, "Correcting timebase errors in ultra-wideband equivalent-time sampling receivers," in *2024 21st European Radar Conference (EuRAD)*, Paris, France: IEEE, Nov. 2024, pp. 47–50. DOI: 10.23919/EuRAD61604.2024.10734877.

The proposed equivalent-time sampling receiver (ETSR) was developed, designed, and validated under my leadership. I also established the experimental framework and measurement methodology, investigated and formally analyzed the results, created the visualizations, and wrote, edited, and presented the manuscript. Mihail Georgiev played a key role in developing the proposed calibration method and provided feedback

during the manuscript review. Natalia K. Nikolova supervised the project, guided the design reviews and testing process, and assisted with editing the manuscript.

A.1 Introduction

Emerging sensing and imaging systems are rapidly adopting ultra-wideband (UWB) technology. The main advantages of this technology are the use of non-ionizing harmless radiation, the low-power emissions spread over large bandwidths, and the good penetration capabilities, especially in the low-gigahertz spectrum. Applications operating in various frequency bands between 100 MHz to 10.6 GHz [1] include ground penetrating radar (GPR), non-destructive testing (NDT), and security [2]–[8].

Due to the large bandwidth, time-sampling receivers require sampling rates on the order of several tens of giga-samples per second (GSa/s). Analog-to-digital converters (ADCs) that sample at tens of GSa/s exist, but they cost thousands of dollars [9], [10]. Real-time (RT) sampling high-speed oscilloscopes capable of these rates also exist, but they are large, heavy, and very expensive [11], [12]. As a result, low-cost compact UWB systems have remained out of reach, impeding the growth of the emerging UWB applications. These applications require lightweight compact systems that can be mounted on mobile platforms, and provide accurate sampling with a stable timebase and high data throughput.

Recent advancements in high-frequency electronics have enabled custom low-cost receiver architectures employing equivalent-time (ET) sampling [2]–[5], [13]–[15]. At the core of an ET receiver are electronic circuits, which, under the control of a clocking network, delay the ADC sample point with respect to an initial sample point. Two common technologies are used: (i) a phase-locked loop (PLL) [2], [13], [14] and (ii) a programmable delay chip (PDC) [3], [4], [15]. A PLL synchronizes the phase of the

output signal with respect to the input one by using a reference clock. The drawback is the relatively long time required to phase-lock onto the signal and create the sampling delays, which is in the microseconds range [16], [17].

The alternative is to use a PDC, which delays the input clock signal by preset amounts. The PDC is a cascaded network of various delay paths (each enabled or disabled by a control 'tap'). Thus, the available delays belong to a discrete set of digitally controlled temporal steps. Compared to the PLL circuit, the PDC offers much quicker response time, since the control is a latch-enabled input and the cascading network delay stabilizes within picoseconds [18]. The disadvantage of the PDC is that the available delays of the chip constrain the step sizes, and these steps are not equispaced. Moreover, environmental factors such as temperature cause non-negligible deviations (in the range of several to tens of picoseconds) from the delays specified in the chip's datasheets. Previously reported systems do not address these problems, the likely reason being that such deviations are considered negligible. However, for a 20-GSa/s receiver, the delays must ensure an accurate 50-ps sampling step, and such deviations become unacceptable. This is why a calibration procedure is needed to extract the true nonuniform step sizes achieved with the PDC delays. Then, the data can be interpolated from the nonuniform to an equispaced 50-ps timebase.

Here, a calibration procedure is presented for estimating a PDC tap delays using a stable sine wave from a radio frequency (RF) generator. The equivalent-time sampling receiver (ETSR) presented in [4] is used for verification as it employs a PDC. The results show that the true tap settings can be estimated accurately. The method is employed to monitor the system tap delays over time and to analyze their stability.

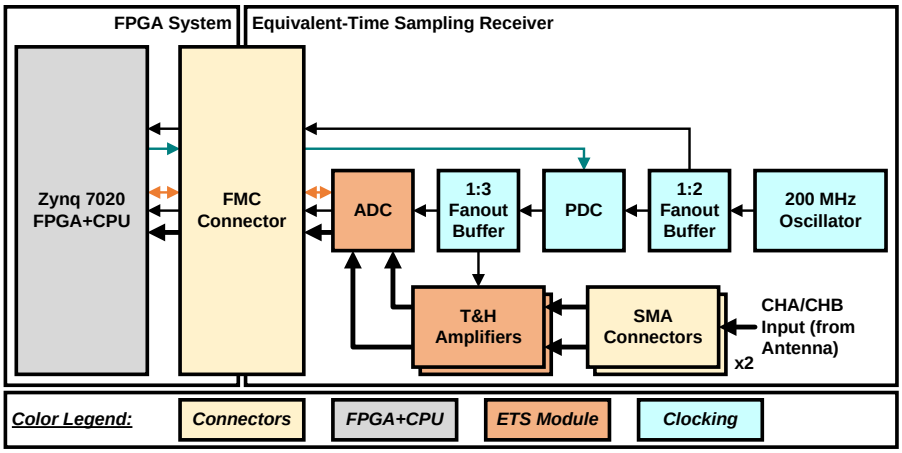


Figure A.1: High-level block diagram of UWB ETSR. The colour legend located on the bottom helps to identify the functionality of the ETSR.

A.2 Receiver Architecture

A high-level system block diagram for the ETSR is shown in Fig. A.1. The custom ETSR is integrated with a field-programmable gate array (FPGA) board [19] through an FPGA mezzanine card (FMC) (160-pin) connector. The FPGA board with its built-in dual-core ARM microcontrollers (MCUs) configures and controls the ETSR.

Each input of the dual-channel 16-bit ADC [20] is connected to a track and hold (T&H) amplifier [21] featuring an analog bandwidth of 5 GHz and a differential (balanced) signal input. Baluns [22] are employed to connect the two RF channels to the inputs of the T&H amplifiers. The ADC sampling rate is 200 mega-samples per second (MSa/s).

A 200-MHz ultra-low-jitter oscillator [23] drives the clocking network, and it features root-mean-square (RMS) jitter of a few femtoseconds. A 1:2 fan-out buffer [24] distributes the 200-MHz reference to the FPGA and the remaining clock network. The FPGA uses the reference for internal synchronization and to control the transmitter. The PDC [18] provides the delay control necessary to shift the ADC's sampling point.

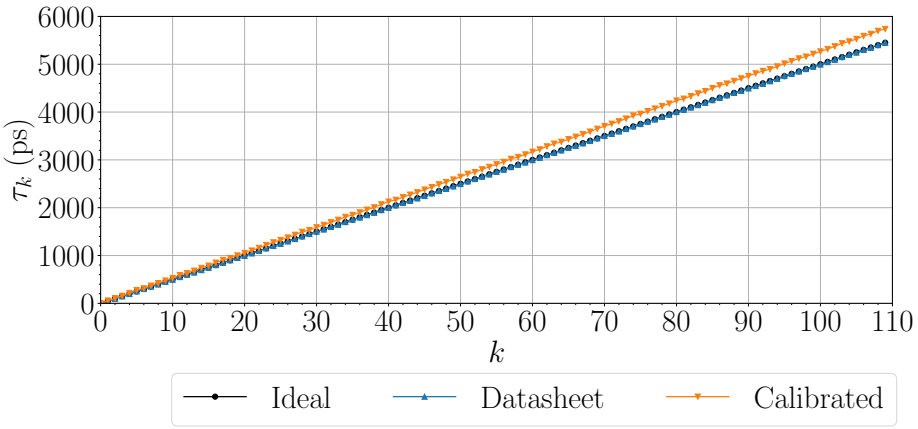
A 1:3 fan-out buffer [25] further distributes the clock signal to the two T&H amplifiers and the ADC. Additional fixed-delay lines from the last fan-out buffer to the T&H amplifiers and the ADC ensure that ADC sampling occurs only during the hold stage of the T&H amplifier [4].

The PDC is critically important for the accuracy and stability of the temporal sampling. Delay instabilities and deviations from the prescribed tap delays place the samples at inaccurate temporal positions. As discussed below, these errors increase with the delay's length. Here, we employ an industrial grade PDC chip [18], which guarantees the stability of ±10-ps per tap over an operating temperature range −40°C to 85°C. The FPGA controls the PDC through a 10-bit digital latch signal. Each enabled bit (the tap) adds a delay. The delays (in ps) are:

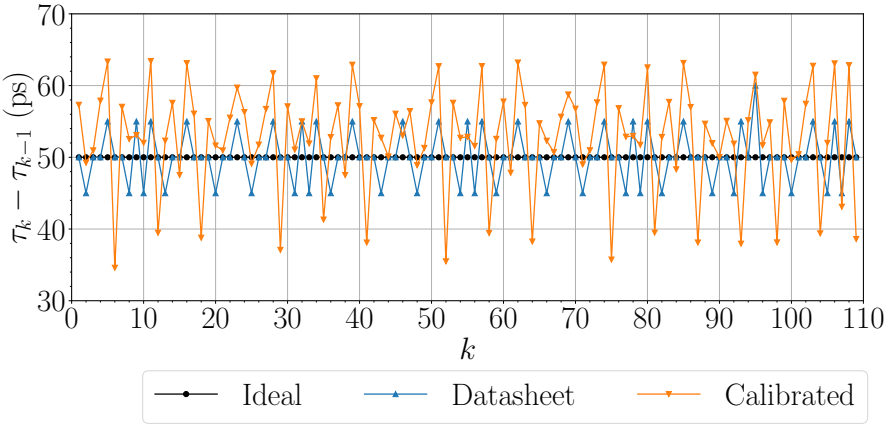
$$\text{taps} = [10, 15, 35, 70, 145, 290, 575, 1150, 2300, 4610]\,. \tag{A.1}$$

The current receiver realizes an equivalent time sampling step of $\Delta t = 50$ ps. The overall signal $x(t)$ of length 1 μs is reconstructed by interleaving K sequences ($K = 110$), $x_k[n] = x(\tau_k + nT)$, where τ_k ($k = 0, \ldots, K-1$) is the delay determining the start time of the k-th sequence, and $T = 5$ ns is the ADC sampling period. Each sequence has N samples ($N = 200$). Ideally, $\tau_k = k\Delta t$ and $T = 100\Delta t$, in which case exactly 100 sequences $x_k[n]$, $n = 0, \ldots, N-1$, would be needed to reconstruct $x(t)$. The PDC, however, cannot provide equispaced delays. For this reason, 110 sequences are used, which provide a temporal overlap between the samples in $\{x_{100}[n] \cdots x_{109}[n]\}$ and those in $\{x_0[n+1] \cdots x_9[n+1]\}$. The overlap allows for correct concatenation and aids in timebase correction. The timebase correction, along with interpolation, provides a smooth uniformly sampled overall signal.

Fig. A.2a shows the delay τ_k *versus* the index k for the $x_k[n]$ sequence. The "Ideal"



(a)



(b)

Figure A.2: Timebase error in terms of: (a) tap delays, (b) step sizes between consecutive tap delays. In (a), the "Ideal" slope is 50 ps per sample. The "Ideal" trace overlaps visually but not exactly the "Datasheet" trace. In (b), the chosen tap delays from the "Datasheet" are close but not always equal to the ET sampling period of 50 ps. Significant differences are observed between the so-chosen tap delays and their estimates from the calibration procedure.

trace depicts the desired uniform delay increment of 50 ps. The "Datasheet" trace shows the delays achieved by assigning a 10-bit latch signal for each k. Note that these delays are not spaced by exactly 50 ps from one sample to the next. The visual overlap of these two traces verifies the proper choice of tap delays. The difference between the actual "Datasheet" delay increment and the ideal delay increment of 50 ps is shown in Fig. A.2b. It is evident that, while the averaged delay increment is 50 ps, the deviation can be as large as 10 ps (at $k = 94$) and it is often close to ± 5 ps. Moreover, when estimated by the proposed calibration method, the actual delays ("Calibrated" trace) differ from those in the "Datasheet" trace. The plot of the "Calibrated" traces in Fig. A.2 is just one example of measurements with the chosen PDC. The actual delays may differ from one PDC chip to another. They also depend on the device temperature. It is evident that a calibration procedure is necessary to estimate the actual delays achieved by the PDC tap settings.

A.3 Calibration Procedure

The ET sampling $\check{x}(t)$ of the continuous signal $x(t)$ is represented by the interleaving of the sequences $\check{x}_k(t)$ which are sampled at $t = \tau_k + nT$, i.e.,

$$\check{x}(t) = \sum_{k=0}^{K-1} \check{x}_k(t),\ \check{x}_k(t) = \sum_{n=0}^{N-1} x(t)\delta\left(t - (\tau_k + nT)\right), \tag{A.2}$$

where τ_k is the k-th tap delay, n is the ADC sample index, T is the ADC sampling period, and $\delta(t)$ is the delta function. The goal of the timebase calibration is to accurately specify the sampling instants $(\tau_k + nT)$. Assuming the period T is known, this requires an estimation of the tap delays τ_k, acquired via the (discrete-time) Fourier

transform of $\check{x}_k(t)$, which is

$$\check{X}_k(f) = \int_{-\infty}^{\infty} \check{x}_k(t) e^{-j2\pi ft} \mathrm{d}t = \sum_{n=0}^{N-1} x_k[n] e^{-j2\pi f(\tau_k + nT)}, \tag{A.3}$$

where $x_k[n] = x(\tau_k + nT)$ are the samples. In practice, we approximate $\check{X}_k(f)$ with a discrete spectrum via the fast Fourier transform (FFT). For periodic signals below the Nyquist limit of $1/(2T)$, the spectra $\check{X}_k(f)$ differ only by a phase shift. Thus, using $\check{X}_0(f)$ as a reference, where the first tap delay is set to $\tau_0 \equiv 0$, we obtain the relationship

$$\check{X}_k(f) = e^{-j2\pi\tau_k f} \check{X}_0(f). \tag{A.4}$$

Thus, each tap delay can be estimated by

$$\tau_k = -\frac{1}{j2\pi f} \log\left(\frac{\check{X}_k(f)}{\check{X}_0(f)}\right) = -\frac{\log \check{X}_k(f) - \log \check{X}_0(f)}{j2\pi f}. \tag{A.5}$$

The choice of $x(t) = \cos(2\pi f_c t + \phi)$, where $f_c < 1/(2T)$, is particularly attractive as a reference signal since the spectra $\check{X}_k(f)$ are concentrated at $f = f_c$, where they all have the same magnitude and distinct (unwrapped) phases ϕ_k. Thus, (A.5) need only be evaluated at $f = f_c$, yielding

$$\tau_k = -\frac{\phi_k - \phi_0}{2\pi f_c}. \tag{A.6}$$

To account for noise and sampling jitter, (A.6) is evaluated for M signals $x_m(t) \approx \cos(2\pi f_{c,m} t + \phi_m)$ with samples $x_{k,m}[n]$, each yielding an estimate $\tau_{k,m}$ of the k-th tap delay. $f_{c,m}$ and ϕ_m need not be the same for all m. The delay estimates are then averaged as $\bar{\tau}_k = \frac{1}{M} \sum_{m=0}^{M-1} \tau_{k,m}$ (see Algorithm 2).

Algorithm 2 Algorithm for PDC tap delay estimation

Input: sampling period T, sinusoidal signal samples $x_{k,m}[n]$
Output: average tap delay estimates $\{\bar{\tau}_k\}$

for $k = 0$ to $K - 1$ **do**
  for $m = 0$ to $M - 1$ **do**
    approximate spectrum $\check{X}_{k,m}(f)$ as FFT of $x_{k,m}[n]$
    identify carrier frequency $f_{c,m} = \arg\max \left|\check{X}_k(f)\right|$
    identify phase $\phi_{k,m}$ of $\check{X}_{k,m}(f_{c,m})$
    if k = 0 **then**
      set $\tau_{0,m} = 0$ and store $\phi_{0,m}$
    else
      compute $\tau_{k,m} = -(\phi_{k,m} - \phi_{0,m})/(2\pi f_{c,m})$ per (A.6)
    end if
  end for
  compute $\bar{\tau}_k = \frac{1}{M}\sum_{m=0}^{M-1} \tau_{k,m}$
end for

A.4 Results

The ETSR port is connected to an RF generator [26]. The calibration procedure employs $M = 1024$ signals, where each signal is the result of a time-domain average of 256 "raw" signals. Thus, each tap-delay estimation is based on 262 144 individually sampled waveforms.

The "Calibrated" (orange) traces in Fig. A.2a and Fig. A.2b are the result of the calibration procedure and they indicate appreciable deviations from the tabulated "Datasheet" PDC values (in blue). The per-tap error is positively biased (see Fig. A.2b). Also, Fig. A.2b shows that the step sizes are not equispaced; therefore, an interpolation scheme must be employed to achieve an equispaced timebase.

To evaluate the stability of the actual tap delays, the automated calibration procedure is left to run every 5 minutes over the course of 5 consecutive days. Select probability distribution functions (PDFs) of the tap delays τ_1 and τ_{109} are shown in Fig. A.3. Fig. A.3a shows that the small delay setting is more stable than the large

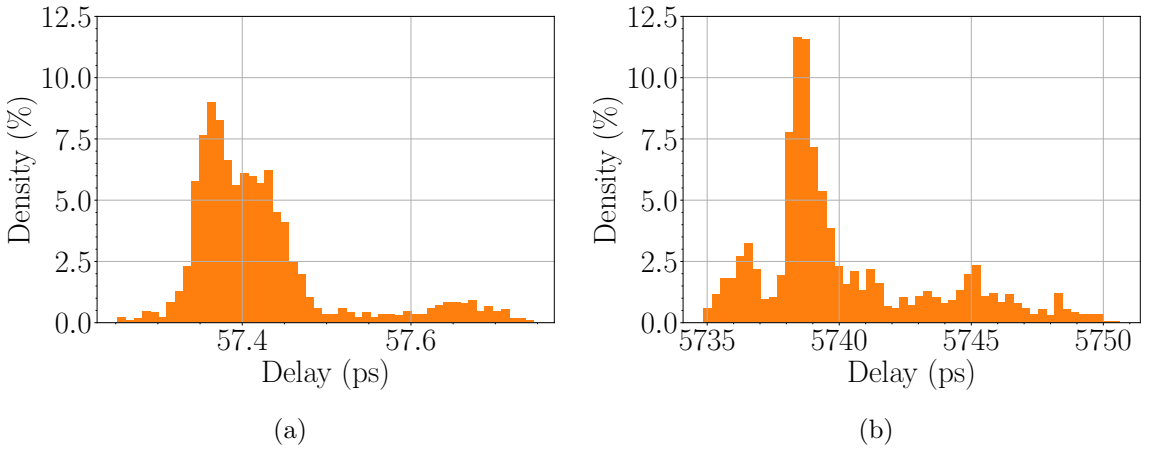
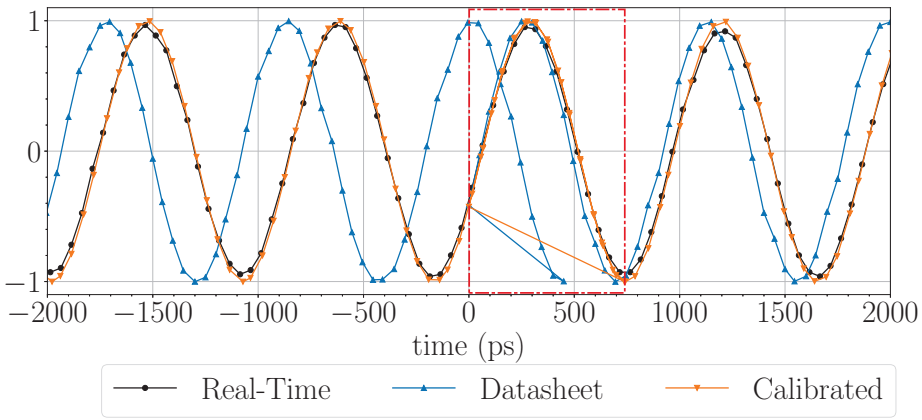


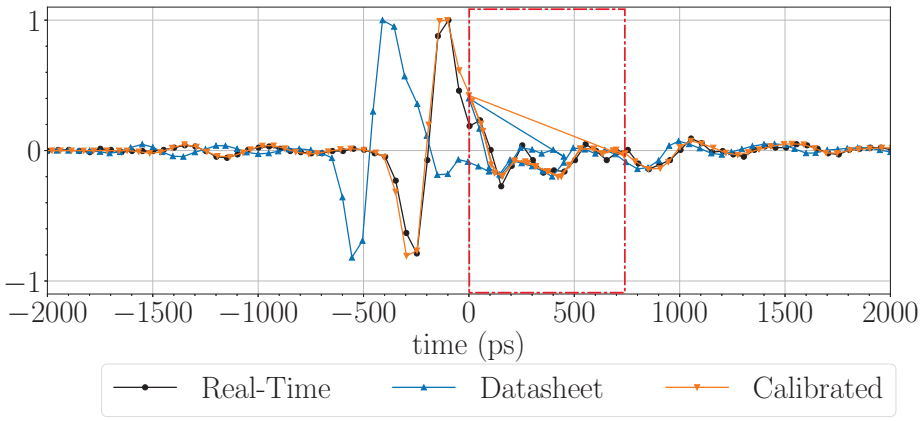
Figure A.3: PDC stability in terms of the probability density of the tap estimates over the course of 5 consecutive days with measurements taken every 5 minutes for: (a) first tap delay and (b) last tap delay. According to the device datasheet, the first tap delay is 50 ps and the last tap delay is 5450 ps.

one in Fig. A.3b. The former shows a drift confined within 0.6 ps, whereas the latter has a drift range of 15 ps but is mostly concentrated within the 3-ps range, which is small compared to the ET sampling period of 50 ps. Nonetheless, the delay drift is evident and likely caused by ambient temperature fluctuations as the system remained undisturbed during the 5 day test campaign. Thus, calibration is recommended immediately before measurements.

Finally, to demonstrate the importance of the proposed calibration procedure, two ET sampled signals are provided in Fig. A.4. Fig. A.4a shows a 1.1-GHz sinusoidal waveform measured with and without the calibrated tap delays. As a reference, the signal is also acquired with a RT oscilloscope [11] with a 20-GSa/s sampling rate (see "Real-Time" trace). It is evident that the reconstructed signal's timebase is inaccurate without calibration. On the other hand, the proposed calibration procedure provides a highly accurate signal, which matches the measurement well with the benchtop high-speed oscilloscope. Fig. A.4b shows the picosecond pulse from a UWB pulse generator



(a)



(b)

Figure A.4: Measured waveforms using: RT oscilloscope ("Real-Time" trace), ETSR with uncalibrated tap delays ("Datasheet" trace), and ETSR with calibrated tap delays ("Calibrated" trace). Example waveforms include: (a) 1.1-GHz sine wave, (b) UWB differentiated Gaussian pulse. The red rectangle indicates the overlapping of two sequences.

[27]. It is again observed that the calibrated timebase provides an accurate signal acquisition. The red rectangle indicates the overlapping of two sequences. While the uncalibrated signals ("Datasheet" trace) are discontinuous (the beginning and end overlapping sections are different), the beginning and end sections of the calibrated signals ("Calibrated" trace) are indistinguishable. Note that the line segments that differ from the waveform's shape are artifacts of drawing lines between the end and beginning of two sequences.

A.5 Conclusion

We have identified timebase distortion in PDC-based ETSRs and presented an effective method to calibrate for it. We have further shown that this distortion varies over time, suggesting that such systems need regular calibration prior to measurement collection. The realized UWB radar receiver offers a low-cost compact yet highly accurate ET sampling performance.

References

[1] "First report and order, revision of part 15 of commission's rule regarding UWB transmission system FCC 02-48," Federal Communications Commission (FCC), Washington, DC, USA, Tech. Rep. FCC 02-48, Apr. 2002.

[2] Y. Yang and A. Fathy, "Development and implementation of a real-time see-through-wall radar system based on FPGA," *IEEE Trans. Geosci. Remote Sens.*, vol. 47, no. 5, pp. 1270–1280, May 2009.

[3] Q. Liu, Y. Wang, and A. Fathy, "A compact integrated 100 GS/s sampling module for UWB see through wall radar with fast refresh rate for dynamic real time imaging," in *2012 IEEE Radio and Wireless Symposium*, Santa Clara, CA, USA: IEEE, Jan. 2012, pp. 59–62.

[4] A. D. Pitcher, "Compact low-cost ultra-wideband pulsed-radar system," M.A.Sc. thesis, Department of Electrical and Computer Engineering, McMaster University, Hamilton, ON, Canada, Aug. 2019.

[5] K. G. Kjelgård and T. S. Lande, "Evaluation of UWB radar module for snow water equivalent monitoring," in *2022 52nd European Microwave Conference (EuMC)*, Milan, Italy: IEEE, Sep. 2022, pp. 87–90.

[6] C. Noviello, G. Gennarelli, G. Esposito, *et al.*, "An overview on down-looking UAV-based GPR systems," *MDPI Remote Sensing*, vol. 14, no. 3245, pp. 1–28, Jul. 2022.

[7] Y. López, M. García-Fernández, G. Álvarez-Narciandi, and F. Las-Heras, "Unmanned aerial vehicle-based ground-penetrating radar systems: A review," *IEEE Geosci. Remote Sens. Mag.*, vol. 10, no. 2, pp. 66–86, Apr. 2022.

[8] M. García-Fernández, G. Álvarez-Narciandi, Y. López, and F. Las-Heras, "Array-based ground penetrating synthetic aperture radar on board an unmanned aerial vehicle for enhanced buried threats detection," *IEEE Trans. Geosci. Remote Sens.*, vol. 61, pp. 1–18, May 2023.

[9] "AD9213 12-bit, 6 GSPS/10.25 GSPS, JESD204B, RF analog-to-digital converter," Analog Devices, Inc., Datasheet AD9213 Rev. A, 2020.

[10] "ADC12DJ5200RF 10.4-GSPS single-channel or 5.2-GSPS dual-channel, 12-bit, RF-sampling analog-to-digital converter (ADC)," Texas Instruments, Inc., Datasheet SLVSEN9E, Rev. E, 2023.

[11] "Keysight technologies InfiniiVision 6000 X-series oscilloscope," Keysight Technologies, Inc., Datasheet 5991-4087EN, Dec. 2024.

[12] "6 series B MSO: Mixed signal oscilloscope," Tektronix, Inc., Datasheet 48W-61716-09, May 2023.

[13] Y. Masui, A. Toya, M. Sugawara, *et al.*, "Differential equivalent time sampling receiver for breast cancer detection," in *2017 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, Turin, Italy: IEEE, Oct. 2017, pp. 1–4.

[14] L. M. M. De Almeida, B. Sanches, and W. A. M. Van Noije, "High-speed sampler for UWB breast cancer detection system," in *2023 IEEE 14th Latin America Symposium on Circuits and Systems (LASCAS)*, Quito, Ecuador: IEEE, Feb. 2023, pp. 1–4.

[15] M. Saad, A. Maali, M. S. Azzaz, and M. Benssalah, "An efficient FPGA-based implementation of UWB radar system for through-wall imaging," *International Journal of Communication Systems*, e5510, May 2023.

[16] "AN1365: Si5361/62/63 lock time parameters," Skyworks Solutions, Inc., Application Note AN1365, Nov. 2022.

[17] I. Collins, "Phase alignment and control of the ADR4356/ADF5356 devices," Analog Devices, Inc., Technical Article, Aug. 2017.

[18] "SY89295U 2.5V/3.3V 1.5GHz precision LVPECL programmable delay," Micrel, Inc., Datasheet SY89295U, Mar. 2011.

[19] "Zedboard," Digilent, Inc., Hardware User's Guide, v1.1, Aug. 2012.

[20] "ADS42LBx9 14- and 16-bit, 250-MSPS, analog-to-digital converters," Texas Instruments, Inc., Datasheet SLAS904F, Rev. F, May 2016.

[21] "HMC760LC4B wideband 4 GS/s track-and-hold amplifier DC - 5 GHz," Analog Devices, Inc., Datasheet HMC760LC4B, v01.0514.

[22] "BAL-0026 broadband isolation balun (300 KHz to 26.5 GHz)," Marki Microwave, Inc., Datasheet BAL-0026, Rev. E, Oct. 2020.

[23] "Ultra series crystal oscillator Si545 data sheet," Skyworks Solutions, Inc., Datasheet Si545, Rev. 206613A, May 2023.

[24] "CDCLVP1102 two-LVPECL output, high-performance clock buffer," Texas Instruments, Inc., Datasheet SCAS884D, Rev. D, Dec. 2015.

[25] "CDCLVP1204 four LVPECL output, high-performance clock buffer," Texas Instruments, Inc., Datasheet SCAS880F, Rev. F, Sep. 2015.

[26] "EXG X-series signal generator N5173B microwave analog 9 KHz to 13, 20, 31.8, or 40 GHz," Keysight Technologies, Inc, Datasheet 5991-3132EN, Feb. 2023.

[27] A. D. Pitcher, C. W. Baard, and N. K. Nikolova, "Design and performance analysis of a picosecond pulse generator," *IEEE Trans. Instrum. Meas.*, vol. 71, pp. 1–14, Aug. 2022.