CAD Review: the 7GHz doubler circuit

For our latest CAD benchmark, a doubler circuit was supplied to commercial vendors of non-linear microwave CAD. The results are presented here for simulators from Compact Software, Hewlett Packard and Optimization Systems Associates.

The CAD reviews in Microwave Engineering Europe, run every May and November, have proved to be very popular. In this exercise, the CAD vendors were supplied with circuit details for a class B frequency doubler built on Duroid. Compact Software and Optimization Systems Associates rapidly agreed to take part and had encouraged us to publish additional benchmarks.

Hewlett Packard declined to formally take part, citing the pressure of work after last year's acquisition of Eesof as the principal reason. However, with HP, including Eesof, now representing the largest single vendor of microwave CAD it was thought inappropriate to leave the company out. Hence the circuit designers in Belfast undertook the HP Microwave Design System (MDS) simulation while OSA and Compact devoted their own engineering resources to the problem.

Sonnet Software submitted results for the electromagnetic aspects of the simulation, and Sonnet's "em" planar simulator was also used by OSA.

Engineering resources are valuable and we would like to thank all the companies that gave so freely of their time for taking part. The results have again proved to be interesting.

Doubler circuit

The circuit outline, which was supplied to the vendors with dimensions, is shown in figure 1. Designed by Dr Aaron Tang at Queen's University, Belfast, it uses RT Duroid with a nominal dielectric constant of 2.2 and a height of 0.254mm. The active device is a NEC 7100 FET in die form and the two capacitors are AVX Accuwave 8.2pF.

In common with last November's review, the circuit was intended to be a practical one, using a commercial substrate and active device, but the FET was not packaged on this occasion. Measurements were taken using a Wiltron launcher and a University harmonic balance simulator was also used to provide an alternative set of simulated results.

Models

It will be clear to all users of microwave CAD that the accuracy of the models used for both active and passive devices is the key to good simulation. Both OSA and Compact initially used their own library models for the microstrip elements in the circuit, but their approaches to the active device were different.

Compact's team observed that the NEC FET was well suited to the application but added that modelling the device for harmonic balance simulation is not straightforward. They actually produced two models. NEC's European sales office supplied one, based on a Curtice cubic model (NEC model) while Compact undertook dc IV and bias dependent S-parameter measurements to produce a Materka-

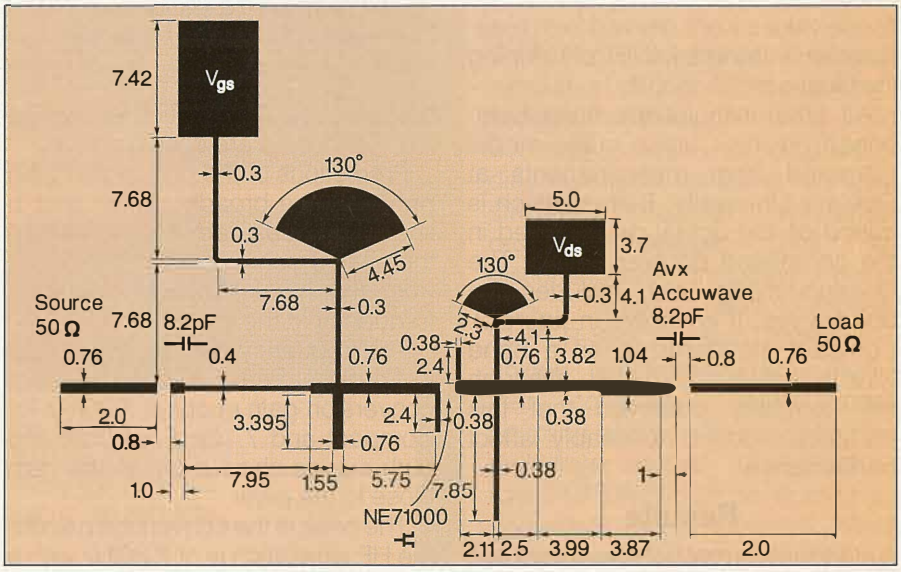


Figure 1: Circuit layout for the 7GHz doubler.

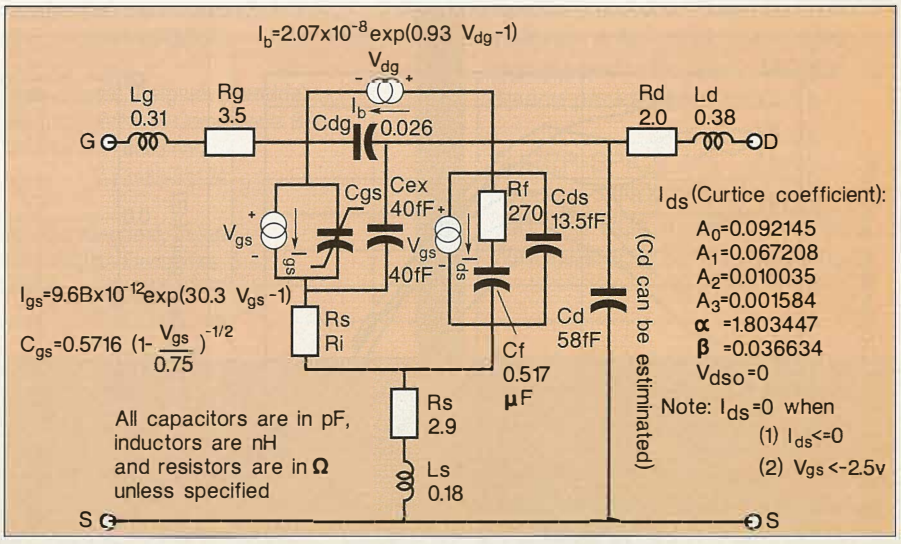


Figure 2: The Queen's model for the NEC 71000 FET.

Kacprzak model, which we will call the CS model. OSA used published data for the device at two bias points and for frequency points at 1GHz increments from 2-26GHz. The company's Harpe parameter extractor derived a Curtice and Ettenberg model from the data.

Hewlett Packard includes a model for the 71000 FET in the MDS "Fetlib" library, so this was used by the team at Queen's in all MDS simulations, with passive elements also drawn from the MDS libraries. Bond wire inductances of 0.3nH were added for the gate and drain, which use two 0.0254mm bond wires in the actual circuit, while the 3 source bond wires were represented by 0.18nH. These values were derived from measurements undertaken in developing the Queen's FET model.

All other simulations have been based on the Curtice cubic model extracted from measurements at Queen's University, Belfast which is based on the actual device used in the completed doubler circuit. The Queen's model also includes the bond wires. It is shown in figure 2. Compact standardized on a bond wire inductance of 0.3nH, although the company observed that this parameter could noticeably affect performance.

Results

A standard format has been adopted to allow easy comparison of the simulations and the measured data. The colours used and notation for the first four harmonics are shown above.

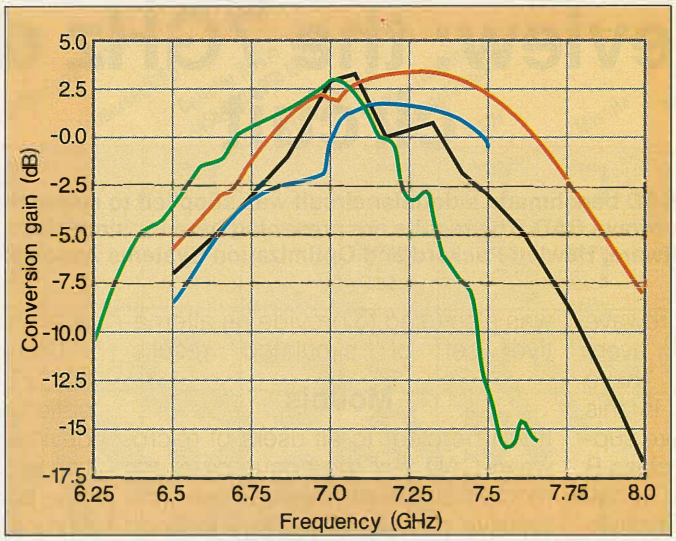


Figure 3: Conversion gain results plotted against frequency.

Key:
Compact
OSA
Measured
HP MDS
+ Fundamental (7GHz)
× 2nd harmonic
○ 3rd harmonic
● 4th harmonic

Predictions of the conversion gain proved to be broadly similar and in line with measurements. However, there were some shifts in frequency from the nominal 7GHz operating frequency at the input.

The frequency sweeps are plotted in figure 3. Peaks in the values of conversion gain occur at 7.3GHz for Compact and 7.1GHz for OSA and both curves show a dip in the gain close to the peak.

The peak in the conversion gain for the HP simulation is at 7.2GHz with a value of 1.4dB at an input power of 9.0dBm. At this frequency, the simulation shows 21dB suppression of the fundamental at the output. The third and fourth harmonics are at -27dBm and -30dBm respectively.

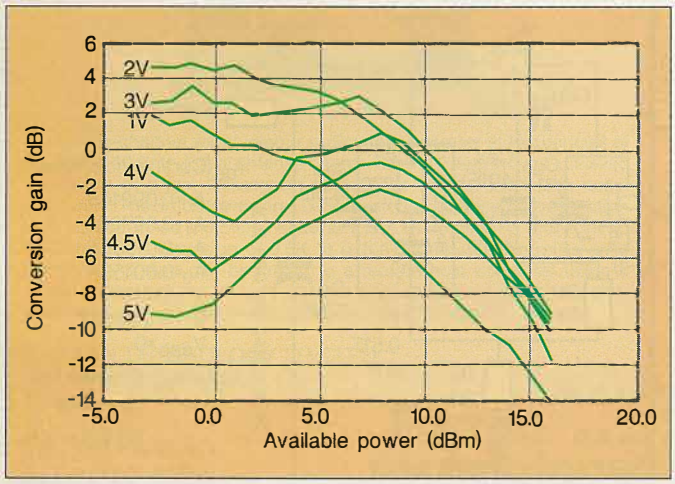
Power sweeps were requested at a nominal 7GHz, so these relatively small frequency shifts should be considered when we compare the power sweeps. One non-constant factor is the drive level applied. OSA used 9dBm as the peak of the conversion gain while Compact used 5dBm. Reference to the power sweeps below will show that this could influence the results but is unlikely to be a dominant factor.

For the HP simulations, a drive level in excess of 9dBm was needed to achieve conversion gain, rather than loss at 7.0GHz.

Measured results for the actual circuit show a conversion gain in excess of 2dB at 7.0GHz for drive levels between -2 and +8dBm, with a 3V Vds, but an increased Vds causes the conversion gain to drop rapidly at the lower drive levels - see figure 4. While Vds determines the different curves in the figure, variations between the active device models might be expected to similarly influence the results.

Conversion gain peaks occur with a +7dBm input or -1dBm input at 2.8dB and 3.8dB respectively.

Compact's second simulation with the 0.6nH bond wires may give us a further explanation. The company



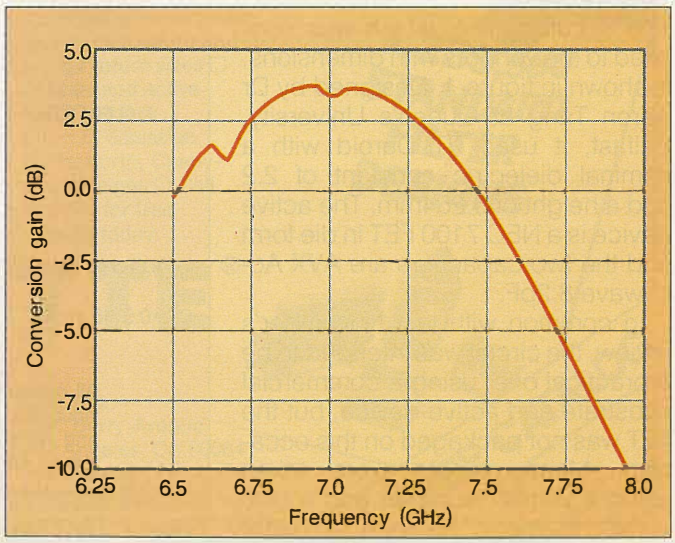


Figure 4: Conversion gain measurements for different Vds. Figure 5 (right): Compact's simulation with 0.6nH bond wires to the chip.

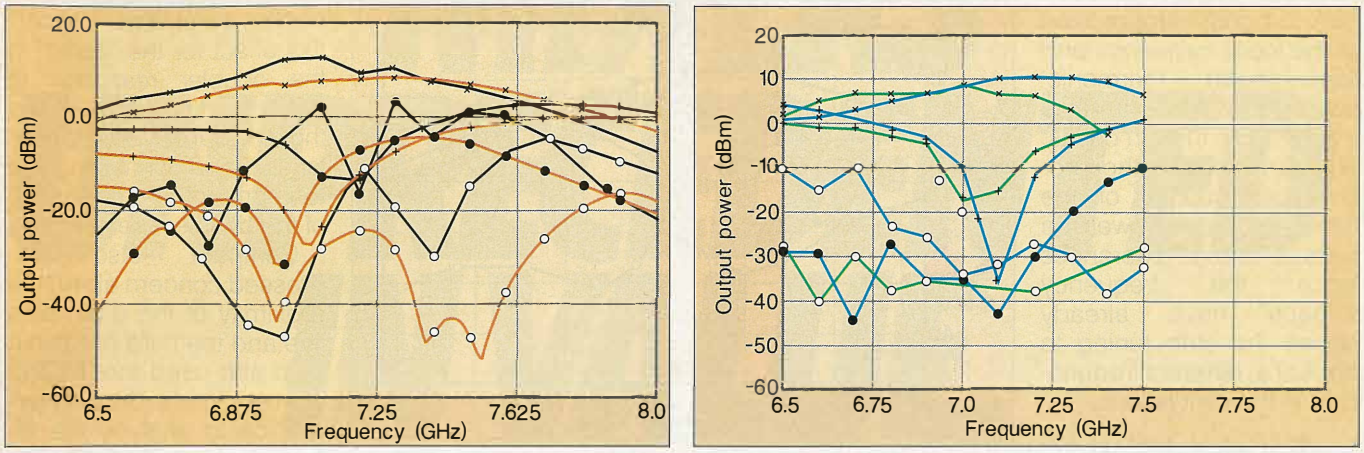


Figure 6 (a) and (b): Swept frequency results for the first four harmonics. Note that drive levels are not constant.

found that the increased inductance caused the centre of the response to be shifted down to 7.0GHz and the conversion gain to slightly increase, to 4.0dB as shown in figure 5. Compact identified the bias decoupling circuit as the cause of the dip at 7.0GHz and an equivalent spike in the predicted return loss.

The results from the frequency sweep for the first four harmonics also prove to be interesting in figure 6. Here the results diverge further than the simple conversion gain plots and the suppression of the input frequency at the output is significantly lower for OSA, at 24dB, than for the Compact simulation, at 36dB or HP at 45dB. The maximum value occurs at 7.1GHz and the 7.85mm drain stub was identified as the reason for this. The 2.4mm third harmonic stubs at the gate and drain are also clearly evident on Compact's and HP's results.

Although the plots show the output power for each simulation to allow a comparison, it should be remembered that the drive levels are not constant. To achieve satisfactory conversion gain levels, HP and OSA used a 9dBm input power, and the respective power sweeps show hor the conversion gain dropped below these input levels. The Compact results are with a 5dBm input, which is closer to the 6dBm value used for the measurements. In practice, conversion gain for the actual circuit was far less sensitive to the input level than the simulations.

In OSA's simulation, the third harmonic stubs have have an almost identical effect at 7.0GHz but the fourth harmonic, is at 7.2GHz compared to Compact's 7.0GHz.

The simulations with HP's MDS are broadly in line with Compact's when the frequency characteristics are considered although the drive levels used to achieve conversion gain is 4dB higher.

The best suppression of the fundamental and the fourth harmonic are at 7.1GHz but the third harmonic stub appears to be most effective at 7.0GHz. Suppression of the fundamental is the highest of all the simulations at 46dB, and well above the best measured result of 26dB, which occurred at 7.0GHz.

These results, so influenced by the modelling of the passive elements, suggest that there is some considerable variation in the passive library elements included with the simulators.

For the only two external passive elements, the AVX Accuwave 8.2pF capacitors, Compact also considered how critical the modelling of these elements would be in the overall simulation. It was concluded that for values above 3pF, the simulation is quite insensitive to the parameters of these devices.

Power sweep

The power sweep simulations again show some significant differences, all using 7GHz as the input frequency. At 5dBm input, the OSA simulation predicts a conversion loss of almost 5dB, while the Compact simulation is predicting a conversion gain in excess of 3dB - see figure 7. Compact's simulation is certainly predicting a rather better doubler,

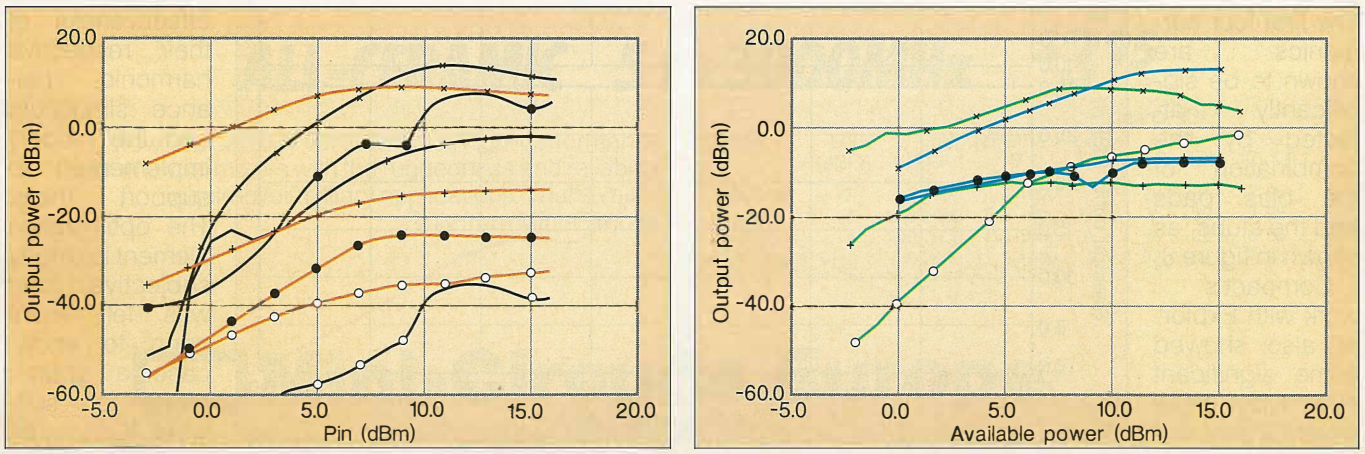


Figure 7 (a) and (b): Swept power simulations and measurements.

with superior suppression of the input frequency and the fourth harmonic' although the third harmonic is well down in both cases. The sensitivity to the precise performance of the tuning stubs may well be behind these differences since the frequency sweeps have already shown the stub tuning to appear at different frequencies in the simulations.

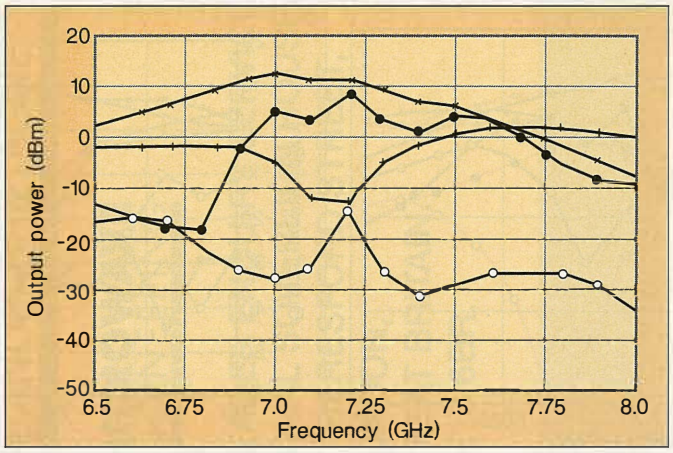


Figure 7: OSA's results with full "em" simulation of the bias pads and third harmonic stubs.

Em simulation

Both Compact and OSA opted to look further into the coupling of the stubs. OSA has links from the OSA90/Hope software into Sonnet's EM planar electromagnetic simulator and used this program, while Compact used its Explorer software. With the third harmonic stub coupling simulated by EM as a four port, OSA's results showed a smoother response for conversion gain against frequency, with 3.5dB gain from 7 to 7.1GHz, again using the 9dBm drive level.

The third harmonic suppression proved not to be as great but the stub resonances were still at 7GHz and 7.4GHz. The predicted increase in the third and fourth harmonic levels produced a more distorted waveform when OSA plotted the input and output voltage waveforms.

OSA went on to consider the effects of the bias pads and the radial stubs adjacent to them, simulating them as a two port in EM. The first four harmonics are shown to be significantly affected by the combination of the bias pads and the stubs, as shown in figure 8.

Compact's work with Explorer also showed some significant effects but these were largely out of band and affected the doubler simulation relatively little.

For the large bias pads, the company found resonances at 19.5GHz and 24.0GHz which were "due to a transverse mode and a patch antenna mode". However, it was observed from a plot of the phase component of S11 that the gate bias stub was operating as a quarter wavelength at 5.0GHz rather than the intended 7.0GHz, due to "the large width of the transmission line and the large impedance step discontinuity from the connecting line". The effect on the circuit is small as the radial stub is "providing a wideband short circuit near 7.0GHz" and this impedance is transformed through the half wavelength connecting line. Compact's engineers blamed this effect for the "bump" in the doubler response at 7.0GHz and recommended the removal of the rectangular stub and connecting line to improve the smoothness of the doubler's response.

Compact also expressed concern about the proximity of the drain bias line and the third harmonic stub and used the "MCPL" element in Microwave Harmonica to analyse the effect. Any resulting change to the conversion gain was found to be very small, varying by less than 0.1dB.

Sonnet's electromagnetic analysis encompassed the second fan stub and the Vds pad. It shows the pad radiating at frequencies between 20 and 25GHz, including the third harmonic, and a magnitude of 0.9 for S_{11} at these frequencies was predicted.

Plots of the current density across the pad show a broadly similar distribution to a patch antenna.

With the Vds probe in the centre of the pad, the distribution is much the same, but short circuiting the end of the pad changes the situation significantly. Hence, the company warns against placing the bias probe in the centre of the pad. Otherwise the current density was insensitive to the impedance of the supply.

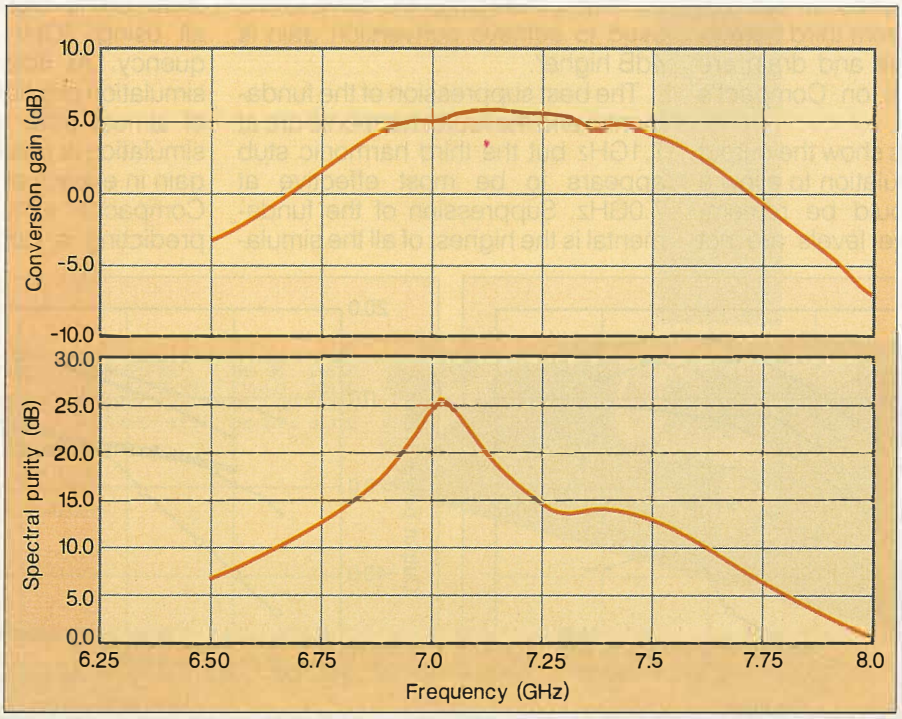


Figure 8: Spectral purity and conversion gain for Compact's optimized circuit.

Optimization

The objective part of the benchmark gave an opportunity for the companies to show the effectiveness of their respective harmonic balance simulators and the models implemented to support them. The optimization element is clearly subjective and was left more open to showcase a greater range of software. It draws on the skill of the

companies' support engineers as well as the scope of the CAD tools.

Compact stayed within the circuit topology given, varying only the lengths and widths of the transmission lines. They aimed to improve the conversion gain to 6dB and the spectral purity of the 2nd harmonic to better than 15dB. They defined a band of interest as 6.8 to 7.6GHz.

The spectral purity is defined by the ratio of the power at the second harmonic divided by the sum of the power in all other harmonics. The results are shown in figure 9.

OSA set the more conservative figure of 3dB conversion gain as a target but aimed for a higher spectral purity of 20dB. Data was based on simulations of the circuit with the EM analysis included for the bias pads and stubs. The fifteen variables picked for the optimization defined lengths of the transmission lines. The conversion gain is shown for the optimized circuit in figure 10.

In the two companies' optimizations, the changes in the lengths are quite different for each. In a majority of cases, one company's increase, corresponds to the other's decrease, as shown in table 2.

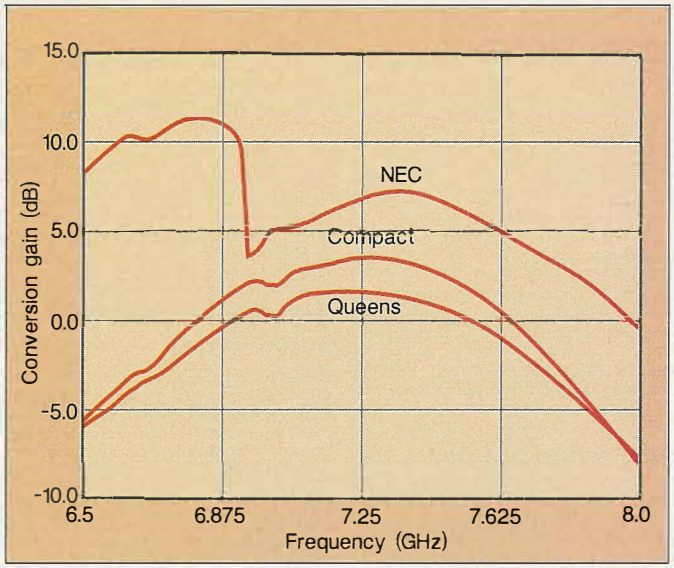


Figure 10: A comparison of results with the three models for the NEC 71000 FET. Shown are the Queen's University model, Compact's model and NEC's model.

Device models

The choice of the correct device model to use when there is not an obvious one in the FET manufacturers data book is clearly critical to a good simulation. OSA and Compact both looked at this problem.

OSA ran a Monte Carlo simulation to assess the effect of model uncertainty on simulation result and assigned a 20% tolerance to all model parameters to do this. The conclusion was that the frequency doubling would not be very sensitive but the spectral purity would be. The conversion gain spread in 50 outcomes was between -2.4dB and 4.7dB.

Compact compared three transistor models. They found that the NEC-Europe-supplied FET model did not exhibit pinch-off and although a hard pinch-off could be forced, this would be at the expense of a discontinuous model with accompanying convergence problems in the simulation. The CS model and the Queen's model were broadly similar except for the variation in Idss and Vpo. Conversion gain results for all three models are compared in figure 10.

Compact also ran multiple conversion gain analyses for the circuit based on different Idss and Vpo values, since the device data sheet predicts that these parameters can vary from 20 to 120mA and from -0.5 to -3.5V respectively. A 20dB range of conversion gain values was actually predicted, suggesting large error bars could be placed on the simulations. Nevertheless, the results had consistently been much closer to measurements for the particular device used at Queen's in the circuit.

HP was the only company with a model for the FET already in the MDS library and, with shared library resources, this should also be available to Libra users. The design team at Queen's were not as confident about the HP model as their won and with HP choosing not to take part in the benchmark, the details were not available as tot he origin of the model. Nevertheless, the ground-rules for the benchmarks were based on each software vendor using their own model.

Table 2

Original (mm)	Optimized Compact (mm)	Optimized OSA (mm)
5.7	5.73	5.182
3.395	3.93	4.5
2.11	2.44	1.601
7.85	7.79	7.903
7.68	7.86	7.51
3.82	3.82	3.804
1.55	1.58	1.759
7.95	8.36	6.792
2.5	2.57	2.842
3.99	4.35	3.903
3.87	4.10	3.698

Conclusions

All three simulators used in the benchmark showed a doubler operating around 7.0GHz. The differences came from the models of both the active device and the passive elements. Subjectively, the HP and Compact simulations are most similar in the prediction of the passive tuning of the circuit, although their simulations diverge in the parameters related to the active device.

The Compact and Queen's models for the FET appear to produce the best results, and both have been extracted from measurements of an actual NE71000 device. Despite the broad specification range on the NEC data sheet, the different transistors measured have produced similar results. Good simulations need good models.

Simulation times were not conclusive. OSA claimed a slightly shorter CPU time of 0.3s per point with a Sun Sparc station 10 workstation. Compact quoted 1.6s and 0.7s/point for frequency and power sweeps respectively.

Acknowledgements

Significant time and resources have gone into the benchmark. We would like to thank Aaron Tang and David Linton at Queen's University, Belfast. Bill McGinn in the USA and Hendrik Nagel at Technical Software Services in Germany undertook the Compact simulations while Radek Biernacki supplied the OSA results. Thanks also to Jim Merrill and Jim Rautio at Sonnet.