Non-linear CAD benchmark

For the latest in our series of CAD reviews, a challenging bipolar amplifier circuit was supplied to the major rf CAD vendors. An original concern that the results might all prove to be identical proved far from reality. OSA, Hewlett Packard, Eesof and Compact Software took up the challenge and supplied the simulation results here.

The principal aim of this year's CAD review was to challenge companies with simulation products significantly beyond the entry level products featured in the same issue of *Microwave Engineering Europe* last year. The circuit is certainly practical: it is a power amplifier with less than 1W output at 2GHz and is clearly aimed at commercial applications with a standard silicon bipolar transistor and inexpensive FR4 substrate. With a significant body of work aimed at communications applications around 2GHz at present, the circuit outlined is quite a realistic test of a simulation capability.

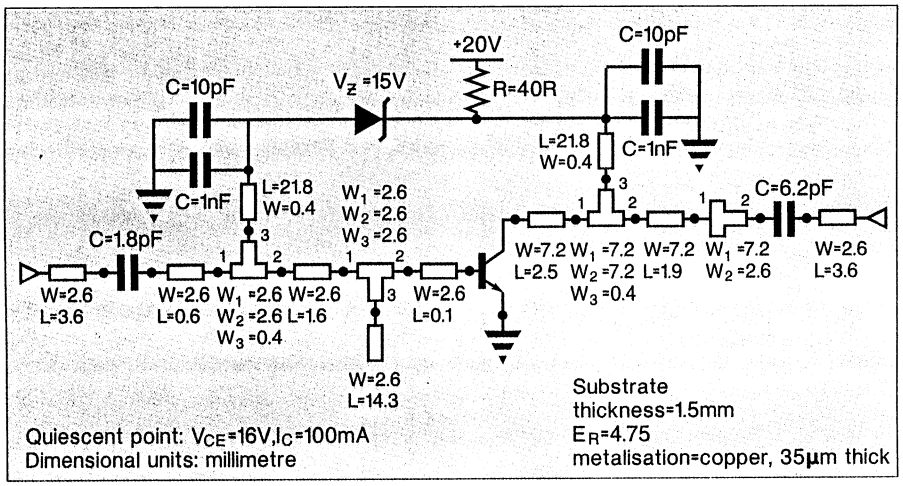

Figure 1: The power amplifier circuit, as supplied to the CAD vendors.

The supply of a circuit example to the software vendors, and the use of their own applications staff to programme the example, answered a criticism levelled at last year's exercise; that an independent review team would not necessarily have all the training needed to get the best out of a particular simulator. Nevertheless, the companies that protested about the training-level of any independent review team also proved the most reluctant to undertake this year's review! We are certainly grateful for the efforts of the four companies reported here, who clearly had the confidence to join this very public debate. You now have an opportunity to form a judgement on whether that confidence has been fully vindicated or shown to be misplaced.

Review process

The circuit details were despatched on the 13th of September to a comprehensive list of rf and microwave CAD vendors and both linear and power sweep results were requested. All companies had prior warning that this and two other circuits would be provided, but with the results from the first circuit not arriving until shortly before going to press, it was concluded that the further two examples should be sent after completion of the first circuit and the results featured in a future issue.

Each company was supplied with the circuit diagram, including physical dimensions of the components, and the part number of the Avantek device, AT 64023. Avantek is now part of Hewlett Packard (HP) but this was not considered to give an unfair advantage to that company since the Spice model from the data book or any vendor's library could be used. To avoid confusion with HP as a software vendor, the Avantek name is used throughout. Similarly, we refer to "Eesof" which is now also owned by HP.

The four companies that followed through the simulation challenge were, in order of response with results: Optimization System Associates, Hewlett Packard, Eesof and Compact Software. Each encountered some problems and stated some limitations on the basis of the circuit information made available to them and these are reported.

Both Jansen Microwave and Ingsoft also proposed to contribute, but Jansen was not prepared to undertake the simulation without a full characterisation of the substrate and measured data for the transistor to derive an alternative model to the manufacturer's and Ingsoft had insufficient resources available to undertake the task in the time allowed, partly due to the imminent release of an enhanced version of the company's RF Designer program.

One further problem could have arisen from the purchase of Eesof by Hewlett Packard after the benchmark process had commenced, but both companies agreed to take part, to some extent driven by the enthusiasm of the Eesof staff in Europe. Eesof was, at least to our knowledge, the only company to undertake the benchmarking with European-based applications staff. HP and OSA used staff at their respective home bases in Santa Rosa, California and Dundas, Ontario while Compact used a specialist in a field office in Dallas, Texas.

The circuit

The amplifier shown in figure 1 was designed at University College Dublin, Ireland by Ruairi Jennings and Philip Perry.

It is used to provide a high power driver to saturate other high power devices which are being tested under non-linear operation.

The design uses mainly distributed elements realised in microstrip on standard 1.5mm thick FR4 board. It consists of a single stub input equaliser, and a quarter wave transformer on the output. The input and output blocking capacitors provide a further degree of freedom in the design of

the matching networks.

This configuration results in a very narrow band response centred on 2GHz, with the power characteristics having been somewhat sacrificed in favour of good impedance and gain characteristics.

The transistor used is the Avantek AT64023, biased for a constant collector current of 100mA and a constant collector emitter voltage of 16V. It is capable of providing +23dBm at 1dB gain compression under these bias conditions. It is a classic power BJT, with a poor S12 (ie the device must be regarded as bilateral), an electrically large package, and an emitter ballast resistor.

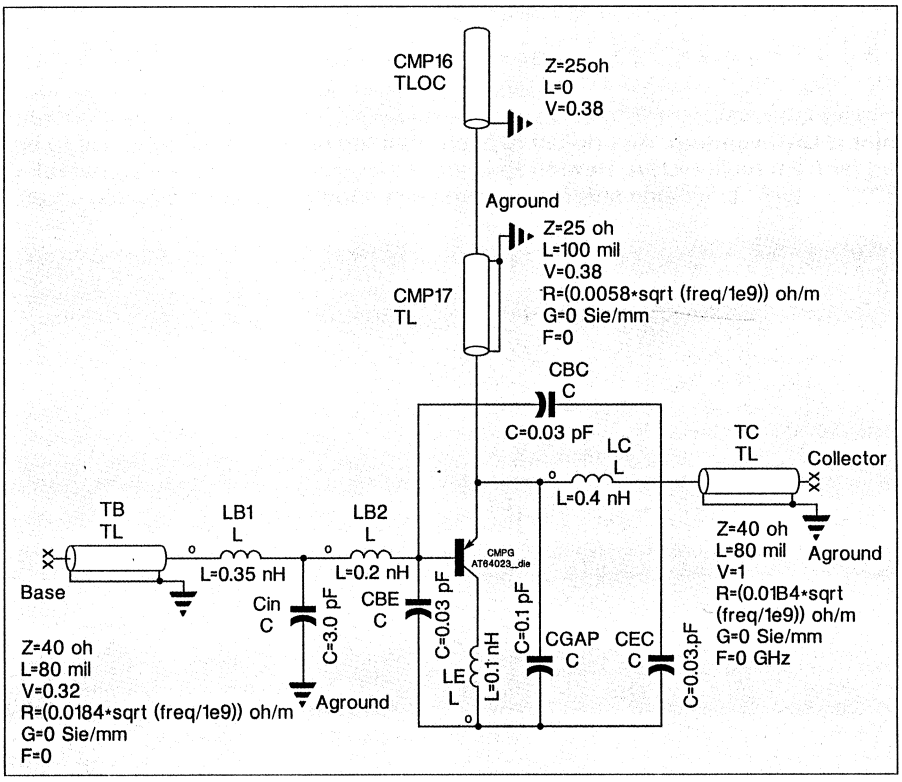

Figure 2: The equivalent circuit model for the transistor, with the package shown too. This format is from Hewlett Packard.

The non-linear model being used in this example is the model provided by Avantek. It consists of a standard SPICE type model, with a distributed RC base, where the capacitances are simulated by nonlinear diodes. The extra elements around the basic device model represent the device package. The entire device model is shown in figure 2.

The amplifier circuit was not chosen for complexity since it is appreciated that application resources are expensive. However, despite the circuit working well in practice it had proved very difficult to simulate using non-linear harmonic-balance simulators and was therefore considered to be an appropriate challenge.

Success and failure

The two most feared scenarios in waiting for the simulation results to be returned were either a complete success where four identical S21 plots proved nothing or a total failure with no convergence. Neither turned out to be the case but at one stage the failure of three simulators to handle the circuit looked likely.

The first company to return results was OSA, but by mid October we had still not received any further simulations and more questions about the circuit were being sent to the journal and to the circuit's designers in Dublin.

There was a common thread in that the linear simulations based on S-parameters in the Avantek data book had been successful but the harmonic balance simulations had failed to produce an amplifier. Hewlett Packard's simulation was an oscillator while both Eesof and Compact were achieving about 40dB of attenuation at 2GHz. Some of the explanations were simple. HP's application engineer had neglected to include the device package in the non-linear simulation. The S-parameters given by Avantek include the package while the Spice parameters do not. This simple oversight was rapidly corrected.

Eesof's "attenuator" was also cured by checking the input parameters and a more realistic simulation produced.

Compact's simulation took significantly longer to return and again the non-linear Microwave Harmonica program initially showed a significant level of insertion loss. This raised the question of the appropriate value to use for a parameter known as the Kirk current or IK. It describes the corner point in the plot of log(Ic) versus Vbe.

The value in the data sheet is quoted for a "unit" transistor and a scaling factor must be applied for a particular transistor. For the device used here, the value of $10^{-4}Am^{-2}$ needs to be scaled by a factor of 1560, yielding a value of 156mA which is compatible with a bias current of 100mA for the circuit. Thus these "process" description parameters can be used for a much wider range of devices. Definition of the Spice model in this way is stated in the data sheets from the transistor manufacturer.

Forward gain

Results for the gain of the amplifier, derived from a linear simulation using S-parameters in the Avantek data book, are broadly similar. They are shown in figure 3.

The frequency range shown is chosen to match the measured data available for the amplifier fabricated at UCD, although this does go beyond the useful operating range of the unit. A good agreement between the different simulators would be expected in this context, although differences in the way that the passive elements in the circuit are modelled in the different simulators will clearly impact the results.

OSA did not supply results above 2.5GHz, and indeed were not asked to, but from the other three simulators a resonance at 2.75GHz is clearly visible. This resonance is notable both as a common feature in the simulations and for its complete absence from the measurements of the actual circuit! Eesof elected to sup-

ply two sets of results, making use of different Tee models. The plots shown here define the Tees in the same way as HP, which was considered to be closer to the reality of the fabricated amplifier. In practice the difference in small signal gain is less than 1dB.

In summary, the small signal gains at 2GHz were 16.35dB (OSA), 11dB (HP), 11.4dB (Eesof) and 11.8dB for (Compact's modified circuit) compared with the measured value of 12.2dB.

Non-linear analysis

It is in the area of non-linear simulation that some of the most interesting features of the simulations have been found. The results are plotted for a 2GHz tone, in figure 4.

The problems with getting to this stage have already been described, although the data made available to each of the companies precisely matched that available to an engineer designing a circuit in the laboratory.

OSA, Eesof and HP simulated the circuit as supplied, although OSA alleged that the measured S-parameters supplied in the databook were not wholly in agreement with the Spice model, and produced an "optimised" model by extraction from the S-parameters. Compact Software predicted the circuit supplied to have an output at the 1dB compression point of only +17dBm, with a linear gain of 7.4dB. The values are significantly below expectations, and the company suggests that this is due to "an improperly matched device". A phase-plane analysis feature in the software was applied to examine the ac load line of the transistor which showed it to have a full range of current swing but a very poor voltage swing of less than ±3.5V. Compact's results are therefore from the simulation of a circuit with a different output match. Subsequent examination of the circuit schematic used by Compact for the simulation led the circuit's designers at UCD to conclude that the company had not included the transistor package with the non-linear simulation, hence causing a mismatch in much the same way experienced by HP.

OSA's reaction to concerns about discrepancies between the S-parameter-derived and Spice models led it to undertake a Monte Carlo sweep of output power versus input power for 100 outcomes. It showed a spread in 1dB compression values between 23.2dBm and 27.2dBm. The former value is actually closer to the measurements at UCD.

A further sensitivity analysis was also carried out which led OSA to suggest that the output power at 1dB gain compression was more sensitive to the length of the open stub in the input matching circuits and the lengths of the microstrip lines in the output matching circuits than to any other parameters in the circuits.

Despite the additional work undertaken by the company, OSA was by far the quickest company to return results. In this context, it is certainly surprising that the total terminal time quoted for the simulation problem, before the additional work, was actually the longest of any of the companies, 10hours.

OSA's results include a small signal gain of 16.35dB and a 1dB compression point of 26.6dBm, rather higher than the 12.2dB and 23.0dBm measured for the actual circuit.

Eesof's results were the next to arrive, and proved to be closer to the measurements. Gain was 11.3dB while the 1dB compression was at 21.8dBm. With the alternative Tee structure, the gain was increased by 0.8dB to provide an even closer value

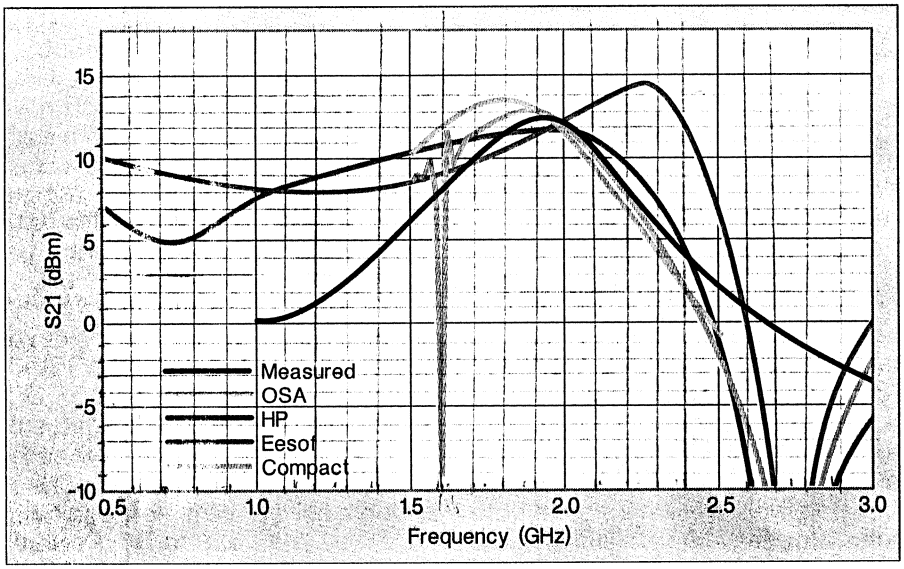

Figure 3 (above left): The linear simulation results for small signal gain, compared with the results measured at University College Dublin.

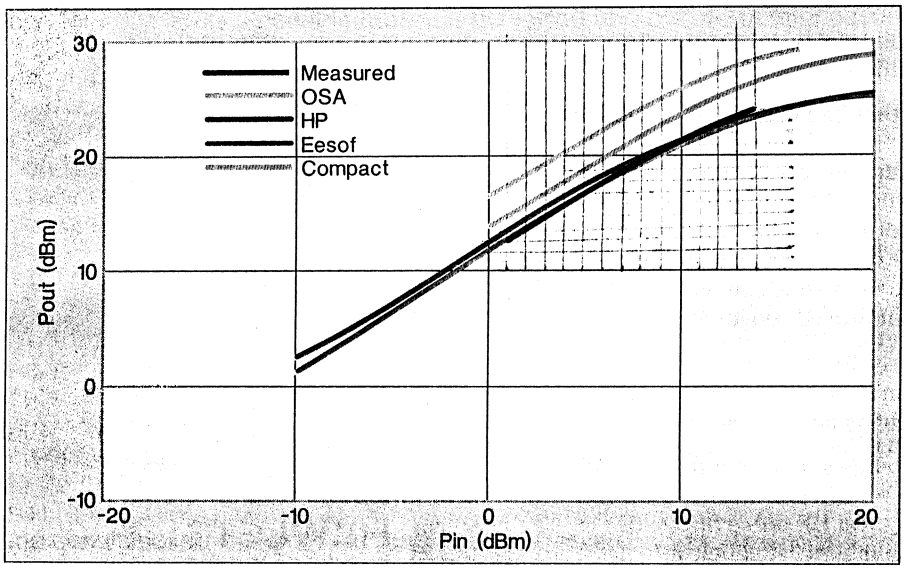

Figure 4 (left): Swept power results at 2GHz for amplifier, showing 1dB saturation point.

Table 1: Simulation times and platforms

	Results received	Terminal time	Simulation time F sweep/Power sweep	Platform
OSA	30/9/93	10 hours	* / 12s (5pts)	Sun Sparcstation 10
HP	19/10/93	40 minutes	0.4 (51pts) / 80 (121pts)	HP735
EEsof	28/10/93	60 minutes	150s (351pts) / 27s (121pts)	HP730
Compact Software	8/11/93	*	15s (101pts) / 180s (41pts)	50MHz 486PC

Benchmark circuit sent 13/9/93 with transistor Spice parameters (i.e. data sheet) 20/9/93.
* Information not supplied.

although the increase in the compression point was rather less, 0.2dB. The results plotted in figures 3 and 4 are not the closest to the measurements but have been selected since the Tee used is believed to be closest to the actual circuit.

Eesof made several comments. All lumped components were modelled as "ideal" and both the connector and the tanδ losses have been ignored.

Turning now to Hewlett Packard, several similar assumptions are quoted which could affect the simulated results. The small capacitors have been modelled as surface mount components while the larger capacitors are assumed ideal. The capacitors in the bias circuit were unfortunately read by the HP application engineer to be 1μF rather than the actual value of 1nF, an error which may well have been caused by the resolution of the FAX transmission. This dramatic change in the value is not, however, thought by the circuit designers to have had a similarly dramatic effect on the performance at 2GHz, and this hypothesis seems to be borne out by the results.

Zener diodes are not common features in microwave simulator libraries so this was created as a "complete fiction" simply to provide the correct dc bias conditions for the transistor. Again substrate loss is ignored.

The predicted performance from S-parameters had understated that obtained from the actual circuit, with 11.0dB gain achieved but the 12.5dB value achieved with the Spice model was very close. The 1dB gain compression point was at 21.5dBm.

The final results to arrive were from Compact Software, a delay that had partly been caused by international travel by leading members of their team, and partly by some confusion over the scaling parameters in the Spice model for the transistor.

The company carried out the work on a 50MHz 486 platform rather than the workstations employed by the other three vendors, so the simulation times quoted should be considered in this context.

In the simulation of the circuit as supplied, Compact suggested that the amplifier would only be capable of 7.4dB linear gain with a 1dB compression point at 17dBm. The explanation for this poor performance has already been reported, but the results plotted in figure 4 are those for an optimised circuit with the netlist changed. Performance achieved is then a 1dB compression point at 2GHz of 25.8dBm with an input of 13dBm. The linear gain prediction had been 11.8dB.

Conclusions

It is certainly rare that four different simulators, should be directed at the same circuit. The efforts of all the companies and their openness in providing the results for scrutiny are appreciated.

Clearly the simulators do not all come up with the same answers. Indeed, taking the results from Compact before modification of the netlist, we have a spread in linear gain predictions and 1dB compression point simulations of 9dB. There is also a significant variation between the small signal gain predictions according to whether they come from the linear simulations or the harmonic balance simulations. The values from Eesof and OSA did not show this discrepancy, although the optimisation by OSA of the non-linear device model using the S-parameters may have made the agreement inevitable.

The closest match to the measured results came from HP and Eesof. Although there were variables in the circuit that could have influenced the results, this would be the case for any real circuit where the simulation is to be undertaken as part of the design process, before building it!

Our original intention was to examine not just single tone responses shown here, but also to look at the first four harmonics, expecting that the results would otherwise be too alike to draw any conclusions. In practice, the time taken by some of the applications engineers to achieve a correct non-linear model for the circuit, basically from a thorough understanding of the Avantek three layer packaged transistor model, precluded that extra level of analysis. This did leave a question mark over the problems an engineer might have with the input of a similar circuit if the world's best CAD-dedicated engineers found it a problem. Beyond that we leave you to judge.

We gratefully acknowledge the contribution of University College Dublin to the CAD review, and here Philip Perry makes some comments on the results.

The CAD review has certainly been an education! The principal problem seems to have come from the use of different models for the bipolar transistor in its packaged form. In the Avantek data book a three layer model is presented with the conventional Spice model embedded in a network of non-linear diodes and capacitors. This, in turn is embedded in a package model of transmission lines, capacitors and inductors.

When Compact presented the full implementation of the model to us, it became apparent that the package model had been omitted. This would account for the discrepancies in the simulated results and the company's inability achieve a good impedance match. HP fully implemented the Avantek model after initially omitting the package.

Upon examining the OSA results, I felt that they too had not included the package. Whilst the optimisation of the model towards the given S-parameters would have offset some of the effects, the use of S-parameters at a single bias point would also have caused some errors. However OSA insists that the package was included in the non-linear model.

It is not clear how Eesof implemented the model, but the simulations do seem close to the measured values.

One common feature of the simulations was the 2.75GHz resonance. This may well be due to the bias circuit, which the companies all chose to simulate, rather than assuming that its effects could be negated by additional circuitry (chokes) as was actually the case, This omission would have allowed a feedback path, but the effect would have been minimal compared to the transistor model problem.