A LOW-POWER AND LOW-JITTER ANALOG FREQUENCY SYNTHESIZER FOR 5G WIRELESS COMMUNICATION AND IoE/IoT APPLICATIONS

A LOW-POWER AND LOW-JITTER ANALOG FREQUENCY SYNTHESIZER FOR 5G WIRELESS COMMUNICATION AND IoE/IoT APPLICATIONS

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TITLE: A low-power and low-jitter analog frequency synthesizer for 5G wireless communication and IoE/IoT applications
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Lay Abstract

The data rate in wireless, cellular communications, and wireline keeps growing by nearly 10 times per 5 years. To fulfill such date rate, implementing complex systems is necessary. Consequently, new challenges are imposed to implement these systems such as noise performance and output power. At the heart of these systems lie frequency synthesizers. Frequency synthesizers are used to up or down convert the carrier signal in communication systems. Phase-locked loops (PLLs) are routinely utilized for frequency synthesis in Radio Frequency (RF)/mm-wave transceivers. The main challenges to design a PLL are phase noise (PN) or jitter, as well as power consumption.

This dissertation aims to implement an ultra-low power and low jitter frequency synthesizer for 5G wireless communication and IoE/IoT applications in 180-nm standard CMOS technology (TSMC). An analog PLL is used in this frequency synthesizer.

Abstract

In the early 1980s and 1990s, the first- and second-generation networks in wireless communication, called 1G and 2G, were introduced with only limited data connectivity in the world. The former could only transfer voices while the latter could transfer voices and messages. By the early 2000s, however, the 3G networks began working and let people have real access to the internet. The greater functionality enabled by 4G networks evolved from increased demand for higher data rates in the early 2010s. Nowadays, we are totally engaged in 4G world of LTE (Long Term Evolution) owing to the eruptive increase of mobile internet in smart phones or other mobile devices. The 5G networks are categorized into two branches according to their frequencies: (i) sub-6 GHz (700 MHz to 6 GHz) and (ii) near-millimeter wave (25 to 30 GHz). Commonly used applications are included in the sub-6 GHz, also called the Internet-of-Everything (IoE) and Internet-of-Things (IoT).

To fulfill the date rate required for 5G applications, implementing complex systems is necessary. Consequently, new challenges are imposed to implement these systems such as noise performance and output power. At the heart of these systems lie frequency synthesizers. Frequency synthesizers are used to up or down convert the carrier signal in communication systems. Phase-locked loops (PLLs) are routinely utilized for frequency synthesis in Radio Frequency (RF)/mm-wave transceivers. The main challenges to design a PLL are phase noise (PN) or jitter, as well as power consumption.

The main objective of this thesis is to carry out research on a fully integrated analog PLL fractional-*N* frequency synthesizer for 5G wireless communication and IoE/IoT

applications in sub-6 GHz. To do this, we have studied the trends in the research of LC-VCOs (voltage-controlled oscillators) and identified the methods for going towards a low flicker-noise corner. Then, we have implemented the designed LC-VCO which is the main noise source in PLLs. In the final step we have designed the sub-blocks of the fractional-N analog frequency synthesis. The sub-blocks have been optimized to have less power dissipations. The implementation of a fully integrated analog PLL fractional-*N* frequency synthesizer is done in 180-nm standard CMOS technology (TSMC). It covers two frequency ranges including 2.4 to 2.48 GHz and 5 to 5.825 GHz. The phase noise at 10KHz varies between -94 dBc/Hz to -115dBc/Hz.

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Elmira, my beloved wife and mother of our little daughter, Liyana, thank you for bringing joy into my life. Now that I've finished my studies, I can enjoy the beautiful world around me!

Mohammad

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Abbreviations

2G	second generation
3G	third generation
4G	fourth generation
5G	fifth generation
LTE	long term evolution
IoE	internet-of-everything
IoT	internet-of-things
AGC	automatic gain control
AM	amplitude modulation
CAD	computer-aided design
CMOS	complementary metal-oxide-semiconductor
FCW	frequency control word
FM	frequency modulation
FoM	figure of merit
GSM	global system for mobile communications
ISF	impulse sensitivity function

LTV linear time-variant

LDO low dropout

MOS metal-oxide-semiconductor

MOSFET MOS field-effect transistor

NMF noise modulating function

NMOS n-channel MOS

PLL phase-locked loop

ADPLL all digital phase-locked loop

PM phase modulation

PMOS p-channel MOS

PNOISE periodic noise

PSD power spectral density

RF radio-frequency

RFIC radio-frequency integrated circuit

RMS root mean square

SFDR spurious-free dynamic range

VCO voltage-controlled oscillator

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Chapter 1 Introduction

1.1 What are 5G and IoE/IoT?

Illustrated in Figure 1-1 (a), in the early 1980s and 1990s, the first- and second-generation networks in wireless communication, called 1G and 2G, were introduced with only limited data connectivity in the world. The former could only transfer voices while the latter could transfer voices and messages. By the early 2000s, however, the 3G networks began working and let people have real access to the internet. Thanks to improved internet speeds, users could now stream music and videos and browse the web, among other things. These capabilities were made possible by increasing the bandwidth of the channels up to 5 MHz.

The greater functionality enabled by 4G networks evolved from increased demand for higher data rates in the early 2010s. Nowadays, we are totally engaged in 4G world of LTE (Long Term Evolution) owing to the eruptive increase of mobile internet in smart phones or other mobile devices. The 5G networks are categorized into two branches, shown in Figure 1-1 (b), according to their frequencies: (i) sub-6 GHz (700 MHz to 6 GHz) and (ii) near-millimeter wave (25 to 30 GHz). Commonly used applications are included in the sub-6 GHz, also called the Internet-of-Everything (IoE) and Internet-of-Things (IoT). Such applications are customer, commercial, infrastructure, and industrial applications, as well as wireless communication standards, for example, 802.11, Unlicensed National Information Instructure (U-NII), High Performance European Radio Local Area Network

(HIPERLAN), and so forth, are included in the sub-6 GHz, shown in Figure 1-2 [1]–[3]. The main requirements for IoE and IoT system-on-chip (SoC) implementations are low power consumption, low phase noise, small silicon area, and low cost.

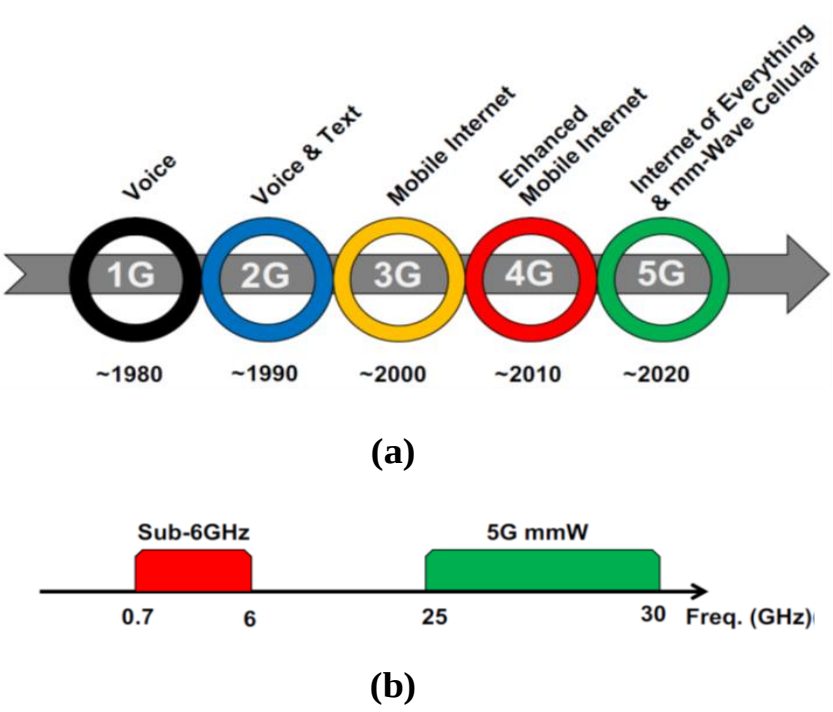


Figure 1-1 (a) 5 generations of wireless communications. (b) Two frequency bands of 5G communications [1].

The data rate in wireless, cellular communications, and wireline keeps growing by nearly 10 times per 5 years, presented in Figure 1-3 [4]. To fulfill such date rate, implementing complex systems is necessary. Consequently, new challenges are imposed to implement these systems such as noise performance and output power. At the heart of these systems lie frequency synthesizers. Frequency synthesizers are used to up or down convert the carrier signal in communication systems. Besides, they can function as

frequency/phase modulators such as FMCW radars. Phase-locked loops (PLLs) are routinely utilized for frequency synthesis in Radio Frequency (RF)/mm-wave transceivers. The main challenges to design a PLL are phase noise (PN) or jitter, as well as power consumption.

This dissertation aims to implement an ultra-low power and low jitter frequency synthesizer for 5G wireless communication and IoE/IoT applications. An analog PLL is used in this frequency synthesizer.

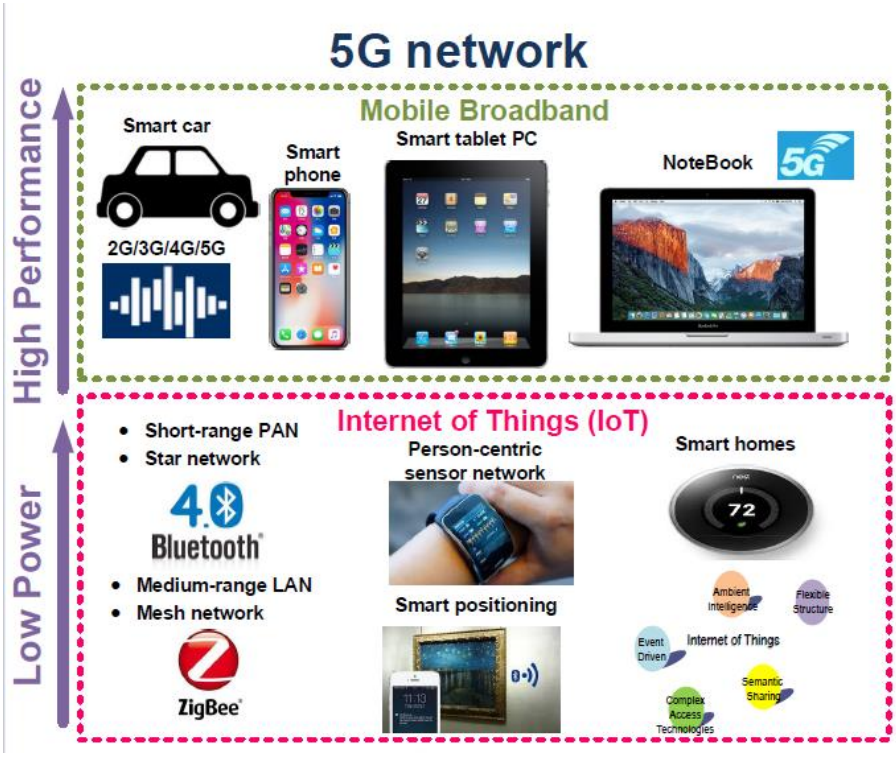


Figure 1-2 Some 5G applications [2].

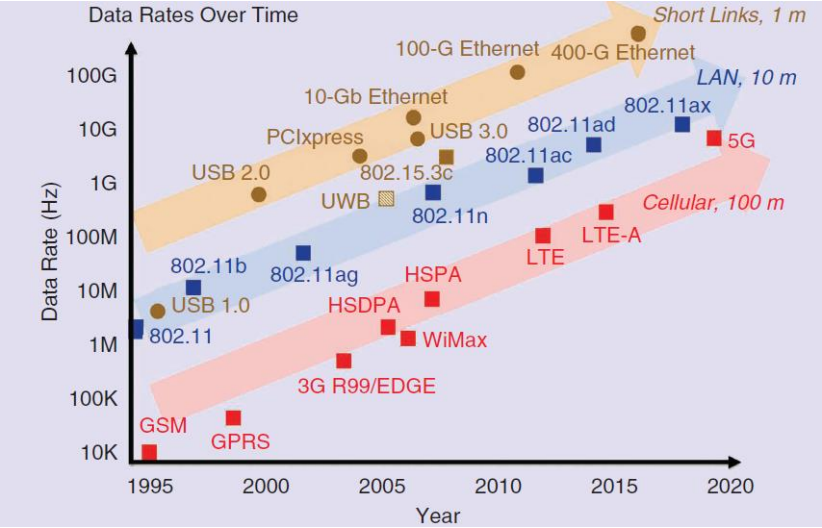


Figure 1-3 Data rate trends in wireline, wireless and cellular communications [4].

1.2 Phase noise required for 5G

Table 1-1 shows some wireless communication standards with their required phase noise. The 5G standard requires jitter less than 90-fs for some applications. To fulfill this requirement and fast lock time, analog phase-locked loops (PLLs) have been recently employed [5]–[7]. As such, we have designed an analog phase-locked loop frequency synthesizer in this thesis for sub-6 GHz applications with an emphasis on reduction of the power dissipation, lock time, and Jitter, all of which are crucial to wireless applications.

We select three frequency ranges, which are often used in IoE/IoT applications. The first frequency range is 2.4-2.48 GHz. Bluetooth and IEEE 802.11b use this frequency range. The second frequency range is 5–5.825 GHz. IEEE 802.11a employs this frequency range. The third frequency range is 5.15-5.35 GHz. U-NII and HIPERLAN utilize this frequency range. Since we design an analog PLL for 5G applications, the PN should be less than

105dBc/Hz and 156dBc/Hz at 200KHz and 20 MHz offset frequencies from the carrier frequency to fulfil requirements for 5G, not for U-NII, HIPERLAN, and IEEE 802.11a. It is worth to mention the approaches provided in this thesis can be easily applied to other wireless communication standards as well.

Table 1-1 Operating carrier frequencies and PN requirements of some wireless communication standards.

Standard	Frequency band (MHz)	PN (dBc/Hz)
GSM 900/1800	880-960 1710-1880	-122 @ 0.6 MHz -132 @ 1.6 MHz -139 @ 3 MHz
UMTS	1920-2170 1900-2025	-132 @ 3 MHz -132 @ 10 MHz -144 @ 15 MHz
Bluetooth & IEEE 802.11a	2402-2480	-84 @ 1 MHz -114 @ 2 MHz -129 @ 3 MHZ
WiFi	2412-2472 5150-5350 5470-5825	-102 @ 1 MHz -125 @ 25 MHz
IEEE 802.11a	5–5.825	-110 @ 1 MHz
4G (LTE)	700-2690	-105 @ 200 KHz -162 @ 20 MHz
5G	700-6000 25000-30000	-105 @ 200 KHz -156 @ 20 MHz

1.3 Analog PLLs: Challenges

With the advance CMOS technology nodes, the supply voltage keeps decreasing for reliability concerns, which is around 0.8 V for 5nm node. However, it imposes new challenges for analog PLLs. The charge-pump current in an analog PLL is reduced, which decreases the loop dynamic range. In the PLLs with a large tuning range, it will cause phase noise (PN) [8], [9].

The noise spectrum of CMOS transistors is nearly dominated by flicker noise, in low frequencies, and thermal noise, in high frequencies. Flicker noise is one of the prominent noise sources in PLLs because it cannot be filtered out like thermal noise. Besides, if CMOS transistors with high-k material are used to reduce the leakage currents [10], the transistor channels will not have uniform threshold across the channel [11], which exacerbates flicker noise. For instance, in RF voltage control oscillators (VCOs) used in PLLs flicker noise can be upconverted to noise around the carrier frequency through various mechanisms and creates PN [12]. The flicker noise is inversely proportional to the channel area of transistors. It means flicker noise becomes worse in the advance CMOS technology nodes (short-channel effects).

Wireless standards for IoE/IoT applications require low PN and spurious tones at the same time. The next part is advocated to PN in 5G.

1.4 Phase Noise in Analog PLLs

Figure 1-4 depicts an s-domain linear model of an analog PLL with noise sources. All the noise sources in Figure 1-4 contribute to the output PN. Each noise source experiences, however, different transfer function to the output. In most analog PLLs, the main phase noise contributions are the VCO, the CP, the PFD, and the divider.

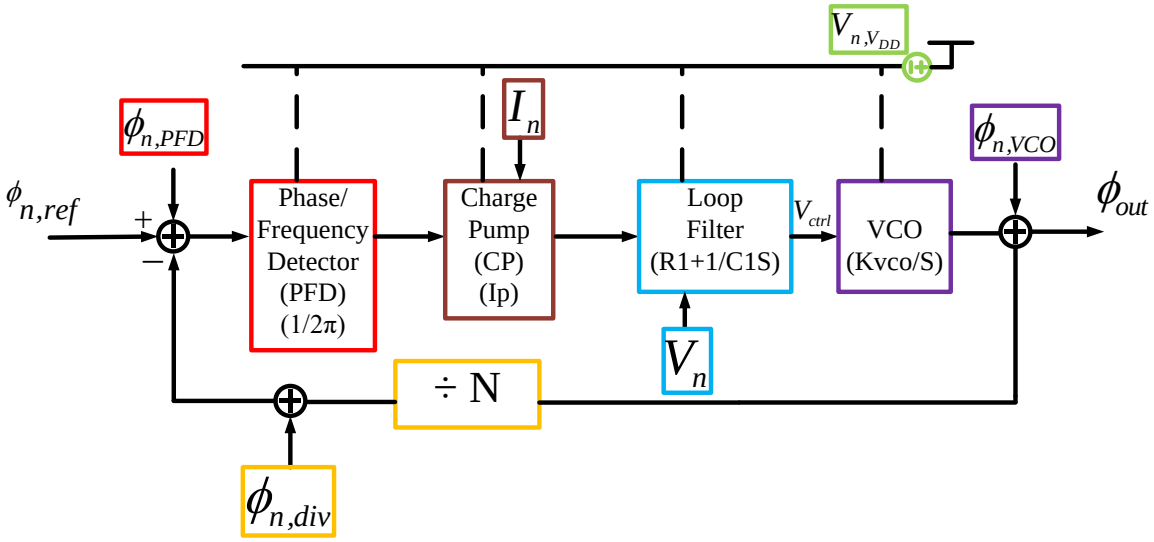


Figure 1-4 The basic block diagram for an analog PLL with noise sources.

The close-loop transfer function between the reference noise, $\phi_{n,ref}$, and output, ϕ_{out}, is

$$\frac{\varphi_{out}}{\varphi_{n,ref}}(s) = \frac{\left(\frac{I_p K_{vco}}{2\pi C_1}\right)\left(R_1 C_1 S + 1\right)}{S^2 + \left(\frac{I_p K_{vco} R_1}{2\pi N}\right) S + \frac{I_p K_{vco}}{2\pi N C_1}}, \tag{1-1}$$

Where we define ω_n, natural factor, and ξ, damping factor, as:

$$\omega_n = \sqrt{\frac{I_p K_{vco}}{2\pi C_1 N}} \quad , \quad \xi = \frac{R_1}{2}\sqrt{\frac{I_p K_{vco} C_1}{2\pi N}} \, . \tag{1-2}$$

The close-loop -3dB bandwidth can be obtained as:

$$\begin{aligned} \omega_{-3dB} &\approx 2.5\omega_n \quad for\ \xi = 1 \\ \omega_{-3dB} &\approx 2\xi\omega_n \quad for\ \xi^2 \gg 1. \end{aligned} \tag{1-3}$$

The transfer function, equation 1-1, exhibits a low-pass response. If we write a transfer function for the charge pump noise, I_n, PFD noise, $\phi_{n,PFD}$, and divider noise, $\phi_{n,div}$, we will see a low-pass behaviour as well. That is, slow noise fluctuations from those blocks travel to the output. However, fast noise fluctuations are filtered out. To reduce the impacts of the slow noise fluctuations, we should reduce the -3dB bandwidth of the low-pass response.

The noise of the resistor in the loop filter can modulate the VCO frequency and give rise to phase noise. The close-loop transfer function between the loop-filter resistor noise, V_n, and output, ϕ_{out}, is

$$\frac{\varphi_{out}}{V_n}(s) = \frac{K_{vco}S}{S^2 + 2\xi\omega_n S + \omega_n^2}\ . \tag{1-4}$$

The transfer function, equation 1-4, shows a band-pass response. Also. the supply noise, $V_{n,VDD}$, illustrates a band-pass response. It means very slow and fast noise fluctuations are filtered out, but the noise fluctuations that are not very fast and slow travel to the output. For reducing the noise influences of these blocks, we should still diminish -3dB bandwidth. For an example, the ripples on the VCO control line because of the loop filter experiences the same transfer function as 1-4, and we need to reduce the -3dB bandwidth to attenuate its effects.

VCO noise experiences a high-pass response. The transfer function related to VCO noise to the output is

$$\frac{\varphi_{out}}{\varphi_{n,vco}}(s) = \frac{S^2}{S^2 + 2\xi\omega_n S + \omega_n^2}. \tag{1-5}$$

The close-loop -3dB bandwidth for the equation 1-5 is

$$\begin{aligned} &\omega_{-3dB} \approx 1.55\omega_n \quad for\ \xi = 1. \\ &\omega_{-3dB} \approx 2\xi\omega_n \quad for\ 2\xi^2 \gg 1. \end{aligned} \tag{1-6}$$

The high-pass response for the VCO noise shows the slow VCO noise is supressed, but the fast VCO noise, or jitter integration, travel to the output. We summarize the above discussion in Table 1-2.

It is clear that there is a trade-off between the VCO noise suppression and the reference, charge pump, loop filter, divider, and supply noise suppression. While increasing the close-loop -3dB bandwidth for the VCO noise suppression is essential, we need to decrease the close-loop -3dB bandwidth for the other noise source suppression in an analog PLL. To alleviate this issue, we need to reduce the flicker noise corner in the VCO phase noise. As shown in Figure 1-5, if the VCO phase noise is moved to the left side of the coordinate axis, the close-loop ω_{-3dB} can be reduced while the VCO noise is suppressed. This trade-off and the flicker-noise corner reduction are the foundations of this thesis.

Table 1-2 A summary of noise rejection in an analog PLL.

Parameters	LPF	BPF	HPF
Rejection of input, PFD, and charge pump noise	Yes	No	No
Rejection of loop filter noise and supply noise	No	Yes	No
Rejection of VCO noise	No	No	Yes
Fast acquisition	No	No	Yes
Reduction of jitter integration	No	No	Yes
Rejection ripple on VCO control line	Yes	No	No
Improve loop stability against parasitic poles	Yes	No	No

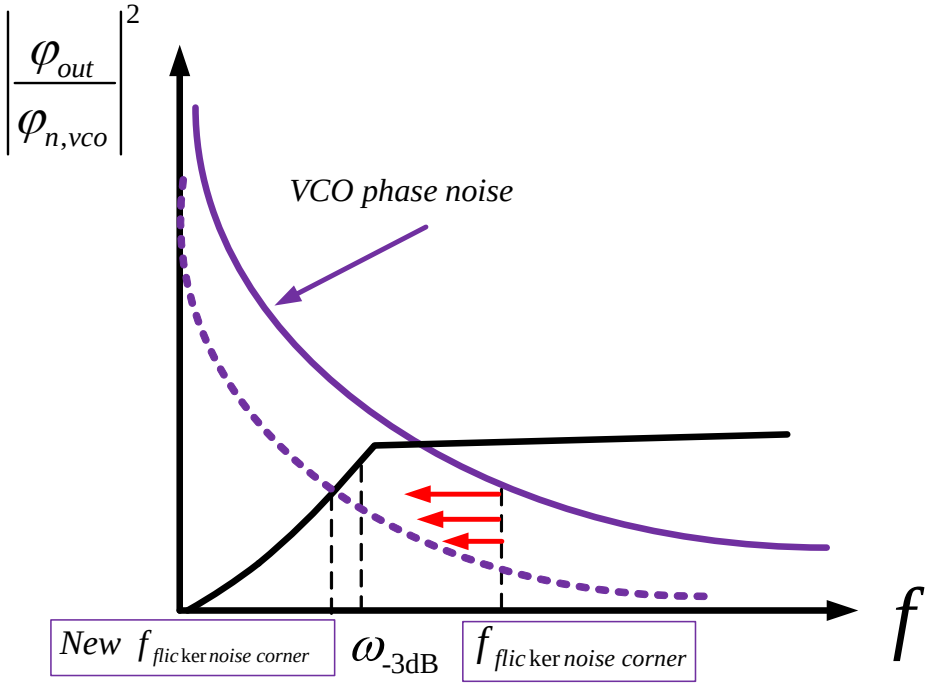


Figure 1-5 This plot shows the idea of moving the flicker noise corner to the left side of the coordinate axis to release the trade-off between supressing VCO noise and the other noise sources in an analog PLL.

1.5 Thesis objective

The main objective of this thesis is to do research and followed by an implementation of a VCO with a low-flicker noise corner to be capable of releasing the trade-off between supressing the VCO noise and the other noise sources in an analog PLL. Consequently, the first objective is to study and understand the trends in the research of VCOs and identify the methods for going towards a low flicker-noise corner. Between LC-VCOs and Ring-VCOs, we prefer LC-VCOs because they have better phase noise than its counterpart. Therefore, we devote one chapter to study LC-VCOs.

With these insights the second objective is to implement the required LC-VCO which is the main noise source in PLLs. The final objective is to design a low-jitter and low-power fractional-N analog frequency synthesis for IoE/IoT applications. To achieve this aim, the performance-limiting sub-blocks need to be optimized.

1.6 Thesis Outline

This thesis is organized as follows. Chapter 2 presents a comprehensive study of PN suppression in LC-tank oscillators. The goal of this study is to provide designers with the latest techniques for reducing PN in cross-coupled oscillators. To this end, we begin with a discussion of two prevalent PN models in oscillators: Hajimiri and Demir. We prefer the Hajimiri model because it does not involve very complicated math and it offers engineers better insight into designing low-PN oscillators in the two-PN close-in regions in an oscillator spectrum ($1/f^2$ and $1/f^3$). In $1/f^2$ region, we show that a need for a large output-voltage swing leads to class D and B oscillators, and a large output-current swing results in

class C oscillators. Also, reduction of the Impulse Sensitivity Functions (ISFs) of an oscillator core can happen in class F oscillators.

A few solutions are presented for mitigating flicker noise up-conversion, such as adding resistances, controlling the oscillation amplitude, decreasing the conduction angle, guiding the high-frequency harmonics of current, and shifting the phase of V_{GS} against V_{DS}. We also provide a comparison of recent state-of-the-art literature to show what constitutes a good PN in both $1/f^2$ and $1/f^3$ regions in cross-coupled oscillators. We conclude that a cross-coupled oscillator can reach the best performances in $1/f^3$ and $1/f^2$ PN regions if the oscillator is designed in class C with the K block and uses the techniques of narrowing the conduction angle, the tail inductor, and the modified tank simultaneously.

Chapter 3 offers a modified cross-coupled oscillator in 0.18um CMOS process. The argument in this chapter is to provide an innovative approach to improve the phase noise. The proposed method offers an improved phase noise specification compared to the most traditional ideas in which the higher current dissipations is the key element of the phase noise improvement. The proposed oscillator is capable of an extra oscillation amplitude without increasing the current level, taking advantages of tail current elimination and topology optimization. Analysis of the peak voltage amplitude can verify the optimum performance of the proposed oscillator. This chapter also presents a rigorous theoretical phase noise analysis of the proposed oscillator. A closed-form formula is derived of the phase noise in the $1/f^2$ region. To verify the derived results, the results are validated against

the simulations and illustrate good matches. The overall phase noise error has less than 3 dB error over the offset frequencies from the carrier.

Chapter 4 presents a fully integrated analog phase-locked loop (PLL) fractional-*N* frequency synthesizer for 5G wireless communication and IoE/IoT applications. To demonstrate the effectiveness of this frequency synthesizer, we apply it to three wireless communication standards. Contrary to using Verilog or VHDL to implement the programmable frequency divider, we propose a new approach in the transistor level with a new divide-by-2/3 circuit, dynamic asynchronous resettable D and JK flipflops, and the OR & AND gates to customize the divider for low-power, low-jitter, and fast-lock time applications. In addition, we have designed a new frequency phase detector (PFD) to overcome the dead region issue. An ultra-low phase noise and low-power voltage control oscillator (VCO) is exploited from Chapter 3 with the flicker noise corner frequency around 10 KHz to achieve the lowest possible phase noise. The implementation is done in 180-nm standard CMOS technology. It covers two frequency ranges including 2.4 to 2.48 GHz and 5 to 5.825 GHz for these wireless communication standards.

Chapter 5 concludes this dissertation and gives suggestions for future developments.

1.7 Original Contributions

The original contributions of the thesis are as follows:

1) Design of a LC VCO with a low flicker noise corner (10KHz) suitable for 5G applications; we designed and implemented a LC VCO in 180-nm standard CMOS

technology (TSMC) in Chapter 3. This LC VCO can have a low flicker noise corner around 10 KHz in simulations and nearly 50 KHz after the implementation.

2) Design of a PFD without glitches; we designed a PFD in Chapter 4 in 180-nm standard CMOS technology (TSMC) to get rid of the output glitches in the PFD.

3) Design of dynamic asynchronous resettable D flipflop based on TSPC D flipflop; since we use 180 nm CMOS technology, the simple TSPC D flipflops cannot work over 2 GHz. To solve this problem, we designed a modified dynamic asynchronous resetable D flip-flop in Chapter 4.

4) Design of a frequency synthesizer for 5G applications.

Chapter 2 A Comprehensive Overview of LC-VCOs

2.1 Introduction

Technological advances and the growth in wireless communication systems, data rates and channels are increasing at unprecedented rates. To comply with strict and exact PN specifications in modern communication standards, oscillators need a special design. It is well known that a PN close-in spectrum of CMOS RF oscillators nearly consists of two significant regions, 1/f^2 and 1/f^3, arising from white and flicker noise respectively, as illustrated in Figure 2-1[13]. There is tremendous interest in mitigating PN in these regions in LC oscillators, particularly voltage biased oscillators, in which the tail current is eliminated. Using the oscillators in phase locked-loops (PLLs) can mitigate PN in those regions. On the other hand, if the loop bandwidth (BW) of a PLL is less than 1 MHz in order to decrease the noise contribution of charge-pump, reference and frequency divider, virtually applied to all cellular phones, $1/f^3$ PN region can still be problematic [14]. For example, a type-II all digital PLL (ADPLL) needs to have a BW less than 400 MHz to prevent the reference noise from dominating the ADPLL's PN [15].

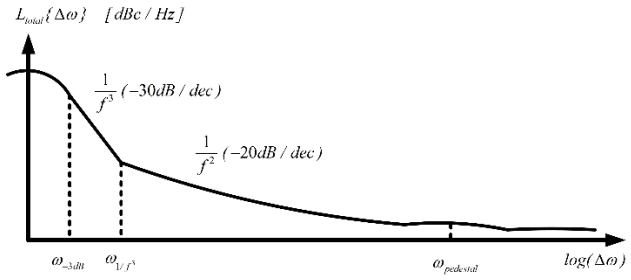


Figure 2-1 A diagram of PN for an oscillator [13].

In the last few decades, many studies have been undertaken to model comprehensively the nature of PN in electrical LC oscillators since the oscillators are nonlinear and produce large signals. In addition, the conversion of noise into the PN is not constant but varies with time over one oscillation period. Many of the phase-noise formula are more complicated than Leeson's experimental formulation [16]. In the last two decades, two models have been commonly employed [17], [18].

The first model, provided by Demir *et al.*, which is rooted in Kartner [19], is very precise and applies to any oscillator such as optic oscillators. In this model the perturbation is decomposed into a phase-deviation component and an additive component termed orbital deviation by Demir [20]. Although this model is extremely accurate and used in modern commercially available circuit simulators such as Spectrum RF [21], the mathematical model is very complicated and does not allow the designer to gain physical insight into the PN generation mechanism [17].

The second model, introduced by Hajimiri and Lee [13], is a linear time-variant (LTV) model applied only on electrical oscillators. It uses a time-dependent transfer function called an Impulse Sensitivity Function (ISF). An ISF indicates how much phase shift stems from exerting a unit current impulse, which is the ratio between the phase shift caused by an instantaneous current perturbation and the amount of injected electric charge. This model defines two impulse response functions for any noise source, which are concerned with amplitude and phase perturbations. The impulse response related to the amplitude perturbations is routinely of little interest because the amplitude noise is eliminated by the

amplitude-limiting mechanism. By contrast, the impulse response corresponding to the phase perturbations is of particular interest since the PN cannot be omitted by the same technique.

Even though this model can capture the time variant nature of electrical oscillators and help designers gain better insight into PN generation mechanism, it fails to predict PN once the perturbation is injected whose frequency is very close to the oscillation frequency. That is why the model is not able to predict injection-locking phenomena [22]. For these reasons, all the methods provided in this thesis are based on Hajimiri and Lee model [17].

To clarify the Hajimiri and Lee model, consider, as an example, a parallel LC resonating tank, shown in Figure 2-2 with the voltage across the capacitor and the current flowing through the inductor being given by $V_C(t) = A_0 \cos(\omega_0 t + \varphi)$ and $I_L(t) = A_0 \omega_0 C \sin(\omega_0 t + \varphi)$, respectively. The injection of a charge pulse $i(t) = \Delta q \delta(t-\tau)$ at time $t = \tau$ results into an instantaneous variation of the voltage across the tank equal to $\Delta V_C = \Delta q/C$. As shown in Figure 2-3, if the charge pulse is injected at the peak of the voltage, no phase perturbation occurs and $h_\varphi(t, \tau) = 0$. On the other hand, if the injection happens during the zero crossing, as depicted in Figure 2-4, the phase error reaches its maximum value, given by $\Delta\varphi = \Delta q/q_{max}$; where $q_{max} = A_0 C$ is the maximum charge stored in the tank capacitor. Since the oscillator has no time references, such an induced phase error is permanent and cannot be recovered. On the contrary, the amplitude perturbation is progressively attenuated by the transconductor non-linearity.

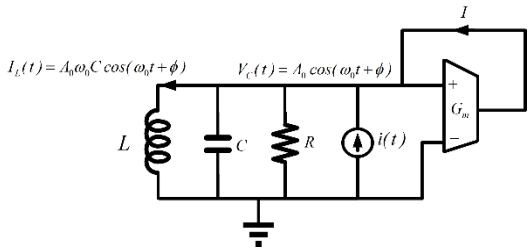


Figure 2-2 Equivalent circuit of a LC oscillator [13].

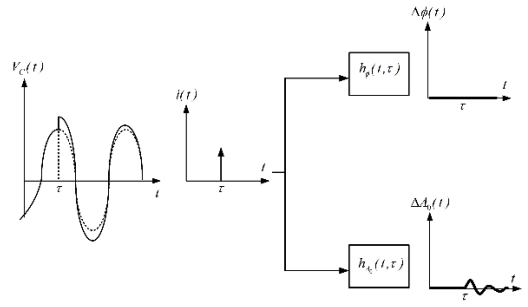


Figure 2-3 Impulse response of oscillator output waveform to a charge pulse injected during the peak of the sinusoidal voltage across the tank capacitor [13].

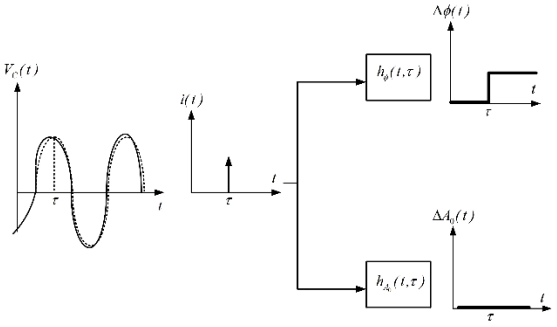


Figure 2-4 Impulse response of oscillator output waveform to a charge pulse injected during the zero crossing of the sinusoidal voltage across the tank capacitor [13].

The impulse phase response, $h_\varphi = \Delta\varphi/\Delta q$, is given by:

$$h_\varphi(t,\tau) = \frac{\Gamma(\tau)}{A_0 C} u(t-\tau), \tag{2-1}$$

where $\Gamma(t)$ is the so-called impulse sensitivity function, taking into account the periodic dependence of the induced phase shift on the charge injection time, and $u(t)$ is the unity-step function. In general, given a current disturbance $i_n(t)$ between two nodes, the corresponding phase perturbation $\Delta\varphi(t)$ can be calculated by using (2-1), resulting:

$$\Delta\varphi(t) = \frac{1}{q_{\max}} \int_{-\infty}^{t} \Gamma(\tau) i_n(\tau) d\tau, \tag{2-2}$$

where q_{max} is the maximum charge across the capacitor placed between the nodes of interest.

It could be argued that the most recent researches in LC oscillators are derived from an innovative change in differential Colpitts and cross-coupled oscillators [23]–[36]. A precise study of phase noise in these oscillators was conducted in [37] according to Hajimiri's method. The results show that the cross-coupled oscillator has better phase noise than the other one. Moreover, a Colpitts oscillator is of a poorer startup current than that of cross-coupled structures, thereby leading to higher power consumption. Thus, most of work on the Colpitts oscillator could not present an impressive improvement from the side of dissipating power consumption and phase noise [38]. In this dissertation we only address the topologies concerned with the cross-coupled oscillator; see Figure 2-6.

The purpose of this chapter is to provide a logical view of how the topology of a cross-coupled oscillator is evolved to improve PN in $1/f^2$ and $1/f^3$ regions. With this perspective, a designer can choose the best topology that is suitable with his needs. To this end, we first provide a general PN formula in $1/f^2$ region. By using this formula, we show that a need of a large output-voltage swing leads to class D and B oscillators and a demand of a large output-current swing results in class C oscillators while class F oscillators can reduce the ISFs of an oscillator core. In $1/f^3$ PN region, we are seeking alleviation in the DC value of effective ISFs in an oscillator core and symmetry in the output waveforms. They can be done by rising linearity, adding resistances, controlling the oscillation amplitude, decreasing the conduction angle, guiding the high-frequency harmonics of current, and shifting the phase of V_{GS} against V_{DS}.

This chapter is organized as follows. Section 2.2 provides a comprehensive study on thermal noise converted to $1/f^2$ PN and techniques used to mitigate it. Sections 2.3 expands on this topic but addresses flicker noise up-conversion. Section 2.4 provides a comparison of recent state-of-the-art literature. Section 2.5 gives a conclusion.

2.2 $1/f^2$ PN Region

A LC-tank oscillator can be generally shown as Figure 2-5 [39], in which R_T is $Q/(\omega_0 C)$ indicating the LC-tank losses and the energy restoration representing active devices. The PN $L(\Delta\omega)$ and figure of merit (*FoM*) of this oscillator based on the Hajimiri and Lee model in $1/f^2$ region may be given by [39].

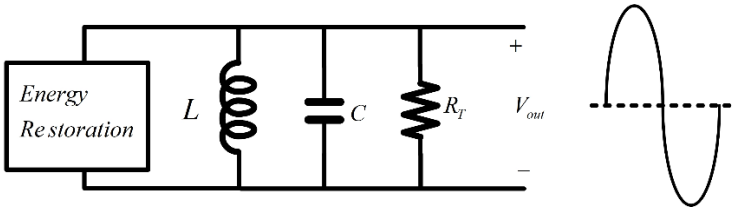


Figure 2-5 A general schematic for a LC-tank oscillator [39].

$$L(\Delta\omega) = 10Log\left[\frac{4kT}{P_{DC}}\frac{\Gamma_{T,rms}^2 + \Gamma_{M,rms}^2\alpha}{\eta_P}(\frac{\omega_0}{2Q\Delta\omega})^2\right], \tag{2-3}$$

$$FoM = 173.8dBc/Hz + 10Log\left[\frac{\eta_P Q}{\Gamma_{T,rms}^2 + \Gamma_{M,rms}^2\alpha}\right], \tag{2-4}$$

Where K is Boltzmann's constant, T is the absolute temperature, ω_0 is the oscillation frequency, α is a noise factor that includes γ_{MOS} and attenuation between tank and MOS gates, $\Gamma_{M,rms}$ and $\Gamma_{T,rms}$ are the rms values of impulse sensitivity function (ISF) for active devices and R_T, Q is the tank quality factor, P_{DC} is DC power, $\Delta\omega$ is the offset frequency, and η_P is power efficiency defined as

$$\eta_P = \frac{P_{RF}}{P_{DC}} = \frac{I_{RF}}{I_{DC}}\frac{V_{RF}}{V_{DC}} = \eta_I\eta_V, \tag{2-5}$$

where I_{RF} and V_{RF} are the rms values of the fundamental components of current and voltage across R_T also called voltage and current efficiency since DC voltage and current are converted to RF voltage and current, V_{DC} and I_{DC} are the supply voltage and current. From (2-3), to improve the PN and *FoM*, one can plays with Q, V_{RF}, I_{RF}, the rms ISFs, and α.

2.2.1 Tank Quality Factor

There are two approaches to implementing the tank inductor: passive and active. The passive inductor is commonly designed since the quality factor of a tank is nearly dominated by the inductor *Q* and the passive inductors available in the technology files (libraires) usually have quality factors less than 10. The literature shows the *Q* of the designed passive inductors is virtually between 10 to 16 [13], [40], [41]. Note that if the tank *Q* is doubled, the PN is improved by 6 dB.

Active inductors have been an active area of research for many years [42], [43]. An active inductor based on gyrator-C network is a promising candidate in the design of reconfigurable RF front-end blocks like oscillators. Oscillators based on active inductors find applications in SerDes, frequency doublers, bandpass filters, and so on [44]. Less area is consumed in oscillators with an active inductor and wide tuning range in multi-standard IoT applications.

Oscillators that use a passive inductor to form the resonator network provide superior phase noise but a limited tuning range. By contrast, oscillators with active inductors are more power-consuming than oscillators with passive inductors. But they have a wide tuning range and a moderate phase noise. Power consumption can be minimized by a suitable choice of active inductor topology [45]–[47]. Nonetheless, in this chapter we only focus on evaluations in the oscillator core rather than tank. Therefore, no discussion of active inductors is provided.

2.2.2 Class D Oscillators

Larger V_{RF} gives lower PN as long as the active devices do not enter the triode region over an oscillation period. One way to have large voltage swings across the tank is to use the voltage-biased oscillators, represented in Figure 2-6, but at the cost of less current efficiency because the core transistors will enter the triode region. In this structure the tail current source is eliminated. Therefore, a source of PN is omitted. Notwithstanding, it gives rise to increasement of the sensitivity to supply voltage.

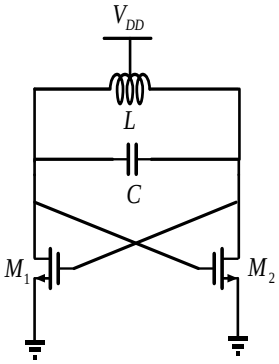


Figure 2-6 A voltage-biased oscillator.

Another way to have a large V_{RF} is to exploit a class *D* oscillator that resembles a voltage-biased oscillator, shown in Figure 2-7, [48]. The differences between the class D and the voltage-biased oscillator are rooted in this fact that the sizes of the transistors are very large in the class D oscillator to make the transistors as an ideal switch. The single-ended maximum swing is nearly equal to 3 V_{DD}. In [48] the core transistors are considered ideal switches and their noises converted to PN are ignored, but the noise that the transistors

inject into the tank should be considered [49]. Besides, such oscillators suffer from high supply pushing and flicker PN corner.

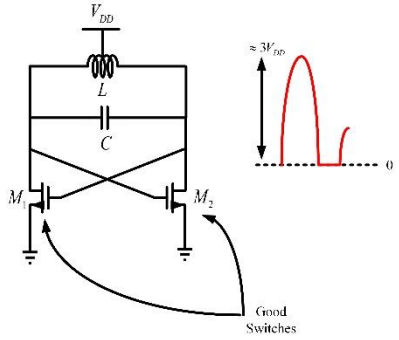


Figure 2-7 A class D oscillator [48].

2.2.3 Class B Oscillators

Another approach to increase the voltage efficiency (V_{RF}) is to employ a class B oscillator as indicated in Figure 2-8 (a) [50]. Ideally, the class B oscillator can have a single-ended output swing equivalent to V_{DD}, the first harmonic of the tank current is $(2/\pi)\ I_{DC}$, and the tank current looks like a square wave, shown in Figure 2-8 (b). Therefore, the voltage and current efficiency are 1 and $2/\pi$, respectively.

One drawback of this approach is that the tail transistor does not act as an ideal current source and requires a voltage to be dropped across its drain and source nodes to keep this transistor in the active region. Consequently, the voltage and current efficiencies in the class B oscillator are dropped to 0.8 and $1.57/\pi$ respectively, as demonstrated in Figure 2-8 (c). In this case, the core transistors enter the triode region, and there is a valley at the peak of the current, which indicates the shape of tank current is not like a square wave

anymore. By augmenting the size of the tail transistor, the voltage efficiency could be enhanced, but cause PN deterioration since g_m is increased and PN is proportional to g_m in $1/f^2$ region.

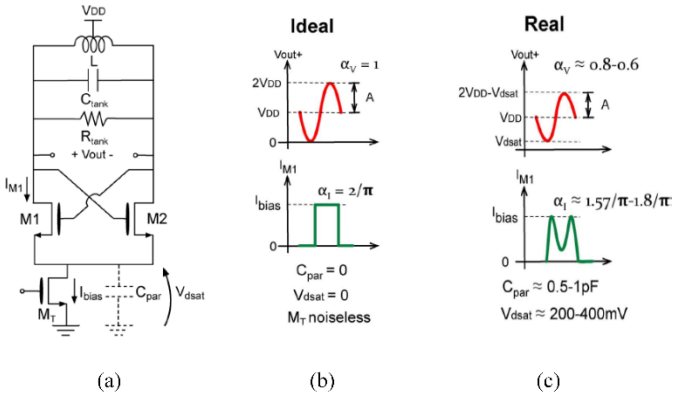


Figure 2-8 A class B oscillator (a) its topology (b) its transistor current in the ideal condition (c) its transistor current in the real condition [50].

2.2.4 Class C Oscillators

To have a higher current efficiency (I_{RF}), a class C oscillator, presented in Figure 2-9, can be used since active devices are more in the active region.

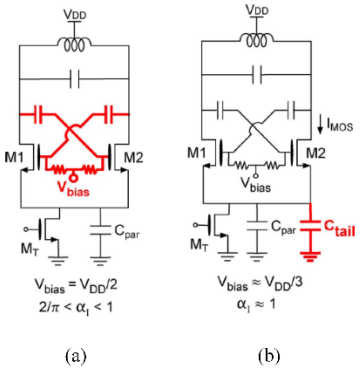
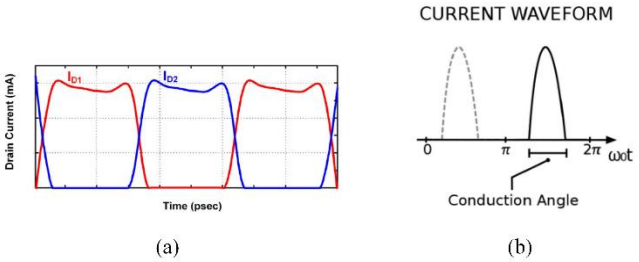


Figure 2-9 A class C oscillator (a) when Vbias is VDD/2 (b) Vbias is VDD/3 [50].

The topology of class C is analogous to class B with two differences. One difference is to bias the gate of switching transistors separately, and another difference is to use a capacitor in the tail node. In Figure 2-9 (a) the gates of the core transistors are biased separately below V_{DD}. The bias voltage V_{bias} is $V_{DD}/2$. The current of transistor M_1 is shown in Figure 2-10 (a). As can be seen, there is still a valley in the current waveform, but it is less than that of the current waveform in class B, as shown in Figure 2-8. In this case, the current efficiency is between $2/\pi$ and 1. This topology is not fully a class C oscillator since the cross-coupled transistors enter slightly the triode region, but they are prevented from entering the deep triode and PN is improved. Note that the capacitor in tail node in Figure 2-9 (a) is the parasitic capacitor and this capacitor is not deliberately implemented.

In Figure 2-9 (b), an additional large capacitor (C_{tail}) is purposely added in parallel to the tail current source along with applying a voltage bias to the gates of the core transistors. The bias voltage V_{bias} is $V_{DD}/3$. Contribution of the extra capacitance C_{tail} and the bias voltage changes the drain current of M_1 and M_2, demonstrated in Figure 2-10 (b). The shape of the current waveform looks like a tall and narrow pulse, which means the conduction angle is reduced. In this case, alleviation of flicker noise up-conversion is expected [51]. Furthermore, the added capacitance can filter out the high frequency noise of the transistor current, which allows us to have a greater transistor current, thereby improving the voltage efficiency.



(a) (b)

Figure 2-10 The current of transistors related to (a) Figure 2-9 (a) [52] (b) Fig. 9 (b) [39].

Nonetheless, the class C oscillator suffers from achieving the largest possible oscillation amplitude. There is a trade off between a robust start-up and the utmost achievable oscillation amplitude. At the start-up, the bias voltage should be high enough to keep the current transistor in the active region, but when the oscillator reaches steady-state, the lower bias voltage would be enough. Also, as mentioned above, the cross-coupled transistors are not allowed to enter the triode region. Consequently, it confines again the maximum achievable oscillation amplitude. To solve this issue, dynamic bias class C oscillators have been put forward in [50], [53], [54], as exhibited in Figure 2-18. Although the voltage efficiency is improved by the dynamic bias technique, the dynamic bias class C oscillators are not still able to reach the maximum achievable oscillation amplitude.

2.2.5 Class F Oscillators

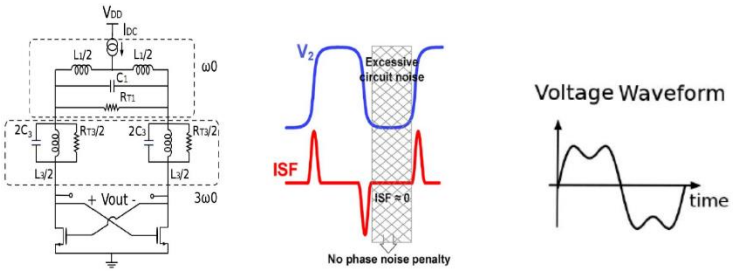
When it comes to $\Gamma_{M,rms}$ and $\Gamma_{T,rms}$, ideally if the ISFs are zero, no noise is converted to PN. Hence, lower ISFs lead to PN improvement. Reduction in ISFs occurs in class F oscillators, presented in Figure 2-11 (a) [55]. Class F uses two tanks; one is oscillated at ω_0 and the other is oscillated at $3\omega_0$, since a square waveform at the output is desirable. The idea is to have an output waveform resembling a square wave to decrease PN. Two

mechanisms will improve PN. First, it is well known that none normalized ISF can be obtained by [21].

$$\Gamma(t) = \omega_0 \frac{q_{\max}}{C} \frac{\vec{\dot{X}}}{\left|\vec{\dot{X}}\right|^2}, \tag{2-6}$$

Where $\Gamma(t)$ is the ISF, X is a state variable that is the voltage across the tank capacitance, $q_{max} \approx A_0 C$ is the maximum dynamic charge across the tank capacitance (A_0 being the oscillation amplitude), ω_0 is the angular frequency of oscillation, $\vec{X}$ is the first derivative of the state vector. We know the voltage waveform across the tank capacitor looks like a square wave. This means that the first derivative of the square wave over the entire period when the waveform is flat is zero, as represented in Figure 2-11 (b). Even though the cross-coupled transistors are pushed deeply into the triode region and inject significant noise into the tank during this interval, the ISF is zero and no noise is converted into PN.

The real output voltage of the class F oscillator is shown in Figure 2-11 (c). As can be seen, because the waveform is not quite a square wave, the ISF is not zero anymore but the ISF is reduced. Another mechanism in the class F oscillator resulting in PN improvement is due to increasing the oscillation zero-crossing slope. The reason why it can improve PN is because the transistors are dissipating power for a shorter span. Thus, PN is improved for the sake of the increasement of power efficiency.



(a) (b) (c)

Figure 2-11 A class F oscillator (a) its schematic (b) its ISF (c) its output voltage [55].

2.2.6 More on ISF Reduction

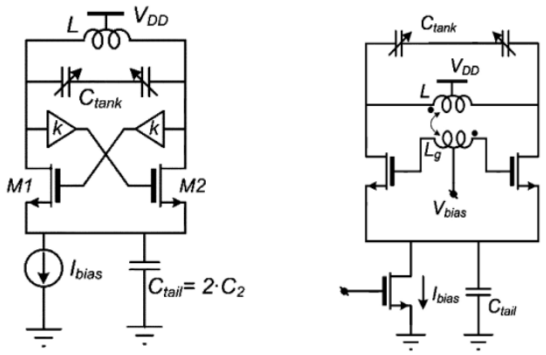
α is proportional to the inverse of the voltage gain between tank and active devices. It can reduce the ISF effects since its value is less than one, see (2-3). To gain better insight into how it can improve PN and *FoM*, (2-4) is rewritten as [56],

$$FoM = \frac{2\eta_p Q^2}{kTF} 10^{-3}, \tag{2-7}$$

Where F is $1+\beta\alpha$, at which β is a constant that relates the current noise of the conductance with its instantaneous conductance. The rest of parameters are already defined. As can be seen from (2-7), if α become small enough, F approaches nearly one. Besides, from (2-4) the ISFs for active devices could be ineffective if α is small enough. Thus, α can play a very important role in designing a high *FoM* and low PN LC oscillator. Once F in (2-7) is equal to one, optimum *FoM* becomes:

$$FoM_{Opt} = 176.8 + 20\log_{10} Q. \tag{2-8}$$

From which only the noise of the tank from Figure 2-5 is converted to PN and the noise of the other elements are not involved. Figure 2-12 (a) displays the conceptual way to change α. If K is 1, the gates of the core transistors are connected to the tank by a wire, like the ones are shown in the class B and C oscillators. K can also be less than one by utilizing a transformer, as depicted in Figure 2-12 (b). While employing a transformer is an ordinary technique to change the α value, making this factor very small is problematic because there is a trade-off between the maximum efficiency and reliability issues for the active devices [56].



(a) (b)

Figure 2-12 (a) A conceptual way to apply α (b) using a transformer to implement α [57].

2.3 1/f^3 PN Region

The analog Section of transceivers must cope with the limitations imposed by the adoption of scaled CMOS processes. One of these limitations is the increasing flicker noise corner frequency of minimum channel-length transistors. The flicker noise (1/f) up-conversion becomes worse when the advance CMOS sub-micrometer technology is

exploited [58]. The flicker noise PN theory has not been developed, such as the thermal PN theory that has been studied since 1966 [16], until the ISF was introduced by Hajimiri in 1998. The flicker noise ($1/f^3$) corner frequency can be described by [13]

$$\omega_{1/f^3} \approx \frac{1}{2}\omega_{1/f}\left(\frac{\Gamma_{EFF,dc}}{\Gamma_{EFF,H1}}\right), \tag{2-9}$$

Where $\omega_{1/f}$ is the 1/f noise corner frequency of a MOS transistor, and $\Gamma_{EEF,dc}$ and $\Gamma_{EEF,H1}$ are the DC value and first harmonic of effective ISF, respectively. $\omega_{1/f}$ is the range of MHz in the advance CMOS technology, which is substantially high for the 5G/6G wireless communication standard. On the other hand, as can be seen from (2-9), the $1/f^3$ can be, in principle, zero if $\Gamma_{EEF,dc}$ becomes zero. $\Gamma_{EEF,dc}$ is the area under the effective ISF waveform. It can be zero if there is a certain symmetry in the drain-source voltage waveform. For instance, this symmetry can be obtained in ring oscillators by adding more delay stages [59]. Nonetheless, the theory was quiet regarding LC-tank oscillators until [60] showed in 2016 that the symmetry could be attained if the even harmonics of current were guided not to enter the capacitive path rather than the resistive path in the tank.

Note that [60] wrongly claimed odd harmonics of current did not have any influences on the waveform asymmetry. This is because [60] just studied a special form of a LC oscillator that was the class B oscillator. Nevertheless, [14], [58], [61] had already shown in 2012 and 2013 that the odd harmonics of current had effects on the waveform asymmetry in the form of harmonic distortion.

Nonetheless, even harmonics of current were not wrongly considered in [14], [58], [61] either. It was again because the case study was another form of a LC oscillator that was the complementary cross-coupled voltage-biased oscillator, illustrated in Figure 2-13. Later in 2020, [62] demonstrates both the odd and even harmonics of current have effects on the 1/f noise up-conversion.

Surprisingly, however, the waveform symmetry is not the only method to suppress the 1/f noise up-conversion [62]. The next Sections discuss other techniques for suppressing the 1/f noise up-conversion.

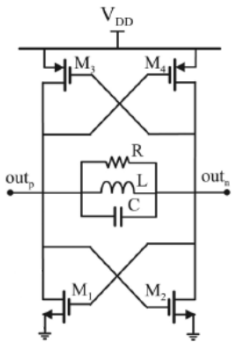


Figure 2-13 The complementary cross-coupled voltage-biased oscillator used in [58].

2.3.1 Methods for the Flicker Noise Up-Conversion Reduction in Current-Biased LC-tank Oscillators

In the last two decades, extensive efforts have been devoted to understanding and minimizing mechanisms of flicker noise up-conversion [31], [62]. Between 2000 and 2010, extensive studies on current-biased LC-tank oscillators, where the tail current source controls the current of the switching transistors such as class B and C oscillators, have been

undertaken since they show more promising robustness against process, voltage, and temperature (PVT) variations. Four major up-conversion mechanisms have been identified so far for this type of oscillators, namely:

1. Conversion of amplitude modulation (AM)-to-phase modulation (PM) due to non-linear varactors;

2. Modulation of the current flowing through the tail capacitance in a current-biased VCO topology;

3. Modulation of parasitic capacitances of the transconductor stage;

4. The Groszkowski effect, i.e., modulation of the harmonic content of the output voltage waveform.

These mechanisms are discussed in the following Sections.

2.3.1.1 A Bank of Digitally-Controlled Capacitors

The first up-conversion mechanism comes from conversion of amplitude modulation (AM)-to-phase modulation (PM) owing to non-linear varactors [63][64], [65][66]. Fortunately, it has been well clarified and can be minimized by employing smaller analog varactors for a finer frequency tuning and a bank of digitally-controlled capacitors for a coarse tuning. This can drastically reduce the AM-to-PM conversion owing to the non-linear capacitances, without impairing the overall VCO tuning range [67].

2.3.1.2 Eliminating Tail Current

The second up-conversion mechanism is rooted in modulation of the current flowing through the tail capacitance in a current-biased oscillator topology [68] [69][70], and the third mechanism comes from modulation of parasitic capacitances of the transconductor stage [71][72].

The literature has investigated the second and third up-conversion mechanisms primarily from a qualitative perspective. No detailed quantitative explanation has been given yet in the literature. Furthermore, although being closely related to each other, they have been studied independently and no comparison has been provided showing which one of these two effects is dominant in current-biased oscillators. Since the up-conversion cause is the presence of a tail node oscillating at even harmonics, one possible solution is to resort to a voltage-biased topology, in which the tail current source is eliminated, see Figure 2-6, [66][67][15][51].

Another solution is to adopt a tail LC resonant filter tuned at twice the oscillation frequency, as presented in Figure 2-14, [56] [73]. The main drawback of this technique is the non-negligible silicon real-estate needed to integrate the filter inductor. Note that a tuning mechanism is needed because the efficiency of this technique is highly sensitive to the variation of oscillation frequency. This technique can introduce more noise if the oscillator has to cover a large frequency band. Hence, it can eventually impair the effectiveness of this solution.

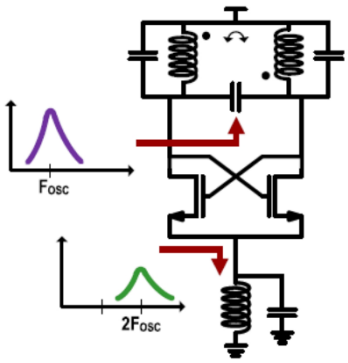


Figure 2-14 A LC oscillator with a tail LC resonant filter [56].

2.3.1.3 Groszkowski Effect

In 1933 Janusz Groszkowski noticed the oscillation frequency in steady state did not perfectly match the resonance frequency of the tank because the current high-frequency harmonics of the active elements flowed into the low-impedance path, which is the tank capacitor, as signified in Figure 2-15 [74]. This phenomenon will increase the tank's net capacitive reactive power. To sustain the oscillation, the tank's net inductive reactive power must rise since the average reactive power delivered to the tank in one oscillation period should be zero. The oscillation frequency is automatically shifted to make the average power zero. Hence, to deliver the inductive power, the current first harmonic of the tank should lag the voltage of the tank, see Figure 2-20. In [74], the oscillation frequency was found to be

$$\omega_0^2 = \omega_R^2 \frac{\sum_{k=1}^{\infty} V_k^2}{\sum_{k=1}^{\infty} k^2 V_k^2}, \tag{2-10}$$

where $\omega_R/(2\pi)$ is the tank resonance frequency and V_k is the amplitude of the k-th voltage harmonic.

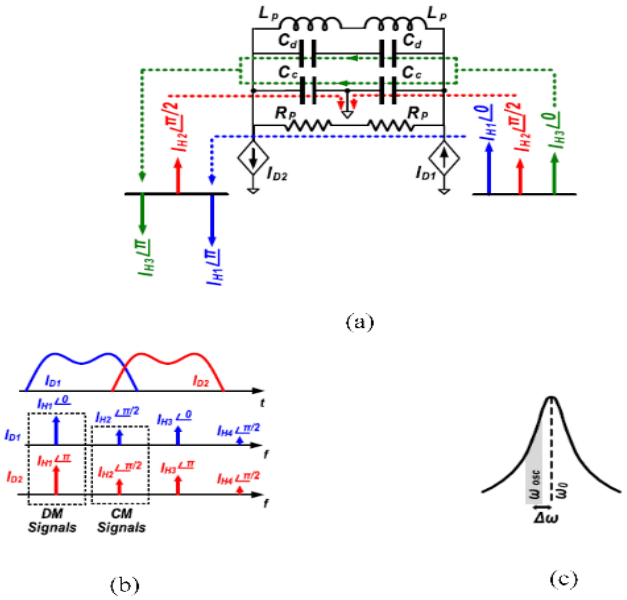


Figure 2-15 The conceptual way to show the Groszkowski effect (a) Current harmonics paths (b) Drain current in time and frequency domains (c) Frequency drift due to Groszkowski's effect [60].

2.3.1.4 Limiting Oscillation Amplitude

The last up-conversion mechanism is originated from the Groszkowski effect, i.e., modulation of the harmonic content of the output voltage waveform [75][69][76][77][78][5][79]. This mechanism, which has received much attention in the literature, can result in PN degradation in oscillators. For instance, [79] showed that use of an automatic gain control (AGC) circuit in a crystal oscillator to limit the amplitude of

oscillation can reduce harmonic distortion. [78] presented the same idea by using an AGC loop to reduce harmonic distortion and improve PN, as represented in Figure 2-16.

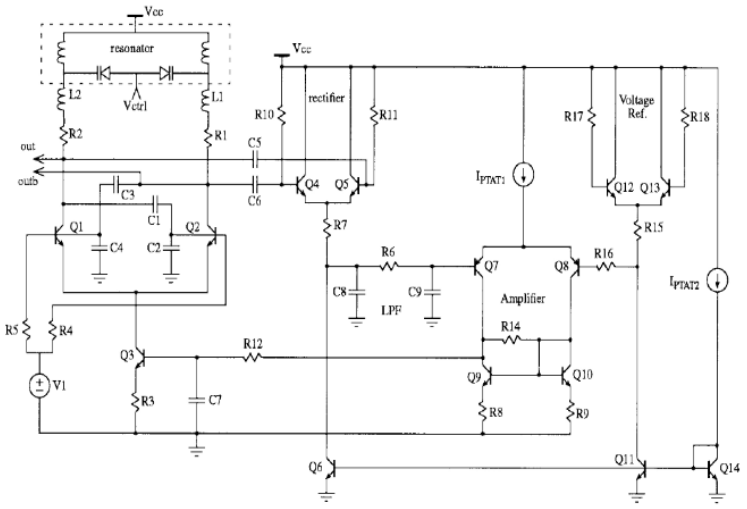


Figure 2-16 A VCO with AGC [78].

Reduction of the device width of switching transistors, thereby increasing the overdrive voltage, in current-biased oscillators to extend the linearity of the transistors was proposed in [76]. In this method the harmonic distortion is mitigated by taking advantage of improvement of PN from both the switching transistors and the flicker noise up-conversion of the bias current.

[77] portrays another solution at which the sources of the switching transistors are degenerated by damping resistors, represented in Figure 2-17, so as to suppress 1/f noise up-conversion and to linearize the transconductor. The harmonic distortion, thereby the Groszkowski effect [74], is reduced. However, the excess gain, thus start-up margin, is deteriorated since the overall transconductor, G_m, in Figure 2-17, changes from g_m to

$g_m/(1+g_m.R_{damp})$, where g_m is the transconductor of a transistor, and supposed that PMOS and NMOS have the same transconductors.

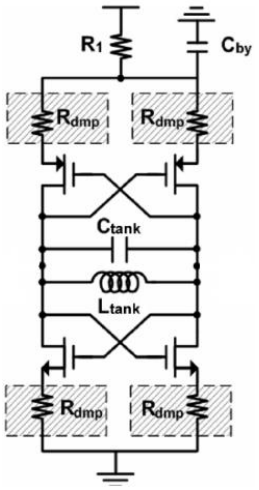


Figure 2-17 A LC oscillator with source damping resistors [77].

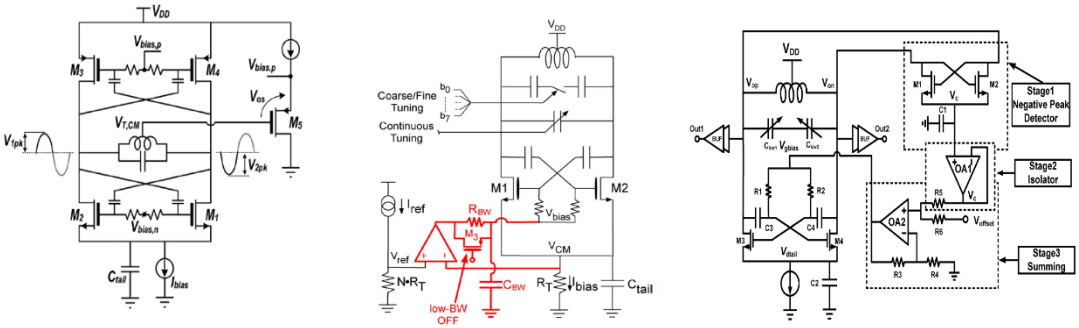
2.3.2 Methods for the Flicker Noise Up-Conversion Reduction in Voltage-Biased LC-tank Oscillators

After 2010, the voltage-biased LC-tank oscillator, where the tail current source transistor is omitted, has become extremely common among designers, see Figure 2-6. Although this topology is more sensitive to PVT, the 1/f noise corresponding to the supply voltage can be suppressed by sizing the core transistors largely in the voltage regulator and bandgap-reference [58]. The tail transistor elimination can also improve linearity (Groszkowski effect [74]). In addition, this topology can be used in the low-power applications since the headroom voltage is increased by removing the tail transistor.

The four 1/f noise up-conversion mechanisms mentioned for the current-biased LC-tank oscillators are reduced to two for the biased-voltage oscillators because the tail transistor is removed. This means that the mentioned second and third noise up-conversion mechanisms do not need to be taken into account. The solutions provided for the first mechanism are still valid for this type of oscillator. The last mechanism, i.e., the Groszkowski effect, has been investigated since 2012 and several solutions have already been provided.

2.3.2.1 Narrowing the conduction angle

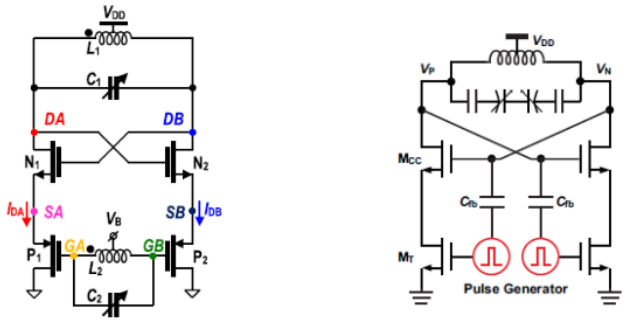
[80] first studied the Groszkowski effect on both Colpitts and the current-biased LC oscillators. [80] provided two solutions to reduce the Groszkowski effect: (1) using an inductor with high-quality factor in the tank and (2) narrowing the conduction angle; see Figure 2-10 (b). The first solution is obvious. The second one is not surprising given that a transistor creates noise only when it is ON. Therefore, the shorter a transistor is ON, the less noise it makes. Narrowing the conduction angle means that the LC-tank oscillator is biased in Class C. Interestingly, [57] had introduced the Class C oscillator in 2008; refer to Figure 2-9. [57], however, did not understand why the $1/f^3$ PN region was improved. In 2013 [53], [50], and [54] proposed a modified class C oscillator to control the oscillation amplitude, and all showed an improvement in the $1/f^3$ PN region, represented in Figure 2-18.



(a) (b) (c)

Figure 2-18 A modified class C oscillator provided in a) [53] b) [50] c) [54].

Recently, [81] and [52] exploited the same idea to narrow the conduction angle by adding two controlled switches under the switching transistors, as shown in Figure 2-19. Note that the current odd and even harmonics are not guided to make the oscillation waveform symmetrical, as mentioned earlier.



(a) (b)

Figure 2-19 A VCO uses the narrowing the conduction angle idea by the controlled switches in (a) [81] (b) [52].

2.3.2.2 Adding Resistors

The Groszkowski effect comes from the fact that the currents of switching transistors have harmonics. The first harmonic is trapped in the resistive path of the tank. But the other high-frequency harmonics will take the low impedance path of the tank, which is the capacitive path. These high-frequency harmonics cause the tank reactive energy to become higher than the tank inductive energy. This unbalanced tank energy must be compensated in order to sustain the oscillation. Thus, the tank inductive energy must be increased. This will be done by shifting the resonance frequency down as shown in (2-10). In other words, the tank current should be lagged with respect to the tank voltage. The phasor plot in Figure 2-20 demonstrates this condition [61].

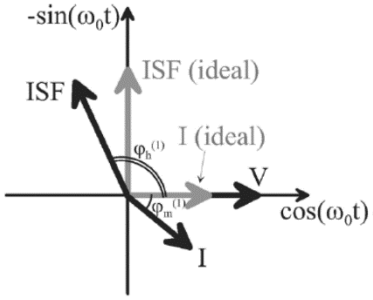


Figure 2-20 Phasor plot of the first harmonics of tank voltage, current, and its corresponding ISF [61].

[14] also depicts if the tank voltage in Figure 2-13 is $A\ cos(\omega_0 t)$, where ω_0 is the resonance frequency, the ISF related to the switching transistors can be estimated mathematically by $1/2\ cos(\omega_0 t+\pi/2)$. Once this ISF is simulated, however, the result is somewhat different, as illustrated in Figure 2-21. As can be seen, there is a discrepancy (φ_ε)

between the ideal ISF, calculated mathematically, and the simulated ISF. The simulated ISF slightly leads the ideal ISF. Figure 2-20 shows this condition. This is why the estimated ISF should be amended as $1/2\cos(\omega_0 t+\pi/2+\varphi_\varepsilon)$. Moreover, it has already been proven that φ_ε has the following relation with the excess gain (G_X), which is the transconductor of the switching transistors:

$$\varphi_\varepsilon \approx \frac{G_X - 1}{4Q} \tag{2-11}$$

At where Q is the tank quality factor and the excess gain is

$$G_X = g_m R \tag{2-12}$$

And g_m is:

$$g_m = \frac{g_{m,n} + g_{m,p}}{2} \tag{2-13}$$

To eliminate the error (φ_ε), we need to decrease the excess gain or to increase the tank quality factor. Keep mind that the excess gain determines the non-linearity of the oscillator. In that case, the linearity of the oscillator should be increased.

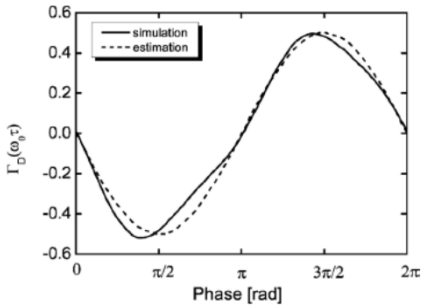


Figure 2-21 Simulated and estimated ISF associated with the switching transistor in Figure 2-8 [14].

[58] showed that if resistors were added to the drains of complementary voltage-biased oscillator in Figure 2-13, the flicker noise up-conversion due to harmonic distortion was suppressed, as depicted in Figure 2-22. Indeed, in this technique the start-up margin is not imposed like that of which resistors are added in the sources of the switching transistors.

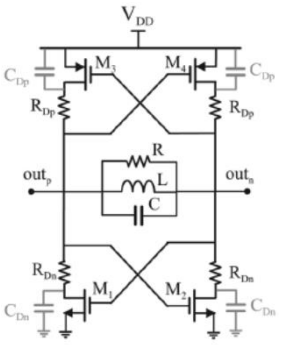


Figure 2-22 A complementary voltage-biased oscillator that resistors are added in the drains of transistors [58].

2.3.2.3 Modifying Tank

Another solution for suppressing the $1/f^3$ PN is to guide the tank-current odd and even harmonics to not take the capacitive paths, and unbalance the tank energy. There are two ways to achieve this goal. One way is to use a tail inductor along with the decoupling capacitance, as exhibited in Figure 2-23 [15], [51], [56], [62]. Note that only the tank-current second harmonic is trapped; the other high-frequency harmonics still make the tank energy unbalanced.

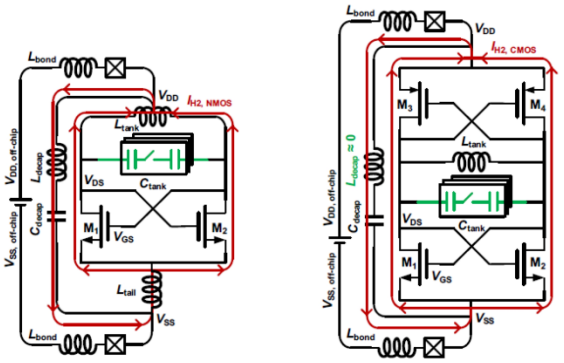


Figure 2-23 The tail inductor technique not to allow the tank energy unbalanced in (a) n-MOS only and (b) complementary oscillators [62].

The other way is to use a tank, resonating at ω_0, with auxiliary resonances at $2\omega_0$, $3\omega_0$, …, and so on. As the current high-frequency harmonics are trapped in a resistive path, the tank energy will not be unbalanced, whereby there is a symmetry in the oscillation waveform. Figure 2-24 displays the idea, at which the designed tank can resonate at ω_0, $2\omega_0$, $3\omega_0$, $4\omega_0$ [82].

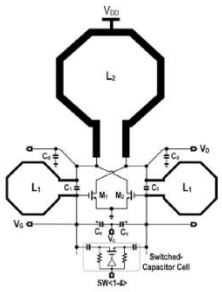
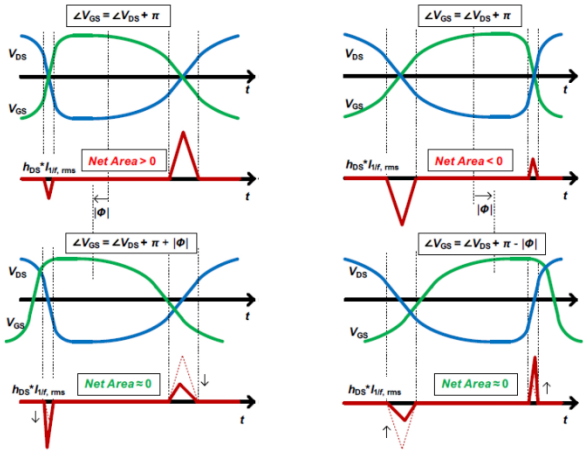


Figure 2-24 An oscillator with auxiliary resonances at $2\omega_0$, $3\omega_0$, $4\omega_0$ [82].

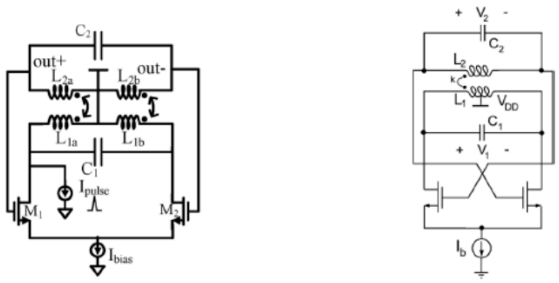
2.3.2.4 Shifting Phase of V_{GS} against V_{DS}

The last solution for mitigating $1/f^3$ PN, investigated so far, is to shift the phase of V_{GS} against V_{DS} [62]. Figure 2-25 shows this basic concept of this technique. When the peak of V_{GS} is moved toward the sharper edges of V_{DS}, the net area of effective ISF becomes zero. Therefore, there is no up-conversion flicker noise to $1/f^3$ PN. [41] and [40] use a transformer to take advantage of this idea, as exhibited in Figure 2-26.



(a) (b)

Figure 2-25 The conceptual idea of moving the peak of VGS towards the sharper edges of VDS to mitigate 1/f3 PN (a) failing (b) rising edges of VDS [62].



(a) (b)

Figure 2-26 A transformer-base oscillator used in (a) [41] (b) [40] to shift the peak of VGS towards the sharper edges of VDS.

2.4 A Comparison Between Literature

Table 2-1 compares the oscillator performances presented in this chapter. The most important parameters in an oscillator are operation frequency, frequency offset, phase noise, power dissipation, tuning range, supply, technology file (process), tank quality factor, and flicker PN corner frequency. It is impossible to embrace all the parameters of an oscillator with one *FoM*. Four *FoMs* are used to meet that objective. The first FoM_1 can capture the operation frequency, frequency offset, phase noise, and power dissipation. Indeed, the oscillator performances in the $1/f^2$ PN region are evaluated by FoM_1. It can be defined by [17]:

$$FoM_1 = -L(\Delta f) + 20\log(\frac{f_0}{\Delta f}) - 10\log(\frac{P_{DC}}{1mW}). \quad (2\text{-}14)$$

The second FoM_2 can take into account not only FoM_1 but also the tuning range. It still evaluates the $1/f^2$ PN region and can be described by [55]:

$$FoM_2 = -L(\Delta f) + 20\log[(\frac{f_0}{\Delta f})(\frac{TR(\%)}{10})] - 10\log(\frac{P_{DC}}{1mW}) \quad (2\text{-}15)$$

Where *TR* is the tuning range expressed as percentage. The third FoM_3 evaluates oscillator performances in $1/f^3$ PN region. It can be defined as [61]:

$$FoM_3 = -L(\Delta f_m) + 20\log[(\frac{f_0}{f_m^{1.5}})(\frac{TR(\%)}{10})] - 10\log(\frac{P_{DC}}{1mW}) \quad (2\text{-}16)$$

Where f_m is a frequency offset from a carrier, which is usually less than 10 KHz. The four

Table 2-1 A comparison between literature provided in this chapter.

Ref.	Topology	Fig.	Tuning Range [%]	Fre. (GHz)	VDD (V)	Power (mW)	$1/f^3$ PN Corner (KHz)	Tank Quality Factor (Q)	Process (nm)	Phase noise (dBc/Hz)	FoM_1 (dBc/Hz)	FoM_2 (dBc/Hz)	FoM_3 (dBc/Hz) @ 10KHz	FoM_4 (dB)
[48]	Class D	2-7	46	3	0.5	14	800	14	65	-152 @ 10MHz	190	203	≈153	9.7
[37]	Class B	2-8	15	2.9	2	16	100	13	350	-142 @ 3MHz	189	192.5	≈145	10
[57]	Class C	2-9	13	4.9	1	1.4	200	16	130	-130 @ 3MHz	194	196.2	≈144	6.8
[55]	Class F	2-11	25	3.7	1.25	15	300	16	65	-142.2 @ 3MHz	192.2	200.2	NA	8.6
[57]	Class C With K Block	2-12 (b)	10	4.5	1	1.3	200	16	130	-132 @ 3MHz	196	196	≈144	4.8
[58]	Complementary Voltage-Biased	2-13	18.2	3.3	1.2	0.72	NA	10	65	-114 @ 1MHz	186	191.2	≈140	10.8
[56]	Tail Inductor	2-14	27.2	2.85	0.9	6.6	200	10	28	-139.7 @ 3MHz	192	200.7	≈140.8	4.8
[77]	Resistor in Source	2-17	NA	2.2	1.8	18.54	NA	NA	180	-122 @ 1MHz	176	NA	NA	NA
[60]	Modified Tank (Class-D/F_2) Resonating @ ω_0 and $2\omega_0$	2-15	31	3.3	0.5	4.1	60	12	40	-123.4 @ 1MHz	187.6	197.4	≈147.8	10.7
[53]	Modified Class C	2-18 (a)	10	6.09	1.8	2.16	200	10	180	-120 @ 2MHz	189	195.3	≈140	7.8
[50]	Modified Class C	2-18 (b)	28	3.4	1.2	6.6	≈600	13	90	-127 @ 1MHz	191	199.9	NA	8
[52]	Narrowing Conduction Angle (Class C)	2-19 (b)	18.6	2.05	1.2	2.53	32	15	130	-132.46 @ 1MHz	194.7	200	≈154.4	5.6
[58]	Resistor in Drain	2-22	18.2	3.3	1.2	0.72	≈70	10	65	-114 @ 1MHz	186	200.7	≈141.1	10.8
[15]	Modified Tank + Class C +Guiding 2nd Harmonic	2-23	14	27.3	1	12	120	10	28	-106 @ 1MHz	184	187	≈133.7	12.8
[82]	Modified Tank Resonating @ ω_0, $2\omega_0$, $3\omega_0$, and $4\omega_0$	2-24	15.7	14.2	0.55	6.6	550	NA	65	-114.7 @ 1MHz	189.5	193.5	≈130.8	A

FoM_4 is the most important one since it can evaluate oscillator performances without affecting tank quality factor. As mentioned in Section 2-2, (2-8) gives the maximum

FoM_{max} that can be obtained by an oscillator. In FoM_{max}, only the thermal noise of the tank is converted to PN. Now, if we subtract FoM_1 from FoM_{max}, the result evaluates the performance of oscillator core (active elements) without the tank quality factor effect.

Here is an example to clarify this point. Imagine FoM_1 of oscillator number one (OSC_1) is 200 dBc/Hz whereas its FoM_{max} is 250 dBc/Hz. Now, FoM_1 and FoM_{max} of OSC_2 are 190 dBc/Hz and 200 dBc/Hz, respectively. If the tank quality factor is not considered, it seems OSC_1 has a better performance. However, OSC_2 has much better performance given that $FoM_{4,OSC2}$ is less than $FoM_{4,OSC1}$. FoM_4 can be given by [39]:

$$FoM_4 = [176.8 + 20\log_{10} Q] - FoM_1 . \tag{2-17}$$

Note that tuning range should not be considered. As can be seen in Table 2-1, the class C oscillators especially with the *K* block or the narrowing conduction angle have a great performance in $1/f^2$ PN region among the other oscillators since the core transistors do not enter the triode region and it is reflected with the high FoM_1. The class D oscillator has the best FoM_2. The main reason is that it has a very large tuning range, which is not due to a great performance of the oscillator core. For the same reason, the class D has a good FoM_3. However, the modified tank (class-D/F_2) and the narrowing conduction angle have the best FoM_3 that is related to $1/f^3$ PN region.

The primary reason for the modified tank (class-D/F_2) having the greatest $1/f^3$ PN corner frequency is that the tank is modified and resonates at ω_0 and $2\omega_0$. The modified tank, in turn, prevents the tank's energy from becoming unbalanced. Note that the narrowing

conduction angle has a smaller $1/f^3$ PN corner frequency because it is implemented in the bigger technology file. The tail inductor oscillator and class C oscillator with the K block have the best topology without the tank quality factor effect in $1/f^2$ PN region since they have the smaller FoM_4.

To summarize, we conclude a LC-tank oscillator can reach the best performances in $1/f^3$ and $1/f^2$ PN regions if the oscillator is designed in class C with the K block, and uses the techniques of narrowing conduction angle, the tail inductor, and the modified tank simultaneously.

2.5 Conclusion

This chapter provides a comprehensive study of PN mitigation in LC-tank oscillators. Colpitts and cross-coupled oscillators are the two common topologies among LC-tank oscillators. We choose the latter to show its topology evolution with respect to PN performance since it has a better PN performance than the former. To this end, the Hajimiri model is preferred between two accepted phase-noise models for oscillators because it offers designers better insight into the design of a low-phase noise oscillator. With the help of this model, we discuss $1/f^2$ and $1/f^3$ phase noise regions for the different evolved topologies and introduce class B, C, D, and F oscillators. For mitigating $1/f^2$ phase noise region, we present several methods, ranging from rising I_{RF} and V_{RF}, and minimizing $\Gamma_{M,rms}$ and $\Gamma_{T,rms}$. We also analyze $1/f^3$ phase-noise region and a few techniques are suggested to diminish flicker noise up-conversion. These techniques are rising linearity, adding

resistances, controlling the oscillation amplitude, decreasing the conduction angle, guiding the high-frequency harmonics of current, and shifting the phase of V_{GS} against V_{DS}.

Finally, a comparison between literature is presented and it is concluded a LC-tank oscillator can reach the best performances in $1/f^3$ and $1/f^2$ PN regions if the oscillator is designed in class C with the K block, and uses the techniques of narrowing conduction angle, the tail inductor, and the modified tank simultaneously.

Chapter 3 Design and Implementation of A LC-VCO

3.1 Introduction

In this chapter, a cross-coupled circuitry is used as the rudimentary structure. In order to decrease the phase noise, two solutions based on amplitude enlargement are opted. First, a technique to enhance the signal amplitude after the cross-coupled transistors are used to boost the oscillation amplitude. Second, the tail current source is eliminated to improve the phase noise at the output. The phase noise of the proposed oscillator is theoretically analyzed according to Hajimiri's model and verified by simulations. Since the theorical calculation of the phase noise is complicated, all the necessary steps are provided. This chapter is organized as follows. Section 3.2 presents the technique mentioned above. Section 3.3 explains how the proposed oscillator works in detail. schematics also are demonstrated in Section 3.3. The large signal analysis is done in Section 3.4, which provides the oscillation amplitude. A closed-form formula of the phase noise of the proposed oscillator is derived in Section 3.5. The simulations and verifications of the theorical calculations are placed in Section 3.6. The conclusion is in Section 3.7.

3.2 Proposed Architecture

Figure 3.1 (a) presents a cross-coupled structure in which the phase noise is relatively high due to mainly three reasons. First, the switching transistors spend more time in the triode region than the active region. Second, the tail current source gives rise to 1/f noise up-conversion. Third, the direct injection of the noise from the switching transistors into the tank.

The main idea of this chapter arises from Figure 3.1 (b) with a K-block above the cross-coupled transistors so that their phase noise can be re-circulated before injecting to the tank. Supposing that the noise converted to phase noise of the mentioned block is relatively low contributed to the output phase noise, proven in Section 3.5, it can be stated that the noise circulations as well as the oscillation amplitude enlargement are the benefits of this block. In addition, the 1/f noise up-conversion can be suppressed by omitting the tail current source. Figure 3.1 (c) presents the exact idea mentioned above. Note that, without the K-block since the tail current source is eliminated in Figure 3.1 (c), the transistor currents strongly depend on VDD. However, the K-block distinguishes the cross-coupled transistors from VDD.

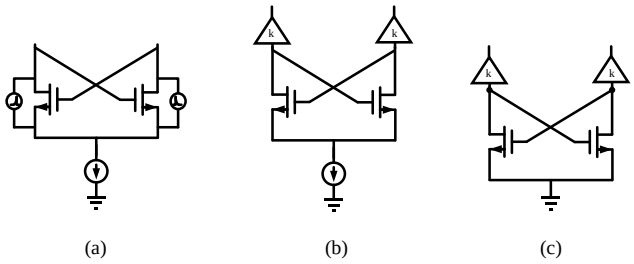


Figure 3-1cross-coupled structure (a) with its noise sources (b) with k-blocks (c) without tail current source.

Figure 3.2 presents the schematic of the proposed oscillator. M_1 and M_2 are switching transistors. The amplifying stage, K-block, is replaced with M_3, M_4, M_5, M_6, C_1 and C_2. The circuit current is determined with M_1 and M_2 while their drain voltage is fixed with M_5 and M_6. So, the circuit current is controllable. V_b is provided by an external supply voltage.

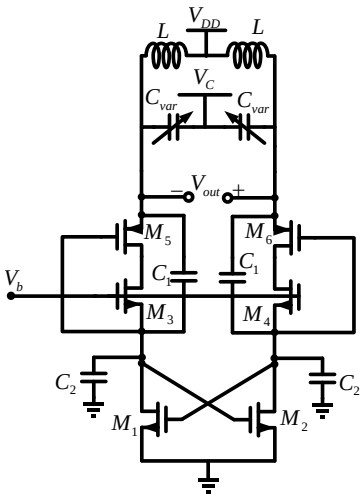


Figure 3-2 The proposed oscillator.

3.3 Suggested Circuitry

3.3.1 K-Block

Figure 3.3 prepares a precise presentation of the K-block. C_1, C_2 and assisting transistors (M_3 and M_5) can reduce the phase noise while increasing the swing level of the output voltage. The signal first meets the node M of the switching transistor. As shown in Figure 3.3, three paths of active and passive elements are now encountered. Active signal paths through M_3 (Common-Gate) and M_5 (Common-Drain) are a couple of those. The mentioned transistors are in their linear region; thus, signal amplification without any change in the phase is expected. Also, there will be no gain roll-off in the signal path. The third path is through C_1 which prepares a direct way to the node *M*. Finally, the estimated output signal would be the summation of three signals with the same phase, resulting in an amplified output swing. Meanwhile, the large capacitance of C_2 will lead to a better filtering behavior in the circuit, but the oscillation frequency will be decreased. On the other hand, C_2 is not

a good noise circulated if it has a small value. Therefore, its value is a challenge and should be optimized. The role of C_1 in the circuit is re-circulating the injected noise of M_3 and M_5. Thus, the K-block can be considered low phase noise due to the enhanced final output and the added noise circulations (C_1 and C_2). Later, in Section 3.6.1 the optimized sizes of C_1 and C_2 are obtained based on the closed-form formula of the phase noise in Section 3.5.6.

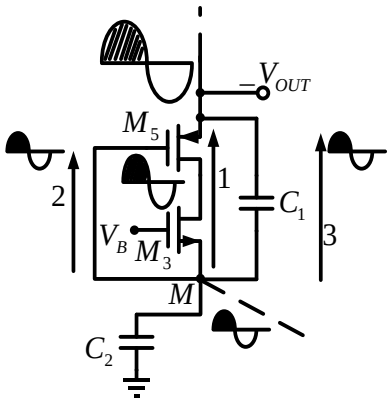


Figure 3-3 The K-block circuitry.

In another analysis, it might be safe to say that the current noise of transistors will create the maximum phase noise when the output voltage cross zero [13], [37]. On the other hand, the K-block operates as an amplifier in this region and intensify the signal amplitude. It means closing the signal angle to degree 90 around zero crossing region as illustrated in Figure 3.4. Furthermore, it can be stated that the swing enhancement in the same current will improve the phase noise behavior.

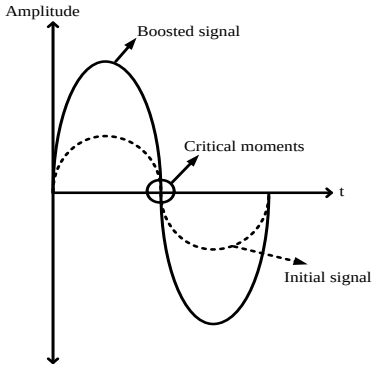


Figure 3-4 A comparison between initial and boosted signal.

3.4 Large Signal Analysis

3.4.1. Bias Circuitry Properties

In Figure 3.5, the bias current of M_1 or M_2 can be presented as (3-1) due to the symmetry of the elements:

$$I_B = K(V_{gs2} - V_{TH})^2 \quad , \tag{3-1}$$

Where K=0.5$\mu_n C_{ox} W_{M2}/L_{M2}$ (μ_n being the electron mobility, C_{ox} the gate oxide capacitance per unit area, and W_{M2} and L_{M2} the transistor width and length) and $V_b > 2V_{TH}$. In 0.18 um CMOS technology, V_{TH}≈0.55V, V_b goes to more than 1.1V; so, we choose 1.3V for V_b.

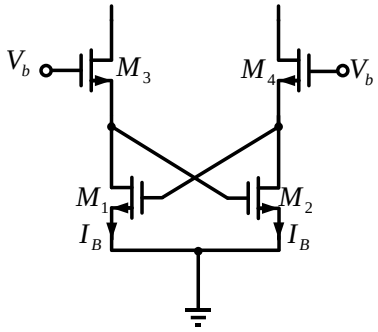


Figure 3-5 Intended bias circuitry.

3.4.2 Output Voltage Swing

In order to find the output voltage of the tank in Figure 3.2, the large signal trans-conductance must be calculated [83], [84]:

$$G_m = I_1 / V_{gs} \,. \tag{3-2}$$

In (3-2), I_1 is amplitude of the first harmonic of drain current and V_{gs} is the gate-source voltage of the transistor. Accordingly, I_1 can be approximated as [37]

$$I_1 \approx 2I_B \,. \tag{3-3}$$

Substituting (3-3) in (3-2),

$$G_m = 2I_B / V_{gs} \,. \tag{3-4}$$

In the next step, the large signal model (half-circuit model) is predicted in Figure 3.6. I_1, C_{in}, R_{in}, C_{var}, R_{tank}, and L are the amplitude of the first harmonic of drain current, the capacitance shown in Figure 3.7, the impedance seen via the tank, the varactor of the tank, the series resistance of output inductance and the output inductance, respectively.

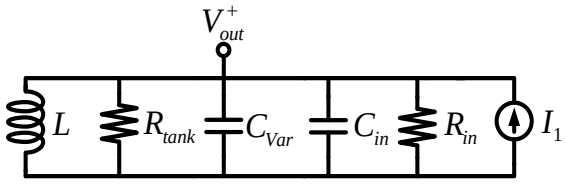


Figure 3-6 Equivalent large signal model to find resonance amplitude signal.

C_{in} can be found from Figure 3.7. Where $C_{1,T}$ and $C_{2,T}$ are as follows

$$C_{2,T} = C_2 + C_{gs1} \,, \tag{3-5}$$

$$C_{1,T} = C_1 + C_{gs6} \,, \tag{3-6}$$

C_{gs1} and C_{gs6} are negligible compared to C_1 and C_2. Thus (3-5) and (3-6) roughly can be simplified as

$$C_{2,T} \approx C_2 , \tag{3-7}$$

$$C_{1,T} \approx C_1 , \tag{3-8}$$

Eventually, C_{in} can be presented as

$$C_{in} = C_1 / (C_1 + C_2), \tag{3-9}$$

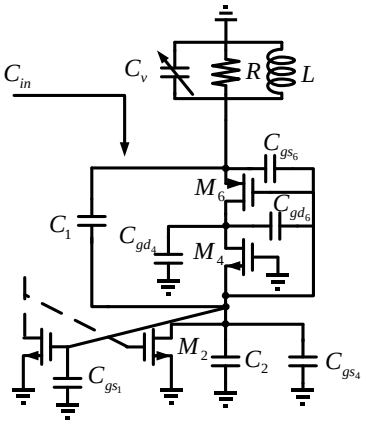


Figure 3-7 A circuit showing how to find C_{in}.

In the next step, Figure 3-8 is used to find R_{in} [37], Where Z_1 roles as an equivalent impedance at the source node of M_6. Considering Figure 3-8, i_1 is approximately closed to zero and R_x can be shown as:

$$R_x = [(1/\ j\omega C_{gd4}) \ + \ (1/\ j\omega C_{gd6} \| \ r_{o4})] / (1 + [G_{m4}(1/\ j\omega C_{gd6} \| \ r_{o4})]). \tag{3-10}$$

For $ro4 \approx \infty$ (3-10) is simplified to (3-11)

$$R_x = [(1/\ j\omega C_{gd4}) \ + \ (1/\ j\omega C_{gd6})] / [G_{m4}(1/\ j\omega C_{gd6})]. \tag{3-11}$$

Obviously, C_{gd4} and C_{gd6} and R_x can be simplified to

$$R_x \approx 2/G_{m4}. \tag{3-12}$$

So, R_{in} can be found as below [85], [37]:

$$R_{in} = R_x / n^2. \tag{3-13}$$

Where n is $C_1=(C_1 + C_2)$ V^+_{out} can be calculated:

$$V_{out}^{+} = I_1[R_{tank} \| 2/\left(n^2 G_{m4}\right)]. \tag{3-14}$$

G_{m4} can be replaced by $I_1/(nV^+_{out})$, then (3-14) results in

$$V_{out}^{+} = I_1 R_{tank}[1-(n/2)]. \tag{3-15}$$

Finally, in the differential mode, the output signal amplitude can be shown as below

$$V_{out} = V_{out}^{+} - V_{out}^{-} = 4I_B R_{tank}[1-(n/2)]. \tag{3-16}$$

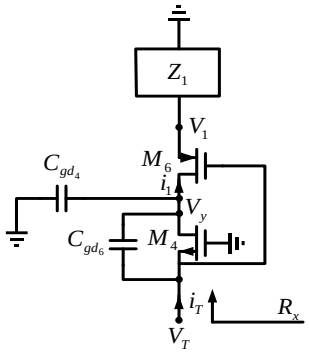


Figure 3-8 Suitable model to find R_x.

Table 3-1 is provided in order to compare some of the presented output amplitude with (3-16). In [86], the output oscillation amplitudes of cross-coupled and double switch (DS) VCO were shown. The related structures are shown in Figure 3-9. It is obvious that both structures have a lower output oscillation amplitude compared to the proposed VCO. Given that in the mentioned structures C_1 and C_2 are not used, factor n does not appear in their

output oscillation amplitudes. As the noise of switching transistors is directly injected into the tank, both structures approximately have high phase noise.

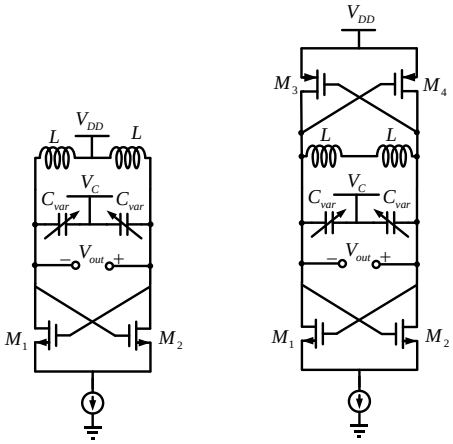


Figure 3-9 Schematic of (a) cross-coupled, and (b) double switch (DS) VCOs.

In [37], [87], and [88], the output oscillation amplitudes of Colpitts, *gm* -boosted differential gate-to-source (G-S) feedback Colpitts, and *gm* -boosted differential drain to-source (D-S) feedback Colpitts were calculated, respectively. The three structures are shown in Figure 3-10. Taking a quick look at the presented equations, it can be easily figured out that the output oscillation amplitude of the proposed oscillator is higher than three mentioned oscillators. The simulation coming in the next part shows that a voltage swing improvement of at least 25% is gained compared to that of the three oscillators with the same current and n=0.5.

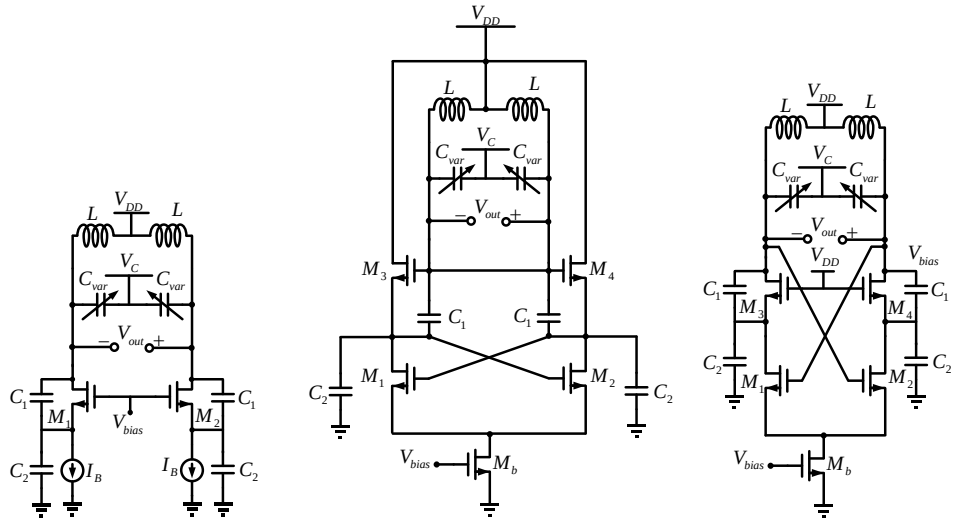


Figure 3-10 Schematic of (a) Colpitts, (b) *gm* -boosted gate-to-source (G-S) Colpitts, and (c) *gm* -boosted drain-to-source (D-S) Colpitts oscillators.

Table 3-1 The comparison of output oscillation amplitude VCOs with the proposed oscillator

Reference	Name	Output Oscillation Amplitude
[86]	Cross-coupled	$(2/\pi)R_BI_B$
[86]	DS-VCO	$(4/\pi)R_BI_B$
[37]	Colpitts	$4I_BR_{tank}$ (1-n)
[87]	G_m-Boosted Differential G-S	$4I_BR_{tank}$ n
[88]	G_m-Boosted Differential D-S	$4I_BR_{tank}$ (1-n)
This Work	Proposed VCO	$4I_BR_{tank}$ [1-(n/2)]

3.5 Phase Noise Analysis in The Proposed Oscillator

3.5.1 Oscillation Amplitude

To derive analytically the phase noise in a LC oscillator, the oscillation amplitude in a large signal analysis should be first calculated. This is rigorously done in Section 3.4.

3.5.2 Effective ISF

Based on Hajimiri's theory, the phase noise $L(\Delta\omega)$ at an offset frequency $\Delta\omega$ from the carrier induced by a white current noise source i_n^2 in a harmonic oscillator is given by [13], [37], and [57],

$$L(\Delta\omega) = 10\log\left(\frac{\Gamma_{rms}^2}{q_{\max}^2}\cdot\frac{\frac{\overline{i_n^2}}{\Delta f}}{2\Delta\omega^2}\right), \tag{3-17}$$

Where q_{max} is the maximum charge swing across the tank capacitance, $i_n^2/\Delta f$ is the white current noise power spectral density, Γ^2_{rms} is effective ISF. (3-17) can be simplified by,

$$\Gamma_{rms}^2\frac{\overline{i_n^2}}{\Delta f} = \frac{1}{2\pi}\int_0^{2\pi}\Gamma^2(\varphi)\frac{\overline{i_n^2}(\phi)}{\Delta f}d\phi\,. \tag{3-18}$$

Therefore, (3-17) can be written,

$$L(\Delta\omega) = 10\log\left(\frac{\sum_i N_{L,i}}{2\Delta\omega^2 C^2 V^2}\right), \tag{3-19}$$

Where $N_{L,i}$ is

$$N_i = \frac{1}{T}\int_0^{T}\Gamma_i^2(t)\overline{i_{n,i}^2}(t)dt. \tag{3-20}$$

In (3-20), T_o is the oscillation period and i is the *ith* device. $i_{n,i}^2(t)$ can be either stationary or cyclo-stationary.

3.5.3 Tank Effective ISF

If the voltage across the tank is $Acos(\omega t)$, the tank ISF corresponding to its current noise source, presented in Figure 3-11, is a sinusoid in quadrature with the tank voltage, which its magnitude is inversely proportional to the number of the resonators (N) in the oscillator [89], [90]. Therefore, it can be given by

$$\Gamma_{\tan k} = \frac{-1}{N}\sin(\omega_\circ t) = \Gamma_R . \tag{3-21}$$

The square rms value of Γ_R is

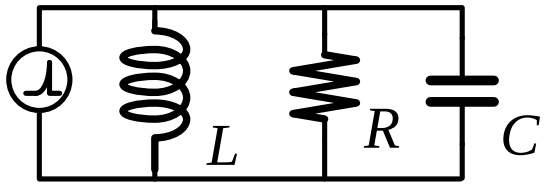


Figure 3-11 The tank circuitry to calculate its ISF.

$$\Gamma_{R,rms}^2 = \frac{1}{2}\int_{-\pi}^{\pi}\Gamma_R^2(\phi)\,d\phi = \frac{1}{2N^2}\ , \tag{3-22}$$

Where the angle $0 \le \varphi \le 2\pi$ is employed rather than $\omega_0 t$. Note that N is one for single-ended oscillators and two for the differential oscillators.

3.5.4 Effective ISFs of Transistors

Since the proposed oscillator only works in the differential mode and in order to simplify the calculations in the effective ISFs for the active devices, the half circuit, represented in

Figure 3-12, is considered. Besides, the transistor ISFs are related to the tank ISF to make the calculation easy as well.

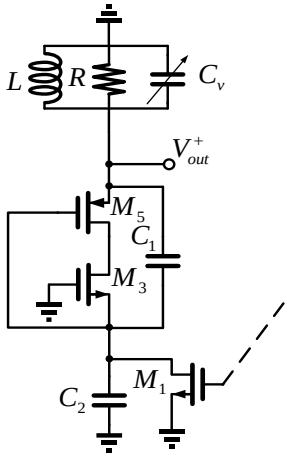


Figure 3-12 The half circuit of the proposed oscillator.

The ISF for M_5, Γ_{M5}, can be calculated by utilizing Figure 3-13. A current impulse is injected between the drain and source nodes of M_5 as shown in Figure 3-13. It is obvious to say that the applied current impulse just influences C_1 and its voltage changes. As a result, the voltage across C_1 is yielded as

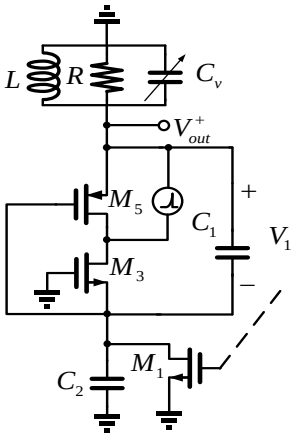


Figure 3-13 Proposed the suitable half circuit to calculate Γ_{M5}.

$$\Delta V_1 = (1-n)\Delta V_{out} \ . \tag{3-23}$$

$$n = \frac{C_1}{C_1 + C_2}, (1-n) = \frac{C_2}{C_1 + C_2} \ . \tag{3-24}$$

The voltage changes across the tank capacitance lead to the tank ISF. This means,

$$\Delta V_{out}^{+} \rightarrow \Gamma_R^{+} \ . \tag{3-25}$$

Thus, the voltage changes across C_1 results in

$$\Delta V_1 \rightarrow \Gamma_{M_5} \ . \tag{3-26}$$

Γ_{M5} can be written as

$$\Gamma_{M_5} = (1-n)\frac{-\sin(\omega_o t)}{N} \ . \tag{3-27}$$

Γ_{M3} is the same as Γ_{M5} since M_5 and M_3 are series.

$$\Gamma_{M_3} = (1-n)\frac{-\sin(\omega_o t)}{N} \ . \tag{3-28}$$

Figure 3-14 is used to study the ISF of M_1, Γ_{M1}. A current impulse is applied to the node a in Figure 3-14. V_a can be associated to V_{out}^{+} as

$$V_a = nV_{out}^{+} \ . \tag{3-29}$$

Consequently, Γ_{M1} is

$$\Gamma_{M_1} = n\Gamma_R = n\frac{-\sin(\omega_o t)}{N} \ . \tag{3-30}$$

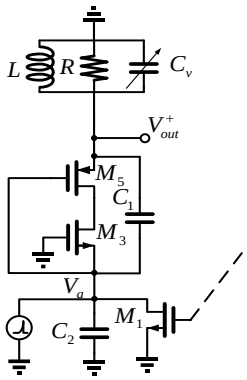


Figure 3-14 The suitable half circuit to calculate Γ_{M1}.

3.5.5 Noise Modulating Function (NMF)

As transistors have a cyclostationary noise, their noise modulating functions must be calculated. The drain noise current power of NMOS transistor can be expressed as follows

$$\frac{\Delta \bar{i_n^2}}{\Delta f}(\omega_\circ t) = 4KT\gamma g_m(\omega_\circ t) = 4KT\gamma \frac{\partial id(\omega_\circ t)}{\partial V_{gs}(\omega_\circ t)}, \tag{3-31}$$

Where K is Boltzmann's constant, T is the absolute temperature, ω_0 is the oscillation frequency, g_m is the transistor transconductance, and γ is the channel noise factor, which is commonly 2/3 in long -channel transistors. Because the drain current is periodic, it can be expressed with its Fourier series as

$$id(\omega_\circ t) = \sum_{i=\circ}^{\infty} I_{i,d} \cos(i\omega_\circ t + \phi_p)\,. \tag{3-32}$$

$g(\omega_0 t)$ in (3-31) can be rewritten as

$$g(\omega_\circ t) = \frac{\partial id(\omega_\circ t)}{\partial Vgs(\omega_\circ t)} = \frac{\dfrac{\partial id(\omega_\circ t)}{\partial t}}{\dfrac{\partial V_{gs}(\omega_\circ t)}{\partial t}}\,. \tag{3-33}$$

Besides, since the tank *Q* is moderately high, the voltage nodes in an LC oscillator is nearly sinusoidal. Consequently, V_{sg5} can be written as

$$Vsg_5 = V_{dc} + A(1+n)\cos(\omega_\circ t)\ , \tag{3-34}$$

Where V_{g5} is $-nA$ [37]. Upon substituting (3-32) and (3-34) in (3-31), the drain noise current can be obtained as

$$\frac{\Delta \bar{i_n^2}}{\Delta f}(\omega_\circ t) = 4KT\gamma \frac{-i\omega_\circ \sum_{i=\circ}^{\infty} I_{i,out}\sin(i\omega_\circ t + \phi p)}{-A(1+n)\omega_\circ \sin(\omega_\circ t)}\ . \tag{3-35}$$

Using (3-20), (3-27), and (3-35), as well as supposed φ_P is zero and $\omega_0 t$ is φ, N_{M5} is

$$N_{M_5} = 4KT\gamma \frac{1}{2\pi}\int_\circ^{2\pi} \frac{\sum_{i=\circ}^{\infty} iI_{i,d}\sin(i\omega_\circ t)}{A(1+n)\sin(\omega_\circ t)}\left(\frac{(1-n)^2}{N^2}\sin^2(\omega_\circ t)\right) d\omega_\circ t\ . \tag{3-36}$$

$$N_{M_5} = \frac{2KT(1-n)^2}{\pi AN^2(1+n)}\int_\circ^{2\pi}\left(\sum_{i=\circ}^{\infty} i \quad I_{i,d}\sin(\phi)\right)\sin(\phi)d\phi. \tag{3-37}$$

Note that the tank filters out the higher harmonics except for the first harmonic, therefore

$$N_{M_5} = \frac{2KT(1-n)^2 I_{1,d}}{N^2 A(1+n)}\int_\circ^{2\pi}\sin^2(\phi)d\phi\ . \tag{3-38}$$

$$N_{M_5} = \frac{(2KT\gamma)}{N^2}\frac{(1-n)^2}{(1+n)}\left(\frac{I_{1,d}}{A}\right). \tag{3-39}$$

With a good approximation, $I_{1,d}/A$ is $1/R_{tank}$. Remember *N* is 2 since there are two resonators in the proposed oscillator.

$$N_{M5} = \frac{KT\gamma}{2}\frac{(1-n)^2}{(1+n)}\frac{1}{R_{\text{tank}}} . \quad (3\text{-}40)$$

In the same manner, N_{M3} and N_{M1} can be obtained as

$$N_{M3} = \frac{KT\gamma}{2}\frac{(1-n)^2}{n}\frac{1}{R_{\text{tank}}} . \quad (3\text{-}41)$$

$$N_{M1} = \frac{KT\gamma}{2} n \frac{1}{R_{\text{tank}}} . \quad (3\text{-}42)$$

Also, the noise of tank resistance is stationary and $N_{R,tank}$ using (3-22) is yield as

$$N_{R\tan k} = \frac{K_B T}{2}\frac{1}{R_{\text{tank}}} . \quad (3\text{-}43)$$

3.5.6 Phase Noise

Replacing (3-43), (3-42), (3-41), (3-40), and (3-15) into (3-19), phase noise is obtained as

$$L(\Delta\omega) = 10\log\left(\frac{K_B T}{4\Delta\omega^2 C^2 I_B^2 R_{\text{tank}}^3}\left(\frac{1}{(2-n)^2} + \frac{\gamma n}{(2-n)^2} + \frac{\gamma(1-n)^2}{n(2-n)^2} + \frac{\gamma(1-n)^2}{(2-n)^2(1+n)}\right)\right) .$$

(3-44)

Where in (3-44) supposed $\gamma_p \approx \gamma_n \approx \gamma$ and C is

$$C = C_v + \frac{C_1}{C_1 + C_2} . \quad (3\text{-}45)$$

In order to size C_1 and C_2 optimally, we take advantage of (3-44). When n is 0.46, 4 terms in the parenthesises, which are related to n in (3-44), have a minimum. This value of n plus the mentioned technique in Section 3.6.1 as filtering behavior of K-block help us obtain the optimal values of C_1 and C_2.

3.6 Simulation and Post Layout Simulations

The proposed oscillator is designed in 0.18 um TSMC CMOS technology with 1.8 V power supply. Figure 3-15 shows the simulation of the output voltage swing in which the output signal peak to peak is about 4.1 V, the center frequency is 2.4 GHz, the tank quality factor is 8 and the output current is 1.3mA. The simulated and theoretically derived phase noise is demonstrated in Figure 3-16. The derived phase noise is compared with the simulated one in Figure 3-16 representing a good accuracy between them so that the differences between them are less than 3 dB over the offset frequencies. As demonstrated, the simulated phase noises at the offset frequency of 1MHz and 3MHz are -127.2 dBc/Hz and -138 dBc/Hz, respectively, as well as the $1/f^3$ phase noise corner is only around 10 KHz. Also, Figure 3-17 shows the layout schematic of the proposed circuit. The core area is 0.41 mm^2.

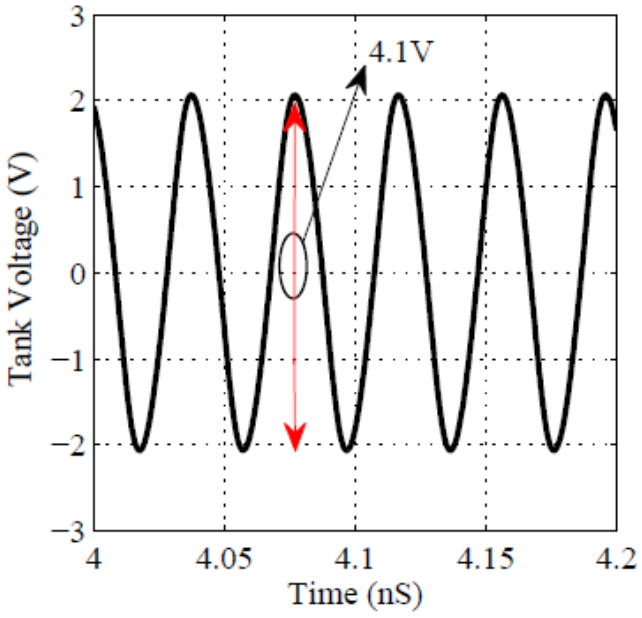


Figure 3-15 The simulation result of the oscillation amplitude.

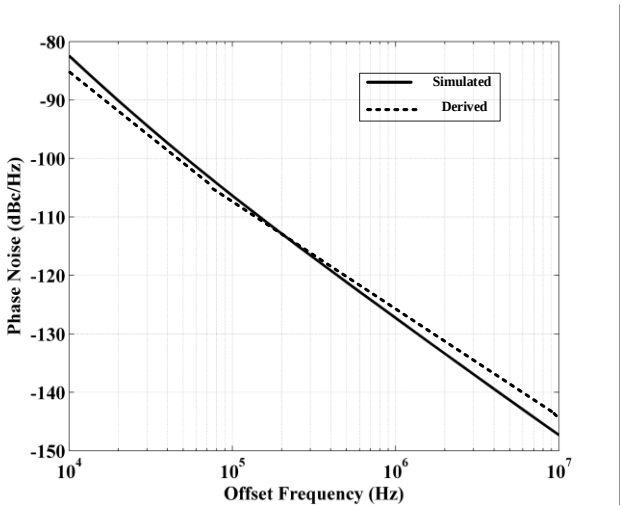


Figure 3-16 The simulated and derived phase noise

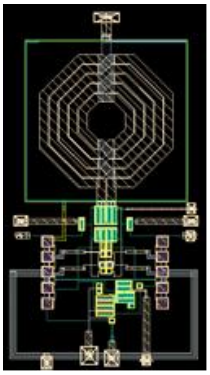


Figure 3-17 The layout schematic of the proposed oscillator.

A comparison among the state-of-the-art published CMOS-based oscillators with the proposed oscillator is provided in Table 3-2. Also, a figure-of-merit (FoM) is considered as [22]

$$FoM = 20log(\frac{f_0}{\Delta f}) - 10log(\frac{P_{DC}}{1mW}) + L(\Delta f\ ). \quad (3\text{-}46)$$

Where f_o is the resonance frequency, Δf is the offset frequency, P_{DC} is the power dissipation and $L(\Delta f)$ is the phase noise (dBc/Hz). Although the comparisons are presented in this table are the measurement results, the amplitude results have been obtained from simulation. It should be mentioned that the reported results of [38] is obtained from simulation using 1.8V power supply.

Table 3-2 Comparison of the proposed oscillator with the published state-of-the-art counterparts.

References	[88]	[54]	[91]	[53]	This Work
[1]TR (GHz)	1.76–1.93	4.74-4.85	6.09-7.5	2.05-2.47	2.3-2.5
Frequency (GHz)	1.84	4.84	6.09	2.05	2.4
Supply (V)	0.9	1.2	1.8	1.2	1.8
P_{DC} (mW)	1.35	3.4	2.16	2.53	2.16
PN (dBc/Hz)	-126@1MHz	-125@1MHz	-120@2MHz	-111@100KHz	127.2@1MHz -138@3MHz
FoM (dBc/Hz)	-190@1MHz	-193@1MHz	-189@2MHz	193.3@100KHz	191.5@1MHz 192.7@3MHz
$1/f^3$ PN Corner (KHz)	NA	N.A.	200	32	10
Amplitude (V)	≈2.6**	≈2.5*	0.9*	1.6*	4.1*

[2]TQF (Q)	N.A.	N.A.	10	15	8
Process (nm)	180nm	180nm	180nm	130nm	180nm

Simulation* simulation and with 1.8 V power supply** [1]Tuning Range [2]Tank Quality Factor

To verify that the proposed oscillator is promising through PVT variations, Table 3-3 is provided to show the post-layout simulation results. It is clear that FoM of the proposed oscillator remain relatively constant throughout the PVT variations.

Table 3-3 PVT variations in the proposed VCO.

	Frequency [GHz]	Current [mA]	Phase Noise [dBc/Hz]	FOM [dBc/Hz]
TT [27*oC*]	2.4	1.3	-127.2@1MHz	-191.5
FF [-40*oC*]	2.5	1.3	-126.2@1MHz	-190.45
SS [125*oC*]	2.1	1.2	-123.4@1MHz	-186.5

3.6.1 Phase Noise and Filtering Behavior Of K-block

To clarify the K-block role in the phase noise improvement, a phase noise simulation in the same frequency and current was done with K-block and without it. Figure 3-18, demonstrating this simulation, shows around 7 dBc/Hz improvement in the phase noise while K-block is present.

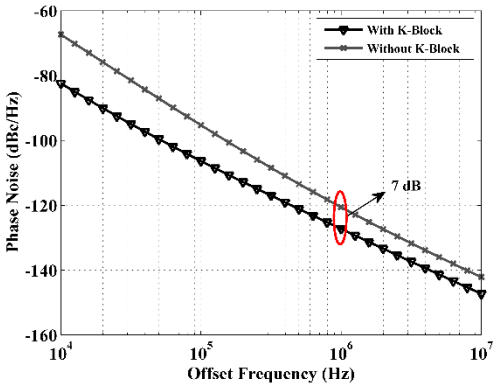


Figure 3-18 Phase noise behavior comparison with and without k-block.

The reason why this improvement occurs may be related to the filtering behavior of K-block. A simulation to check out the mentioned filtering effect is of great interest. Figure 3-19 demonstrates the output of the circuit in the frequency domain with and without K-block. Again, as the previous simulation, the currents are the same in both cases. Figure 3-19 can satisfy the beneficial filtering behavior of K-block which clearly can improve the phase noise.

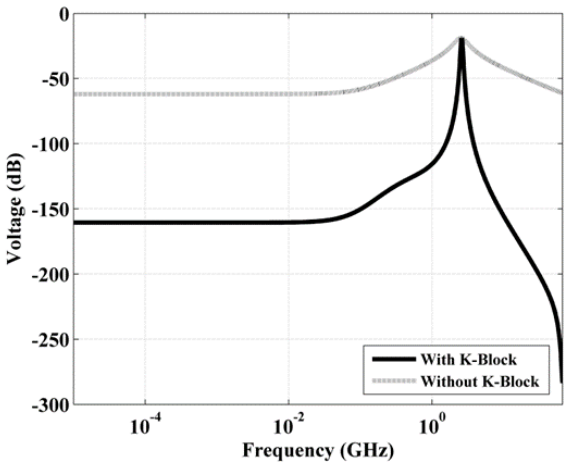
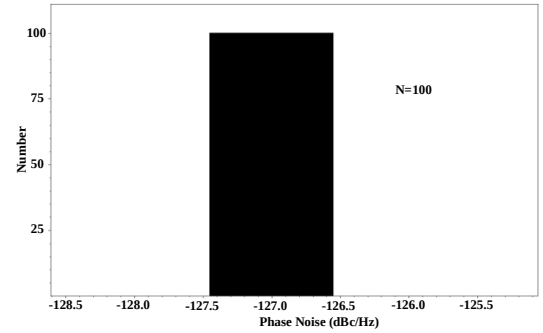


Figure 3-19 Frequency response comparison with and without k-block.

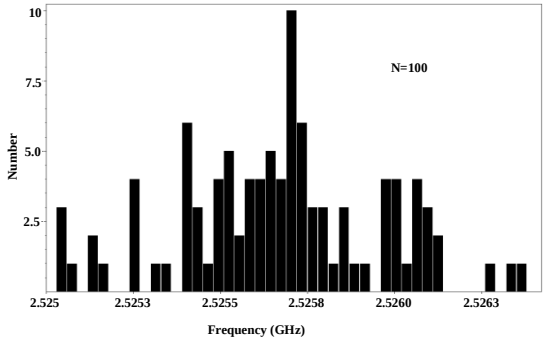
Also, the values of C_1 and C_2 are selected using the frequency response chart and the optimal *n* in Section 3.5.6, so that the best filtering behavior achieved. Clearly, the ratio of C_1 and C_2 and the sum of them will affect the oscillating amplitude and frequency, respectively. So, maximizing the oscillation amplitude as well as making the filtering behavior narrower, can improve the phase noise definitely. Therefore, the optimized sizes of C_1 and C_2 are selected as 270 PF and 305 PF, respectively.

3.6.2 Monte Carlo Simulation Result

The transistors W, L and also process variation were examined taking advantage of Monte Carlo simulation. The results show that the proposed oscillator is very promising and confirm the performance of the circuit. In 100 times of simulation, the phase noise variation is less than 1 dBc/Hz, and the frequency variation is less than 290 KHz over the center frequency of 2.5GHz. Figure 3-20 depicts the mentioned simulation results.



(a)



(b)

Figure 3-20 Monte Carlo simulation results (a) Phase noise (b) frequency variation.

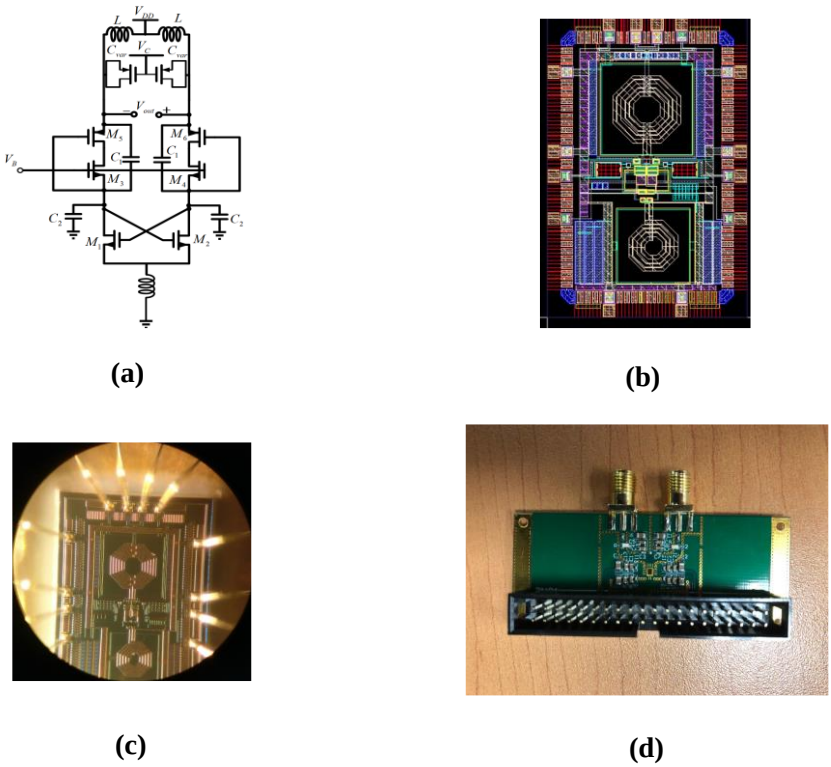
3.7 Measurement Results

The VCO has been fabricated in a 180 nm CMOS technology with 1.8 V nominal voltage supply. The complete schematic, layout, fabricated layout, and PCB of the proposed VCO are shown in Figure 3-21. The core transistors M_1 and M_2 have been sized with $(W/L)_{1\text{-}2}$ $20\mu m/0.18\mu m$. The transistors M_3 and M_4 act as an amplifier for the drain signals of M_1 and M_2. Note that the transistors M_3 and M_4 can be simply biased in the active region through V_b. As such, their W/L can be sized largely to suppress phase noise induced by their flicker noise whereas their white noise is recirculated by means of C_1 and not be injected into the

tank. Remember that their *W/L* should not be significantly large to force transistors M_1 and M_2 to enter the triode region as well. The $(W/L)_{3\text{-}4}$ is $50\mu m/0.18\mu m$.

M_5 and M_6 shield the current of M_1 and M_2 from changes of power supply through the feedback of the gates of M_5 and M_6 to the drains of M_1 and M_2. Moreover, electron mobility in a channel of NMOS (u_n) is two times of electron mobility in a channel of PMOS (u_p). This means that $(W/L)_{5\text{-}6}$ should be doubled than $(W/L)_{3\text{-}4}$ since M_5 and M_6 are series with M_3 and M_4. Otherwise, M_5 and M_6 will not work properly. The $(W/L)_{5\text{-}6}$ is $100\mu m/0.18\mu m$.

The tank and tail inductances were set equal to L_{tank} = 3.75 nH and L_{tail} = 1.9 nH. C_1 and C_2 are selected as 270 PF and 305 PF. A discrete tuning scheme employing 63 MIM-based capacitance cells allows to vary the oscillation frequency between 2.3 to 2.5 GHz. The measured quality factor *Q* is about 8 at 2.5 GHz.



(a) **(b)**

(c) **(d)**

Figure 3-21 The proposed VCO (a) schematic (b) layout (c) fabricated layout (d) PCB.

3.8 Conclusion

In this chapter a basic idea of how to improve the phase noise in a conventional cross-coupled oscillator is presented by adding a K-block. The dominant feature of this new structure is the improvement in output voltage swing compared to the state-of-the-art published counterparts. This improvement is achieved through intensifying the output oscillation amplitude without increasing the circuit current and power as well.

Besides, a comprehensive analytical phase noise study of the proposed oscillator is presented in this chapter too. To derive a closed-form formula of the phase noise in the $1/f^2$ region by Hajimiri's phase noise theory, the large signal oscillation amplitude is first

provided, which can be used to prove the voltage swing enhancement too, and then the effective ISFs of the tank and transistors are calculated. Since the transistors have a cyclostationary noise, the noise modulating function is derived for them as well. The simulation of the phase noise shows it has a good precision between the simulation and the derived one. The phase error between the simulated phase noise and the calculated one indicates less than 3 dB errors over the offset frequencies.

The post-layout simulation in 0.18 um CMOS technology with oscillation frequency of 2.4 GHz shows the phase noise at the offset frequency of 1 MHz is -127.2 dBc/Hz with the power supply of 1.8 V and total current of 1.2 mA while the tank quality factor is only 8. Based on the mentioned results and the Monte Carlo simulation, the proposed idea shows a promising and improved performance compared to the other works published recently.

Chapter 4 Design of Fractional Frequency Synthesizer

4.1 Introduction

In this chapter, we have designed the frequency synthesizer for IEEE 802.11a/b, Bluetooth, U-NII, and HIPERLAN with the 5G requirements. On the other hand, the approaches provided in this chapter can be easily applied to other wireless communication standards as well.

The basic block diagram for a frequency synthesizer is shown in Figure 4-1. Both fractional-N and integer-N frequency synthesizer architectures can cover the frequency ranges needed for these wireless communication standards. Although integer-N architecture is fairly easy to be designed, it has some fundamental shortcomings that make it unsuitable for this purpose. For example, it has a high-division ratio. Moreover, the output channel spacing is equal to the reference frequency that limits the loop bandwidth, causing weak VCO phase noise suppression. On the contrary, in fractional-N architecture the forementioned constraints can be mitigated since there is a fractional relation between the channel spacing and the reference frequency [92]. This is why we adopted a fractional-N architecture. In order to improve the lock time, a divide-by-2/3 circuit is exerted before the programmable digital counter [93], [94]. Although a delta–sigma modulation-based fractional-N frequency synthesizer has a higher frequency resolution, this approach is not suitable for low-power applications [6], [95]. Therefore, it is not used in this chapter.

Three frequency synthesizers are designed to cover 3 different wireless communication standards. The first communication standard is based on IEEE 802.11b and Bluetooth, which creates 14 carrier frequencies with 5 MHz channel bandwidth in band of 2.4 to 2.48 GHz. The seven channels of this standard embrace the HIPERLAN standard as well. The second communication standard builds on the U-NII standard, which produces 8 carrier frequencies with 25 MHz channel bandwidth in band of 5.15 to 5.35 GHz. The third communication standard draws on IEEE 802.11a standard, which has 32 carriers with 20 MHz channel bandwidth over the frequencies of 5.15 to 5.8 GHz.

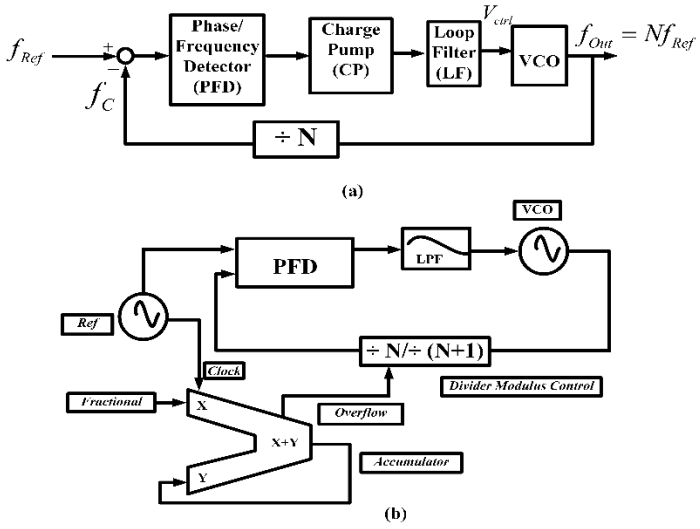


Figure 4-1 A conventional block of a) a phase-locked loop frequency synthesizer b) a fractional-N frequency synthesizer.

The rest of this chapter presents the design and simulated building blocks of the frequency synthesizer. Section 4.2 reveals the design and simulation of a phase frequency detector (PFD) by implementing a new PDF and overcoming the dead region issue. Section

4.3 is dedicated to the design and simulation of the programmable frequency divider. In this Section we provide the circuit level design of the programmable frequency divider. Section 4.4 illustrates the design and simulation of a voltage-controlled oscillator (VCO). Section 4.5 discusses the design and simulation of a charge pump and loop filter. Section 4.6 shows the simulation of the whole designed frequency synthesizer. Section 4.7 gives a conclusion of this chapter.

4.2 Phase frequency detector (PFD)

Figure 4-2 illustrates a logical implementation of the PDF [92]. The detector consists of two edge-trigged resettable D flipflops with D inputs tied to V_{DD}. *Ref* and *Div* act as clock inputs of those D flipflops, and the NAND gate resets the flipflops if *Ref* and *Div* equivalent to 1. A major problem of the PFD is the dead region. The dead region is due to the delay of the reset path of the NAND gate and D flipflops that can cause problems in the frequency synthesizer.

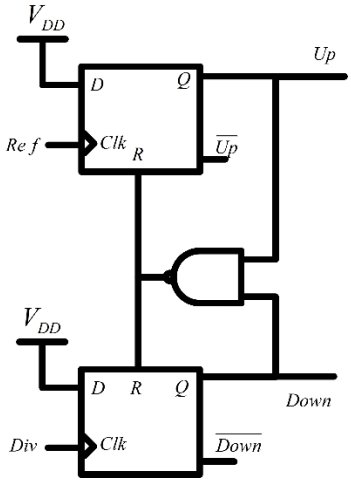


Figure 4-2 PDF implementation.

Since edge-trigged flipflops are widely used in the PFD and frequency divider, these flipflops are designed before the PFD is designed. Each resettable D flipflop can be implemented with two latches with positive feedbacks (these latches are placed as back-to-back), as shown in Figure 4-3.

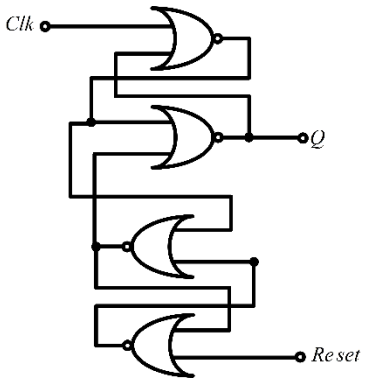


Figure 4-3 Logical implementation of a resettable D flipflop [92].

At high frequencies the latches are implemented in the current mode logic (CML), which consists of a differential pair and regenerative transistors in order to produce positive feedback [96], [97]. These configurations are used in divide-by 2 circuits up to 40-GHz frequencies [98]. If the current of these transistors is not specified, the output swing will be unpredictable. Also, high-speed D flipflops are implemented in source-coupled logic (SCL) with 18 transistors [99]. In SCLs, the value of the output swing is limited by the fact that transistors are stacked. Therefore, the *W/L* ratio of the transistors cannot be minimized and SCL circuits have a high input and output capacitance. Besides, the traces between the transistors in a layout are long so that the parasitic capacitances can be greater than the

input capacitances. Because of this, a buffer is used when VCO is connected to the dividers constructed by SCL, which increases the power consumptions [100].

Both the CML and the SCL flipflops are affected by high capacitive loads. A D flipflop, implemented by dynamic laches, operating with a true signal phase clock (TSPC) is introduced in [99], [101], [102]. In this structure, the transistors triggered by the input clocks are placed in the closest path to V_{DD} in order to have smaller capacitances. The D flipflops for this structure have only 9 transistors. Consequently, the traces in the layout are shorter than when 18 transistors are employed and the input and output capacitances for this configuration are much less than the SCL and CML. Therefore, the *W/L* ratio of the transistors can be lower than the transistors of the SCL and CML, which results in decreasing the power consumption.

For these reasons, the TSPC flip-flop is mostly beneficial in high-frequency and low-power dividers. So as to increase the output swing, the D flipflop with TSPC structure is modified in [99], called Extended True Single-Phase Clock (E-TSPC). The disadvantage of TSPC and E-TSPC flipflops is that the output is not complementary. Figure 4-4 shows the D flipflop designed in classical TSPC, implemented in 180 nm CMOS technology. The value of the *W/L* ratio of the transistors is as follows: *[$(W/L)_{0\text{-}7,9}$= 240 nm/180nm, $(W/L)_{8,10}$=480nm/180nm*].

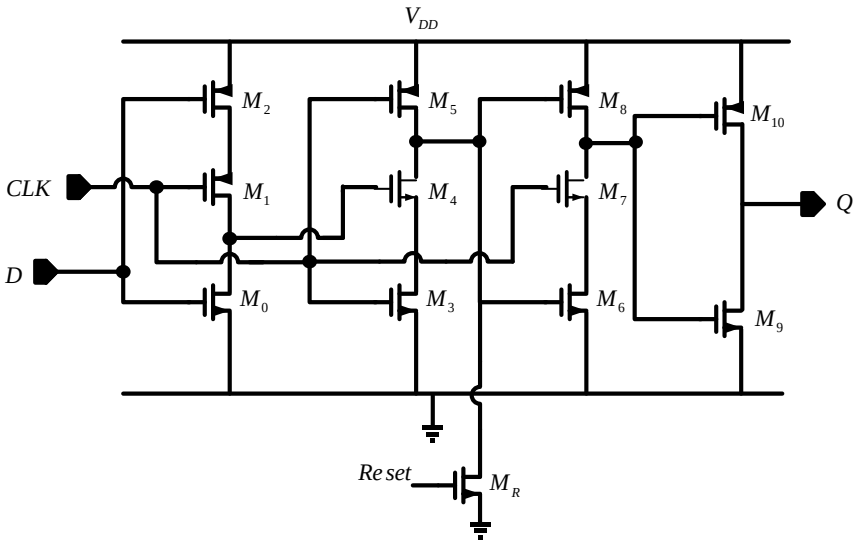


Figure 4-4 The D Flip-Flop designed in TSPC.

Taking into account the D flipflop designed in TSPC, PFD can be implemented as demonstrated in Figure 4-5. The simulation results for PFD shown in Figure 4-6 indicate that the PDF works nearly correctly. However, it does not work perfectly because of the glitches. The value of the *W/L* ratio of the transistors is as follows: *[(W/L)$_{0,2\text{-}8,10,12\text{-}20,22}$= 240 nm/180nm, (W/L)$_{1,9,11,13,21,23}$=480nm/180nm*]

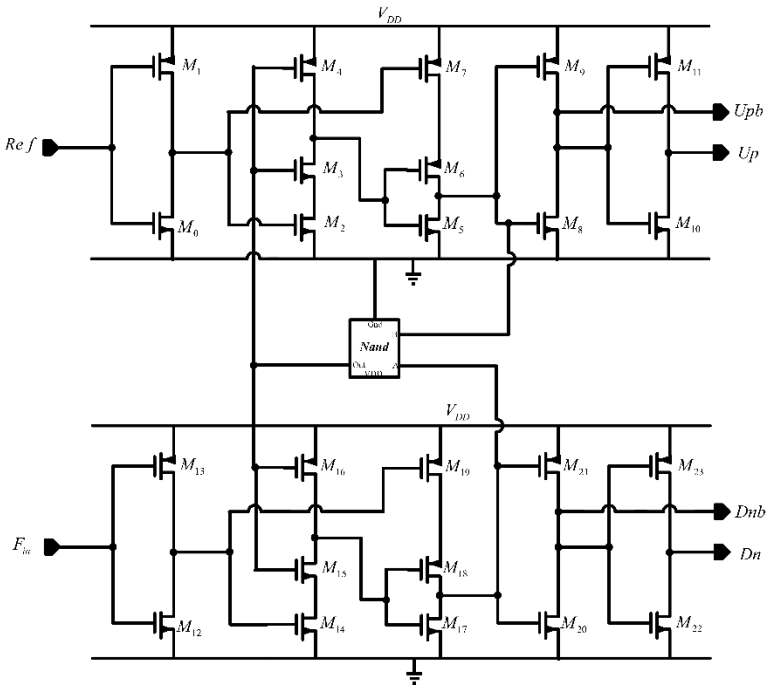


Figure 4-5 The PFD circuitry designed with TSPC flip-flops.

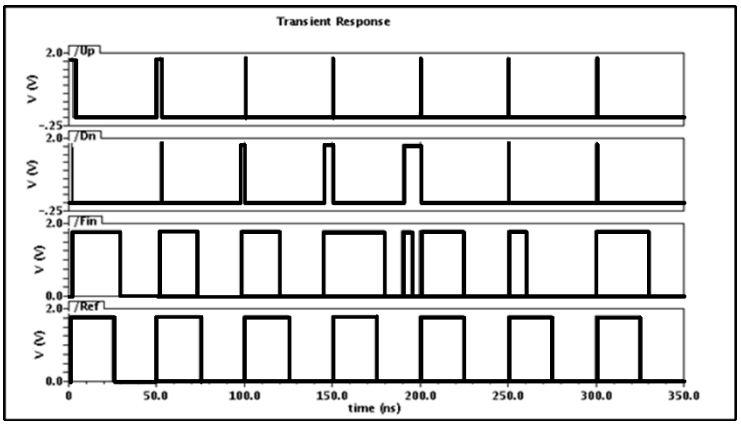


Figure 4-6 The simulation results for the PFD designed with TSPC flipflops.

As shown in Figure 4-6, when *Ref* and F_{in} are at the high state (ONE) simultaneously, the PFD is reset to zero and the pulse width of one output signal (*Up* or *Down*) is proportional to the phase error, and another output signal is a glitch. To remove these

glitches, a delay element is usually added in the reset path, as indicated in Figure 4-7. In this case, the phase difference is no longer represented by the pulse width of *Up* or *Down*, but by the edge difference between the edges of *Up* and *Down*. The idea is that we must not have any glitches (sharp sparks shown in Figure 4-6) when *Up* and *Down* are ONE. To do this, as demonstrated in Figure 4-8 we add two NAND gates (G_4 and G_5) and 4 inverters (G_2, G_3, G_6, and G_7) at the output of the D flipflops, to remove the glitches. Once the Q_1 and Q_2 become high at the same time, the G_2 and G_3 outputs will be zero and it forces the NAND gates (G_4 and G_5) outputs to become ONE. Since the *Up* and *Down* are the inverted G_4 and G_5 outputs, the *Up* and *Down* will be set to zero immediately.

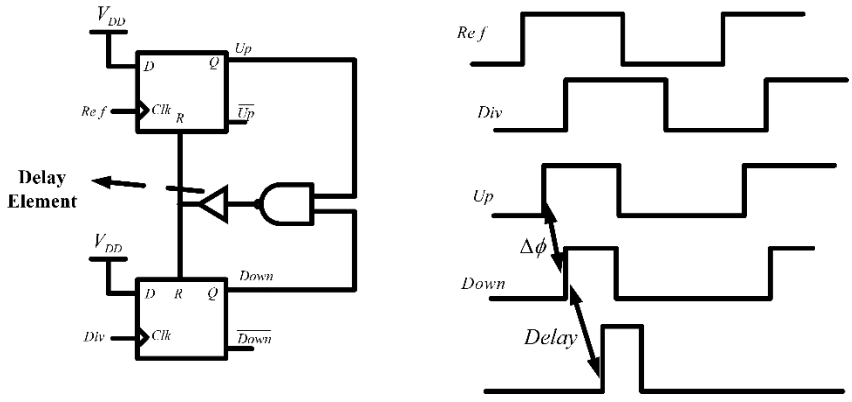


Figure 4-7 Adding a delay element to remove the dead zone.

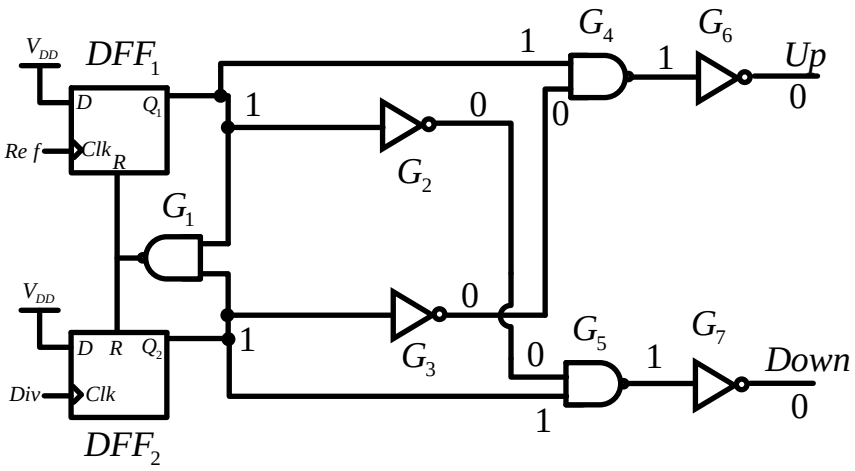


Figure 4-8 A gate level schematic of the proposed PFD to remove glitches.

Figure 4-9 and Figure 4-10 represent the proposed PFD in the transistor level, and the simulation results for this PFD respectively. The value of the *W/L* ratio of the transistors is as follows: *[(W/L)$_{0\text{-}11}$= 240 nm/180nm*]

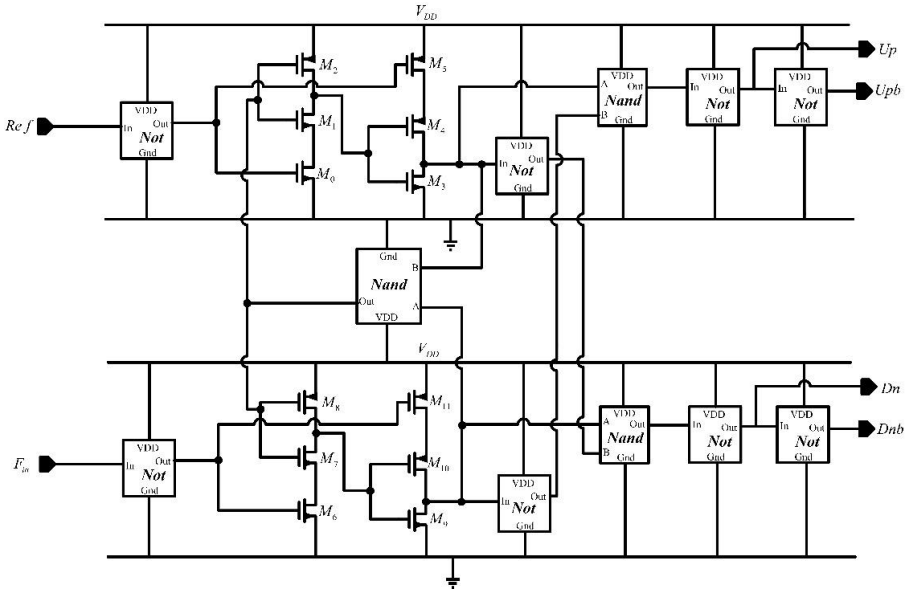


Figure 4-9 A transistor level schematic of the proposed PFD to remove glitches.

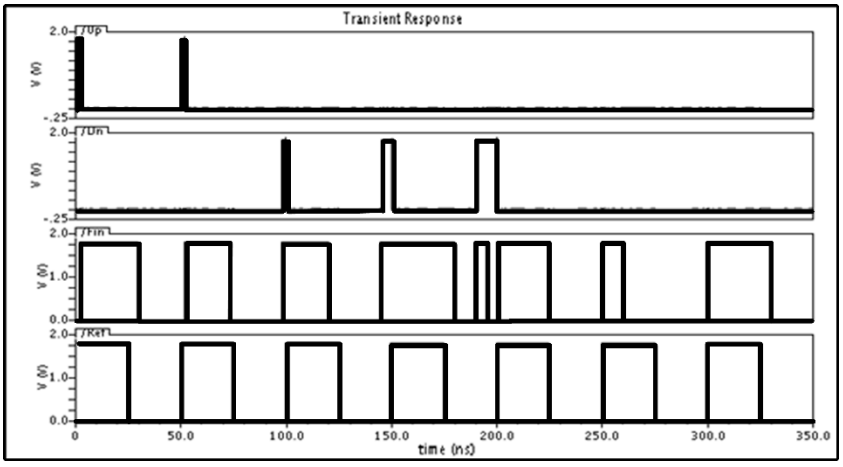


Figure 4-10 The simulation results for the proposed PFD.

As can be seen, there is no glitch at the output signal. But because of the delay of logic gates, the propagation delay in the PFD increases, which leads to increasing the lock time in the frequency synthesizer.

4.3 Programmable frequency divider

The output of Figure 4-1 is $f_{out} = Nf_{ref}$. Hence, the ability to control the output frequency is contingent on the controllability of N (the division ratio). Although it is quite easy to make N programmable, employing a divider (such as a divide-by-2 circuit) before the actual programmable divider is helpful if the output frequency is in the range of gigahertz since a divide-by-2 circuit lowers the operating frequency and the lock time [95], [103]–[106] . Therefore, we use a divide-by-2 circuit before the programmable divider.

To have a fractional division, we must use a prescaler. Fixed modulus and dual modules prescalers are two types of prescalers. The former suffers from limited programmability. To overcome this shortcoming, we can decrease the reference frequency; however, doing

so would degrade overall phase noise in the synthesizer. Hereupon, the letter is selected in this thesis. As mentioned in the introduction, the delta-sigma modulator has a higher frequency resolution that is unsuitable for low power applications. Therefore, it is not used.

The prevalent prescaler is illustrated in Figure 4-11 [92]. The ÷ 2/3 circuit employs an OR gate to permit ÷ 3 operation if the modulus control, *MC*, is low or ÷ 2 operation if it is high. Figure 4-12 shows a transistor level schematic of Figure 4-11. This circuit is combinations of logical gates and TSPC D flipflops. The value of the *W/L* ratio of the transistors for Figure 4-12 is as follows: *[(W/L)$_{0\text{-}19,21,22}$=240nm/180nm, (W/L)$_{20}$=480nm/180nm, (W/L)$_{23,24}$=300nm/180nm, (W/L)$_{25,26}$=720 nm/180nm*].

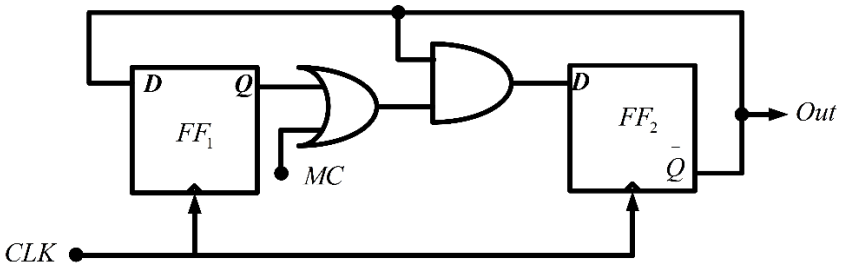


Figure 4-11 A divide-by-2/3 circuit [92].

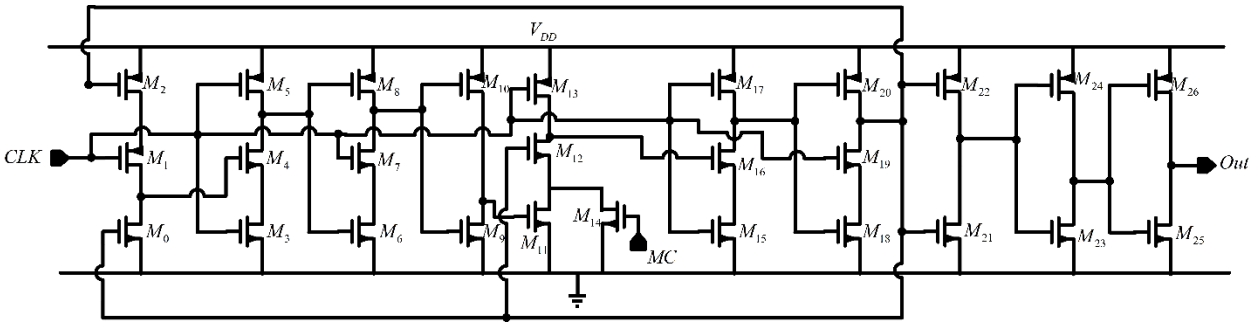


Figure 4-12 The divide-by-2/3 circuit based on Figure 4-11.

The simulation results of Figure 4-12 show that this divide-by-2/3 circuit cannot work over 2 GHz due to input capacitances. For this reason, a proposed dynamic asynchronous resettable D flipflop has been designed based on TSPC and E-TSPC D flipflops, represented in Figure 4-13. The value of the *W/L* ratio of the transistors for this D flipflop is as follows: *[$(W/L)_{0\text{-}3,5,7}$=240nm/180nm, $(W/L)_4$=360nm/180nm, $(W/L)_6$=600nm/180nm, $(W/L)_8$=480 nm/180nm*]. With this new D flipflop, another new divide-by-2/3 circuit is designed as shown in Figure 4-14.

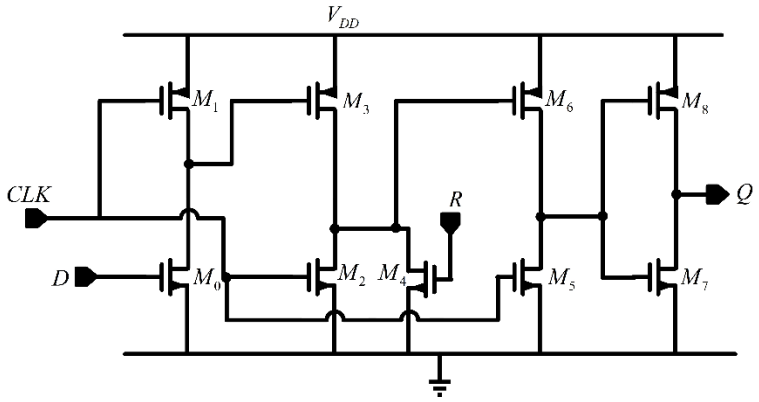


Figure 4-13 The proposed dynamic asynchronous resettable D flipflop based on TSPC and E-TSPC D flipflops.

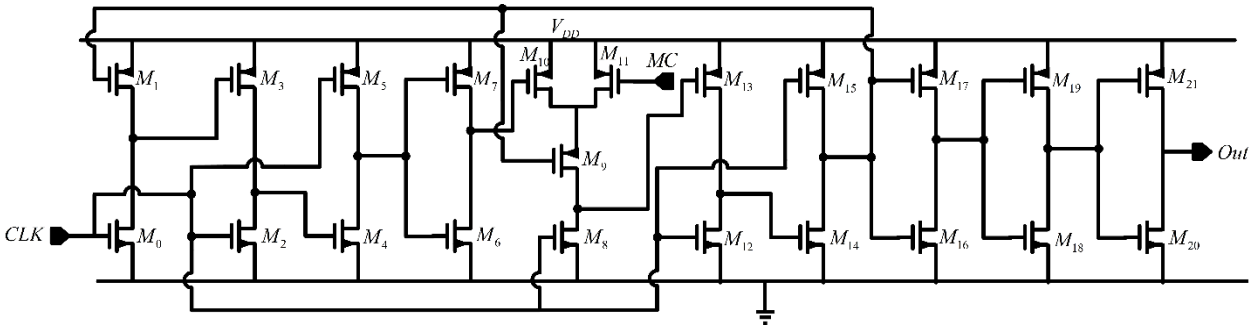


Figure 4-14 The new divide-by-2/3 circuit with the proposed dynamic-asynchronous resettable D flipflop.

The new divide-by-2/3 circuit is simulated with pulse and sinusoidal signals at 5.5 GHz, and its results are shown in Figure 4-15 and 4-16, respectively. Table 4-1 also represents the power consumption of these divide-by-2/3 circuits. Note that the simulations show that Figure 4-14 can work simply up to 6.4 GHz, but Figure 4-12 cannot work up to that frequency because the input capacitances in Figure 4-12 are higher than Figure 4-14. In this chapter, Figure 4-14 is employed as the prescaler. The value of the *W/L* ratio of the transistors for Figure 4-14 is as follows: *[$(W/L)_{0\text{-}9,12\text{-}21}$=5µm/180nm NF=5, $(W/L)_{10,11}$=5µm/180nm NF=10*].

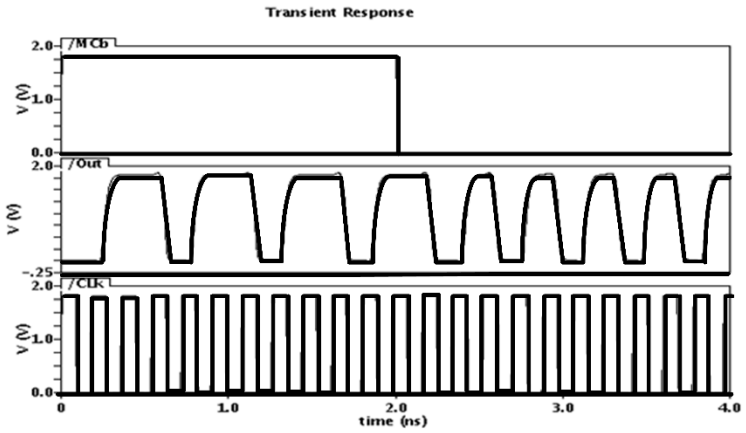


Figure 4-15 The simulation results of Figure 4-14 with a pulse input.

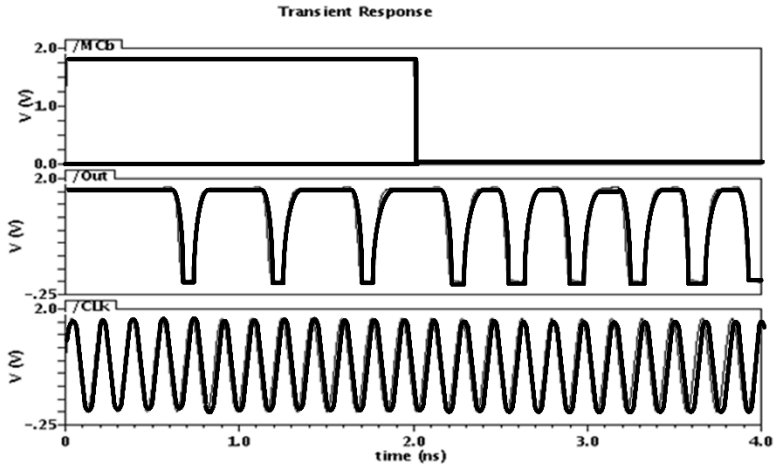


Figure 4-16 The simulation results of Figure 4-14 with a sinusoidal signal.

Table 4-1 The power consumption for Figure 4-12 and 4-14.

Circuit	Input signal	Power (mW)
Figure 4-12	Pulse	0.32
	Sinusoidal	-
Figure 4-14	Pulse	0.4
	Sinusoidal	0.38

Designers usually use VHDL or Verilog and auto route place in cadence to design *P* and *S* counters. However, these techniques are not good since the Cell Bases used in these approaches do not work optimally in high frequencies. That is why these methodologies are not used here. The *P* counter can be simply implemented by some divide-by-2 and 3 circuits.

The fractional parts for IEEE 802.11b, U-NII, and IEEE 802.11a standards are $n_1/8$, $n_1/3$, $n_1/2$, in where $n_1 = 0,1,\ldots,7$, $n_2 = 0,1,2$, $n_3 = 0,1$, respectively. These parts can be implemented by 3-bit and one-bit accumulators in IEEE 802.11a and IEEE 802.11b. However, the fractional parts of U-NII should be implemented by an accumulator with larger numbers of bits or a delta-sigma modulator, that would increase power dissipations. To solve this problem, a 3-bit parallel-input/serial-output shift register is exerted.

One way to implement a programmable divider is to use JK flipflops and then designing the counters with it. To this end, we implement AND-D and OR-D flipflops from the

proposed D flipflop of Figure 4-13, which are presented in Figure 4-17 and 4-18, respectively. We then design the JK flipflop by these AND-D and OR-D flipflops as illustrated in Figure 4-19. Moreover, a RS latch can be made via Figure 4-20. The performance of the designed JK flip flop is simulated and the results are shown in Figure 4-21. The power consumption is 0.1 mW when the frequency of the input signal is 3 GHz. The value of the *W/L* ratio of the transistors for Figure 4-17 is as follows: *[$(W/L)_{0\text{-}7,9,11}$=240nm/180nm, $(W/L)_8$=600nm/180nm, $(W/L)_{10,12}$=480nm/180nm*], for Figure 4-18 is as follows: *[$(W/L)_{0\text{-}7,9,11}$=240nm/180nm, $(W/L)_8$=600nm/180nm, $(W/L)_{10,12}$=480nm/180nm*], And for Figure 4-19 is as follows: *[$(W/L)_{0,2\text{-}5,7\text{-}9,11,12,14,16}$=240nm/180nm, $(W/L)_{1,6,13,15,17}$=480nm/180nm, $(W/L)_{10}$=360nm/180nm*].

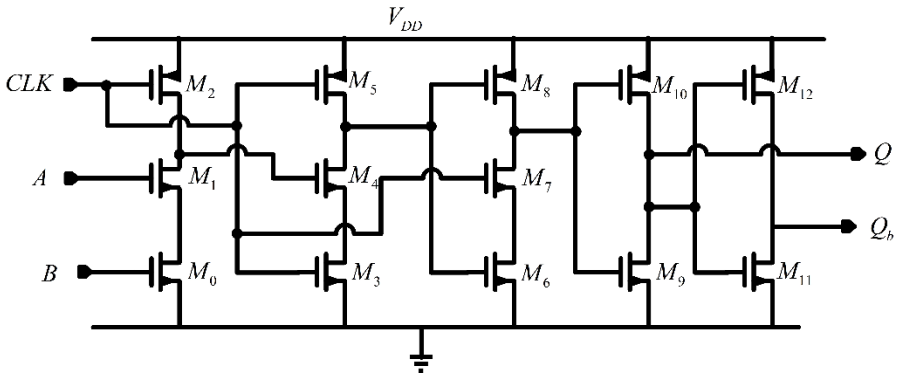


Figure 4-17 A proposed AND-D flipflop.

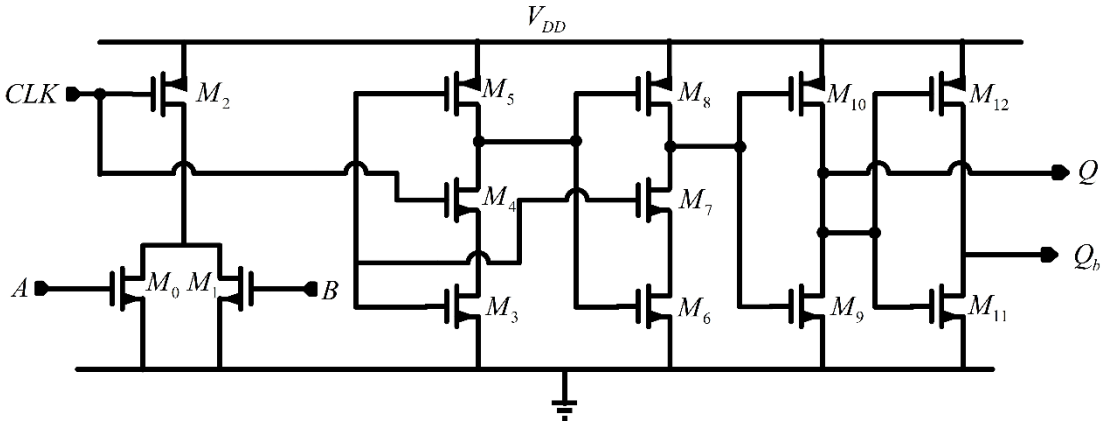


Figure 4-18 A proposed OR-D flipflop.

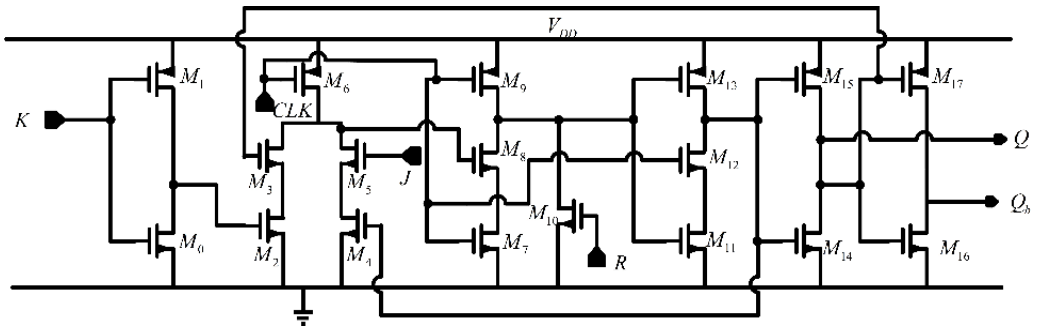


Figure 4-19 A proposed asynchronous JK flipflop.

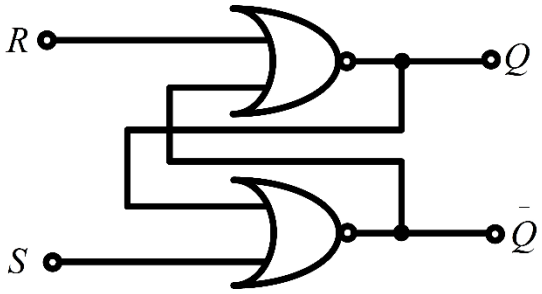


Figure 4-20 A RS latch.

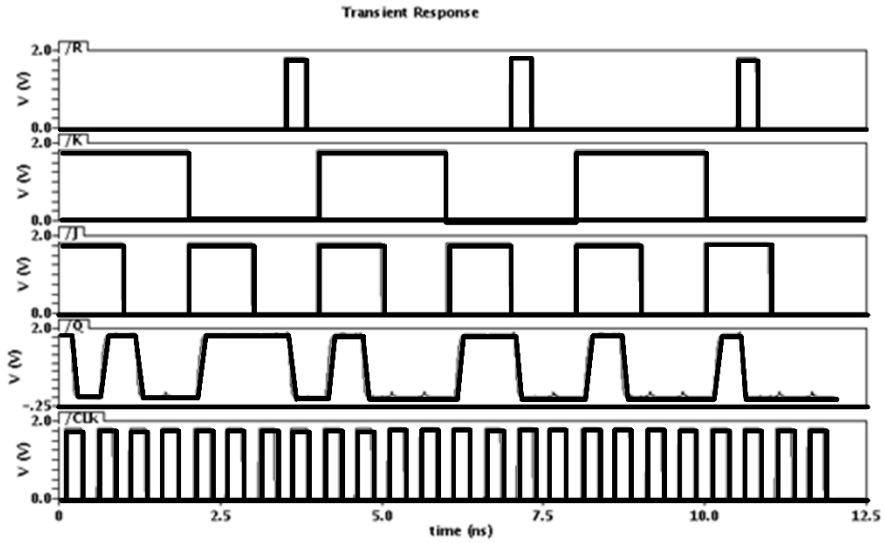
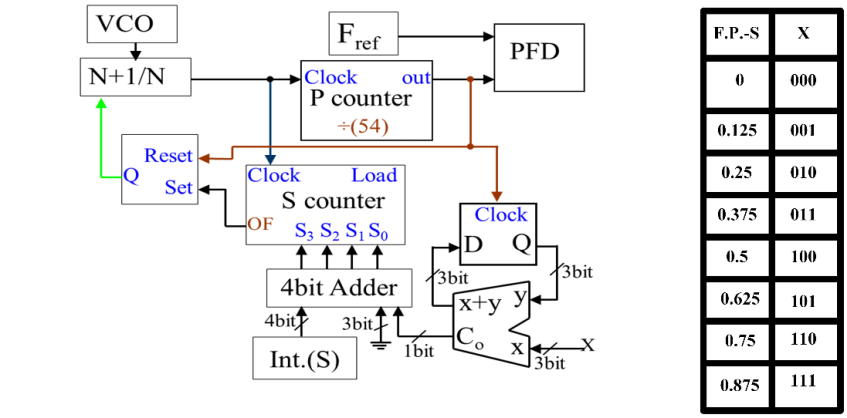


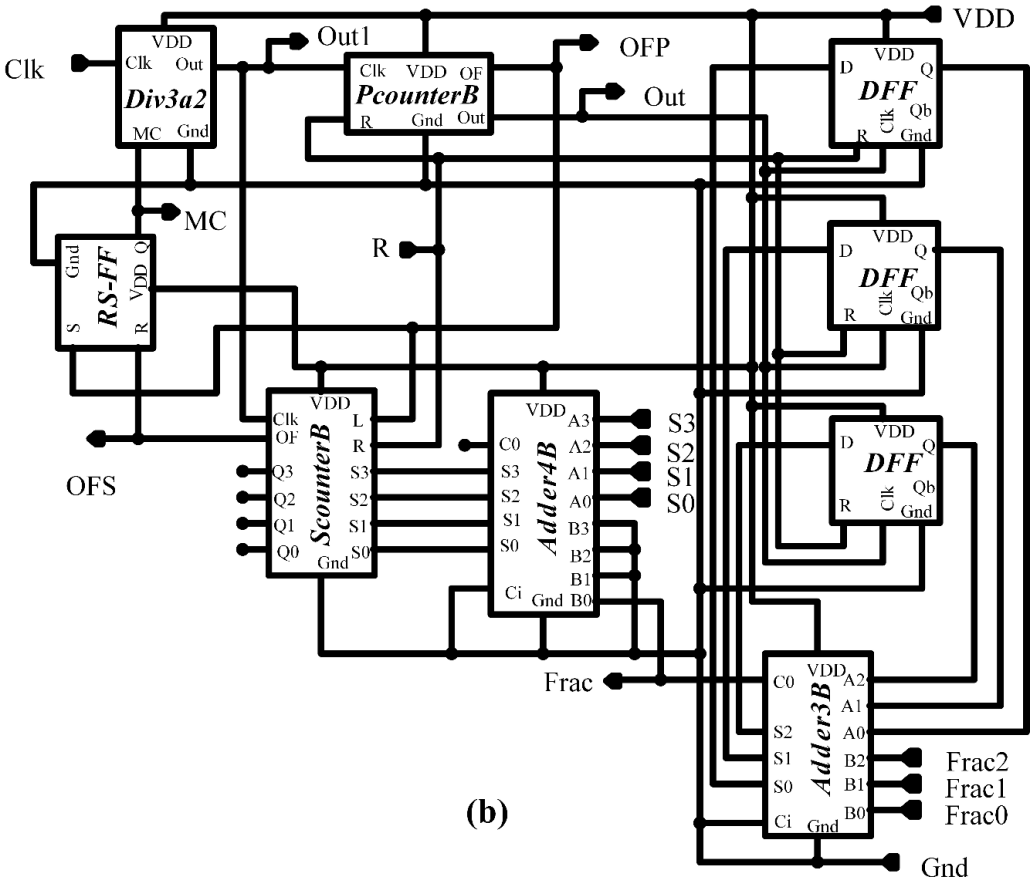
Figure 4-21 The simulation results of the proposed JK flipflop.

Figure 4-22 indicates the frequency divider designed for IEEE 802.11b and Bluetooth standards. Figure 4-22 (a) demonstrates the conceptual way to implement the frequency divider whereas Figure 4-22 (b) exhibits the actual way to implement it. The block "*Div3a2*" is a divide-by-2/3 circuit, the block "*PcounterB*" is a divide-by-54 circuit, the block "*ScounterB*" is a 4-bit programmable counter, the D flipflops and "*Adder3B*" are for the fractional part of the *S* counter, and the "*Adder4B*" is for the integral part of the *S* counter. Figure 4-23 represents the block "*ScounterB*" and Figure 4-24 illustrates the block "*Dcella*".



F.P.-S	X
0	000
0.125	001
0.25	010
0.375	011
0.5	100
0.625	101
0.75	110
0.875	111

(a)



(b)

Figure 4-22 The frequency divider for IEEE 802.11 b and Bluetooth standards (a) conceptual one (b) actual one.

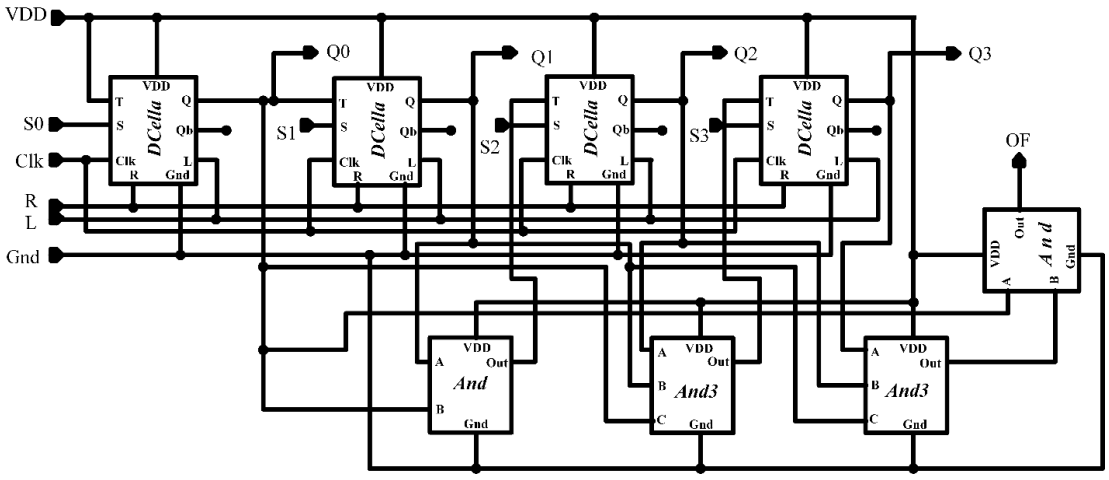


Figure 4-23 The "ScounterB" block.

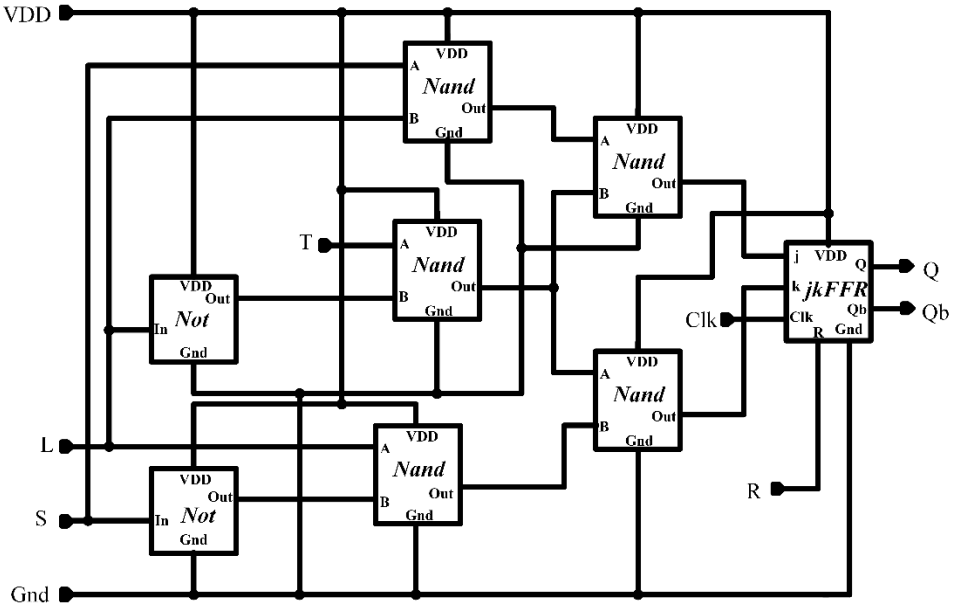


Figure 4-24 The "Dcella" block.

Figure 4-25 and 4-26 represent the performance of Figure 4-22 (b) by pulse and sinusoidal signals when the frequency of the signals is 2.5 GHz. The divider value is 8.5. In these figures, *Out, Out1*, *OFS*, *OFP*, and *Frac* are the divider output, prescaler output,

overflow of "*Scounter*", overflow of "*Pcounter*", and fractional part of the divider, respectively. It is also easily seen from Figure 4-25 and 4-26 that the number of divide-by-2/3 times changes with the *Frac* value. The power consumption for this simulation is presented in Table 4-2.

Table 4-2 The power consumption for Figure 4-22 (b).

Standard	Input signal	Power (mW)
IEEE 802.11b and Bluetooth	2.5-GHz pulse clock	0.8
	2.5-GHz sinusoidal clock	0.8

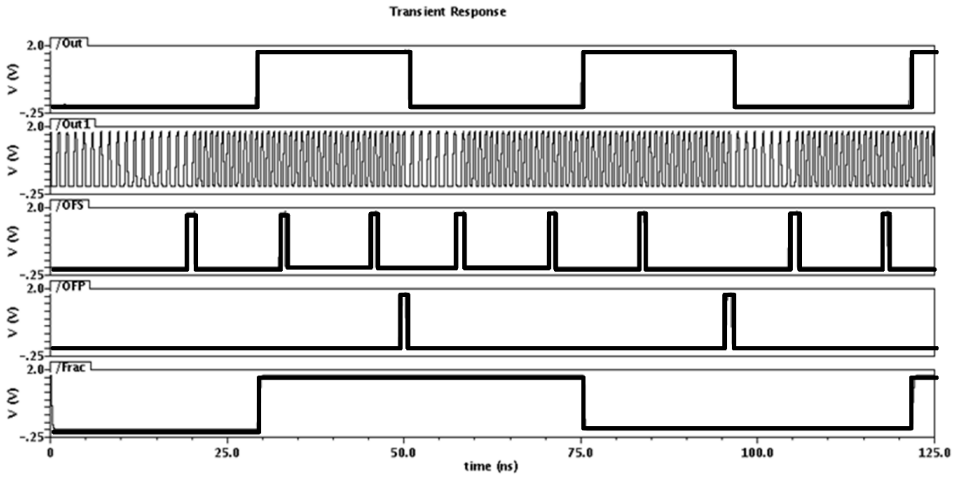


Figure 4-25 The simulation results for the frequency divider in IEEE 802.11b and Bluetooth standards once the input signal is a pulse signal.

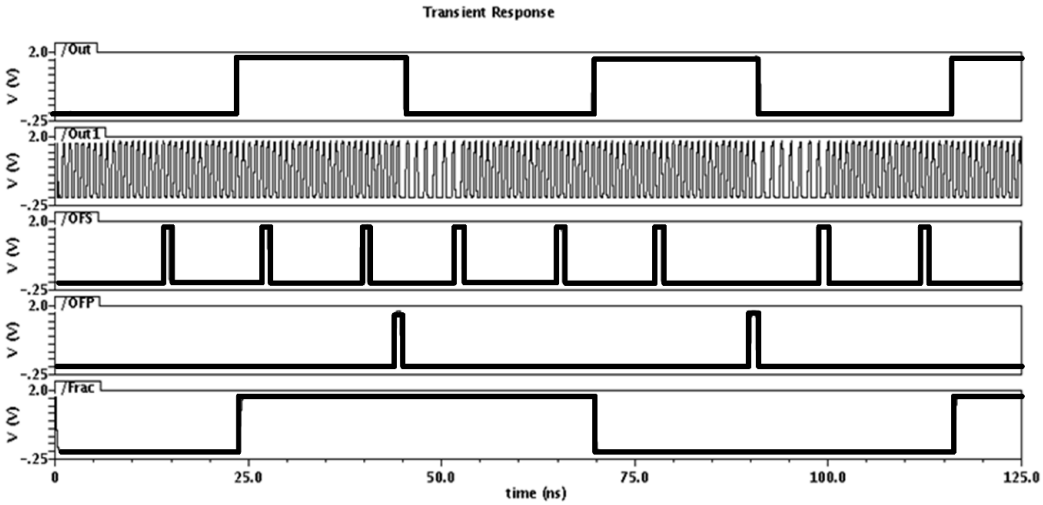


Figure 4-26 The simulation results for the frequency divider in IEEE 802.11b and Bluetooth standards once the input signal is a sinusoidal signal.

The frequency divider for U-NII standard is designed in the same way as IEEE 802.11b and Bluetooth standards as represented in Figure 4-27. The block "*Div3a2*" is again a divide-by-2/3 circuit, the block "*Pcounter*" is a divide-by-64 circuit, the block "*Scounter*" is a 5-bit programmable counter, the "*ShiftReg*" is a 3-bit parallel input/series output shift register for producing the fractional part of the S counter, the "*Mux2-1*" is a 2 to 1 multiplexer, and the "*S4-S0*" is for selecting the integral part of the *S* counter, shown in Figure 4-23.

The performance of Figure 4-27 is simulated and the results are represented in Figure 4-28 and 4-29. Pulse and sinusoidal signals are applied to the Figure 4-27. The frequency of these signals is 5.5 GHz. *S* has two values, that both have the same integer value equivalent to 24, and the fractional values equal to 2.3 and 1.3. *Out*, *Out1*, *OFS*, *OFP*, and *Frac* are

the divider output, prescaler output, overflow of "*Scounter*", overflow of "*Pcounter*", and fractional part of the divider, respectively. The power consumption for this simulation is presented in Table 4-3.

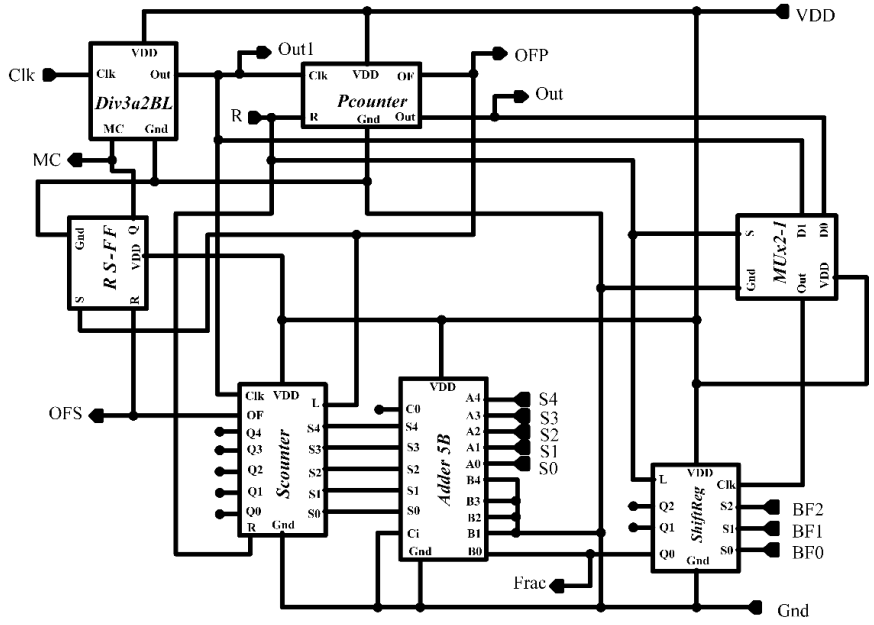


Figure 4-27 The frequency divider for U-NII standard.

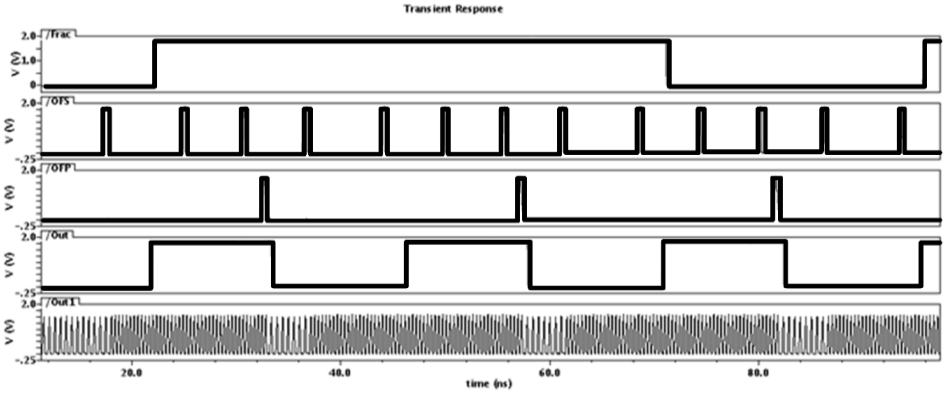


Figure 4-28 The simulation of Figure 4-27 when the integer value is 24 and the fractional value is 2.3.

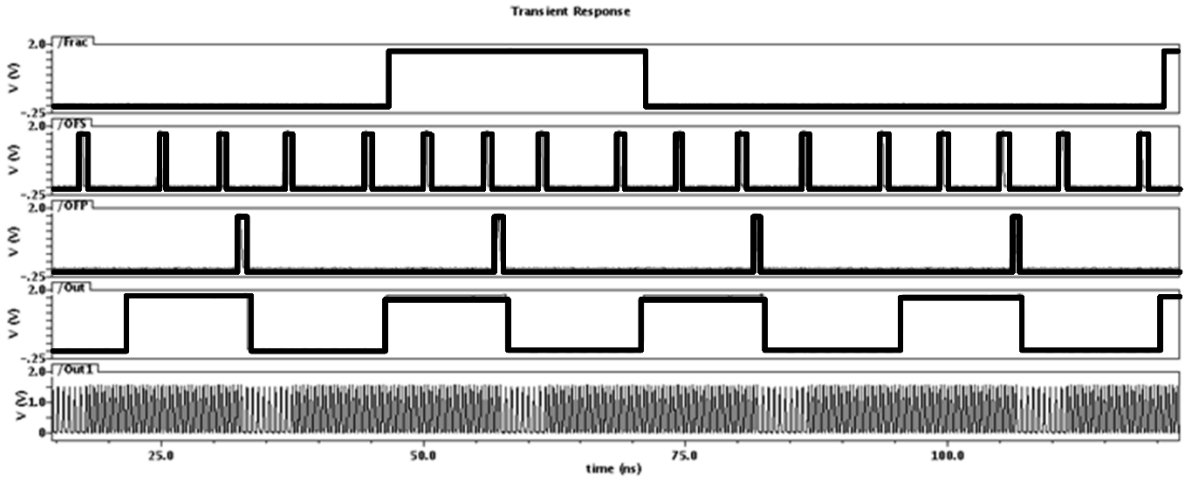


Figure 4-29 The simulation of Figure 4-27 when the integer value is 24 and the fractional value is 1.3.

Table 4-3 The power consumption for Figure 4-27.

Standard	Input signal	Power (mW)
U-NII	5.5-GHz pulse clock	1.8
	5.5-GHz sinusoidal clock	2

The frequency divider for IEEE 802.11a standard is designed and represented in Figure 4-30. The block "*Div3a2*" is again a divide-by- 2/3 circuit, the block "*Pcounter*" is a divide-by-64 circuit, the block "*Scounter*" is a 5-bit programmable counter, the D flip flops and "*FullAdder*" is for the fractional part of the *S* counter, and the "*Adder5B*" is for the integral

part of the *S* counter "*S0-S4*". *Out, Out1, OFS, OFP*, and *Frac* are the divider output, prescaler output, overflow of "*Scounter*", overflow of "*Pcounter*", and fractional part of the divider, respectively.

The performance of Figure 4-30 is simulated and the results are represented in Figure 4-31. Pulse and sinusoidal signals are applied to the Figure 4-30. The frequency of these signals is 5.5 GHz. The value of *S* is 24.5. The power consumption for this simulation is presented in Table 4-4.

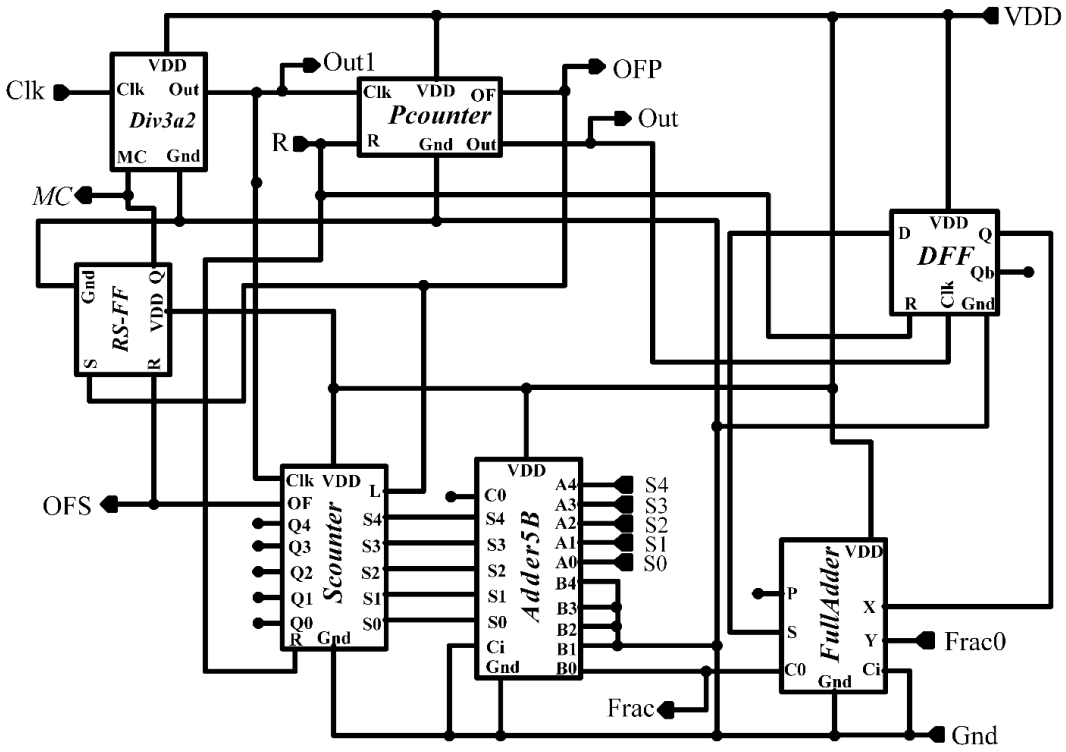


Figure 4-30 The frequency divider for IEEE 802.11a standard.

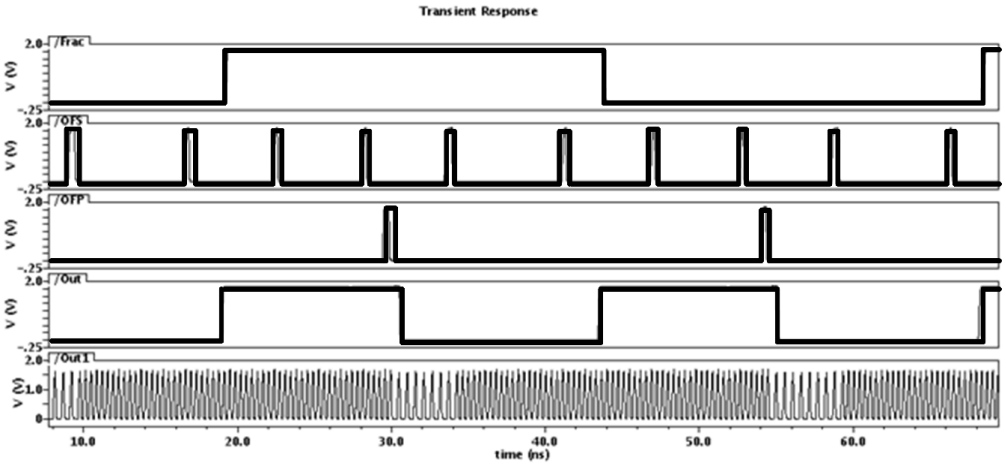


Figure 4-31 The simulation of Figure 4-30.

Table 4-4 The power consumption for Figure 30.

Standard	Input signal	Power (mW)
IEEE 802.11a	5.5-GHz pulse clock	1.7
	5.5-GHz sinusoidal clock	1.85

4.4 Design and simulation of voltage control oscillator (VCO)

We use the designed VCO in the chapter 3, depicted again in Figure 4-32. M_1 and M_2 are switching transistors and act as *-gm*. The circuit current is determined with M_1 and M_2 while their gate and drain voltages are fixed with the feedback of the gates of M_5 and M_6. The circuit current therefore is controllable. V_b is provided by an external supply voltage. M_3

and M_4 are employed to amplify the signals in the drains of M_1 and M_2. As a result, the output oscillation amplitude is increased and the phase noise of VCO is decreased [13]. The output voltage (peak to peak) is 4.1 V, represented in Figure 4-33. It means that there is no need to use a buffer between the VCO and prescaler in order to drive the prescaler. Consequently, the power consumption of the frequency synthesizer will be diminished substantially. C_1 and C_2 filter out the white noise of the transistors. These capacitors along with the varactors determine the operating frequency.

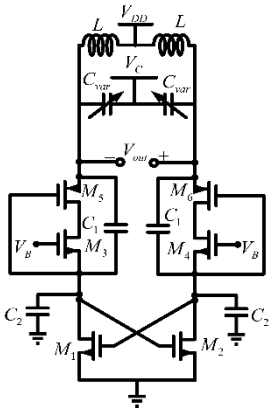


Figure 4-32 The designed VCO in the chapter 3 is used for the frequency synthesizer.

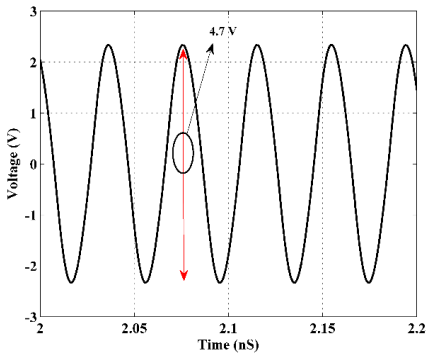


Figure 4-33 The simulation of the oscillation amplitude of the VCO in Figure 4-32.

The following steps are applied to design the VCO. The first step is to determine the (*W/L*) of the transistors. Note that the power spectral density of a transistor for white noise is presented as [92]

$$S(f) = 4kT\gamma g_m \quad (\frac{A^2}{Hz}), \tag{4-1}$$

While for flicker noise

$$S(f) = \frac{k}{WLC_{ox}f} \quad (\frac{V^2}{Hz}), \tag{4-2}$$

where *k* is Boltzmann constant and *T* is the absolute temperature. Therefore, there is a trade-off between them in terms of *W/L*. While a larger *W/L* leads to less flicker noise, white noise will be increased. It seems that the *W/L* transistors M_1 and M_2 should be big enough to have an easy startup, because M_1 and M_2 provide *-gm* for the VCO, while decreasing phase noise induced by their flicker noise, since C_2 can filter out their white noise. On the other side, a larger *W/L* can increase the current and thereby the oscillation amplitude. As a result, M_1 and M_2 will enter the triode region and the transistors will not work in class C [57]. It is extremely important to keep M_1 and M_2 in the active region to suppress not only phase noise induced by the white noise but also the flicker noise [62]. For the aforementioned reasons, the *W/L* transistors M_1 and M_2 should be not sized extremely large. The $(W/L)_{1\text{-}2}$ is *20µm/0.18µm*.

As mentioned, the transistors M_3 and M_4 act as an amplifier for the drain signals of M_1 and M_2. Note that the transistors M_3 and M_4 can be simply biased in the active region through

V_b. As such, their *W/L* can be sized largely to suppress phase noise induced by their flicker noise whereas their white noise is recirculated by means of C_1 and not be injected into the tank. Remember that their *W/L* should not be significantly large to force transistors M_1 and M_2 to enter the triode region as well. The $(W/L)_{3\text{-}4}$ is *50µm/0.18µm*.

M_5 and M_6 shield the current of M_1 and M_2 from changes of power supply through the feedback of the gates of M_5 and M_6 to the drains of M_1 and M_2. Moreover, electron mobility in a channel of NMOS (u_n) is two times of electron mobility in a channel of PMOS (u_p). This means that $(W/L)_{5\text{-}6}$ should be doubled than $(W/L)_{3\text{-}4}$ since M_5 and M_6 are series with M_3 and M_4. Otherwise, M_5 and M_6 will not work properly. The $(W/L)_{5\text{-}6}$ is *100µm/0.18µm*. Bear in mind that M_5 and M_6 are in the active region at the beginning of each period. However, they will enter the triode region for the rest of a period, which can help to suppress the flicker noise even more [58].

The second step is calculation of power consumption, which is shown in (4-3)

$$P = V_{DD} \times I_B . \tag{4-3}$$

where P, V_{DD}, and I_B are power consumption, power supply (1.8 V), and the current drawn for the power supply, respectively. The third step is selection of the *W/L* of MOS-varactor and value of inductors to set the tuning rang and operation frequency. The following formula are used for this purpose

$$f_{\min} \le \frac{1}{\sqrt{LC_{\max}}}. \tag{4-4}$$

$$\frac{1}{\sqrt{LC_{\min}}} \leq f_{\max} \ . \tag{4-5}$$

where f_{min}, f_{max}, C_{min}, C_{max}, and L are the minimum frequency, maximum frequency, minimum and maximum capacitors seem across the tank, and inductor of the tank, respectively.

Figure 4-34 demonstrates the post-layout simulation of the phase noise for the designed VCO when the frequency is 2.4 GHz. The inductor used in this VCO is not designed. We have used the inductor provided by TSMC in the 180 nm technology file. The quality factor of the tank is about 10. Table 4-5 summarizes the performance of this VCO.

Note that this VCO can cover the required frequencies for IEEE 802.11b and Bluetooth standards, thereby a capacitor bank is not used. However, we have used a capacitor bank for U-NII, HIPERLAN, and IEEE 802.11a standards to cover the frequencies of 5 to 5.9 GHz required for these standards. The phase noise is slightly degraded in this case since the quality factor of the tank is somehow decreased and the transistors will spend more time in the triode region.

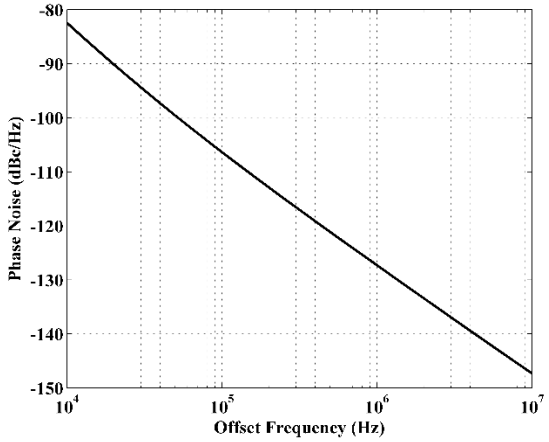


Figure 4-34 The post-layout simulation of the phase noise for the designed VCO.

Table 4-5 A summary of the VCO performance @ 2.4 GHz.

Phase noise	-83dBc/Hz @ 10-KHz offset frequency (Flicker noise corner) -127dBc/Hz @ 1-MHz offset frequency -148.5dBc/Hz @ 10-MHz offset frequency
VCO Gain	120 MHz
Tuning range	2.3–2.5 GHz
Power consumption	2.16 mW

4.5 Design of Charge Pump (CP) and Loop Filter (LP)

Figure 4-35 shows the charge pump and loop filter designed for this frequency synthesizer. Transistors M_5 and M_8 operate as a switch for M_4 and M_9. Hence, the clock feedthrough issue is somehow solved. Any mismatches between *Up* transistors (M_4 and M_5) and *Down* transistors (M_8 and M_9) cause ripples in the filter output. Increasing W of the transistors can help reduce these mismatches. The loop filter impedance can be calculated by (4-6):

$$Z(S) = \frac{b(\tau S + 1)}{SC_2(\tau S + b + 1)}, \tag{4-6}$$

where $\tau = C_2 R_2$ and $b = C_2/C_1$. Note that the VCO input capacitors will have loading effects on the loop filter in the PLL loop. Thus, once the filter is connected to the VCO, the input capacitors VCO should be deducted from C_1. The loop gain can be calculated by (4-7):

$$\begin{aligned} Loop\,Gain &= \frac{I_p}{2\pi}\frac{k_{VCO}}{N}Z(S) \\ &= \frac{k_{VCO}I_p}{2\pi N}\frac{b(\tau S + 1)}{SC_2(\tau S + b + 1)}, \end{aligned} \tag{4-7}$$

where k_{VCO}, I_P, and N are the VCO gain, charge pump current, and ratio of the output frequency to reference frequency, respectively. The phase margin is:

$$PM = \tan^{-1}(\tau\omega_c) - \tan^{-1}(\frac{\tau\omega_c}{b+1}), \tag{4-8}$$

where, ω_c is the loop bandwidth. By derivative of (4-8) with respect to ω_c, the maximum phase margin in the following frequency can be obtained.

$$\omega_c = \sqrt{b+1}/\tau\,, \tag{4-9}$$

$$PM_{\max} = \tan^{-1}(\sqrt{b+1}) - \tan^{-1}(\frac{1}{\sqrt{b+1}})\,. \tag{4-10}$$

Note that the maximum phase margin is the function of b (the ratio of C_2 to C_1) and for $b < 1$ the phase margin is less than 20 degrees. As a result, the PLL will be unstable. The following equation will be obtained once the loop gain is equivalent to ω_c.

$$\frac{k_{VCO} I_p}{2\pi N}\frac{b}{b+1} = \frac{C_2}{\tau^2}\sqrt{b+1}\,. \tag{4-11}$$

In this design, the value of N is a geometric mean of its minimum and maximum, which can be calculated as follows:

$$N_{design} = \sqrt{N_{\min} N_{\max}}\,. \tag{4-12}$$

In order to design the second order loop filter, the algorithm provided in [110] is used. The advantage of this algorithm is to obtain a high phase margin [49-50]. In the design to achieve a stable loop, the loop bandwidth (ω_c) is chosen less than 10 ω_{ref}.

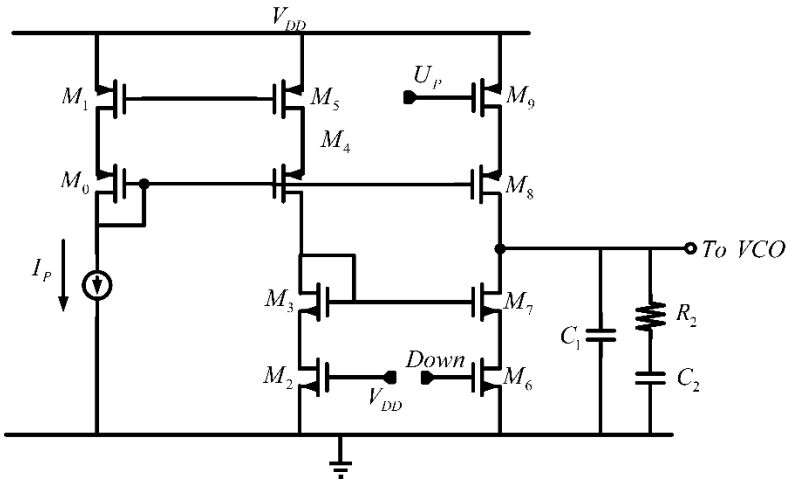


Figure 4-35 The charge pump and loop gain circuitry.

1- Finding k_{VCO} from simulation of VCO

2- Selecting a desirable phase margin and calculation of b from (4-10)

3- Selecting loop bandwidth and τ from (4-9)

4- Choosing C_2 and I_P from (4-11)

5- Calculating the noise caused by R_2, if the noise is negligible, design is ended. If not, come back to 4 and increment C_2.

We simulate the current mismatch of the charge pump at different Process, Voltage and Temperature (PVT) corners. These corners are Slow-Slow (SS) with 125 ^{o}C, Fast-Fast (FF) with -40 ^{o}C, and Typical-Typical (TT) with 27 ^{o}C. Figure 4-36 represents this simulation. When the output voltage of the CP changes from 0.2 to 1 V, the maximum current mismatch is equal to 3 µA. I_p is 50 µA.

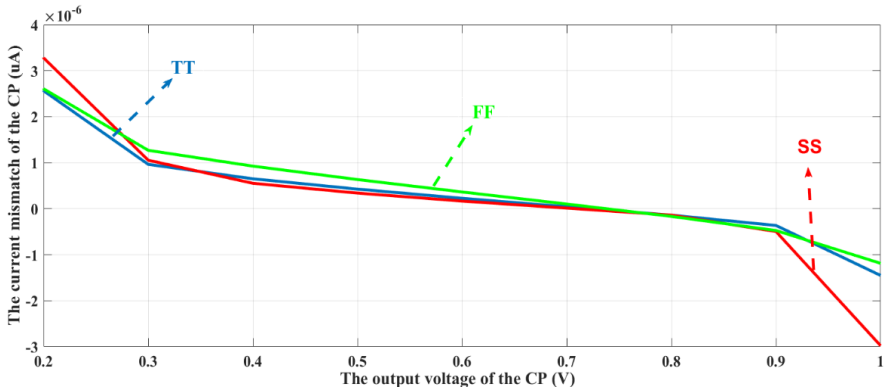


Figure 4-36 The simulated current mismatch of the CP.

4.6 Simulation of the frequency synthesizer

The previous Sections of this chapter discussed the design of the entire the frequency synthesizer along with their trade-offs. However, the loading effects should be considered. For example, upon connecting the VCO to the prescaler, the VCO operating frequency will change and the value of the capacitor seen across the tank should be adjusted. As noted, there is no need to employ a buffer between the VCO and the prescaler because the VCO output signal is large enough to drive the prescaler.

Figure 4-37 shows the block diagram of the frequency synthesizer for IEEE 802.11b and Bluetooth, U-NII, HIPERLAN, IEEE 802.11a standards. "*S0-S3*" and "*F0-F2*" form digital numbers, which the former portrays the integral part and the latter illustrates the fractional part. *Out*, *OutDiv*, *Out Pr*, *OFS*, *OFP*, *Fraco*, F_{ref} are the frequency synthesizer output, the divider output, the prescaler output, the "*Scounter*" overflow, the "*Pcounter*" overflow, the fractional part of the division, the reference frequency, respectively.

Figure 4-38, 4-39, 4-40 illustrate the transient responses for the power supply current and the output voltage of the filter for the different standards. The simulation results show that when the charge pump current is raised, the lock time declines. As a result, the frequency synthesizer phase noise decreases. Figure 4-41 depicts the output frequency spectrum of the frequency synthesizer, where the level of the supers is 60 dB less than the carrier for IEEE 802.11b standard. Figure 4-42 plots the behavioral simulations of the phase noise contributions of each block in Figure 4-37. Note that when the output phase noise of the individual block is simulated, the noise contribution of the other blocks is not considered. The noise of the Ref, PFD-CP, and divider are shaped as a low-pass filter. However, the noise of the LPF is shaped as a band-pass filter and VCO is shaped as a high-pass filter.

In addition, in order to show the fractional-N and integer spurs of the phase noise, the frequency synthesizer phase noise is plotted with the Transient-Noise simulation for IEEE 802.11b standard at 2.4 GHz, indicated in Figure 4-43. Because the VCO flicker noise corner frequency is low, the synthesizer phase noise is suppressed significantly. Table 4-6 represents the simulation results for the designed frequency synthesizer that is compared with the measurement results of other literature. The rms jitters are less than 90-fs for three standards, which is suitable for IoE applications. The power dissipations are less than 4-mW for three standards, which means that the synthesizer can be used in low-power applications. The synthesizer has fast lock time for U-NII and IEEE 802.11a standards, which is less than 4-µs whereas the lock time for IEEE 802.11 b is 18-µs.

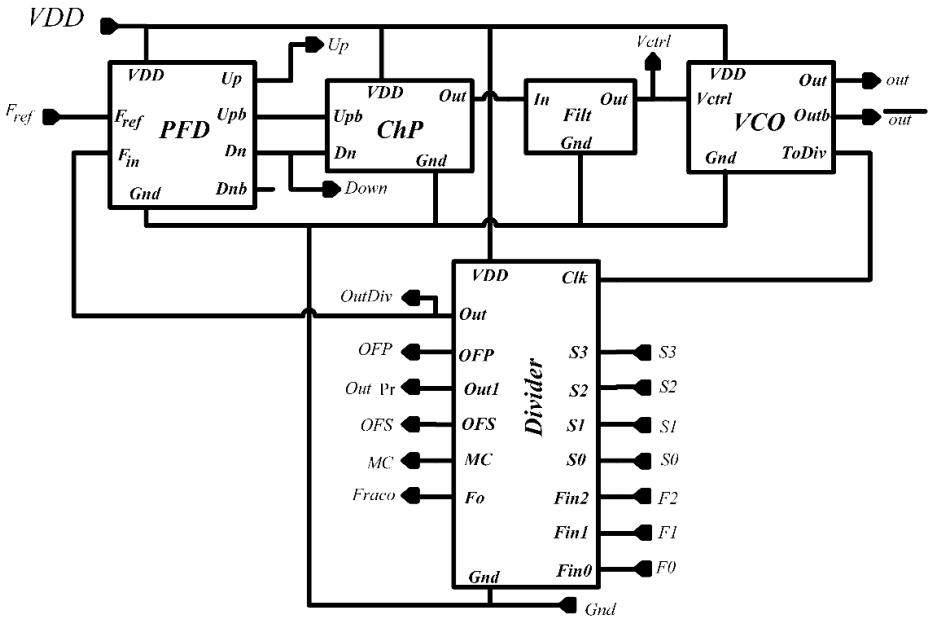


Figure 4-37 The frequency synthesizer block for IEEE 802. 11a/b, Bluetooth, U-NII, HIPERLAN standards.

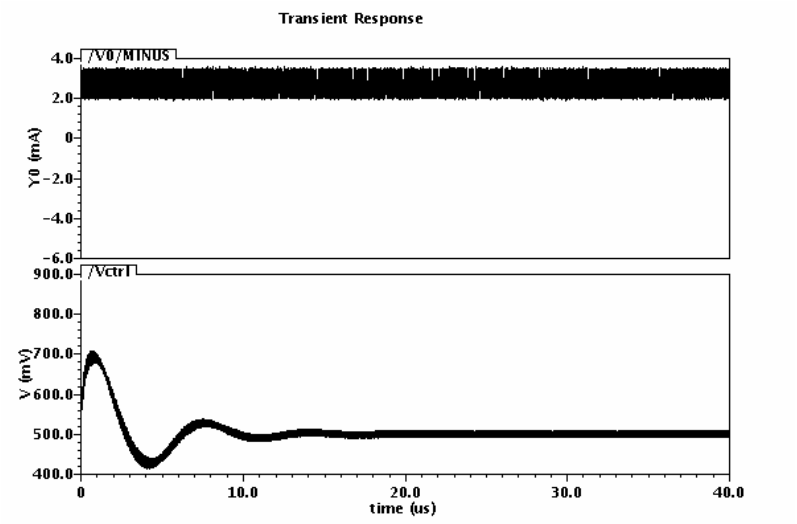


Figure 4-38 The simulation results of the power supply current and the control voltage of the VCO for IEEE 802. 11b standard.

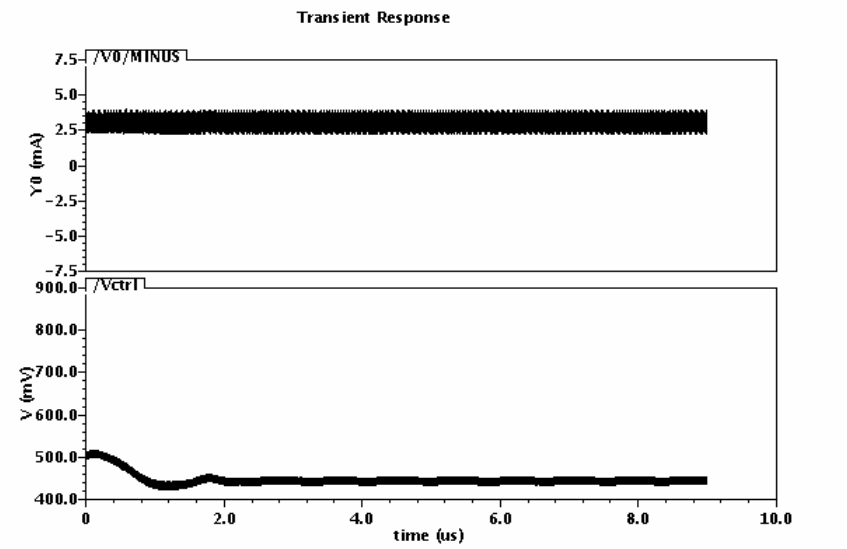


Figure 4-39 The simulation results of the power supply current and the control voltage of the VCO for U-NII standard.

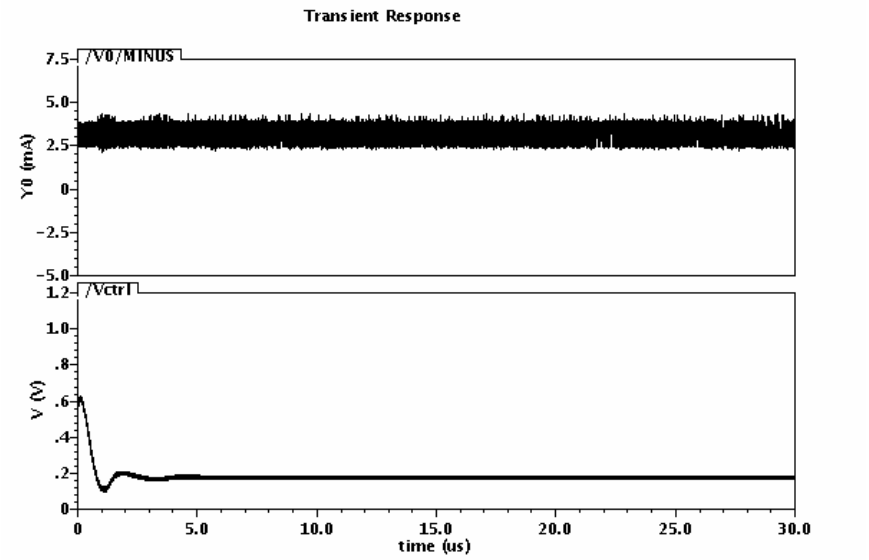


Figure 4-40 The simulation results of the power supply current and the control voltage of the VCO for IEEE 802.11a standard.

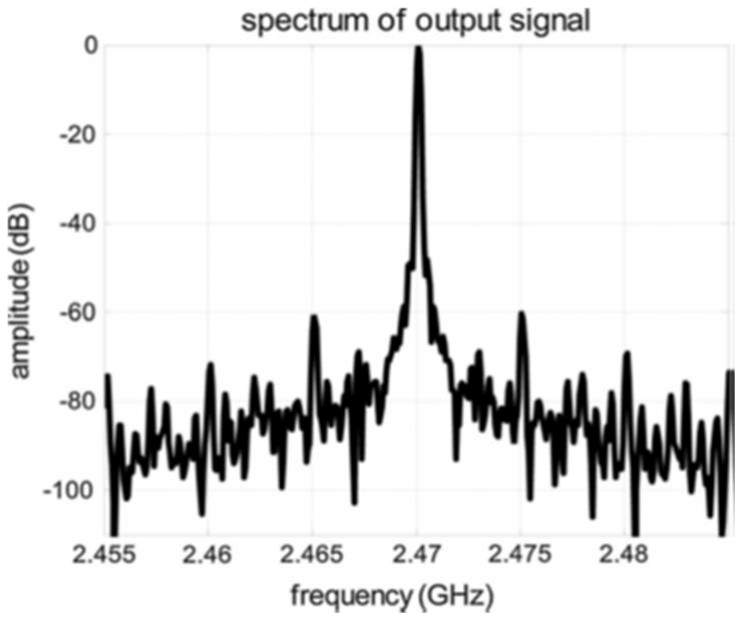


Figure 4-41 The frequency synthesizer output spectrum for IEEE 802.11b standard.

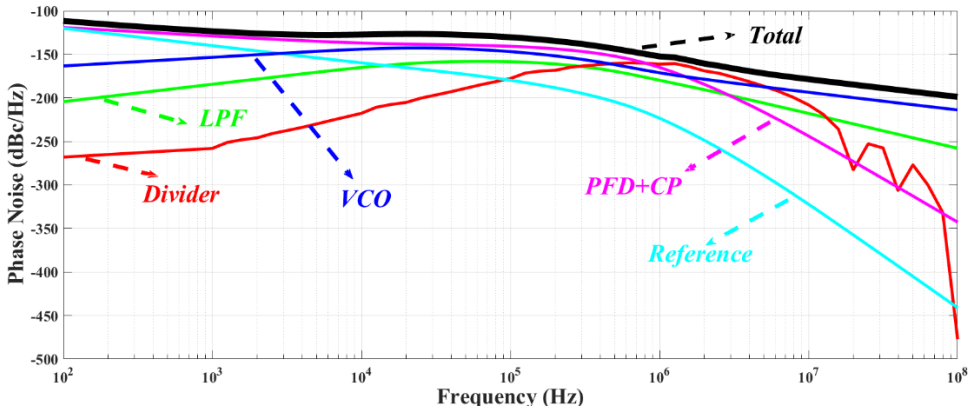


Figure 4-42 The behavioral simulations of the phase noise contributions of each block in Figure 4-37.

Table 4-6 The simulation results for the designed frequency synthesizer compared with the measurement results of the other literature.

Ref	[6]	[106]	[111]	[112]	This Work		
					IEEE 802.11a	U-NIII	IEEE 802.11b
Type	Fractional-N	Integer-N	Integer-N	Fractional-N	Fractional-N	Fractional-N	Fractional-N
[1]FR (GHz)	12.8-15.2	2-3	5.3-5.6	0.32-0.520	5-5.825	5.15-5.35	2.4-2.48
Ref. Frequency (MHz)	500	22.6	50	10	40	37.5	20
Power (mW)	19.8	4	19.8	2.7	3.9	4	3
RMS Jitter	66.2 (fs)	970 (fs)	NA	17.6 (ps)	**≈ 56 (fs)**	**≈ 41 (fs)**	**≈20 (fs)**
Phase noise (dBc/Hz) @ 10 KHz	-105.5	-95.22	-72	-84@200KHz	-94	-97	-115
@ 1 MHz	-115.7	-113.78	-114.28	NA	-117	-119	-128
@ 10 MHz	-126.22	-116.30	NA	NA	-125	-128	-148.7
Settling time (µs)	18.55	NA	20	NA	4	3	18
Fractional Spur (dBc)	-61	-62	NA	-36	-63	-63	-60
*FoM	-250.6	-234.1	NA	-210.9	**-259**	**-261.7**	**-269.2**
Process (CMOS)	28 nm	45 nm	180 nm	28 nm	180 nm	180 nm	180 nm
Supply (V)	0.9	1	1.8	0.9	1.8	1.8	1.8

*FoM = 10 log [(Jitter/1S)^2 . (Power/1mW)] [1]Frequency Range

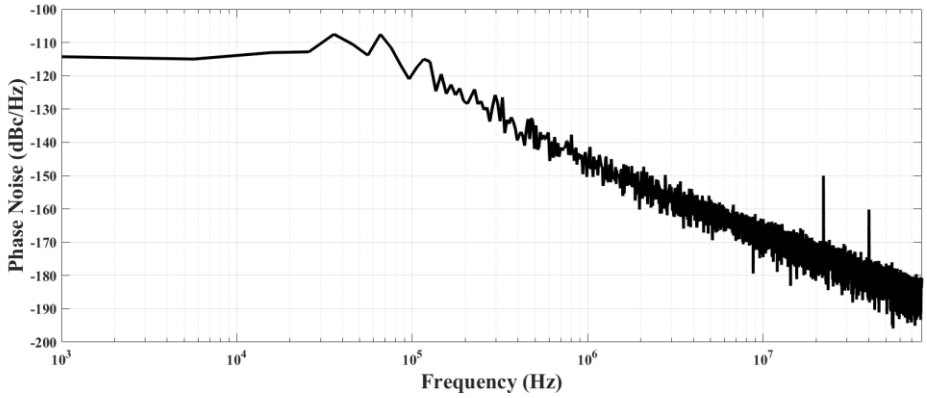


Figure 4-43 The frequency synthesizer phase noise for IEEE 802.11b standard at 2.4 GHz.

4.7 Conclusion

An analog phase-locked loop fractional-*N* frequency synthesizer for IoE applications (sub-6 GHz, which is a branch of 5G wireless communication standard) is provided in180 nm standard CMOS process. The proposed architecture uses several techniques in the frequency divider, such as a new divide-by-2/3 circuit, dynamic asynchronous resettable D and JK flipflops, AND & OR gates, and phase frequency detector (PFD) to improve the performance of the synthesizer.

Chapter 5 Conclusions and Future Work

This dissertation has mostly focused on the design of an analog fractional-N frequency synthesizer with low phase noise for IoT/IoE applications. In this chapter, we present the thesis outcomes in Section 5.1. Then, we will provide suggestions for future developments.

5.1 Thesis Outcomes

In Chapter 2, we studied phase noise deduction in cross-coupled oscillators. Based on the Hajimiri model, we showed that $1/f^2$ phase noise regions can be reduced by rising I_{RF} and V_{RF}, and minimizing $\Gamma_{M,rms}$ and $\Gamma_{T,rms}$. For $1/f^3$ phase noise regions, we provided some methods to diminish phase noise in this region, ranging from rising linearity, adding resistances, controlling the oscillation amplitude, decreasing the conduction angle, guiding the high-frequency harmonics of current, and shifting the phase of V_{GS} against V_{DS}. Finally, we concluded that cross-coupled oscillator can reach the best performances in $1/f^3$ and $1/f^2$ PN regions if the oscillator is designed in class C with the K block, and uses the techniques of narrowing conduction angle, the tail inductor, and the modified tank simultaneously.

In Chapter 3, with insights from Chapter 2 we designed and implemented a low-phase noise modified cross-coupled oscillator. In this oscillator, we added a K-block, which could improve the output voltage swing without increasing the current and power. We provided a large signal analysis to prove the oscillation amplitude increment. We also derived a closed-form formula of the phase noise in the $1/f^2$ region by Hajimiri's phase noise theory to optimize the oscillator performance in terms of phase noise.

In Chapter 4, we designed an analog fractional-N frequency synthesizer to cover 3 different bandwidths. The first bandwidth is from of 2.4 to 2.48 GHz, which can be used for IEEE 802.11b and Bluetooth. 5.15 to 5.35 GHz is the second bandwidth. This bandwidth can be used for U-NII standard. Finally, the last bandwidth is from 5.15 to 5.8 GHz. The IEEE 802.11a standard uses this bandwidth.

5.2 Future Work

Our suggestions for future research based on the research done in this thesis are as follows:

1) One can investigate different structures for the analog PLL building blocks in order to achieve better phase noise. For example, any mismatches between the output transistors in the charge pump can cause phase noise. Using different charge pump structures which utilize feedback can be helpful.
2) In this thesis we used an analog PLL for our synthesizer. However, All-digital PLLs (ADPPLs) have better performance in terms of area and power consumption than the analog counterparts. Ones can combine both analog and digital blocks to achieve better results. In ADPLLs, a time to digital converter (TDC) is used rather than the PFD and charge pump in analog PLLs. Therefore, if a TDC is used, we could save more power.
3) To have robust performance against process-temperature-voltage (PVT) variations, ones can exert low-dropout regulator (LDO regulator) for the supply voltages.

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Appendix A List of Publications Related to the Thesis Work

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