SIC-BASED SIX-PHASE TRACTION INVERTERS

DESIGN AND CONTROL OF A 100 KW SIC-BASED SIX-PHASE TRACTION INVERTER FOR ELECTRIC VEHICLE APPLICATIONS

BY

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Lay Abstract

Electric cars are continuously challenged to meet regulatory mandates that become stricter by the day. This is driven by the need for a clean, reliable, affordable, and sustainable transportation system. In this research, a novel, more reliable, and cost-effective power control unit (PCU) is proposed. The PCU manages the power flow regulation between the battery and the motor(s). The proposed PCU employs the same number of devices as a traditional counterpart, yet in a more modular architecture that doubles the safety factor compared to the standard design. In fault scenarios where the traditional PCU would fail, the proposed PCU would continue operating at half power, allowing the driver and passengers to reach a safe destination before the car is repaired. Extensive analyses were undertaken to identify an optimal design in terms of performance, size, and cost. Then, an engineering prototype is constructed and tested on an electric drivetrain testbed. Finally, the prototype is benchmarked against commercial competitors in the market to establish its economical feasibility.

Abstract

This thesis investigates the feasibility of using Silicon Carbide (SiC)-based multiphase inverters (MPIs) for transportation electrification applications. The research begins with a comprehensive review on the state-of-the-art of MPIs, focusing on voltage source inverters (VSIs) and nine-switch inverters (NSIs), with five-, six-, and nine-phase configurations. The quantitative and qualitative analyses demonstrate that the six-phase VSI is the most promising topology, offering reduced DC-capacitor requirements, lower cabling cost, and higher fault tolerance capability while maintaining the same efficiency and power device count of a three-phase VSI. The feasibility of the SiC-based six-phase inverter is further investigated at the vehicle level, where a vehicle model is developed to study the energy consumption under different drive cycles. The resulting indicate an 8% improvement in vehicle mileage and fuel economy of the SiC-based six-phase inverter compared to its Si-based counterpart.

This thesis also examines the current and voltage stresses on the DC-bus capacitor in two-level six-phase VSIs. The study considers two configurations of load/winding spatial distribution: symmetric and asymmetric. Consequently, analytical formulas for the DC-bus capacitor current and voltage ripples are derived. Furthermore, simple capacitor sizing rules in six-phase VSIs with different load configurations are

provided. The accuracy of the derived formulas is verified by simulation and experimental testing, and their boundary conditions are identified. Six-phase VSI supplying symmetric loads was found to yield the smallest capacitor size.

Based on the foregoing technology review and analyses, a holistic design methodology for a 100 kW SiC-based six-phase traction inverter for an electric vehicle application is presented. The proposed methodology considers the device power level, where discrete SiC MOSFETs are utilized, and the DC-capacitor sizing, where a multi-objective optimization algorithm is proposed to find the most suitable capacitor bank. Mechanical and thermal design constraints are also explored to deliver a compact housing with an integrated coolant channel. The resultant inverter design from the proposed electrical-thermal-mechanical design methodology is prototyped and experimentally tested, demonstrating a 7% reduction in DC-capacitor volume and 21% reduction in cabling cost when compared to conventional three-phase inverters of the same volt-ampere rating. The peak power density of the prototype inverter is 70 kW/L, demonstrating a compact design. Besides, the proposed design is benchmarked against commercial six-phase inverter models, whereby the competitiveness of the proposed design is highlighted.

Finally, the unique control aspects of six-phase electric motor drives are investigated to identify suitable controls strategies for various operating conditions. The study places special emphasis on high-speed operation and evaluates several overmodulation techniques. An adaptive flux-weakening control algorithm is also proposed for the six-phase motor drive, which significantly improves the DC-bus voltage utilization of the inverter when used in conjunction with overmodulation.

Overall, this thesis provides a comprehensive study of SiC-based six-phase traction

inverters and proposes a holistic design methodology that considers electrical, thermal, and mechanical aspects. The results demonstrate the feasibility and advantages of SiC-based six-phase traction inverters for electric vehicle applications.

To my wife

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Abbreviations and Nomenclature

Abbreviations

Al	Aluminum
ANL	Argonne National Laboratory
BD	Bidirectional
BSD	Belt Starter-Generator
CAD	Computer Aided Design
CB-PWM	Carrier Based Pulse Width Modulation
CF	Common-Frequency
CFD	Computational Fluid Analysis
CMV	Common Mode Voltage
CNC	Computerized Numerical Control
CSI	Current Source Inverter

DBC Direct Bonded Copper

DESAT Desaturation

DF Different-Frequency

DOE Department of Energy

DPT Double Pulse Test

DPWM Discontinuous Pusle Width Modulation

DSP Digital signal processor

DTP Dual Three-Phase

DUT Device Under Test

EM Electric Machine

EMC Electromagnetic Capability

EMF Electromotive Force

EMI Electromagnetic Interference

EPA Environmental Protection Agency

ESL Equivalent Series Inductance

ESR Equivalent Series Resistance

ETDS Electric Traction Drive System

EV Electric Vehicle

FEA	Finite Element Analysis
FW	Flux-Weakening
GaN	Gallium Nitride
GPIO	General-Purpose Input/Output
HCF	Harmonic Content Factor
HEMT	high electron mobility transistors
HEV	Hybrid Electric Vehicle
HV	High Voltage
IC	Integrated Circuit
ICE	Internal Combustion Engine
IEC	International Electrotechnical Commission
IGBT	Insulated Gate Bipolar Transistor
IMD	Integrated Motor Drive
IOs	Inputs/Outputs
IP	Ingress Protection
IPC	Institute for Printed Circuit
IPMSM	Interior Permanent Magnet Synchronous Motor
IR	Insulation Resistance

ISO International Organization for Standardization

JBD Junction Barrier Diode

JFET Junction Field Effect Transistor

KSS Keeping Switching State

KVL Kirchhoff's Voltage Law

LPF Low Pass Filter

LV Low Voltage

MDE Minimum Distance Error

MDP Multiphase drive

MEA More Electric Aircrafts

MIL Modulation Index Linearization

MLI Multilevel Inverter

MME Minimum Magnitude Error

MMPE Modified Minimum Phase Error

MOSFET Metal Oxide Silicon Field Effect Transistor

MPC Model Predictive Controller

MPE Minimum Phase Error

MPI Multiphase Inverter

MPMLI Multiphase Multilevel Inverter

MV Medium Voltage

NC Normally-Closed

NO Normally-Open

NPT National Pipe Thread

NSI Nine Switch Inverter

OEM Original Equipment Manufacturer

OVM Overmodulation

PCB Printed Circuit Board

PF Power Factor

PHEV Plug-In Hybrid Electric Vehicle

PI Proportional-Integral

PMSM Permanent Magnet Synchronous Motor

PR Proportional-Resonant

PS-PWM Phase-Shifted Pulse Width Modulation

PWM Pulse Width Modulation

RB Reverse Blocking

RCA Root Cause Analysis

RMS Root Mean Square

RMSE Root Mean Square Error

SAE Society of Automotive Engineers

SBD Schottky Barrier Diode

SiC Silicon Carbide

SRM Switched Reluctance Motor

SVM Space Vector Modulation

THD Total Harmonic Distortion

THI Third Harmonic Injection

TIM Temperature Interface Material

TTL Transistor-Transistor Logic

VA Volt-Ampere

VC Vector Classification

VR Voltage Regulation

VSD Vector Space Decomposition

VSI Voltage Source Inverter

WBG Wide Bandgap

XOR Exclusive OR logic gate

ZSI	Zero Sequence Injection

Nomenclature

δ	displacement angle between three phase sets
k	Number of subspaces of a multiphase system in vector space decomposition
$\underline{f}_{\alpha-\beta}$	A variable in stationary $\alpha-\beta$ subspace
$\underline{f}_{x_k-y_k}$	A variable in stationary $x-y$ subspace number k
$\underline{f}_{0_1-0_2}$	A variable in zero-sequence subspace 0_1-0_2
$\underline{f}_{d_k-q_k}$	A variable in rotating $d-q$ subspace number k
$I_{n-\phi}$	Phase current in an n-phase system
$I_{3-\phi}$	Phase current in a 3-phase system
E	Switch rated blocking voltage
C_{dc}	Capacitance of the dc-bus capacitor
M	Modulation index
$\hat{V}_1$	Peak fundamental-component of the phase voltage
V_{dc}	DC-bus voltage
M_{max}	Maximum modulation index

S_u, S_m, S_l	Upper, middle, and lower switch in the nine switch inverter topology
f_1	Fundamental line frequency
f_s	Switching frequency
i_{dc}	Input dc current
i_{inv}	Inverter input current
i_c	DC-bus capacitor current
v_c	DC-bus capacitor voltage
ϕ	Power factor angle
I_L	Load RMS current
$i_{A1,B1,C1,A2,B2,C2}$	Current of phase A1, B1, C1, A2, B2, and C2

Chapter 1

Introduction

1.1 Background

Recent years have seen an uptake of electrification in the automotive industry [1–3]. In 2019, we witnessed many original equipment manufacturers (OEMs) entering the electric market, and auto products extending beyond the standard passenger vehicle to include exotic cars [4]. Globally, sales of electric passenger vehicles have grown by over 60% per year since 2012 and are projected to exceed 70 million in 2025. As for Canada, the fourth largest car exporter in the world, more than half of all passenger vehicle sales are expected to be electric by 2030. This trend is only expected to grow into the future. Figure 1.1 shows the global long-term sales of passenger vehicles by drivetrain and region. It is projected that more than half of the global sales of passenger vehicles will be electric by 2040 [5]. This is driven by the need for clean, reliable, inexpensive and sustainable transportation system as global warming concerns continue to rise [3].

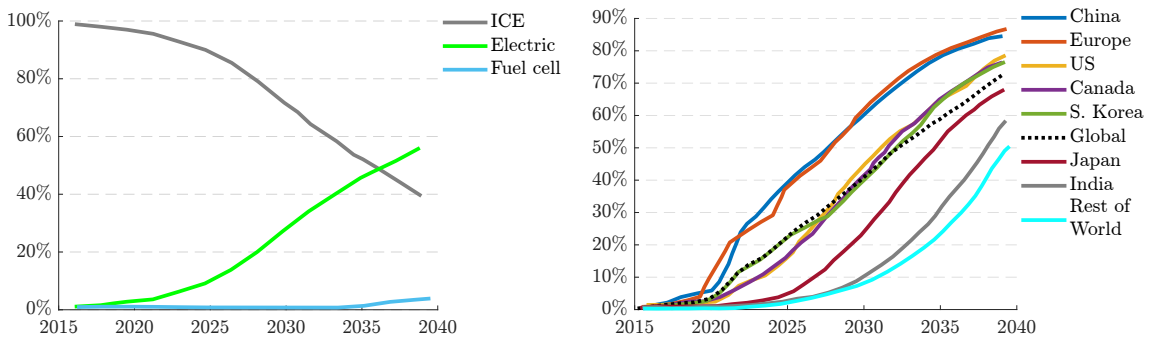


Figure 1.1: Global long-term share of passenger vehicle sales (a) by drivetrain, (b) by region (electric vehicle only).

Electrified vehicles include pure electric vehicles (EVs), hybrid EVs (HEVs), plug-in HEV (PHEV), and fuel cell vehicles, each having a different powertrain architecture [3]. The driving power of all electrified powertrains is always one or more electric machines (EMs) that operate either alone or in conjunction with an internal combustion engine (ICE) [2, 6, 7]. Driving and controlling the EM is achieved by a traction inverter, which converts the DC current drawn from the battery to a variable frequency AC current in motoring mode. Conversely, in generation mode, the inverter acts as a rectifier to transfer the energy from the EM to the battery. Accordingly, optimizing the efficiency, power density, control techniques, and cost is crucial for further development of EVs.

To accelerate the paradigm shift towards electrified transportation, regulatory mandates are becoming more stringent. In 2015, the U.S. Department of Energy (DOE) announced new targets, concerning the electric traction drive system (ETDS), to be met by 2025 [8]. A power density of 33 kW/L at \$6/kW is expected for a 100 kW traction drive system. Specifically, the power inverter module (referring to a single 100 kW inverter and, if applicable, a boost converter) is expected to achieve a

power density of 100 kW/L at a cost of \$2.7/kW. This constitutes an 87% and 18% reduction in volume and cost, respectively, compared to earlier targets set for 2020 [8]. Hence, disruptive innovative solutions are imperative to close in on the technology gap.

In the context of the traction inverter, research and development (R&D) efforts are focusing on a couple of frontiers. One promising frontier is the deployment of wide bandgap (WBG) devices, as an alternative to silicon (Si) devices. Over the past decade, WBG devices have gained a tremendous interest, owing to their superior material properties [9–19]. Normally, the term WBG is synonym with silicon carbide (SiC) and gallium nitride (GaN) semiconductor materials [20]. While both technologies are market-ready, the latter is limited to applications below 650 V [6, 17, 18, 21], and therefore, is not suitable for traction applications.

SiC devices offer a multitude of features that can be exploited to produce traction inverters with a significantly higher power density. Currently, the cost premium associated with SiC is a challenge for its wide adoption. Nonetheless, as SiC market share expands, and manufacturing techniques improve, the cost is expected to dramatically decline [16]. In fact, Tesla's Model 3 already employs a fully SiC traction inverter [22].

On a second frontier, multiphase drives (beyond three phases) for ETDS have been drawing the attention of OEMs in the automotive industry [23, 24]. The multiphase drive was first introduced in the late '60s of the past century [25]. Its popularity, though, had remained stagnant until the early 2000s. The major technological advancement in power electronics and microprocessors of this century provided the means to adopt such a technology thereafter. Multiphase drives offer many advantages

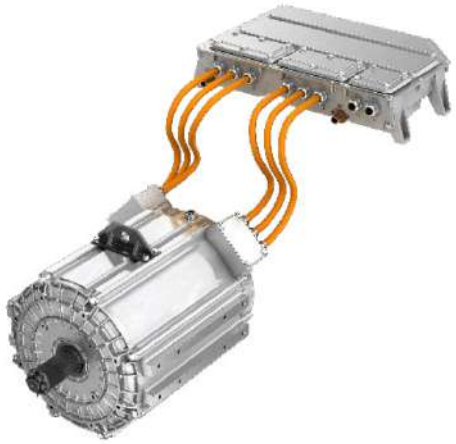


Figure 1.2: A Commercial 265 kW six-phase drive by Dana TM4 [24].

when compared to their three-phase counterparts, with two of particular interest to EVs: 1) reduced per-phase current rating, thus relaxing the requirements on employed semiconductors of the inverter, and 2) fault tolerance capability, which is of utmost importance to vehicle safety [26–29]. The first feature can complement the low-current-rated SiC devices. Figure 1.2 shows a commercial six-phase motor/inverter system designed for light- to medium-duty trucks.

1.2 Motivation

Extensive research has been conducted on the modeling [30], motor design [31], control [32], and fault-tolerance [33] of six-phase drives. However, the design of six-phase inverters is often overlooked. This originates from the notion that three-phase inverters can be extended to multiphase by mere addition of (half-bridge) switching legs [34]. Moreover, six-phase motors with two isolated neutrals are commonly referred to as dual three-phase motors [35]. As the name suggests, with respect to inverter construction, such motors can be driven by two three-phase voltage source

inverters (VSIs), resulting in a six-phase inverter that is typically oversized with switches rated at twice the rated current and two bulky DC-capacitor banks.

Therefore, it is imperative to have an elaborate design of six-phase inverters to achieve a compact and cost-effective solution. A thorough design should take advantage of the inherent benefits of six-phase systems such as lower torque ripple (in the case of an asymmetric motor) [36], reduction of DC-capacitor requirements [37], and reduced cabling costs [38]. It should also address the challenges such as higher numbers of sensors and gate drivers.

Dana TM4 offers commercial multiphase inverters (MPIs) for traction drives for light- to heavy-duty trucks [24]. The CO200-HV (depicted in Figure 1.2) and CO300-HV are MPIs dedicated for six- and nine-phase traction applications rated at 260 kW and 430 kW, respectively, for operating voltages less than 750 V. The employed semiconductor technology is not disclosed. The power density of both inverters, at the rated power, is smaller than 10 kW/L, which is not competitive when compared to state-of-the-art three-phase traction inverters [16]. Recently, Koenigsegg has released David, a 700 kW SiC-based six-phase inverter for its limited production PHEV, the Gemera [39]. The technical and commercial details of the inverter are not disclosed and, at the time of writing of this thesis, the Gemera was not in production yet [40].

This objective of this thesis is to design and develop a SiC-based six-phase traction inverter, while addressing the advantages and disadvantages of six-phase systems with respect to inverter design.

1.3 Contributions

This thesis has contributed to technical advances in six-phase traction inverters, including efficiency analysis, DC-capacitor sizing, controls, and electro-thermal inverter design, as well as their implementation in EV applications. The summary of these contributions is as follows:

1. State-of-the-art review on multiphase traction inverters and their technical and commercial feasibility in EV applications.

2. Comparative vehicle level efficiency evaluation of Si- and SiC-based six-phase traction inverters.

3. Current and voltage DC-ripples evaluation, harmonic analysis, and DC-capacitor sizing in six-phase inverters and benchmarking to three-phase counterparts.

4. DC-capacitor sizing rules for six-phase inverters based on maximum allowable current stress and voltage ripple.

5. Holistic electro-thermal-mechanical design of a SiC-based six-phase traction inverter.

6. Comprehensive evaluation of six-phase electric motor drive in terms of current control, flux-weakening, and overmodulation using two three-phase modulators.

1.4 Thesis Publications

Journal Articles

1. **W. Taha**, F. Juarez-Leon, M. Hefny, A. Jinesh, M. Poultan, B. Bilgin, and A. Emadi, "Design of a 100 kW SiC-based six-phase voltage source inverter for an electric vehicle application," *IEEE Transactions on Transportation Electrification*, under review.

2. **W. Taha**, P. Azer, A. Poorfakhraei, S. Dhale, and A. Emadi, "Comprehensive analysis and evaluation of DC-link voltage and current ripples in symmetric and asymmetric two-level six-phase voltage source inverters," *IEEE Transactions on Power Electronics*, vol. vol. 38, no. 2, pp. 2215–2229, Feb. 2023.

3. **W. Taha**, P. Azer, A. D. Callegaro, and A. Emadi, "Multiphase traction inverters: State-of-the-art review and future trends," *IEEE Access*, vol. 10, pp. 4580-4599, 2022.

4. J. Taylor, D. F. Valencia Garcia, **W. Taha**, M. Mohamadian, D. Luedtke, B. Nahid-Mobarakeh, B. Bilgin, and A. Emadi, "Dynamic modelling of multiphase machines based on the VSD transformation," *SAE International Journal of Advances and Current Practices in Mobility*, vol. 3, no. 4, pp. 1620–1631, Apr. 2021.

Conference Proceedings

1. F. Sun, W. Agnihotri, S. Dhale, S. Pradhan, **W. Taha**, and B. Nahid-Mobarakeh, "Digital sliding-mode-based xy-current suppression in dual three-phase PMSM

drives," in *2023 IEEE Applied Power Electronics Conference (APEC)*, Orlando, FL, 2023, pp. 1183–1188.

2. **W. Taha**, A. Jinesh, and A. Emadi, "On the feasibility of SiC-based multiphase traction inverters for EV applications: A case study," in IECON 2022 – 48th IEEE Annual Conference Industrial Electronics Society, Brussels, 2022, pp. 1–6.

3. **W. Taha**, P. Azer, and A. Emadi, "Harmonic analysis of input DC current in multiphase voltage source inverters," in *2022 IEEE Energy Conversion Congress & Expo (ECCE)*, Detroit, MI, 2022, pp. 1–6.

4. Z. Zhang, **W. Taha**, M. Mohamadian, B. Nahid-Mobarakeh, A. Emadi, "Overmodulation strategies for dual three-phase PMSM drives," SAE Technical Paper, 2022-01-0722, 2022.

5. **W. Taha**, D. F. Valencia, Z. Zhang, B. Nahid-Mobarakeh and A. Emadi, "Adaptive flux weakening controller for dual three-phase PMSM drives in vector space decomposition," in *IECON 2021 – 47th Annual Conference of the IEEE Industrial Electronics Society*, Toronto, Canada, 2021, pp. 1–6.

6. S. Absar, **W. Taha**, and A. Emadi, "Efficiency evaluation of six-phase VSI and NSI for 400V and 800V electric vehicle powertrains," in *IECON 2021 – 47th IEEE Annual Conference Industrial Electronics Society*, Toronto, 2021, pp. 1–6.

7. **W. Taha**, B. Nahid-Mobarakeh, and J. Bauman, "Efficiency evaluation of 2L and 3L SiC-based traction inverters for 400V and 800V electric vehicle powertrains," in *2021 IEEE Transportation Electrification Conference and Expo (ITEC)*, Chicago, IL, 2021, pp. 625–632.

1.5 Thesis Outline

The organization of this thesis is as follows. Chapter 2 provides a comprehensive review of MPIs and their application in transportation electrification, with a focus on the VSI and nine-switch inverter (NSI) topologies due to their popularity and potential as traction inverters. The state-of-the-art review covers topics such as modeling and control techniques, DC-capacitor sizing, modulation strategies, inverter losses, and cost. Promising future trends in MPIs are also investigated.

In Chapter 3, a quantitative and qualitative analysis is conducted to examine the feasibility of SiC-based multiphase traction inverters. VSI and NSI topologies with different phases (five-, six-, and nine-phase) are evaluated in terms of device count, DC-capacitor sizing, efficiency, power density, and cost. The six-phase VSI is found to have the best feasibility, offering reduced DC-capacitor requirements, lower cabling cost, and higher fault tolerance capability while maintaining the same efficiency and power device count.

The feasibility of the SiC-based six-phase inverter is further investigated at the vehicle level in Chapter 4, where a dynamic powertrain model comprising the inverter and motor is developed to evaluate efficiency and energy consumption under different drive cycles. Furthermore, an EV model is developed to study the energy consumption under the different traction inverters at different drive cycles. The resulting data provides valuable insights into the performance of the SiC-based six-phase inverter compared to its Si-based counterpart, including vehicle mileage and fuel economy.

Chapter 5 examines the current and voltage stresses on the DC-bus capacitor in two-level six-phase VSIs. Analytical formulas for the DC-bus capacitor voltage ripples and sizing for six-phase VSIs with different load/winding spatial distribution

are derived, and their accuracy is verified by simulation and experimental testing. Six-phase VSI supplying symmetric loads was found to yield the smallest capacitor size.

In Chapter 6, a holistic design methodology for a 100 kW SiC-based six-phase traction inverter for electric vehicle applications is presented. The proposed methodology considers the power device level, where discrete SiC MOSFETs are utilized, and the DC-capacitor level, where a multiobjective optimization algorithm is proposed to find the most suitable capacitor bank. Mechanical and thermal design constraints are also considered to deliver a compact housing with an integrated coolant channel. The resultant inverter design is prototyped and experimentally tested in Chapter 7, demonstrating a 7% reduction in DC-capacitor volume and 21% reduction in cabling cost compared to three-phase inverters of the same rating. The peak power density of the prototype inverter is 70 kW/L, demonstrating a compact design.

In Chapter 8, the unique control aspects of the six-phase electric motor drives are investigated. More specifically, control and overmodulation techniques for operation beyond the base speed are proposed. An adaptive flux-weakening control algorithm is proposed using the vector space decomposition modeling to be seamlessly integrated in the six-phase field-oriented control. Overmodulation techniques based on three-phase modulators are investigated for employment in six-phase drives. Based on this investigation, a simpler overmodulation technique with superior performance characteristics is also proposed.

Finally, Chapter 9 outlines the conclusions drawn from this thesis. Additionally, potential directions for future research and development are suggested.

Chapter 2

Fundamentals of Multiphase Traction Inverters

Extensive efforts are being invested in optimizing the efficiency, power density, and cost of traction inverters. Such efforts are in line with the next-generation framework of electrified transportation that includes increased voltage and power ratings [41] and employment of WBG devices [13].

At the heart of traction inverters are power semiconductor devices, whose ratings might be limited in the face of the aforementioned trends. When voltage is a limiting factor, multilevel inverters (MLIs) constitute a viable solution [42]. MLIs are able to utilize switching devices with lower voltage ratings for the same or higher DC-bus voltages when compared to two-level inverters. Thereby, their application in power-trains rated at and beyond 800 V is gaining a a significant attention [43]. On the other hand, when current is a limiting factor for the semiconductor devices, discrete device paralleling is the industry-accepted solution; multiple devices are connected in parallel to withstand the output current of the inverter. Tesla's Model 3 (2018),

for example, employs four SiC discrete metal oxide semiconductor field effect transistor (MOSFET) devices per switch [44]. However, device paralleling poses design challenges pertaining to static and dynamic current sharing among the paralleled devices [45–48]. Mismatches between the paralleled devices lead to current unbalance, which in turn causes hot spots [47].

Alternatively, multiphase drives (MPDs), beyond three phases, thrive in delivering high-power, owing to their improved per-phase current handling [29]. With more phases to share the required output power, device paralleling issues are alleviated, or eliminated altogether [49]. Besides improved current handling, MPDs offer improved fault tolerance capability, lower torque pulsations, better noise characteristics, and modularity [28, 29].

Whether to use a multilevel inverter or a multiphase drive is a subtle question, and rather application-oriented. Increasing the powertrain voltage rating is attractive for EVs as it enables fast charging and reduces cabling footprint. On the other hand, it compounds insulation requirements. Improper insulation leads to partial discharge, which in turn causes machine failures [50]. This poses a serious threat for more electric aircrafts (MEA), for example, where reliability is of utmost importance. In such applications, meeting high power demand can be achieved by increasing the current supply at a relatively low voltage, around 400 V [51]. Heavy-duty vehicles resemble another example of high-power electrified powertrain. In such cases, MPDs are more suitable, thanks to their reduced per-phase current requirements. From another perspective, electrified aircrafts can also exploit MPDs to leverage reliability as multiphase drives have superior fault-tolerance capabilities. Figure 2.1 summarizes the pros and cons of MPIs.

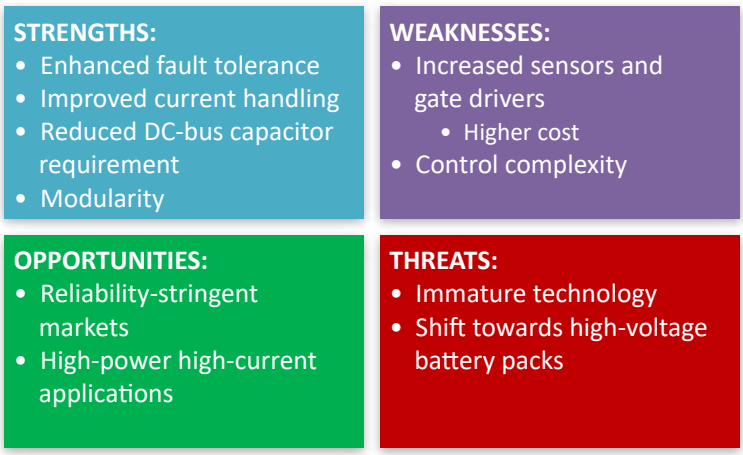


Figure 2.1: Strengths, weaknesses, opportunities, and threats (SWOT) analysis of MPIs.

Both technologies, MLI and MPI, have been widely investigated in literature. Application of MLIs in transportation electrification was recently reviewed in [42]. MPDs for traction applications was reviewed [29], with a focus on six-phase drives. A little attention, though, has been paid to MPIs. This arises from the notion that conventional three-phase inverters are extendable to MPIs by simply adding additional switching legs to the existing ones [34]. Another reason is the modularity of six-phase machines with two isolated neutrals, which can be treated as two three-phase sets, commonly known as *dual three-phase* machines [35]. In principle, for n-phase machine with n multiples of three, the system can be decomposed into $n/3$ three-phase systems [52]. Thus, as far as hardware implementation is concerned, these machines can be driven by multiple three-phase inverters. While such reasoning is valid, the resulting MPI is usually oversized with switches rated at twice the rated current and two DC-bus capacitors, in the case of six-phase drives.

Proper considerations invested in MPI design can yield improved inverter design.

Along with addressing the aforementioned device paralleling issues, input parasitic can be made smaller, thanks to improved current handling in MPIs. Therefore, a higher power density can be achieved. To this end, this thesis presents an in-depth review of MPIs for traction applications. More specifically, two MPI topologies are reviewed: VSI and NSI. The selection of those topologies is based on their potential for the applications listed in Figure 2.1.

This chapter is organized as follows. Modeling techniques for MPIs are discussed in Section 2.1. Sections 2.2 and 2.3 review multiphase VSI and NSI, respectively. Section 2.4 investigates the future trends for MPIs and the challenges hindering their adoption. Finally, Section 2.5 concludes the chapter.

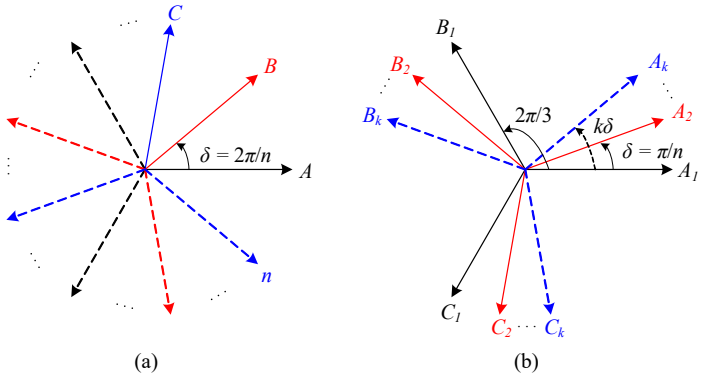


Figure 2.2: General phase distribution in n-phase inverters for different spatial displacement configurations. (a) Symmetric: $\delta = 2\pi/n$. (b) Asymmetric: $\delta = \pi/n$, $k = (n-3)/3$ for n multiples of 3.

$$\begin{bmatrix} \underline{f}_{\alpha-\beta} \\ \underline{f}_{x_1-y_1} \\ \vdots \\ \underline{f}_{x_k-y_k} \\ \underline{f}_{0_1-0_2} \end{bmatrix} = \frac{2}{n} \underbrace{\begin{bmatrix} 1 & a & a^2 & a^3 & \cdots & a^{(n-1)} \\ 1 & a^2 & a^4 & a^6 & \cdots & a^{2(n-1)} \\ \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ a^{(k+1)} & a^{2(k+1)} & a^{3(k+1)} & a^{4(k+1)} & \cdots & a^{(k+1)(n-1)} \\ b & b^7 & b & b^7 & \cdots & b \end{bmatrix}}_{\mathbf{T_{VSD}}} \begin{bmatrix} f_A \\ f_B \\ \vdots \\ f_n \end{bmatrix}, \quad \begin{aligned} a &= e^{j2\pi/n} \\ b &= e^{j\pi/4} \end{aligned} \tag{2.0.1}$$

2.1 Modeling of Multiphase Inverters

The spatial displacement between the phases, δ can be symmetric or asymmetric. For symmetric systems, each two consecutive phases are $\delta = 2\pi/n$ apart. Asymmetric distribution is exclusive to n-phase system where n is a multiple of three. In this case, the system is composed of $n/3$ multiples of three-phase systems with a displacement of $\delta = \pi/n$ between each three-phase set. Figure 2.2 depicts the general phase distribution for symmetric and asymmetric MPIs.

Modeling of MPIs is an n-dimensional problem. There are two main methods to model n-phase inverters, namely vector space decomposition (VSD) and multiple dq. The two modeling approaches are reviewed in this section for multiphase inverters, in addition to the general structure of the current control loop based on such approaches.

2.1.1 Vector Space Decomposition

The VSD technique is applicable to any n-phase system and any spatial displacement configuration. It decomposes the n-dimensional system into multiple orthogonal 2D planes or subspaces [53]. For example, the vectors in six-phase inverter—six-dimensional—are mapped into three two-dimensional subspaces, namely α–β, x–y, and 0_1–0_2. Clarke's transformation is extended to n-phase to yield a single transformation matrix for the multiphase space. The VSD transformation is equally applicable for symmetric and asymmetric MPIs. The power-invariant VSD transformation, in the complex vector form, for symmetric n-phase MPI is given in (2.0.1), where $\underline{f}_{\alpha-\beta} = f_\alpha + jf_\beta$ and f can be any n-phase variable, e.g. voltage or current. Similarly, f_X, $X \in \{A, B, \ldots, n\}$ is the X-phase variable in the stationary $ABC\ldots n$ frame.

The vector mapping is selected in such a way that the fundamental component

is mapped into the α–β plane, whereas low order harmonics and zero-sequence components are mapped into the x–y and 0_1–0_2 planes, respectively. Applying the VSD transformation to MPIs with $n > 6$ yields multiple x_k–y_k planes, $k \in [1, 2, ..]$. A general formulation for k in terms of n cannot be established. Five- and Six-phase MPIs have a single x–y plane, while seven- and nine-phase MPIs have two x-y planes [26,54]. Additionally, applying VSD transformation to MPIs with odd number of phases, n, produces a single zero-sequence component ($0_2 = 0$), whereas two zero sequence components are produced in inverters with n even phases [55]. A special case, however, is asymmetric MPIs with $3j, j \in [1, 2, ...]$ isolated neutrals. In such a configuration, all the vectors in 0_1–0_2 are mapped at the origin, thus, nullifying the zero-sequence subspace [30]. Table 2.1 summarizes the harmonic mapping of the VSD transformation in the 2D orthogonal subspaces for five-, six-, seven-, and nine-phase MPIs.

Table 2.1: Harmonic mapping into different planes using VSD transformation for multiphase systems ($k = 0, 1, 2, 3 \ldots$, $m = 1, 3, 5 \ldots$)

Plane	**5-Phase**	**6-Phase**	**7-Phase**	**9-Phase**
α–β	$10k \pm 1$ (1,9,11...)	$12k \pm 1$ (1,13,25...)	$14k \pm 1$ (1,13,15...)	$18k + 1$ (1,19,37...)
x_1–y_1	$10k \pm 3$ (3,7,13...)	$6m \pm 1$ (5,7,17...)	$14k \pm 5$ (5,9,19...)	$18k + 17$, $8m \pm 4$ (5,13,17...)
x_2–y_2	—	—	$14k \pm 7$ (3,11,17...)	$9k \pm 2$ (7,11,25...)
Zero sequence	$5(2k + 1)$ (5,15,25...)	$3(2k + 1)$ (3,9,15...)	$7(2k + 1)$ (7,21,35...)	$3(2k + 1)$ (3,9,15...)

2.1.2 Multiple d–q

Known in the literature as double d–q for six-phase inverters [29], the notion is extended herein to *multiple* d–q for MPIs with n multiples of three. Alternative to the VSD modeling, which treats the n-dimensional space as one, the multiple d–q decomposes the system into multiples of three-phase systems [56]. While multiple d–q is applicable to symmetric and asymmetric spatial distributions, it is only famous for the latter in the literature.

Each three-phase set is transformed using Clarke's and Park's transformation. The stationary frames, α_k–β_k obtained from Clarke's transformation are transformed into the rotational frame using Park's transformation with a phase shift of $k\delta$, $k \in [1, 2, ..., (n-3)/3]$. In this case, the same Clarke's transformation is used for all α_k–β_k frames. Thus, the transformations can be defined as:

$$\begin{aligned}
\begin{bmatrix} f_{\alpha 1} & f_{\beta 1} \end{bmatrix}^T &= \mathbf{T_3} \begin{bmatrix} f_{A1} & f_{B1} & f_{C1} \end{bmatrix}^T \\
\begin{bmatrix} f_{\alpha 2} & f_{\beta 2} \end{bmatrix}^T &= \mathbf{T_3} \begin{bmatrix} f_{A2} & f_{B2} & f_{C2} \end{bmatrix}^T \\
&\vdots \\
\begin{bmatrix} f_{\alpha k} & f_{\beta k} \end{bmatrix}^T &= \mathbf{T_3} \begin{bmatrix} f_{Ak} & f_{Bk} & f_{Ck} \end{bmatrix}^T
\end{aligned}, \tag{2.1.1}$$

$$\begin{aligned}
\underline{f}_{d1-q1} &= e^{j\theta} \underline{f}_{\alpha 1-\beta 1} \\
\underline{f}_{d2-q2} &= e^{j(\theta+\delta)} \underline{f}_{\alpha 2-\beta 2} \\
&\vdots \\
\underline{f}_{dk-qk} &= e^{j(\theta+k\delta)} \underline{f}_{\alpha k-\beta k}
\end{aligned}, \tag{2.1.2}$$

$$\mathbf{T}_3 = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \tag{2.1.3}$$

where $\theta \in [0, 2\pi]$ is the angular position. The resulting d-q frame is considered to be the sum of all d_i-q_i components, i.e. $f_{d,q} = f_{d1,q1} + f_{d2,q2} + \cdots + f_{dk,qk}$.

2.1.3 Vector-Oriented Control

Figure 2.3 depicts the general structure for the current control of MPIs using VSD and multiple d-q modeling techniques. In VSD (Figure 2.3a), the n-phase currents are

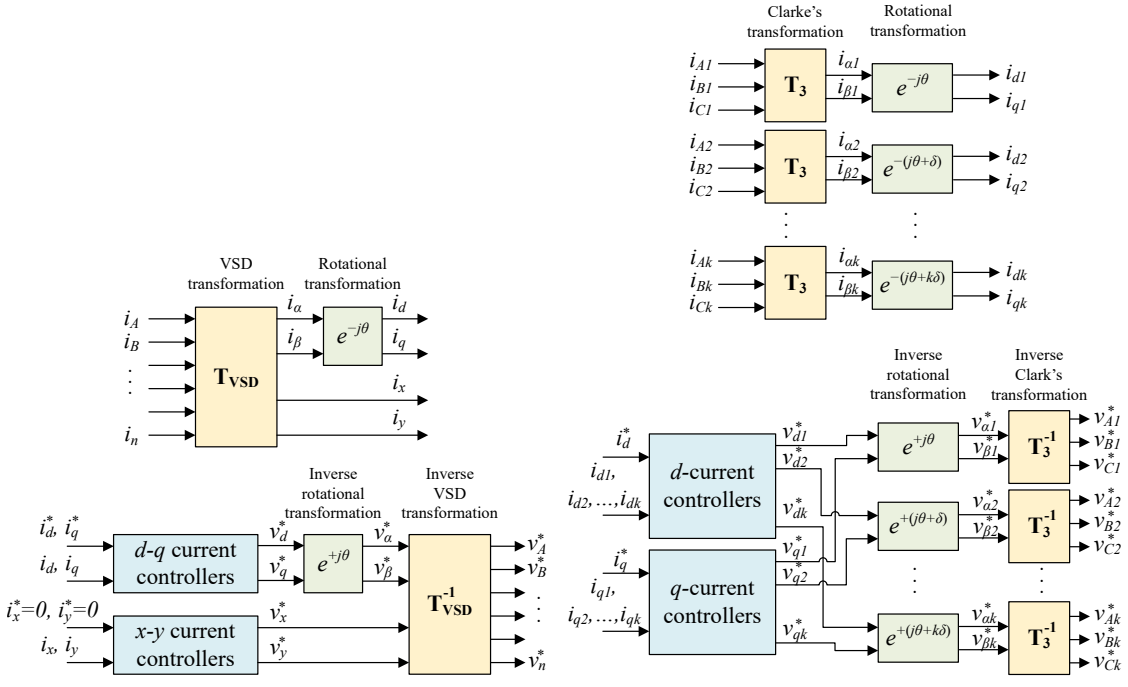


Figure 2.3: General current control structure of MPIs using the two different modeling techniques. (a) VSD modeling: $\mathbf{T_{VSD}}$ is given in (2.0.1). (b) Multiple d–q modeling: $\mathbf{T_3}$ is Clarke's transformation, $\delta = \pi/n$ and $k = (n-3)/3$ for n multiples of 3.

transformed into the stationary frame using $\mathbf{T_{VSD}}$ in (2.0.1). Only the α-β frame is transformed to the synchronous d-q frame using Park's transformation, whereas current components in the x_i-y_i, $i = 1, 2, ..., k$ are controlled in the stationary frame. Since the latter components carry the undesired harmonics, they are controlled to zero. The employed controllers can be proportional-integral (PI), proportional-resonant (PR), a combination of both [57], or model predictive controller (MPC) [58]. The output of the current controllers, i.e. reference voltages, are mapped back to phasor quantities using inverse transformations. The reference phase voltages are then used to generate the switching pulses. Note that an additional zero-sequence controller(s) is required when the n-phase inverter is connected to a single neutral point [36].

Current control in multiple d–q (Figure 2.3b) is straightforward. Currents are transformed into multiple d-q frames using Clarke's and Park's transformations given in (2.1.1) and (2.1.2), respectively. Each $i_{di,qi}$ ($i \in [1, 2, ..., k]$, $k = (n-3)/3$) is controlled to a reference d- and q-axis current, $i^*_{d,q}$.

The number of required controllers in both modeling techniques is usually the same, regardless of spatial distribution (Figure 2.2). For example, for a six-phase inverter with two isolated neutrals, four PI controllers are required in the VSD to control d-, q-, x-, and y-currents. In multiple d–q, the same controllers regulate d_1-, q_1-, d_2-, and q_2-currents. A similar performance can be achieved using both modeling techniques when the system is balanced [56]. However, multiple d–q is unable to correct for system asymmetries such as magnitude unbalance or inverter dead-time compensation. This is because the contribution of each d–q subspace to such asymmetries is usually undetermined. In this case, current control in VSD is superior as xy-currents can be exploited to correct for system asymmetries [57].

Furthermore, from drives perspective, integration of existing three-phase controls, such as flux-weakening, is seamless in VSD since the MPD is treated as a single system in the synchronous dq-frame [59, 60]. For such attributes, in addition to generality, VSD modeling is favored over multiple d–q. Table 2.2 summarizes the comparison between VSD and multiple d–q modeling.

After establishing the modeling techniques and the general vector control structure of MPIs, the most relevant MPI topologies are reviewed next.

2.2 Multiphase Voltage Source Inverter

Owing to its simplicity, high efficiency and low cost, VSI is the most commonly used inverter topology in transportation electrification applications [61]. This holds true irrespective of the number of phases, n or the type of the load machine [34]. Nevertheless, multiphase VSIs have distinctive attributes that distinguish them from

Table 2.2: Comparison between VSD and multiple d–q modeling for MPIs

Modeling Technique	**VSD**	**Multiple d–q**
Applicable to	any n	n multiple of 3
Physical interpretation of subspaces	Fund. & low-order harmonics	Contributions of fund. component from each 3-ph set
Asymmetry compensation	Yes	No
Integration of 3-ph control techniques	Simple	Complex
Specific modulation schemes	n-dimensional SVM	Vector classification

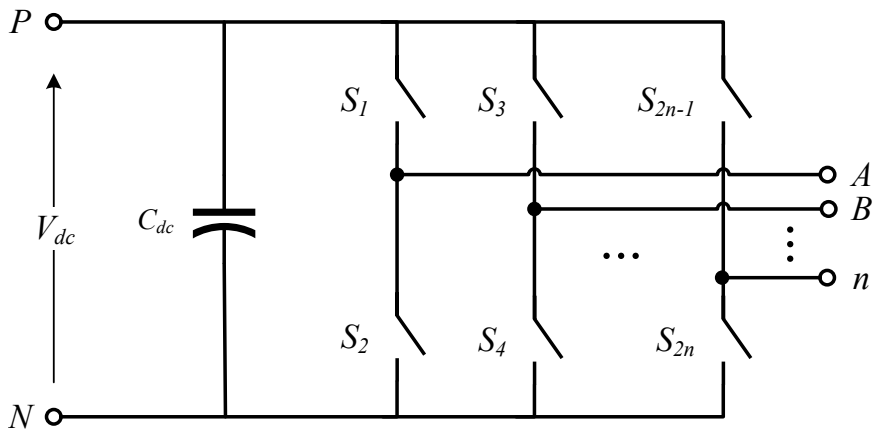


Figure 2.4: Multiphase voltage source inverter (VSI).

their conventional three-phase counterpart, such as DC-bus capacitor sizing and modulation techniques. The remainder of this section reviews such features.

2.2.1 Topology

Figure 2.4 depicts the two-level (2L) multiphase VSI topology with n number of phases. For traction applications, Si insulated gate bipolar transistor (IGBT) and SiC MOSFET are the two most commonly used devices, with a breakdown voltage range of 600 V – 1700 V [6,16]. The DC-bus capacitor is an indispensable component in VSI as it reduces voltage fluctuations and current ripples [62]. The VSI is known for its high efficiency and low cost, however, it suffers some drawbacks. Firstly, the VSI exhibits a buck behavior where the output voltage level is lower than the DC-bus voltage. Secondly, for high power applications, multiple power semiconductor devices are usually paralleled per switch, which poses design challenges as will be discussed next. Thirdly, the DC-bus capacitor is bulky and has a limited operating temperature range. In fact, it is the bottleneck in the face of achieving higher power densities as it

occupies up to two thirds of the total volume of the inverter [29, 63]. While the first drawback is inherent in the VSI topology, multiphase VSIs alleviate the foregoing challenges as discussed next.

2.2.2 Per-Phase Requirements

One of the most notable features of MPIs is the reduced per-phase current. The phase current of MPIs can be defined with respect to their three-phase counterpart as:

$$I_{n-\phi} = \frac{3}{n} I_{3-\phi}, \quad n \geq 3 \tag{2.2.1}$$

The reduction in per-phase current in MPIs with respect to three-phase VSI is depicted in Figure 2.5. The higher the number of phases the lower the per-phase current requirement is. However, this trend exhibits a diminishing return where at a certain point the reduction in per-phase current is no longer appreciated in the face of increased complexity. On the other hand, n-phase MPIs have, in large part, the same cost, owing to the same volt-ampere (VA) rating. The inverter VA rating reflects the power rating of the semiconductor switches, which in turn drives the cost in large part [64, 65]. The VA rating is given based on the per-unit voltage stress, E and the per-unit current stress, I, multiplied by the total number of switches, k. Note that E is the rated blocking voltage of the switches and is equal to V_{dc} for 2L MPIs. Since there are two switches per leg in an n-phase VSI (i.e. $k = 2n$), the VA rating can be defined as:

$$VA = (2n) \times E \times I_{n-\phi} \tag{2.2.2}$$

Substituting (2.2.1) in (2.2.2) yields $6EI$, irrespective of n.

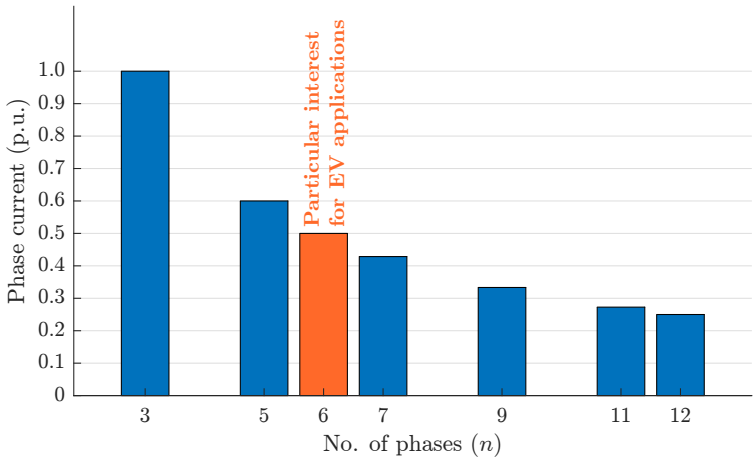


Figure 2.5: Reduced per-phase current requirement in MPIs.

The significance of the reduction in per-phase requirements is twofold. Firstly, it enables the use of smaller and lighter cables. The considerable reduction in cable size outweighs the increase in number of cables rendering a lower cost overall. This is demonstrated in Table 2.3, where AC cable sizing and pricing is calculated based on a 100 kW, 0.8 power factor (PF), and 230 V system for MPIs with $n \geq 3$. Compared to the conventional three-phase VSI, a six-phase VSI yields a 21% reduction in cabling cost.

Secondly, the reduction in per-phase current mitigates the current limitation of the employed power semiconductor devices, especially SiC MOSFET. As of this writing, the maximum current rating of commercially available, automotive-grade discrete SiC MOSFETs is around a 100 A (see Table 7 in [6]). This limitation renders paralleling of multiple discrete devices in three-phase inverters inevitable. Tesla's Model 3 (2018), for example, employs four discrete SiC MOSFET devices per switch [22, 44]. Device paralleling makes the design of gate drivers more challenging to ensure proper dynamic and static current sharing among the paralleled devices [46–48]. Mismatches among

Table 2.3: AC cable sizing and cost for MPIs to deliver 100 kW at 230 VAC and 0.8 PF (length ≤ 10 m)

n	Per-Phase Current (A)	Cable Size (AWG)[†]	Cable Unit Price (USD/m)[‡]	Total Price (USD/m)
3	181	1	36.9	110.8
5	109	4	21.2	105.8
6	91	6	14.6	87.4
7	78	6	14.6	101.9
9	60	8	10.1	91.2

[†]Calculated using the online tool in [66] based on IEC 60364-5-52 standard for Copper conductor

[‡]Based on shielded single-core motor cables from Igus® [67]

the paralleled devices lead to current unbalance, which in turn causes localized over-temperature [47]. According to [48], ON-state resistance, $R_{DS(\mathrm{ON})}$, pinch-off voltage (which determines at what gate voltage the device enters forward conduction mode), reverse breakdown voltage of the gate, transconductance, and device placement on the circuit are all factors that should be carefully monitored/designed to ensure proper operation of the paralleled devices.

2.2.3 DC Capacitor Requirement Reduction

Multiphase VSIs offer reduced capacitor requirements in terms of capacitance and physical volume [63]. The DC-bus capacitance, C_{dc} is determined based on the allowable DC-voltage ripple (typically 5%) [68]. It was shown in [63] that the required C_{dc} decreases with increasing phase number. A 50% capacitance reduction can be achieved in six-phase VSI. Additionally, the DC-voltage ripple is inversely proportional with C_{dc} and switching frequency. This means that the same voltage ripple can be achieved with a lower C_{dc} and higher switching frequency using SiC

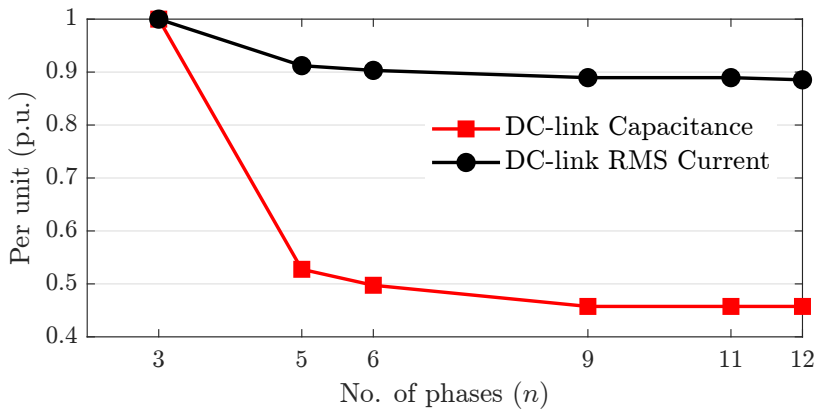


Figure 2.6: Normalized DC-bus capacitor requirements for multiphase VSI with different phase number, n in terms of capacitance and RMS current using SPWM [63].

devices. The volume of the DC-bus capacitor, on the other hand, is dictated by the DC-bus root mean square (RMS) current [52, 68–71], which depends on a couple of factors including modulation technique, modulation index, and PF. Similarly, the increased number of phases can decrease the DC-bus RMS current, but the reduction is not as appealing. Yet, since the DC-bus capacitor can take up to two thirds of the total volume of the traction inverter [29], even a small reduction is appreciated nonetheless. A 10% reduction in the DC-bus RMS current for $n \geq 6$ was demonstrated in [63]. Figure 2.6 illustrates the reduction in the C_{dc} and DC-bus RMS current for multiphase VSI with different n, with respect to three-phase VSI.

2.2.4 Modulation

The basic PWM modulation techniques of three-phase systems are extendable to multiphase inverters. The majority of available techniques, irrespective of inverter topology, can be classified into two groups: carrier-based PWM (CBPWM) and space vector modulation (SVM) [72], which are discussed in this subsection. Figure 2.8

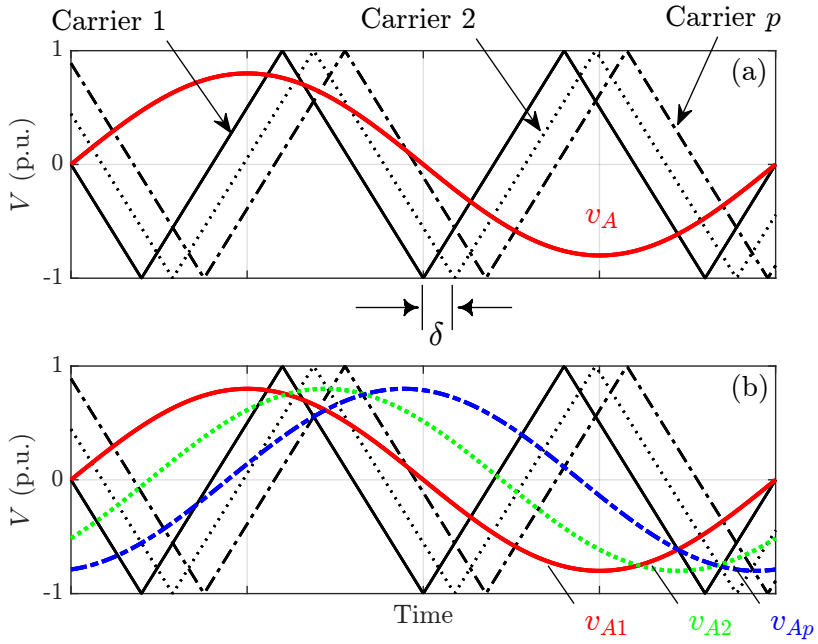


Figure 2.7: Interleaved CBPWM techniques for n-phase inverter where $n = p \cdot m$ is a multiple of three and $m = 3$. (a) Three-phase modulating signals, $m = 3$ with p carriers. (b) n-phase modulating signals, $p \cdot m = n$ and p carriers.

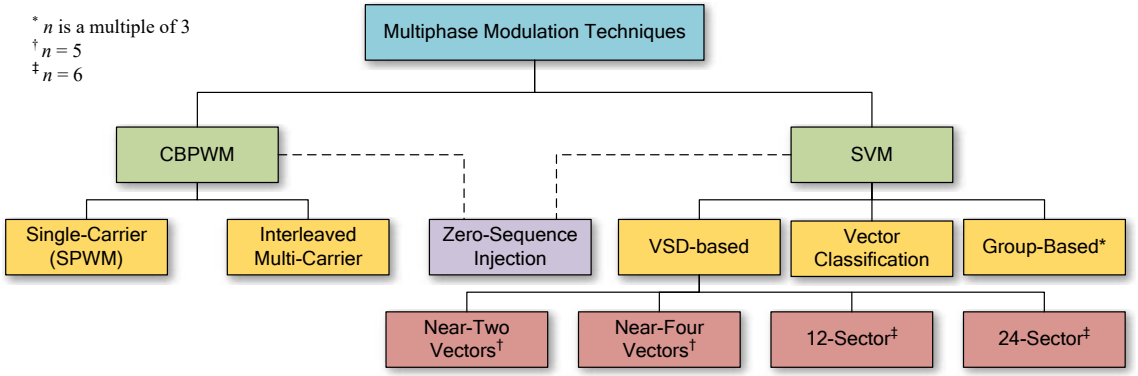


Figure 2.8: Classification of modulation techniques for multiphase inverters.

depicts the classification of the most common modulation techniques for multiphase VSI.

CBPWM

CBPWM is the most favorable technique for multiphase inverters. This is due to the high number of permissible states in SVM that incurs a heavy computational burden. Furthermore, a comparison between CBPWM and SVM in 2L seven-phase VSI in [73], in terms of voltage and current total harmonic distortion (THD), concluded that both techniques exhibit a similar performance. Hence, CBPWM is deemed a simpler yet effective technique for multiphase systems. Similar to three-phase inverters, the carrier is either a periodic triangular or sawtooth signal that control the gating signals when compared to n number of modulating sinusoidal signals, for multiphase VSI with n-phases. The CBPWM with a single carrier is commonly known as sinusoidal PWM (SPWM). Unlike three-phase VSIs, the additional legs in multiphase inverters provide an additional degree of freedom to address PWM-associated issues. For example, CBPWM techniques that reduce the common-mode voltage (CMV) in five-phase VSI were suggested in [74, 75].

Extension beyond the traditional SPWM to interleaved multi-carrier techniques for multiphase inverters have been suggested for n multiples of three. In interleaved multi-carrier PWM, the n phases are divided into p groups of m phases, $n = p \cdot m$. A multiple of p carriers, shifted by δ degrees, can be used to modulate $m = 3$ signals to generate the gate pulses for n switches, as shown in Figure 2.7a. This strategy was implemented and reported in [76] on a 15-phase inverter. Implementation of such interleaving technique in [77] resulted in a 60% volume reduction in the DC-bus capacitor for a 55 kW six-phase inverter. However, this strategy is only limited to a segmented MPD[1] and reduces the n-dimensional control to 3-dimensional. In

[1]Motor drive segmentation is to segment inverter switches and motor windings to form multiple parallel connected three-phase drive units

other words, some degrees of freedom are lost. Alternatively, the same p carriers can be used to modulate the n phases, as shown in Figure 2.7b. Furthermore, phase-shifted PWM (PS-PWM) with n number of carriers, with δ phase shift between two consecutive carriers, was proposed in [78] for five- and six-phase 2L VSI in order to reduce the CMV. However, the high number of carriers increases the computational time dramatically.

Despite its simple implementation, CBPWM suffers low DC-bus voltage utilization. The maximum level of DC-bus utilization is determined by the modulation index, M. The M is defined as the ratio of the peak fundamental-component of the phase voltage, $\hat{V}_1$ to one half of V_{dc}:

$$M = \frac{\hat{V}_1}{0.5V_{dc}} \tag{2.2.3}$$

In linear modulation region, the maximum output voltage is $0.5V_{dc}$ (i.e. $M_{max} = 1$), regardless of the number of phases [73]. CBPWM techniques in conjunction with zero-sequence injection (ZSI) were proposed for multiphase inverters in order to improve the DC-bus utilization [79], increase the torque density [80], and reduce output distortion [81]. Analogous to third-harmonic injection in three-phase VSI, n^{th} harmonic injection for multiphase VSI with n odd phases was suggested in [79]. The M_{max} for n odd number of phases is defined as [82]:

$$M_{max} = \frac{1}{\cos\left(\pi/2n\right)}, \quad n \in \{3, 5, 7, \dots\} \tag{2.2.4}$$

For example, 5^{th} harmonic injection in CBPWM for five-phase 2L VSI results in 5.15% increase in output fundamental voltage, making it equal to that of SVM. A

Table 2.4: Percentage increase in maximum modulation index in multiphase inverters using single and multiple zero sequence injections (ZSIs)

No. Phases	**Phase Spatial Displacement**	**Single ZSI**	**Multiple ZSI**
3	Symmetric	15.4	—
5	Symmetric	5.15	—
6	Symmetric Asymmetric	— 3.53	15.4
7	Symmetric	2.57	—
9	Symmetric Asymmetric	15.4	15.4

special case is $n = 6$, where (2.2.4) is only applicable when the load has asymmetric windings with a single neutral point [83]. Alternatively, multiple ZSIs can be applied to achieve a 15.4% DC-bus voltage utilization, similar to SVM, when n is a multiple of three and the neutral points are isolated [84]. For example, six-phase VSI with dual ZSIs was demonstrated in [85]. Table 2.4 summarizes the maximum attainable M_{max} in multiphase inverters with single and multiple ZSI for symmetric and asymmetric loads.

SVM

In spite of its complexity, SVM is yet attractive in multiphase traction inverters owing to its improved DC-bus voltage utilization, lower harmonic components, and improved fault tolerance owing to the redundant switching states for the same voltage vectors. This redundancy also provides the designer with an additional degree of freedom to optimize the performance based on a desired criterion.

Numerous SVM techniques have been proposed in the literature for MPIs. The

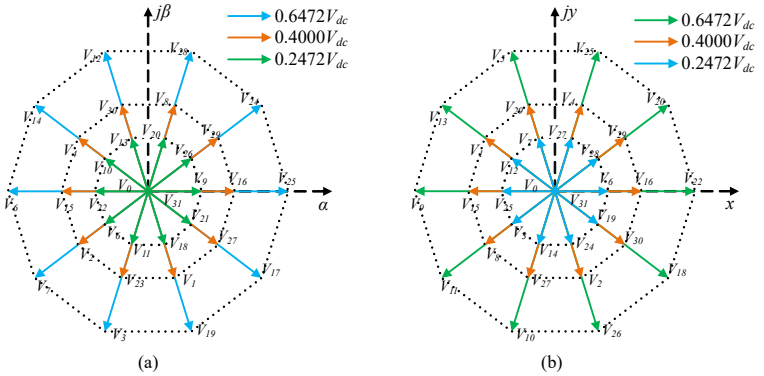


Figure 2.9: All possible voltage vectors in five-phase 2L VSI and their projection on (a) α–β subspace, and (b) x–y subspace.

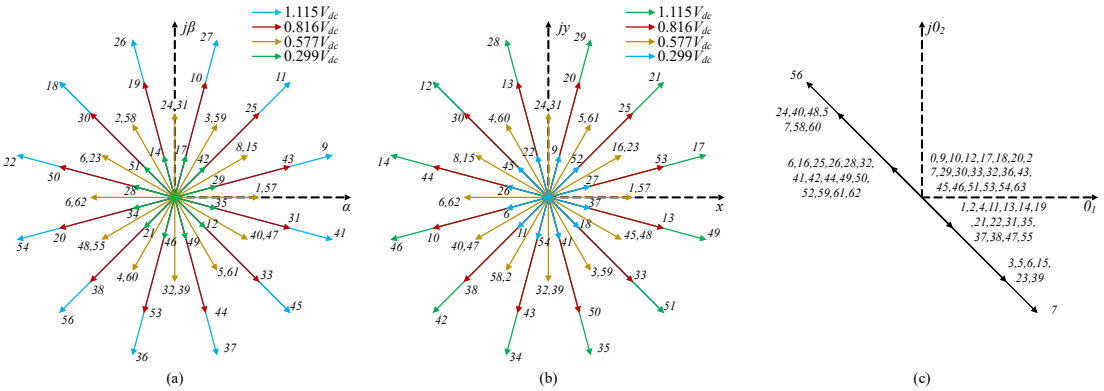


Figure 2.10: All possible voltage vectors in six-phase 2L VSI and their projection on (a) α–β subspace, (b) x–y subspace, and (c) 0_1–0_2 subspace.

different techniques vary in the applied vectors and/or switching sequence. Consequently, different maximum modulation indices are derived. Nonetheless, many of the proposed techniques are based on the VSD approach discussed in Section 2.1.1.

The α–β and x–y subspaces are commonly referred to as torque-producing subspace and harmonic-producing subspace, respectively. Put otherwise, the vectors in α–β subspace contain the fundamental components of the machine that produce a rotating magnetomotive force, while the vectors in x–y subspace only produce losses.

Hence, modulation techniques usually focus on minimizing the x–y subspace contribution. While completely eliminating its effect is impossible, using the volt–second principle alternating vectors in x–y subspace can be chosen to produce a zero average of those components. Note that for multiphase inverters with $n > 6$ there exist more than one x–y subspaces (see Table 2.1).

VSD-based SVM for $n = 5$ decomposes the 5D space into two orthogonal subspaces, α–β and x–y. In general, for any n odd number of phases, voltage and current vectors are mapped into $(n-1)/2$ orthogonal subspaces. Figure 2.9 depicts the voltage vectors in 2L five-phase VSI, where the vectors form two concentric decagons. In VSI, there exist $2^5 = 32$ voltage vectors, of which 30 are active [86]. Those vectors are categorized in three groups: large, medium, and small vectors. SVM techniques for 2L five-phase VSI are normally classified, based on voltage vectors selection, as near-two vectors and near-four vectors [87]. While the former techniques enjoy a superior maximum modulation index, the latter techniques are preferred for their 3^{rd} harmonic suppression capability.

VSD-based SVM for $n = 6$ can be classified as 12-sector based [53, 81, 88, 89] and 24-sector based techniques [90–92]. The latter is digitally easier to implement and yields reduced current harmonic distortion. However, two transitions belonging to two or more inverter legs occur at the same time during a sampling period [90]. As a result, asymmetric PWM waveforms are expected. On the other hand, the digital implementation of 12-sector modulation techniques is challenging since inverter legs can switch more than once in a switching period. In both schemes, the vectors are categorized in four groups: large, medium-large, medium, and small vectors, as shown in Figure 2.10. The switching sequence and the applied zero vector yields continuous

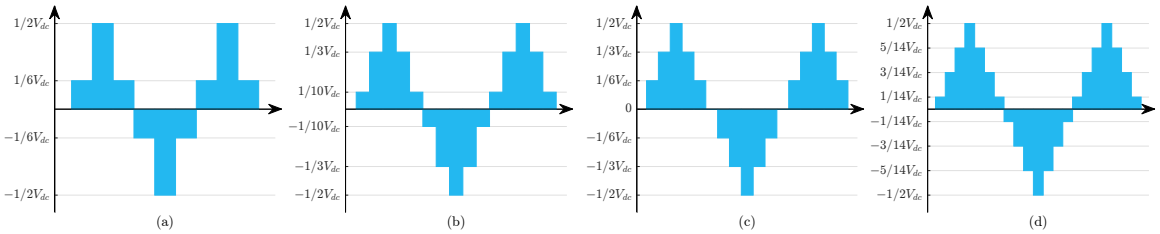


Figure 2.11: Common-mode voltage (CMV) waveform in 2-level multiphase VSIs as a function of DC-bus voltage. (a) $n = 3$. (b) $n = 5$. (c) $n = 6$. (d) $n = 7$.

or discontinuous (DPWM) modulation [88, 92, 93]. In continuous modulation, all switching legs change their ON/OFF state within one switching period at least once, whereas one (or more) leg(s) is clamped to $+V_{dc}$ or $-V_{dc}$ for at least one sector in DPWM. Discontinuous SVM techniques can reduce the implementation complexity at the cost of higher distortions [93, 94].

Numerous VSD-based SVM techniques for MPIs are invested in the reduction of CMV, induced by the high-frequency modulated inverters. The CMV excites a common-mode current, which is detrimental for many applications including motor drives and PV systems [95, 96]. The excited common-mode current contributes to motor aging rate by causing a bearing damage, insulation breakdown and electromagnetic interference (EMI) [97]. For n-phase VSI, the CMV varies in the range of $\pm 0.5V_{dc}$, regardless of n. However, the number of levels in CMV increases with n. Figs. 2.11 demonstrates the CMV in 2L VSI with $n \in \{3, 5, 6, 7\}$ when conventional SVM is employed. Hence, the higher the phase count the higher the degrees of freedom are to be exploited to reduce the CMV. CMV reduction based on SVM techniques for five-phase VSI was investigated in [97–102]. The conventional SVM technique for five-phase VSIs employs large, medium and zero vectors. The latter are

responsible for the highest level of CVM (i.e. $\pm 0.5V_{dc}$). Hence, the suggested techniques in [97–102] offer alternative switching techniques and patterns that eliminate the need for zero vectors, thus reducing the CMV. However, the reduction of CMV comes at the expense of performance deterioration in either voltage THD, current THD, switching loss, modulation range, or a combination of them.

Utilization of only medium vectors or only large vectors were suggested in [100]. Such techniques yield a constant CMV (i.e. ΔCMV= 0). On the other hand, the RMS value of the CMV was still high. A competitive technique using only a combination of large vectors was suggested in [98] and employed in [97] for motor drives applications. This technique results in a CMV of $\pm 0.1V_{dc}$ while maintaining an adequate current THD. Its switching loss can also be improved when combined with the method suggested in [101] at high M. A MPC controller was proposed in [103] to improve the current performance while simultaneously reducing the CMV to $\pm 0.1V_{dc}$ and maintaining a full modulation range. This, however, is achieved at the expense of increased switching frequency.

Similarly, CMV reduction by SVM for n = 6 [93,104,105] and n = 7 [106] have been proposed. In [93, 105, 106], zero vectors are avoided to reduce, and even eliminate, the variations in CMV at the expense of reduced modulation range. In [104], a phase shifting strategy for the PWM signals of a six-phase VSI supplying a dual three-phase asymmetric machine was proposed. The shifting strategy leads to two CMVs (from each three-phase set) that are 180° out of phase. As a result, the total CMV, which is the sum of both, is zero.

Besides VSD, other SVM techniques have been investigated for 2L multiphase VSIs such as group-based and vector classification. When n is a multiple of 3, the

n-dimensional space can be treated as $n/3$ independent three-phase systems, given that the load has $n/3$ isolated neutrals. Such an approach is known as a group-based SVM. In [52,63], group-based SVM techniques were applied to 2L nine-phase VSI. An improved performance, in terms of voltage and current harmonics, was reported when compared to VSD-based SVM techniques. Additionally, it was demonstrated in [63] that group-based SVM can reduce DC-bus capacitor requirements. More specifically, it was found that C_{dc} in a nine-phase VSI with group-based SVM has to handle only one third of the DC-bus RMS current when compared to a three-phase VSI modulated via SPWM. Hence, the modulation technique can play a key role in achieving a higher power density in multiphase inverters.

Vector classification (VC)-SVM was investigated in 2L six-phase VSI in [107–109]. The VC-SVM is based on the double d–q modeling theory for multiphase systems. He *et al.* [109] compared VC-SVM to 12-sector VSD-based SVM techniques. They concluded that VC-SVM achieves a higher DC-bus voltage utilization with a simpler implementation, at the expense of higher output harmonics.

2.3 Nine-Switch Inverter

NSI is a special VSI topology. Originally conceived in the late 2000's to independently drive two three-phase machines with reduced switch count [110], NSI was later adopted for six-phase machines [111–116]. This section reviews the NSI topology and compares it to the six-phase VSI in terms of cost, control, and efficiency.

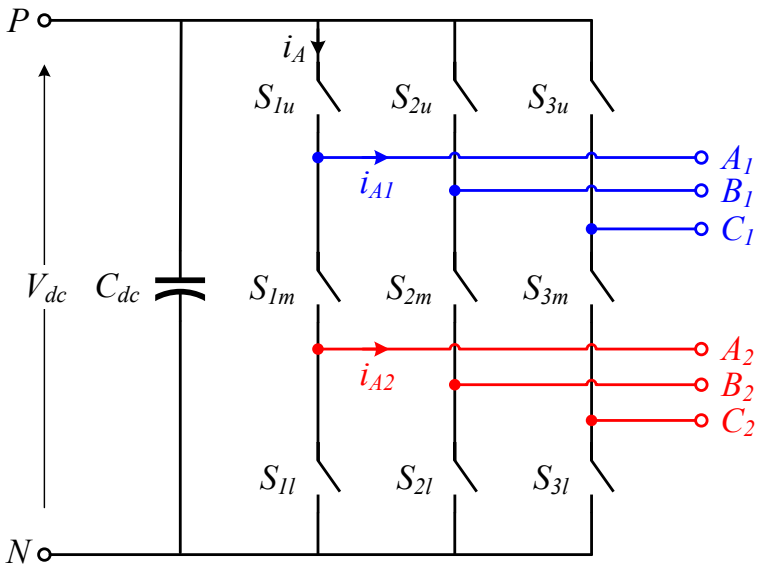


Figure 2.12: Nine-switch inverter (NSI) topology for six-phase machines (S_u, S_m, and S_l are upper, middle, and lower switches, respectively).

Table 2.5: VA rating comparison between VSI and NSI

No. Phases	**Config.**	**VSI**			**NSI / 12-Switch Inverter**		
		Switch Rating	Amount	Total	Switch Rating	Amount	Total
6	Symm.	$E \times 0.5I$	12	$6EI$	$E \times 0.87I$	9	$8EI$
	Asymm.	$E \times 0.5I$	12	$6EI$	$E \times 0.97I$	9	$9EI$
9	Symm.	$E \times 0.3I$	18	$6EI$	$E \times 0.63I$	12	$8EI$
	Asymm.	$E \times 0.3I$	18	$6EI$	$E \times 0.66I$	12	$8EI$

2.3.1 Topology

The NSI topology is depicted in Figure 2.12, where a six-phase inverter is realized by three legs only, each comprising three switches. Instead of the twelve switches needed for six-phase machines in the traditional 2L VSI topology (Figure 2.4), NSI

utilizes only nine switches. The middle switches of the NSI, S_m are controlled via an exclusive OR (XOR) logic gate to prevent a leg short-circuit, as detailed in the next subsection. The NSI topology is also extendable to any $(3n + 3)$-switch inverter, where n is the number of three-phase sets [110]. For example, a 12-switch inverter can be developed for nine-phase applications with four switches per leg, in contrast to the 18 switches in nine-phase VSI.

While NSI employs reduced switch count, the current rating of its switches is relatively larger than their counterparts in six-phase VSI. Figure 2.13 depicts the relationship between input leg current and output phase currents of the NSI for leg A, when connected to an asymmetric load (i.e. $\delta = 30^{\circ}$). The input leg current is the vector summation of the two output phase currents as illustrated in Figure 2.14. Its magnitude for an arbitrary δ, defined in Figure 2.2, can be generally defined as:

$$I_A = \sqrt{2(1 + \cos\delta)} \cdot I_{A1} \tag{2.3.1}$$

where I_A and I_{A1} are the magnitude of leg and phase currents, respectively, as depicted in Figure 2.12.

A fair comparison of inverter cost can be evaluated using the VA rating of the inverter, as discussed in Section 2.2. Table 2.5 compares the inverter VA ratings of the NSI and VSI for the different load configurations. The values in Table 2.5 assumes three-phase VSI for base values. Since the discussion is limited to 2L inverters, the switches in both, VSI and NSI, are rated at E, irrespective of number of phases. The per-unit current rating, I of the switches in VSI for n phases is given in (2.2.1),

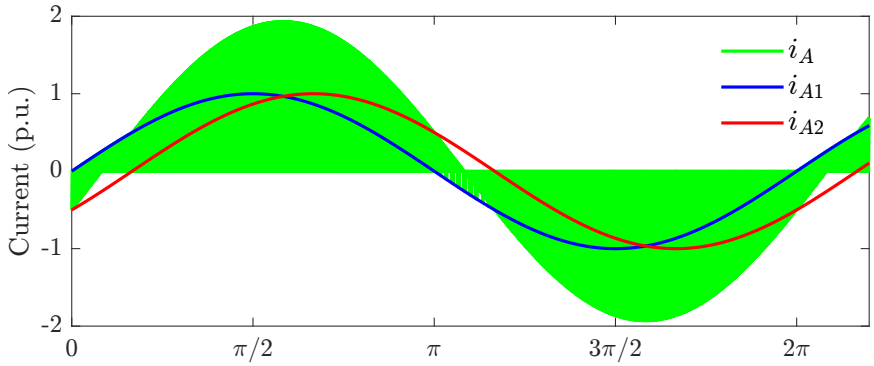


Figure 2.13: Current waveforms of leg A, i_{legA} and associated phase currents, i_{A1} and i_{A2} of the NSI in Figure 2.12 for asymmetric six-phase load (switching frequency: 30 kHz).

whereas for NSI it is defined as:

$$\begin{aligned} I &= (3/n) \cdot I_A / I_{A1} \\ &= (3/n) \cdot \sqrt{2(1+\cos\delta)}, \quad n = \{6, 9, \dots\} \end{aligned} \tag{2.3.2}$$

From the VA rating comparison, it is evident that NSI has a higher cost compared to six-phase VSI. The total VA rating for VSI is always 6 p.u., as discussed in the previous section. Considering six-phase asymmetric machine as a load, the cost ratio of NSI to VSI is three to two. Power semiconductors dictate around 40% and 70% of the total cost of traction inverters in the case of Si IGBT and SiC MOSFET, respectively [8, 117]. Hence, the NSI topology could be more expensive than VSI. It also follows that the reduced switch count in NSI does not necessarily mean reduced cost.

At the expense of increased cost, NSI has the potential for higher power density owing to its reduced switch count and associated gate drivers. Furthermore, because the commutation time of the inverter legs is relatively larger, to supply two phase

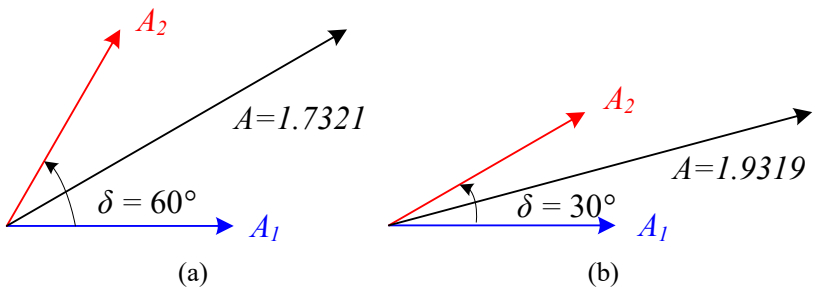


Figure 2.14: Input and output current vectors of leg A in six-phase NSI. (a) Symmetric. (b) Asymmetric.

currents, the stress on the DC-bus capacitor is alleviated. In other words, there exists a current path from the switching pole to the load for a longer time within one switching cycle, when compared to VSI. Therefore, less commutation spikes are experienced by the DC-capacitor in NSI. Figure 2.15 compares the normalized maximum stress on the DC-bus capacitor in VSI and NSI topologies. Judging by the maximum current stress, NSI can achieve DC-capacitor size reduction by approximately 16% when compared to its six-phase VSI counterpart, or 26% with respect to the conventional three-phase VSI.

One of the main drawbacks of the NSI, however, is the low DC-bus voltage utilization by the established modulation techniques [29]. The NSI requires 20% or 33% higher input voltage with respect to its VSI counterpart in order to produce the same output power when the winding of the load machine is asymmetric or symmetric, respectively [111]. A NSI topology with a boosting feature has been recently proposed in [118] to overcome this issue. With the help of input inductor and diodes the boosting NSI yields a higher DC-bus voltage utilization.

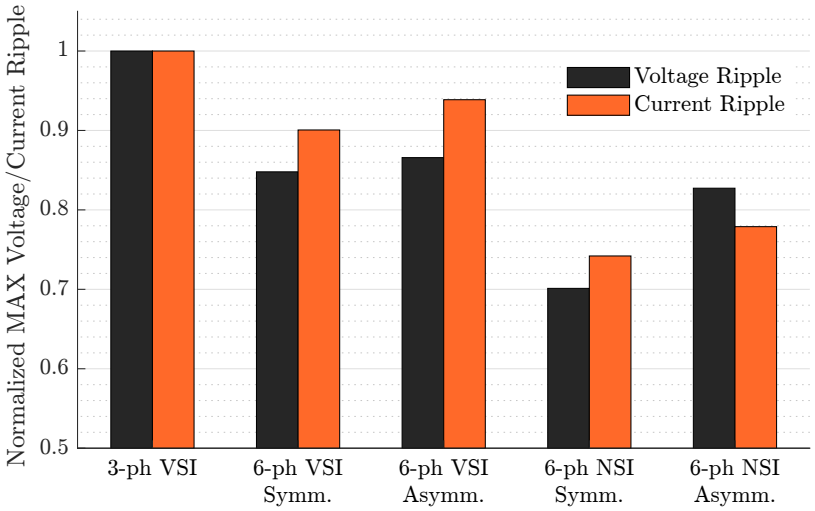


Figure 2.15: Normalized DC-bus capacitor requirements for NSI compared to six-phase VSI for symmetric and asymmetric load configurations.

2.3.2 Modulation

Similar to the VSI topology, the modulation techniques of the NSI can generally be categorized into CBPWM and SVM techniques. Additionally, the operation of the NSI can be divided into common-frequency (CF) and different-frequency (DF) modes [119]. In CF mode, both three-phase sets (upper and lower sets in Figure 2.12) operate at the same frequency, whereas in DF mode each of the two sets is operated at different frequency. Again, when the NSI is utilized to drive a six-phase machine, it is desired to have all sets operating at the same frequency, thus only CF mode is considered for multiphase drives applications. The CBPWM and SVM techniques of the CF mode of the NSI are reviewed in this subsection.

CBPWM

Similar to the VSI, the reference voltages of the NSI are compared with a carrier waveform to produce the gating signals of the switches in CBPWM [111–113, 115].

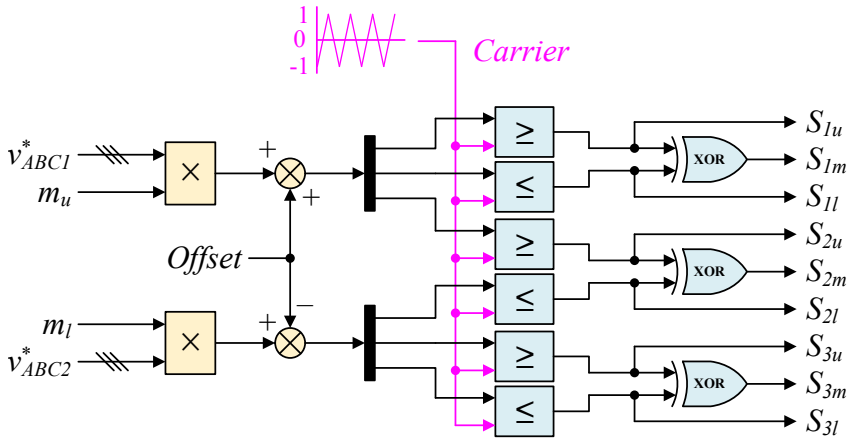


Figure 2.16: CBPWM scheme for NSI. m_u and m_l denote the modulation index for the upper and lower three-phase sets, respectively.

However, there are three distinct differences in CBPWM for the NSI. Firstly, each three-phase set can be controlled independently, and as such, has its own modulation index. Secondly, to guarantee that each of the two three-phase sets supply the same power, the modulating signals of the two sets must not overlap. Consequently, a vertical offset in the positive and negative directions is added to the upper and lower three-phase sets, respectively. While the modulation index and the offset values can be different for each three-phase set, they are chosen to be the same when supplying a single six-phase machine [111]. Thirdly, as mentioned earlier, the gate signals of the middle switches are generated by XOR-ing the gate signals of the upper and lower switches to prevent a short-circuit. Figure 2.16 depicts the CBPWM technique for the NSI.

As mentioned in the previous subsection, the modulation index of the NSI in CBPWM is influenced by the winding configuration of the six-phase machine. The

Table 2.6: Comparison between modulation schemes for the NSI topology

Modulation Technique	Ref.	Voltage THD	Max Modulation Index		Thermal Distribution Among Switches	Switching Loss	Complexity
			Symm.	Asymm.			
CBPWM	[110]	High	0.6667	0.7944	Not balanced	High	Low
	[113]	Medium	0.7694	0.9167	Not balanced	High	Low
	[119]	Medium	0.7694	0.9167	Top and bottom	Medium	Medium
	[120]	Low	0.6667	0.7944	All switches	Low	High
SVM	[121]	Medium	0.7694	0.9167	Not balanced	High	High
	[122]	Low	0.7694	0.9167	Not balanced	High	High
	[123]	Low	0.7694	0.9167	Not balanced	Medium	High

maximum modulation index for the NSI topology, as a function of the spatial displacement between the two three-phase sets, δ is defined as [115]:

$$M_{max} = \frac{1}{1 + \sin \delta/2} \tag{2.3.3}$$

Using (2.3.3), the M_{max} is 0.667 and 0.794 for symmetric ($\delta = \pi/3$) and asymmetric ($\delta = \pi/6$) machines, respectively. Therefore, the NSI topology is deemed more competitive when utilized in asymmetric six-phase drives. Sinusoidal modulating signals with proper offsets are used in [110]. Although the method is simple, it suffers from uneven thermal distribution among the three switches of the same leg and high switching loss. Additionally, shifting the modulating signals vertically leads to unsymmetrical switching profiles of the positive and negative half cycles, which in return increases the voltage THD. Modifying the modulating signals by ZSI is investigated in [113]. The addition of the third order harmonic increases M_{max} by 15.4%, similar to SVM technique [121]. However, the method in [113] could not reduce the switching loss.

In order to reduce the switching loss of NSI, DPWM was in [119], where one modulating signal is shifted vertically and the other one remains symmetric along the time axis, which is the modulating signal of higher magnitude. The method

in [119] reduces the THD and the switching loss of the top and bottom switches. This method is extended in [120] to include the middle switch as well, achieving a minimum switching loss at the expense of complexity. Table 2.6 summarizes the comparison between those different modulation techniques.

SVM

Based on the surveyed literature, SVM techniques are not as common when compared to CBPWM techniques, although they enjoy the potential of improved DC-bus voltage utilization and reduced switching commutation [112, 121]. This is mainly attributed to the simplicity of the CBPWM. Conversely, the SVM scheme for NSI is not as involved as its six-phase VSI counterpart. For the NSI, the SVM scheme is found upon the hexagon of the conventional 2L three-phase VSI. However, each voltage vector of the hexagon can be generated by two redundant switching states in the NSI [114]. Hence, there are a total of 14 switching states in the SVM of the NSI. Nevertheless, X. Li *et al.* [114] argue that not all switching states are necessary to generate the desired output. In [114], a six-mode SVM switching sequence was proposed, which resulted in improved efficiency at the expense of slightly higher output voltage harmonics. Authors in [122] and [123] developed an SVM that provides a decoupled control for the NSI similarly as it is two 2-level 6-switch VSIs. The decoupled control in [122] and [123] eliminates the need for XOR gate to generate the PWM signals for the middle switches. In [123], the selection of voltage vectors to reduce the switching loss is considered which was not in [122].

2.3.3 Inverter Losses

Based on the foregoing relative VA ratings of VSI and NSI, the efficiency of both multi-phase inverter topologies can be evaluated by comparing the power losses incurred by the switches. For this analysis, the considered switch is SiC MOSFET (1200V/115A) by Cree (C3M0016120D). Also, the modulators used for both topologies is SPWM.

The device switching loss is determined by the rated voltage and current stress and switching frequency, while the conduction loss is determined by the average current and $R_{DS(\mathrm{ON})}$, from the datasheet. All operating conditions including junction temperature, gate resistance and switching frequency, along with modulation index, are assumed the same. Normalized power loss with respect to the switching loss is adopted to yield a generalized comparison. Put otherwise, the rated switching loss of the SiC MOSFET is set to 1 p.u. It follows that the total per-leg switching loss for six-phase VSI is 2 p.u. The switching loss of the upper and lower switches (S_u and S_l) in NSI is similar to that of the VSI, i.e. 1 p.u. However, the switching frequency for the middle switch (S_m) is twice as that of S_u/S_l. Thus, the total per-leg switching loss of NSI is 4 p.u.

The conduction loss of the SiC MOSFET can be determined by the average current and $R_{DS(\mathrm{ON})}$ from the datasheet. For a duty cycle $D = 0.6$, the conduction loss is found to be 0.6 p.u. per switch, or 1.2 p.u. per-leg in six-phase VSI. In NSI, the average current is higher than that of the VSI and can be determined by using (2.3.2). For $n = 6$, $I = 1.73$ and 1.93 for symmetric and asymmetric loads, respectively. Therefore, the conduction loss ratio between S_u and S_l to that of the VSI is I^2. The difference in duty cycle for S_u and S_l due to the modulation offset in Figure 2.16

Table 2.7: Per-unit inverter loss comparison between six-phase VSI and NSI using SiC MOSFET

Type of Losses	**6-phase VSI**	**Symm. NSI**	**Asymm. NSI**
Inverter VA Rating	$6EI$	$8EI$	$9EI$
Switching Loss	12.0	12.0	12.0
Conduction Loss	7.1	12.0	14.7
Total Loss (p.u.)	**19.1**	**24.0**	**26.7**

balance out when considering per-leg losses. It follows that the conduction loss for $(S_u + S_l)$ is (0.6 p.u. $\times\ 2I^2$) or 3.6 p.u. and 4.5 p.u. for symmetric and asymmetric loads, respectively. Lastly, S_m is only ON for a fraction of D equal to the modulation offset value, which is considered 0.2 herein. It follows that the conduction loss of S_m is (0.6 p.u. $\times\ 0.2 \times I^2$). Thus, the total per-leg conduction loss in NSI is 4 p.u. and 4.9 p.u. for symmetric and asymmetric loads, respectively.

Table 2.7 summarizes the total inverter loss of NSI and VSI based on the respective VA rating of each topology. Based on this analysis, NSI is inferior to VSI in terms of inverter efficiency, and it is at its worst when supplying an asymmetric load/machine due to high I rating. VSI enjoys approximately 25% and 40% higher efficiency when compared to NSI with symmetric and asymmetric loads, respectively. The same analysis was verified numerically using the thermal model of the SiC MOSFET in PLECS by Plexim. Figure 2.17 depicts the normalized losses of VSI and NSI, which are in line with those tabulated in Table 2.7.

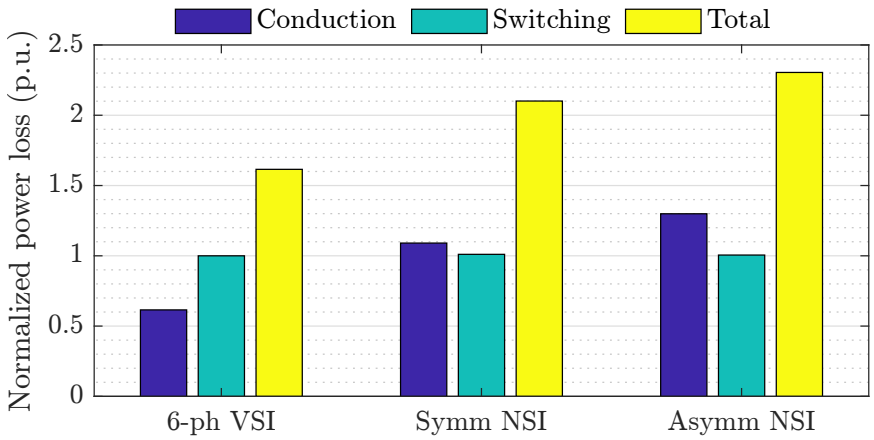


Figure 2.17: Normalized power losses of six-phase VSI and NSI using SiC MOSFET for symmetric and asymmetric loads (V_{dc} = 800 V, f_1 = 50 Hz, f_s = 10 kHz, M = 0.6, PF = 1).

2.4 Future Trends

To further advance the viability and commercial feasibility of MPIs, some recent research trends have been noticed in literature. Such trends focus on improving efficiency, power density, and reliability of the MPIs. This section reviews such trends and highlights the challenges that must be addressed prior to their adoption, which are summarized in Table 2.8.

2.4.1 Topologies

Multiphase Current Source Inverter

By principle of duality, the current source inverter (CSI), shown in Figure 2.18, constitute an alternative family of inverter topologies [147]. The CSI offers inherent advantages that are unavailable in VSI, such as a voltage boosting capability which enables an extended range of operation [124–126]. Additionally, the bulky and volatile

Table 2.8: Future trends on multiphase inverters and the challenges associated with them

Trend	Sub-category	Potential	Challenges
Multiphase Topologies	Current source inverters	• Boosting capability • Improved reliability • High operating temp.	• Conduction loss by prestage converter • Control complexity
	Multilevel Inverters	• Higher voltage • Improved EMC	• Higher complexity • Increased cost
WBG Devices	SiC MOSFET	• Miniaturization • High efficiency	• High EMI • Oxide layer failures
	GaN HEMT	• High operating temp. • High efficiency	• Low breakdown voltage • Gate driver design
Multiphase Integrated Motor Drives		• Higher power density • Reduced cost • Improved EMC	• Complex cooling • Mechanical stress on electronics • Limited space

Table 2.9: Recent studies on CSI topology from different perspectives

Topic	Reference	Highlights
Inverter topology	[124–126]	Basic CSI topology and control for traction applications
Advanced topologies	[127–131]	Inclusion of additional switches and resonant circuits
Control schemes	[124, 125, 132–134]	Control schemes for CSI drives
WBG devices	[135–137]	Employment of SiC and GaN devices
Machine design	[138, 139]	CSI-specific machine design
Over-lap time	[140, 141]	New techniques to compensate over-lap time effects
Multiphase CSI	[142–146]	Modulation and control of multiphase CSI (predominantly 5-phase)

DC-bus capacitor in the VSI is replaced with a choke input inductor, which can improve the power density of the inverter and reduce maintenance cost. Unlike the

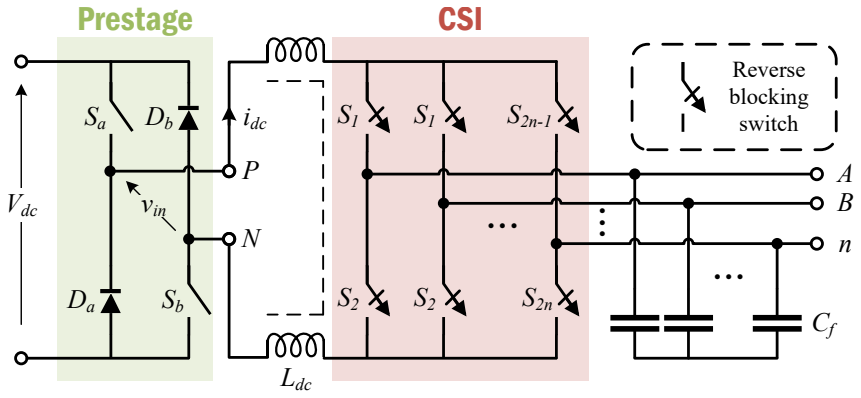


Figure 2.18: Multiphase current source inverter (CSI) topology with prestage buck converter for voltage-to-current source conversion.

DC-bus capacitor, the input inductor is not temperature-limited and its size can be reduced by increasing the switching frequency [148]. This in turn gives way for wider operating temperatures and higher power density. Last but not least, the CSI output is PWM currents and not voltages as in VSI. Therefore, the high dv/dt issue associated with VSI is non-existent in CSI [138]. The CSI requires switches with reverse blocking (RB) capability, which has conventionally been realized using Si controlled rectifiers (SCRs) or Si IGBT with a diode in series.

On the other hand, CSI suffers a relatively low efficiency and increased control complexity. Consequently, it has traditionally been considered inferior to VSI. However, with the emergence of WBG devices, as will be discussed in the next subsection, the employment of CSI drives for automotive and MEA applications has been revisited [135–138]. WBG devices with RB or bidiretional (BD) capabilities, such as SiC MOSFET and GaN high electron mobility transistors (HEMT), yield superior efficiency performance and reduce the size of the input inductor, thus improving the power density. An efficiency of 97.2% was reported in [135] for a three-phase CSI with RB SiC MOSFETs. Further efficiency improvement using BD GaN HEMT devices

over RB SiC MOSFET was demonstrated in [136, 137]. Extension to multiphase CSI has been reported in literature, albeit limited to five phases. In [142–146], five-phase CSI-fed drive operation, modulation, and fault tolerance techniques were investigated.

Nevertheless, the bottleneck for CSI in battery-powered applications is the need for a prestage converter to be installed between the battery and the CSI to provide a controlled DC-current [130], as shown in Figure 2.18. The prestage is normally set to operate in continuous conduction mode, thus incurring high conduction loss [138]. The future of CSI traction inverter is promising, yet its commercialization is contingent upon overcoming its inherent drawbacks. For example, inclusion of a seventh switch (in addition to the six switches in three-phase systems), in different topologies, was proposed in [127, 128, 131] to reduce CMV. In [129], an LC resonant circuit across the input inductor was proposed to enable soft-switching, and therefore, improve the inverter efficiency. A summary of recent research related to CSI from various perspectives is listed in Table 2.9.

Multiphase Multilevel Inverter (MPMLI)

As mentioned in earlier, MLIs have been proposed for higher efficiency, reduced harmonic distortion, lower electromagnetic compatibility (EMC) requirements, and improved fault tolerance [42]. With the trend in the automotive industry to upgrade powertrains from 400 V to 800 V and beyond [41, 149], MLI is expected to compete with the dominant 2L VSI, let alone supersede it.

Multiphase MLIs (MPMLIs) have been studies in [150–154]. Five-, six- and seven-phase 3L neutral-point-clamped (NPC) inverters were investigated in [153], [151, 154] and [155], respectively. The 3L T-type was examined in [150–152] for asymmetric

six-phase drives.

Currently, the high complexity and cost associated with the high part count, make MPMLIs feasible only for medium voltage (MV) and high voltage (HV) applications. However, as the market share of 800 V powertrains is expected to grow [156, 157], MPMLIs will become more feasible.

2.4.2 WBG Devices

A paradigm shift from conventional Si IGBT to WBG devices has been noticed over the past decade, thanks to their superior material properties [14, 19, 158]. Normally, the term WBG is synonym to SiC MOSFET and GaN HEMT semiconductor switches as they dominate the market share of WBG devices. However, other devices such SiC junction field effect transistor (JFET) [159] and vertical GaN [158] are under development.

In terms of technology, GaN semiconductors are considered superior to SiC as they enjoy higher breakdown field, higher switching frequency, and lower $R_{DS(\mathrm{ON})}$ [21, 158]. In contrast, device packaging, gate driver design, and EMC are deemed more challenging for GaN HEMT due to gate and parasitics ringing arising from ultra-fast switching [6]. Yet the main shortcoming of GaN HEMT is its low voltage rating ($\leq$ 650 V). Hence, GaN devices are not applicable in traction inverters, but rather limited to on-board chargers and DC-DC converters. Figure 2.19 shows the power–frequency envelope of the most famous Si, SiC and GaN power semiconductor devices, highlighting the suitability for traction inverters and on-board chargers in the automotive industry.

SiC MOSFETs enjoy a multitude of features that can be exploited to produce

traction inverters with a significantly higher power density [13]. Currently, the cost premium associated with SiC is challenging its wide adoption. Despite the compelling advantages of SiC switching devices over Si counterparts, they suffer reliability issues due to the thinner gate oxide layer (typically 50 nm for SiC versus 100 nm for Si) [11, 160, 161]. The thinner oxide layer can introduce degradation to the gate and body diode. Since SiC switching devices experience higher stress of electric field, it has been concluded that applying positive gate voltage for a long time causes a change in the threshold voltage (i.e. the minimum voltage required to turn on the device) and vice-versa for applying a negative gate voltage. This can be explained by moving the trapped electrons or holes when a gate voltage is applied causing a shift to the threshold voltage [162]. Although this phenomenon has been reduced in the second generation of the SiC MOSFETs, still 0.25 V variation is expected. This change can be limited when applying positive and negative gate voltages [161]. The gate leakage current is another concern for SiC switching devices. MOSFETs should be capable of withstanding a short-circuit current for small periods, where these currents are usually tenfold the rated value. When MOSFET experiences short-circuit current, the entire DC-bus voltage is applied across the MOSFET terminals. This introduces a high electric field that causes a leakage current from the gate to the source of the MOSFET, depending on the thickness of the gate oxide layer (which is relatively thin in SiC compared to the Si devices) and the applied electric field. This leakage current causes degradation to the gate oxide layer [163].

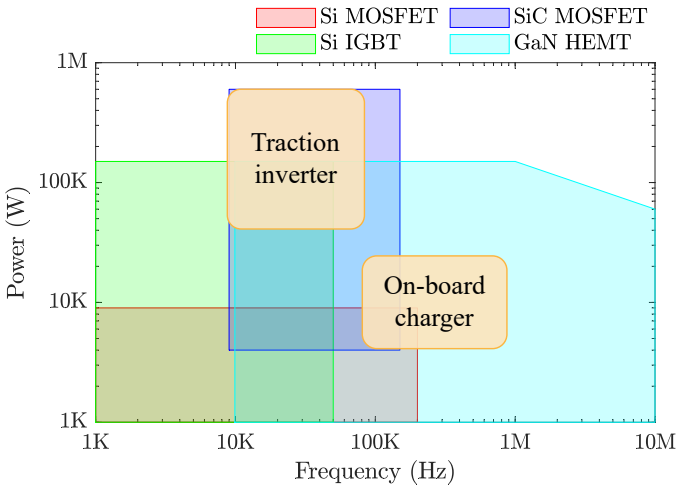


Figure 2.19: Power–frequency envelope of power semiconductor devices and application to the automotive industry [21].

2.4.3 Multiphase Integrated Motor Drives

The integrated motor drive (IMD) is a structural integration of the electric motor and the driving power electronics in a single unit. As a result of the physical integration, cost cutting is possible by the elimination of shielded cables and separate inverter housing [164–166]. The elimination of such components leads to 20%–40% volume reduction [167]. Furthermore, enhanced EMC is achieved, thanks to the direct connection between the two components. Researchers have been interested in combining the merits of IMDs with the merits of multiphase drives, such as higher torque density, lower torque ripple and improved fault tolerance, to yield a highly competitive motor drive for traction applications [23, 76, 168, 169]. A five-phase IMD with a disk-shaped, air-cooled inverter was proposed in [168]. The authors reported a reduced volume when compared to its three-phase counterpart, thanks to the reduction in the DC-bus capacitor. Another disk-shaped, nine-phase inverter in an IMD

structure was reported in [23]. A high power density of 35 kW/L was achieved by exploiting the reduced per-phase power handling of the MPI. In [169], a six-phase IMD drive for 48 V belt starter-generators (BSGs) was suggested for mild hybrid vehicles. The six phases were divided into three direct bonded copper (DBC) modules with air-cooling.

On the contrary, thermal management and mechanical design of IMD is very challenging [165]. Such challenges are compounded in multiphase IMD due to increased electronic components, such as sensors and gate drivers [164]. A potential solution for thermal management is the employment of WBG devices that can intrinsically operate at higher temperatures when compared to Si-based counterparts. The employment of GaN HEMT in IMD is currently a hot topic of research as reported in [136, 137, 165, 166].

2.5 Summary

This chapter reviewed the state-of-the-art of multiphase (beyond three) inverters and their application in transportation electrification. Two main topologies were reviewed: voltage source inverter and nine-switch inverter. While the former is extendable to any number of phases the latter is only limited to multiples of three phases. The benefits reaped from multiphase inverters in terms of improved per-phase current handling, reduced cabling cost, DC-capacitor sizing, control flexibility were reviewed in detail and benchmarked against the conventional three-phase inverter. Comparing six-phase to three-phase inverters for example, the former employs lighter AC cables whose total cost is lower than that of the latter. Also, the volume of the DC-bus capacitor can be reduced by up to 10% or 25% when utilizing a voltage source inverter

or a nine-switch inverter, respectively. Furthermore, while multiphase voltage source inverters employ a higher number of switches when compared to three-phase counterparts, both systems have the same volt-ampere rating, thus incurring similar cost in terms of power semiconductors. Such benefits make multiphase inverters suitable for high-power traction and aerospace applications.

It was found in this chapter that voltage source inverter is more competitive than nine-switch inverter in terms of efficiency, fault tolerance, DC-bus voltage utilization, and cost. Although the latter employs a fewer number of switches (nine versus twelve for six-phase systems), it exhibits a higher volt-ampere rating due to the reduced number of legs, which in turn increases the current stress on the switches.

Despite the foregoing merits of multiphase inverters, they require increased number of sensors and gate driver circuitry. Additionally, design for electromagnetic compatibility can be more complex. This is due to the higher switch count, which means more sources of electromagnetic noise.

Chapter 3

Silicon Carbide (SiC)-Based Multiphase Traction Inverters

The utilization of WBG devices as an alternative to Si devices is a promising area [13]. WBG devices, such as SiC, have attracted a lot of attention in the last decade because of their superior electrical and thermal properties. The wider band gap energy enhances resilience to electric fields, thereby increasing the ability to sustain higher voltages. It also offers a lower thermal resistance and subsequently improved power dissipation. These features facilitate the development of smaller devices with higher power density [19]. The high cost of SiC devices is currently a barrier to its mass acceptance. Aside from the cost, SiC devices have low current ratings and require several devices to be connected in parallel to tolerate the rated current of typical traction inverters.

Another frontier of innovation is the use of multiphase inverters (beyond three phases) [38]. This technology is drawing the attention of many original equipment manufacturers.

Existing studies have profusely discussed the merits reaped from the deployment of SiC devices in traction inverters [13, 19] and the benefits that multiphase machines enable [29, 38], each quite exclusively. The application in [13] is three-phase electric drives, whereas the application in [19] is even more generic. Also, the recent survey papers [29, 38] focus on the multiphase drives, including modeling and control, irrespective of device technology. However, the assessment and feasibility of SiC-based multiphase inverters are lacking from the literature. To this end, the objective of the present chapter is to analyze the use of SiC-based multiphase inverters. This chapter provides quantitative and qualitative analysis of SiC-based multiphase traction inverters when benchmarked to conventional three-phase counterparts. The presented analysis is designed for 100 kW traction inverters in 400 V and 800 V EV powertrains. It contributes to existing knowledge with analyses related to the number of devices used in each SiC-based multiphase inverter topology, the potential for DC-bus capacitor reduction, efficiency, power density, and cost.

The remainder of the chapter is organized as follows. The characteristics of SiC devices is discussed in Section 3.1. The power loss calculation of power semiconductors is reviewed in Section 3.2. In Section 3.3, a case study that showcases the feasibility of SiC-based multiphase inverters when compared to the conventional three-phase inverter is presented. Finally, Section 3.4 summarizes this chapter.

3.1 SiC Devices

The switching device constitutes the heart of any power converter. Conventional traction inverters, of any topology, normally use Si IGBT rated in the range of 600-1700 V. The highest voltage rating of a commercial Si IGBT has been 6.5 kV with a

highest operating junction temperature of 175 °C and a limited switching capability [9, 18]. SiC based devices offer supervisor performance from all foregoing aspects. Figure 3.1 illustrates the main material properties of SiC compared to Si. Advantages of SiC can be summarized as follows [9, 10, 12–15, 17, 18, 20, 170]:

1. Higher breakdown voltage ratings. Compared to highest 6.5 kV Si IGBT, SiC IGBT commercial devices are currently in excess of 20 kV [171]. Higher voltage rating yields increased inverter power density.

2. Higher switching frequency. While there is no theoretical limit on switching frequency, the maximum allowable frequency is normally dictated by switching losses due to turn-ON and turn-OFF delays. Consequently, Si IGBTs are limited to a few kilo hertz. SiC devices enjoy very fast switching performance allowing switching frequencies as high as 100 kHz [172]. Higher switching performance results in improved bandwidth and reduces the size of parasitic components.

3. Higher operating temperature. SiC devices has a theoretical junction temperature limit of 600 °C compared to 200 °C for Si devices [13]. The ability to operate at higher temperatures relaxes cooling requirements and leads to packaging miniaturization.

4. Higher thermal conductivity. SiC features at least twice the thermal conductivity of Si. Such a feature enables a higher thermal loading and reduces the risk of thermal runaway [173], thus, higher reliability.

All aforementioned features lay the foundation for dense traction inverters with higher efficiency. Nonetheless, the reliability of SiC devices and EMI issues that stem from operating at very high switching frequencies are still under investigation.

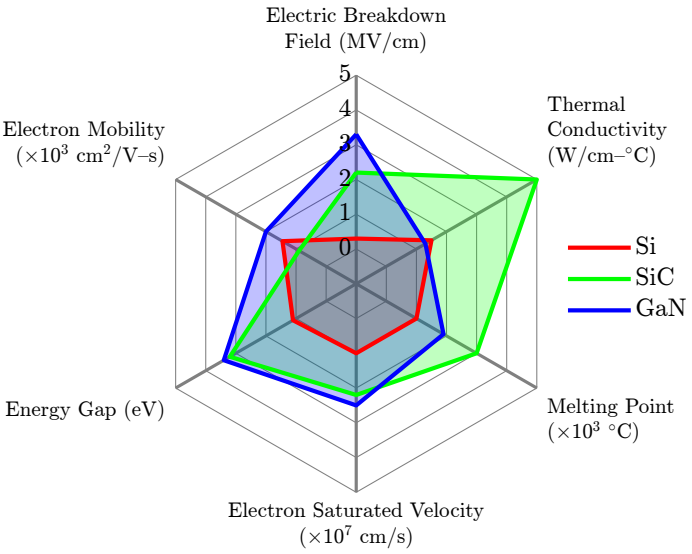


Figure 3.1: Material properties of SiC versus Si.

SiC devices can exist in various crystal structures, called *polytypes*. Each polytype has different semiconductor properties, including impact ionization rate, charge carrier mobility, and field/velocity characteristics. Among over 170 existing polytypes of SiC, only a few are commonly acceptable for use in electronic semiconductors. Currently, the most commonly known polytypes are the cubic (C) 3C-SiC and the hexagonal (H) 4H-SiC and 6H-SiC, where the number preceding the structure type (geometry) is inherent from the periodicity of the stacking sequence of atoms in the lattice structure. The first commonly used polytype was 3C [10], which was shortly supplanted by 6H as manufacturing techniques matured. By the mid-1990s, the growth of 4H had surpassed 6H and become the dominant polytype for SiC in almost all devices. Table 3.1 lists the electrical and thermal properties of the most famous SiC polytypes in comparison with Si. It is noteworthy to mention that, when compared to Si, SiC is deficient in terms of electron mobility due to low inversion layer mobility, irrespective of the polytype. In fact, this is the reason why 4H-SiC is the

dominant polytype nowadays, as it exhibits the highest electron mobility among all SiC polytypes.

SiC offers a multitude of devices. In addition to the commonly used Si devices,

Table 3.1: Electrical and thermal properties of Si and SiC polytypes at 300 K*.

Property	**Si**	**3C-SiC**	**4H-SiC**	**6H-SiC**
Bandgap (eV)	1.1	2.3	3.2	3.0
Electron effective mass (m_0)†	1.06	0.67		
$\|\|c$-axis			0.33	2.0
$\perp$ c-axis			0.42	0.48
Hole effective mass (m_0)†	0.59	~1.5		
$\|\|c$-axis			1.75	1.85
$\perp$ c-axis			0.66	0.66
Intrinsic carrier concentration (cm^{-3})	10^{10}	~10	~10^{-10}	10^{-5}
Breakdown field (MV/cm) at N_D = $10^{17}cm^{-3}$	0.6	1.8		
$\|\|c$-axis			3.0	3.2
$\perp$ c-axis			2.5	>1
Electron mobility (cm/V-s) at N_D = $10^{16}cm^{-3}$	1200	750		
$\|\|c$-axis			800	60
$\perp$ c-axis			800	400
Hole mobility (cm/V-s) at N_A = $10^{16}cm^{-3}$	420	40	115	90
Saturated electron velocity ($\times 10^7$ cm/s)	1.2	2.5	2.0	2.0
Thermal conductivity (W/cm-K)	1.5	3.3–4.9	3.3–4.9	3.3–4.9
Thermal expansion coefficient ($\times 10^{-6}$ K^{-1})	2.2	2.9	–	4.2‡
Debye Temperature (K)	600	1200	1200	1300

*Data compiled from [174–176] and the references therein.
$^{\dagger}m_0 = 9.11 \times 10^{-31}$ kg
‡ Measured at 700 K

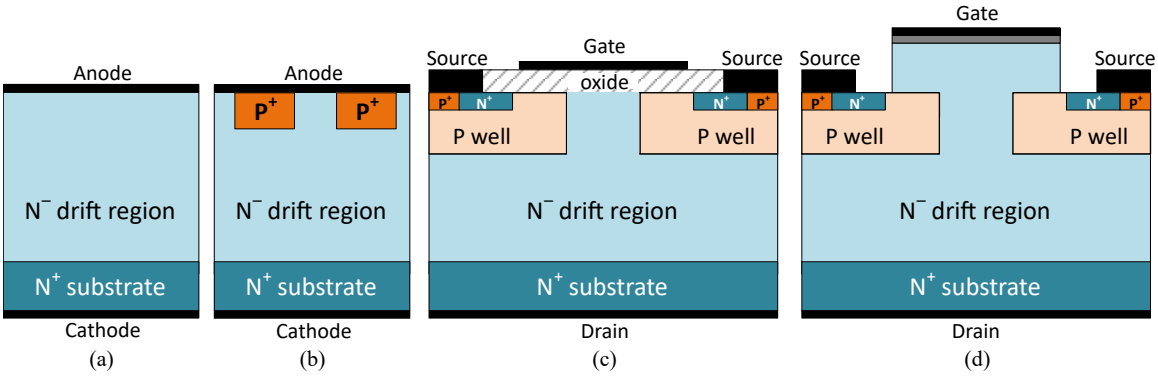


Figure 3.2: Cross-sectional view of cell structures of SiC devices. (a) SBD. (b) JBD. (c) MOSFET. (d) JFET.

SiC makes it possible for unipolar devices to exist, such as MOSFET and JFET, thanks to the high thermal conductivity and wide bandgap [173]. While SiC-based devices have matured enough to reach beyond 10 kV, this section reviews viable device options in the range of 600 V to 1700 V, which is the acceptable range for devices in traction inverters. A comprehensive list of commercial, automotive-grade SiC devices by major manufacturers can be found in [6], p. 11.

3.1.1 Diodes

There are three types of SiC power diodes: 1) Schottky barrier diode (SBD), 2) junction barrier diode (JBD), and 3) PiN diode [177]. For low breakdown voltages <1.7 kV, SBD is the most suitable diode [9,18,19]. Figure 3.2a shows the cell structure of SiC SBD. SBDs enjoy an extremely high switching speed, thanks to the majority carrier conduction mechanism that yields almost zero reverse recovery losses. Also, it features a very low R_{ON}. On the other hand, SBDs are prone to high leakage current that also increases as temperature increase due to the Schottky barrier effect [9,18,19].

For higher breakdown voltage >1.7 kV, JBD and PiN diode are preferred [18].

In fact, PiN diodes are only feasible for voltages 2–3 kV or higher due to high PN junction knee voltage, which results in high conduction losses. Additionally, PiN diodes exhibit a large reverse recovery loss. Therefore, it is not typically employed in automotive applications [6, 9]. JBD combines Schottky-like low ON-state losses and high switching characteristics, and PiN-like OFF-state behavior. Hence, JBDs offer an excellent performance over the voltage range of 600 V–3 kV. Figure 3.2b depicts the cell structure of the SiC JBS. Compared to SBD, JBD is inferior in terms of static performance; the reason why the former is more applicable in low voltage applications.

SiC diodes have been employed in traction inverter ever since the first commercial SBD in 2001. Even before the commercialization of SiC switches, SiC diodes were employed as free wheeling diodes with Si IGBT and Si MOSFET as a hybrid module, instead of Si PiN diode [178]. Currently, SiC Schottky diodes for traction inverters are available with voltages in the range of 600 V–1.7 kV and current ratings up to 50 A [6, 9].

3.1.2 Switches

MOSFET

SiC MOSFET is, by far, the most famous and commonly-used SiC device, owing to its superior characteristics and its market availability. Figure 3.2c shows the cell structure of the SiC MOSFET. Normally, the characteristics of SiC MOSFET are benchmarked against those of Si IGBT, and not Si MOSFET, owing to the popularity rivalry. Switching frequency in Si IGBT is very limited owing to the fact that it is a bipolar device with minority carriers. At turn-OFF, the minority carriers take

time to re-combine and dissipate, a phenomenon known as *tailing current*. Such a phenomenon is nonexistent in SiC MOSFET. Being a unipolar device with majority carriers, it enjoys a much smaller turn-OFF time, which significantly reduces switching losses and, in turn, enables higher switching frequencies [15,19,179]. While MOSFET has generally a higher R_{ON}, it is the ON-resistance per unit area that is relevant at the device level [179]. Thanks to the higher bandgap energy, SiC MOSFET can be manufactured with a considerably lower thickness, which in turn reduces R_{ON}. Additionally, the lower thickness leads to a smaller gate charge, thus, shorter turn-ON time [180]. Nevertheless, for blocking voltages ≥1.7 kV, R_{ON} of the SiC MOSFET becomes detrimental in terms of conduction losses, rendering it infeasible. Therefore, IGBT is the device of choice for voltages ≥1.7 kV. Another interesting feature related to the turn-ON time of SiC MOSFET is its negative temperature coefficient (NTC) [173]. In other words, the switching energy decreases when temperature increases, making it favorable to operate SiC MOSFET at ambient temperatures as high as 105 °C. Furthermore, MOSFET is capable of operating in the third-quadrant as a synchronous rectifier, which significantly reduce the conduction losses at nearly zero reverse recovery current [19, 172]. Such a feature has triggered a trend lately to exploit the intrinsic SiC MOSFET body diode for free-wheeling and concurrently eliminate the external anti-parallel diode [6,18,19]. Unlike Si MOSFET, the lifetime of the minority carriers of SiC MOSFET is short, and so is the reverse recovery charge [18,179]. Rohm Semiconductors and Wolfspeed have demonstrated that the elimination of the anti-parallel SBD does not harm the efficiency. On the other hand, this raises reliability concerns. As such, practitioners still recommend the installation of anti-parallel diodes.

Despite the many foregoing advantages SiC MOSFET has to offer, it suffers shortcomings in terms of EMI and reliability. The very high switching frequency comes at the cost of EMI noise. When connected to the EM, especially via a long cable, the switching time will increase twofold and lead to a 30% increase in switching losses [181]. Hence, a switching frequency/loss tradeoff should be carefully evaluated beforehand [182]. Also, most of the device failures are attributed to the oxide layer in the MOS [11]. Furthermore, compared to its Si counterpart, the gate driver requirements are more involved [19, 183].

JFET

Although not as famous as SiC MOSFET, SiC JFET is theoretically more efficient that MOSFET [20]. In fact, SiC JFET was commercialized before SiC MOSFET [15]. The cell structure of SiC JFET is shown in Figure 3.2d. JFET can be a suitable alternative to MOSFET for blocking voltages ≥1.7 kV, owing to its ultra low R_{ON} and high operating temperature capability [9,15,184]. Its ability to operate at as high as 500 °C was reported in [185]. Moreover, SiC JFET promises improved reliability, especially at high temperatures due to the absence of gate oxide [10]. In addition to avoiding failures related to the gate oxide, the gate terminal is intrinsically isolated from the body diode, thus, eliminating failures related to gate isolation material in MOSFET [15]. The main drawback in employing SiC JFET in traction inverters, however, is its normally-ON behavior. This has an obvious fatal consequence on the inverter in start up and shut down events due to a short circuit [15]. For this reason, a JFET with Si MOSFET in cascode configuration is usually studied. The resulting device in such a configuration is a normally-OFF JFET. Recently, 650 V

SiC cascode JFET was benchmarked against 650 V SiC tench MOSFET and 900 V SiC planar MOSFET in [184]. The devices were employed in a two-level inverter and the corresponding inverter efficiency was evaluated at the vehicle-level. It was found that the SiC cascode JFET is only superior at low power operating points. This is attributed to the higher conduction losses at high operating points (e.g. vehicle acceleration) that superseded the lower switching losses at lower operating points.

Alternatively, the normally-ON JFET can be exploited in the CSI, whereby inherent short circuit protection is available [147]. In CSI topology, the advantages of JFET can leverage a highly efficient and power dense traction inverter [186]. The CSI topology will be discussed in the next section.

Other Switches

Other SiC switches such as IGBT, bipolar junction transistor (BJT), and gate turn-off thyristor (GTO) were also investigated in literature. SiC IGBT is the most promising device among all SiC devices as it combines the advantages of SiC MOSFET and Si IGBT [6, 9]. The reduced gate charge and carrier lifetime of SiC and reduced conduction losses of IGBT enable high voltage SiC IGBT (>10 kV) switching at high frequencies (beyond 10 kHz) and high temperatures (beyond 200 $^{\circ}$C). Nevertheless, as of this writing, there is no commercial SiC IGBT due to reliability issues, predominantly related to forward voltage drift [6]. However, SiC IGBT breakdown voltage range would be beyond traction applications. Figure 3.2e depicts the cell structure of SiC IGBT. SiC BJT and SiC GTO are commercially available, however, similar to IGBT, they are limited to high voltage (>10 kV) applications.

3.2 Power Loss Evaluation

Power loss in semiconductors are classified as: conduction loss and switching loss. The loss profile during the operation of a semiconductor is shown in Figure 3.3. The total loss in a semiconductor, P_{loss} is the summation of conduction loss, P_{cond} and switching loss, P_{sw} as given in (3.2.1). From Figure 3.3, P_{loss} is the integration of the area under the power curve.

$$P_{loss} = P_{cond} + P_{sw} \tag{3.2.1}$$

This section describes the evaluation of conduction and switching loss based on the linear model of the MOSFET switch using the device's characteristics that are usually found in the datasheet. The dependency on junction temperature is tackled by thermal curve fitting. The coefficient of such curve fittings are assumed to be provided by the manufacturer. As such, power loss evaluation, in terms of junction temperature, can be carried out in PLECS software using its thermal model.

3.2.1 Switch Conduction Loss

Conduction loss occurs when the semiconductor is ON. In the ON-state, the current, I_o passes through the switch with a voltage, V_{ON} is present across the switch. In the case of a MOSFET, this is due to the equivalent resistance across the drain–source terminals, $R_{DS(\text{ON})}$. Figure 3.4a shows the equivalent conduction loss circuit of a MOSFET. The conduction energy, E_{cond} dissipated during the ON-state is:

$$E_{cond} = \int_{T_{\text{ON}}} V_{\text{ON}} I_o \, dt \tag{3.2.2}$$

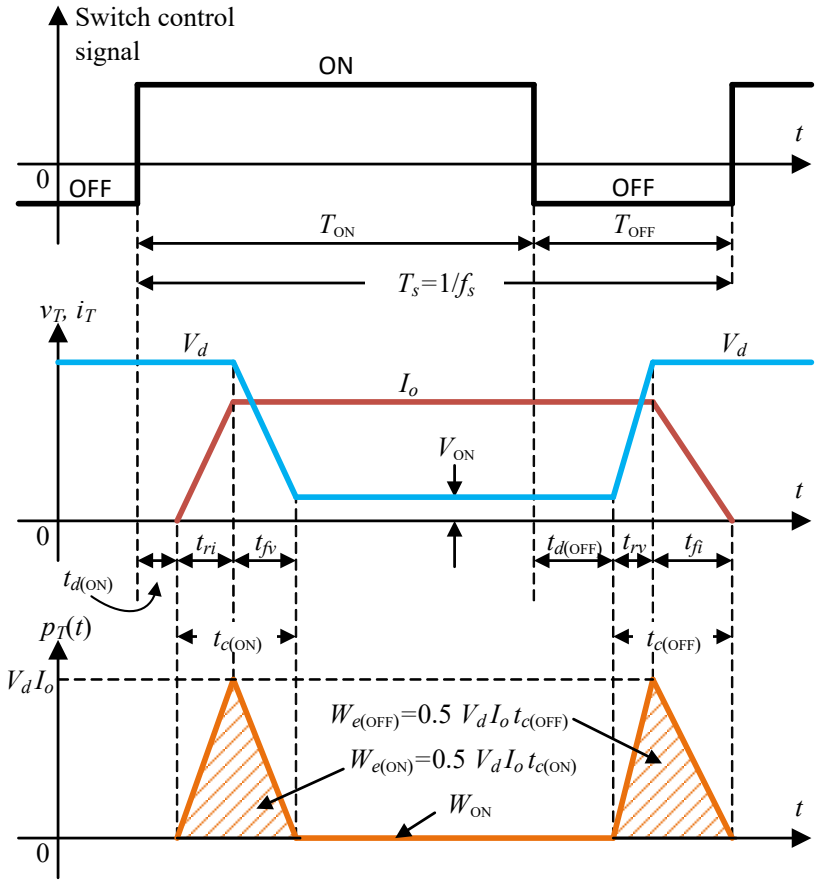


Figure 3.3: Electrical waveforms of the switch during one switching period and the generated loss.

Assuming a constant E_{cond} within T_{ON}, the conduction loss in (3.2.2) can be expressed in terms of power as:

$$P_{cond} = V_{ON} I_o D \tag{3.2.3}$$

where P_{cond} is the power conduction loss in watts and $D = T_{ON} f_s$ is the duty ratio. Alternatively, (3.2.3) can be expressed in terms of $R_{DS(ON)}$ as:

$$P_{cond} = I_o^2 R_{DS(ON)} D \tag{3.2.4}$$

The datasheet of a device usually defines V_{ON} at two temperature values: T_1 and T_2. A linear interpolation can be used to calculate V_{ON} at any T_j as [187]:

$$V_{\text{ON}}(T_j) = V_{\text{ON}}(T_2)\frac{T_1 - T_j}{T_1 - T_2} + V_{\text{ON}}(T_1)\frac{T_j - T_2}{T_1 - T_2} \tag{3.2.5}$$

3.2.2 Switch Switching Loss

The switching losses are produced at turn-ON and turn-OFF events, as shown in Figure 3.3. Switch current rises from zero to I_o while voltage drops from V_d to zero during turn-ON, and vice-versa during turn-OFF. Thus, the switching energy dissipated is the product of voltage and current during the switching events, defined as:

$$E_{sw} = \frac{1}{2}V_d I_o (t_{c(\text{ON})} + t_{c(\text{OFF})}) \tag{3.2.6}$$

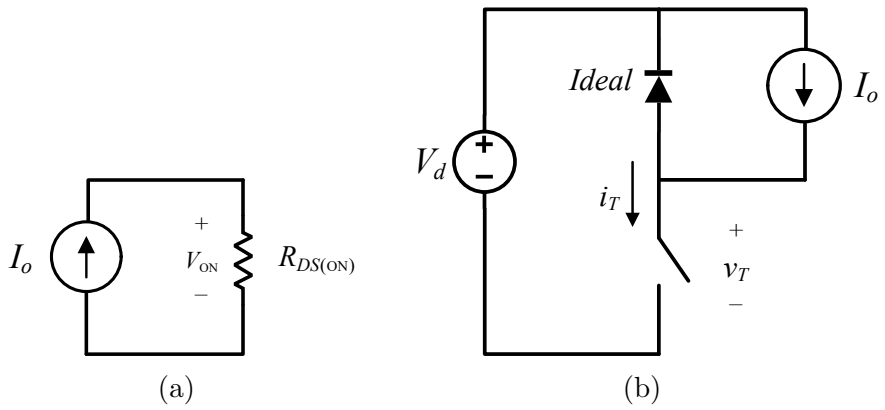


Figure 3.4: Equivalent circuit of (a) conduction loss and (b) switching loss.

where $t_{c(\text{ON})}$ and $t_{c(\text{OFF})}$ are the turn-ON and turn-OFF times of the switch, respectively, defined as:

$$\begin{aligned} t_{c(\text{ON})} &= t_{ri} + t_{fv} \\ t_{c(\text{OFF})} &= t_{fi} + t_{rv} \end{aligned} \tag{3.2.7}$$

where t_{ri} and t_{fi} are the current rise and fall times, respectively, and t_{rv} and t_{fv} the voltage rise and fall times, respectively.

The E_{sw} is different under various test conditions such as blocking voltage, junction temperature, and gate resistance. Therefore, the datasheet of a device provides E_{sw} at one or several given operating conditions in terms of a specified blocking voltage V_1 and junction temperature T_1. The E_{sw} at any T_j and blocking voltage V_2 can be calculated as [187]:

$$E_{sw}(T_j, V_2) = \beta \frac{E_{sw}(T_1, V_2) V_2}{\alpha V_1} \tag{3.2.8}$$

where

$$\begin{aligned} \alpha &= a_1 T_j^2 + b_1 T_j + c_1 \\ \beta &= a_2 T_j^2 + b_2 T_j + c_2 \end{aligned}, \tag{3.2.9}$$

α and β are the voltage and temperature coefficients, respectively, and a_1, a_2, b_1, b_2, c_1, and c_2 are the quadratic curve fitting coefficients. Such coefficients can be provided by the manufacturer or characterized experimentally. The E_{sw} in (3.2.6)

can be expressed in terms of power as:

$$P_{sw} = E_{sw} f_s \tag{3.2.10}$$

where P_{sw} is the power switching loss in watts.

3.3 Inverter Level Evaluation

A case study is undertaken in this section to analyze the SiC-based multiphase inverters in Section 2.2 and 2.3, quantitatively and qualitatively. The aim of this study is to showcase the potential of such inverters when benchmarked against the conventional three-phase counterpart in terms of device count, efficiency, power density, and cost. The investigated multiphase inverters in this study are rated at 100 kW, and designed for EVs with 400 V and 800 V powertrains.

All the studied topologies employ SiC MOSFET as the switching device. The selected SiC MOSFETs for the 400 V and 800 V powertrains are 650V/97 (C3M-0025065D) and 1200V/115A (C3M0016120K), respectively, both by Cree. Table 3.2 lists the test parameters used in this study.

3.3.1 Device Count

Table 3.3 tabulates the minimum per-leg current requirement for the 100 kW three-, five-, six-, and nine-phase VSIs and six-phase NSI. Also, based on the chosen SiC MOSFETs, the minimum number of paralleled devices required per switch position is listed. From Table 3.3, five-phase VSI with 800 V battery requires a lower total number of devices when compared with its three-phase counterpart. Therefore, cost

savings are attainable in multiphase VSI as SiC power switches dictate a significant portion of the total cost of the traction inverter, as will be shown later. This is not unique to the 800 V powertrain, but can rather be generalized for a given voltage level. Figure 3.5 demonstrates a range of inverter output current, in terms of device rated current, where five-phase VSI employs a lower number of total devices than three-phase. The reduction in the total number of devices comes at the expense of lower efficiency nonetheless.

Six-phase VSIs require the same number of devices when compared to three-phase, since the number of inverter legs is doubled, but the per-phase current is halved. On the other hand, the minimum number of devices needed for the NSI is 1.5 times higher than that of the six-phase VSI. This is due to the higher current rating of the NSI switches as given in (2.3.2). Generally, NSI employs a lower total number of devices only when the rated current of the inverter is lower than that of the power device [188].

Table 3.2: Parameters for Multiphase Inverter Topologies

Parameter	**Value**	**Unit**
Rated power	100	kW
Switching frequency	30	kHz
Output frequency	50	Hz
Load power factor	0.9	–
Modulation index	0.8	–
Junction temperature	80	$^{\circ}$C
Gate resistance	5	Ω
Modulation technique	Sinusoidal PWM	

3.3.2 Efficiency

Now that the inverters are sized to supply the same output power with adequate current sharing for the SiC MOSFETs in all topologies, the inverters are built in the PLECS environment. Figure 3.6 depicts the PLECS simulation schematic for the six-phase VSI as an example. The employed load for all topologies is a 100 kW inductive load with a 0.9 PF. The load is connected in asymmetrical configuration for six- and nine-phase topologies, i.e. phase shift of $\delta = 30^{\circ}$ and 20° between each three-phase set, respectively.

Asymmetrical configuration is selected since, as mentioned in Section 2.3, NSI is more competitive in such configuration, and therefore, rendering a fair comparison.

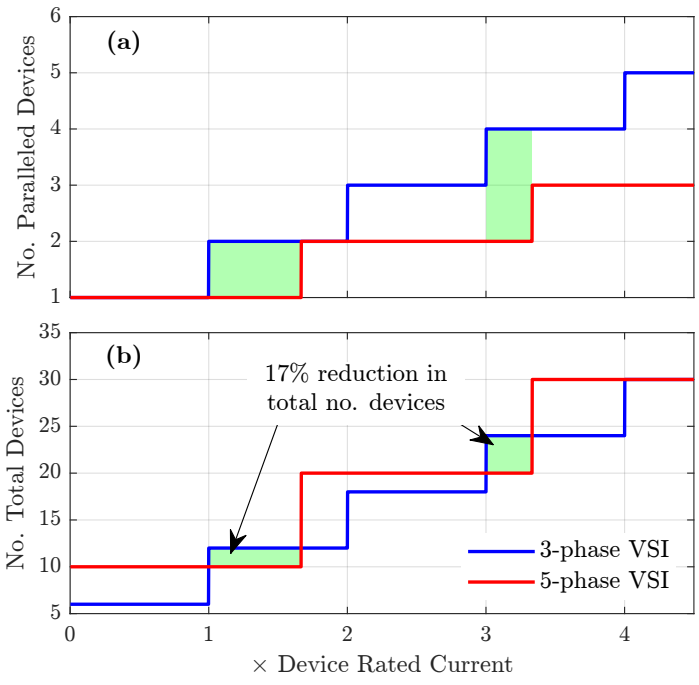


Figure 3.5: Reduction in total number of devices in five-phase VSI when compared to its three-phase counterpart in terms of device rated current, at a specific voltage level. (a) Number of paralleled devices per one switch. (b) Total number of devices.

Table 3.3: Comparison between different 100 kW multiphase inverters in terms of number of devices

V_{dc}	**Switch Rating**	**Inverter Topology**	**Current per Leg (A)**	**No. Paralleled Devices per Switch**	**Total No. Devices**
400 V	650V/97A	3-ph VSI	375.0	4	24
		5-ph VSI	225.0	3	30
		6-ph VSI	187.5	2	24
		6-ph NSI	375.0	4	36
		9-ph VSI	125.0	2	36
800 V	1200V/115A	3-ph VSI	187.5	2	12
		5-ph VSI	112.5	1	10
		6-ph VSI	93.8	1	12
		6-ph NSI	187.5	2	18
		9-ph VSI	62.5	1	18

Table 3.4: Comparison between different 100 kW multiphase inverters in terms of efficiency and cost

V_{dc}	**Inverter Topology**	**Efficiency**	**Cost**[†]
400 V	3-ph VSI	★☆☆☆☆	$ $ $
	5-ph VSI	★★★★☆	$ $ $
	6-ph VSI	★☆☆☆☆	$ $ $
	6-ph NSI	★★★☆☆	$ $ $
	9-ph VSI	★★★★★	$ $ $
800 V	3-ph VSI	★★★☆☆	$ $ $
	5-ph VSI	★☆☆☆☆	$ $ $
	6-ph VSI	★★★☆☆	$ $ $
	6-ph NSI	★★★★☆	$ $ $
	9-ph VSI	★★★★★	$ $ $

[†]Considering the cost of devices only.

All topologies are controlled using SPWM. Regardless of the number of phases, multiphase VSIs have the same maximum output voltage of $0.5V_{dc}$ in the linear region [189]. On the other hand, the maximum output voltage for the NSI with asymmetric load

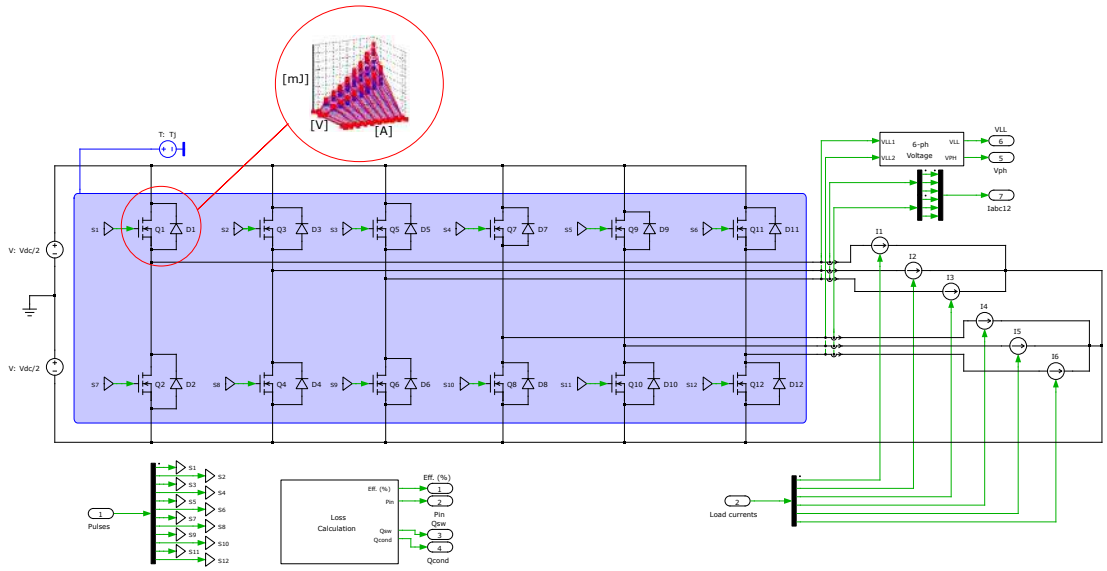


Figure 3.6: Efficiency evaluation model of a six-phase VSI in PLECS using SiC MOSFET thermal model.

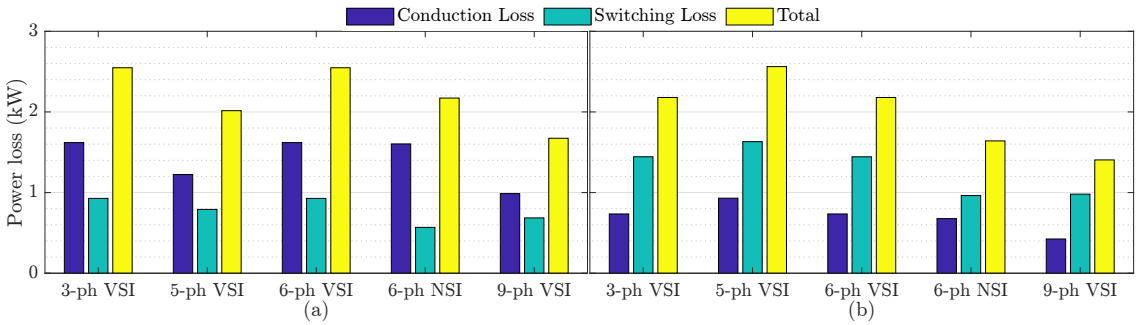


Figure 3.7: Conduction and switching loss for different multiphase topologies rated at 100 kW. (a) 400 Vdc. (b) 800 Vdc.

is $0.794V_{dc}$ [188]. The conduction and switching losses of the power switches are computed using the thermal model of the devices provided by the manufacturer. Figure 3.7 depicts the inverter losses for all the topologies listed in Table 3.3. In the case of the 400 V powertrain (Figure 3.7a), five- and nine-phase VSIs and six-phase NSI all yield reduced losses when compared to their three-phase counterpart, when using the minimum number of devices. Nine-phase VSI yields the highest efficiency, followed

by five-phase, and then six-phase NSI. Comparing three-phase VSI to six-phase VSI and NSI, all three exhibit a similar conduction loss. On the other hand, six-phase NSI enjoys a lower switching loss, rendering it more efficient.

In the case of the 800 V powertrain (Figure 3.7b), only six-phase NSI and nine-phase VSI yield reduced losses, with the latter being superior when benchmarked against the three-phase VSI. For both powertrains, the three- and six-phase VSIs have the same efficiency. When comparing the results of both powertrains, the switching loss is dominant in the 800 V powertrain and vice versa. While the showcased study is not all inclusive (i.e. different testing parameters or devices can lead to different results), it is nonetheless the potential that multiphase inverters can offer, in terms of improved efficiency and reduced device count, that should be emphasized. Additionally, some testing parameters scale linearly along all topologies. Switching frequency, for instance, has a linear relationship with switching loss, and varying it while keeping all other variables fixed will invariably lead to the same comparative findings.

3.3.3 Power Density

The power density of traction inverters is a complex problem that is dictated by many variables including electrical components, thermal management, and mechanical packaging [190, 191]. Figure 3.8a depicts a typical volumetric breakdown of a liquid-cooled SiC-based inverter [117, 191, 192]. Multiphase inverters are expected to have a higher gate driver requirements and increased cabling and current sensors. Nonetheless, such components do not consume a large portion from a volume perspective. From Figure 3.8a, gate drivers and cables constitute a meager 6% of the

total inverter volume. Furthermore, with a proper design, increased gate driver requirements can be accommodated on the existing printed circuit board (PCB) of the three-phase inverter, especially when the total number of devices in the multiphase inverter is equal to that of its three-phase counterpart (i.e. six-phase VSI). In other words, a six-phase VSI traction inverter would use more electronic components for the gate driver that will be placed on a single PCB whose dimensions are equivalent to that of a three-phase inverter. Hence, the volume of the gate driver board can be somewhat the same. Similarly, for cabling, a six-phase VSI would use double the cables (AC output cables) used in three-phase counterparts, yet lighter ones as the per-phase current is halved, for the same output power.

On the other hand, as mentioned earlier in Section 2.2, multiphase inverters offer a reduced capacitor size, which occupies more than a quarter of the total volume of SiC-based three-phase traction inverters. In the case of six-phase VSI, a 10% reduction in the capacitor size can offset the additional volume incurred by phase current sensors and cables.

Other components such as the DC-busbar, cold plate, and controller board are expected to remain the same when upgrading from three-phase to multiphase inverter, for the same output power. The volume of power modules in multiphase inverters can either be higher, lower, or the same as in three-phase counterparts, depending on the power level, per-phase current requirement and number of paralleled devices as explained in the previous subsection. For instance, a five-phase SiC-based inverter rated at 100 kW for 800 V powertrain would lead to a reduced volume of power SiC semiconductors (see Table 3.3).

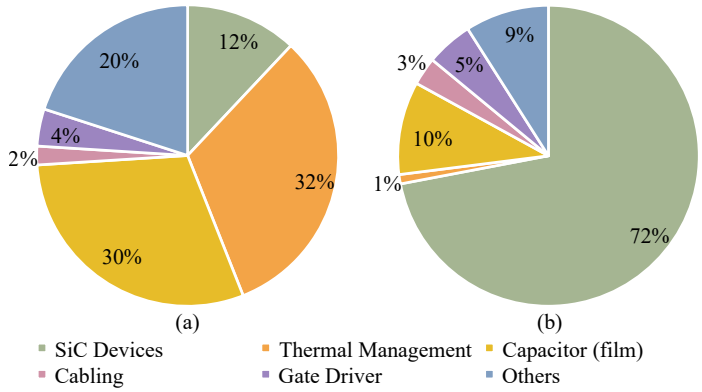


Figure 3.8: Breakdown of liquid-cooled SiC-based traction inverter by (a) volume and (b) cost.

3.3.4 Cost

The cost of SiC-based inverters, whether three-phase or multiphase, is mainly dictated by the cost of the SiC power modules (or discrete devices) [117, 192]. For instance, the cost breakdown of an air-cooled SiC-based three-phase inverter in [117] indicated that 77% of the total inverter cost is attributed to the SiC power modules. A cost breakdown of liquid-cooled SiC-based inverter is shown in Figure 3.8b, since liquid-cooling is, so far, the accepted industry practice for the automotive industry [16]. From Figure 3.8b, the capacitor and power SiC devices constitute more than 80% of the total inverter cost. Therefore, the additional gate driver requirements and higher sensors count in SiC-based multiphase inverters are not expected to affect the overall inverter cost significantly. On the contrary, the SiC-based five-phase VSI can lead to a reduced inverter cost, since it employs a lower total number of devices when compared to its three-phase counterpart. This is true when the designed inverter output current falls in the green regions in Figure 3.5. In this case, a 17% reduction in the total number of devices leads to a 12% reduction in total inverter cost. Additionally, while the rightmost column in Table 3.4 compares the cost in terms of

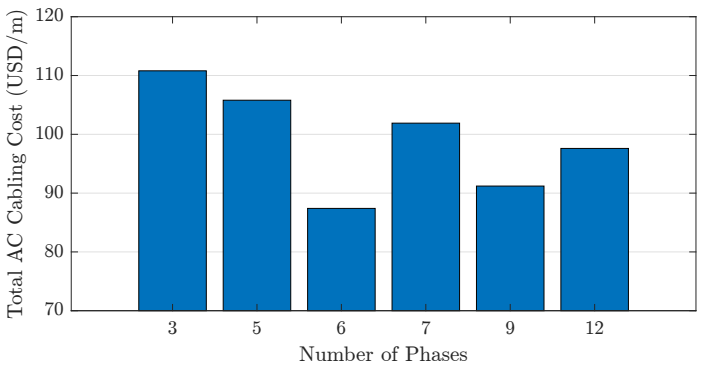


Figure 3.9: Total cost of AC cables of multiphase inverters rated at 100 kW and 0.8 PF (length ≤10 m).

SiC power devices only, it is deemed nonetheless representing the overall inverter cost with adequate confidence, since more than 80% of the total cost is attributed to the power devices and capacitor.

In terms of cabling, it was demonstrated in [38] that multiphase inverters can lead to reduced total cost of AC cables. The reduction in the cable size outweighs the increase in cable count in multiphase inverters. Figure 3.9 showcases the estimated total cost of AC cables for multiphase inverters rated at 100 kW. Six-phase VSI demonstrates the best tradeoff between cable count and size with a reduction of 21% of AC cable cost when compared to the three-phase VSI.

3.3.5 Case Study Summary

The spider plot in Figure 3.10 summarizes the comparison between the different multiphase topologies based on the foregoing quantitative analysis in addition to the DC-bus capacitor requirement in Figure 2.6, maximum DC-bus utilization [84], and fault tolerance capability. Benchmarked against the three-phase VSI, the nine-phase VSI yields the best improvement in efficiency and reduced C_{dc} size at the expense

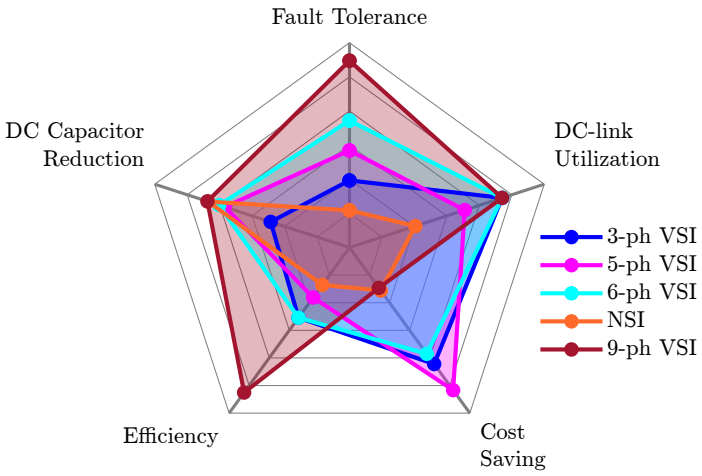


Figure 3.10: Comparison plot between SiC-based multiphase inverter topologies with different phase number for EV powertrains rated at 800 V.

of increased cost and control complexity. Six-phase VSI, however, offers a better tradeoff, which can be summarized as follows:

- It is as efficient as its three-phase counterpart, while using the same total device count which is lower compared to the six-phase NSI.
- Similar to the nine-phase VSI, it offers 10% volume reduction in C_{dc} when compared to three-phase VSI.
- Modularity and fault tolerance is improved when compared to three-phase VSI.
- Voltage utilization of the DC-bus is superior in six-phase VSI when compared to six-phase NSI and five-phase VSI.
- The greater reduction in AC cabling cost when opting for multiphase inverters occurs in six-phase systems.

Hence, six-phase VSI is deemed the most competitive multiphase inverter topology for traction applications. Additionally, from a qualitative perspective, features such

as improved fault-tolerance and reduced torque pulsation raises its competitive edge when compared to its three-phase counterpart.

3.4 Summary

This chapter reviewed the opportunities and challenges for SiC-based multiphase (beyond three) traction inverters in EVs. Multiphase traction inverters can complement the limitation of low current ratings of SiC devices by providing lower per-phase current requirements. Although they employ more switches in the additional phase legs, the total number of semiconductor devices is not necessarily increased. It was shown in this study that the total number of devices can be lower, which reduces the cost pertaining to SiC devices. Moreover, MPIs enjoy a reduced DC-capacitor requirement and reduced AC cabling cost, which can be exploited to improve the power density. Nevertheless, additional cost is expected from the higher count of sensors and gate drivers.

A case study pertaining to the efficiency and the total number of devices for SiC-based multiphase (five-, six-, and nine-phase) traction inverters rated at 100 kW was undertaken. Such inverters were benchmarked against the conventional three-phase VSI in 400 V and 800 V powertrains. The analyses showed that SiC-based MPIs can lead to improved efficiency. Special attention was given to the six-phase VSI for its competitiveness when compared to the three-phase VSI. Employing the same number of total devices of the latter, yielding the same efficiency, yet reducing the capacitor volume by almost 10% and AC cabling by 21%, and improving modularity and fault tolerance capability. Therefore, the remainder of this thesis will focus on the application of six-phase traction inverters for EV applications.

Chapter 4

Vehicle Level Comparative Analysis of Si- and SiC-Based Six-Phase Inverters

Vehicle level evaluation of traction inverters is a crucial aspect of EV development, as it provides a comprehensive assessment of the performance of the inverters in real-world conditions. This evaluation allows for the identification of valuable data for comparison with other similar vehicles, such as mileage and fuel economy. By benchmarking and analyzing such data, manufacturers and researchers can improve the design and performance of future inverters, thereby enhancing the overall efficiency and effectiveness of EVs.

However, limited studies evaluate the inverter efficiency at the vehicle level. To the author's best knowledge, efficiency evaluation of SiC-based MPIs for 800 V batteries has not yet been reported. In [184], vehicle level comparison was reported for a three-phase traction inverter using different types of Si and SiC devices. Vehicle

level evaluations for MLI inverters was reported in [65, 193, 194] for different aspects. The efficiency of asymmetrical 3L inverters for switched reluctance motor drives was evaluated in [65]. Power loss comparison between 3L NPC and 3L T-type using different modulation techniques was examined in [194] using Si IGBTs. SiC-base 3L NPC and 3L T-type for three-phase traction inverters in 400 V and 800 V powertrains was reported in [43].

The present study fills a gap in the literature by evaluating the efficiency of Si- and SiC-based six-phase VSIs at the vehicle level, in 800 V powertrains. The efficiency of the inverters is initially evaluated at the inverter and powertrain levels in Sections 4.1 and 4.2, respectively, using a permanent magnet synchronous motor (PMSM). Then, an EV model for the Chevrolet Spark is developed in Matlab/Simulink in Section 4.3, and employed in Section 4.4 to evaluate the efficiency of the Si- and SiC-based inverter topologies at the vehicle level. As a result, energy consumption and mileage from the studied inverters are obtained.

4.1 Efficiency at Inverter Level

For the target inverter design ratings of 100 kW at 800 Vdc, the per-phase current is below 100 A, as demonstrated in 3.3. Currently, many device manufacturers offer SiC MOSFETs rated beyond 100 A. As such, discrete SiC MOSFET C3M0016120K (1200 V/115 A) by Cree [195] is selected, eliminating the need for device paralleling. Hence, the complexity of the design is reduced. Also, the selected device features a low on-state resistance, $R_{DS(\mathrm{ON})}$ of 16 mΩ. A competitive Si IGBT discrete device is sought to provide a fair comparison between the two technologies. Hence, the Si IGBT IKY75N120CS6 (1200 V/75 A) from Infineon [196] was selected.

The conduction and switching losses of the Si- and SiC-based inverters are then evaluated by conducting a load current sweep using SPWM at multiple switching frequencies. The losses are evaluated in PLECS using the thermal model of the device provided by the manufacturer, as shown in Figure 3.6. Figure 4.1a shows the efficiency curves of the inverters when considering the device losses, whereas Figure 4.1b shows the loss breakdown at an output power, S_{out} of 110 kVA. The efficiency gain achieved by the SiC MOSFET is clearly noticeable in Figure 4.1a. Besides, the use of SiC MOSFET is more justifiable at higher f_s. While the conduction loss of both devices is somewhat similar, the switching loss is significantly lower in the SiC MOSFET, thanks to its low switching energy. At 50 KHz, the SiC-based inverter enjoys, on average, a 3% higher efficiency when compared to the Si-based inverter. Notably, the switching loss of the SiC MOSFET becomes more dominant than the conduction loss beyond 30 kHz.

4.2 Efficiency at Powertrain Level

In vehicle level modeling and testing, the electric traction drive unit is usually modeled by efficiency maps over the torque–speed envelope of the motor [184, 197]. Therefore, a powertrain level efficiency evaluation of the studied inverters is sought. In this case, the six-phase traction inverter is driving a dual three-phase PMSM, as depicted in Figure 4.2. The PMSM is chosen owing to its superiority in EV applications. The parameters of the PMSM are dynamically modeled using finite element analysis (FEA) that is verified experimentally in [30]. Note that the IPMSM in [30] is rated at a 100 kW, 3 kRPM, 400 V. Thus, its parameters are scaled on a per-unit basis to match the 800 V inverters in this study. A VSD-based field-

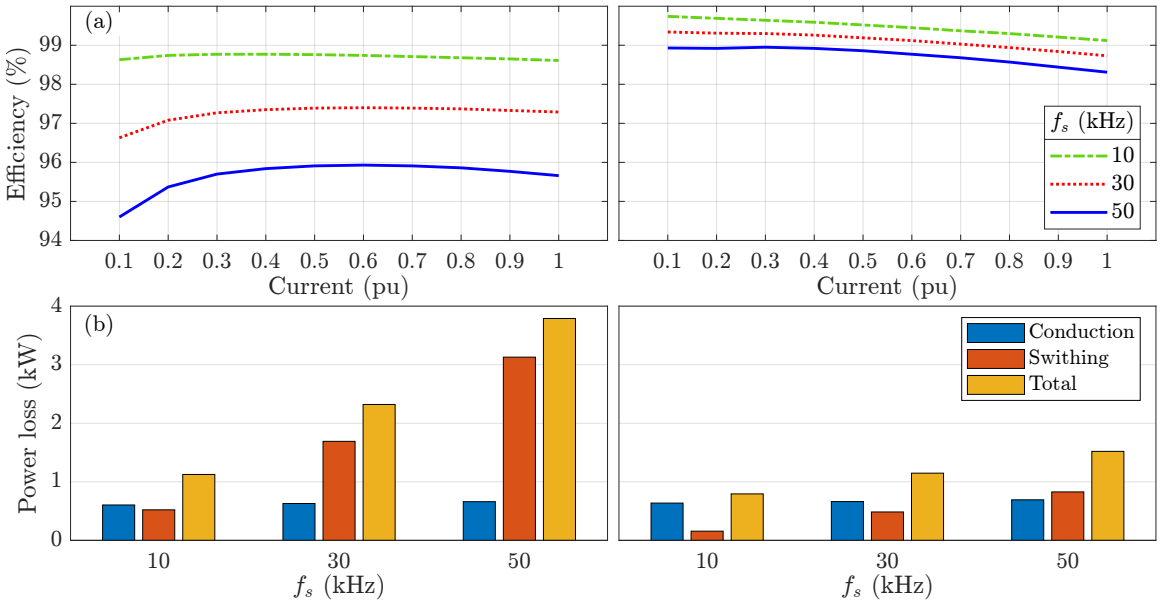


Figure 4.1: Si IGBT (left column) and SiC MOSFET (right column) losses in a 100 kW six-phase inverter. (a) Efficiency vs. load current. (b) Loss breakdown at S_{out} = 110 kVA.

oriented control (FOC) scheme is employed to control the inverter and drive the motor at the desired torque and speed. The inverter controller requires the measured stator current, i_s and rotor position, θ_r. Based on the desired torque and speed, the reference currents in the d–q subspace are generated using look-up tables (LUTs). The LUTs generate the reference currents based on the maximum torque per ampere (MTPA) control and flux-weakening (FW) control at high-speed, using the dynamic parameters of the motor model. As the name suggests, the MTPA control maximizes the torque generation (or minimize stator current) in the constant-torque region of the motor, whereas the FW control weakens the flux in the constant-power region of the motor, where the maximum allowable voltage is reached, by reducing the d-axis current. Motor controls will be studied further in Chapter 8. The reference currents for the x–y subspace are always set to zero. The reference currents are fed to the

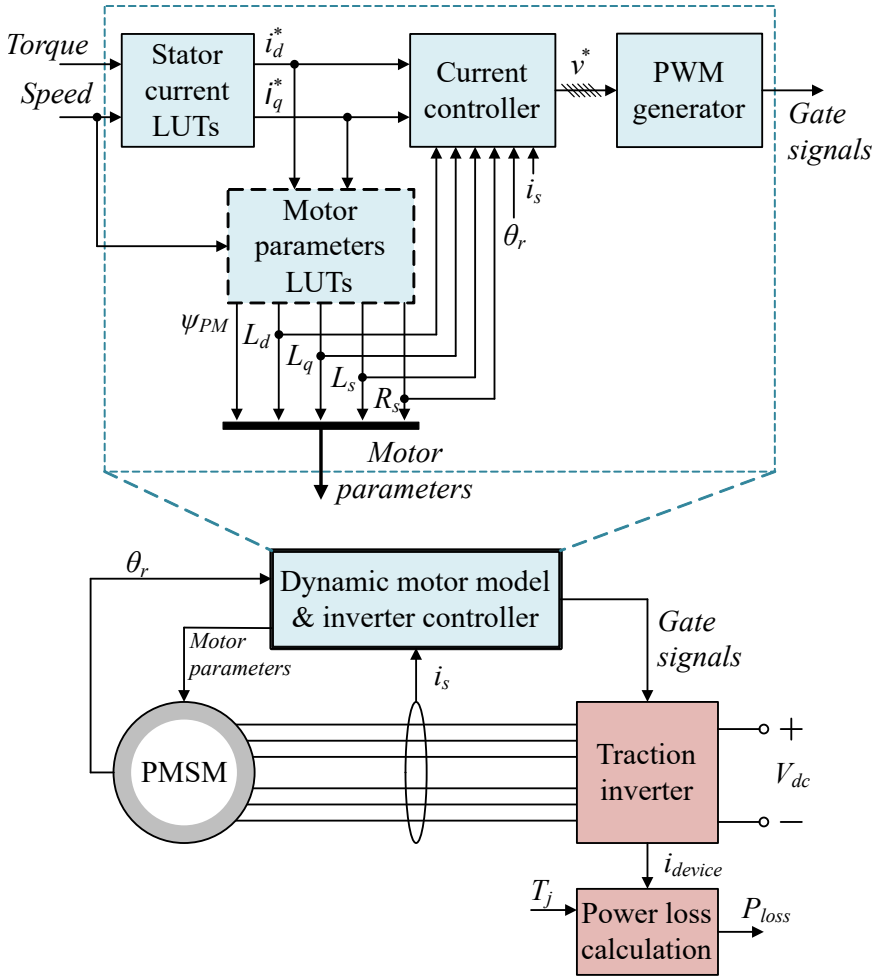


Figure 4.2: Inverter powertrain model using a dynamic model of a dual three-phase PMSM.

current controllers that generate the reference six-phase voltages. Such voltages are then modulated to generate the gate signals. To this end, the red blocks in Figure 4.2 utilize the same PLECS simulation model shown in Figure 3.6 to yield the efficiency information at the specified junction temperature, T_j.

Sweeping the reference torque and speed in the model shown in Figure 4.2 yields a 2D efficiency map for the studied inverter. The testing conditions (f_{sw}, T_j, etc.) for this efficiency evaluation are the same as those in the previous chapter. Figure 4.3

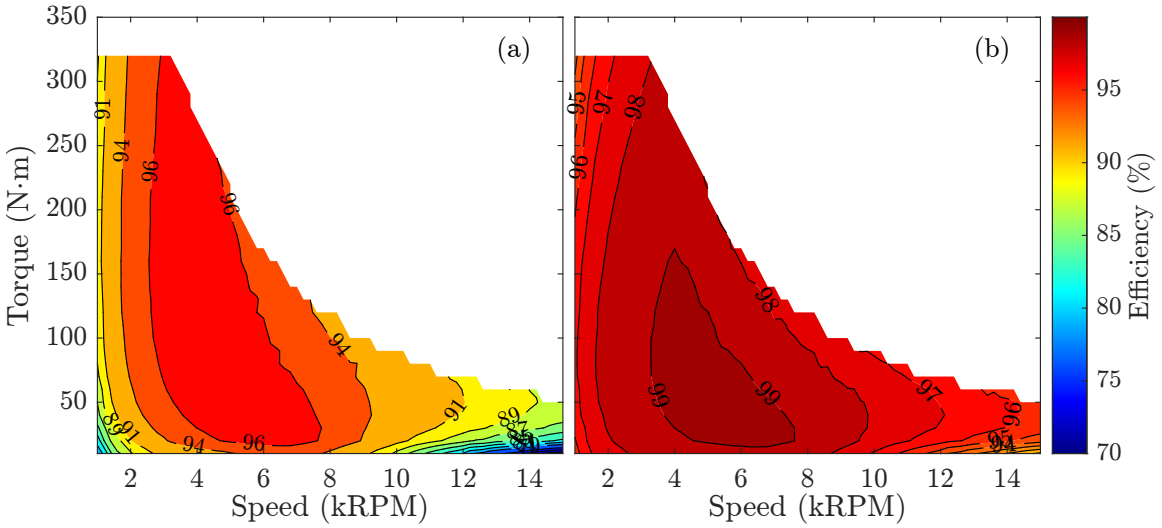


Figure 4.3: Six-phase traction inverters efficiency maps in a 100 kW PMSM drive. (a) Si IGBT. (b) SiC MOSFET.

illustrates the efficiency maps of the Si- and SiC-based inverters. The SiC-based inverter (Figure 4.3b) achieves a higher efficiency overall with a peak efficiency of 99% compared to a peak efficiency of 96% in the Si-based inverter. A more significant efficiency difference is observed in the high-torque/low-speed and low-torque/high-speed regions of the PMSM. The efficiency maps in Figure 4.3 are employed in Section 4.4 in order to evaluate the energy saving of each of the investigated inverter topologies at the vehicle level.

4.3 Electric Vehicle Model

4.3.1 Model Design

Figure 4.4 illustrates the top-level block diagram of the developed vehicle model. The model is divided into three subsystems: (i) the driver, (ii) the vehicle controller,

and (iii) the vehicle plant. In the driver subsystem, the demanded torque is generated using a PI speed controller, based on the instantaneous chassis speed and the reference speed provided by the drive cycle input. The demanded torque is also adjusted to compensate for vehicle losses incurred by rolling resistance, grade, and aerodynamic drag forces. In the vehicle controller subsystem, the torque command, generated by the driver subsystem, is adjusted based on propulsion/braking mode of operation. The vehicle plant includes the model for the battery, electric traction drive system (i.e. traction inverter and motor), final drive, wheels, chassis, and electrical accessories. The current consumed by the electric drive and the electrical accessories are summed and used to calculate the battery output voltage and state of charge (SOC). The electric drive system is modeled by two cascaded efficiency maps for the inverter and the motor. The final drive, wheels and chassis models are used to calculate the instantaneous vehicle speed which is fed-back to the driver. All related modeling equations for the vehicle model depicted in Figure 4.4 can be found in [197]. Table 4.1 lists the vehicle parameters of the Chevrolet Spark used in the developed EV model. This reason for selecting this EV model is its publicly available vehicle parameters and dynamometer performance.

4.3.2 Model Validation

The developed EV model for the Chevrolet Spark is validated by benchmarking its battery data (i.e. voltage, current, and SOC) against the experimental dynamometer data of the actual vehicle reported by Argonne National Laboratory (ANL) [198]. For verification purposes, the electric drive system of the model is loaded with efficiency maps (for the inverter and the motor) for the 2010 Toyota Prius available in [199],

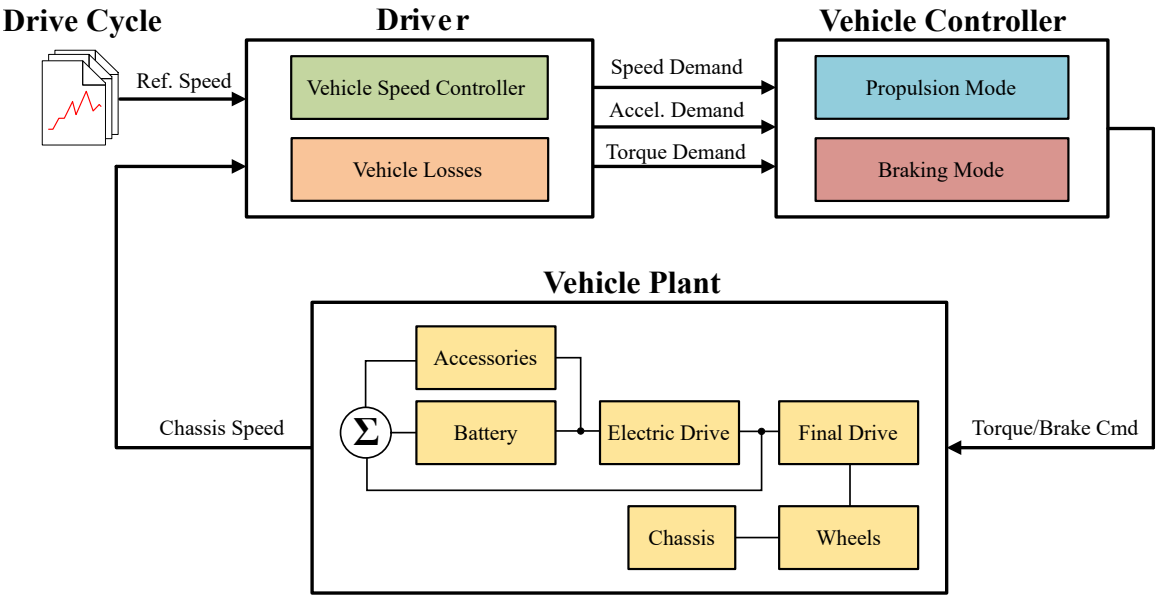


Figure 4.4: Top-level block diagram of the developed EV model built in Simulink.

since such maps are unavailable for the modeled vehicle, i.e. Chevrolet Spark. Nevertheless, the accuracy of the developed EV model is not compromised. To demonstrate its validity, Figure 4.5 shows the simulation results of the EV model versus the experimental data recorded by ANL, for test ID#61508014 as an example. The drive cycle depicted in Figure 4.5 is composed of a constant speed (at 65 mph) for the first 9 mins, followed by a US06 drive cycle. Figure 4.5 demonstrates a strong agreement between the developed EV model and the experimental data.

The model was further validated against four other tests, reported by ANL, that involve universal dynamometer driving schedule (UDDS), highway fuel economy test (HWFET) and US06 drive cycles with different testing conditions, e.g. different grade elevations. The resulting root mean square error (RMSE) between the simulated battery SOC and the experimental ANL data is $0.92 \pm 0.44\%$. Therefore, the developed Chevrolet Spark EV model is very accurate. After validating the EV model, the

Table 4.1: Vehicle parameters of the Chevrolet Spark 2015

Parameter	Value	Parameter	Value
Mass of vehicle	1300 kg	Wheel radius	0.29 m
Vehicle frontal area	2.22 m^2	Wheel inertia	1 kg·m^2
Coefficient of drag	0.32	Vehicle mass on driven axle (ratio)	0.64
Final drive ratio	3.78	Effective wheel radius (ratio)	0.95
Final drive inertia	0.01 kg·m^2	Battery capacity	54 Ah

performance of the investigated inverter topologies is evaluated next at the vehicle level.

4.4 Simulation Results and Discussions

Using the efficiency maps obtained in Figure 4.3 and the EV model developed in the previous section, the EV performance is evaluated for the investigated Si- and SiC-based six-phase inverters on different drive cycles. As mentioned in the previous section, testing of the different inverter topologies entails replacing the efficiency maps in the electric drive system of the EV model (Figure 4.4) with the corresponding efficiency map in Figure 4.3. It is worth highlighting that the vehicle model is based on a three-phase PMSM drive, whereas the current study focuses on six-phase traction inverters. However, since the inverter is only modeled by an efficiency map, the evaluation at the vehicle level remains independent.

Figure 4.6 presents the SOC performance of the EV using the Si- and SiC-based six-phase inverters on a UDDS, HWFET, and US06 drive cycles, respectively. The

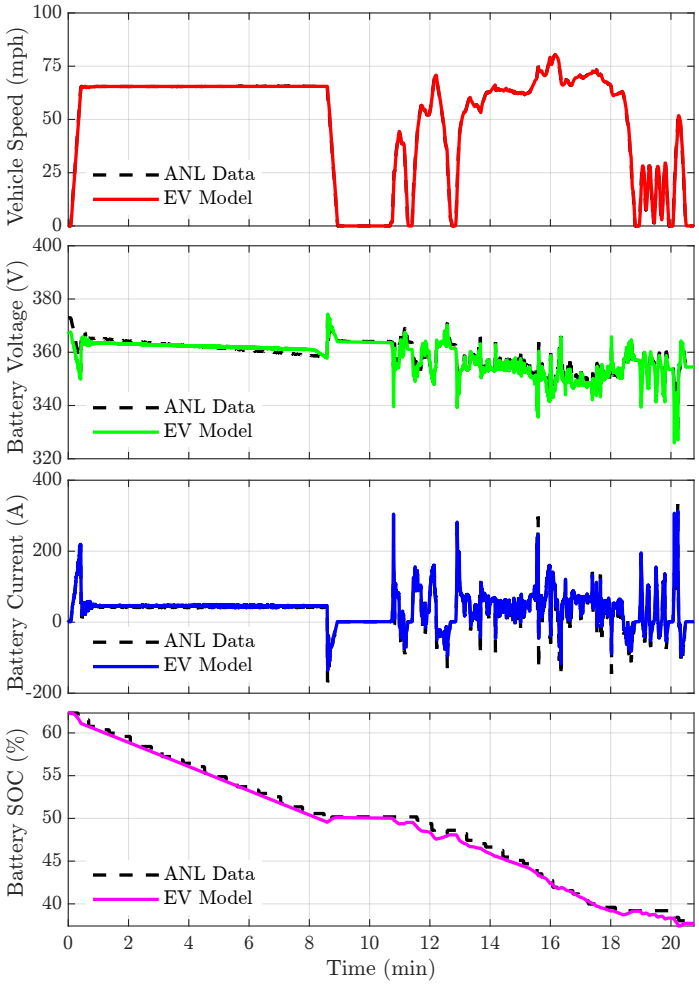


Figure 4.5: EV Model verification by benchmarking its results to the reported data by ANL for Chevrolet Spark, test ID#61508014, showing drive cycle speed, battery voltage, current and SOC.

initial battery's SOC in all tests is assumed 100%. By analyzing the final SOC in Figure 4.6, the SiC-based inverter demonstrates the best utilization of battery SOC. The variation in SOC between different inverter topologies is most pronounced during the UDDS drive cycle and least noticeable during the HWFET drive cycle, with a difference of 0.7% in the former compared to 0.4% in the latter. This is due to repetitive acceleration and deceleration in the UDDS drive cycle, as shown in

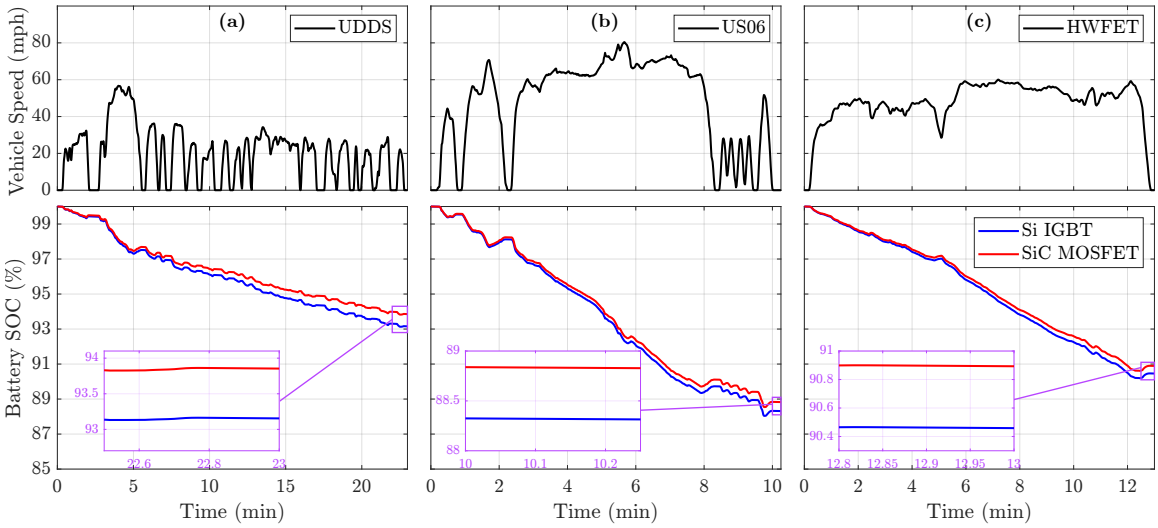


Figure 4.6: Battery SOC of the EV using Si- and SiC-based six-phase inverters. Drive cycles: (a) UDDS, (b) US06, and (c) HWFET.

Figure 4.6a. This requires the electrical drive unit to operate at the corners of the torque–speed envelope, where the efficiency difference between the studied inverters is more apparent, as illustrated in Figure 4.3. In contrast, the HWFET drive cycle emulates low-torque and high-speed driving conditions, where the efficiency difference between the inverters is minimal.

To further analyze the energy consumption of the vehicle when using the different studied inverters, the power drawn from the battery is studied. Table 4.2 lists the energy consumption (kWh/100 km) of the vehicle using the different inverter topologies. The SiC-based inverter offers a 10% energy savings when compared to the Si-based inverter in the UDDS drive cycle, and 4% in the US06 and HWFET drive cycles.

To determine the efficiency the studied traction inverters, vehicle mileage and fuel economy are examined. Firstly, the range of the EV can be calculated as:

$$\text{Range (km)} = \frac{\text{Battery Capacity (Ah)} \times V_{dc}}{\text{Energy Consumption (Wh/km)}} \tag{4.4.1}$$

Table 4.2: EV energy consumption using Si- and SiC-based six-phase traction inverters

Six-Phase Inverter	**Energy Consumption (kWh/100 km)**			
	UDDS	**US06**	**HWFET**	**Combined**[†]
Si IGBT	11.86	18.31	12.01	**11.93**
SiC MOSFET	10.65	17.51	11.47	**11.02**

[†] 0.55 UDDS + 0.45 HWFET

For the particular case of this study (i.e. Chevrolet Spark), the battery capacity is taken from Table 4.1. To determine the combined energy consumption for urban and highway conditions, the US environmental protection agency (EPA) regulations require weighting factors of 55% and 45% for the UDDS and the HWFET drive cycles, respectively [197]. Accordingly, the combined electrical energy consumption values for the different inverter topologies are derived from Table 4.2, and then substituted in (4.4.1) to calculate the mileage range. Secondly, the fuel economy of EVs is determined by the miles per gallon gasoline equivalent (MPGe) metric introduced by the EPA, given as [197]:

$$MPGe = \frac{E_G}{E_M \, E_E} \tag{4.4.2}$$

where E_G is the energy content per gallon of gasoline, E_E is the energy content per watt-hour of electricity, and E_M is the wall-to-wheel electrical energy consumed per mile (Wh/mi). The E_G and E_E are set by the DOE as 11,500 BTUs/gal and 3.412 BTUs/Wh, respectively. The E_M is taken from Table 4.2 for the combined drive cycles. The mileage and fuel economy of the vehicle when using a Si- and SiC-based six-phase traction inverters are reported in Table 4.3. The results demonstrate an 8% improvement in vehicle performance when using the SiC-based inverter.

Table 4.3: Vehicle range and fuel economy using Si- and SiC-based six-phase traction inverters

Six-Phase Inverter	Range (km)	MPGe (gal)
Si IGBT	362	127
SiC MOSFET	392	138

4.5 Summary

This chapter presented a comparative study between a Si- and SiC-based six-phase traction inverter topologies for EV applications. The performance of such inverters was assessed for an 800 V battery voltage. The efficiency of the examined inverter topologies was assessed on the vehicle level in terms of battery SOC and electrical energy consumption over standard drive cycles. It was found that the SiC-based six-phase inverter yields an 8% improvement in vehicle mileage and fuel economy when compared to its Si-based counterpart.

Chapter 5

DC Ripples Analysis and Capacitor Sizing for Six-Phase Inverters

The DC-bus capacitor is an indispensable component of VSI and accounts for one to two thirds the volume of the inverter [117]. Hence, optimizing its size is imperative to improving the power density of the inverter. Capacitor sizing is mainly dictated by two metrics [200]: RMS current ripple and allowable DC-voltage ripple. The current rating of the capacitor must withstand the inverter input current ripple, and its capacitance must be high enough to allow only a small voltage ripple, typically 5%. Engineers and researchers alike depend on mathematical formulas to evaluate those two metrics for a given inverter rating in order to design the capacitor [201]. However, such formulas have not been established for six-phase inverters.

Input voltage and current ripples for three-phase VSIs have been investigated in [201–209]. The fundamentals of DC ripples analysis was outlined in [202] and [203] for various modulation schemes, including SPWM, SVM, and third harmonic injection (THI). It was found that SVM leads to reduced DC voltage ripples when compared to

SPWM for three-phase VSIs. However, the DC current ripple was found to be almost the same [205]. Evaluation of the DC current ripple for switched reluctance motor (SRM) drives was explored in [209]. Spectral analysis of the DC current ripples using double Fourier series was investigated in [204] and [206] for continuous and discontinuous modulation schemes in two-level and multilevel three-phase VSIs. DPWM was observed to result in a higher DC current stress [207]. Multicarrier DPWM was recently suggested in [210] to reduce the DC current ripple, at the expense of increased output current THD. The DC ripples analysis in [202] was extended to unbalanced loads in [208]. Segmentation of three-phase motor windings to from two three-phase drives connected in parallel demonstrated a significant DC ripple current reduction by about 50% [77]. An adaptive minimization modulation technique was proposed in [211] to reduce the DC ripple current further in the segmented motor drive. Lastly, the effect of the reverse recovery of the anti-parallel diodes on the DC voltage and current stresses was studied in [201] and found to be negligible.

Evaluation of input voltage and current ripples for MPIs have been investigated in literature for n odd number of phases. In this case, the spatial distribution of phases is always symmetric with $2\pi/n$ radians between subsequent phases. In [212], the input current ripple and voltage ripple analytical expressions for five-phase VSI were derived and verified experimentally. Additionally, the authors found that SPWM yields the minimum input voltage ripple. In [213–215], the peak-to-peak voltage ripple amplitude was analytically derived for five- and seven-phase VSIs. The derived peak-to-peak voltage ripple expressions enable visualizing the instantaneous ripple envelope experienced by the DC-bus capacitor. The authors considered two modulation schemes: SPWM and SVM, and their impact on voltage ripple was examined. In

contrast to conventional three-phase VSI [202], the reported results showed no tangible attenuation in voltage ripples when using SVM over SPWM. On the contrary, at high modulation index, SPWM led to reduced voltage ripples in [213] in seven-phase VSI when compared to SVM, which is in line with the findings in [212] for five-phase VSIs. Numerical analysis of input and output current ripples of nine-phase VSI was attempted in [216] using conventional SPWM and dual-carrier PWM. The authors claimed a reduced input and output current ripple for asymmetric loads with dual-carrier PWM.

For $n = 6$, fewer studies were reported. In [217], input current ripple for six-phase VSI with arbitrary spatial displacement angle, δ between the two three-phase sets was examined. It was found that the input current ripple is minimal when the load is symmetric (i.e. $\delta = \pi/3$). Therefore, unlike n-phase inverters with odd number of phases, input current stress is a function of δ for six-phase VSI. Analytical expression of the input current ripple for six-phase VSI with symmetric load was derived in [217]. In [218], the input current ripple analytical expressions were given for six-phase VSI supplying split ($\delta = 0$), asymmetric ($\delta = \pi/6$), and open-end winding machines with a single power source. However, mathematical derivations were not outlined for all cases.

A generalized model for the DC-bus capacitor in MPIs with $n > 3$ phases was reported in [63]. The modeling assumed symmetric and balanced loads operating in the linear modulation region. Accordingly, a comparative analysis for the DC-capacitor, in terms of input voltage and current ripples, was presented. Also, the effects of modulation scheme (SPWM vs. SVM), carrier waveform (triangular vs.

sawtooth) and interleaving techniques on voltage ripples were examined for nine-phase VSI. The authors reported a potential for DC-bus capacitor size reduction in nine-phase VSI of up to two-thirds when using SVM with three interleaving triangular carriers. In interleaved multi-carrier PWM, the n phases are divided into p groups of 3-phases. A multiple of p carriers, shifted by δ degrees, can be used to modulate three signals to generate the gate pulses for n switches. The same strategy was implemented and reported in [76] for $n = 15$. However, the same did not apply to six-phase VSIs; no improvement was observed with two interleaving triangular carriers [63].

To this end, there exists a gap in knowledge for input current and voltage ripples in six-phase VSIs with different load configurations (i.e. different δ). More specifically, input current ripple analysis was partially covered in [217] and [218] for symmetric and asymmetric loads, respectively. Furthermore, to the best of the authors' knowledge, input voltage ripple for six-phase VSI was not examined for any load configuration, and therefore, their analytical formulas have not been established yet. Subsequently, this chapter fills in this gap by delivering:

1. A thorough analysis of input current ripple analysis for symmetric and asymmetric six-phase loads, along with analytical formulas;

2. Mathematical formulas derivation of input voltage ripple for symmetric and asymmetric six-phase VSIs;

3. Experimental validation of derived formulas at various PFs and modulation indices;

4. Capacitor design rules for six-phase VSIs based on maximum DC voltage and DC current stresses.

The foregoing contributions enables the designer to properly size the DC-bus capacitor in six-phase VSIs in order to achieve the best power density. The remainder of the chapter is organized as follows. Six-phase VSI modeling with symmetric and asymmetric loads is reviewed in Section 5.1. Derivations of DC-capacitor current and voltage ripples are investigated in Sections 5.2 and 5.3, respectively. DC-capacitor design rules for six-phase inverters are derived in Section 5.4. Simulation and experimental validations of derived analytical formulas and benchmarking against conventional three-phase VSI are presented in Section 5.5. Finally, concluding remarks are outlined in Section 5.6.

5.1 Six-Phase VSI Modeling

The schematic of the six-phase VSI is depicted in Figure 5.1. The DC supply is assumed constant and is connected through a line impedance, $Z_{dc} = R_{dc} + j\omega_s L_{dc}$, where ω_s is the switching angular frequency. The six-phase load/motor windings, ABC_1 and ABC_2, can be configured as split ($\delta = 0$), symmetric ($\delta = \pi/3$), or asymmetric ($\delta = \pi/6$) manner. Asymmetric six-phase machines are the most popular among the three configurations owing to reduced torque pulsation [36]. On the other hand, symmetric six-phase machines have been finding application in EVs for their superior fault-tolerance capability [219–221]. Split configuration is the least popular as it exhibits the worst fault-tolerance capability. Moreover, no DC ripples reduction over three-phase system is obtained using split configuration [217], and therefore was not considered in this thesis. Figure 5.2 shows the symmetric and asymmetric six-phase configurations. The modulating voltage signals and fundamental phase currents

of the six-phase inverter are given in (5.1.1) and (5.1.2), respectively.

$$\begin{aligned}
v_{A1} &= M\sin\theta + v_0 \\
v_{B1} &= M\sin\left(\theta - \frac{2}{3}\pi\right) + v_0 \\
v_{C1} &= M\sin\left(\theta + \frac{2}{3}\pi\right) + v_0 \\
v_{A2} &= M\sin\left(\theta - \delta\right) + v_0 \\
v_{B2} &= M\sin\left(\theta - \frac{2}{3}\pi - \delta\right) + v_0 \\
v_{C2} &= M\sin\left(\theta + \frac{2}{3}\pi - \delta\right) + v_0
\end{aligned} \tag{5.1.1}$$

$$\begin{aligned}
i_{A1} &= \sqrt{2}I_L\sin\left(\theta - \phi\right) \\
i_{B1} &= \sqrt{2}I_L\sin\left(\theta - \frac{2}{3}\pi - \phi\right) \\
i_{C1} &= \sqrt{2}I_L\sin\left(\theta + \frac{2}{3}\pi - \phi\right) \\
i_{A2} &= \sqrt{2}I_L\sin\left(\theta - \phi - \delta\right) \\
i_{B2} &= \sqrt{2}I_L\sin\left(\theta - \frac{2}{3}\pi - \phi - \delta\right) \\
i_{C2} &= \sqrt{2}I_L\sin\left(\theta + \frac{2}{3}\pi - \phi - \delta\right)
\end{aligned} \tag{5.1.2}$$

where $\theta = 2\pi f_1 t$ and f_1 is the fundamental frequency, ϕ is the angle between the phase voltage and phase current (i.e. PF angle), δ is the phase displacement angle between the two three-phase sets ($\delta = \pi/3$ and $\pi/6$ for symmetric and asymmetric spatial displacements, respectively), I_L is the RMS load current, M is the modulation index, and v_0 is an arbitrary zero-sequence voltage.

The DC-capacitor current, i_c is obtained from Figure 5.1 and given in (5.1.3). Decomposing i_c, the input DC current, i_{dc}, and the inverter input current, i_{inv} into

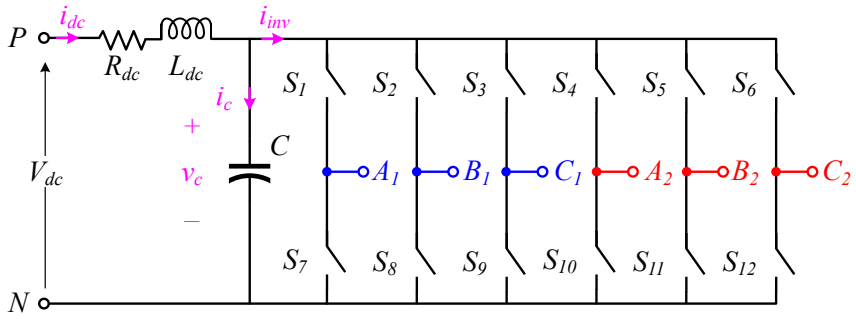


Figure 5.1: Schematic diagram of a six-phase voltage source inverter (VSI).

average and ripple components, (5.1.3) can be re-written as given in (5.1.4) [202]. The average current components are represented by capital letter and a $\bar{}$ accent, whereas ripple components are represented by a $\tilde{}$ accent. Moreover, by equating the right- and left-hand sides of (5.1.4), it can be decomposed into average only and ripple only expressions, as given in (5.1.5) and (5.1.6), respectively.

$$i_c = i_{dc} - i_{inv} \tag{5.1.3}$$

$$\bar{I}_c + \tilde{i}_c = \bar{I}_{dc} + \tilde{i}_{dc} - \bar{I}_{inv} - \tilde{i}_{inv} \tag{5.1.4}$$

$$\bar{I}_c = \bar{I}_{dc} - \bar{I}_{inv} \tag{5.1.5}$$

$$\tilde{i}_c = \tilde{i}_{dc} - \tilde{i}_{inv} \tag{5.1.6}$$

In steady-state, the average capacitor current is zero (i.e. $\bar{I}_c = 0$). It follows that $\bar{I}_{dc} = \bar{I}_{inv}$. Additionally, if the capacitance of the DC-bus capacitor, C is large enough to filter most of the ripple of the DC input current, then $\tilde{i}_{dc} \simeq 0$. It follows that

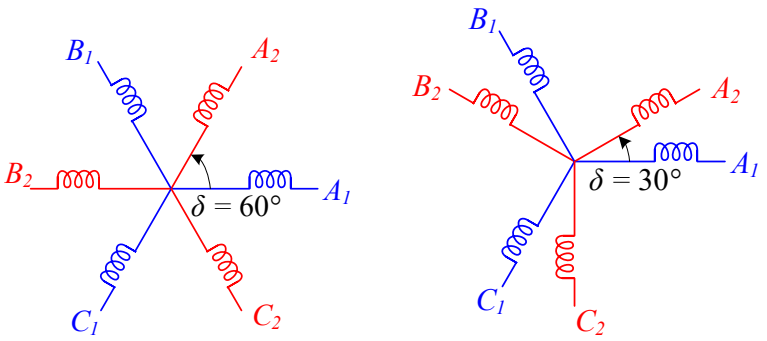


Figure 5.2: Six-phase winding configurations. (a) Symmetric. (b) Asymmetric.

$\tilde{i}_c \simeq -\tilde{i}_{inv}$. Therefore, the DC-bus current ripple can be analyzed by analyzing i_{inv}. The i_{inv} can be defined in terms of the output phase currents and the switching states of the inverter legs as [63]:

$$i_{inv} = \sum_{x} i_x \times S_x \tag{5.1.7}$$

where $x \in \{A1, B1, C1, A2, B2, C2\}$, i_x is the inverter output currents, and S_x is a Boolean switching function that models the ON/OFF state of the switch, and can be expressed as:

$$S_x = \begin{cases} 1, & \textit{top switch is ON} \\ 0, & \textit{bottom switch is ON} \end{cases} \tag{5.1.8}$$

Next, we develop the numerical expressions of i_{inv} and its average and ripple components for the symmetric and asymmetric spatial displacements in six-phase VSI.

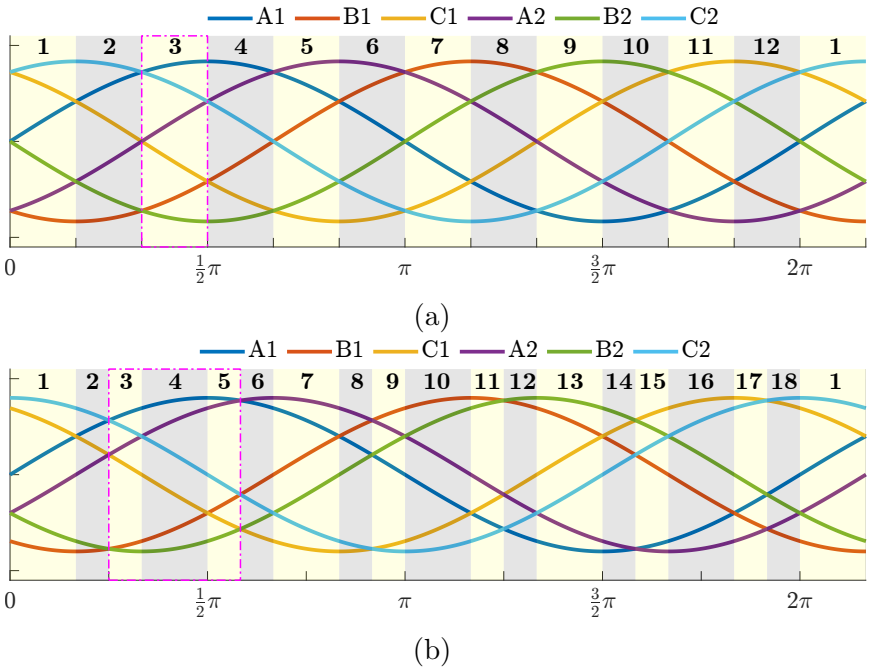


Figure 5.3: Six-phase waveforms with corresponding modes of operation within one fundamental period. (a) Symmetric load. (b) Asymmetric load.

5.2 DC-Bus Current Ripples

The derivations of the DC-bus current ripples herein assumes sinusoidal output current, which is a valid assumption when the switching frequency, f_s is very high. This is typically the case in low to medium voltage applications. The current ripple analysis in this section considers symmetric and asymmetric loads. Figure 5.3 shows the output sinusoidal current waveforms for symmetric and asymmetric six-phase configurations. Additionally, when the modulation frequency $m_f = f_s/f_1$ is very high, the reference voltages can be treated as constants within one switching period, T_s [202]. Owing to its simplicity and wide application, the modulation technique considered in the derivation is SPWM with a triangular carrier, $v_{cr} \in [-1, 1]$.

5.2.1 Symmetric Configuration

When the six-phase VSI is connected to a load (machine) with symmetric spatial displacement (windings), i_{inv} has 12 unique modes of operation in one fundamental cycle, as shown in Figure 5.3a. Those modes are evenly distributed with $\pi/6$ intervals. Figure 5.4 shows the detailed PWM and switching states of the upper switches, along with i_{inv} and v_c when the inverter is in Mode 3 ($\pi/3$ to $\pi/2$). From (5.1.7) and Figure 5.4, i_{inv} can be expressed as given in (5.2.1). Also, from Figure 5.4, the relationship between the dwell times, T_0 to T_6 and T_s can be defined as given in (5.2.2) [202].

$$i_{inv} = \begin{cases} 0, & \text{for } t_0 \le t < t_1 \\ i_{A1}, & \text{for } t_1 \le t < t_2 \\ i_{A1} + i_{C2}, & \text{for } t_2 \le t < t_3 \\ i_{A1} - i_{B2}, & \text{for } t_3 \le t < t_4 \\ -(i_{B1} + i_{B2}), & \text{for } t_4 \le t < t_5 \\ -i_{B2}, & \text{for } t_5 \le t < t_6 \\ 0, & \text{for } t_6 \le t < t_8 \\ -i_{B2}, & \text{for } t_8 \le t < t_9 \\ -(i_{B1} + i_{B2}), & \text{for } t_9 \le t < t_{10} \\ i_{A1} - i_{B2}, & \text{for } t_{10} \le t < t_{11} \\ i_{A1} + i_{C2}, & \text{for } t_{11} \le t < t_{12} \\ i_{A1}, & \text{for } t_{12} \le t < t_{13} \\ 0, & \text{for } t_{13} \le t < t_{14} \end{cases} \tag{5.2.1}$$

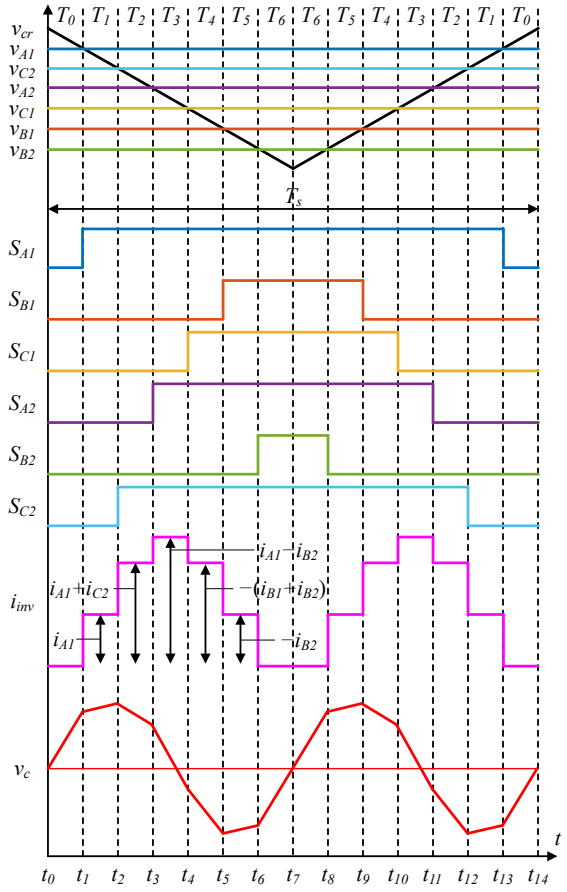


Figure 5.4: Symmetric six-phase VSI: switching pulses of upper switches, $S_{ABC1,ABC2}$, inverter input current, i_{inv}, and capacitor voltage, v_c during one switching period in Mode 3.

$$
\begin{aligned}
T_0 &= \frac{T_s}{4}(1 - v_{A1}) \\
T_1 &= \frac{T_s}{4}(v_{A1} - v_{C2}) \\
T_2 &= \frac{T_s}{4}(v_{C2} - v_{A2}) \\
T_3 &= \frac{T_s}{4}(v_{A2} - v_{C1}) \\
T_4 &= \frac{T_s}{4}(v_{C1} - v_{B1}) \\
T_5 &= \frac{T_s}{4}(v_{B1} - v_{B2}) \\
T_6 &= \frac{T_s}{4}(1 + v_{B2})
\end{aligned}
\tag{5.2.2}
$$

The mean square value of i_{inv} is defined as [202]:

$$
\begin{aligned}
I_{inv}^2 &= \frac{1}{T_s}\int_{t_0}^{t_0+T_s} i_{inv}^2 \, dt \\
&= \frac{2T_1}{T_s} i_{A1}^2 + \frac{2T_2}{T_s}\Big(i_{A1} + i_{C2}\Big)^2 + \frac{2T_3}{T_s}\Big(i_{A2} - i_{B2}\Big)^2 + \frac{2T_4}{T_s}\Big(i_{B1} + i_{B2}\Big)^2 + \frac{2T_5}{T_s} i_{B2}^2
\end{aligned}
\tag{5.2.3}
$$

Substituting (5.1.1)–(5.1.2) and (5.2.1)–(5.2.2) in (5.2.3), the average square value of (5.2.3) can be computed as:

$$
I_{inv,avg}^2 = \frac{6}{\pi}\int_{\pi/3}^{\pi/2} I_{inv}^2 \, d\theta \tag{5.2.4}
$$

Since the inverter is connected to a symmetric load, the average value over the other eleven 60° intervals (Figure 5.3a) is the same. The average inverter input current, $\bar{I}_{inv}$ can be derived from the power balance between the AC and DC sides of the inverter, neglecting power loss. Therefore:

$$
\bar{I}_{inv} = \frac{3}{\sqrt{2}} M I_L \cos\phi \tag{5.2.5}
$$

At last, the RMS value of the inverter input current ripple, $\tilde{I}_{inv}$ is computed as:

$$\begin{aligned}\tilde{I}_{inv} &= \sqrt{I_{inv,avg}^2 - \bar{I}_{inv}^2} \\ &= I_L\left\{\frac{M}{\pi}\left[3+3\sqrt{3}-\frac{9\pi}{4}M+\underbrace{(11\sqrt{3}-19)}_{\approx 0}\sin 2\phi+\left(4+2\sqrt{3}-\frac{9\pi}{4}M\right)\cos 2\phi\right]\right\}^{1/2} \\ &= I_L\left\{\frac{M}{\pi}\left(3+3\sqrt{3}-\frac{9\pi}{4}M+\left(4+2\sqrt{3}-\frac{9\pi}{4}M\right)\cos 2\phi\right)\right\}^{1/2}\end{aligned} \tag{5.2.6}$$

5.2.2 Asymmetric Configuration

When the six-phase VSI is connected to a load (machine) with asymmetric spatial displacement (windings), i_{inv} has 18 unique modes of operation in one fundamental cycle, as shown in Figure 5.3b. That is *six* additional modes when compared to the symmetric case. Unlike symmetric loads, the modes are not evenly distributed. Six out of the 18 modes span an interval of $\pi/6$ (Modes 1, 4, 7, 10, 13, and 16 in Figure 5.3b), whereas the other intervals span an interval of $\pi/12$. The former and later modes are henceforth called *large modes* and *small modes*, respectively. In between two consecutive large modes, there are two small modes. If *large* and *small* modes were to be represented by '1' and '0', then the sequence of modes for asymmetric currents would be '100100...' In light of this breakdown of modes of operation, three intervals are required to derive the DC-current ripple. In this analysis, Modes 3–5 are considered, as shown in Figure 5.3b. Figure 5.5 shows the detailed PWM and switching states of the upper switches, along with i_{inv} and v_c when the inverter is in Mode 3 ($\pi/4$ to $\pi/3$) and Mode 4 ($\pi/3$ to $\pi/2$) for asymmetric spatial displacement. Note that the vertical spacing between phase voltages in Figure 5.5 is due to asymmetry.

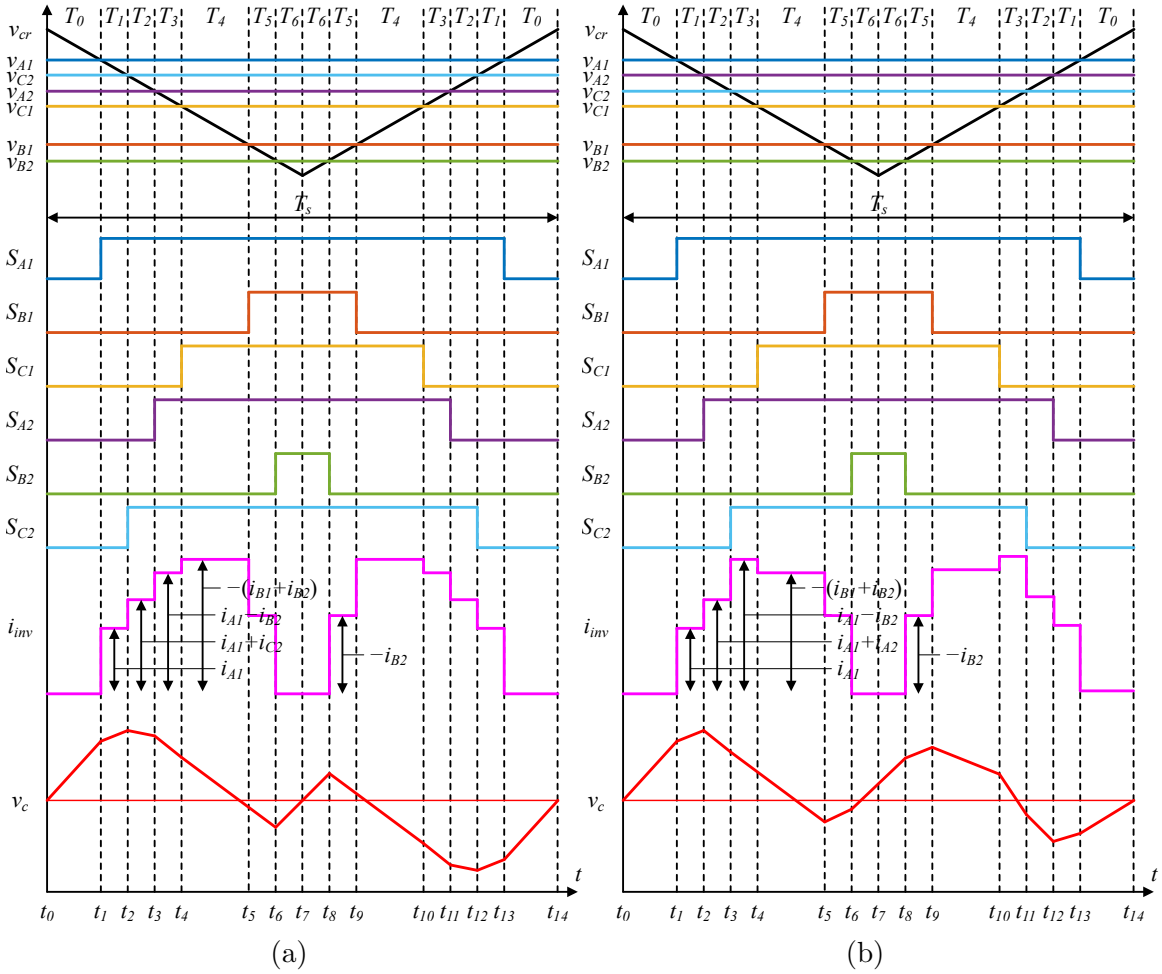


Figure 5.5: Asymmetric six-phase VSI: switching pulses of upper switches, $S_{ABC1,ABC2}$, inverter input current, i_{inv}, and capacitor voltage, v_c during one switching period in (a) Mode 3 and (b) Mode 4.

The i_{inv} and dwell times for Modes 3 and 4, can be deduced from Figure 5.5 in the same manner discussed in the previous subsection. Let us start by analyzing the operation in Mode 3. From Figure 5.5a, i_{inv} is similar to that of the symmetric case in Figure 5.4, with uneven dwell times in the former due to asymmetry. Nevertheless, the mathematical derivations for the symmetric operation in Mode 3 in (5.2.1)–(5.2.3) are equally applicable to the asymmetric case in the same mode. Hence, the derivations

for Mode 3 for the asymmetric configuration are not given for brevity. Furthermore, the $I^2_{inv,avg}$ in (5.2.4) is also the same for small intervals.

Regarding Mode 4, from (5.1.7) and Figure 5.5a, the inverter input current in Mode 4 can be expressed as given in (5.2.7), where the '4' subscript in i_{inv4} denotes operation in Mode 4, to distinguish it from that of Mode 3, denoted with '3' subscript. The dwell times in Mode 4, are defined in (5.2.8).

$$i_{inv4} = \begin{cases} 0, & \text{for } t_0 \le t < t_1 \\ i_{A1}, & \text{for } t_1 \le t < t_2 \\ i_{A1} + i_{A2}, & \text{for } t_2 \le t < t_3 \\ i_{A1} - i_{B2}, & \text{for } t_3 \le t < t_4 \\ -(i_{B1} + i_{B2}), & \text{for } t_4 \le t < t_5 \\ -i_{B2}, & \text{for } t_5 \le t < t_6 \\ 0, & \text{for } t_6 \le t < t_8 \\ -i_{B2}, & \text{for } t_8 \le t < t_9 \\ -(i_{B1} + i_{B2}), & \text{for } t_9 \le t < t_{10} \\ i_{A1} - i_{B2}, & \text{for } t_{10} \le t < t_{11} \\ i_{A1} + i_{A2}, & \text{for } t_{11} \le t < t_{12} \\ i_{A1}, & \text{for } t_{12} \le t < t_{13} \\ 0, & \text{for } t_{13} \le t < t_{14} \end{cases} \tag{5.2.7}$$

$$
\begin{aligned}
T_0 &= \frac{T_s}{4}(1 - v_{A1}) \\
T_1 &= \frac{T_s}{4}(v_{A1} - v_{A2}) \\
T_2 &= \frac{T_s}{4}(v_{A2} - v_{C2}) \\
T_3 &= \frac{T_s}{4}(v_{C2} - v_{C1}) \\
T_4 &= \frac{T_s}{4}(v_{C1} - v_{B1}) \\
T_5 &= \frac{T_s}{4}(v_{B1} - v_{B2}) \\
T_6 &= \frac{T_s}{4}(1 + v_{B2})
\end{aligned}
\tag{5.2.8}
$$

Intermediate steps involving mean square value of i_{inv4} derivations are similar to those in (5.2.3), and hence are not repeated. For Mode 5, the same derivations in Mode 3 apply, being another *small mode*, yet with different dwell times. For space limitation, derivations of Mode 5 are not given.

The average square value of the inverter input current over one fundamental cycle is computed using the weighted average of Modes 3–5 as:

$$
\begin{aligned}
I^2_{inv,avg} &= \frac{1}{4}\Big(I^2_{inv3,avg} + 2I^2_{inv4,avg} + I^2_{inv5,avg}\Big) \\
&= \frac{3}{\pi}\int_{\pi/4}^{\pi/3} I^2_{inv3}\, d\theta + \frac{3}{\pi}\int_{\pi/3}^{\pi/2} I^2_{inv4}\, d\theta + \frac{3}{\pi}\int_{\pi/2}^{7\pi/12} I^2_{inv5}\, d\theta
\end{aligned}
\tag{5.2.9}
$$

The RMS value of the inverter input current ripple for the asymmetric six-phase inverter is [218]:

$$
\tilde{I}_{inv} = I_L\left\{\frac{M}{2\pi}\left[2\big(\sqrt{3}-\sqrt{2}\big) + \sqrt{6} + \Big(4\sqrt{2} + 8\sqrt{3} + 4\sqrt{6} - 9\pi M\Big)\cos^2\phi\right]\right\}^{1/2}
\tag{5.2.10}
$$

Note that v_0 cancels out in $\tilde{I}_{inv}$ in (5.2.6) and (5.2.10). Therefore, $\tilde{I}_{inv}$ cannot be made smaller using SVM, or any other zero-sequence injection technique. Also, $\tilde{I}_{inv}$ is independent of C and f_s, but rather a function of I_L, M, and PF only. Put otherwise, $\tilde{I}_{inv}$ cannot be reduced by increasing the switching frequency or enlarging the DC-bus capacitor. This is not the case for voltage ripples, as will be shown next.

5.2.3 Harmonic Spectrum Comparison

Comparing the analytical expressions in (5.2.6) and (5.2.10), the behavior of $\tilde{I}_{inv}$ is obviously different for the symmetric and asymmetric six-phase loads. Further analysis, in terms of harmonic spectrum, is sought to identify the underlying reasons for this difference. The analysis is conducted with respect to the conventional three-phase VSI to provide a benchmark measure for the six-phase counterpart. Furthermore, the following analysis can be generalized to any $3k$-phase systems ($k \in [1, 2, \dots]$).

Six-phase systems can be treated as dual three-phase systems with a phase displacement δ between the two sets of three-phases. As such, (5.1.7) can be re-written as:

$$\begin{aligned} i_{inv} &= \sum_{x1} i_{x1} \times S_{x1} + \sum_{x2} i_{x2} \times S_{x2} \\ &= i_{inv_1} + i_{inv_2} = i_{inv}\angle 0 + i_{inv}\angle \delta \end{aligned} \tag{5.2.11}$$

where $x1 \in \{A1, B1, C1\}$, $x2 \in \{A2, B2, C2\}$, and $i_{inv_{1,2}}$ is the inverter input current for each of the three-phase sets. Since the input DC current is the superposition summation of all phase-leg currents, the fundamental, the second harmonic, and all triplen carrier-sidebands get cancelled for balanced three-phase loads [206]. Hence, $\tilde{i}_{inv_1}$ only includes switching carrier harmonics and non-triplen sidebands. The presence of i_{inv_2}

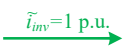
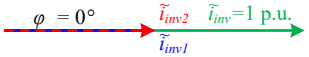
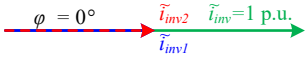
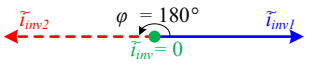
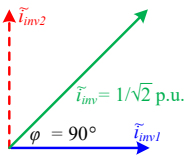
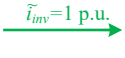
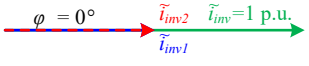
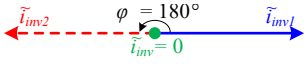
in six-phase systems affect the remaining harmonics. The harmonic content of the input DC-current ripple in three-phase VSI (i.e. i_{inv_1}), shown in Figure5.6a, can be categorized into three groups:

- **Group 1**: carrier harmonics, mf_s with even m;
- **Group 2**: sideband harmonics, $mf_s \pm nf_1$ with odd m and triplen n;
- **Group 3**: sideband harmonics, $mf_s \pm nf_1$ with even m and $n = 6k$, $k \in \mathbb{N}$.

For six-phase VSI, Group 1 harmonics are equal to those in the three-phase VSI, irrespective of load configuration. This is because each three-phase set (i.e. ABC_1 and ABC_2) produces harmonics of equal magnitude and zero phase shift (i.e. $\tilde{i}_{inv1} = \tilde{i}_{inv2}$), thus they sum up. Yet, the magnitude of each of them is half of that of the three-phase VSI for the same VA rating.

For six-phase VSI with symmetric loads (Figure 5.6b), Group 2 harmonics get eliminated. The magnitude of such harmonics from each three-phase set (i.e. ABC_1

Table 5.1: Harmonic spectrum comparison between symmetric and asymmetric six-phase VSI by harmonic groups

Harmonic Group*	**Three-Phase System**	**Six-Phase Configuration**	
		Symmetric	**Asymmetric**
Group 1			
Group 2			
Group 3			

*Normalized $\tilde{i}_{inv}$ per harmonic group to their three-phase equivalent

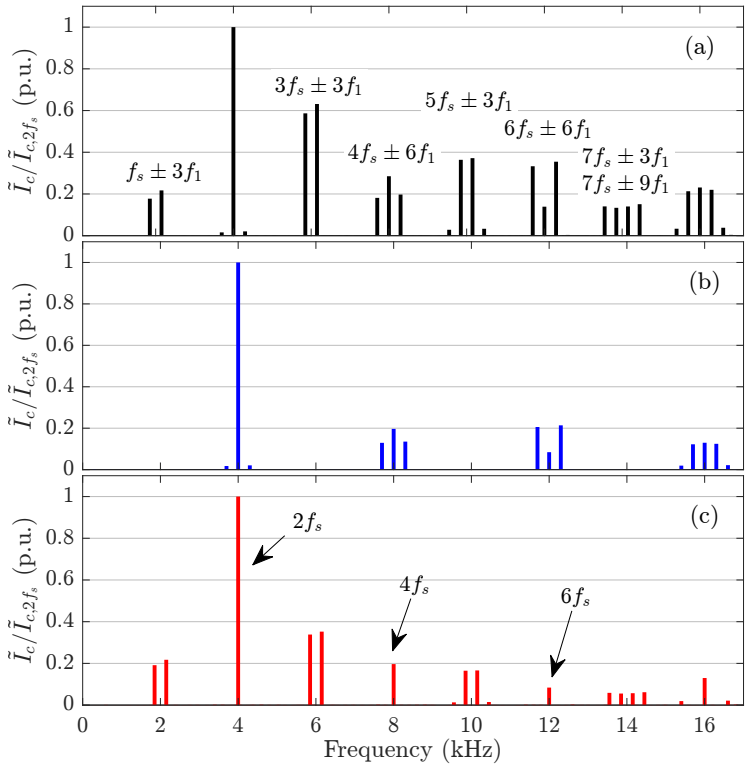


Figure 5.6: Simulated harmonic spectra of input current ripple, $\tilde{I}_{inv}$ for three- and six-phase VSIs of the same VA rating (f_1 = 50 Hz, f_s = 2 kHz, PF = 0.6, M = 0.7). (a) Three-phase VSI. Six-phase VSI with (b) symmetric load and (c) asymmetric load.

and ABC_2) is equal but 180° out of phase (i.e. $\tilde{i}_{inv1} = -\tilde{i}_{inv2}$). Hence, they cancel out due to symmetry. This originates from $\delta = \pi/3$ for symmetric six-phase loads. So, Group 2 harmonics of the second three-phase set (i.e. ABC_2) are phase shifted by $\varphi = n\delta = n\pi$, for triplen n. On the other hand, Group 2 harmonics are 90° out of phase for six-phase VSI with asymmetric loads. In this case, $\delta = \pi/6$ and $\varphi = n\delta = n(\pi/2)$, for triplen n. Thus, their per-unit magnitude sum is $\sqrt{2}$. But since the phase current in six-phase systems is half of that of three-phase ones, the resulting magnitude of such harmonics are reduced by a factor of $1/\sqrt{2}$ (Figure 5.6c).

Group 3 harmonics in each of the three-phase sets of the six-phase VSI with

symmetric loads are in-phase (i.e. $\varphi = n\delta = n2\pi$ for $\delta = \pi/3$ and $n = 6k$), and thus remain the same, for the same reason as Group 1 (i.e. the halves add up). However, such harmonics are 180° out of phase for six-phase VSI with asymmetric loads, hence they cancel out (i.e. $\varphi = n\delta = n\pi$ for $\delta = \pi/6$ and $n = 6k$).

In summary, each of the different six-phase configurations contain only two out of the three harmonic groups in three-phase VSI, with even multiples of carrier harmonics being mutual in both six-phase loads. Yet the harmonics eliminated in the six-phase symmetric load (i.e. Group 2) are more dominant than those eliminated in the asymmetric load (i.e. Group 3). Therefore, six-phase VSI with symmetric loads yields the lowest DC-capacitor RMS current.

Table 5.1 summarizes the vector diagrams of the different harmonic groups of the input DC current ripple in the symmetric and asymmetric six-phase VSI. This analysis is extended to nine-phase inverters in [222].

5.3 DC-Bus Voltage Ripples

After deriving numerical expressions for the DC-capacitor RMS current ripple in the previous section (recall $\tilde{i}_c \simeq -\tilde{i}_{inv}$), numerical expressions for the DC-capacitor voltage ripple, $\tilde{v}_c$ are now sought for symmetric and asymmetric six-phase configurations. The $\tilde{v}_c$ can be defined as [202]:

$$\tilde{v}_c = \frac{1}{C}\int \tilde{i}_c \, dt = \frac{1}{C}\int \left(\bar{I}_{inv} - i_{inv}\right) dt \tag{5.3.1}$$

5.3.1 Symmetric Configuration

The $\tilde{v}_c$ can be obtained by substituting (5.2.1) in (5.3.1). This yields $\tilde{v}_c$ in (5.3.2), with $C_i = v_i(t_i), \quad i \in \{1, 2, ..., 5\}$.

$$\tilde{v}_c = \frac{\bar{I}_{inv}}{C} \begin{cases} v_0 = t - t_0, & \text{for } t_0 \le t < t_1 \\ v_1 = \left(1 - \frac{i_{A1}}{\bar{I}_{inv}}\right)(t - t_1) + C_1, & \text{for } t_1 \le t < t_2 \\ v_2 = \left(1 - \frac{i_{A1}+i_{C2}}{\bar{I}_{inv}}\right)(t - t_2) + C_2, & \text{for } t_2 \le t < t_3 \\ v_3 = \left(1 - \frac{i_{A1}-i_{B2}}{\bar{I}_{inv}}\right)(t - t_3) + C_3, & \text{for } t_3 \le t < t_4 \\ v_4 = \left(1 + \frac{i_{B1}+i_{B2}}{\bar{I}_{inv}}\right)(t - t_4) + C_4, & \text{for } t_4 \le t < t_5 \\ v_5 = \left(1 + \frac{i_{B2}}{\bar{I}_{inv}}\right)(t - t_5) + C_5, & \text{for } t_5 \le t < t_6 \\ v_6 = t - t_7, & \text{for } t_6 \le t < t_8 \\ \left(1 + \frac{i_{B2}}{\bar{I}_{inv}}\right)(t - t_5) - C_5, & \text{for } t_8 \le t < t_9 \\ \left(1 + \frac{i_{B1}+i_{B2}}{\bar{I}_{inv}}\right)(t - t_4) - C_4, & \text{for } t_9 \le t < t_{10} \\ \left(1 - \frac{i_{A1}-i_{B2}}{\bar{I}_{inv}}\right)(t - t_3) - C_3, & \text{for } t_{10} \le t < t_{11} \\ \left(1 - \frac{i_{A1}+i_{C2}}{\bar{I}_{inv}}\right)(t - t_2) - C_2, & \text{for } t_{11} \le t < t_{12} \\ \left(1 - \frac{i_{A1}}{\bar{I}_{inv}}\right)(t - t_1) - C_1, & \text{for } t_{12} \le t < t_{13} \\ t - t_{14}, & \text{for } t_{13} \le t < t_{14} \end{cases} \tag{5.3.2}$$

The C_i in (5.3.2) are the constants resulting from the integration operation in

(5.3.1). C_i is obtained by evaluating $v_{(i-1)}$ at $T_{(i-1)}$. This yields:

$$\begin{aligned}
C_1 =& T_0 \\
C_2 =& C_1 + \Big(1 - \frac{i_{A1}}{\bar{I}_{inv}}\Big)T_1 \\
C_3 =& C_2 + \Big(1 - \frac{i_{A1} - i_{C2}}{\bar{I}_{inv}}\Big)T_2 \\
C_4 =& C_3 + \Big(1 - \frac{i_{A1} - i_{B2}}{\bar{I}_{inv}}\Big)T_3 \\
C_5 =& C_4 + \Big(1 + \frac{i_{B1} - i_{B2}}{\bar{I}_{inv}}\Big)T_4
\end{aligned} \tag{5.3.3}$$

The $\tilde{v}_c$ for symmetric six-phase VSI in Mode 3 is depicted in Figure 5.4. One can note that $\tilde{v}_c$ is symmetric around t_7. Hence, the mean square value of $\tilde{v}_c$ can be calculated as:

$$\begin{aligned}
\tilde{V}_c^2 &= \frac{1}{T_s}\int_{t_0}^{t_0+T_s} \tilde{v}_c^2 \, dt = \frac{2\bar{I}_{inv}^2}{C^2 T_s}\Bigg[\sum_{i=0}^{6}\int_0^{T_i} v_i^2 \, dt\Bigg] \\
&= \frac{2\bar{I}_{inv}^2}{C^2 T_s}\Bigg[\int_0^{T_0} t^2 \, dt + \int_0^{T_1}\Bigg(\Big((1 - \frac{i_{A1}}{\bar{I}_{inv}}\Big)t + C_1\Bigg)^2 dt \\
&+ \int_0^{T_2}\Bigg(\Big((1 - \frac{i_{A1} + i_{C2}}{\bar{I}_{inv}}\Big)t + C_2\Bigg)^2 dt + \int_0^{T_3}\Bigg(\Big((1 - \frac{i_{A1} - i_{B2}}{\bar{I}_{inv}}\Big)t + C_3\Bigg)^2 dt \\
&+ \int_0^{T_4}\Bigg(\Big((1 + \frac{i_{B1} + i_{B2}}{\bar{I}_{inv}}\Big)t + C_4\Bigg)^2 dt \\
&+ \int_0^{T_5}\Bigg(\Big((1 + \frac{i_{B2}}{\bar{I}_{inv}}\Big)t + C_5\Bigg)^2 dt + \int_0^{T_6} t^2 \, dt\Bigg]
\end{aligned} \tag{5.3.4}$$

The RMS inverter DC-bus voltage ripple, $\tilde{V}_c$ over Mode 3 is computed as:

$$\tilde{V}_c = \sqrt{\frac{6}{\pi}\int_{\pi/3}^{\pi/2} \tilde{V}_c^2 \, d\theta} \tag{5.3.5}$$

Substituting (5.1.2) and (5.2.2) in (5.3.4) and performing the integration in (5.3.4), results in:

$$\tilde{V}_c = K_v M \sqrt{\frac{1}{60}M + \left(6 - \frac{65}{2\pi}M + \frac{9}{2}M^2 + 18v_0^2\right)\cos^2\phi} \tag{5.3.6}$$

where $K_v = I_L/8Cf_s$. For symmetric balanced loads, the average value over the other eleven 60° intervals (Figure 5.3a) is the same.

5.3.2 Asymmetric Configuration

Similar to the methodology undertaken in Section 5.2.2, Modes 3–5 are analyzed to derive $\tilde{V}_c$ for six-phase VSI with asymmetric loads. Again, derivations for $\tilde{V}_c$ in Mode 3 are similar to those carried out in the previous subsection and hence are not repeated. For Modes 4 and 5, $\tilde{v}_c$ is similar to that of Mode 3 defined in (5.3.1), but using i_{inv4} and i_{inv5} instead of i_{inv3} in (5.2.1), respectively. Therefore, intermediate steps pertaining to $\tilde{v}_c$ and $\tilde{V}_c^2$ are not shown for brevity. The RMS inverter DC-bus voltage ripple over one fundamental cycle is the weighted sum of $\tilde{V}_c^2$ in Modes 3–5, given as:

$$\tilde{V}_c = \left\{\frac{3}{\pi}\int_{\pi/4}^{\pi/3}\tilde{V}_{c3}^2\,d\theta + \frac{3}{\pi}\int_{\pi/3}^{\pi/2}\tilde{V}_{c4}^2\,d\theta + \frac{3}{\pi}\int_{\pi/2}^{7\pi/12}\tilde{V}_{c5}^2\,d\theta\right\}^{1/2} \tag{5.3.7}$$

Performing the integration in (5.3.7) yields:

$$\tilde{V}_c = K_v M\left\{3 - \frac{24}{5}M + \frac{9}{4}M^2 + 9v_0^2 - \frac{16}{5\pi}Mv_0\sin 2\phi + \left(3 - \frac{21}{4}M + \frac{9}{4}M^2\right)\cos 2\phi\right\}^{1/2} \tag{5.3.8}$$

Note that some numerical approximations were conducted in (5.3.6) and (5.3.8) in order to yield simple and closed-form formula. While this study is limited to SPWM

(i.e. $v_0 = 0$), previous studies [212–215] suggested no improvement in input voltage ripples for MPIs when using SVM. Nonetheless, the expressions are given in terms of v_0 for future work.

5.4 DC Capacitor Design

The DC-bus capacitor is designed to meet the requirements of the inverter system. Among them, it must satisfy two criteria related to DC stresses: 1) a continuous current rating higher than the maximum $\tilde{I}_c$, and 2) withstand an allowable voltage ripple, typically below 10%. As such, the points at which the current and voltage ripples are at their maximum must be defined. Using the derived expressions for $\tilde{I}_c$ and $\tilde{V}_c$ in Section 5.2 and 5.3, the maximum DC stress points in six-phase VSI are found in this section. Then, simple formulas for capacitor selection is provided, considering symmetric and asymmetric loads.

Consider the variables affecting the current and voltage ripples in (5.2.6), (5.2.10), (5.3.6), and (5.3.8). They can be classified as design-specific and operation-specific variables. The former variables are I_L, C, and f_s, whereas the latter variables are M and ϕ. The design-specific variables are irrelevant when determining the points of maximum stress and rather act as scaling factors. Thus, they can be normalized when solving for the maximum points. It follows that the normalized capacitor current and voltage ripples are $\hat{I}_c = \tilde{I}_{inv}/I_L$ and $\hat{V}_c = \tilde{V}_c/K_v$, respectively. The maximum stress points can then be treated as an optimization problem defined as:

$$\mathbf{x}^* = \arg\max_{\mathbf{x}} f(\mathbf{x}) \tag{5.4.1}$$

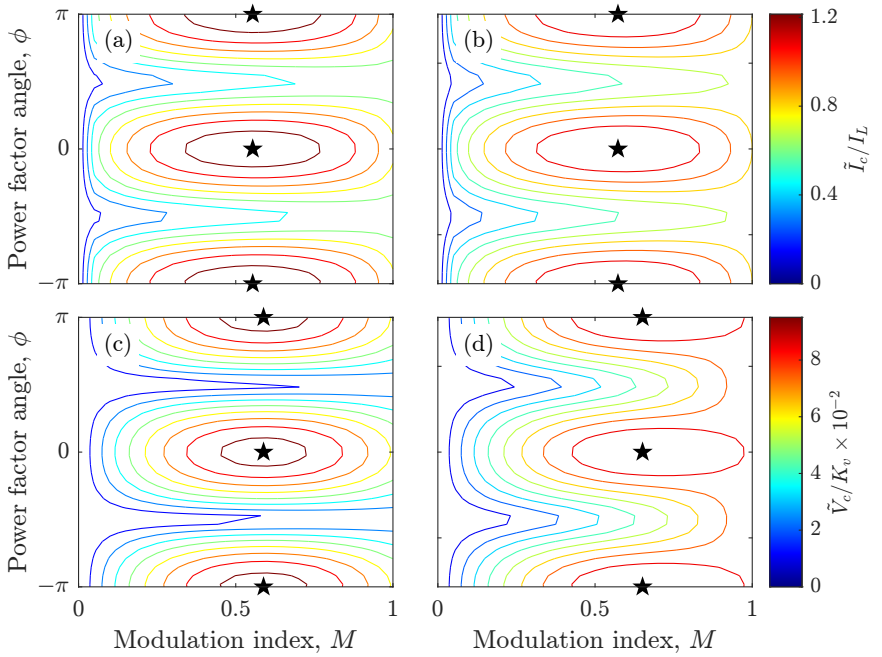


Figure 5.7: Contour map of $f(\mathbf{x})$ showing $\mathbf{x}^*$. Normalized current ripple, $\hat{I}_c = \tilde{I}_c/I_L$ for (a) symmetric and (b) asymmetric loads, and normalized voltage ripple, $\hat{V}_c = \tilde{V}_c/K_v$ for (c) symmetric and (d) asymmetric six-phase loads.

subject to

$$\begin{aligned} 0 \leq \mathrm{x}_1 \leq 1 \\ 0 \leq \mathrm{x}_2 \leq 2\pi \end{aligned} \tag{5.4.2}$$

where $f(\mathbf{x})$ is $\hat{I}_c$ and $\hat{V}_c$, and $\mathbf{x} = [\mathrm{x}_1 \quad \mathrm{x}_2]^T = [M \quad \phi]^T$. The two-dimensional nonlinear $f(\mathbf{x})$ can be solved using any of the classical optimization methods [223]. Figure 5.7 depicts the maximum stress points, $\mathbf{x}^*$ in the $f(\mathbf{x})$ space. In terms of ϕ, the maximum current and voltage stress occurs at the same point: $\phi^* = k\pi, k \in \{0, 1, 2...\}$ (i.e. unity PF), irrespective of load configuration. On the other hand, the maximum stress points occur at different M: the maximum current stress occurs at $M^* = 0.55$ and 0.57 and the maximum voltage stress occurs at $M^* = 0.59$ and 0.65 for symmetric and asymmetric loads, respectively.

Evaluating $\tilde{I}_{inv}$ in (5.2.6) and (5.2.10) at $\mathbf{x}^*$ yields:

$$I_{CAP} \geq \begin{cases} 6/5 \cdot I_L, & \text{for symmetric loads} \\ 5/4 \cdot I_L, & \text{for asymmetric loads} \end{cases} \tag{5.4.3}$$

where I_{CAP} is the rated continuous current of the DC-capacitor. Similarly, the required capacitance, C to guarantee an acceptable DC voltage ripple can be found by evaluating $\tilde{V}_c$ in (5.3.6) and (5.3.8) at $\mathbf{x}^*$. This yields:

$$C \geq \begin{cases} \dfrac{3\sqrt{3}I_L}{16 f_s \Delta V_{pp}}, & \text{for symmetric loads} \\ \dfrac{4\sqrt{3}I_L}{21 f_s \Delta V_{pp}}, & \text{for asymmetric loads} \end{cases} \tag{5.4.4}$$

where ΔV_{pp} is the allowable peak-to-peak voltage ripple. Note that I_{CAP} and C for asymmetric six-phase loads is higher than its symmetric counterpart by approximately 5%. Hence, if the six-phase inverter is designed to be suitable for both load configurations, the formulas for asymmetric loads should be employed for the DC-capacitor sizing.

The accuracy of the derived formulas for the DC-capacitor current and voltage stresses is examined next.

5.5 Results and Discussions

The developed analytical formulas for the DC-bus capacitor RMS voltage and current ripples are verified by numerical simulations and experimental testing. Figure 5.8 depicts the experimental setup a six-phase VSI connected to a passive RL

Table 5.2: Experimental setup and simulation parameters

Parameter	**Symbol**	**Value**	**Unit**
DC-bus voltage	V_{dc}	100	V
DC-bus capacitor	C	80	μF
DC-line resistance	R_{dc}	30	mΩ
DC-line inductance	L_{dc}	10	μH
Fundamental frequency	f_1	50	Hz
Switching frequency	f_s	10	kHz
Switching dead time	t_d	2	μs

load. The passive load is chosen for its flexibility to be configured as symmetric and asymmetric load by simply adjusting the angle δ of the virtual reference voltage in the controller. Nevertheless, the following experimentation and analysis are equally applicable to motor loads, if the load currents are balanced and almost sinusoidal. Table 5.2 lists the experimental setup parameters. The VSI is made up of six Infineon half-bridge 1200V/600A IGBT FF600R12IE4 modules connected via DC busbars made of copper. The inverter is controlled via a 32-bit, dual-core, floating-point Texas Instruments TMS320F28379D digital signal processor (DSP). The employed DC-bus capacitor bank is two-paralleled 40 μF film capacitors. Note that the effect of equivalent series resistance (ESR) and equivalent series inductance (ESL) of the film capacitors on the voltage ripple estimation is negligible [215]. The DC voltage is supplied from a Keysight N8932A DC source. The employed RL load is made adjustable to facilitate testing at different PF points where industrial drives are typically operated (0.6–0.9), as tabulated in Table 5.3. The DC-line impedance, Z_{dc} is the impedance of the DC cable between the power source and the inverter, whose resistance is R_{dc} = 30 $m\Omega$ and its inductance is estimated based on the cable's length and diameter to be L_{dc} = 10 μH.

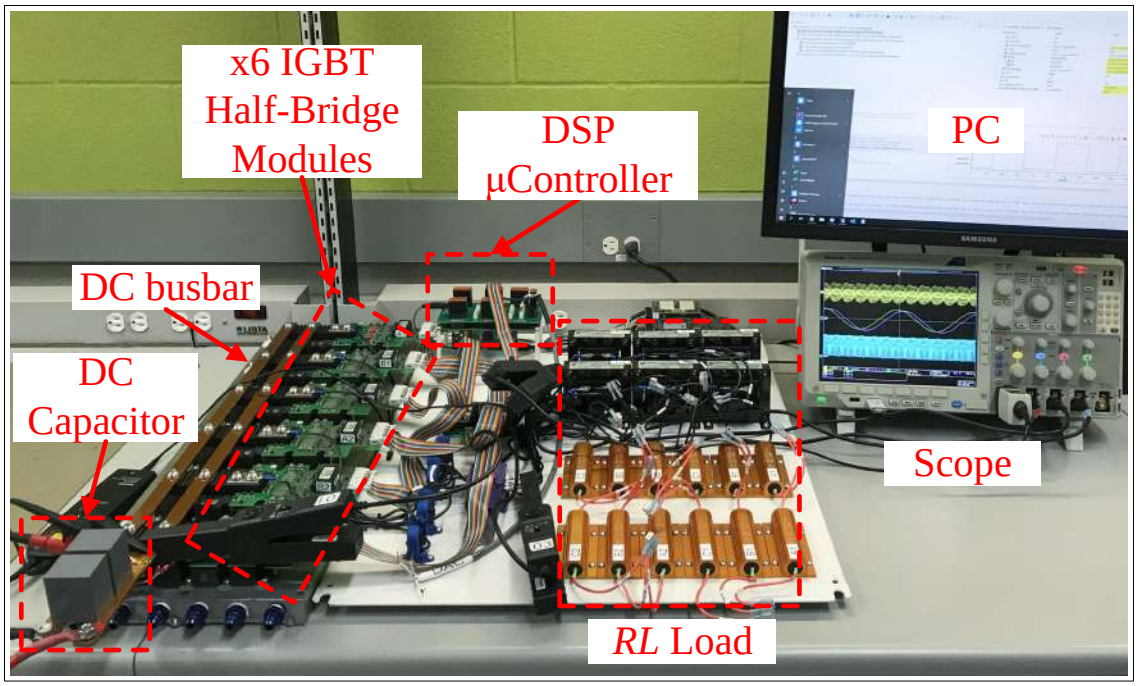


Figure 5.8: Experimental setup of a six-phase VSI with RL load.

Table 5.3: Per-phase RL load parameters

PF (f_1 = 50 Hz)	**0.6**	**0.8**	**0.9**
R (Ω)	1.1	2.2	4.4
L (mH)	5.0	5.0	5.0

Experimental measurements are acquired using MDO4024C Tektronix oscilloscope with THDP0200 differential voltage probe and SL261 current probes. A low-pass filter (LPF) with a cut-off frequency of 100 kHz is applied to the measured signals (both experimentally and in simulation) to eliminate high frequency spikes due to IGBT switching. The remainder of the section discusses the experiments and simulations by 1) comparing symmetric to asymmetric six-phase VSI, in terms of voltage and current stress on the DC-capacitor, 2) validating the accuracy of the derived formulas, 3) comparing six-phase VSI to conventional three-phase counterpart, and 4) practical

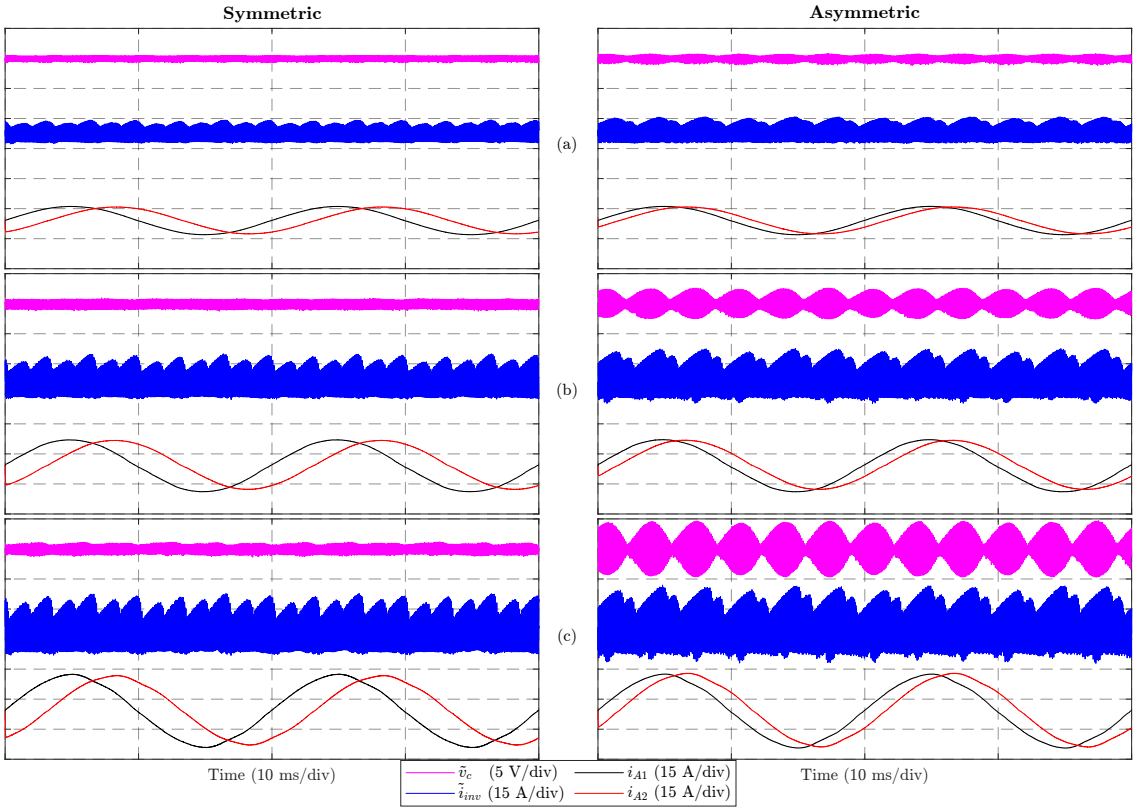


Figure 5.9: Experimental results for DC-bus capacitor voltage and current ripples in six-phase VSI for symmetric (left column) and asymmetric (right column) loads (f_1 = 50 Hz, f_s = 10 kHz, V_{dc} = 100 V, PF = 0.6). (a) M = 0.4. (b) M = 0.7. (c) M = 0.9.

considerations on the employment of the derived formulas.

5.5.1 Symmetric vs. Asymmetric Six-Phase VSI

Figure 5.9 depicts the experimental measurements of the DC-capacitor voltage and current stresses at PF = 0.6 for symmetric and asymmetric loads for M = 0.4, 0.7, and 0.9. It can be observed that the DC-capacitor experiences a higher voltage and current stresses when the load is asymmetric, especially at low PFs. Therefore,

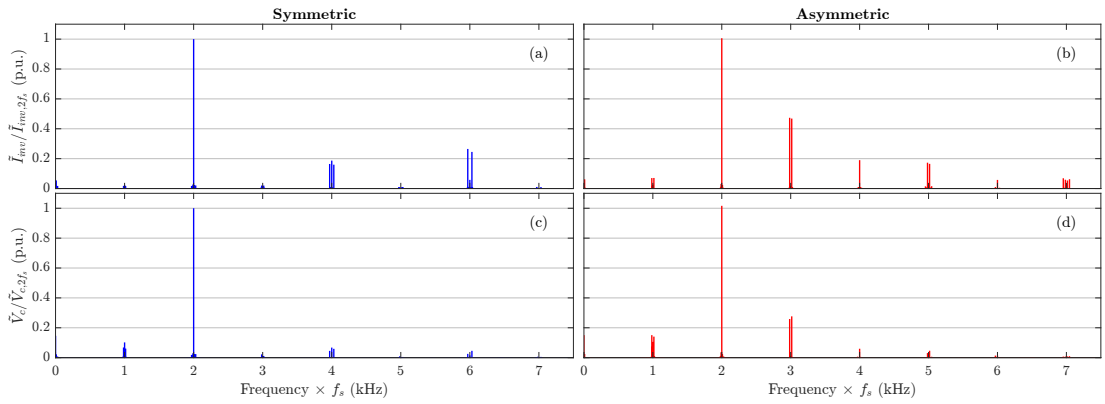


Figure 5.10: Experimental harmonic spectra of DC-capacitor voltage and current ripples in six-phase VSI with symmetric (left column) and asymmetric (right column) loads (f_1 = 50 Hz, f_s = 10 kHz, V_{dc} = 100 V, PF = 0.6, M = 0.7). (a)–(b) $\tilde{I}_{inv,n}$. (c)–(d) $\tilde{V}_{c,n}$.

the symmetric distribution leads to reduced voltage and current stress on the DC-capacitor.

To further analyze the voltage and current stresses on the DC-capacitor for the different load configurations, the experimentally-obtained harmonic spectra of $\tilde{i}_{inv}$ and $\tilde{v}_c$ in Figure 5.9b are shown in Figure 5.10. The dominant harmonic of $\tilde{i}_{inv}$ and $\tilde{v}_c$ is at $2f_s$. This dominant harmonic is of the same magnitude for both load configurations, symmetric and asymmetric, when the operating conditions are similar. However, the harmonic distribution is different, which is why $\tilde{I}_{inv}$ and $\tilde{V}_c$ differ from one load configuration to the other. Sideband harmonics, $mf_s \pm nf_1$ around mf_s where m is an even multiple exist only in the asymmetric load for $\tilde{I}_{inv}$ and $\tilde{V}_c$ (Figure 5.10b and d). Put otherwise, even sideband harmonics are cancelled when supplying a symmetric six-phase load. This confirms the harmonic analysis of the DC current ripple discussed in Section 5.2.3. Furthermore, the harmonic spectra in Figs. 5.6b and 5.6c match the experimentally measured spectra in Figs. 5.10a and 5.10b, respectively.

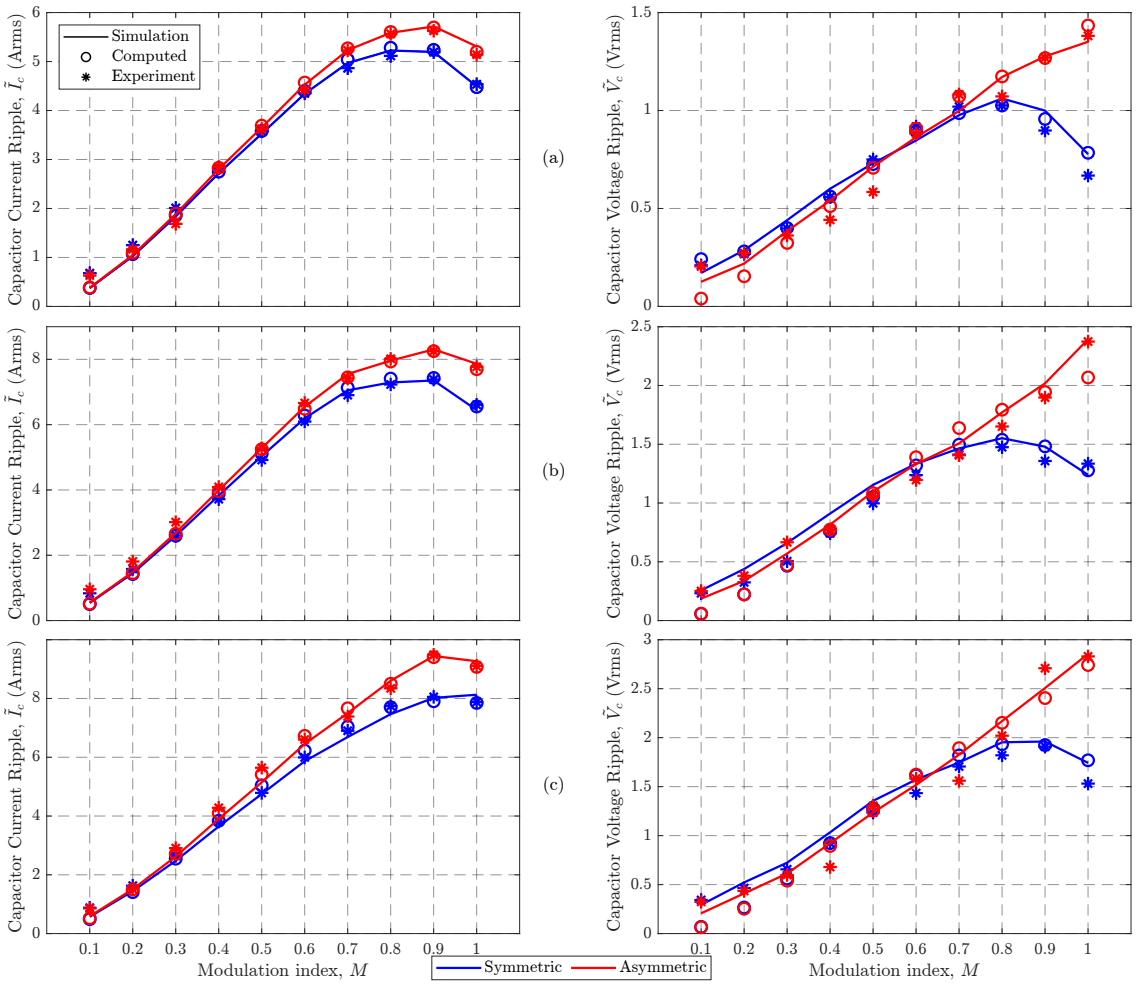


Figure 5.11: Experimental verification of $\tilde{I}_{inv}$ formulas in (5.2.6) and (5.2.10) (left column) and $\tilde{V}_c$ formulas in (5.3.6) and (5.3.8) (right column) for symmetric and asymmetric six-phase loads, respectively. (a) PF = 0.9. (b) PF = 0.8 (c) PF = 0.6.

5.5.2 Validity of the Derived formulas

For accuracy verification of the derived formulas of $\tilde{i}_{inv}$ and $\tilde{v}_c$ for symmetric and asymmetric six-phase VSI, a modulation index sweep is conducted at PF =0.6, 0.8, and 0.9. The measured RMS values of $\tilde{I}_{inv}$ and $\tilde{V}_c$, both experimentally and in simulation, are benchmarked against the computed values using the derived formulas. The simulations are conducted in MATLAB/Simulink using the same parameters in Table

Table 5.4: Root Mean Square Error (RMSE) between calculated and experimentally-measured DC-capacitor RMS voltage and current ripples

Configuration	Symbol	Eq.	PF	RMSE	Unit
Symmetric	$\tilde{I}_{inv}$	(5.2.6)	0.9	0.15	A
			0.8	0.18	
			0.6	0.29	
	$\tilde{v}_c$	(5.3.6)	0.9	0.05	V
			0.8	0.09	
			0.6	0.15	
Asymmetric	$\tilde{I}_{inv}$	(5.2.10)	0.9	0.12	A
			0.8	0.23	
			0.6	0.19	
	$\tilde{v}_c$	(5.3.8)	0.9	0.09	V
			0.8	0.18	
			0.6	0.20	

5.2, along with the IGBT module characteristics and DC-capacitor parasitics (series-connected RLC model) found in the datasheets. Figure 5.11 show the measured and computed values of $\tilde{I}_{inv}$ and $\tilde{V}_c$ at the different PF points. A very good agreement between the measured, simulated, and computed $\tilde{I}_{inv}$ and $\tilde{V}_c$ is evident in Figure 5.11, for both load configurations. Additionally, Figure 5.11 reiterate the findings in Figs. 5.9 and 5.10 that the DC-capacitor experiences a higher voltage and current stress when supplying an asymmetric load. The RMSE between the calculated $\tilde{I}_{inv}$ and $\tilde{V}_c$ using the derived formulas and the experimentally measured counterparts over the range of $M \in [0.1, 1]$ of Figure 5.11 is given in Table 5.4. A very high accuracy of the derived formulas for $\tilde{I}_{inv}$ and $\tilde{V}_c$ is demonstrated with a RMSE below using the derived formulas (5.2.6) and (5.2.10), for symmetric and asymmetric loads, respectively, with a RMSE below 0.25 A and 0.20 V, respectively.

5.5.3 Six-Phase vs. Three-Phase VSI

To summarize the harmonic content of I_c for the three inverters, the harmonic content factor (HCF) is computed for each harmonic group. The HCF in this thesis is defined as the ratio of the RMS square of the harmonics in a given group to the RMS square of I_c, as:

$$\text{HCF} = \frac{\sum_{m,n} I^2_{c,mf_s \pm nf_1}}{I_c^2} \tag{5.5.1}$$

where the selection of m and n in the numerator is based on the aforementioned harmonic group definition. Table 5.5 summarizes the HCF of each harmonic group for the three inverters, computed to the 600th harmonic. Table 5.5 confirms the fact that Group 2 harmonics are more dominant than Group 3 in three-phase VSI, with a ratio of five to two. Thus, the elimination of Group 2 in the symmetric six-phase VSI yields the smallest I_c.

The same harmonic content analysis applies to the DC-capacitor voltage ripple, as demonstrated in Figs. 5.10c and 5.10d, since $\tilde{V}_{c,n} = \tilde{I}_{c,n}/Z_{c,n}$, where Z_c is the impedance of the capacitor and the n subscript denotes frequency order. However, the ratio of voltage harmonic to current harmonic ($V_{c,n}/I_{c,n}$) is not the same for all nth harmonic in Figs. 5.10c and 5.10d as the reactance of the capacitor, $X_{c,n} = 1/(\omega_n C)$ decreases for higher frequencies.

To quantify the DC-capacitor requirement reduction in six-phase VSI, when compared to its three-phase counterpart, the DC-capacitor voltage and current ripples are evaluated over the entire operation envelop. Figure 5.12 depicts the normalized $\tilde{I}_c$ (i.e. $\hat{I}_c = \tilde{I}_c/I_L$) and $\tilde{V}_c$ (i.e. $\hat{V}_c = \tilde{V}_c/K_v$) for three- and six-phase VSIs over M and $PF \in [0, 1]$. The normalized $\tilde{I}_c$ and $\tilde{V}_c$ maps are in line with the previous findings:

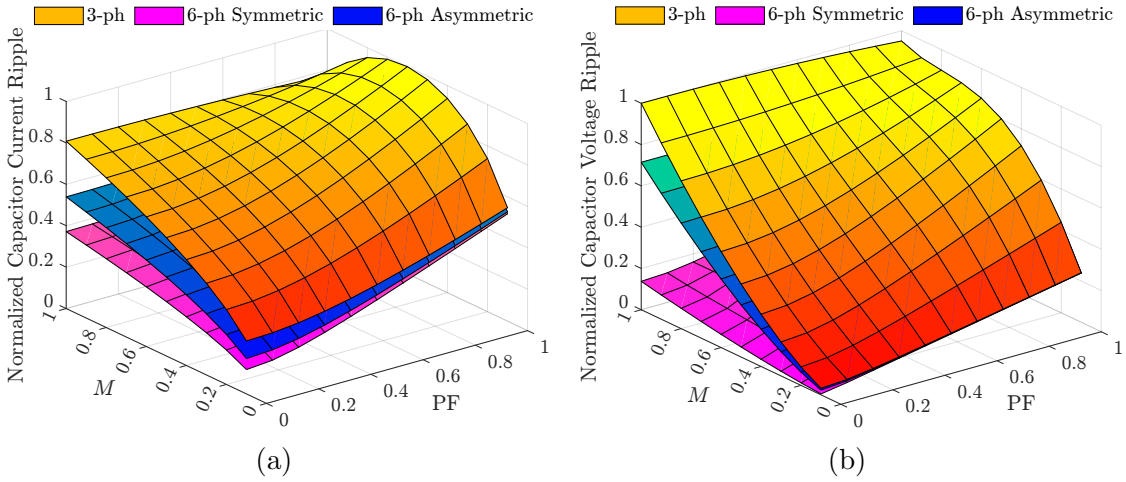


Figure 5.12: Normalized voltage and current stresses on the DC-bus capacitor in three-phase and six-phase VSIs. (a) Current stress. (b) Voltage stress.

six-phase VSI achieves lower DC-capacitor voltage and current ripples, and they are the lowest in the case of symmetric loads/machines. Since the DC-capacitor is always designed to handle the maximum voltage and current stresses, the normalized maximum voltage and current stresses in Figure 5.12 are shown in Figure 5.13. Six-phase VSI with symmetric loads/machines yields DC-capacitor voltage and current ripple reduction by 24% and 10%, respectively compared to 20% and 7% for the asymmetric case, respectively, when benchmarked against the three-phase VSI. It is to be highlighted that current ripple handling by the DC-capacitor are usually the bottleneck

Table 5.5: Harmonic content factor (HCF) of DC-capacitor current harmonic groups in three- and six-phase VSIs

Harmonic Group	**3-phase**	**6-phase**	
		Symm.	**Asymm.**
Group 1	36%	82%	70%
Group 2	46%	0%	29%
Group 3	18%	16%	0%

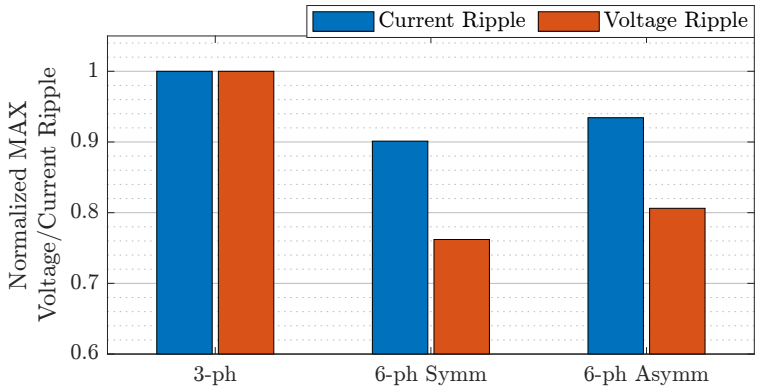


Figure 5.13: Normalized maximum DC-capacitor voltage and current stress in three-phase and six-phase VSIs with symmetric and asymmetric loads.

in capacitor design for inverters operating beyond 10 kHz, and hence dominate the selection criteria.

5.5.4 Practical Considerations

The derived formulas for current and voltage ripples for the six-phase VSI were obtained under two main assumptions: very high capacitance of the DC-bus capacitor and very high switching frequency. The validity of such assumptions are assessed in this subsection.

Input Filter

Ideally, where the DC-side impedance is zero, the current ripple is supplied entirely by the source, and the capacitor voltage ripple is zero. However, some ripple exists in i_{dc} due to the stray inductance of the cables and the DC source. This can also occur when C is not large enough to sink all the ripples, as assumed earlier. In this case, the effect of L_{dc} becomes significant and must be evaluated. Figure 5.14a depicts the equivalent DC circuit of the inverter.

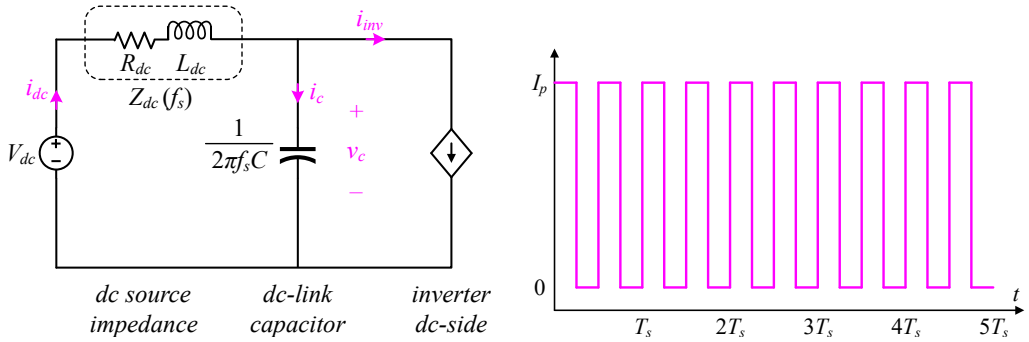


Figure 5.14: Equivalent circuit of the DC-side of the inverter at the switching frequency, f_s. (a) Circuit diagram. (b) i_{inv} waveform.

Assuming a symmetrical pulsating i_{inv} with 50% duty cycle, as shown in Figure 5.14b, i_{inv} can be written as a summation of the DC (average) component and the high-frequency components as:

$$i_{inv} = i_0 - \frac{4}{\pi} I_p \sum_{n=1,3,5,\ldots}^{\infty} \frac{1}{n} \sin(2n\omega_s t) \tag{5.5.2}$$

where $i_0 = I_p/2$ is the average component passing through L_{dc}. By superposition and after phasor calculations, i_{dc} can be expressed as:

$$i_{dc} = \frac{I_p}{2} - \frac{4}{\pi} I_p \sum_{n=1,3,5,\ldots}^{\infty} \frac{1}{n} \sin(2n\omega_s t) \cdot \left| \frac{1/\omega_s C}{\omega_s L_{dc} - 1/\omega_s C} \right| \tag{5.5.3}$$

Using (5.5.3), an inductance sweep code is run in MATLAB to investigate the change in the current ripple with different L_{dc} values. The resulting i_{dc} waveform at $f_s = 10$ kHz with $I_p = 10$ A and $C = 80$ μF is shown in Figure 5.15. The values of L_{dc} at which i_{dc} spikes are the values where L_{dc} and C resonate with the switching frequency and its odd multiples. However, practically, the series resistances of the DC cables

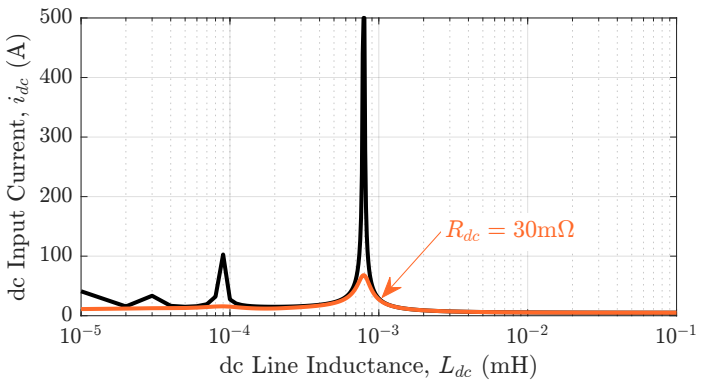


Figure 5.15: DC input current, i_{dc} vs. DC line inductance, L_{dc}.

and the ESR of the DC-capacitor limit the spike value at the resonant frequency, as demonstrated by the orange trace in Figure 5.15 when considering R_{dc} = 30 mΩ. The maximum current ripple is suppressed at all operating conditions, especially at resonant points. In this study, L_{dc} is assumed to be $\geq 2/(\omega_s^2 C)$. In this region, the DC-side current only supplies the DC current and almost all current ripple passes through the capacitor, i.e. $\tilde{i}_{dc} = 0$.

Modulation Frequency

The derived formulas for the DC current and voltage ripples assume mostly sinusoidal output currents. However, this assumption is only valid under certain circumstances for m_f. In order to determine the validity of the analysis under different values of m_f and M, extensive simulations were performed over a range of values for the two foregoing variables. The range for M is 0.1–0.9 with steps of 0.1. The range for m_f is 6–30, with steps of 1. The error in the values of calculated and measured current and voltage are depicted in the Figure 5.16 for both symmetrical and asymmetrical loads. The pink plane is the threshold for a 10% calculation error. The error decreases with the increase in the values of m_f and M.

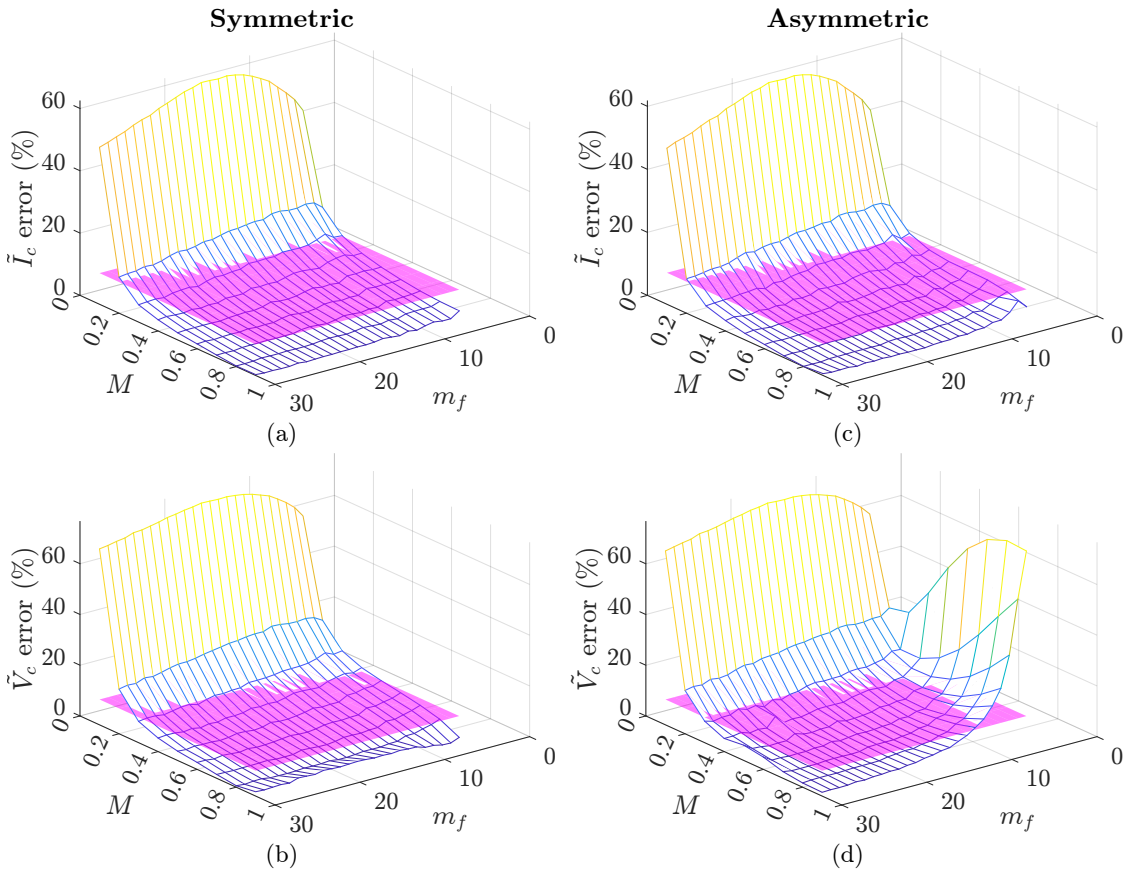


Figure 5.16: Calculation error of derived formulas for current ripple, $\tilde{I}_c$ and voltage ripples, $\tilde{V}_c$ in six-phase symmetric (left column) and asymmetric (right column) load configuration as a function of modulation frequency, m_f and modulation index, M.

In summary, the following conditions must be met to yield a calculation error below 10% using the derived formulas DC current and voltage ripple estimation in six-phase inverters:

1. The switching frequency is higher than or equal to ten times the output fundamental frequency, i.e. $f_s \geq 12 f_1$ or $m_f \geq 12$.

2. The switching frequency is higher than or equal to the $\sqrt{2}$ of the resonant frequency of the DC-side filter, $f_r = 1/(2\pi\sqrt{L_{dc}C})$, i.e. $f_s \geq \sqrt{2} f_r$. This can

alternatively be expressed as $L_{dc} \geq 2/(\omega_s^2 C)$.

3. The output AC currents are balanced, and their THD is ≤15%.

4. The modulation index, M is ≥ 0.3.

The foregoing conditions are normally fulfilled in motor drive applications employing high frequency switching devices, and therefore the derived formulas are applicable over a wide range of operating conditions.

5.6 Summary

Detailed analyses of DC-bus voltage and current ripples in six-phase symmetric and asymmetric VSIs were presented in this chapter. The analyses rendered, for the first time, analytical formulas to evaluate the voltage and current stresses on the DC-capacitor in six-phase VSI supplying symmetric and asymmetric loads. The accuracy of the derived formulas was verified by simulation and experimental testing. The derived formulas can evaluate the DC-capacitor voltage and current ripple over a wide range of operating conditions. Subsequently, simple capacitor sizing rules for symmetric and asymmetric six-phase VSIs were proposed for SPWM. Furthermore, the harmonic spectra of the DC-capacitor current in six-phase VSI was analyzed and benchmarked against its conventional three-phase counterpart. The spatial distribution of the additional three-phases in six-phase VSI leads to cancellation of some dominant carrier-sideband harmonics that renders reduced current stress on the DC-capacitor. This in turn yields a reduced capacitor size in six-phase VSI when compared to its three-phase counterpart, for the same VA rating. The current stress is minimized when the supplied load/machine is of symmetric spatial distribution

with 10% reduction when compared to three-phase VSI, or 3% lower than six-phase asymmetric loads.

The derived formulas are beneficial for DC-capacitor selection in six-phase VSIs based on voltage and current ripples ratings, and can be used for capacitor derating and lifetime prediction.

Chapter 6

Holistic Design and Development of a 100 kW SiC-Based Six-Phase Traction Inverter

As mentioned earlier in the previous chapter, a thorough design of a six-phase inverter is not present in the literature. A thorough design should exploit the inherent advantages of six-phase systems such as lower torque pulsation (in the case of an asymmetric motor) [36], reduction of DC-capacitor requirements as discussed in the previous chapter, and reduced cabling cost [38], and mitigate their drawbacks such as higher number of sensors and gate drivers.

As mentioned earlier in Chapter 1, Dana TM4 offers commercial MPIs for traction drives for light- to heavy-duty trucks [24]. The power density of those inverters is smaller than 10 kW/L, which is not competitive when compared to state-of-the-art three-phase traction inverters [16]. Recently, Koenigsegg has released David, a 700 kW SiC-based six-phase inverter for its limited production PHEV, the Gamera

[39]. The technical and commercial details of the David are not disclosed.

This chapter presents the design and development of a 100 kW SiC-based six-phase traction inverter. Similar designs of SiC-based three-phase traction inverters have been investigated in [117, 127, 224–230]. All of the three-phase designs proposed in [117,127,224–230] use power module packages (either half-bridge or six-pack) for the switching devices. This stems from the high per-phase current requirement versus the relatively low current rating of discrete power devices. Alternatively, discrete power devices can be connected in parallel. A commercial example is the 2018 Tesla Model 3 inverter, which utilizes four parallel discrete SiC MOSFETs per switch [44]. Such a requirement is alleviated in multiphase systems owing to the reduced per-phase current requirement. For instance, an eleven-phase 50 kW traction system with a single SiC MOSFET per switch was proposed in [49]. In the proposed design, a single discrete SiC MOSFET is sufficient for the rated per-phase current, eliminating the need for device paralleling altogether. In [224], a subsystem optimization approach is investigated for a 250 kW SiC-based three-phase inverter, with a focus on the bus bar design. The bus bar is designed to accommodate three half-bridge modules stacked in a planar manner. Similar bus bar designs were discussed in [127, 225]. However, stacking six half-bridge modules for a six-phase inverter significantly deteriorates the power density. This challenge was addressed in [231] with a two-sided bus bar that integrates six half-bridge power modules, three on each side. On the other hand, the resultant design used two cold plates, one on each side, which further complicates the cooling system design. An enhanced integration of six-pack SIC module with bus bar was proposed in [230], achieving a remarkable power density of 43 kW/L. However, the study did not showcase system-level integration involving mechanical housing,

control card, and sensors. Thanks to the flexibility that discrete power devices offer, the proposed design utilizes a printed circuit board (PCB) that integrates the power devices and the DC-capacitor bank. Therefore, a simple, yet power dense design is achieved. PCB-based bus bar designs were proposed in [226] and [228] with half-bridge SiC modules. Given the large footprint of such modules, the PCB size is subsequently made large to integrate the connection points of the modules. This called for a thorough analysis and design precautions to ensure that the PCB design is adequate in terms of stray inductance, current density, and voltage overshoot. A combination of bus bar and PCB-based structures was proposed in [229] to connect the power module to the DC-capacitor bank made of ceramic capacitors on three stacked PCBs. While, the proposed DC-capacitor bank is claimed to improve the power density compared to film capacitors, the addition of PCBs and bus bars increases the cost of the inverter. Furthermore, on-board current sensors were proposed in [226] using a shunt resistor with an isolated amplifier to eliminate the need for bulky hall-effect current sensors. However, shunt resistors incur losses.

In the proposed inverter, the PCB-based design integrates discrete SiC MOSFETs and, hence, offers flexibility and streamlines the design process. Besides, the DC-capacitor is sized specifically for six-phase drives, exploiting the advantages of reduced DC voltage and current ripples in six-phase systems [37]. A coreless monolithic hall-effect current sensor integrated circuit (IC) is utilized to achieve a compact design that mitigates the higher count of current sensors in six-phase systems. The inverter housing encloses the electronics and integrates the coolant channel in a single body, thus delivering a compact mechanical design. As such, the holistic electrical-thermal-mechanical methodology proposed in this paper contributes to the existing literature

by providing the first detailed design of a six-phase inverter. The proposed design aims to facilitate the development of MPD for automotive applications.

The remainder of this chapter is organized as follows. Section 6.1 discusses the characteristics of six-phase drives for traction applications. Sections 6.2–6.6 presents the holistic design methodology of the electrical design for the SiC-based six-phase traction inverter, whereas Sections 6.7 and 6.8 present the thermal and mechanical designs, respectively. Section 6.9 benchmarks the main specifications of the proposed design to commercial six-phase and three-phase counterparts. Finally, Section 6.10 outlines the concluding remarks.

6.1 Fundamental of Six-Phase Electric Drives

To effectively design a six-phase inverter, a basic knowledge on the machine's characteristics must be established first.

A six-phase motor can be configured based on the spatial displacement angle, δ between the two sets of three-phases [232]: split ($\delta = 0$), symmetric ($\delta = \pi/3$), or asymmetric ($\delta = \pi/6$). The neutral of both three-phase sets can be common or isolated. In the latter case, the six-phase motor is commonly referred to as dual three-phase motor [30, 36]. Table 6.1 summarizes the performance characteristics of such motor configurations. For EV applications, symmetric and asymmetric six-phase motors have been investigated intensively [220]. The asymmetric configuration has been the most popular among different configurations owing to its reduced torque pulsation by the elimination of the sixth-harmonic [36]. Additionally, fault-tolerance is at its best when considering asymmetric six-phase motors with isolated neutrals [219]. On the other hand, symmetric motors offer a higher efficiency and lower DC-link

Table 6.1: Six-phase motors comparison based on winding configuration

Property	**Winding configuration**		
	Split	**Symmetric**	**Asymmetric**
Spatial displacement	0	$\pi/3$	$\pi/6$
DC ripples	Worst	Best	Medium
Fault-tolerance	Worst	Best	Best
Torque pulsation	Medium	Medium	Best
Efficiency	Best	Medium	Worst

Based on [36, 37, 219, 220, 232, 233]

voltage and current ripples when compared to the asymmetric motor. Applications of split six-phase motors is limited due to poor fault tolerance capability [219]. Moreover, there is no reduction in the DC-link voltage and current ripples that could lead to reduced DC-capacitor size, as is the case in the other two configurations [37]. To summarize, the six-phase motor configuration impacts the design criteria for the traction inverter. Such criteria are usually distinguishable from the conventional three-phase inverter.

As shown in Figure 3.8a, more than half of the total volume of a three-phase traction inverter is consumed by the DC-link capacitor and the thermal management system. As shown in Figure 3.8b, the most significant cost component is the power semiconductors. As mentioned earlier in the previous section, multiple discrete devices, connected in parallel per switch, are usually employed in three-phase traction inverters to withstand the rated current. While a six-phase inverter has double the number of switches when compared to a three-phase inverter, the per-phase current is halved. Therefore, the total number of devices is equal to that of a three-phase, distributed over six switching legs [234]. For instance, a three-phase inverter with a per-phase rated current of 200 A requires two discrete C3M0016120K (1200 V/115

A) MOSFETs in parallel for each of the six switches; a total of twelve devices. For the same VA rating, the per-phase rated current of the six-phase inverter is 100 A. In this case a single device per each of the twelve switches is sufficient. Therefore, there is no increase in the discrete SiC devices cost. In contrast, six-phase inverters offer up to 10% reduction in the ripple current rating of the DC-capacitor (in the case of a symmetric motor), which, for a traction inverter, is the dominant factor in determining its volume [235]. With respect to Figure 3.8, a 10% reduction in the DC-link capacitor leads to 3% reduction in the total volume of the inverter. Moreover, six-phase systems use smaller and lighter AC outputput cables, which can provide up to 21% lower cost as compared to its three-phase counterpart [234]. On the other hand, six-phase inverters require twice the number of gate drivers and current sensors.

The proposed inverter is designed for asymmetric drives. Nevertheless, since the design for asymmetric drives poses higher constraints to the DC-link capacitor, the proposed inverter is also applicable to symmetric six-phase drives.

A holistic design methodology is undertaken to devise the design of the SiC-based six-phase inverter. Such a methodology involves the electrical, electromagnetic, thermal, and mechanical packaging of the inverter. Figure 6.1 demonstrates the holistic design flowchart of the present inverter. Based on the design specifications in Table 6.2 switching device and DC-bus capacitor selection is made. The resulting physical dimensions are then used to design the power and gate driver PCBs. Consequently, the mechanical housing encompassing all components, as well as an integrated coolant channel, is designed. Finally, the electrical loss evaluation of the design and the mechanical constraints are used to design the thermal heat sink. All of foregoing steps are repeated recursively until all design criteria are met. The remainder of this section

Table 6.2: Six-phase traction inverter design specification

Parameter	Symbol	Value	Unit
Nominal DC-bus voltage	V_{dc}	800	V
Continuous (1 hr) power	P_r	100	kW
Peak (10 s) power	P_{max}	175	kW
Rated output current	I_r	66	Arms
Maximum output current	I_{max}	115	Arms
Power factor	PF	0.9	—
Efficiency	η	≥97	%
Switching frequency	f_s	30	kHz

investigates the design methodology of these steps.

6.1.1 SiC Device Selection & Loss Evaluation

Considering SiC MOSFETs, packaging is available in discrete devices and power modules. The latter is more popular in automotive applications, thanks to its high power density and high current rating [236]. The former, on the other hand, gives

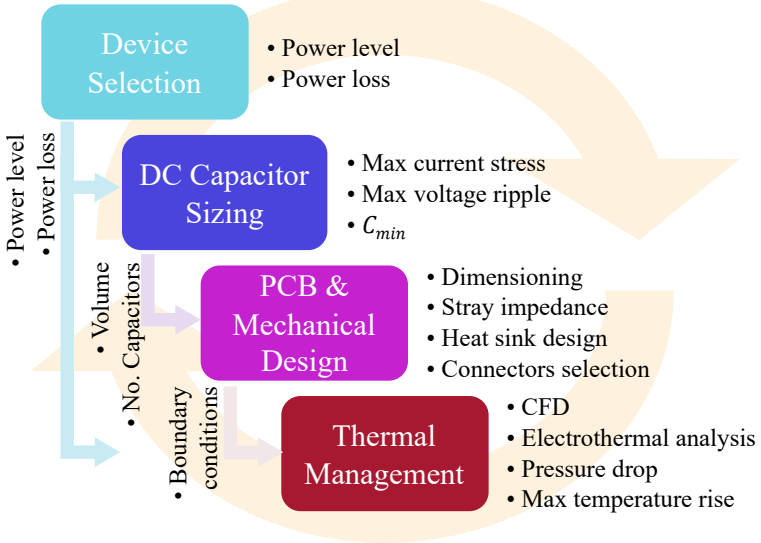


Figure 6.1: Integrated inverter design flowchart.

a higher flexibility in the design but suffers a relatively low current ratings. To mitigate this drawback, discrete device paralleling is an industry-accepted solution. For instance, Tesla's Model 3 (2018) inverter employs four SiC discrete MOSFET devices per switch, totaling 24 devices overall [44]. Device paralleling poses design challenges pertaining to static and dynamic current sharing among the paralleled devices [45,46]. This becomes more prominent as the switching frequency is increased, which is desired for component miniaturization [10].

The foregoing reasons make six-phase inverters very appealing. Since per-phase current is halved in in six-phase systems (when compared to three-phase counterparts), the per-phase current can be handled by a single discrete device, eliminating the need for device paralleling altogether. For the proposed inverter design rated at 100 kW and 800 Vdc, the per-phase current is 66 Arms at 0.9 PF. Currently, most device manufacturers offer SiC MOSFETs rated beyond 100 A. As such, discrete SiC MOSFET C3M0016120K (1200 V/115 A) by Cree is selected for the proposed design owing to its low $R_{DS(\mathrm{ON})}$ of 16 mΩ. Figure 6.2 shows the efficiency map of the SiC-based six-phase inverter when driving an eight-pole 100 kW PMSM using MATLAB/Simulink and PLECS software packages. The losses considered are switching and conduction losses from the twelve switches, which are evaluated using the thermal model of the device provided by the manufacturer. The PMSM is dynamically modeled with flux-linkage characteristics at different stator current magnitude and rotor position. The dynamic model is obtained analytically via FEA and verified experimentally in [30]. The efficiency of the inverter at rated power is 98.8% with a peak efficiency of 99.3%.

6.2 DC Capacitor Bank Sizing

There are three main types of capacitors considered for traction inverters, namely electrolytic, ceramic, and film [117]. The latter is the most popular in automotive applications owing to its high current conduction capability, which is a key factor in sizing the DC-bus capacitor [200]. It also enjoys a relatively low ESR, immunity against thermal runaway, and high reliability. On the other hand, film capacitors suffer a low capacitance density when compared to ceramic and electrolytic. However, ceramic capacitors have low capacitance per device and are costly, whereas electrolytic capacitors are highly susceptible to temperature variations with high ESR. Figure 6.3 depicts the electric impedance characteristics of the three types considering the series model of the capacitor considering its ESR and ESL, which is defined as:

$$Z_C(\omega) = \sqrt{ESR^2 + \left(\omega \cdot ESL - \frac{1}{\omega C}\right)^2} \tag{6.2.1}$$

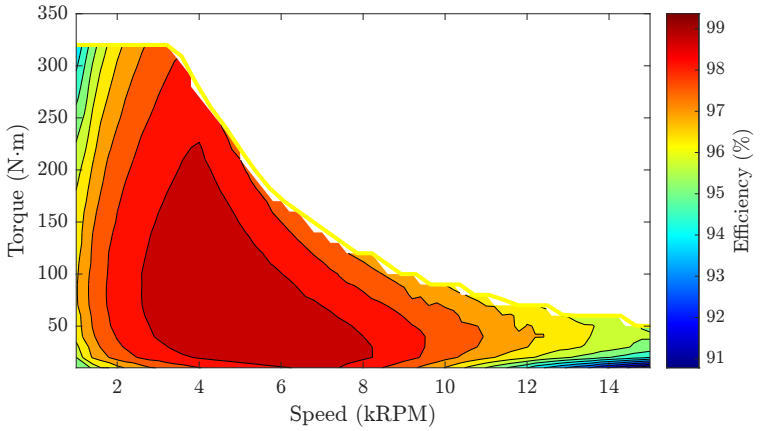


Figure 6.2: Efficiency map of the six-phase SiC-based inverter driving a 100 kW, 4 kRPM, 320 N·m permanent magnet synchronous machine (f_s = 30 kHz, T_J = 80 °C, V_{dc} = 800 V).

where C is the capacitance and Z_C is the impedance of the capacitor. It is noteworthy to highlight that film and ceramic capacitors are usually operate at a switching frequency well below the resonant frequency of the capacitor ($\omega_r = 1/\sqrt{ESL \cdot C}$) in motor drive applications. In such region, the capacitive reactance is dominant, and therefore, the parasitics of the capacitor are negligible [215]. Considering the performance and cost tradeoff, film capacitors are selected for the proposed inverter design.

As mentioned in Section 2.2, the DC-capacitor one of the largest component by size (see Figure 3.8a). Therefore, minimizing the sizing of the capacitors can greatly increase the power density of the inverter. Before the physical sizing of the capacitors can be considered it is imperative to first ensure they meet the electrical requirements of the design which are: (i) the capacitors' current rating, $I(C_B)$ must be larger than the input current ripple, $I_{C,min}$ and (ii) the total capacitance of the DC-capacitor

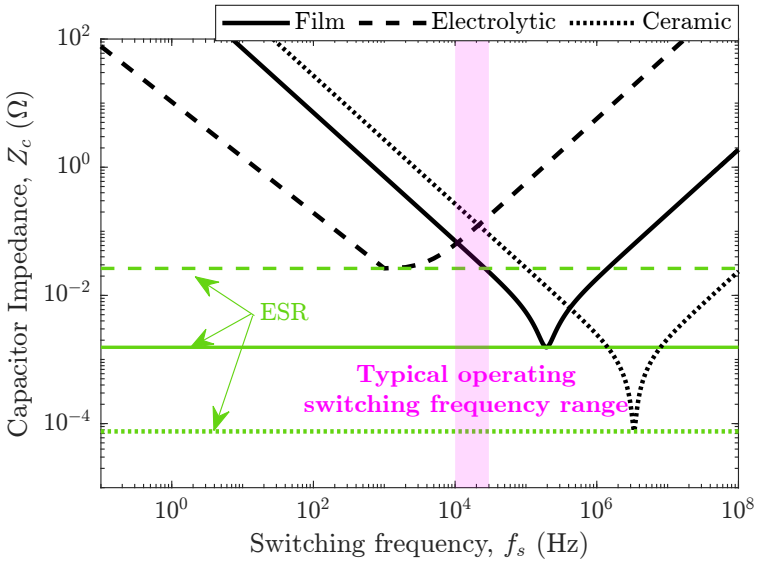


Figure 6.3: Impedance comparison between different DC capacitor banks. Capacitor bank sized for a 100 kW inverter with 5% allowable voltage ripple at 800 Vdc.

bank, C_B should be large enough to minimize the voltage ripple, ΔV_{pp}, typically within 5%. The mathematical expressions for such design criteria are given in (5.4.3) and (5.4.4) in Section 5.4 for an asymmetric six-phase drive are defined as [37]:

$$I(C_B) \geq I_{C,min} = 5/4 \cdot I_L \tag{6.2.2}$$

$$C_B \geq C_{min} = \frac{4\sqrt{3}I_L}{21 f_s \Delta V_{pp}} \tag{6.2.3}$$

where C_{min} is the capacitance required to maintain a certain voltage ripple. In addition to the electrical constraints, it is desirable to reduce the volume of the DC-bus capacitor to improve the power density and decrease its impedance to improve the efficiency. Hence, a multi-objective optimization problem arises with a *Pareto optimum solution* [237]. To find the optimal DC-capacitor bank, a utility weighted-sum objective function is defined as:

$$C_B^* = \arg\min \Big(w_1 V(C_B) + w_2 Z(C_B) + w_3 \cdot 1/I(C_B) \Big) \tag{6.2.4}$$

subject to (6.2.2), (6.2.3), and

$$C_B = (n_s \cdot n_p) \cdot C, \tag{6.2.5}$$

where

$$n_s = \max \left[\frac{V_{dc}}{V_r}, \frac{V_{pk}}{V_s} \right], \tag{6.2.6}$$

$$n_p = \max \left[\frac{I_{C,min}}{I_C}, \frac{n_s C_{min}}{C} \right], \tag{6.2.7}$$

$Z(C_B)$ is the impedance of C_B as defined in (6.2.1). n_s and n_p are the number of DC-capacitor cells connected in series and/or in parallel, respectively. $V(C_B) = n_s n_p V(C)$ and $I(C_B) = n_p I_C$ are the volume and current rating of the DC-capacitor bank calculated from the total number of capacitor cells in the bank, where $V(C)$ is the volume of a single capacitor cell in the bank. V_{dc} and V_{pk} are the rated and peak DC-link voltages, respectively. V_r and V_s are the rated and surge capacitor voltages, respectively. I_C is the rated RMS current of the capacitor cell, and w_i are scalar weighting factors associated with the i^{th} objective function. Note that

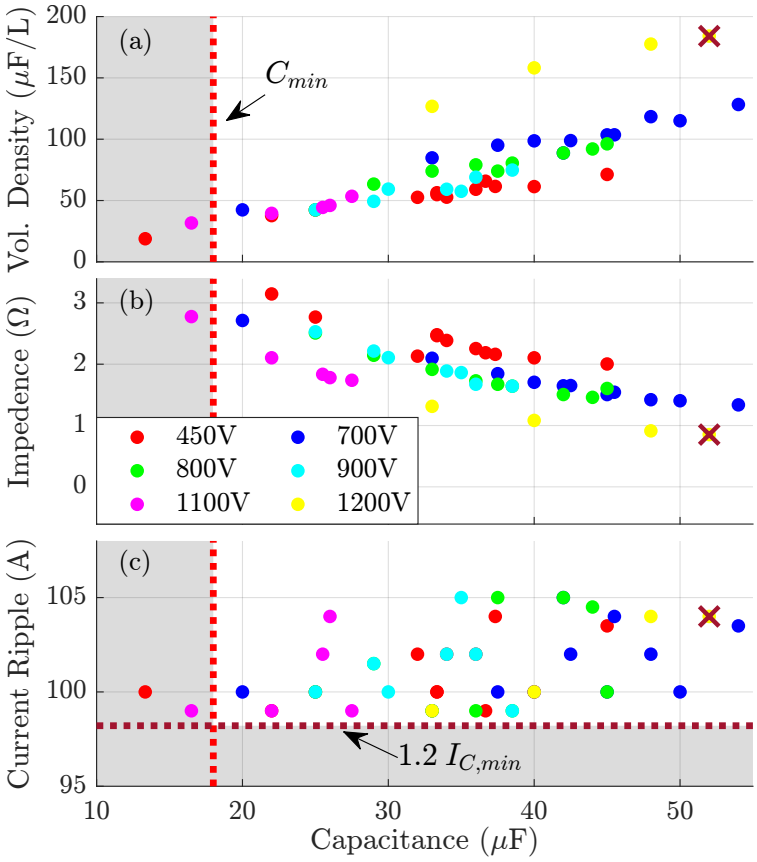


Figure 6.4: Film capacitor candidates from Vishay (MKP1848 series) considering minimum capacitance and current ripple rating: best candidate marked with an X. (a) Volumetric capacitance density. (b) Impedance. (c) Current ripple.

the minimization function considers the reciprocal of $I(C_B)$ since it is desirable to maximize the power rating of the DC-capacitor bank. The optimization problem is solved for the MKP1848 film DC-capacitors by Vishay [238] with a 20% safety margin for $I(C_B)$. The values of the objective functions for the evaluated capacitors are depicted in Figure 6.4, where the best candidate is marked with an 'X.' The optimum DC-capacitor bank is C_B^* = 52 μF built from thirteen MKP1848612704K2 capacitors (4 μF, 1200 V, 8 A) connected in parallel, and occupying a volume of 0.28 L. Note that this C_B^* is one of the optimal Pareto points for the selected w_i's, where volume minimization was given the highest priority to achieve the highest power density possible. In other words, other Pareto optimal points can be found for a different set of w_i's.

The designed DC-capacitor bank is a through-hole PCB mount package that is integrated in the power PCB design as detailed next.

6.3 Power Board Design

A PCB design is selected to the power circuit owing to the low number of the power SiC discrete MOSFETs, which provides a competitive edge when considering parasitic inductance minimization. The power PCB is made of six layers of 113 g (4 oz) Copper to handle the power ratings of the proposed inverter. The layer stack up considers the forward and return current paths to be on opposing layers for flux cancellation, and the DC-capacitors are placed as close as possible to the SiC MOSFETs to minimize the commutation loops of the six half-bridge switching legs. Figure 6.5 depicts the six layers stack up of the Power PCB. Copper width and weight in the PCB were

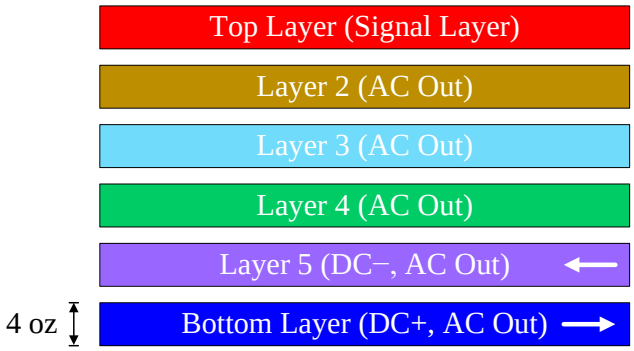


Figure 6.5: Layer stack-up of the power PCB.

designed in accordance with the Institute for Printed Circuits (IPC) standard IPC-2221A [239]. Low voltage signals are placed on the top layer to be as close as possible to the gate driver board placed on top and to separate the low voltage signals from the high voltage ones. However, in situations where separate layers were not feasible, the guidelines outlined in the IPC-2221A standard were followed [239]. Specifically, a minimum electrical clearance of 0.25 mm is maintained, with an additional 0.25 mm for every 100 V above 500 V. Considering V_{dc} = 800 V, a clearance of 1 mm was established to prevent interference between high and low voltage nets.

As for component placement, the MOSFETs and DC-capacitors are placed on the bottom layer to yield an almost flat top layer surface for gate driver board placement. Also, the difference in height between the MOSFET and the DC-capacitor is occupied effectively with the active thermal management system underneath the MOSFET, as will be discussed in this chapter.

In addition to the discrete SiC MOSFETs and DC-capacitors, the power board also includes on-board current sensors on the top layer. The top layer also includes surface mount connectors to interface the MOSFETs to the gate driver board atop of it as well as current sensor output and DC terminals for a DC-bus voltage sensor on

the gate driver board. The schematic of the power board is included in Appendix A.

6.3.1 On-Board Current Sensors

The on-board current sensors are coreless, hall-effect monolithic IC chips from Allegro Microsystems [240]. Employment of such sensors eliminates the need for the bulky core-based hall effect sensors. For six-phase inverter applications, this effectively mitigates the increased sensors drawback.

On the other hand, the current sensor ICs pose a design challenge pertaining to the PCB trace whereby a notch design must be incorporated underneath the IC, as shown in Figure 6.6. Therefore, the current density through the notch and the resulting temperature rise must be carefully designed. An electrothermal analysis was conducted using Ansys Q3D and Ansys Icepak FEA and computational fluid dynamics (CFD) software packages to yield a notch design that satisfies the maximum operating temperature of the current sensor IC (150 °C) and the maximum allowable temperature for the PCB material, which is 170 °C for FR4-TG170. The AC output trace is made up of five layers and each layer is 0.14 mm thick. The width, length,

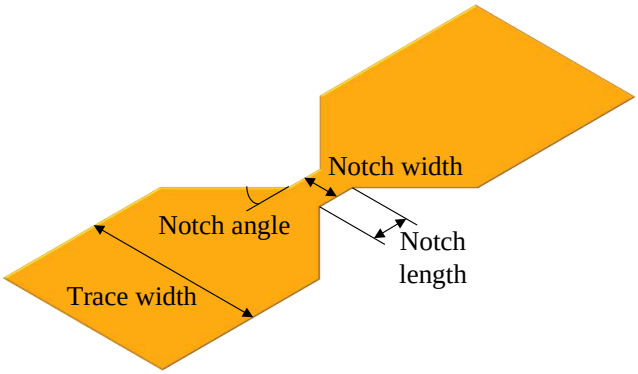


Figure 6.6: Notch design for PCB trace underneath the on-board current sensor IC.

and angle of the notch as well as the width of the trace are iteratively modified to satisfy the thermal boundary conditions. Figs. 6.7a–6.7d present the electrothermal simulation results for four design iterations of the power board section containing the AC output trace, simulated at still air condition, continuous current of 100 A $\approx 1.5I_L$, and an ambient temperature of 60 °C. In Iteration A, the maximum temperature constraint was violated. To address this issue, the notch width was doubled in Iteration B, resulting in the satisfaction of the design constraints. In Iteration C, the physical

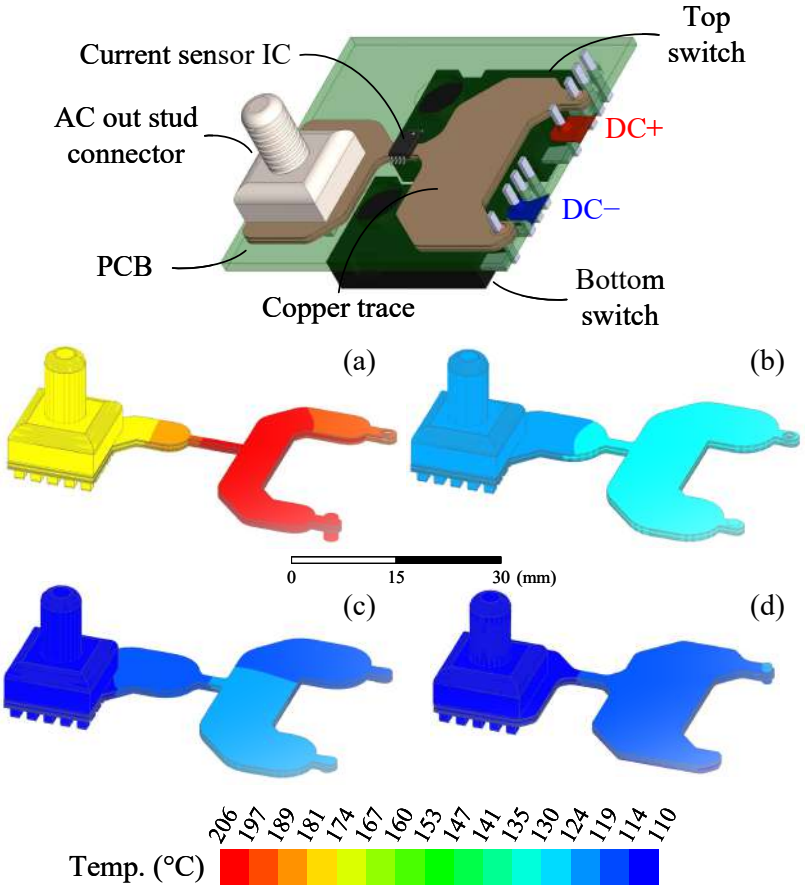


Figure 6.7: Electrothermal analysis for the AC output PCB trace in still air condition at 60 °C ambient temperature. (a)–(d) Iterations A–D, respectively.

dimensions were maintained as in Iteration B, but via stitching was introduced between the AC output layers. However, this modification only provided a negligible thermal improvement at the notch, while causing a slight increase in the stray inductance of the trace. Subsequently, via stitching was removed in Iteration D and the trace width was doubled compared to Iterations B and C. As a result, a temperature reduction of about 15 °C and a stray inductance reduction of 17% were achieved in Iteration D compared to Iteration C. Iteration D exhibited a maximum temperature of 119.4 °C, which is below the specified boundary conditions. Therefore, the design configuration of Iteration D was adopted in the final PCB design. Table 6.3 lists the notch and trace parameters used in the four iterations.

As for the physical size of the power board, the dimension bottlenecks were found to be from the power circuit itself and the associated gate driver of the SiC MOSFETs. The length was restricted by the length sum of the DC-capacitor bank, the AC output trace, and a separation distance between the DC-capacitors and MOSFETs to allow for heat sink walls; a total of 127 mm. In terms of width, the minimum gate driver circuit width was around 20 mm. As such, the total width of the PCB is 240 mm for the twelve SiC MOSFETs placed on a single row.

Table 6.3: Trace notch parameters and impedance for on-board current sensor

Design	**Trace**	**Notch**			**Impedance**	
	Width	**Length**	**Thickness**	**Angle**	**[mΩ]**	**[nH]**
A	6 mm	8 mm	1 mm	90°	0.428	37.0
B	10 mm	5 mm	2 mm	45°	0.211	31.9
C[†]	10 mm	5 mm	2 mm	45°	0.210	32.0
D	20 mm	5 mm	2 mm	45°	0.202	26.7

[†] Same as Design B with via stitching

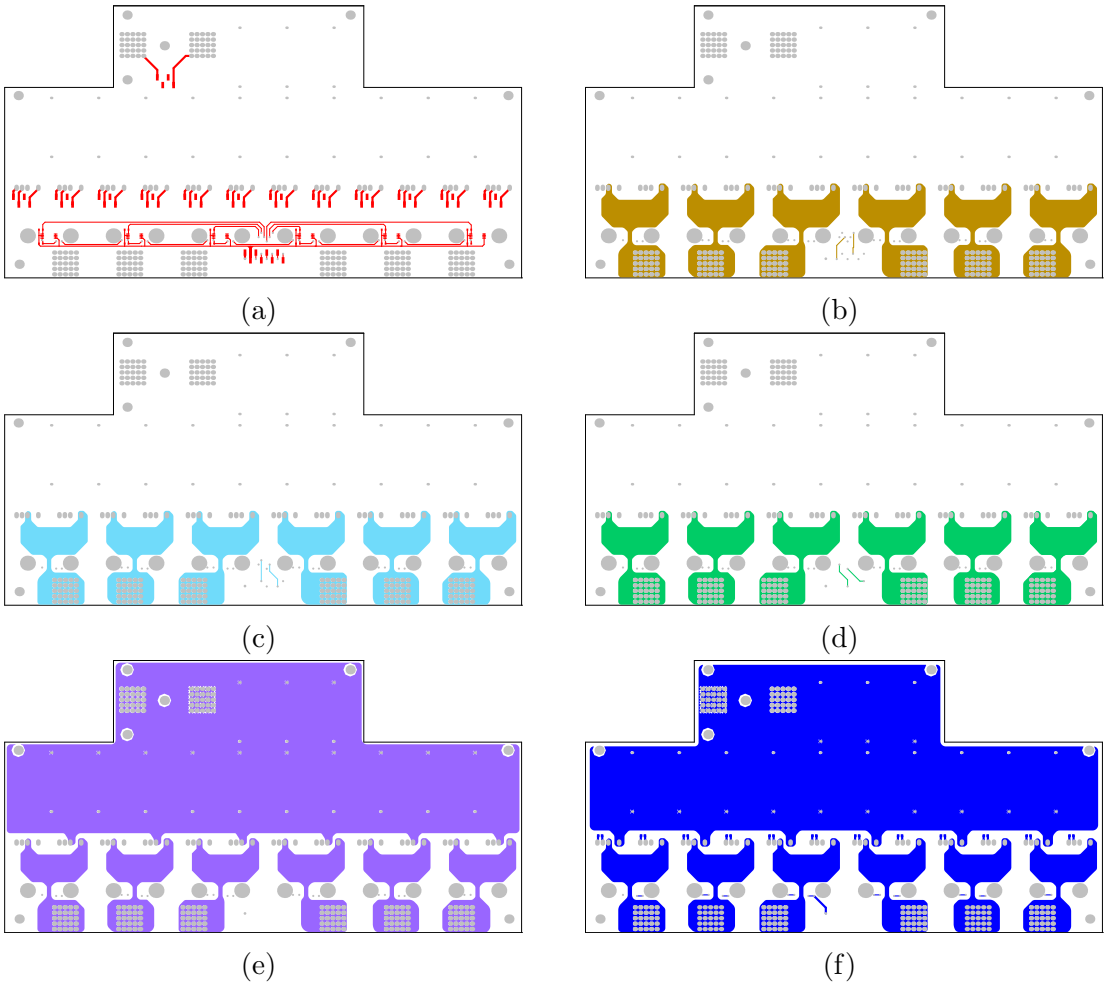
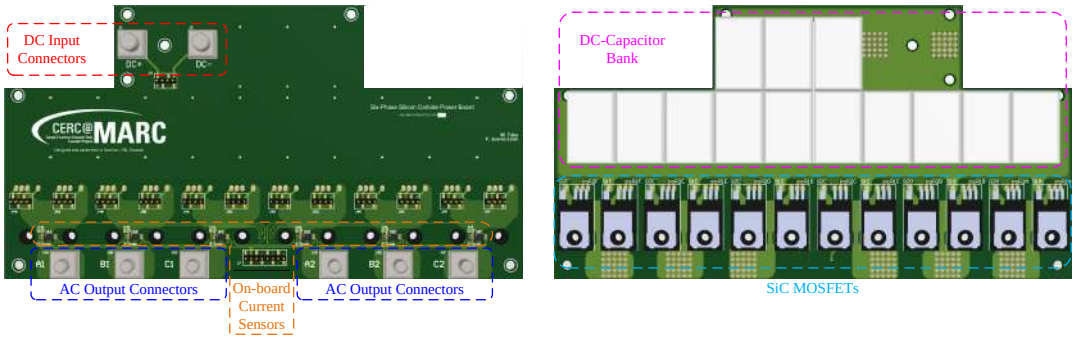


Figure 6.8: Power board layout. (a)–(f) Layers 1–6, respectively.

6.3.2 Impedance Analysis

Stray inductance analysis of the power commutation loop is imperative to check for design integrity and electromagnetic compatibility (EMC). Sources of stray inductance in the present design are: MOSFET self-inductance, DC-bus capacitor ESL, and inductance of PCB traces. Figure 6.10 depicts a single-phase equivalent circuit of the inverter with the main stray inductances in the commutation loop. While the



(a) (b)

Figure 6.9: Power board 3D view. (a) Top view. (b) Bottom view.

Table 6.4: Parameters for the commutation loop voltage overshoot analysis

Parameter	Symbol	Value	Unit
DC-bus voltage	V_{dc}	800	V
Rated switch voltage	V_{sw}	1200	V
Max rated current	$I_{r,max}$	130	A_{pk}
Current falling time	t_{fall}	13	ns

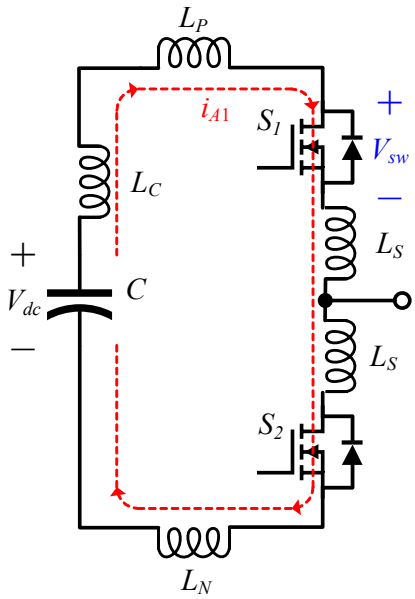


Figure 6.10: Equivalent circuit for the commutation loop on the Power PCB.

Table 6.5: Commutation loop stray inductances

Category	Parameter	Symbol	Value (nH)
Capacitor Bank	DC-capacitor bank ESL	L_C	1.92
Switch	Self-inductance	L_S	5.00
PCB Polygon Pour	Top switch polygon inductance	L_P	7.28
	Bottom switch polygon inductance	L_N	16.92
	Mutual top-bottom inductance	L_{PN}	5.47

self-inductance of the MOSFET, L_S is not reported in the datasheet, a 5 nH is estimated for a typical SiC MOSFET of the same package. The DC-bus capacitor ESL, L_C is found based on the datasheet and the bank design in Section 6.2. Inductance of the PCB traces are found using Ansys Q3D simulation. The voltage overshoot across the switch can be found by applying Kirchhoff's voltage law (KVL) to the commutation loop in Figure 6.10 as:

$$V_{sw} = V_{dc} + (\underbrace{L_C + 2L_S + L_P + L_N - 2L_{PN}}_{L_{loop}})\left|\frac{di_{A1}}{dt}\right| \tag{6.3.1}$$

where L_P is the inductance of the PCB polygon pour between the DC-capacitor bank positive terminal and the drain of the top switch, L_N is the inductance of the PCB polygon pour between the DC-capacitor bank negative terminal and the source of the bottom switch, L_{PN} is the mutual inductance between the positive and negative polygon pours, and L_{loop} is the total loop inductance. The maximum loop inductance, $L_{loop-max}$ is found to be 40 nH, by using the maximum ratings of the inverter as listed in Table 6.4. Based on the stray inductances in Table 6.5, L_{loop} of the inverter design is 25.18 nH, 37% lower than $L_{loop-max}$. Put otherwise, the expected overshoot voltage is 1,020 V, which is acceptable for the switch ratings. Therefore, a snubber-less design

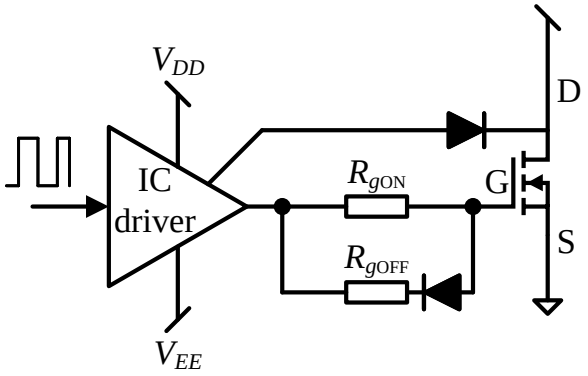


Figure 6.11: High-level schematic diagram of the gate driver circuit.

is achieved.

6.4 Gate Driver Board Design

A gate driver circuit is required to deliver the PWM signals that control the switching of the SiC MOSFET device. The PWM signal must have high voltage and high current capabilities that cannot be provided directly by the microcontroller, whose about is at the transistor-transistor logic (TTL) level [72]. Hence, the gate driver works as an interface between the microcontroller and the power semiconductor devices, as shown in Figure 6.11.

6.4.1 Circuit Design

As for the SiC MOSFET, specific design criteria must be taken into considerations that distinguishes it from Si MOSFET and Si IGBT [183, 241, 242]. Firstly, a relatively higher gate drive voltage of 15–20 V is recommended to provide the lowest ON-resistance. However, the higher supply voltage does not necessarily mean a higher power consumption since the capacitance (and hence the required charges) of

SiC MOSFET are significantly lower when compared to its Si counterparts. Secondly, SiC MOSFET should be pulled-down below ground level (typically -5 V) to ensure a proper turn-OFF since gate threshold voltage, V_{TH} can be <2 V. Thus, the gate driver must facilitate an asymmetrical range of gate-to-source voltage, V_{GS}. Thirdly, V_{GS} must have fast falling and rising edges, in the order of nanoseconds, to enable the high switching capability. Such delicate features are mainly attributed to low transconductance and higher gate resistance. Commercial off-the-shelf SiC MOSFET gate drivers can be sourced from Analog devices (e.g. ADuM4135), Infineon (e.g. 1EDI60I12AF), Texas Instruments (e.g. ISO5852), etc. [241]. However, a custom-made gate driver circuit, based on the device characteristics listed in Table 6.6, is sought in this inverter design to specifically meet the overall design requirements and to deliver the most compact solution, and thus, the highest power density. This is also driven by the increased required number of gate drivers circuits for the six-phase inverter. The schematic of the gate driver board is included in Appendix A.

Power Supply

In terms of power supply, there are multiple power supply solutions to facilitate the aforementioned power requirements of the SiC MOSFET, namely a bootstrap circuit, flyback transformer, multitap transformer, and isolated DC/DC converter [243]. The latter is selected for its design flexibility, simplicity, and adequate regulation. The power supply circuit is designed to provide an asymmetric power supply of V_{DD}/V_{EE} =15V/-4 V, as per the manufacturer's recommendation for the C3M0016120K. The selected isolated DC/DC converter is the MGJ2D121505SC by Murata Power Solutions with a 2 W capability sufficient to drive the gate driver

Table 6.6: Gate driver design parameters for the C3M0016120K SiC MOSFET using UCC21750-Q1 driver IC

Category	Parameter	Symbol	Value	Unit
SiC MOSFET	On-state gate voltage	$V_{GS(\text{ON})}$	15	V
	Off-state gate voltage	$V_{GS(\text{OFF})}$	-4	V
	On-time delay	$t_{d(\text{ON})}$	34	ns
	Off-time delay	$t_{d(\text{OFF})}$	65	ns
	Rise time	t_r	33	ns
	Fall time	t_f	13	ns
	Internal gate resistance	$R_{G(int)}$	2.6	Ω
	Gate charge (total)	Q_G	211	nC
Gate Driver IC	Internal turn-on resistance	R_{OH}	0.7	Ω
	Internal turn-off resistance	R_{OL}	0.3	Ω
	DESAT threshold voltage	V_{DESAT}	9	V
	Internal blanking time	$t_{blk(int)}$	200	ns
	Internal current charge current	I_{chg}	500	μA

circuit.

Gate Driver IC

The selected driver IC is the UCC21750-Q1 from Texas Instruments owing to its high current driving capability, eliminating the need for a and integrated protection features such as short circuit and active miller clamp [244]. The key parameters of the UCC21750-Q1 needed in the gate driver circuit design are listed in Table 6.6. The driver IC is controlled via the microcontroller that sends the logic PWM signal and the reset/enable ($\overline{RST}/EN$) command. The microcontroller also receives information about the status of the circuit through a ready (RDY) and fault ($\overline{FLT}$) signals.

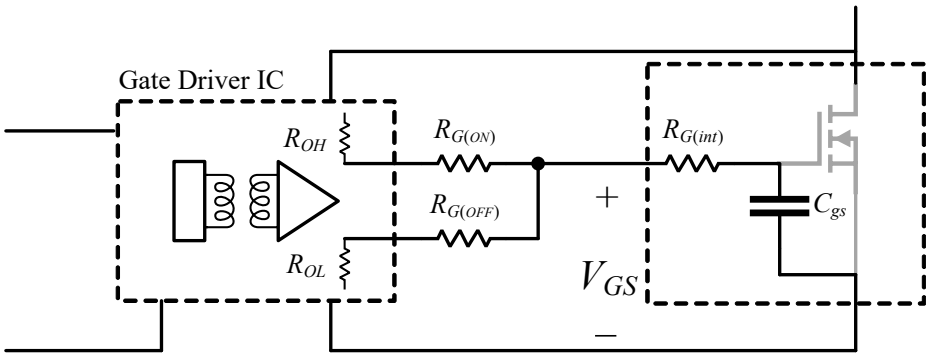


Figure 6.12: Gate Driver Turn-ON and Turn-OFF power dissipation circuit.

Gate Resistance Design

As shown in Table 6.6, the SiC MOSFET exhibits different turn-ON and turn-OFF characteristics. Therefore, different gate resistors are used for an improved performance. Design criteria for such resistors include preventing switching spikes and choosing low values to reduce power losses.

$$I_{G(\text{ON})} = \frac{V_{GS(\text{ON})} - V_{GS(\text{OFF})}}{R_{G(\text{ON})} + R_{OH} + R_{G(int)}} = \frac{Q_G}{t_{d(\text{ON})} + t_r} \tag{6.4.1}$$

$$I_{G(\text{OFF})} = \frac{V_{GS(\text{ON})} - V_{GS(\text{OFF})}}{R_{G(\text{OFF})} + R_{OL} + R_{G(int)}} = \frac{Q_G}{t_{d(\text{OFF})} + t_f} \tag{6.4.2}$$

$$I_{avg} = \frac{Q_G}{f_s} \tag{6.4.3}$$

Substituting the parameters in Table 6.6 in (6.4.1) and (6.4.2), the $I_{G(\text{ON})}$ and $I_{G(\text{OFF})}$ are 3.15 A and 2.71, respectively. Therefore, the $R_{G(\text{ON})}$ and $R_{G(\text{OFF})}$ are designed to be 2.73 Ω and 4.12 Ω, respectively. Multiple resistors are placed in parallel to provide such values and satisfy the power requirement through the resistors.

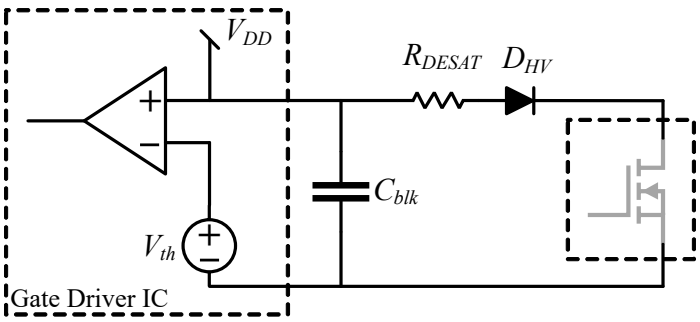


Figure 6.13: Circuit diagram of the DESAT gate driver circuit.

Overcurrent and Short-Circuit Protection

The gate driver IC is equipped with a desaturation (DESAT) pin that enables overcurrent and short circuit protection. Figure 6.13 shows the DESAT circuit design. The protection is implemented by monitoring the V_{DS} of the SiC MOSFET indirectly using an RC circuit and a high voltage diode. In a fault condition, V_{DS} increases such that the DESAT diode is reverse bias. Consequently, the external DESAT capacitor, C_{blk} is charged and its voltage rises above the DESAT threshold voltage, V_{DESAT}. This in turn is detected by the internal DESAT comparator, thus detecting a fault. In this case, the gate signal is pulled down to V_{EE}, and RDY and $\overline{FLT}$ outputs are pulled down to 0 V. The blocking time for the DESAT protection is a function of the driver IC charging current, I_{chg}, C_{blk}, forward voltage voltage of the DESAT diode, V_f, and R_{DESAT}. It can be designed based on the following relation:

$$t_{blk} = \frac{C_{blk} \cdot \left[V_{DESAT} - (V_f + I_{chg} \cdot R_{DESAT})\right]}{I_{chg}} \tag{6.4.4}$$

A 27 pF and 1 kΩ for C_{blk} and R_{DESAT} were chosen to yield a t_{blk} of 0.4 μs. Figure 6.14 shows the complete gate driver circuit design with its DC/DC power supply. A PCB design is sought next to build this circuit for each of the twelve switches of the

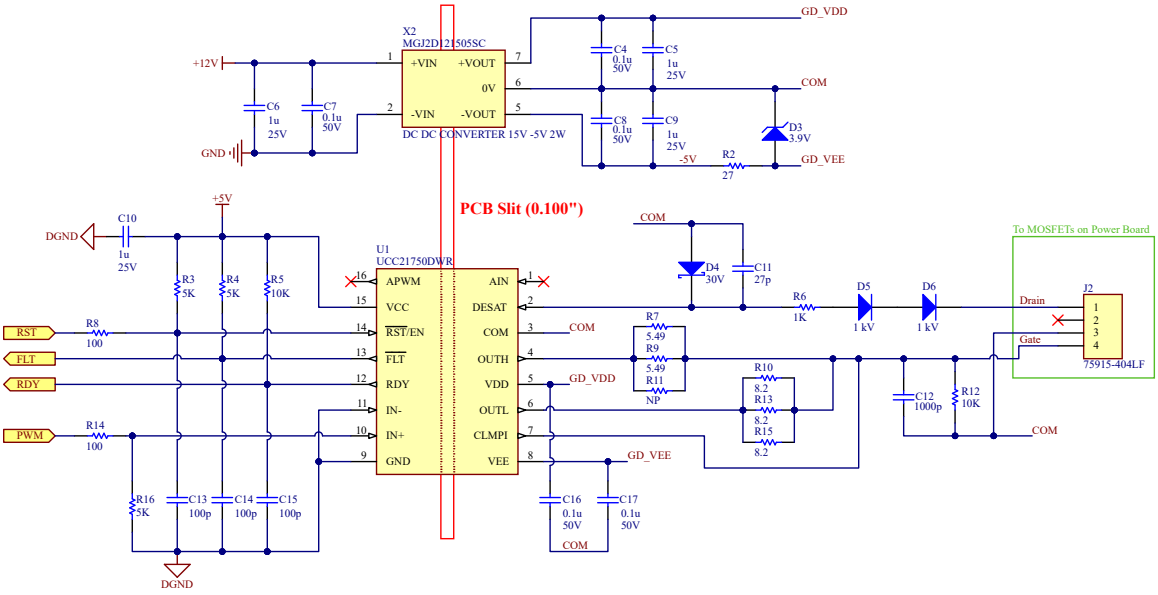


Figure 6.14: Schematic of isolated gate driver circuit design for SiC MOSFET.

six-phase inverter, along with general-purpose inputs/outputs (GPIOs) and sensors interface to the control board.

6.4.2 PCB Design

The PCB components are placed on both sides of the PCB to reduce the physical dimensions as much as possible as shown in Figure 6.15. Moreover, a slit of 2.54 mm is placed under the transmitter/input and receiver/output sides of the driver IC/isolated DC/DC converter for electromagnetic isolation. Similar to the power board, the layer stack up of the gate driver PCB considers the forward and return current paths to be on opposing layers as shown in Figure 6.16. The layer stack-up of the gate driver board, shown in Figure 6.16, is made up of six 1 oz layers for better distribution of isolated ground planes. The PCB also includes the DC-bus voltage measurement using an isolated amplifier ISO224BDWV from Texas Instruments. Header connectors

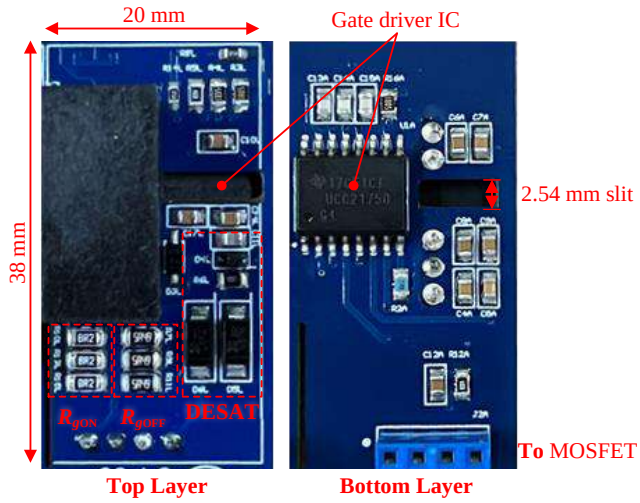


Figure 6.15: Assembled gate driver circuit for SiC MOSFET.

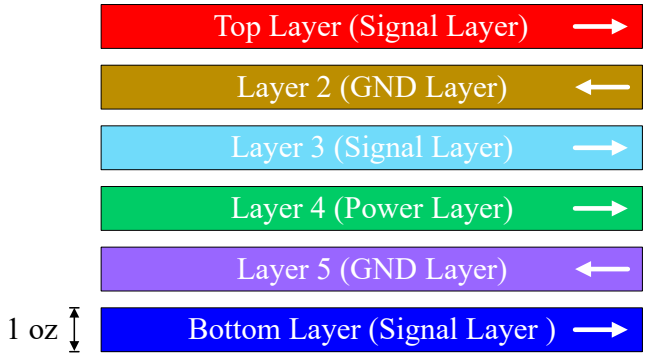


Figure 6.16: Layer stack-up of the gate driver PCB.

are placed on the top layer to interface control signals to the gate driver ICs, current sensors, and DC-bus voltage sensor. Figure 6.18 depicts the 3D view of the designed gate driver board.

6.5 Control Interface Board Design

A control DSP-based board, comprising a TMS320F28379D chip, was planned to be designed. Unfortunately, due to the COVID-19 pandemic and subsequently the

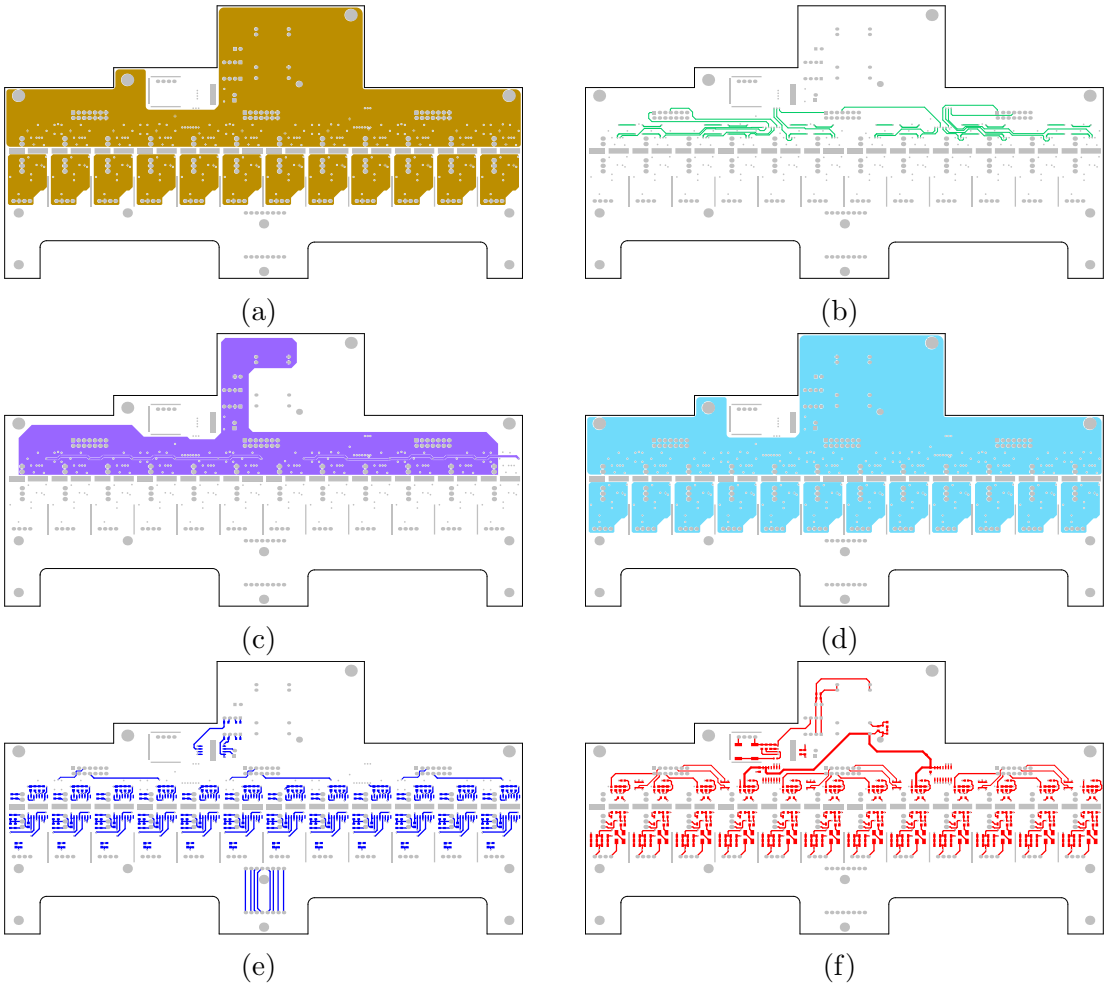


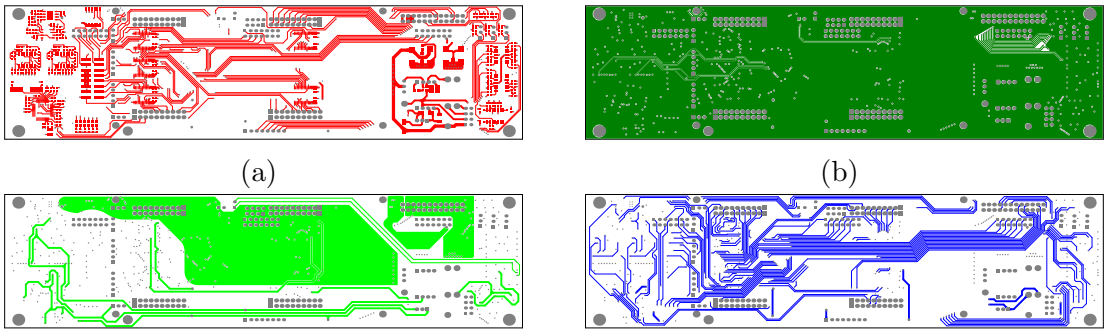
Figure 6.17: Gate driver board layout. (a)–(f) Layers 1–6, respectively.

Figure 6.18: Gate driver board 3D view. (a) Top view. (b) Bottom view.

shortage of electronic chips [245], a full control board was hard to realize in the time frame allotted for this thesis. Instead, a Launchpad^{TM} LAUNCHXL-F28379D [246] development board, comprising of the TMS320F28379D chip and other peripheral ICs, is used. However, to integrate the Launchpad in the designed inverter, an interface control board is needed.

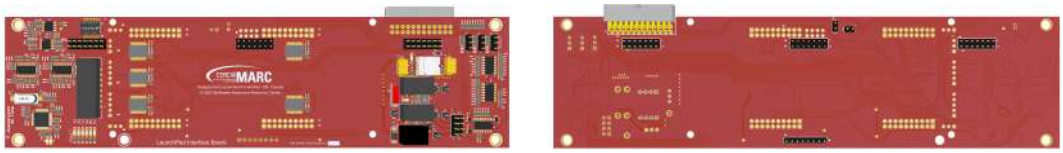
The interface control board, as the name suggests, interfaces the signals between the gate driver board developed in the previous section and the Launchpad. The signals interfaced from the gate driver board are the PWM, $\overline{RST}/EN$, RDY, and $\overline{FLT}$. The interface of such signals is implemented using a 5 V to 3.3 V level-shifter transceiver SN74LVC4245A from Texas Instruments. Additionally, the board encompasses signal conditioning circuitry for the on-board current sensors and DC-bus voltage sensor as well as general-purpose analog and digital inputs/outputs (IOs) available externally for the user at the inverter housing. The interface board also includes a low voltage (LV) power filter to eliminate high frequency noise before supplying the power the LaunchPad, gate driver and power boards. Lastly, a resolver interface circuit is designed for PMSM electric drive purposes using a resolver-to-digital AD2S1210 from Analog Devices.

For the board design, a four layer PCB, with 1 oz thickness per layer, is designed as shown in Figure 6.19. The board dimensions are 62 mm x 240 mm. Figure 6.20 depicts the 3D view of the designed control interface board. The schematic of the control interface board is included in Appendix A.



(a) (b) (c) (d)

Figure 6.19: Control interface board layout. (a) Top signal layer. (b) Ground layer. (c) Power layer. (d) Bottom signal layer.



(a) (b)

Figure 6.20: Control interface board 3D view. (a) Top view. (b) Bottom view.

6.6 High Voltage Cable Sizing

HV cable sizing should be designed properly. A cable that is too small will not withstand the rated current and lead to a thermal event that cause serious failures. On the other hand, a cable that is too big adds weight and cost to the design. Cable sizing must satisfy two criteria: current-carrying capacity and allowable voltage drop. The HV AC and DC cabling of the inverter are sized in accordance with the IEC 60364-5-52 standard [247]. The current-carrying capacity is defined as [247]:

$$I_{capacity} = a \cdot S^m - b \cdot S^n \tag{6.6.1}$$

where S is the cross-sectional area of the conductor in mm^2, whereas a, b, m, and n are coefficient related to the method of installation. Table 6.7 lists the parameters used in (6.6.1) for a single-core >750 V cable installed on a floor. For AC cabling, since a six-phase system with two isolated neutrals count as two three-phase circuits, a reduction factor of 0.85 to the current-carrying capacity is applied [247]. Hence, $I_{capacity} \geq I_{rated}/0.85$.

The voltage drop in in DC cables and AC cables in Y-connected three-phase circuits can be determined as [247]:

$$u = c \cdot \left(\frac{\rho_c}{S}\cos\phi + \lambda \sin\phi\right) \cdot L \cdot I_{rated} \tag{6.6.2}$$

where u is the voltage drop in V, c is a coefficient equal to 1 for three-phase circuits and 2 for DC circuits, ρ_c is the resistivity of the conductor at 1.25 times the resistivity at 20 °C, L is the length of the cable, ϕ is the power factor angle, and λ is the reactance per unit length of the conductor. The values for ρ_c and λ are also listed in Table 6.7. Note that the voltage drop percentage for AC cables is with respect to the line-to-neutral voltage. Based on the IEC 60364-5-52 standard [247], the voltage drop must not exceed 5%. Based on the inverter specifications in Table 6.2, (6.6.1) is solved for S and rounded to the nearest commercially-available nominal cross-sectional area of the cable. Subsequently, u in (6.6.2) is checked whether it is less than 3% of the rated AC and DC voltages. The obtained results are summarized in Table 6.8 along with the sized cable glands.

Table 6.7: Parameters used for high voltage cable sizing

Category	Parameter	Value	Unit
Current-Carrying Capacity (6.6.1)	a	24	–
	b	0	–
	m	0.6	–
	n	0	–
Voltage Drop (6.6.2)	ρ_c	0.0225	$\Omega{\cdot}\text{mm}^2/\text{m}$
	λ	0.08	$\text{m}\Omega/\text{m}$
	c	1 or 2	–

Table 6.8: High voltage cable and cable gland sizing

Cable	Required S (mm^2)	Nearest S (mm^2)	Equivalent AWG	Voltage Drop	Cable Gland
AC	15	16	6	2%	M20
DC	46	50	1	1%	M25

6.7 Thermal Management System

The design of a thermal management system for traction inverters is deemed challenging. This stems from the ever-increasing power demand yet with a compact packaging. In the present 100 kW SiC-based six-phase inverter, a compact design for heat sink is sought to achieve a high power density and lightweight while maintaining a safe junction temperature. Active liquid cooling solution is sought for the proposed design since it is the preferred type of thermal management system in the auto industry [248]. Table 6.9 lists the boundary conditions for the design. The coolant is water/ethylene glycol mixture at 50% concentration. The inlet coolant temperature is assumed to be maintained at T_c =65 °C at a flow rate of 10 L/min. A conventional straight finned heat sink was designed to manage a heat loss, Q of 1.16 kW from the twelve MOSFETs attached to it (obtained in Section 6.1.1). A thermal interface

Table 6.9: Boundary conditions for heat sink design

Parameter	**Value**	**Unit**
Coolant type	Glycol 50/50	—
Coolant flow rate	10	L/min
Coolant inlet temperature	65	°C
Maximum junction temperature	125	°C
Total power	1.16	kW

material (TIM), made of Silicone with a thickness of 1 mm, is inserted between the MOSFETs and the heat sink to provide a galvanic isolation between the MOSFET drain and the Aluminum (Al) body of the heat sink. The objective from the heat sink is to keep the junction temperature of the MOSFETs below 125 °C.

Figure 6.21 depicts the thermal resistance model used in the design of the heat sink to determine the junction temperature and the fin length, L_F. From the equivalent thermal circuit, the relationship between the heat loss and temperature can be quantified as:

$$Q = \frac{T_j - T_c}{R_{TIM} + R_{HS} + R_F + R_{JC}} \tag{6.7.1}$$

where T_j and T_c are the junction and coolant temperatures, respectively, and R_{TIM}, R_{HS}, and R_F are the thermal resistance of the TIM, heat sink, and fins, respectively.

The thickness of the heat sink t_p, below the MOSFETs, was set to 3 mm, similar to commercial heat sinks. The pitch, s between the fins was set to 5 mm, with a spacing of 1.5 mm for the cooling channels between the fins. Hence, the fin thickness, t_F is 3.5 mm. The heat sink is made of Al for lightweight to increase the specific power of the inverter. The dimensions of the heat sink are listed in Table 6.10.

An analytical model is developed to empirically evaluate the junction temperature, T_j by calculating firstly the heat transfer coefficient, h of the coolant flow and

Table 6.10: Heat sink design specifications

Parameter	**Symbol**	**Value**	**Unit**
Heat sink thickness	t_p	3.0	mm
Fins pitch	s	5.0	mm
Width of cooling channel	W_p	30.0	mm
Length of cooling channel	L_p	240.0	mm
Thickness of TIM	t_{TIM}	1.0	mm
TIM Thermal conductivity	K_{TIM}	14.5	W/m·K

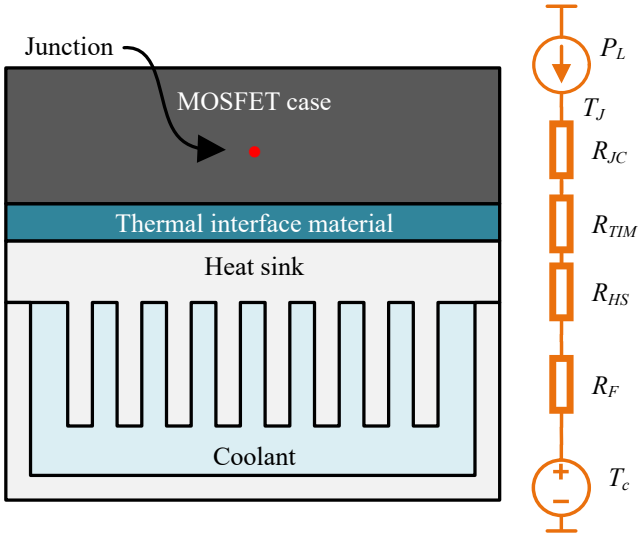


Figure 6.21: Thermal dissipation path of the inverter.

the fin efficiency. The analytical model, which is solved using a numerical program, is instrumental in the iterative design process in which recursive modifications evaluated before CFD analysis. This streamlines the design process and reduces the computational burden. The empirical analytical model is governed by the physics of the conducted heat transfer [249, 250].

Solving the analytical model for boundary conditions in Table 6.9, a fin length of 14 mm was selected to achieve a junction temperature of 102 °C. Moreover, the outlet coolant temperature is found to be 2 °C higher than the inlet temperature. A

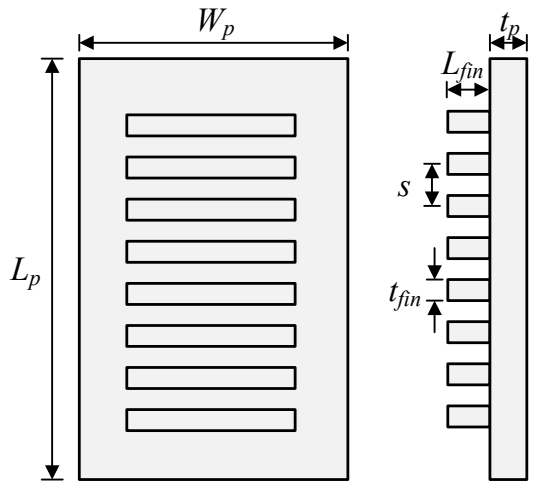
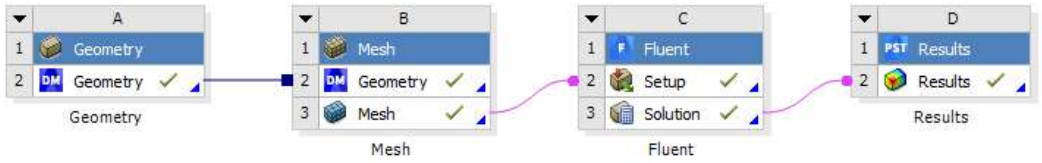
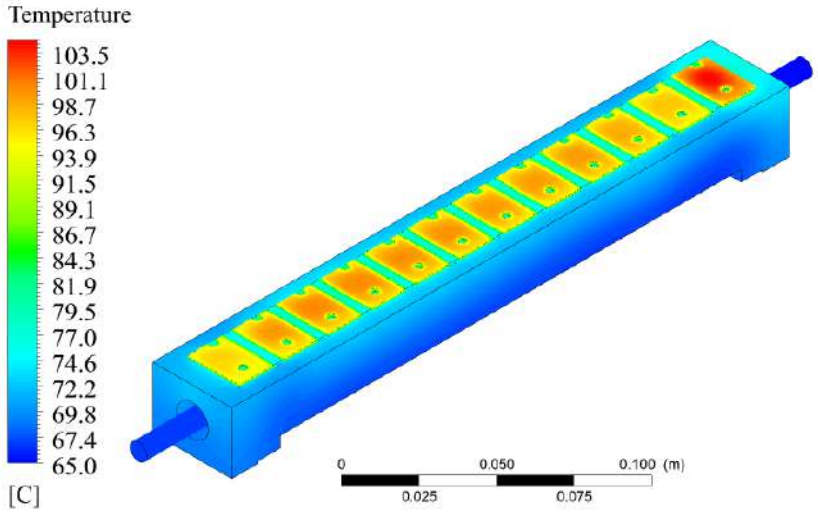


Figure 6.22: Finned base heat sink design.

CFD analysis was then conducted in Ansys Fluent to benchmark and verify the thermal results obtained from the analytical model. Figure 6.23a illustrates the Ansys CFD workflow for the thermal analysis. The number of mesh elements are 210,000 elements. The energy equation and continuity equations were activated for the numerical simulations. The K–ω method was used for the turbulence flow. The residual in the numerical solution for energy equation reached 1e–6, while for the continuity equation reached to 3e–3. A great match was found between the thermal junction temperature from the thermal model and the CFD model, as shown in Figure 6.23b. The CFD model exhibits a maximum junction temperature of 103.5 °C, close to the 102 °C obtained from the analytical result. The estimated pressure drop from the simulations was found to be 16.8 kPa, from inlet to outlet of the heat sink. The outlet temperature of the coolant was found to be 67 °C. To this end, the design requirements for the thermal management system are met, and the housing design is tackled next where the heat sink is integrated within the housing body. The "as-built" drawing of the heat sink is included in Appendix B.

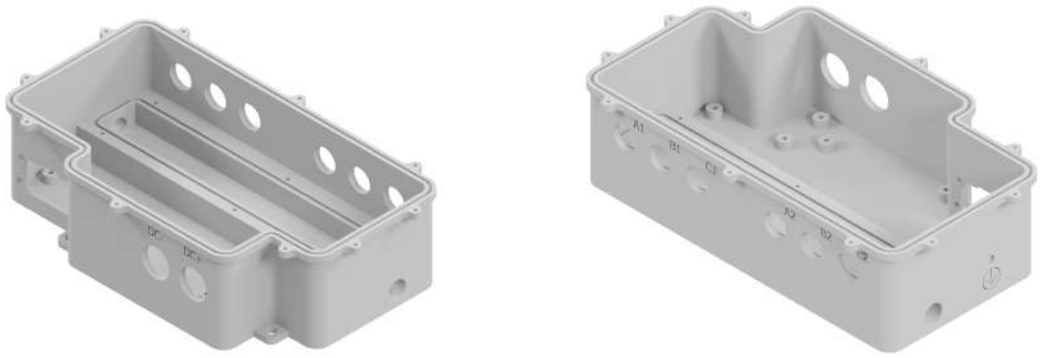


(a)



(b)

Figure 6.23: Ansys Fluent CFD analysis for the thermal management system. (a) Workflow setup. (b) Simulation result at 10 L/min.



(a) (b)

Figure 6.24: Isometric views of the designed inverter housing. (a) Front. (b) Back.

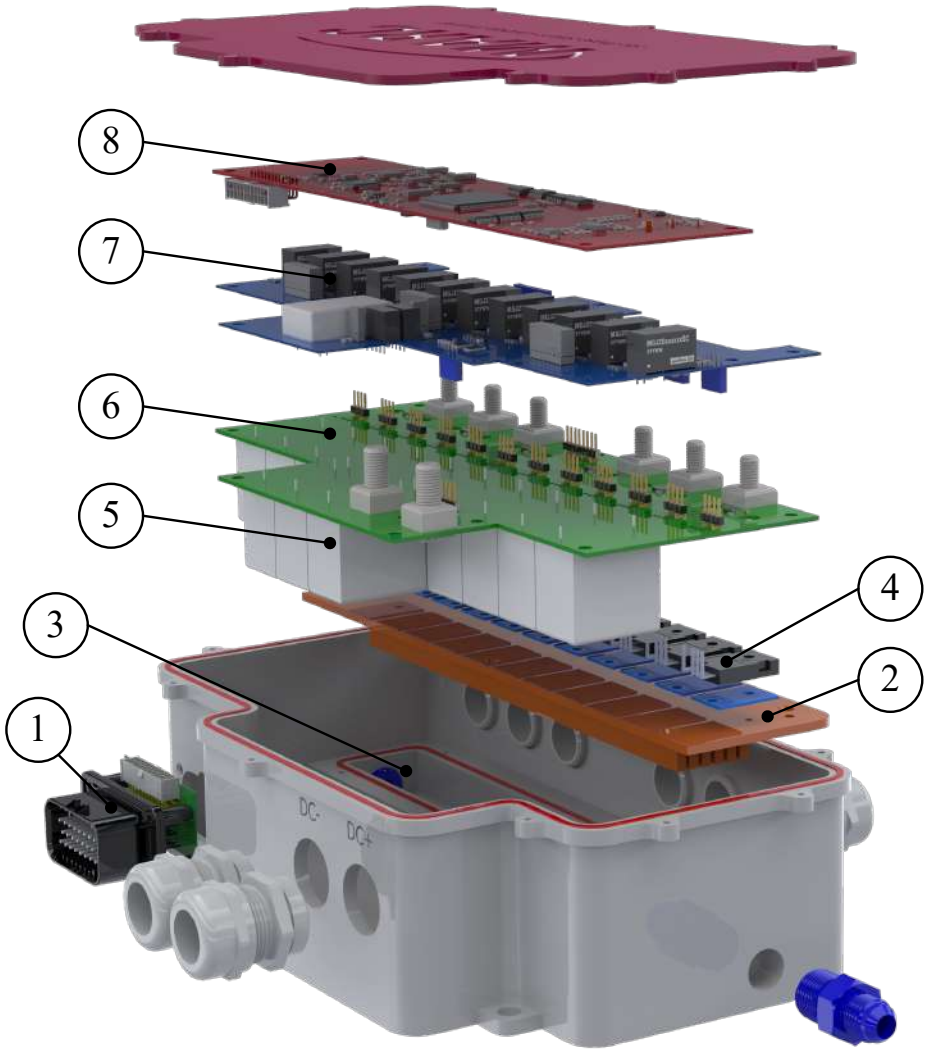


Figure 6.25: Exploded view of the inverter model. (1) Low-voltage connector with interface board. (2) heat sink. (3) Coolant channel. (4) Discrete MOSFETs. (5) DC-capacitor bank. (6) Power board. (7) Gate driver board. (8) Control board.

6.8 Mechanical Packaging

The mechanical enclosure of the inverter must provide 1) electrical shielding of the electrical components, 2) protection of electronic components against water and

dust—i.e., ingress protection (IP), 3) terminal interface of electrical (high voltage and low voltage) and cooling ports, and 4) harshness against vibration. The design of the mechanical enclosure should also observe manufacturing limitations and facilitate easy assembly and testing.

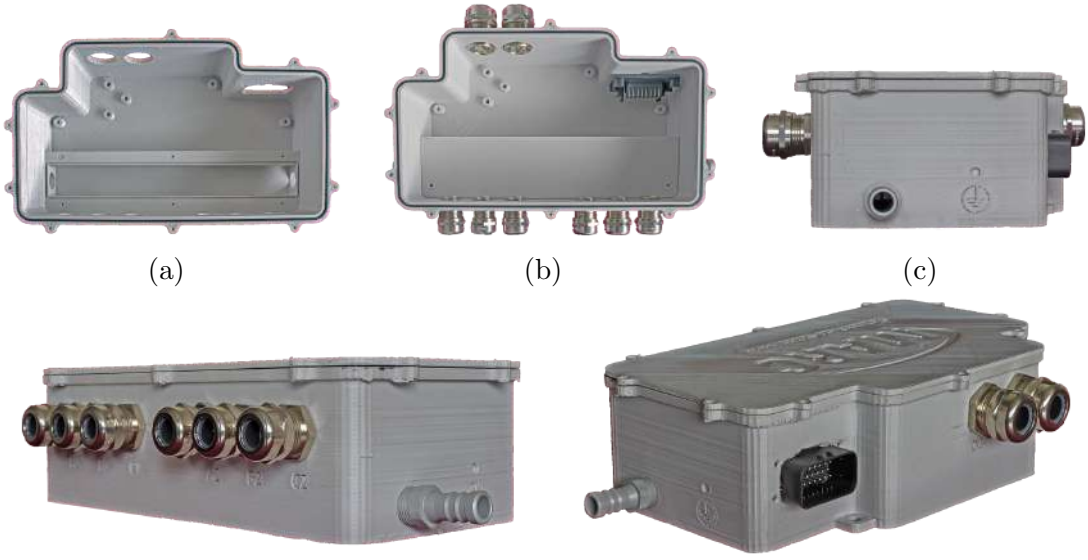
A comprehensive design process was undertaken to optimize power density while considering the thermal management system, cable glands, PCBs, and capacitor placement. The DC cable glands are sized for 1 AWG cables, whereas the AC cable glands are sized for 6 AWG cables, based on IEC 60364-5-52 standard [247] for shielded single-core 1 kV cables. The low voltage connector is a sealed automotive-grade one that encompasses control signals for DC-capacitor pre-charge, resolver interface for motor control purposes, CAN communication, and peripheral IOs. The detailed pin out of the LV connector is provided in Appendix C. The cooling ports are designed for $3/8''$ national pipe thread (NPT) size. The heat sink design in Figure 6.23b was integrated at the bottom of the enclosure by a having a channel of the same dimensions with a removable fin-base heatsink that is bolted inside in the enclosure with o-ring sealing. Similarly, o-ring sealing design is employed at the enclosure lid. Based on the lowest IP rating of the terminals, the IP rating of the designed inverter enclosure is IP68, which is in line with ISO 26262 standard for vehicle functional safety [251].

Figure 6.25 showcases an exploded view of the proposed MARC100 packaging. The base dimensions of the enclosure are determined by the geometry and dimensions of the PCBs, low voltage connector, and capacitors to be placed within it. The housing went through multiple iterations, and in each, the fitting of these electrical components was altered and optimized in an attempt to minimize the volume of

the design. The length and width of the enclosure are dictated by the PCBs, as discussed in Section 6.3. The height of the enclosure is constrained by the stacking of the PCBs and the capacitors. From bottom to top, the enclosure is packaged as follow: the capacitors and coolant channel, the power board, the gate driver board, and the control board. Prior to manufacturing, the enclosure design was tested for deformation due to vibration in FEA, as discussed in [252]. The maximum stress experienced by the enclosure due to a $2.5g$ acceleration was found to be lower than the yield strength of enclosure material. The "as-built" drawings of the enclosure and its lid are included in Appendix B.

6.8.1 3D Printing

To verify the dimensions of the designed mechanical housing, plastic prototypes were printed using a Modix Big-60 3D printer. The 3D printing parameters are listed in Table 6.11. The inspected dimensions include, but not limited to, cable gland holes, cooling ports, LV connector, O-ring grooves, and heat sink. Three iterations were printed starting with a low fidelity print and ending up with a high fidelity print that includes the small details like text engravings. Throughout the 3D printing process, the mechanical housing design was revised iteratively to yield the final design shown in Figure 6.24. Figure 6.26 depicts the final iteration of the 3D printed prototype assembled with the actual exterior parts. To this end, the housing design is ready for manufacturing.



(a) (b) (c)

(d) (e)

Figure 6.26: 3D printed inverter housing. (a) Un-assembled interior. (b) Assembled interior. (c) Side view. (d) Back isometric view. (e) Front isometric view.

6.9 Discussion and Benchmarking

The proposed MARC100 inverter features a peak output power of 175 kW with a peak power densities of 70 kW/L, respectively. The continuous power density (40 kW/L) exceeds the current targets set by the US DOE by threefold [8]. Figure 6.27 shows the breakdown of the MARC100 in terms of mass, volume, and cost. In terms of mass breakdown (Figure 6.27a), about half of the weight is attributed to the Al body of the enclosure and heat sink. In terms of volumetric breakdown (Figure 6.27b),

Table 6.11: 3D Printing Parameters

Printer model	Modix Big-60
Material	PETG
Fill percentage	15%
Nozzle size	0.6 mm
Layer height	0.3 mm

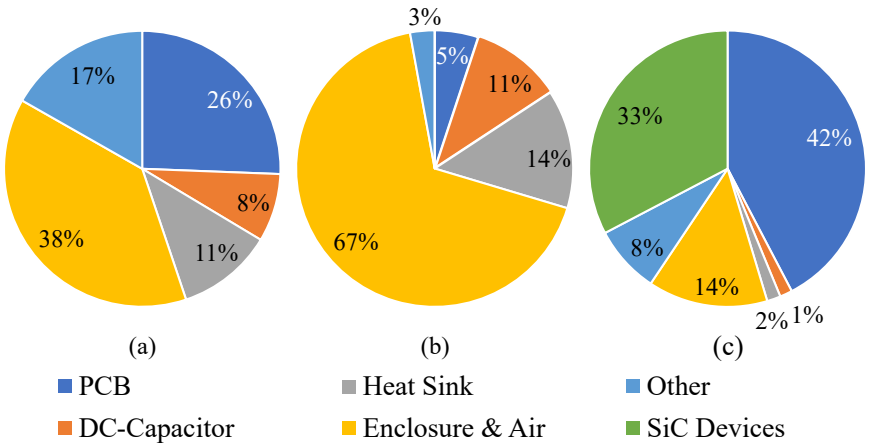


Figure 6.27: Breakdown of the proposed MARC 100 inverter by (a) mass, (b) volume, and (c) cost.

about three quarters the volume is occupied by the enclosure body and the air enclosed in it. This high percentage is attributed to design for testing capability to allow easy assembly and debugging. The DC-capacitor only occupies 11% of the total volume in the proposed inverter. In terms of cost breakdown (Figure 6.27c), the biggest contributor is the manufacturing cost of the power, gate driver, and control PCBs, followed by the cost of the SiC MOSFET discrete devices. In commercial inverters, the cost latter is usually prevails. However, since this the MARC100 is not yet in a mass production stage, the PCBs cost is relatively much higher. The manufacturing cost of the enclosure and heat sink amounts to 16%.

A second generation of the MARC100 has the potential to exhibit far higher power densities, exceeding the 100 kW/L threshold set by the US DOE for 2025. This can be achieved by reducing the spacing between the PCBs stack-up to minimize the free space occupied by air in the present design. Furthermore, the rated current of the MARC100 is at 60% of the SiC MOSFET, which can be increased to deliver more power. Lastly, a more advanced heat sink design, like pin-fin base, can be employed

Table 6.12: Comparison between commercial six-phase inverters and the proposed inverter

Specification	**Dana TM4, CO200 [24]**	**Koenigsegg, David [39]**	**Proposed, MARC100**
Overview			
Year	2018	2023	2023
Power device	Si	SiC	SiC
Continuous power	200 kW	525 kW	100 kW
Peak power	265 kW	700 kW	175 kW
DC-link voltage	600 V	850 V	800 V
Volume	40.6 L	10.0 L	2.5 L
Weight	26 kg	15 kg	3.76 kg
Peak power density	6.5 kW/L	70.0 kW/L	70.0 kW/L
Specific power	10.2 kW/kg	46.7 kW/kg	37.2 kW/kg
Cost	—†	—†	¢3.44/W

†Information not publicly available

to further reduce the mass and volume of the thermal management system.

The proposed MARC100 inverter is benchmarked against commercially available six-phase inverters. The specifications of the MARC100 against those by Dana TM4 and Koenigsegg are listed in Table 6.12. Although the CO200 by Dana TM4 inverter has a higher power output than the MARC100, its mass and volume are high rendering in a low power density. A close competitor to the MARC100 is the David by Koenigsegg. Both inverters showcase a peak power density of 70 kW/L. However, the David inverter is designed for a limited production hybrid supercar. As a result, it is not economically feasible for mass adoption. Whereas, the MARC100 cost is ¢3.44/W.

The power density and cost metrics of the proposed inverters are also competitive to three-phase counterparts. For example, the MARC100 is 29% cheaper than the proposed inverter in [117] at threefold the power density. Had the same design methodology for the MARC100 been used for a three-phase system, it would have used the same number of discrete SiC MOSFETs. However, repeating the steps in Section 6.2 for a three-phase inverter would have resulted in a DC-capacitor bank with a 7% higher volume. Therefore, the six-phase system does not necessarily compromise the cost nor the power density of the inverter design.

6.10 Summary

The design and development of a 100 kW SiC-based six-phase traction inverter for automotive applications was presented in this chapter. The merits and challenges associated with the six-phase two-level VSI topology were discussed and addressed in a holistic inverter design methodology. The electrical-thermal-mechanical design methodology delivered a SiC-based six-phase traction inverter prototype, named the MARC100. Figure 6.28 presents the key performance indices of the MARC100 compared to the conventional Si-based three-phase traction inverter. The MARC100 exploited the reduction in DC ripples in six-phase systems to achieve a capacitance and size reductions by 20% and 7% in the DC-bus capacitor, respectively, when compared to a three-phase counterpart of the same VA rating. The SiC discrete devices were selected in such a way that there is no increase in the device count in a six-phase inverter; instead of paralleling two devices per switch in a three-phase inverter, a single device was used for the twelve switches in six switching legs. Hence, no cost increase was incurred from the SiC discrete devices, which usually dictates the majority of the

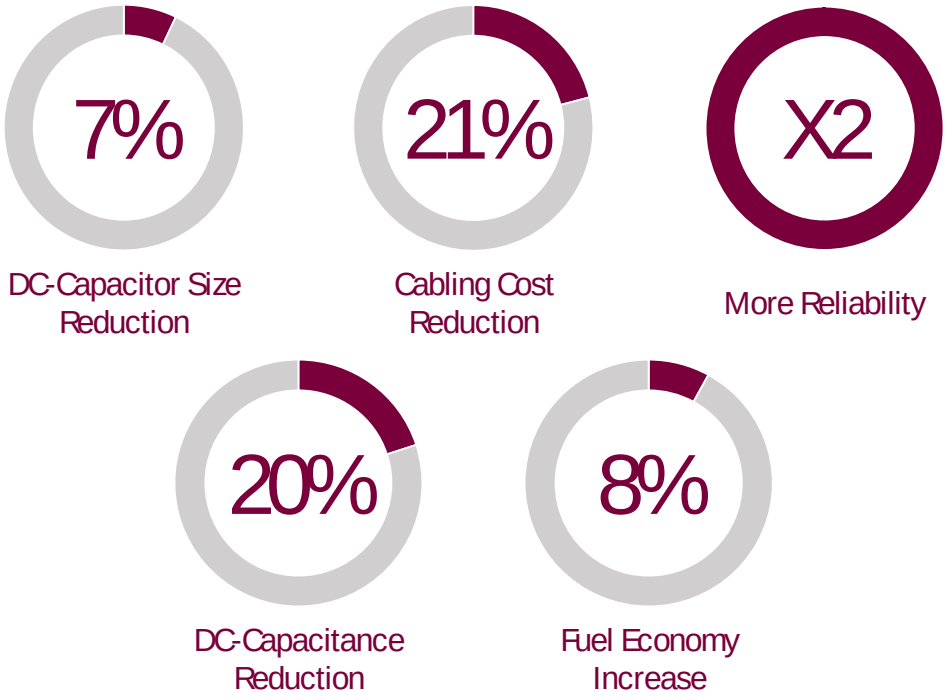


Figure 6.28: MARC100 key performance indices compared to conventional Si-based three-phase traction inverter.

overall cost of SiC-based traction inverters. Furthermore, lighter and smaller cabling for the six-phase inverter yields a cost reduction by 21%. The employment of SiC devices achieves an 8% higher fuel economy. The proposed design tackled the disadvantage of increased current sensors requirement by integrating on-board current sensor chips, rendering a compact and cost-effective design. The validation of the designed prototyped is presented in the next chapter.

Chapter 7

Experimental Validation of the 100 kW SiC-Based Six-Phase Traction Inverter

This chapter presents the experimental validation of the MARC100 inverter designed in the previous section, including, inverter assembly, preliminary testing, test setup, and high-power experimentation. Additionally, the challenges and lessons learned from the experiments are outlined to facilitate future research and development.

7.1 Manufactured Prototype and Assembly

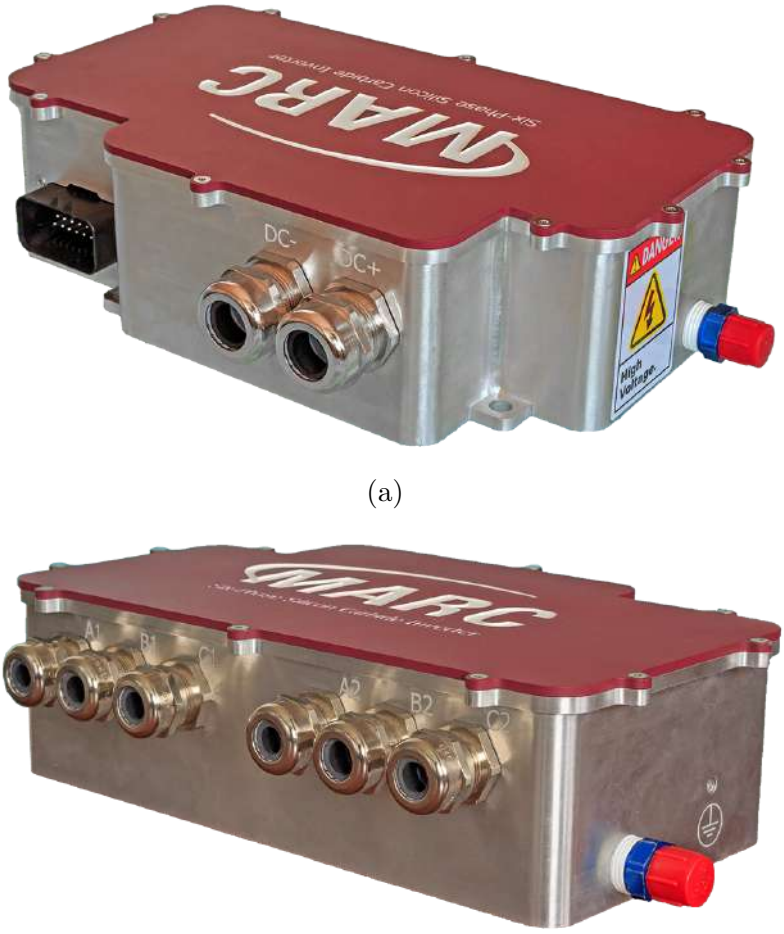
The enclosure is manufactured of 6061 Al alloy using 4-axis computer numerical control (CNC) machining. The volume and mass of the manufactured housing are 2.541 L and 3.763 kg, respectively. Figure 7.1 shows the manufactured parts of the

Figure 7.1: Manufactured inverter housing and heat sink.

inverter. All parts were manufactured with acceptable tolerances. The holes for cable glands, cooling ports, and LV connector were sized correctly, thanks to the 3D printing examination reported in Section 6.8.1. Figs. 7.2 and 7.3 present the exterior and interior of the assembled MARC100 inverter, respectively.

7.2 Preliminary Testing

Prior to high-power testing, the inverter must undergo preliminary tests to verify the correctness of the assembly and the safety of the design. Two tests are discussed in this section.



(a)

(b)

Figure 7.2: Isometric views of the assembled 3D prototype of the MARC100. (a) Front view. (b) Back view.

7.2.1 Insulation Resistance

Insulation resistance (IR), also known as Megger testing, is conducted to ensure a proper galvanic isolation of the MOSFET drains from the inverter housing via the TIM. A short-circuit from one or more MOSFETs to the housing body can lead to catastrophic failures at high voltage. The test procedure is conducted in accordance with the ANSI/NETA ATS-2017 standard [253], as detailed in Table 7.1. A LM2333

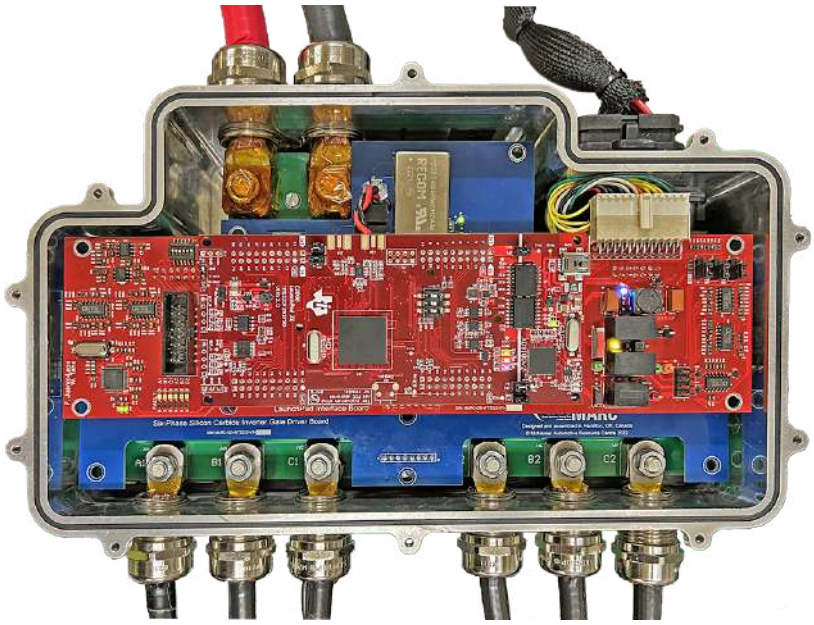


Figure 7.3: Internal assembly of the MARC100 prototype.

Table 7.1: Insulation resistance testing specifications

Cable nominal voltage rating	Minimum test voltage	Minimum IR	Test duration
600 VDC / 1,000 VAC	1,000 VDC	100 MΩ	15 s

Insu 10 insulation meter was used to carry out the IR testing, as shown in Figure 7.4. All twelve drains passed the IR testing with IRs above 500 MΩ. The IR test voltage of 1 kV constitutes a 25% safety factor above the nominal DC-bus voltage of the inverter.

7.2.2 Hydrostatic Test

The cold plate must be hermetically sealed to ensure a healthy inverter operation. Internal leakage in the inverter can cause line-to-ground or line-to-line faults. Therefore, a hydrotatic test is conducted. In a hydrostatic test, the system is pressurized

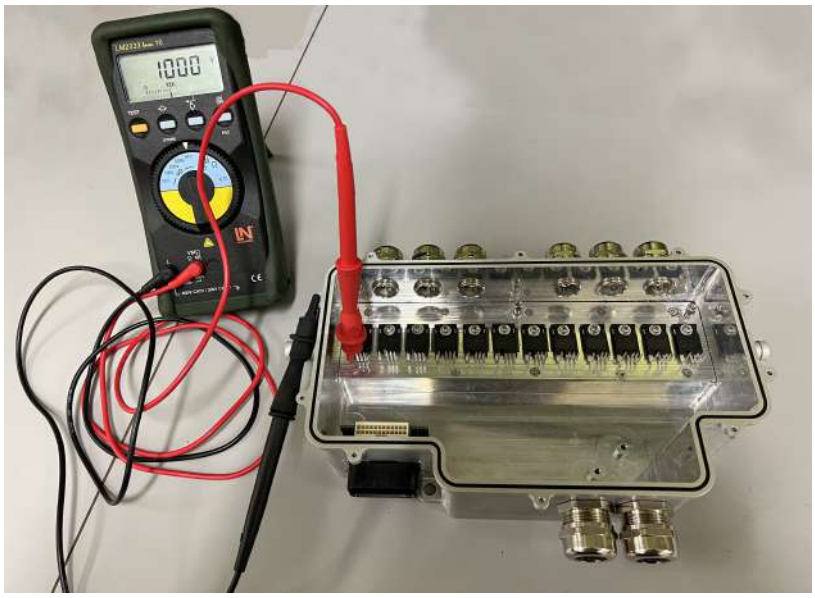


Figure 7.4: IR test at 1 kV between MOSFET drain and housing body.

with an incompressible liquid to check for leaks or permanent change in the shape. The pressure of the hydrostatic test is typically 150% of the operating pressure [254]. For liquid cooling systems in EVs, the pressure is typically 10–30 psi (70–200 kPA). This pressure is provided by a pump that circulates the liquid coolant through the various electronics, including the traction inverter, that requires liquid cooling. Figure 7.5 depicts the MARC100 inverter under a hydrostatic test at 300 kPa. A water-glycol mixture, which is the acceptable coolant in the automotive industry, was used in the test.

During the initial hydrostatic pressure test, multiple leaks were detected. After performing a root cause analysis (RCA), it was determined that two factors contributed to the leaks. Firstly, there were insufficient bolt fixtures on the heat sink's face area. Secondly, the practical guidelines for o-ring groove design were not accurately implemented [255]. To address the first issue, four additional bolts were

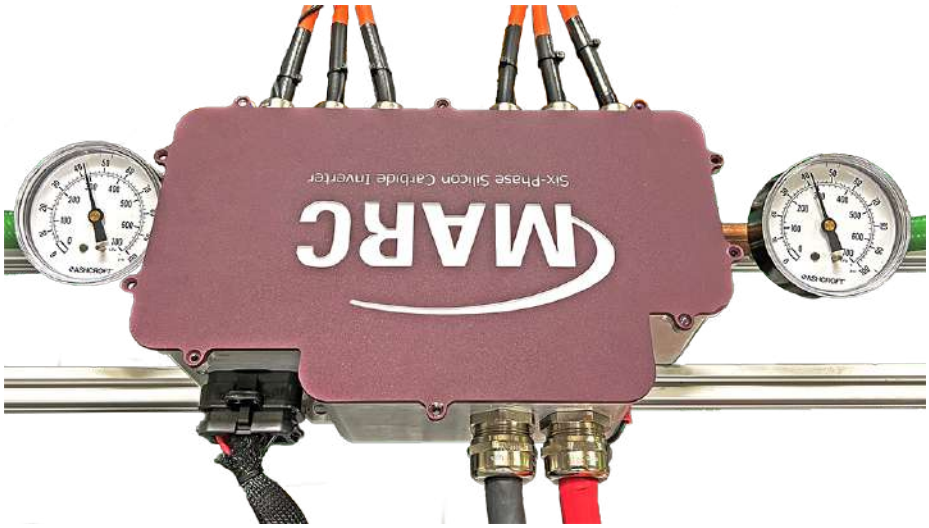


Figure 7.5: MARC100 under hydrostatic pressure for leakage test.

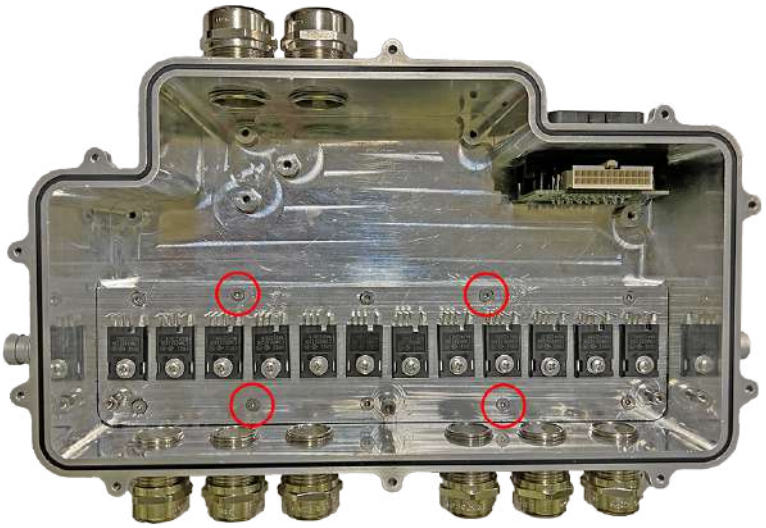


Figure 7.6: Assembled MOSFETs and heat sink showing additional bolt fixtures.

retrofitted in the heat sink and enclosure body, as shown in Figure 7.6. The second factor was more challenging to resolve. Ideally, the o-ring groove would have been re-machined, but this option would have resulted in downtime and associated costs.

Instead, an alternate solution was implemented. The groove and surface area were filled with gasket maker sealant, and the exterior edges were sealed with J-B Weld^{TM} cold weld for additional sealing.

After implementing the foregoing solutions, the hydrostatic test was conduction, and the cold plate passed the test successfully. From Figure 7.5, the pressure drop across the cold plate is below 20 kPA, consistent with the FEA analysis reported in Section 6.7.

7.3 Pre-Charge, Discharge and Safety Circuit

A pre-charge circuit between the EV battery and the inverter is needed to limit the inrush current at start-up. The same applies to a laboratory setting where the inverter is powered by a DC source.

The Pre-charge and discharge circuits are important components in an EV that manage the flow of high-voltage electricity between the battery and the traction inverter. The pre-charge circuit is used to gradually charge the DC-capacitor. This helps to avoid a sudden surge of current or voltage overshoot that can damage the DC-capacitor. On the other hand, the discharge circuit is responsible for safely discharging the DC-capacitor when the vehicle is turned off or during an emergency. The need for such circuits is also applicable in a laboratory setting, where the inverter is connected to a DC source, to avoid damaging the DC-capacitor and prevent any potential hazard. The Society of Automotive (SAE) standard J2945/1 [256] specifies the criteria that a pre-charge and discharge circuits must meet, which include:

- The pre-charge circuit must be properly sized to quickly charge the capacitor.

- The pre-charge circuit must not dissipate too much power in a fault condition.
- The charging sequence must be completed with a short period of type (within few seconds).
- The discharge circuit must bring the voltage of the traction system below 60 V in less than 5 s.
- The discharge circuit must be able to handle the maximum discharge current for 15 s.

The pre-charge(discharge) circuits are typically implemented with high-power resistors connected in series(parallel) with the DC-capacitor of the inverter to form an RC circuit, while the charging(discharging) sequences are controlled by contactors or semiconductor switches. The charging resistor, R_{ch} is sized based on the time constant of the RC circuit defined as:

$$v_{ch}(t) = V_{dc}\left(1 - e^{-t/\tau_{ch}}\right) \tag{7.3.1}$$

where v_{ch} and $\tau_{ch} = R_{ch}C_{dc}$ are the charging voltage and charging time constant, respectively. The sizing of the R_{ch} is based on a charging time of $3\tau_{ch}$, i.e., when v_{ch} reaches 95% of V_{dc}. The $3\tau_{ch}$ is set to 3 s. Accordingly, the R_{ch} and the contactor must be rated for rated charging power.

The sequence of the pre-charge circuit is controlled using two normally-open (NO) HV contactors, namely a pre-charge contactor and a main contactor. The former is sized based on the charging power ratings while the latter is sized based on the rated power of the system. The contactors are driven by LV relays whose signals are controlled by the inverter. The pre-charging sequence is as follows:

1. Pre-charge contactor is engaged to start charging.

2. When $3\tau_{ch}$ is met and $v_{ch} = 0.95V_{dc}$, the main contactor is engaged.

3. Pre-charge contactor is turned OFF.

4. Main contactor remains ON to supply power to the system.

Similarly, the discharge resistor R_{dch} is sized based on the aforementioned criteria following the RC circuit voltage:

$$v_{dch}(t) = V_{dc}\, e^{-t/\tau_{dch}} \tag{7.3.2}$$

where $v_{dch} = 60$ V and $\tau_{dch} = R_{dch}C_{dc}$ are the discharging voltage and time constant, respectively. Then, the maximum R_{dch} is found based on $\tau_{dch} \leq 5$ s.

A normally-closed (NC) contactor is connected in series with R_{dch}. The discharge contactor is only open when either the main or pre-charge contactors are engaged. Else, the system is assumed OFF and the C_{dc} is discharged. Figure 7.7 illustrates a simplified diagram of the pre-charge and discharge circuit.

In addition to pre-charge and discharge circuitry, the test setup is also facilitated with safety feature, both hardware and software, to ensure the safety of the equipment and personnel. The DC line is equipped with fuses to protect against over-current. The enclosures where the inverter, the load and the safety circuit are housed are equipped with limit switches. Such switches interrupt the main and the pre-charge signals when the enclosure is open to cut the HV supply and activate the discharge circuit. Also, an emergency stop (eSTOP) push button is installed to enable the user to shutdown the power in the case of an emergency. In software, over-current and

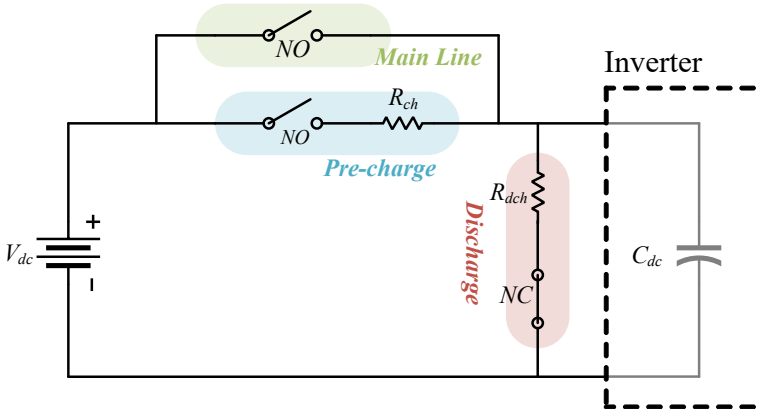


Figure 7.7: Pre-charge and discharge circuit diagram.

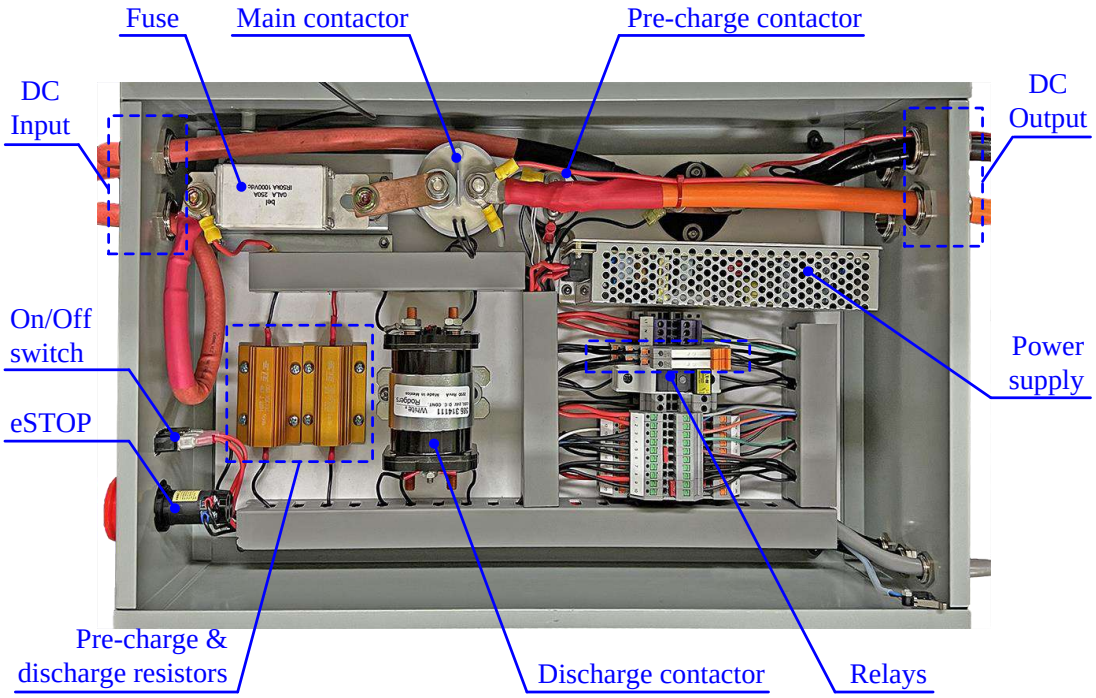


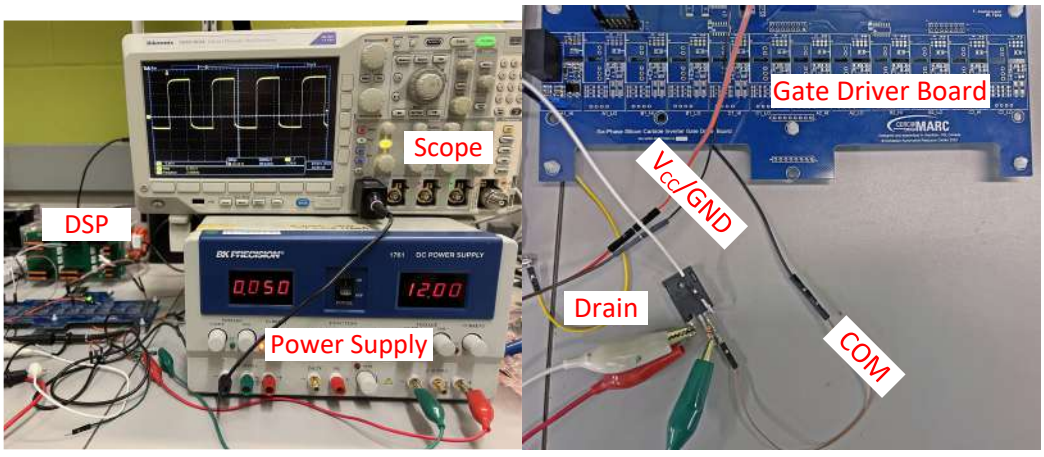
Figure 7.8: Pre-charge, discharge, and safety enclosure.

over-voltage limits are set. The controller disables the PWM operation and shuts down the system if those limits are violated. The assembled safety control panel is shown in Figure 7.8. The detailed schematic of the safety circuit can be found in Appendix A.

7.4 Gate Driver Functionality Testing

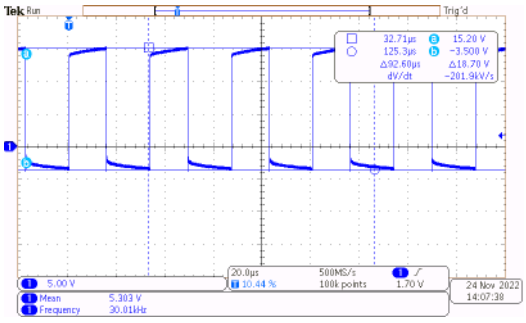
Functionality testing is conducted to the gate driver circuit before fully assembling the gate driver board. Figure 7.9 shows the experimental setup when testing the gate driver circuitry with no MOSFET connected. Only a single gate driver circuit is assembled on the board. The power supply is provided by a 12 V DC power source.

Firstly, the driver circuit is tested with no MOSFET connected to observe gate driver IC input and output signals. To enable a proper testing of the gate driver circuit in this case, the drain output is connected to COM. Otherwise, DESAT circuit will trigger a FLT signal and gate output will be pulled to V_{EE}. The $(\overline{RST}/EN)$, (RDY), and $\overline{FLT}$ were recorded as TTL high, as expected. The selected isolated DC/DC power supply outputs are 15 V and −5 V. However, the MOSFET's datasheet specifies a $V_{GS(\text{OFF})}$ of −4 V when the FET's body diode is used, which is the case in the proposed inverter design. Thus, a Zener diode circuit is used to deliver a −4 V, as shown in Figure 6.14. The current consumption by the Zener circuit was found

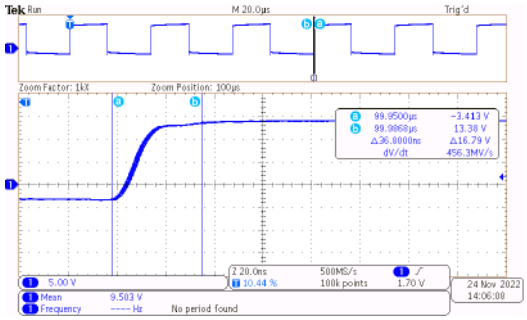


(a) (b)

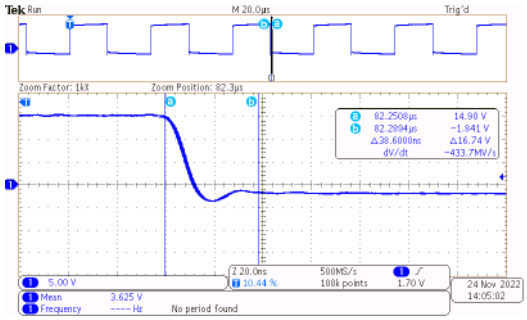
Figure 7.9: Gate driver functionality testing. (a) Setup. (b) Gate driver board.



(a) Waveform.



(b) Rising edge.

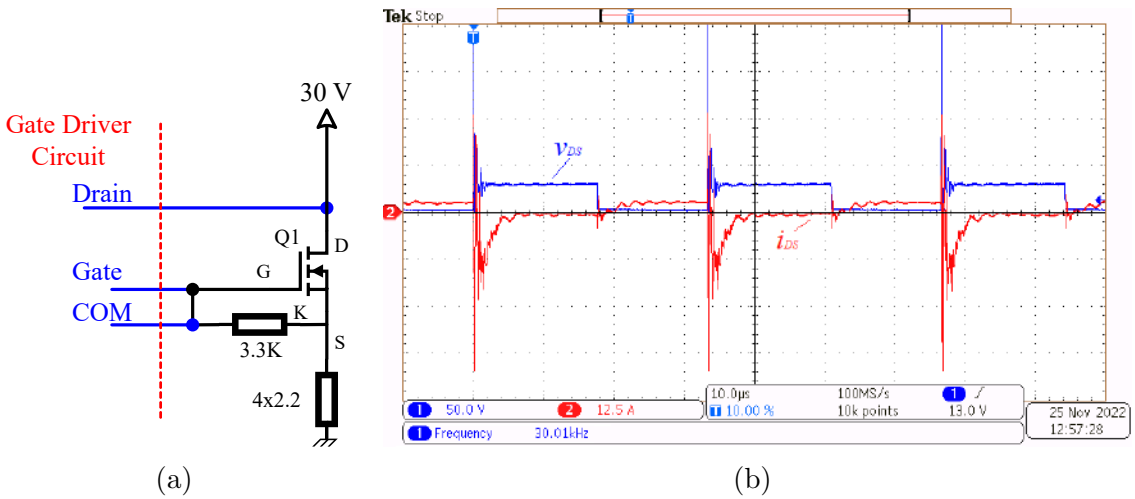


(c) Falling edge.

Figure 7.10: Gate output waveform at f_s = 30 kHz.

to be 18 mA, which is below the maximum output current of −5 V output of the DC/DC (i.e. 40 mA). Figure 7.10 demonstrates the gate output at f_s = 30 kHz. The rise and fall times are approximately 36.8 ns and 38.6 ns, respectively. The power consumption of a single gate driver circuit was recorded as 620 mW, or 7.4 W for the total twelve circuits.

Secondly, the gate driver circuit is connected a SiC MOSFET with a DC load of 8.8 Ω at 30 V as shown in Figure 7.11a. The v_{DS} and i_{DS} at 30 kHz and 50% duty cycle are shown in Figure 7.11b. Excessive noise and ringing are observed in the voltage and current waveforms. This is due to the improper wiring of the circuit shown in Figure 7.9b that uses unshielded and long jumper wires that introduce self and mutual stray inductances. However, since the objective of this test is to establish



(a) (b)

Figure 7.11: Loaded gate driver circuit functionality test at f_s = 30 kHz. (a) Test circuit. (b) Test waveforms at 50% duty cycle.

the working conditions of the gate driver circuit, the functionality test is deemed successful.

7.5 High Voltage Testing

Figure 7.12 shows the HV experimental setup for the MARC100 connected to a passive 100 A, 1 mH inductive load. As discussed in Section 5.5, the load can be configured as symmetric or asymmetric. The DC-bus voltage is supplied by a 20 kW, 2 kV Keysight RP7973A regenerative power system. The MARC100 and the Si-based six-phase inverter used in Section 5.5 are housed in a finger-safe transparent enclosure, along with cooling instruments, external sensors, and probes. Provisions for the back-to-back connection of both inverters are incorporated into the setup for future work. The complete computer aided design (CAD) of the setup is included in Appendix B. The DSP controller of the MARC100 manages the setup operation. The main and pre-charge contractors are controlled using the RLY1 and RLY2 pins

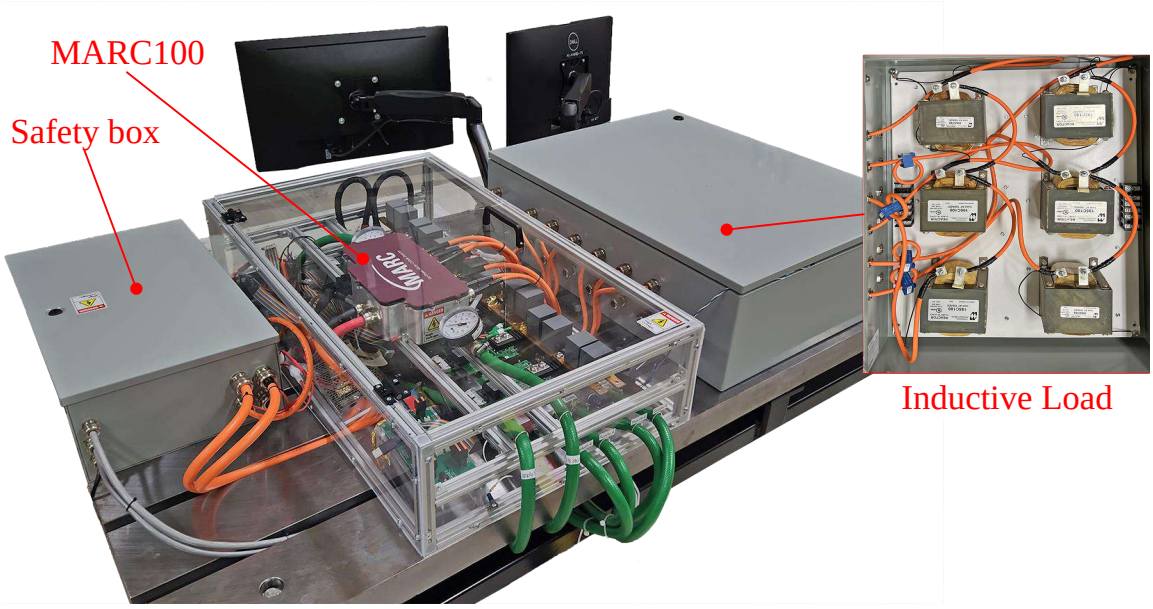


Figure 7.12: High voltage experimental setup for the MARC100.

available at the LV connector of the MARC100, respectively (see Appendices A and C). Software-based safety protocols are programmed in the MARC100 to interrupt the HV power supply in the case of gate driver faults, over-voltage, or over-current.

7.5.1 Double Pulse Test

The double pulse test (DPT) is a widely used method to evaluate the switching characteristics of a power transistor. In this test, two V_{GS} pulses with a short time delay are applied to the device under test (DUT). Figure 7.13 depicts the circuit diagram of the DPT. The first pulse is used to turn ON the device and reach to the test current, while the second pulse is used to evaluate the performance of the DUT during conduction. By measuring the voltage and current waveforms during the second pulse, important parameters such as the turn-ON time, turn-OFF time, voltage overshoot, and switching losses can be calculated. However, to maximize the

power density of the MARC100, provisions to measure the device current were not incorporated. So a typical DPT measuring switching losses cannot be conducted. Nevertheless, measurement of v_{DS} is still attainable, which is important to evaluate the voltage overshoot.

The duration of the first pulse, τ_{p1} is chosen based on the desired test current, given as:

$$\tau_{p1} = L \frac{I_{test}}{V_{dc}} \tag{7.5.1}$$

where L is the load inductor and I_{test} is the test current, which is set equal to the rated current of the inverter. Between the two pulses, a short break period, τ_b is given, where the DUT is turned OFF and the current flows through the freewheeling or body diode, as shown in Figure 7.13. The duration of τ_b is chosen long enough such that the switching transients have decayed before starting the second pulse. With the second pulse, τ_{p2}, the DUT is again turned ON. The duration of τ_{p2} is carefully chosen such that the current does not rise to an impermissible high value.

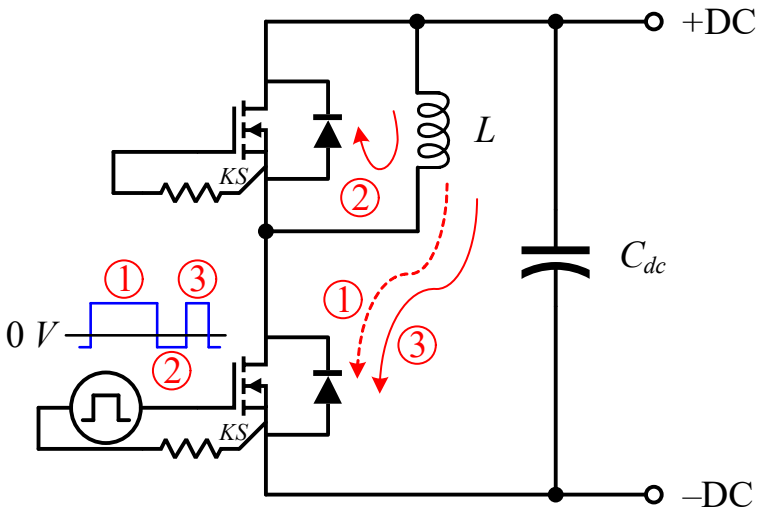


Figure 7.13: Circuit diagram of the DPT.

Before performing the DPT, the circuit components must be properly designed to conduct a successful test. As given in (7.5.1), the duration of τ_{p1} is a function of the load inductor. A high value of L leads to a slower increase in the current, calling for a longer τ_{p1}. However, the duration of τ_{p1} should not exceed 100 μs to avoid self heating of the DUT [257]. On the other hand, L should be high enough to minimize the current drop, ΔI during the break period owing to the parasitic resistance of the inductor and the forward voltage of the body diode. Therefore, the lower and upper boundaries of L are defined as [257]:

$$\frac{-R_p \tau_b}{\ln\left(\frac{\Delta I}{I_{test}+v_F/R_p}+1\right)} \leq L \leq \tau_{p1}\,\frac{V_{dc}}{I_{test}} \tag{7.5.2}$$

where R_p is the parasitic resistance of the load inductor and v_F is the forward voltage drop of the body diode, which can be found in the datasheet of the DUT. Note that ΔI is typically chosen between 1% and 5% of I_{test}. To meet the constraint in (7.5.2), three of the 1 mH load inductors are used in parallel.

The DC-capacitor used in the DPT should be sufficiently large to store enough energy to maintain a constant voltage across the DUT throughout the DPT. During the DPT, the stored electrical energy in the capacitor is converted into magnetic energy in the load inductor. The minimum capacitance can be obtained based on the energy balance in both components and the allowable voltage drop, ΔV_{dc}. Thus, the minimum capacitance is defined as [257]:

$$C_{dc} \geq \frac{L I_{test}^2}{2V_{dc}\Delta V_{dc} - \Delta V_{dc}} \tag{7.5.3}$$

Since the DC-capacitor of the MARC100 was optimized to yield the maximum power

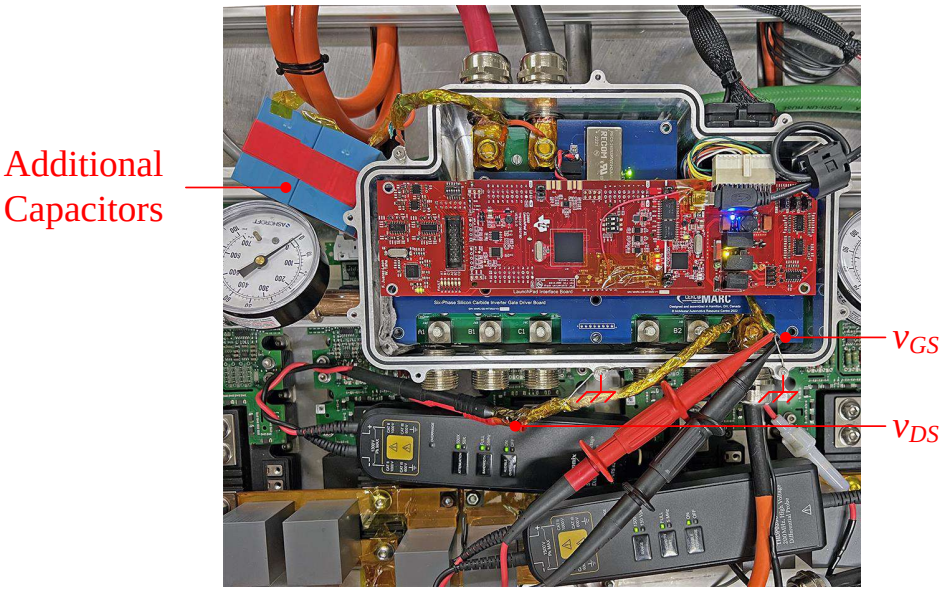


Figure 7.14: Double pulse test setup on phase C2.

density, as discussed in Section 6.2, its capacitance is insufficient to conduct the DPT at the rated voltage and current. Therefore, additional film capacitors with a capacitance of 120 μF are added to the DC-bus. The total DC-bus capacitance is, therefore, 172 μF, resulting in ΔV_{dc} = 10 V, which is acceptable for conducting the DPT.

Figure 7.14 depicts the experimental setup for the DPT. The measurement of v_{DS} and v_{GS} are obtained via soldering twister cable pair on the power and gate boards, respectively. The twister pair is shielded with an aluminum shield and drain wire that is connected to the inverter chassis, to improve the noise immunity. The voltages are measured using Tektronix P5200A 50 MHz isolated differential probes. The load current is measured using a Tektronix TRCP0600 Rogowski coil. The measurements are recorded on a Tektronics MDO3024 200 MHz, 2.5 Gs/s oscilloscope.

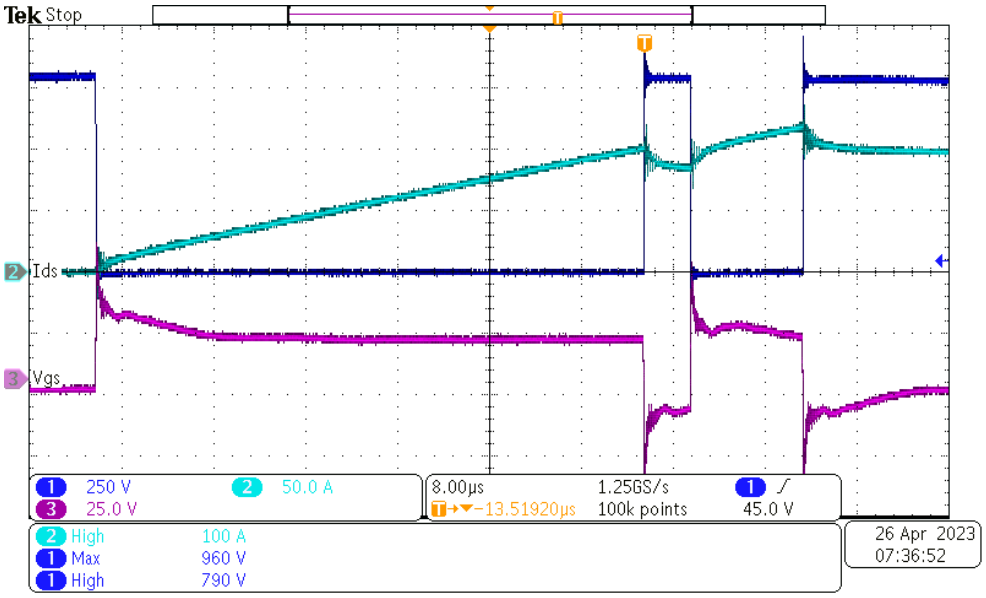
The DPT is performed first for phase C2 as per the parameters given in Table 7.2.

Table 7.2: Double pulse test parameters

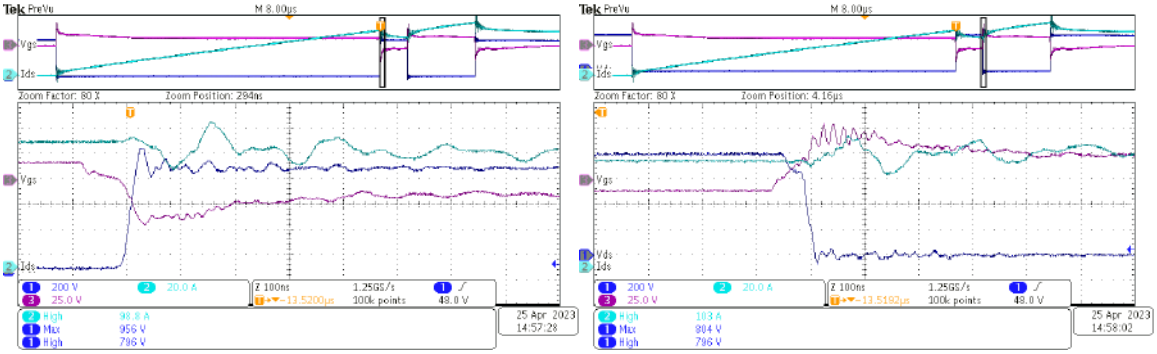
Parameter	**Symbol**	**Value**	**Unit**
DC-bus voltage	V_{dc}	800	V
Test current	I_{test}	100	A
Load inductor	L	333	mH
DC-bus capacitance	C_{dc}	172	μF
First pulse duration	τ_{p1}	40	μs
Second pulse duration	τ_{p2}	10	μs
Break pulse duration	τ_b	4	μs

phase C2 is the farthest from the top row capacitors (see Figure 6.9), thus it is expected to yield the worst-case scenario. Figure 7.15 shows the DPT results on phase C2. The recorded rise and fall times on of v_{DS} are 48.1 ns and 20.4 ns, respectively. The percentage overshoot of v_{DS} at the first turn-OFF instant is 19.8%.

The DPT is then performed on all six phases to confirm their proper operation and to compare their performance with respect to each others. Figure 7.16 presents the first turn-OFF instant of v_{DS} under the same DPT conditions in Table 7.2. The maximum overshoot voltage in Figure 7.16 matches the theoretically calculated one in (6.3.1), thus confirming the FEA analysis of the commutation loop inductance in Section 6.3.2. The average percentage overshoot in v_{DS} is 23.1% with a standard deviation of 1.5%. A similar standard deviation is also observed in the rise. Hence, a very uniform performance on all phases is demonstrated. As expected, a slightly higher ringing on phase C2 is observed when compared to the other phases. After verifying a safe voltage overshoot performance at rated conditions, six-phase VSI operation is tested next.



(a) Full waveform.



(b) Turn-OFF. (c) Turn-ON.

Figure 7.15: DPT on phase C2 of the MARC100 as per the parameters in Table 7.2.

7.5.2 Six-Phase VSI Operation

For six-phase VSI operation, the inductive load is star-connected with two isolated neutrals. A 30 kHz switching frequency is utilized with a 2 μs of dead-time. The inverter is operated in open-loop mode with SPWM at a f_1 = 200 Hz. It is important to note that high base frequencies are necessary to increase the load impedance (ωL), which helps to maintain the current within a safe limit.

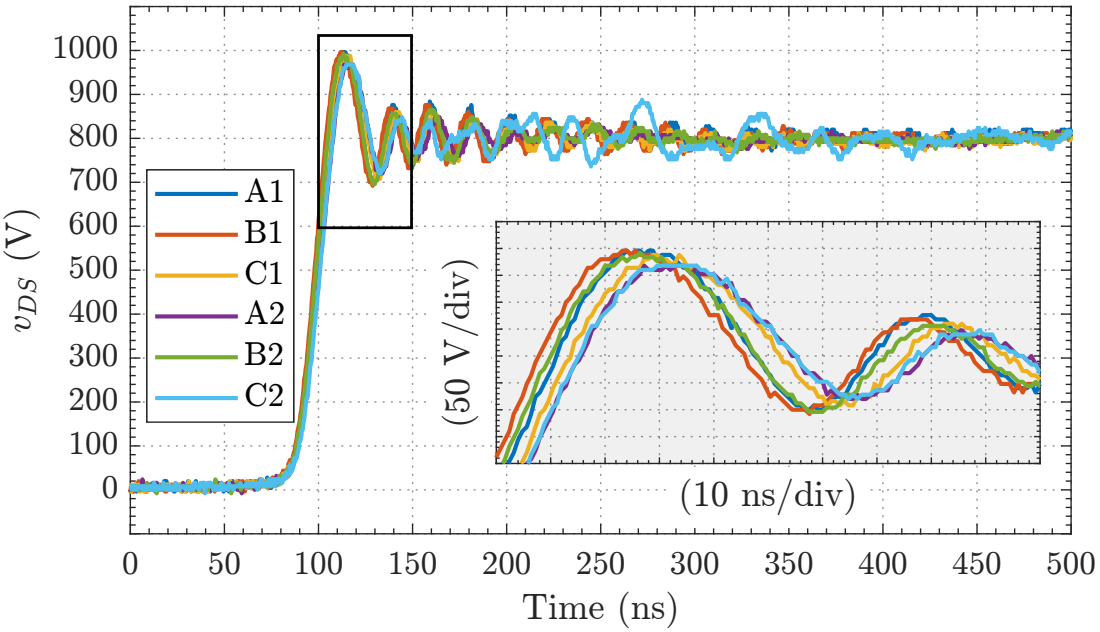


Figure 7.16: v_{DS} waveform in the DPT at the first turn-OFF instant on all phases of the MARC100 at 100 A load current.

Figures 7.17 and 7.18 illustrate the steady-state performance of the six-phase VSI with a symmetric load at M = 0.6 and V_{dc} of 400 V and 800 V, respectively. These figures show that there is a 14% current unbalance between the two sets of three-phases. This unbalance is expected because of the 15% tolerance on the used load inductors. Assuming a balanced load in each three-phase set, the output power in Figures 7.17 and 7.18 is 11.4 kVA and 64.3 kVA, respectively. The harmonic spectra of v_{AB1} and i_{A1} in Figures 7.17 and 7.18 are depicted in Figures 7.19 and 7.20, respectively. At V_{dc} = 800 V, the line-to-line voltage THD is 138%, while the current THD is 3%. The relatively low THD values is attributed to the high modulation frequency, m_f applied in these tests. In a perfectly balanced six-phase system with two isolated neutrals, i_{A1} and v_{AB1} do not contain any triplen harmonics. However, the 3rd harmonic appears in v_{AB1} and i_{A1} in Figures 7.19 and 7.20, albeit with minimal

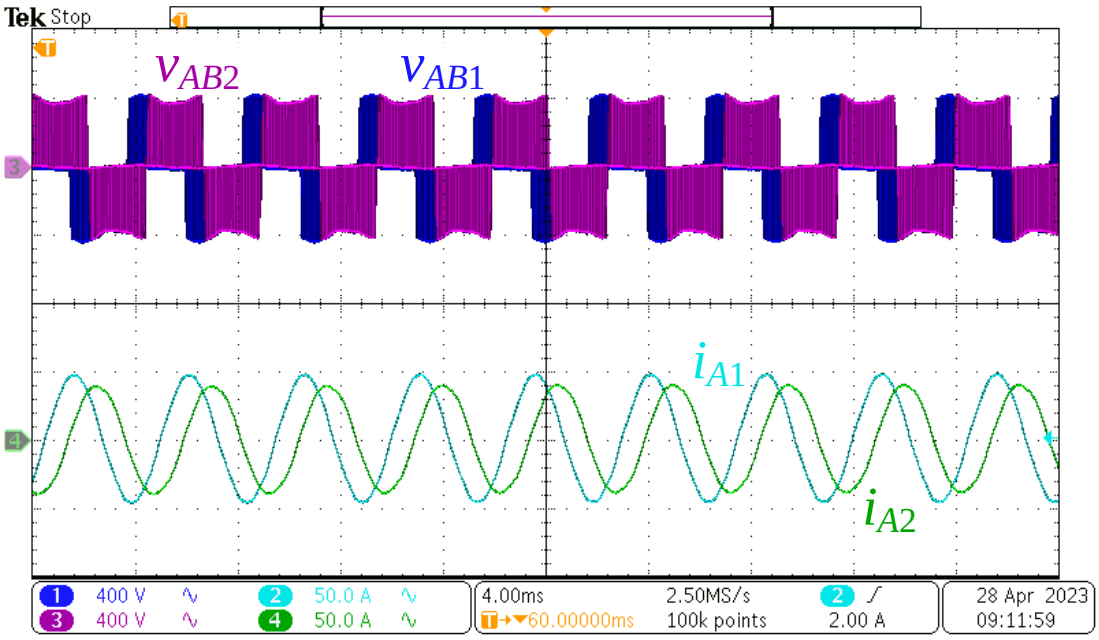


Figure 7.17: Experimental six-phase VSI steady-state performance showing line-to-line voltages and phase currents at V_{dc} = 400 V, S_{out} = 11.4 kVA, f_1 = 200 Hz, f_s = 30 kHz, M = 0.6.

magnitudes of 4% and 1%, respectively, in the case of V_{dc} = 800 V.

Lastly, the dynamic performance of the six-phase VSI is tested at V_{dc} = 800 V. Figure 7.21 presents the voltage and current waveforms under a step change in M from 0.255 to 0.55. An adequate and stable performance is demonstrated.

7.6 Lessons Learned

During prototype assembly and experimentation, several lessons were learned that can facilitate future work. These lessons are as follows:

1. As discussed in Section 7.2.2, the o-ring design must be carefully chosen to withstand the rated pressure, thus avoiding leaks. Also, instead of having the

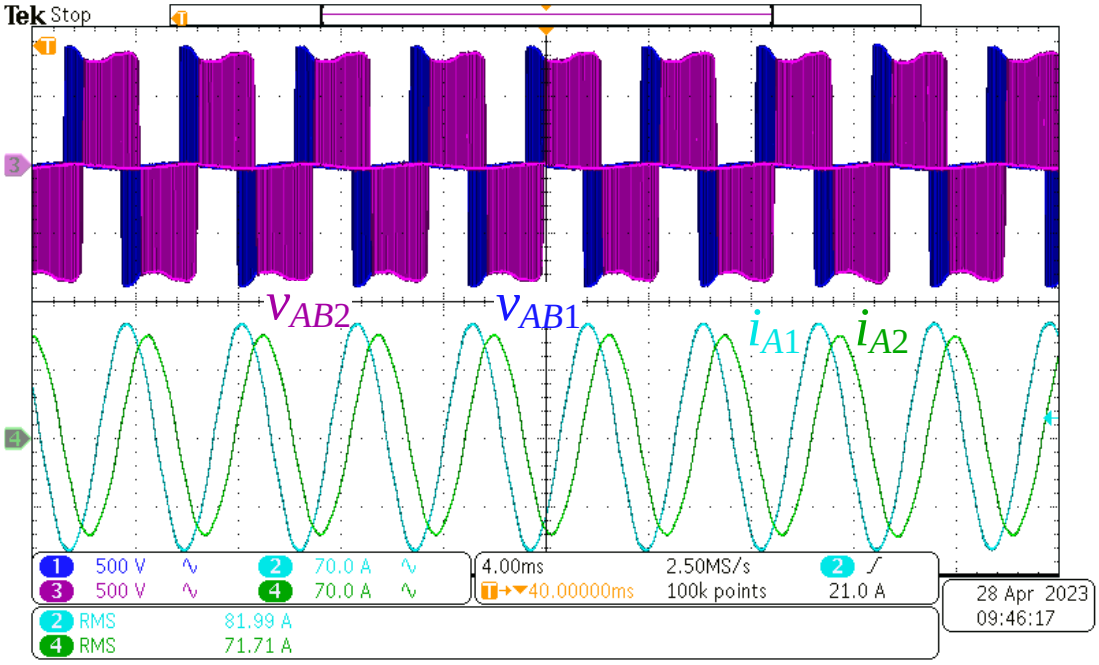


Figure 7.18: Experimental six-phase VSI steady-state performance showing line-to-line voltages and phase currents at V_{dc} = 800 V, S_{out} = 64.3 kVA, f_1 = 200 Hz, f_s = 30 kHz, M = 0.6.

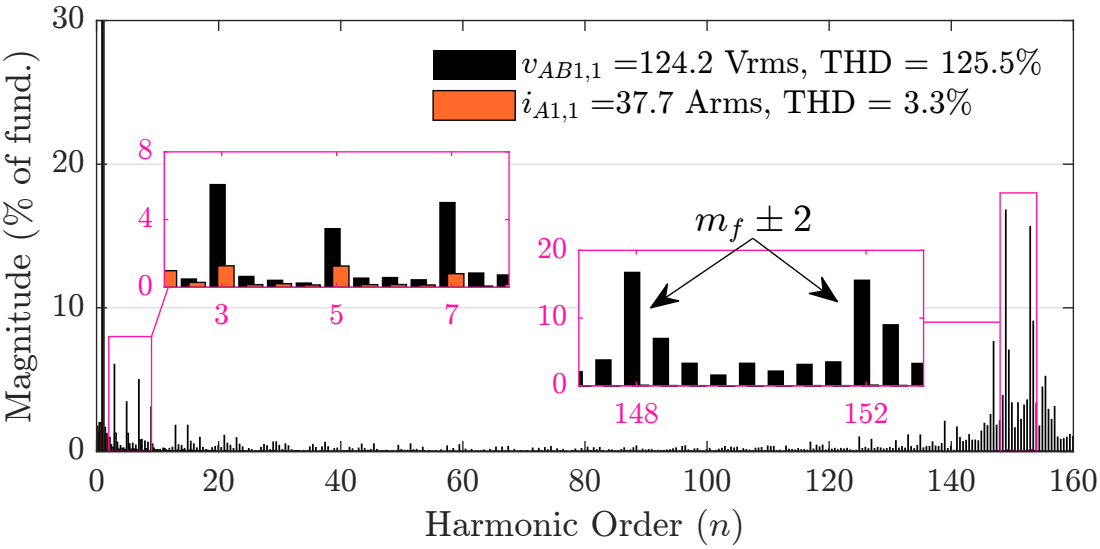


Figure 7.19: Experimental harmonic spectra of v_{AB1} and i_{A1} waveforms in Figure 7.17.

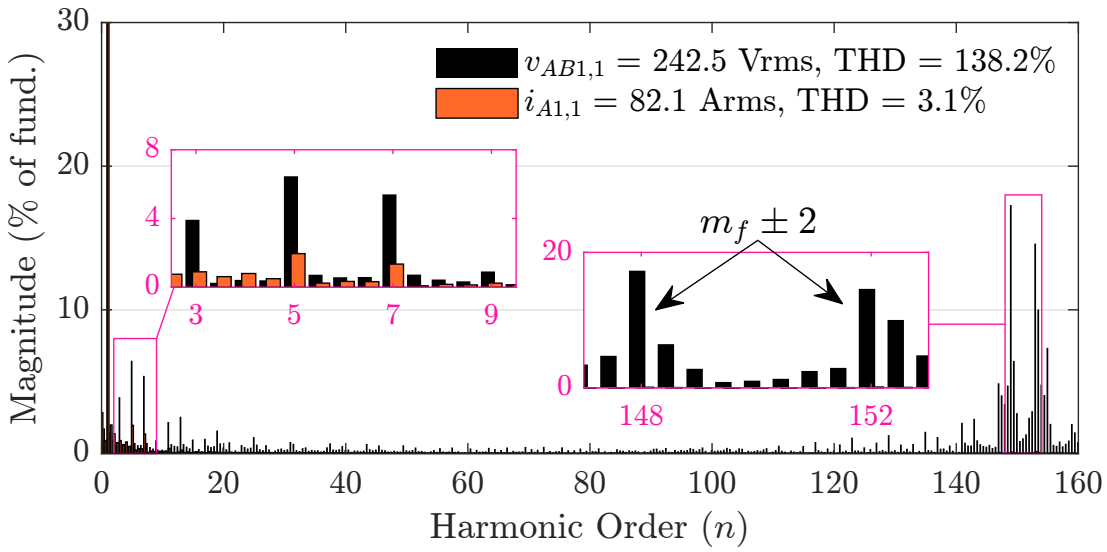


Figure 7.20: Experimental harmonic spectra of v_{AB1} and i_{A1} waveforms in Figure 7.18

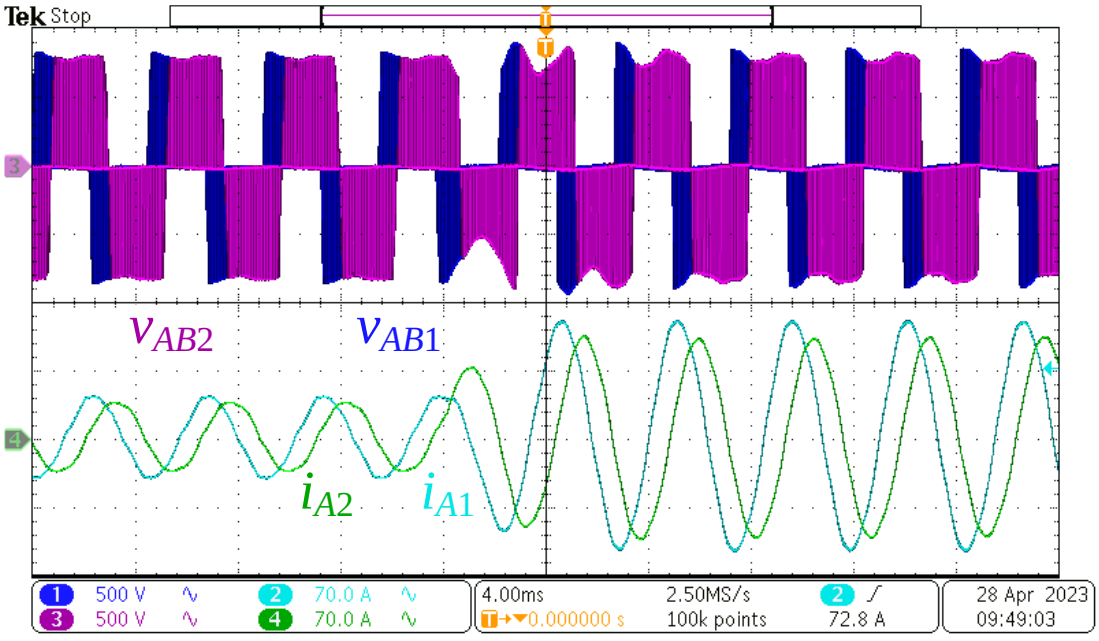


Figure 7.21: Experimental six-phase VSI dynamic performance under a step change in M from 0.255 to 0.55 showing line-to-line voltages and phase currents at V_{dc} = 800 V, f_1 = 200 Hz, f_s = 30 kHz.

removable part of the heat sink inside the mechanical housing, it could be made external. This would improve the inverter servicing process and ensure any potential leak is outside the housing, avoiding a short circuit.

2. The pad material of the TIM and its thickness must be carefully selected for the inverter's rated DC-bus voltage to avoid any short circuit between the MOSFET drain and the inverter housing. During testing, the TIM silicon pads with a thickness of 1 mm were replaced with 2 mm pads after a piercing was observed in the former, which caused a MOSFET failure.

3. A bug in the VSI program caused the application of PWM overlap time, instead of dead-time, to the PWM signals of the same phase leg. This resulted in a shoot through issue that caused some of the MOSFETs to fail. The UCC21750-Q1 [244] gate driver IC utilized in the design includes a PWM interlock feature that could have prevented phase shoot through events. However, this feature was not utilized in the gate driver PCB. To avoid similar issues in the future, it is recommended to incorporate the PWM interlock feature in the gate driver design.

4. After repetitive installation and dismantling of the power PCB, the bolt/nut fixture wore away the surface material of the PCB. This led to arcing between the power PCB's DC-plane and the earthed inverter housing. Therefore, sufficient clearance around the bolt fixture holes on the power PCB, which takes into account the outer diameter of such fixtures, must be made to avoid arcing or short circuiting to earth. The arcing issue was resolved by applying a layer of silicone conformal coating on the PCB and the inverter housing's internal

walls.

5. Operating at 800 V generates excessive noise that can disrupt communication with the control board and lead to false faults on the gate driver. This issue is attributed to the high dv/dt on the SiC MOSFETs operating in hard switching mode. To address this problem, deliberate EMI mitigation measures are required. Incorporating a 1 mm-thick conductive metallic sheet between the power and gate driver PCBs or between the gate driver and control PCBs is recommended to enhance the isolation between HV and LV circuitry. It is essential to earth the sheet by directly bonding it with the inverter housing.

7.7 Summary

The validation of the MARC100—a 100 kW SiC-based six-phase traction—was demonstrated in this chapter. Firstly, the manufacturing and assembly process are discussed. Secondly, the testing methodology for some of the preliminary and functionality tests were discussed, and their results were presented. The gate driver functionality test demonstrated a healthy performance in line with the design specifications outlined in the previous chapter. Thirdly, high power experimentation, including a double pulse test and six-phase inverter operation was showcased. A high degree of consistency in the double pulse test across all phases demonstrated the uniformity of the design. The MARC100 was tested to 60% of its rated power, demonstrating a healthy and stable performance. Lastly, the main challenges and lessons learned were outlined, which can be used to guide future improvements. The proposed MARC100 inverter features a compact design with a peak power density

of 70 kW. Overall, the results of this chapter validate the design and performance of the MARC100, showing that it is a viable solution for high-power applications in electrified transportation.

Chapter 8

Control Aspects of Six-Phase Electric Motor Drives

Dual three-phase (DTP) PMSM drives have been drawing the attention of researchers and engineers alike. PMSMs are known for their high efficiency, ruggedness, and high power density. DTP-PMSMs offer multitude of advantages when compared to their single three-phase counterparts, namely halved per-phase current handling, improved fault tolerance capability, and lower torque pulsations [29]. Their utilization in different applications including automotive [29] and aerospace [258] has been extensively investigated.

As mentioned in Section 6.1, DTP-PMSMs exist in three distinct winding configurations, depending on the separation angle of the back electromotive force (EMF) between the two sets of three phases [30, 36, 233, 259]: split, symmetrical, and asymmetrical. The DTP terminology is mostly associated with asymmetric configuration with two isolated neutrals. Owing to the configuration comparison in Table 6.1, this chapter focuses on the asymmetric motor configuration.

The machine can be modeled using the VSD or double d–q, as explained in Section 2.1. For the VSD merits summarized in Table 2.2, the scope of this chapter is limited to VSD control techniques of DTP-PMSM. The torque-producing components in VSD are mapped into the α–β subspace, the harmonic compo nents are mapped into the x–y subspace, and the zero-sequence components are mapped into the 0_1–0_2 subspace. When the six-phase windings have two isolated neutrals, the zero-sequence components are nullified. The suppression of harmonic components is desirable since they contribute to losses and reduce the maximum attainable power of the motor.

Various control strategies have been proposed for the suppression of xy-currents, including the quasi-proportional resonance controller (QPR) [260], offset-free predictive current control based on virtual vectors [261], sliding mode controller (SMC) [262], bi-subspace predictive current control strategy based on non-virtual vectors [263], and model predictive direct torque control [264]. These methods provide separate control to α–β subspace and x–y subspace to avoid current harmonics. Digital SMC with disturbance rejection was proposed in [265]. Additionally, other methods such as multistage predictive current control based on Virtual Vectors [266] and space vector optimized predictive control [267] have achieved satisfactory results with respect to the xy-current suppression problem.

However, there are some inadequacies in the aforementioned methods. For instance, the QPR method presented in [260] is effective in reducing the harmonics on xy-currents, but it cannot filter the fundamental frequency component. Moreover, offset-free predictive current control based on virtual vectors, model predictive direct torque control method, and space vector optimized predictive control method are

effective in limiting xy current, but these methods require complex designs and calculations. Besides, the xy-current can be controlled in the stationary, synchronous, or asynchronous reference frames. The digital SMC controller in [265] was only implemented in the synchronous frame. The performance of the suggested control techniques in the different control reference frame was not investigated [57]. As such, this chapter focuses on analyzing the xy-current control using simple and well-known controllers, yet in various modeling frames. More specifically, three controllers are considered, namely PI, PR, and SMC, in the stationary, synchronous, and asynchronous reference frames. [268]

Beyond base speed, PMSM operation requires a flux-weakening (FW) controller to prevent an increase in the EMF that may saturate current controllers, potentially leading to an unstable system [61]. One of the earliest and widely used FW control techniques is voltage regulation (VR-FW), which seamlessly integrates into the field oriented control (FOC) and is applicable in both linear and overmodulation (OVM) PWM regions [269].

While the VR-FW control strategy is well established for three-phase PMSM drives [270], its performance for six-phase drives controlled using VSD modeling is yet to be thoroughly investigated. Only a few studies are available in literature on this topic. Early research extended the VR-FW control of conventional three-phase drives to DTP-PMSM. For example, in [271], a split DTP-PMSM was treated as two separate three-phase machines, where two VR-FW controllers were implemented using different torque split ratios between the two three-phase sets. However, the use of two controllers aggravates the tuning effort as the FW currents can be unbalanced [272]. In [273], a switching function between zero i_d vector control and FW control

was suggested for asymmetrical DTP-PMSM. In [59], a VSD-based VR-FW control for asymmetrical DTP-PMSM drives was proposed, where a single PI controller for FW control was employed in the torque-producing subspace of the VSD. Although a superior, sixth-harmonic-free FW current was reported, the testing was limited to 40% above base speed.

In the deep FW region, the static-gain of the voltage control loop changes dramatically due to the nonlinear behavior of the dynamics that relate the current vector to the voltage amplitude, under maximum current and voltage constraints [274–276]. This, in turn, reduces the stability margin of the control loop as speed increases [277]. Therefore, in addition to delicate tuning of the PI controller of the VR-FW control, the proportional gain should also be decreased to counteract the increase in the static-gain of the loop [278]. Gain adaptation has been proposed in [116, 274–276, 279], but limited to three-phase drives. This chapter proposes an adaptive VR-FW controller for DTP-PMSM drives to address this issue.

In addition to the field weakening controls for PMSM drive operation above the base speed, OVM techniques are also employed to mitigate the chopping effect of the VSI topology. OVM can increase the maximum output torque capability, the maximum speed limit, and improve the utilization of the DC-link voltage [280–283]. Although OVM methods have been studied for two-level three-phase VSIs, research on OVM for DTP-PMSMs supplied by six-phase VSIs is a new challenge. The implementation of OVM for DTP-PMSM drives can be divided into two categories: two three-phase modulators and one six-phase modulator.

Six-phase modulation methods are mainly based on SVM techniques [284]. Using a 6×6 orthonormal transformation, the six-dimensional (6-D) space of the DTP-PMSM

can be transformed into three 2-D orthogonal subspaces, namely α–β, x–y, and o_1–o_2 [285–287]. In linear modulation methods, no average voltage is applied in the x–y subspace, but harmonic voltage is added in the x–y subspace for OVM. Conventional six-dimensional SVM techniques are complex and suffer from a circulating current issue. In comparison, two three-phase modulator methods are easier to implement, and therefore, they are studied in this thesis.

When using two three-phase modulators for DTP-PMSM drives, the conventional OVM methods of the two-level three-phase VSI are also applicable. The conventional OVM methods are minimum phase error (MPE), minimum distance error (MDE), keeping switching state (KSS), and minimum magnitude error (MME) [288–291]. MPE has a limited modulation index range and cannot achieve six-step operation [292]. Dong-Choon Lee *et al.* proposed a modified method to solve such problems [293]. Moreover, a sector-based OVM method was proposed based on Fourier analysis to extend the modulation to OVM [294]. Each method has its advantages, and some of them were assessed in a generalized vector form. However, a single and comprehensive study considering all the methods to establish a fair comparison is lacking. Furthermore, the implementation of these methods based on the generalized vector form is only partially covered in the literature. Therefore, this chapter presents a comparative analysis of OVM methods based on four segmented formulas, and a modified MPE (MMPE) is proposed for easy implementation with better performance in terms of fundamental component and harmonic content.

The remainder of this chapter is organized as follows. DTP-PMSM modeling using the VSD approach and FOC is presented in Section 8.1. The xy-current control using different controllers is investigated in Section 8.2. The adaptive VR-FW control

control for DTP-PMSM drives is proposed in Section 8.3. Section 8.4 investigates the three-phase-based OVM techniques and their application to DTP-PMSM drives. Finally, Section 8.5 outlines the concluding remarks of this chapter.

8.1 Motor Modeling and Control

The six-phase IPMSM can be modeled in the synchronous dq-frame as:

$$\mathbf{v_s} = \mathbf{R_s i_s} + \mathbf{L_s}\frac{d\mathbf{i_s}}{dt} - \omega_r \mathbf{J L_s i_s} + \omega_r \mathbf{J}\boldsymbol{\psi_r} \tag{8.1.1a}$$

$$\boldsymbol{\psi_s} = \mathbf{L_s i_s} + \mathbf{J}\boldsymbol{\psi_{PM}} \tag{8.1.1b}$$

$$\mathbf{J} = \begin{bmatrix} 0 & -1 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & -1 & 0 \end{bmatrix}, \tag{8.1.1c}$$

where $\mathbf{R_s}$ is the diagonal stator resistance matrix and

$$\mathbf{L_s} = \begin{bmatrix} L_d & 0 & 0 & 0 \\ 0 & L_q & 0 & 0 \\ 0 & 0 & L_s & 0 \\ 0 & 0 & 0 & L_s \end{bmatrix}, \tag{8.1.2}$$

where $L_{d,q}$ are the inductances in the dq-frame and L_s is the leakage inductance in the x–y frame. $\mathbf{v_s}, \mathbf{i_s}$, and $\boldsymbol{\psi_s}$ are the voltage, current, and flux linkage vectors, respectively, in the form of $\mathbf{f_s} = \begin{bmatrix} f_d & f_q & f_x & f_y \end{bmatrix}^T$. The flux linkage at no load condition is given by $\boldsymbol{\psi_r} = \begin{bmatrix} \psi_{PM} & 0 & 0 & 0 \end{bmatrix}^T$.

The electromagnetic torque of a DTP-PMSM machine is given as:

$$T_e = \frac{3}{2}N_p\Big[\psi_r i_q + (L_d - L_q)i_d i_q\Big] \tag{8.1.3}$$

where N_p is the number of pole pairs and p is the differential (d/dt) operator.

Using the VSD transformation, it is possible to define a FOC scheme to control the DTP-PMSM. Figure 8.1 illustrates the VSD-based FOC scheme employed in this chapter with double three-phase space vector modulations (SVMs). In this case, the advantages of the VSD transformation allow defining a FW control just as in conventional three-phase motors. However, this assumes that the xy components are properly regulated/minimized. For speeds below base speed (i.e. $\omega_r \leq \omega_b$), the outer speed loop provides the reference q-axis current, i^*_{q0}, which in turn is used to find the

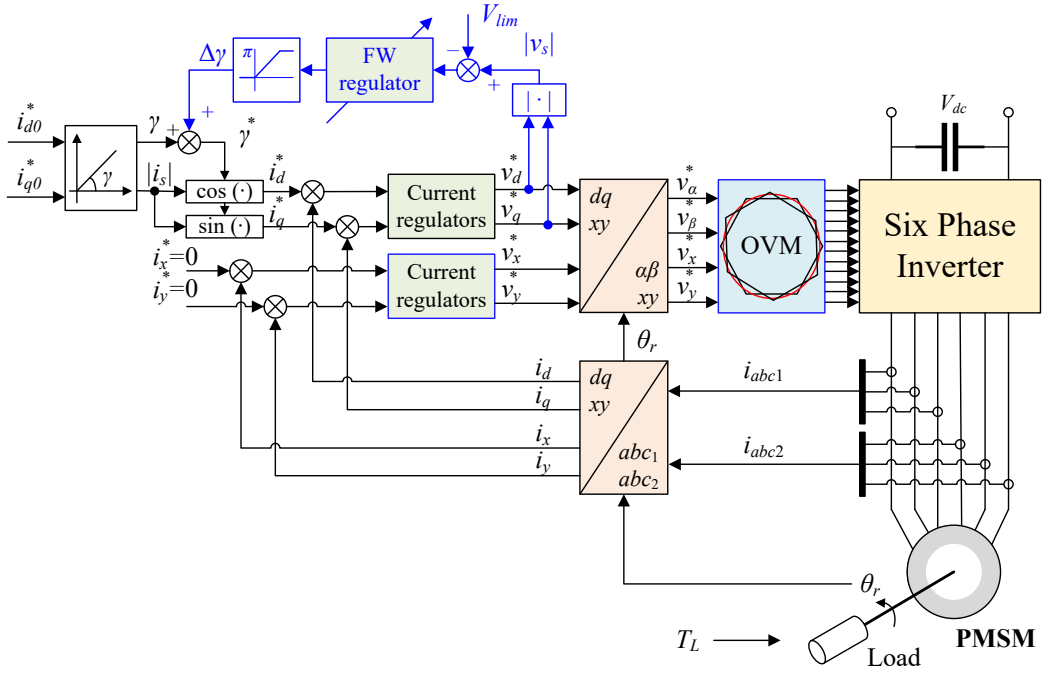


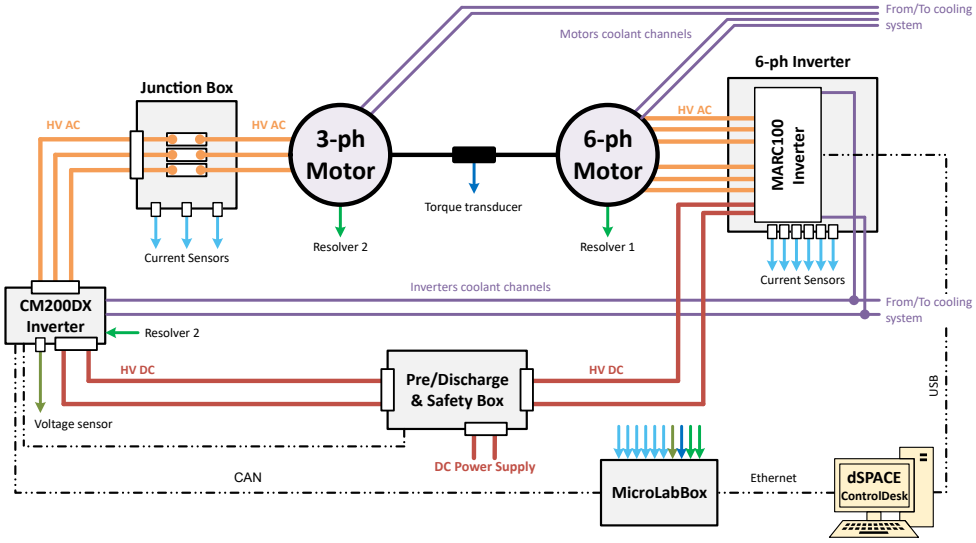
Figure 8.1: VSI-fed DTP-PMSM drive in the FOC scheme using VSD transformation.

reference d-axis current, i_{d0}^{*} using the MTPA control.

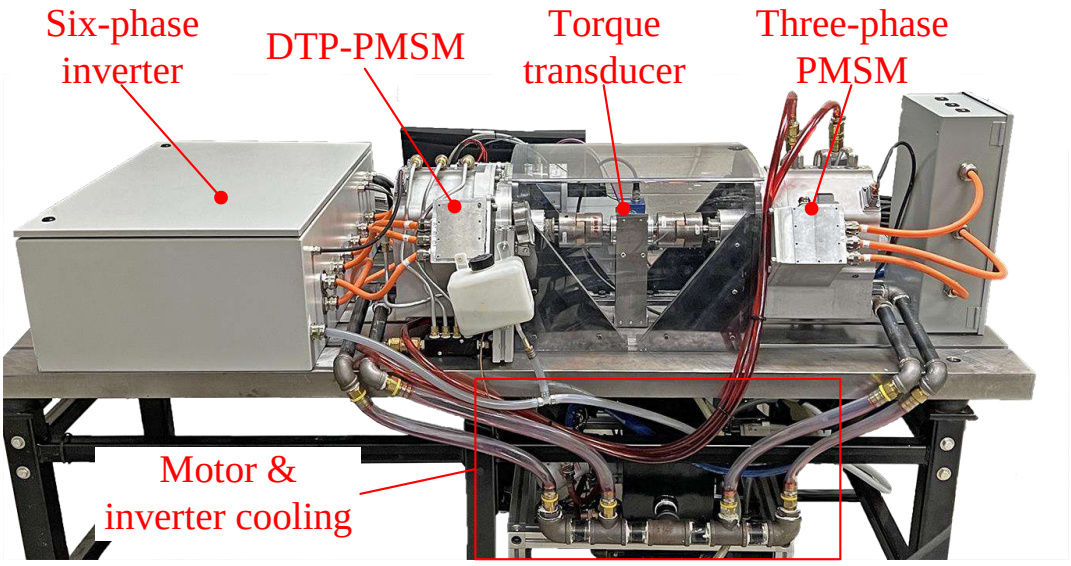
8.1.1 Experimental Implementation and Evaluation

To establish the baseline performance of the DTP-PMSM under FOC using the VSD transformation Figure 8.1, a test bench encompassing a 100 kW, 3 kRPM, 400 V DTP-PMSM is constructed. The DTP-PMSM is mechanically coupled with a three-phase PMSM of the same specifications in a back-to-back configuration. In this configuration, the power is cycled between the DTP-PMSM, operating in motoring (torque) mode, and the three-phase PMSM, operating in speed mode and functioning as a generator. This helps reduce the power requirements from an external power supply, which only needs to supply the power loss in the system [295].

Figure 8.2 shows the motor experimental setup. The same power supply used in the previous chapter is utilized for this experimental setup. The three-phase PMSM is driven by a CM200DX Cascadia Motion inverter [296]. Similar to the MARC100 test bench described in Section 7.5, the DC power supply is connected to a pre-charge and safety circuitry before the power is passed to the motors. The motors are cooled with Dexron VI oil, while the inverters are cooled with a 50/50 water-glycol mixture. The entire system is controlled in dSPACE using the MicroLabBox hardware. The CM200DX was equipped with current sensors and a resolver-to-digital converter to handle inner current control. MicroLabBox communicates with the CM200DX through the CAN bus to read the sensor data and send speed commands. On the other hand, MicroLabBox generates the gating signals for the six-phase inverter. The MicroLabBox is connected to a host PC using Ethernet. A graphical user interface (GUI) is built in ControlDesk for real-time testing, as shown in Figure 8.3.



(a)



(b)

Figure 8.2: High-power six-phase/three-phase motor/dynamometer setup. (a) Top-level diagram. (b) Setup photograph.

The control diagram in Figure 8.1 is implemented in dSPACE and the motor is tested at 30% the rated speed. Figure 8.4, depicts the phase current and line-to-line waveforms of the DTP-PMSM as well as the phase current of the three-phase

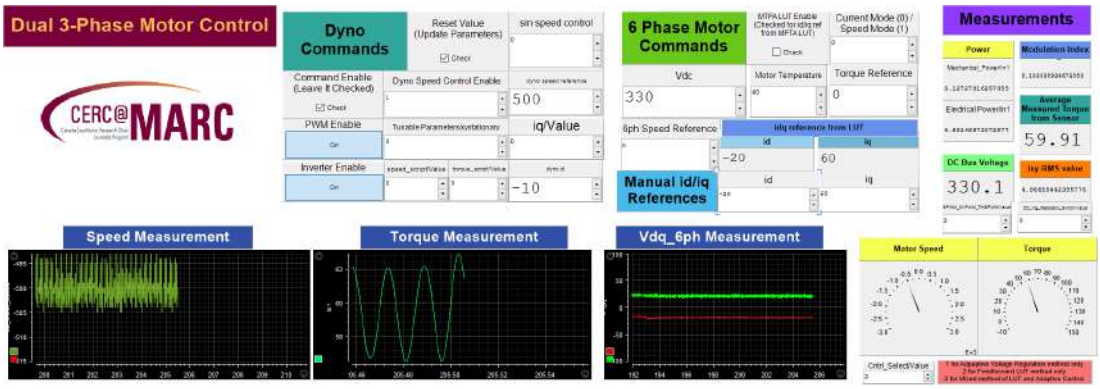


Figure 8.3: Graphical user interface (GUI) for the back-to-back motor/dynamometer setup in ControlDesk.

dynamometer. Both motors are controlled at f_s = 10 kHz. Since $\omega_r \leq \omega_b$, the VR-FW and OVM are not activated in this test. From Figure 8.4, it is observed that the phase current of the dynamometer, i_A is twice as large in amplitude compared to the phase currents of the DTP-PMSM, $i_{A1,A2}$. This is expected as the DTP-PMSM enjoys half the per-phase current of a three-phase counterpart. However, comparing the current quality, i_A enjoys a superior quality with 6% THD compared to almost 13% THD in $i_{A1,A2}$.

To further investigate the current quality of the DTP-PMSM, Figure 8.5 shows the harmonic spectrum of i_A and i_{A1} for the same test reported in Figure 8.4. It can be seen that i_{A1} exhibits a significantly larger 5^{th} and 7^{th} harmonics compared to i_A. This is attributed to the asymmetry between the two three-phase sets of the DTP-PMSM, which can be suppressed with proper xy-control. In this test, the xy-currents were controlled in the stationary frame using a PI controller. The next section investigates other xy-current controls.

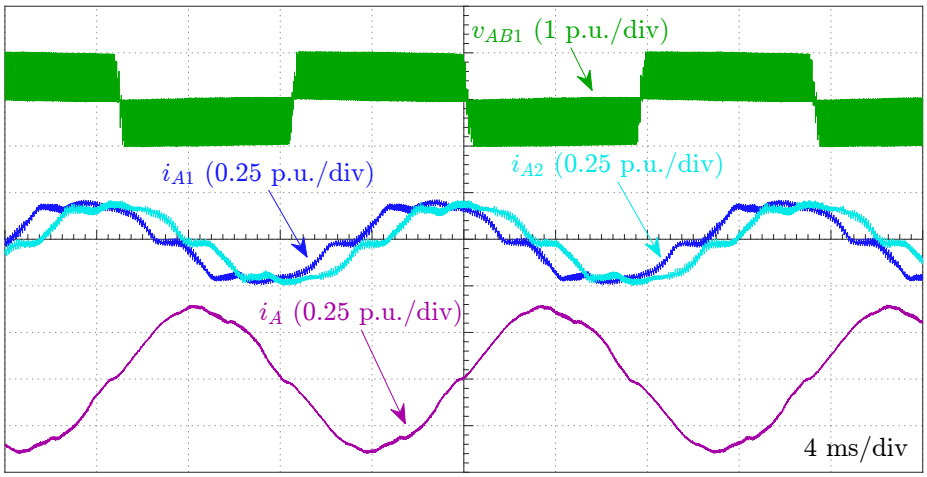


Figure 8.4: Experimental steady-state test of the back-to-back six-phase/three-phase motor/dynamometer setup at 0.3 p.u. speed.

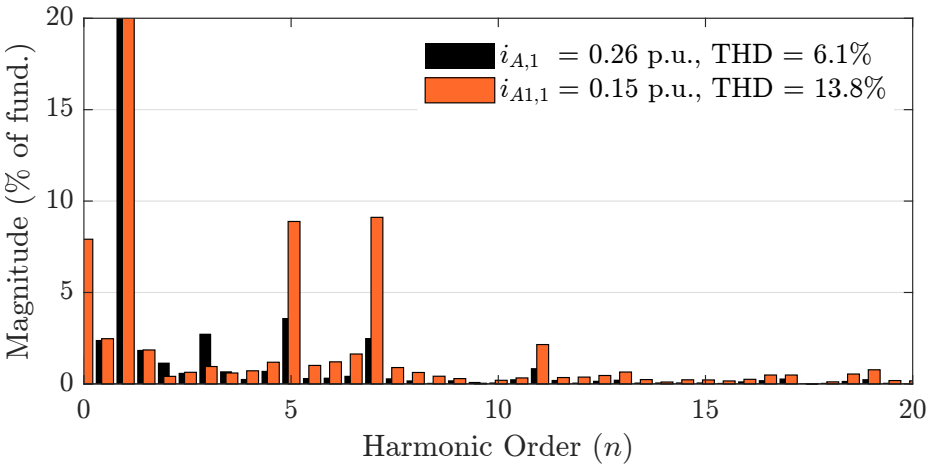


Figure 8.5: Harmonic spectra of v_{AB1} and i_{A1} of the DTP-PMSM in Figure 8.4.

8.2 *xy*-Current Control

From Table 2.1, the xy-currents, i_{xy} of a six-phase motor represent the 5^{th}, 7^{th}, 17^{th}, etc... harmonics of the phase current. Such harmonic components do not contribute to torque production, but rather generate losses. Therefore, their elimination

is desirable (i.e., $i^*_{xy} = 0$). The control of the i_{xy} can be implemented in the stationary frame, synchronous frame, and asynchronous frame as shown in Figure 8.6. In the stationary frame, as the name suggests, the xy components are not rotationally transformed after the VSD transformation as shown in Figure 2.3a and Figure 8.6a. Alternatively, the xy components can be rotationally transformed in the same direction of the Park's transformation applied for the dq components, as shown in Figure 8.6b. In this case, the xy components are controlled in the synchronous frame. If the rotation direction is opposite to that of the dq components, as illustrated in Figure 8.6c, then the xy components are said to be controlled in the asynchronous frame. Applying different transformations is expected to result in a shift in the low-order harmonic, which can be utilized to improve the control performance, as will be shown next.

To suppress i_{xy}, a controller must be used, regardless of the reference frame. However, different combinations of controllers and reference frames will yield different results. The remainder of this section evaluates different controllers for the i_{xy} suppression.

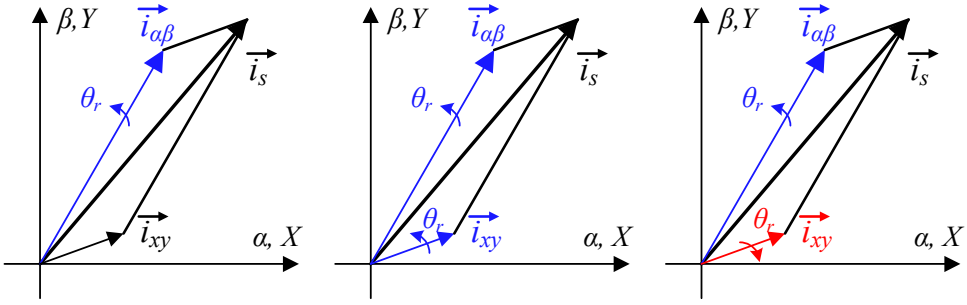


Figure 8.6: Control frames of the xy-currents. (a) Stationary frame. (b) Synchronous frame. (c) Asynchronous frame.

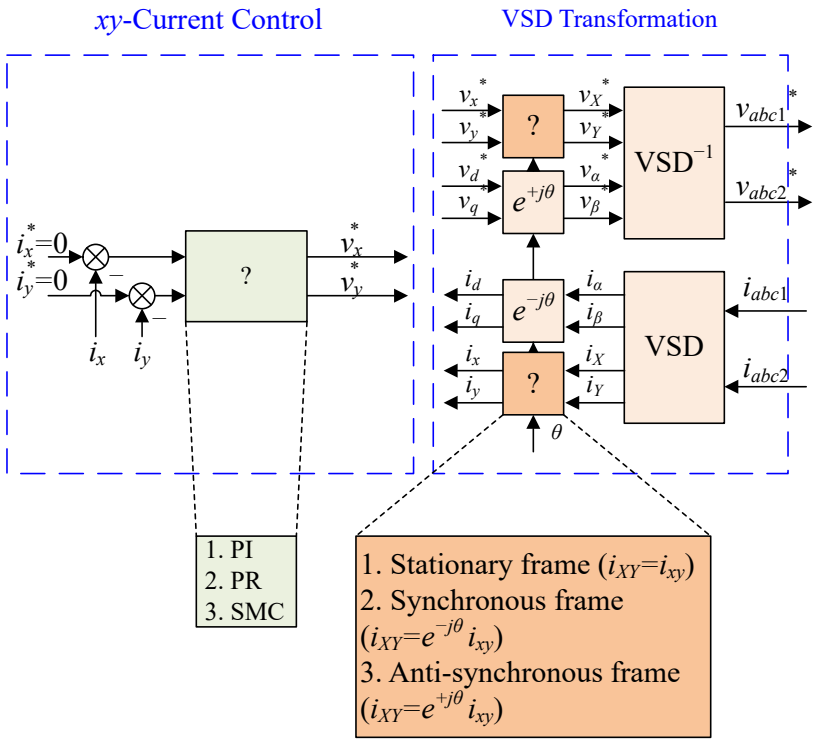


Figure 8.7: Control of xy-currents using different controllers in different reference frames.

8.2.1 Proportional Integral Controller

PI controller is the most commonly used controller owing to its simplicity and well-known characteristics. The transfer function of the PI controller in the s-domain is defined as:

$$C_{PI}(s) = K_P + K_I \frac{1}{s} \tag{8.2.1}$$

where K_P and K_I are the proportional and integral gains, respectively. Tuning of such gains can be conducted using any of the classical control methods, such as zero placement [297, 298].

The PI controller is only effective in suppressing DC components, whereas AC components will be suppressed to a small extent dictated by the controller's bandwidth [57]. Depending on the chosen reference frame in which the PI controller is implemented for i_{xy}, the performance is expected to improve if the frequencies in i_{xy} are shifted closer to DC.

8.2.2 Proportional Resonant Controller

Unlike the PI controller, the PR controller is effective in controlling AC components [299, 300]. The transfer function of an ideal PR controller in the s-domain is defined as:

$$C_{PR}(s) = K_P + K_R \frac{2s}{s^2 + \omega_{rr}^2}, \tag{8.2.2}$$

where K_P and K_R are the proportional and resonant gains, and $\omega_{rr} = \alpha_R \omega_r$ is the resonant frequency where ω_r is the synchronous frequency and α_R is a frame-dependent multiplier to be explained next. The resonance term in (8.2.2) has an infinite gain at ω_{rr} [300]. A more practical implementation of the PR controller includes a damping term. Thus, (8.2.2) is re-written as [301]:

$$C_{PR}(s) = K_P + K_R \frac{2\omega_{cr} s}{s^2 + 2\omega_{cr} s + \omega_{rr}^2} \tag{8.2.3}$$

where ω_{cr} is the damping term. C_{PR} in (8.2.3) has a limited gain at ω_{rr} but can provide high gain at a relatively wide range of frequencies.

The selection of ω_{rr} is dependent on the chosen reference frame in which the C_{PR} is implemented. Therefore, the two-integrator method is utilized to implement the PR controller in the vector proportional-integral form [299], as shown in Figure 8.8. In

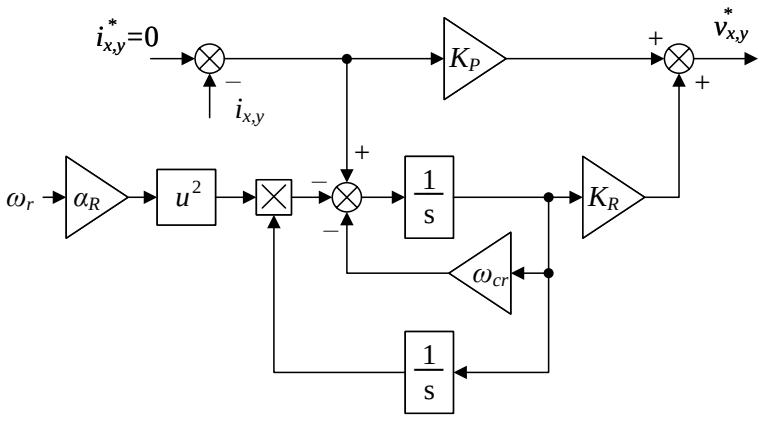


Figure 8.8: Block diagram of the PR controller.

the stationary frame, the PR controller is set to eliminate the lowest order harmonic. Therefore, ω_{rr} is set at $5\omega_r$. If the 5^{th} harmonic is positive sequence, then it will appear at $4\omega_r$ and $6\omega_r$ in the synchronous and asynchronous reference frames, respectively. Therefore,

$$\alpha_R = \begin{cases} 5, & \text{stationary frame} \\ 4, & \text{synchronous frame} \\ 6, & \text{asynchronous frame.} \end{cases} \tag{8.2.4}$$

On the other hand, tuning of K_P and K_R is independent of the reference frame. K_P is selected to obtain the desired selectivity and transient response of the controller, and K_R is selected based on $K_P/K_R = L_s/R_s$. A large K_P yields a quick transient response but reduces selectivity. Additionally, ω_{cr} should be negligibly small compared to ω_{rr} [301].

8.2.3 Digital Sliding Mode Controller

The SMC is easy to implement since no complex functions are required. It breaks down the high dimensional problem to several subproblems in lower dimension to simplify the problem [302]. It also has a strong robustness characteristics which allows the output to reach its desired value regardless the uncertainty in the system [303]. For the $i^*_{xy} = 0$ regulation problem, the xy-current dynamic equation in the discrete-time domain is expressed as

$$i_{xy}[k+1] = \mathbf{A} i_{xy}[k] + \mathbf{B} v_{xy}[k] \tag{8.2.5}$$

where $\mathbf{A}$ and $\mathbf{B}$ are the state transition and input matrices, respectively, obtained via Euler's first-order approximation as

$$\mathbf{A}_{2\times2} = diag\{1 - T_s R_s / L_s\}, \qquad \mathbf{B}_{2\times2} = diag\{Ts / L_s\}. \tag{8.2.6}$$

The desired dynamic behavior of i_{xy} is defined as

$$i_{xy}[k+1] = \zeta\, i_{xy}[k], \tag{8.2.7}$$

where $\zeta < 1$ is the desired rate of descend for i_{xy}. Substituting the x–y subspace of (8.1.1a) in (8.2.7), the equivalent control law is derived as

$$v_{xy}[k] = -\mathbf{B}^{-1}(\mathbf{A} - diag\{\zeta\})\, i_{xy}[k] \tag{8.2.8}$$

The stability of (8.2.8) was proved in [265].

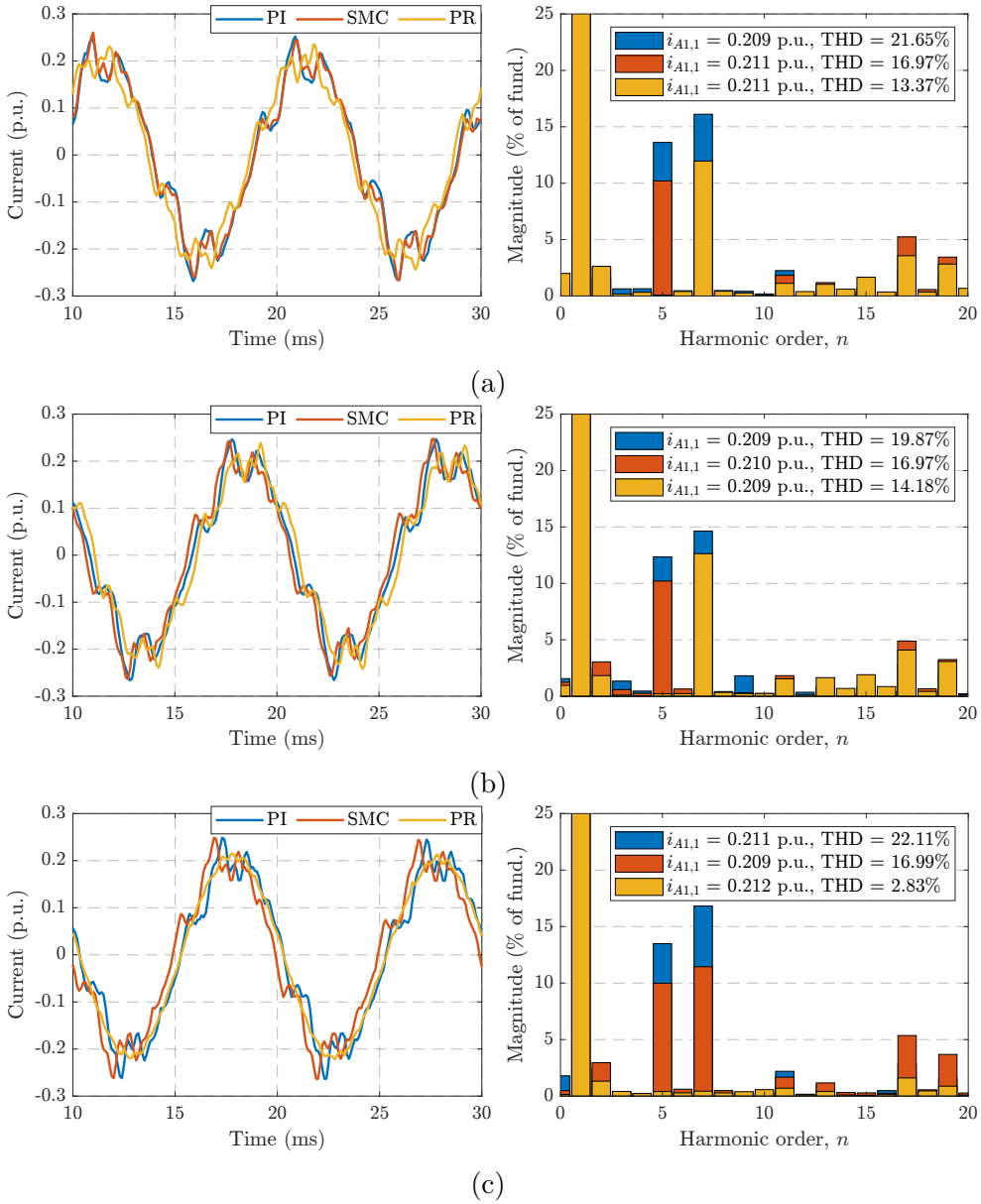


Figure 8.9: Experimental i_{A1} with i_{xy} control at 0.5 p.u. speed and 0.2 p.u. torque: (a) stationary, (b) synchronous, and (c) asynchronous frames.

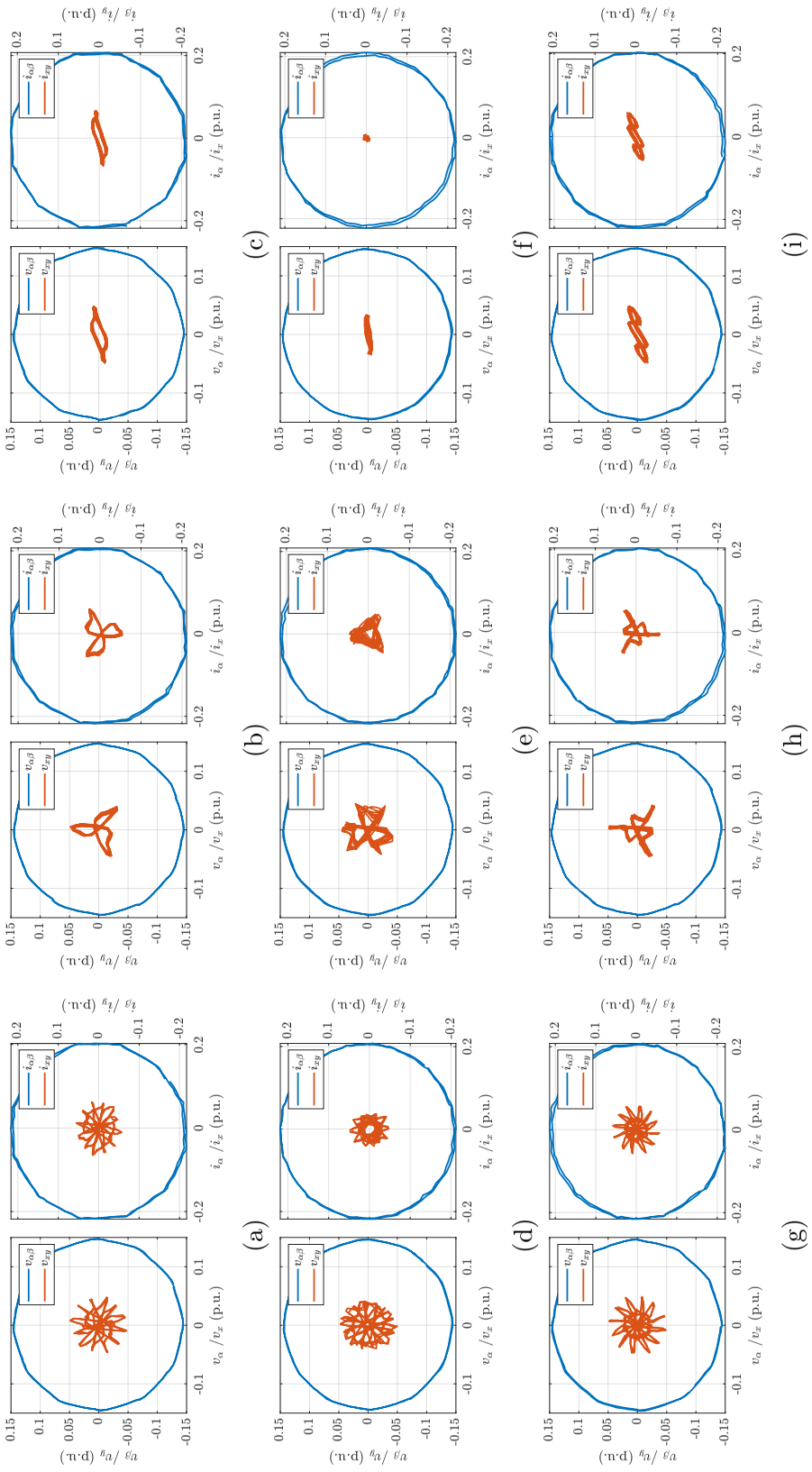


Figure 8.10: Experimental polar plot of $v_{\alpha\beta xy}$ and $i_{\alpha\beta xy}$ controlled using different reference frames and different controllers at 0.5 p.u. speed and 0.2 p.u. torque. Top to bottom row: PI controller, SMC, PR controller. Left to right column: stationary, synchronous, and asynchronous frames.

8.2.4 Experimental Results and Discussions

The effectiveness of the foregoing controllers for xy-current suppression is evaluated through experimental testing using the test bench presented in the previous section. The tests for i_{xy} control are conducted at 0.5 p.u. speed and 0.2 p.u. torque. Figure 8.9 shows the phase current waveform and its respective harmonic spectrum under different i_{xy} controllers implemented in the different reference frames. From Figure 8.9a, the 5^{th} and 7^{th} harmonics are present under PI and SMC. The SMC has a superior suppression of the low-order harmonics compared to PI, thus achieving a lower THD. On the other hand, the only dominant low-order harmonic with PR controller is the 7^{th}. This demonstrates effective elimination of the 5^{th} harmonic when the resonance component is set at $5\omega_r$. As a result, the PR controller achieves a lower THD compared to SMC.

Similar results are observed in the synchronous frame as shown in Figure 8.9b, yet with a slightly improved THD with the PI controller. This means that the positive-sequence low-order harmonics are brought closer to DC, so the PI controller is able to further suppress such AC components with the same bandwidth. The PR controller effectively eliminated the 5^{th} is the synchronous frame with $\omega_{rr} = 4\omega_r$. Therefore, the 5^{th} harmonic is positive-sequence.

In the asynchronous frame (Figure 8.9c), the phase current exhibits a slightly worse THD with PI controller when compared to the stationary frame. On the contrary, PR controller achieves a superior phase current THD below 3%, thanks to the elimination of 5^{th} and 7^{th} harmonics. Therefore, the 7^{th} harmonic is a negative-sequence harmonic that is transformed to 6^{th} harmonic in the asynchronous frame. The positive-sequence 5^{th} harmonic is also transformed into 6^{th} harmonic too in the asynchronous frame.

As such, setting $\omega_{rr} = 6\omega_r$ eliminates both harmonics.

To better visualize the suppression of i_{xy}, and consequently v_{xy}, Figure 8.10 depicts the polar plot of $i_{\alpha\beta XY}$ and $v_{\alpha\beta XY}$ for the results shown in Figure 8.9. The better the suppression of i_{xy} and v_{xy}, the closer they are to the origin. The i_{xy} is closest to the origin under PI controller in the asynchronous frame, as shown in Figure 8.10f. Similarly the v_{xy}, albeit $v_x > v_y$, which suggests an asymmetric dynamics of the x–y space. In other words, R_s and L_s are not exactly the same in the x and y directions. In conclusion, PR controller implemented in the asynchronous frame leads to the best i_{xy} suppression.

8.3 Flux-Weakening Control

Beyond base speed (i.e. $\omega_r \geq \omega_b$), the operation is limited by V_{lim}. Substituting (8.1.1a) in (8.3.1), and neglecting R_s, yields the voltage constraint:

$$\left(\frac{V_{lim}}{\omega_r}\right)^2 = L_d^2\left(\frac{\psi_r}{L_d} + i_d\right)^2 + (L_q i_q)^2. \tag{8.3.1}$$

It follows from (8.3.1) that increasing ω_r beyond ω_b is possible by reducing i_d. In VR-FW techniques, the voltage magnitude is fed back to reduce i_d such that V_{lim} is preserved. Reduction of i_d by means of voltage feedback is attainable by manipulating i_d, i_q, or the current phase angle, $\gamma = \text{atan}(i_q/i_d)$. While all behave similarly from a dynamic perspective, γ adjustment enjoys a relatively lower controller gain variation in deep FW region [274], and therefore is chosen in this study. The γ-command of FW controller, $\Delta\gamma$ is the output of a PI controller. The $\Delta\gamma$ adjusts i_{dq}^* based on FW demand to obtain the reference i_{dq}, as shown in Figure 8.1. While gain variation

is lowest when using the γ-command, it is still high enough that an adaptive gain should be incorporated to maintain the stability margin of the voltage control loop.

The VR-FW control loop is first analyzed using a small-signal model, which provides a systematic tuning methodology of the PI controller based on linear control theory. Then, an adaptive control law is devised to handle the varying stability margin of the voltage control loop as will be shown herein.

8.3.1 Small-Signal Model

Figure 8.11 depicts the small-signal model of the VR-FW control loop. Henceforth, small- and large-signal variables are denoted with ˆ and ˜ accents, respectively. Starting with the FW PI regulator, its output, $\Delta\gamma$ is defined as

$$\Delta\gamma = \underbrace{K_{P\gamma}\left(1 + \frac{1}{T_{I\gamma}s}\right)}_{C_{PI}(s)} e_v, \tag{8.3.2}$$

where $e_v = V_{lim} - v_s^*$, and $K_{P\gamma}$, $T_{I\gamma}$ are the proportional gain and integral time constant of the VR-FW PI controller, respectively. Then, the steady-state current magnitude, I_s and $\Delta\gamma$ are transformed from polar to Cartesian quantities:

$$\begin{aligned}\begin{bmatrix} i_d^* \\ i_q^* \end{bmatrix} &= \begin{bmatrix} \hat{I}_d^* + \tilde{i}_d^* \\ \hat{I}_q^* + \tilde{i}_q^* \end{bmatrix} = \begin{bmatrix} I_s \cos(\Delta\hat{\gamma} + \Delta\tilde{\gamma}) \\ I_s \sin(\Delta\hat{\gamma} + \Delta\tilde{\gamma}) \end{bmatrix} \\ &= \begin{bmatrix} I_s \cos\Delta\hat{\gamma}\cos\Delta\tilde{\gamma} - I_s \sin\Delta\hat{\gamma}\sin\Delta\tilde{\gamma} \\ I_s \sin\Delta\hat{\gamma}\cos\Delta\tilde{\gamma} + I_s \cos\Delta\hat{\gamma}\sin\Delta\tilde{\gamma} \end{bmatrix}.\end{aligned} \tag{8.3.3}$$

Since $|\Delta\tilde{\gamma}| \ll 1$, then

$$\begin{cases} \cos\Delta\tilde{\gamma} \cong 1 \\ \sin\Delta\tilde{\gamma} \cong \Delta\tilde{\gamma} \end{cases}. \tag{8.3.4}$$

So, (8.3.3) can be re-written as:

$$\begin{bmatrix} \hat{I}_d^* + \tilde{i}_d^* \\ \hat{I}_q^* + \tilde{i}_q^* \end{bmatrix} = \begin{bmatrix} I_s\cos\Delta\hat{\gamma} - I_s\sin\Delta\hat{\gamma}\cdot\Delta\tilde{\gamma} \\ I_s\sin\Delta\hat{\gamma} + I_s\cos\Delta\hat{\gamma}\cdot\Delta\tilde{\gamma} \end{bmatrix} = \begin{bmatrix} \hat{I}_d^* - \hat{I}_q^*\cdot\Delta\tilde{\gamma} \\ \hat{I}_q^* + \hat{I}_d^*\cdot\Delta\tilde{\gamma} \end{bmatrix}. \tag{8.3.5}$$

Therefore, the small-signal reference currents, $\tilde{i}_{d,q}^*$ are

$$\begin{bmatrix} \tilde{i}_d^* \\ \tilde{i}_q^* \end{bmatrix} = \underbrace{\begin{bmatrix} -\hat{I}_q^* \\ \hat{I}_d^* \end{bmatrix}}_{G(s)}\Delta\tilde{\gamma}. \tag{8.3.6}$$

The $\tilde{i}_{d,q}^*$ are, in turn, fed to the current loop. A linearized small-signal motor model, assuming $v_{xy} = 0$, is given as

$$\begin{bmatrix} \tilde{v}_d \\ \tilde{v}_q \end{bmatrix} = \underbrace{\begin{bmatrix} L_d s + R_s & -L_q\omega_r \\ L_d\omega_r & L_q s + R_s \end{bmatrix}}_{Z(s)}\begin{bmatrix} \tilde{i}_d \\ \tilde{i}_q \end{bmatrix}, \tag{8.3.7}$$

with $[\tilde{i}_d \quad \tilde{i}_q]^T = T(s)[\tilde{i}_d^* \quad \tilde{i}_q^*]^T$ where $T(s)$ is the PI current regulators modeled using complex vectors [304]. The model can be easily represented using state-space notation as:

$$\begin{aligned} \dot{\mathrm{x}} &= \mathbf{A}\mathrm{x} + \mathbf{b}\mathrm{u} \\ \mathrm{y} &= \mathbf{C}\mathrm{x} + \mathbf{d}\mathrm{u} \end{aligned}, \tag{8.3.8}$$

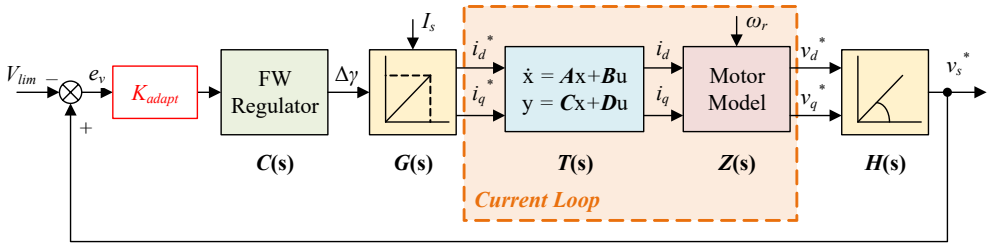


Figure 8.11: Block diagram of the small-signal model for the voltage control loop.

with x = $[\psi_d \quad \psi_q \quad v_d \quad v_q]^T$, u = $[i_d^* \quad i_q^*]^T$, y = $[i_d \quad i_q]^T$,

$$\mathbf{A} = \begin{bmatrix} -(K_{Pd} + R_s)/L_d & \omega_r & 1 & 0 \\ -\omega_r & -(K_{Pq} + R_s)/L_q & 0 & 1 \\ -K_{Id}/L_d & K_{Pq}\omega_r/L_q & 0 & 0 \\ -K_{Pd}\omega_r/L_d & -K_{Iq}/L_q & 0 & 0 \end{bmatrix},$$

$$\mathbf{b} = \begin{bmatrix} K_{Pd} & 0 \\ 0 & K_{Pq} \\ K_{Id} & -K_{Pq}\omega_r \\ K_{Pd}\omega_r & K_{Iq} \end{bmatrix}, \quad \mathbf{C} = \begin{bmatrix} 1/L_d & 0 & 0 & 0 \\ 0 & 1/L_q & 0 & 0 \end{bmatrix},$$

and $\mathbf{d} = \mathbf{0}_{2\times2}$, where K_P and K_I are the proportional and integral gains and the d and q subscripts denote d- and $q-$currents, respectively. Thus, $T(s) = \mathbf{C}(sI - \mathbf{A})^{-1}\mathbf{b}+\mathbf{d}$, where I is the identity matrix. The resulting $T(s)$ is a 2×2 transfer matrix whose diagonal transfer functions are 2$^{\text{nd}}$ order. The PI parameters of the current loop ($T(s)Z(s)$) are tuned based on zero-pole cancellation for a desired bandwidth [298]. For the small-signal model, decoupling terms in steady-state are assumed zero, and hence neglected. The output from the current control loop, i.e. reference dq-axes voltages, $v_{d,q}^*$ from the current loop are then converted to voltage magnitude.

Decomposing the voltage magnitude, v_s^* into large- and small-signal components:

$$\begin{aligned} v_s^2 &= (\hat{v}_s + \tilde{v}_s)^2 \\ &= (\hat{v}_d + \tilde{v}_d)^2 + (\hat{v}_q + \tilde{v}_q)^2 \\ &= V_s^2 + 2(\hat{v}_d\tilde{v}_d + \hat{v}_q\tilde{v}_q) + \underbrace{\tilde{v}_d^2 + \tilde{v}_q^2}_{\ll V_s^2} \\ &= V_s^2\left[1 + 2\frac{\hat{v}_d\tilde{v}_d + \hat{v}_q\tilde{v}_q}{V_s^2}\right]. \end{aligned} \tag{8.3.9}$$

Taking the square root of both sides of (8.3.9) yields

$$(\hat{v}_s + \tilde{v}_s) = V_s + \frac{\hat{v}_d\tilde{v}_d + \hat{v}_q\tilde{v}_q}{V_s}. \tag{8.3.10}$$

Therefore, the small-signal reference voltage, $\tilde{v}_s^*$ is given as

$$\tilde{v}_s = \frac{1}{V_s}(\hat{v}_d\tilde{v}_d + \hat{v}_q\tilde{v}_q) = \underbrace{\begin{bmatrix}\frac{\hat{v}_d}{V_s} & \frac{\hat{v}_q}{V_s}\end{bmatrix}}_{H(s)}\begin{bmatrix}\tilde{v}_d \\ \tilde{v}_q\end{bmatrix}. \tag{8.3.11}$$

8.3.2 Closed Loop Analysis

An acceptable tuning approach for the PI controller of the VR-FW is based on zero-pole cancellation, with $T_{I\gamma}$ set equal to the time constant of the current loop [275]. The proportional gain can be set as

$$K_{P\gamma} = \frac{1}{I_{s,nom}} \cdot \frac{BW_{FW}}{BW_C}, \tag{8.3.12}$$

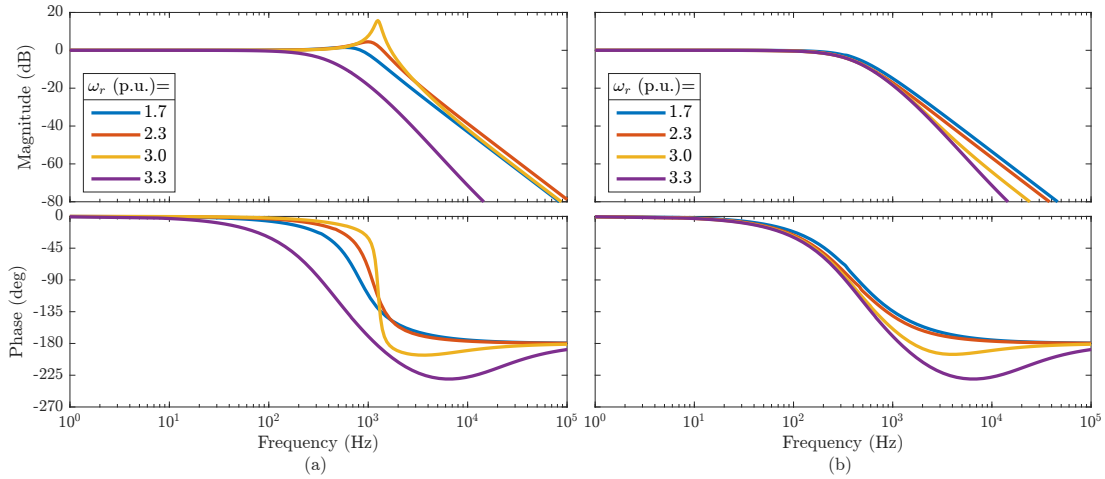


Figure 8.12: Bode plot of FW controller bandwidth using small-signal model. (a) Non-adaptive control. (b) Adaptive control.

where BW_C and BW_{FW} are the bandwidths of the current and FW control loops, respectively, and $I_{s,nom}$ is the rated current of the motor. The reciprocal of $I_{s,nom}$ is necessary to normalize the gain in $G(s)$. The bandwidth of the voltage FW control loop can be designed to yield a 1^{st} order LPF response. This normally takes place over the range of $0.3BW_C$ to $0.6BW_C$.

Figure 8.12a presents the closed-loop Bode diagram of the small-signal model in Figure 8.11, evaluated at various operating speeds. The controller tuning was conducted at a base speed of ω_b = 3 kRPM. Figure 8.12a exhibits the diminishing stability margin of the voltage control loop at higher speeds. This calls for gain adaptation to normalize the static gain of the loop throughout the speed range, which is developed next.

8.3.3 Adaptive Control

A simple and effective adaptive law can be deduced from simplifying the voltage equation in (8.1.1a). When FW control is active, the voltage magnitude is in steady-state and close to V_{lim}. Therefore, the derivative terms in (8.1.1a) can be dropped, along with R_s. As a result, the steady-state relation between voltage and current reduces to:

$$\begin{cases} V_d \approx -\omega_r L_q I_q \approx -\omega_r L_q I_s \sin\gamma \\ V_q \approx \omega_r (L_d I_d + \psi_r) \approx \omega_r (L_d I_s \cos\gamma + \psi_r) \end{cases}. \tag{8.3.13}$$

This assumption has been validated in [274]. Applying the small-signal approach developed in the previous subsection, a steady-state relation between the voltage magnitude, V_s to γ is sought. Assuming that the mechanical time constant is much larger than the electrical one, ω_r and I_s can be treated as constants. As such, the derivative of V_s with respect to γ yields the static gain in (8.3.14) that links the small-signal voltage to γ [275]:

$$\begin{aligned} \frac{\partial V_s}{\partial \gamma} &= \frac{-\omega_r}{V_{lim}} \Big[V_d L_q I_s \cos\gamma + V_q L_d I_s \sin\gamma \Big] \\ &= \frac{-\omega_r}{V_{lim}} \Big[V_d L_q I_d + V_q L_d I_q \Big] \end{aligned}. \tag{8.3.14}$$

The adaptive gain can then be expressed as a weighting factor of the static gain ($\partial V_s/\partial\gamma$) at an operating point to its counterpart at the nominal point (where the controller is tuned offline). Therefore, the adaptive gain, K_{adapt} is given as:

$$K_{adapt} = \frac{\big(\partial V_s/\partial\gamma\big)_{\gamma=\gamma_{nom}}}{\partial V_s/\partial\gamma}, \tag{8.3.15}$$

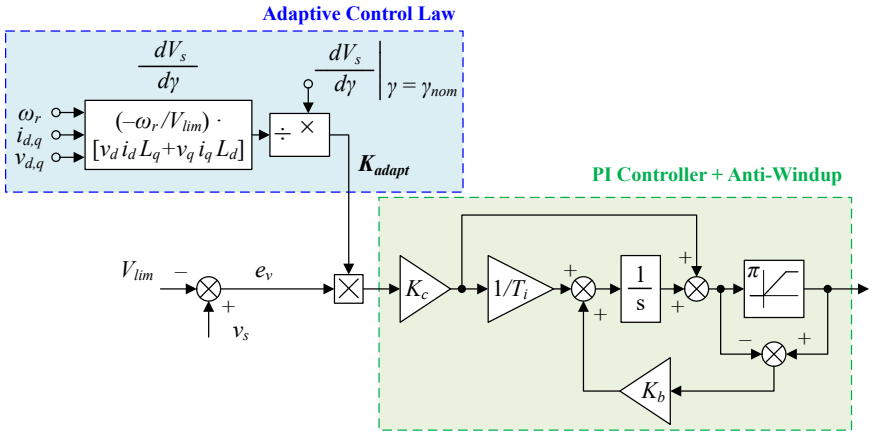


Figure 8.13: Adaptive voltage regulation flux-weakening controller (with anti wind-up) using gain adaptation in (8.3.15).

where γ_{nom} is the current phase angle at the nominal point. The nominal point can be computed at ω_b. The resulting closed-loop behavior with K_{adapt} is shown in Figure 8.12b. Therein, the effectiveness of K_{adapt} to maintain the loop bandwidth at different speeds is demonstrated. In the VSD-based FOC, K_{adapt} is applied in cascade with the gain of the PI controllers, as illustrated in Figure 8.13.

8.3.4 Simulation Results and Discussions

The proposed adaptive VR-FW technique, along with small-signal controller tuning, is tested in Matlab/Simulink on a 100 kW, 3 kRPM DTP-PMSM. Machine modeling was conducted using FEA. The model provides a high accuracy by considering the nonlinear characteristics of L_d, L_q, and L_s using LUTs. The employed switching frequency is 10 kHz. The DC-bus voltage is V_{dc} = 350 V. The effective voltage limit is set at 92% of the theoretical limit (i.e. $V_{dc}/\sqrt{3}$) to account for voltage harmonics and inverter dead-time.

System evaluation entails steady-state and dynamic testing as follows. Firstly, the

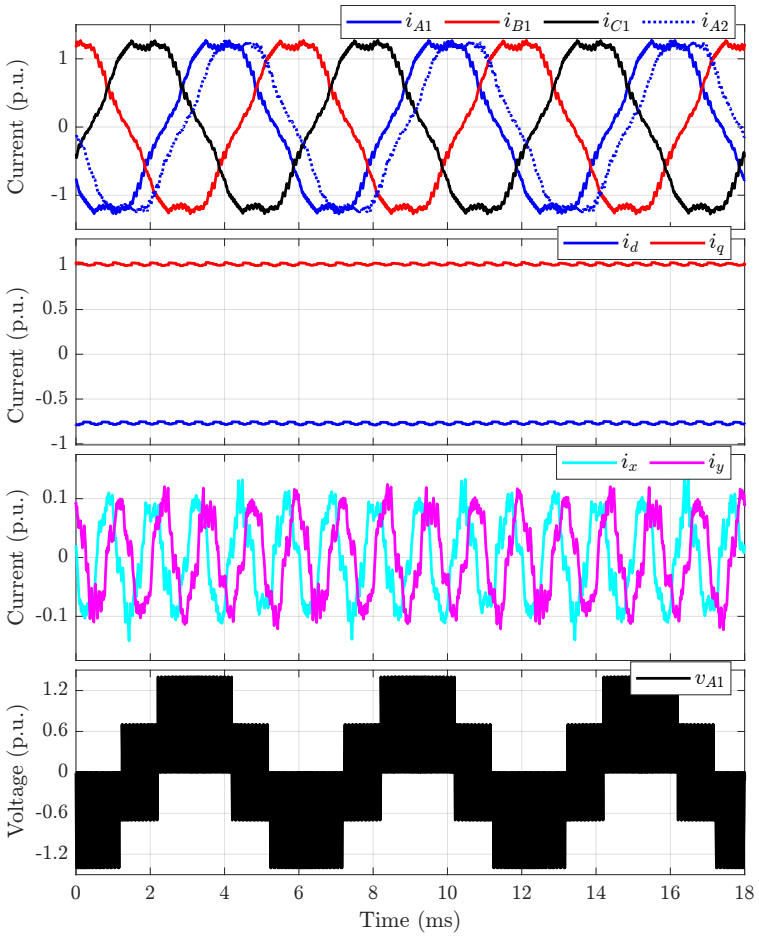


Figure 8.14: Steady-state performance at rated torque and 0.83 p.u. speed: showing phase currents, dq- and xy-currents, and phase voltage.

VSD-based control of the DTP-PMSM drive is tested at low speed, i.e. outside of FW region to establish baseline performance. Figure 8.14 shows current and phase voltage waveforms at 1.0 p.u. load torque and 0.83 p.u. speed. At this stage, FW controller is not activated and $\Delta\gamma = 0$. The i_{xy} are circulating at 5 times the fundamental frequency. The current THD is 8.2%.

Secondly, transition into FW region using non-adaptive and adaptive FW control is studied. Figure 8.15 depicts a speed ramp from 0.97 p.u. to 1.03 p.u. at a rate of 1

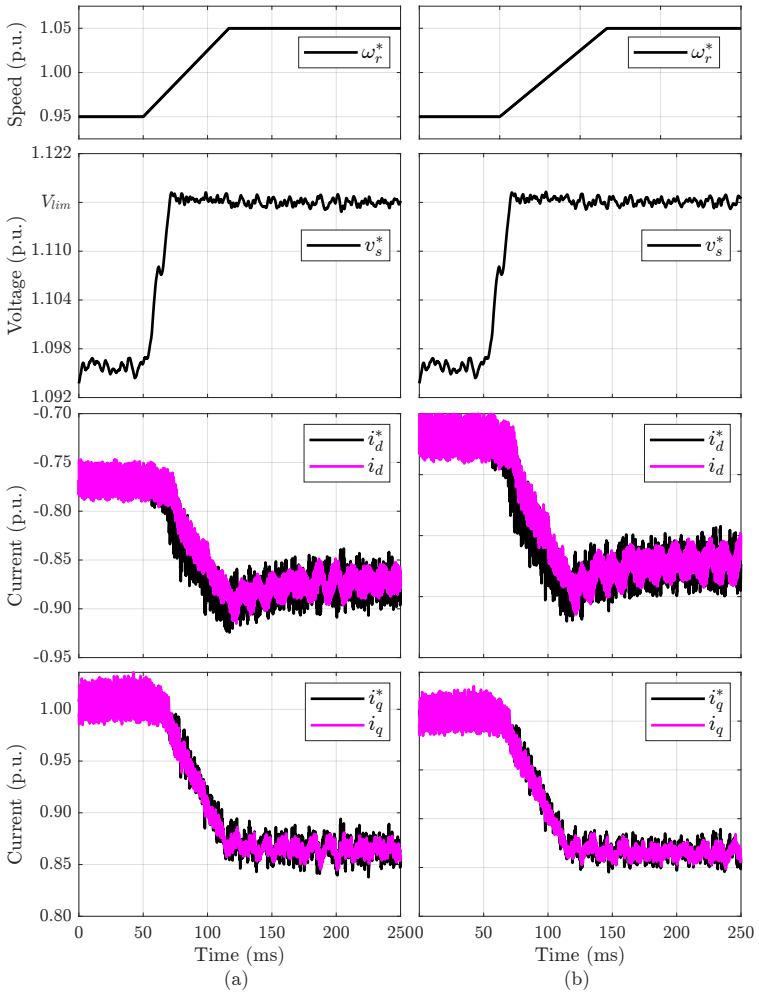


Figure 8.15: Dynamic performance at rated torque and speed ramp from 0.97 p.u. to 1.03 p.u. (a) Non-adaptive FW control. (b) Adaptive FW control.

p.u./s, at rated torque. To this end, FW control is activated as the drive exceeds the base speed (i.e. $\Delta\gamma \neq 0$). Comparing adaptive to non-adaptive FW control in Figure 8.15, the superiority is not evident; only a meager improvement is observed in i_{dq}. This is, nonetheless, expected at the edge of the FW region as the bandwidth of the voltage loop is almost similar to its nominal counterpart. Consequently, $K_{adapt} \approx 1$ in this test.

Thirdly, the change in VR-FW control loop is demonstrated in Figure 8.16, where the speed is increased towards the capability limit of the DTP-PMSM drive. In Figure 8.16 the DTP-PMSM drive is essentially controlled using the proposed adaptive FW control at rated torque and speeds between 1.27 p.u. and 1.28 p.u.. However, K_{adapt} is switched off over some time to study the effectiveness of the adaptive control law. Over the interval of $50 \leq t \leq 100$ ms and 1.27 p.u. speed, non-adaptive VR-FW control suffers higher oscillations in i_{dq}^{*} and v_{s}^{*} when compared to the adaptive controller. Far worse, at 1.28 p.u. when K_{adapt} is turned off at $250 \leq t \leq 290$ ms, the non-adaptive VR-FW controller fails to maintain drive stability. Therefore, the adaptive controller offers an extended speed-range by maintaining a viable voltage loop bandwidth.

8.4 Overmodulation

A comparative analysis of OVM methods based on four segmented formulas is presented in this section [268]. Firstly, the generalized formula is defined for existing methods and a specific average modulation voltage is shown to compare. Secondly, analyses on the fundamental component, harmonic content, transition into six-step, modulation linearization, and complexity of execution are investigated for the studied OVM techniques. Lastly, simulation results are presented to verify the effectiveness of all the methods on a DTP-PMSM platform.

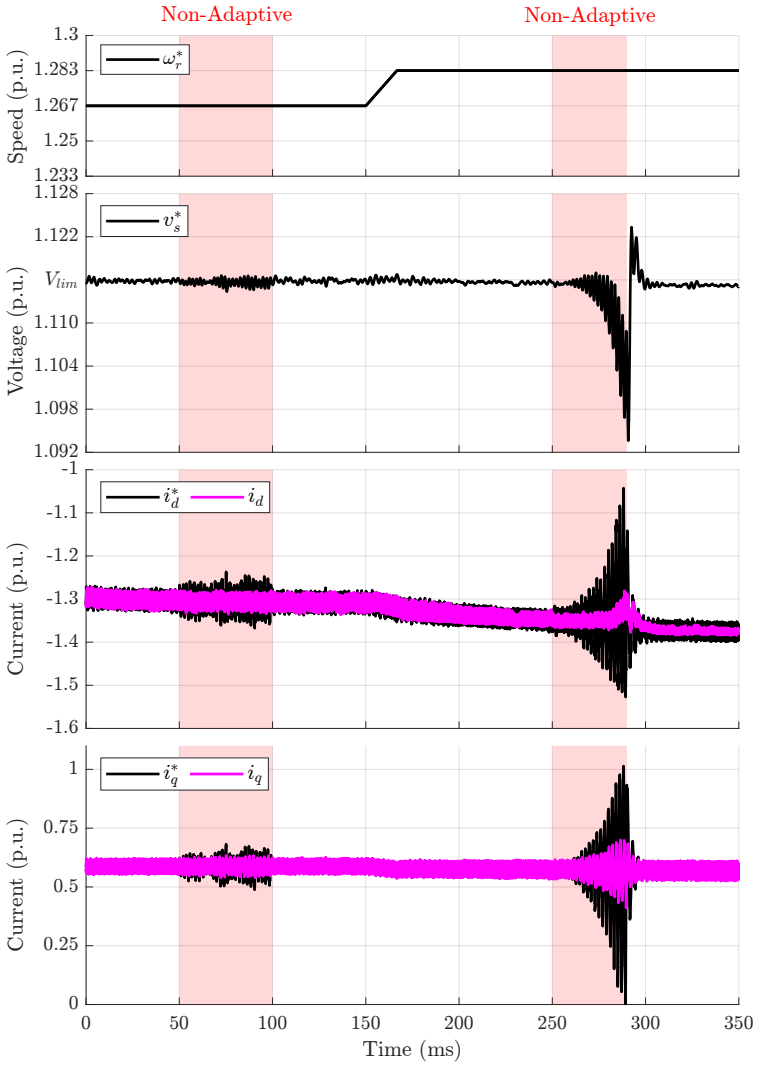


Figure 8.16: Dynamic performance at rated torque and speed ramp from 1.27 p.u. to 1.28 p.u. using non-adaptive FW control over the red-shaded time intervals and adaptive control elsewhere.

8.4.1 Generalized Form of SVM by Two Modulators

The modulation index, M definition in (2.2.3) is used when the modulation is limited to the linear region. To enable OVM, the modulation index is redefined as:

$$MI = \frac{\hat{V}_1}{2V_{dc}/\pi} \tag{8.4.1}$$

According to the definition provided in (8.4.1), the linear region is defined as $0 \leq MI \leq 0.907$. When voltage reference, v_s^* is applied, the corresponding MI reference, MI^* can be calculated as $MI^* = v_s^*/(2V_{dc}/\pi)$. However, when considering the fundamental component, the actual MI can be obtained through Fourier analysis. In linear modulation, MI^* and MI are equal, but in overmodulation, they differ. Therefore, when analyzing overmodulation, two sets of quantities are required, as listed in Table 8.1. In the OVM algorithm, v_s represents the output voltage magnitude, θ_v^* is the voltage vector reference angle, and θ_v is the output angle.

Table 8.1: Overmodulation inputs and outputs

Items of Voltage Vector	Input	Output
Magnitude	v_s^*	v_s
Angle	θ_v^*	θ_v

Generalized Formulas

For a simplified analysis, the reference voltage vector is assumed to be located in the first sector ($0 \leq \theta_v < \pi/3$). Irrespective of the modulation technique applied, the

output voltage vector $\mathbf{v_s}$ can be expressed as

$$\mathbf{v_s} = v_s e^{j\theta_v}. \tag{8.4.2}$$

For linear modulation, $v_s = v_s^*$ and $\theta_v = \theta_v^*$. For OVM, v_s and θ_v are generated by an auxiliary magnitude and angle, defined as:

$$v_s = f_v\left(\theta_v\right), \tag{8.4.3}$$

$$\theta_v = \begin{cases} \theta_1^* & \theta_v^* \in \left[0, \quad \theta_p\right] \\ \theta_2^* & \theta_v^* \in \left(\theta_p, \quad \pi/6\right) \\ \theta_3^* & \theta_v^* \in \left[\pi/6, \quad \pi/3 - \theta_p\right) \\ \theta_4^* & \theta_v^* \in \left[\pi/3 - \theta_p, \quad \pi/3\right] \end{cases}. \tag{8.4.4}$$

Table 8.2: Magnitude and angle in the different overmodulation techniques

–	**MPE**		**MDE**				**KSS**			
Mode	–		I		II		I		II	
$\mathbf{v_s}$	v_s	θ_v	v_s	θ_v	v_s	θ_v	v_s	θ_v	v_s	θ_v
θ_1^*	v_s^*	θ_v^*	v_s^*	θ_v^*	$2V_{dc}/3$	0	v_s^*	θ_v^*	$2V_{dc}/3$	0
θ_2^*	v_1^*	θ_v^*	v_2^*	θ_1	v_2^*	θ_1	v_2^*	θ_3	v_2^*	θ_3
θ_3^*	v_1^*	θ_v^*	v_2^*	θ_2	v_2^*	θ_2	v_2^*	θ_4	v_2^*	θ_4
θ_4^*	v_s^*	θ_v^*	v_s^*	θ_v^*	$2V_{dc}/3$	$\pi/3$	v_s^*	θ_v^*	$2V_{dc}/3$	$\pi/3$
–	**MME**		**LeeD**				**LeeH**		**MMPE**	
Mode	–		I		II		–		II	
$\mathbf{v_s}$	v_s	θ_v	v_s	θ_v	v_s	θ_v	v_s	θ_v	v_s	θ_v
θ_1^*	v_s^*	θ_v^*	v_s^*	θ_v^*	$2V_{dc}/3$	0	$2V_{dc}/3$	0	$2V_{dc}/3$	0
θ_2^*	v_s^*	θ_p	v_3^*	θ_5	v_s^*	θ_5	$V_{dc}/\sqrt{3}$	θ_v^*	v_1^*	θ_v^*
θ_3^*	v_s^*	$\pi/3 - \theta_p$	v_3^*	θ_5	v_3^*	θ_5	$V_{dc}/\sqrt{3}$	θ_v^*	v_1^*	θ_v^*
θ_4^*	v_s^*	θ_v^*	v_s^*	θ_v^*	$2V_{dc}/3$	0	$2V_{dc}/3$	$\pi/3$	$2V_{dc}/3$	$\pi/3$

The specific expression of $f_v(\theta_v)$, θ_p, θ_1, θ_2, θ_3 and θ_4 is determined by the applied OVM method. Table 8.2 summarizes the definition of such expression for the different OVM methods considered in this thesis. The implementation of each OVM method is discussed next.

Minimum Phase Error (MPE)

The objective of the MPE method is to minimize the angle difference between θ_v^* and θ_v. There is only one modulation mode in this technique. When the reference voltage vector $\mathbf{v_s^*}$ lies in the modulation hexagon, $\mathbf{v_s}$ is kept the same as $\mathbf{v_s^*}$. When $\mathbf{v_s^*}$ is outside the modulation hexagon, $\mathbf{v_s}$ is reduced to the modulation hexagon based on θ_v^*. This means that although v_s is not always equal to v_s^*, θ_v is always equal to θ_v^*. Hence, the phase error is 0. It follows that v_1^* and θ_p can be expressed as

$$v_1^* = \frac{V_{dc}}{\sqrt{3}\sin\left(\frac{2\pi}{3} - \theta_v^*\right)} \tag{8.4.5}$$

$$\theta_p = \frac{\pi}{6} - \cos^{-1}\left(\frac{V_{dc}}{\sqrt{3}v_s^*}\right) \tag{8.4.6}$$

Minimum Distance Error (MDE)

The objective of the MDE method is to minimize the length between $\mathbf{v_s^*}$ and $\mathbf{v_s}$. There are two modulation modes in this technique. In Mode I, $\mathbf{v_s^*}$ lies in the modulation hexagon, and the modulation is applied in the same fashion as in the MPE method. When $\mathbf{v_s^*}$ is outside of the modulation hexagon, $\mathbf{v_s}$ is computed as the projection of $\mathbf{v_s^*}$ on the hexagon boundary. In Mode II, $\mathbf{v_s}$ is always generated as the projection. Therefore, the distance error is $\min\left(|\mathbf{v_s^*} - \mathbf{v_s}|\right)$. It follows that v_2^*, θ_1, θ_2,

and θ_p can be expressed as

$$v_2^* = \frac{V_{dc}}{\sqrt{3}\cos\left(|\frac{\pi}{6} - \theta_v|\right)} \tag{8.4.7}$$

$$\theta_1 = \frac{\pi}{6} - \tan^{-1}\left(\tan\Delta\theta - \sin\Delta\theta\left(\frac{\sqrt{3}v_s^*}{V_{dc}} - \frac{1}{\cos\Delta\theta}\right)\right) \tag{8.4.8}$$

$$\theta_2 = \frac{\pi}{6} + \tan^{-1}\left(\tan\Delta\theta - \sin\Delta\theta\left(\frac{\sqrt{3}v_s^*}{V_{dc}} - \frac{1}{\cos\Delta\theta}\right)\right) \tag{8.4.9}$$

where $\Delta\theta = |\left(\pi/6 - \theta_v^*\right)|$.

Mode I: θ_p can be obtained by (8.4.6)

Mode II:

$$\theta_p = \frac{\pi}{6} - \sin^{-1}\left(\frac{V_{dc}}{3v_s^*}\right) \tag{8.4.10}$$

Keeping Switching State (KSS)

The objective of the KSS method is to hold on one active vector switching state. There are two modulation modes in this method. In Mode I, $\mathbf{v_s^*}$ lies in the modulation hexagon, and its implementation is the same as the MPE method. When $\mathbf{v_s^*}$ is outside the modulation hexagon, $\mathbf{v_s}$ is reduced to the modulation hexagon with no change on the α- or β-components of $\mathbf{v_s^*}$. In Mode II, $\mathbf{v_s}$ is always generated on the modulation hexagon with no change on the α- or β-components of $\mathbf{v_s^*}$. The KSS holds on v_α^* or v_β^*. θ_3, θ_4 and θ_p can be expressed as

$$\theta_3 = \frac{\pi}{6} - \tan^{-1}\left(\tan\Delta\theta - \frac{\sqrt{3}\sin(\frac{\pi}{3} - \theta_v^*)}{2}\left(\frac{\sqrt{3}v_s^*}{V_{dc}} - \frac{1}{\cos\Delta\theta}\right)\right) \tag{8.4.11}$$

$$\theta_4 = \frac{\pi}{6} + \tan^{-1}\left(\tan\Delta\theta - \frac{\sqrt{3}\sin\theta_v^*}{2}\left(\frac{\sqrt{3}v_s^*}{V_{dc}} - \frac{1}{\cos\Delta\theta}\right)\right) \tag{8.4.12}$$

where $\Delta\theta = |\pi/6 - \theta_v^*|$.

Mode I: θ_p can be obtained by (8.4.6)

Mode II:

$$\theta_p = \frac{\pi}{6} - \sin^{-1}\left(\frac{V_{dc}}{\sqrt{3}v_s^*}\right) \tag{8.4.13}$$

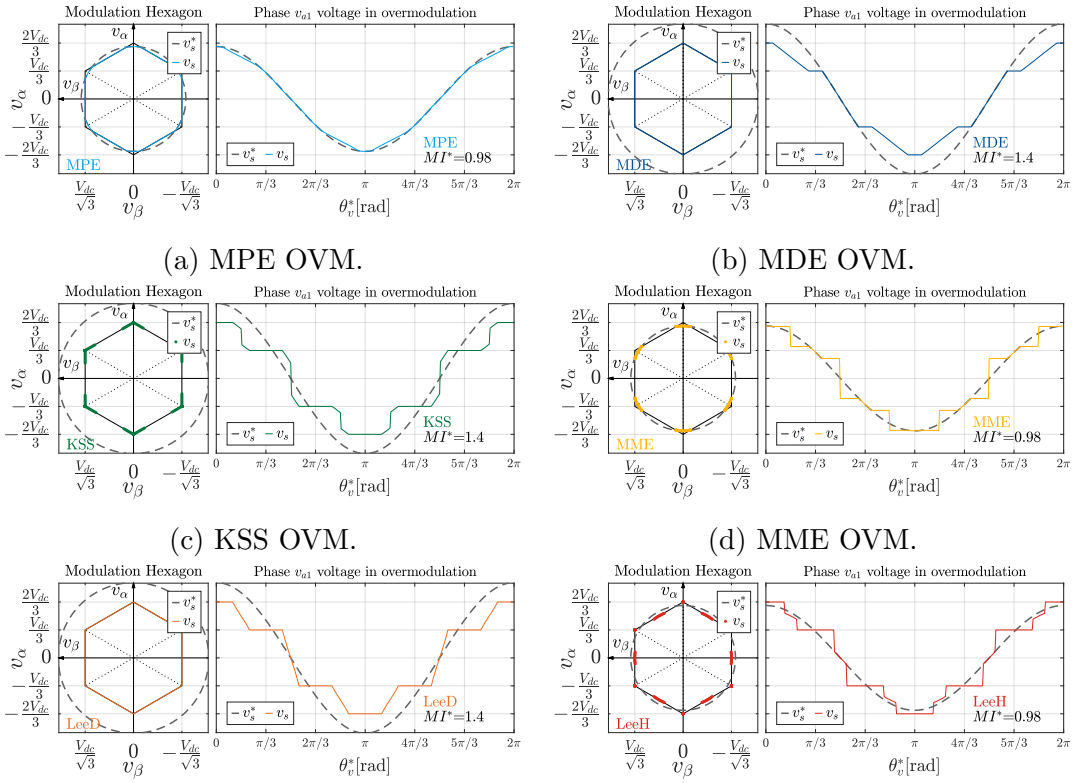
Minimum Magnitude Error (MME)

The objective of the MME method is to minimize the magnitude between $\mathbf{v_s^*}$ and $\mathbf{v_s}$. There is only one modulation mode in this method. When $\mathbf{v_s^*}$ lies in the modulation hexagon, $\mathbf{v_s}$ is kept the same as $\mathbf{v_s^*}$. When $\mathbf{v_s^*}$ is outside the modulation hexagon, $\mathbf{v_s}$ is held at the intersection of reference voltage circle and modulation hexagon. This means that although θ_v is not always equal to θ_v^*, v_s is always equal to v_s^*. Therefore, the magnitude error is zero. It follows that θ_p can be obtained by as defined in (8.4.6).

Dong-Choon Lee's Method

Dong-Choon Lee's method, labeled LeeD henceforth, is a modified version of the MPE method. There are two modulation modes in this method. In Mode I, its implementation is the same as the MPE method. In Mode II, $\mathbf{v_s}$ is held at the modulation vertex first, then it moves along the modulation side, and finally stays at the next vertex. It follows that v_3^* and θ_5 can be expressed as

$$v_3^* = \frac{V_{dc}}{\sqrt{3}\sin\left(\frac{2\pi}{3} - \theta_v\right)} \tag{8.4.14}$$



(a) MPE OVM. (b) MDE OVM.

(c) KSS OVM. (d) MME OVM.

(e) LeeD OVM. (f) LeeH OVM.

Figure 8.17: Modulation hexagon and average phase v_{A1} voltage.

$$\theta_5 = \frac{\pi}{\pi - 6\theta_p}\left(\theta_v^* - \theta_p\right) \tag{8.4.15}$$

θ_p can be obtained by (8.4.6) in Mode I and (8.4.13) in Mode II.

Heekwang Lee's Method

Heekwang Lee's method, labeled LeeH henceforth, is a δ-based OVM. There is only one modulation mode in this technique. This method can be considered as a combination of the maximum linear modulation and the six-step operation. It follows that θ_p can be obtained by (8.4.6).

Average Voltage Modulation Waveforms

For an easy understanding and direct comparison of the six aforementioned OVM methods, the modulation hexagon voltage trajectories and average v_{A1} waveforms are shown in Figure 8.17. The comparison at the same MI^* is discussed in the next section. For MPE in Figure 8.17a, the change in $\mathbf{v_s}$ occurs at $[\theta_p, \quad \pi/3 - \theta_p]$ for each sector and $\mathbf{v_s}$ is reduced to hexagon side. For MDE OVM in Figure 8.17b, the change on $\mathbf{v_s}$ occurs in the whole sector and $\mathbf{v_s}$ is reduced to hexagon boundary. For KSS OVM in Figure 8.17c, there exists the voltage discontinuous problem around the middle of hexagon side in each sector. For MME in Figure 8.17d, $\mathbf{v_s}$ trajectory is part of the $\mathbf{v_s^*}$ circle and voltage discontinuous problem between $[\theta_p, \quad \pi/3 - \theta_p]$ is worse. For LeeD in Figure 8.17e, it looks like MDE, but the LeeD points chosen on hexagon side are different when compared to that in MDE. For LeeH in Figure 8.17e, it is a combination of linear modulation in $[\theta_p, \quad \pi/3 - \theta_p]$ and six-step operation in $[0, \quad \theta_p]$ and $[\pi/3 - \theta_p, \quad \pi/3]$.

Modified MPE (MMPE) Method

There are two main issues in the foregoing OVM methods. One is the voltage discontinuity problem, and the other is the complexity of calculation. To achieve a better performance on these two issues, the MMPE is proposed. There are two modulation modes in this method. In Mode I, MMPE has the same implementation as in the MPE method. In Mode II, MMPE is a combination of part of the hexagon side and six-step operation. Based on the generalized formulas, the corresponding magnitude and angle can be computed as given in Table 8.2. v_1^* and θ_p can be obtained by (8.4.5) for Mode I and II, (8.4.6) for Mode I and (8.4.13) for Mode II,

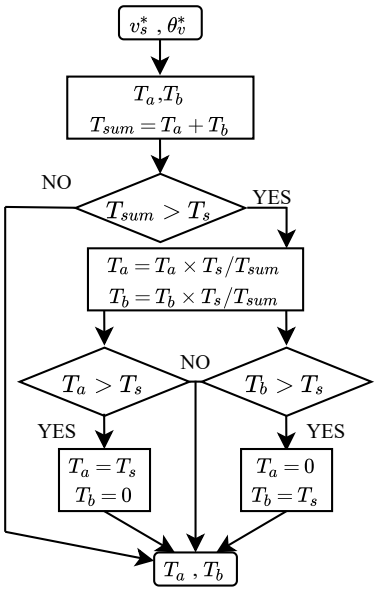


Figure 8.18: Control flowchart of the MMPE overmodulation technique.

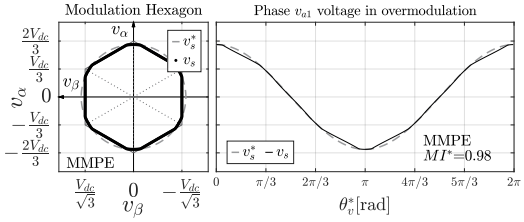
respectively.

Although it seems to be complex to implement with two modes and calculation of magnitude and angle in theory, there is rather a simple way for MMPE implementation in practice. This is demonstrated in Figure 8.18. T_a^* and T_b^* are generated in the same way as that in the linear modulation by (8.4.16) and (8.4.17). Mode I is implemented by the reduction part, and Mode II is implemented by the limitation part. Thus, the calculation burden is light.

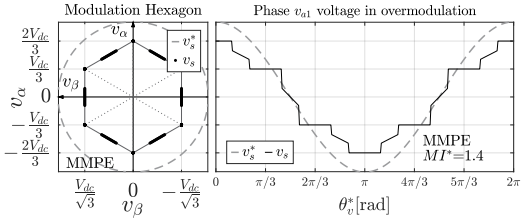
$$T_a^* = \frac{T_s\sqrt{3}v_s^*}{V_{dc}} \sin\left(\pi/3 - \theta_v^*\right) \tag{8.4.16}$$

$$T_b^* = \frac{T_s\sqrt{3}v_s^*}{V_{dc}} \sin\theta_v^* \tag{8.4.17}$$

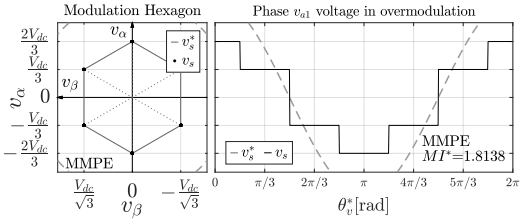
Based on Table 8.2 and Figure 8.18, the MMPE waveforms of Mode I, Mode



(a) Mode I



(b) Mode II



(c) Six-step operation

Figure 8.19: Modulation hexagon and average v_{A1} of MMPE.

II and six-step operation are shown in Figure 8.19. In Figure 8.19 (a), it is the same as MPE, whereas only the magnitude is reduced in OVM when $\mathbf{v_s}$ exceeds the modulation hexagon. In Figure 8.19 (b), six vertex point are applied to extend MI range. In Figure 8.19 (c), after the points on hexagon side are reduced to zero, phase $A1$ voltage transits into six-step operation.

8.4.2 Comparative Analysis in Generalized Form

With the generalized form, aforementioned seven methods can be compared with the aspects: output fundamental component and harmonic content, transition into six-step operation, modulation index linearization, and complexity of execution.

Fundamental Component and Harmonic Content

With Fourier analysis, actual MI and voltage THD are shown in Figures 8.20 and 8.21, respectively. The MPE has a ceiling limit of MI = 0.952. The MI of MDE

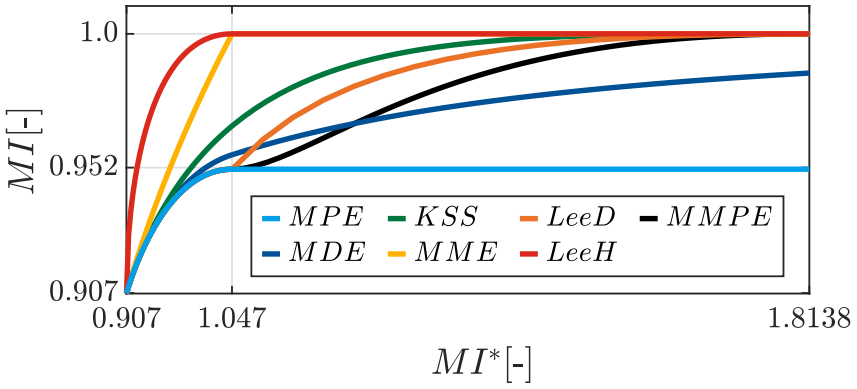


Figure 8.20: MI^* v.s. MI.

Table 8.3: v_s^*, MI^* and MI range

Method	Effective v_s^* range	Effective MI^* range	MI range
MPE	$(V_{dc}/\sqrt{3} \;\; 2V_{dc}/3]$	$(0.907 \;\; 1.047]$	$(0.907 \;\; 0.952]$
MDE	$(V_{dc}/\sqrt{3} \;\; +\infty)$	$(0.907 \;\; +\infty)$	$(0.907 \;\; 1)$
KSS	$(V_{dc}/\sqrt{3} \;\; 2\sqrt{3}V_{dc}/3]$	$(0.907 \;\; 1.8138]$	$(0.907 \;\; 1]$
$LeeD$	$(V_{dc}/\sqrt{3} \;\; 2\sqrt{3}V_{dc}/3]$	$(0.907 \;\; 1.8138]$	$(0.907 \;\; 1]$
$LeeH$	$(V_{dc}/\sqrt{3} \;\; 2V_{dc}/3]$	$(0.907 \;\; 1.047]$	$(0.907 \;\; 1]$
$MMPE$	$(V_{dc}/\sqrt{3} \;\; 2\sqrt{3}V_{dc}/3]$	$(0.907 \;\; 1.8138]$	$(0.907 \;\; 1]$

can reach 1 at $MI^* = \infty$. The maximum MI of the other five methods is 1. The relationship between MI^* and MI is summarized in Table 8.3. In Figure 8.21, the voltage THD is increasing with MI^*. The closer the method to six-step operation, the higher the voltage THD it yields. The performance of MME in terms of voltage THD is the worst, but LeeD OVM and MMPE OVM have the best performance.

Transition into Six-Step Operation

Based on Figure 8.20 and Table 8.3, there is a gap between 0.952 and 1 for MPE. If MPE is forced to transition into six-step operation, the discontinuity problem of the voltage magnitude will result in a significant current overshoot. Therefore, MPE

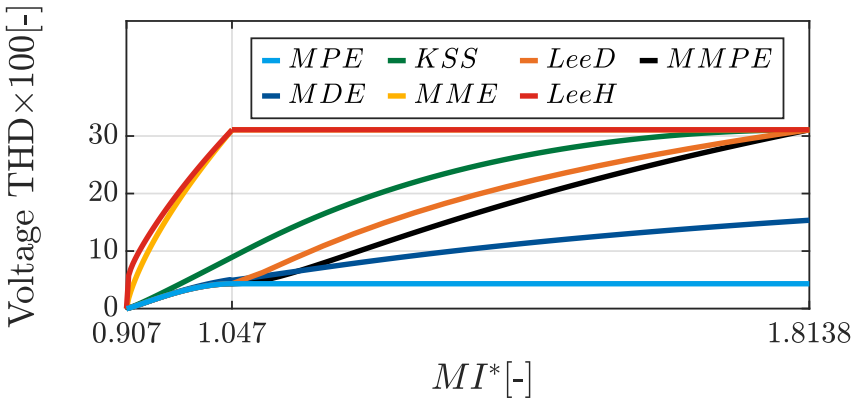


Figure 8.21: Voltage THD.

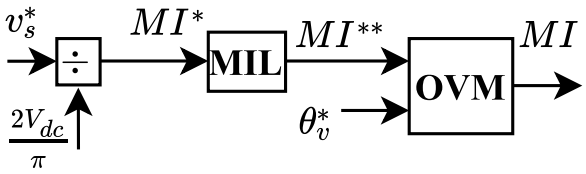


Figure 8.22: Control flow of modulation index linearization.

is unable to transition smoothly. For MDE, a large ceiling limit can be set for the transition into six-step operation, such as MI^* = 10 or MI^* = 70. Although the discontinuity problem of the voltage magnitude still exists, the current overshoot in the transition is much smaller than that in MPE. For the other five methods, the transition is smooth and continuous.

Modulation Index Linearization

In Figure 8.20, there is a non-linearity between MI^* and MI; MI is always smaller than MI^*. With modulation index linearization (MIL) shown in Figure 8.22, MI^* can be boosted to MI^{**}. Using the MIL technique, MI can be made equal to MI^* with the input of OVM as MI^{**}. As a result, the modulation gain MI/MI^* can

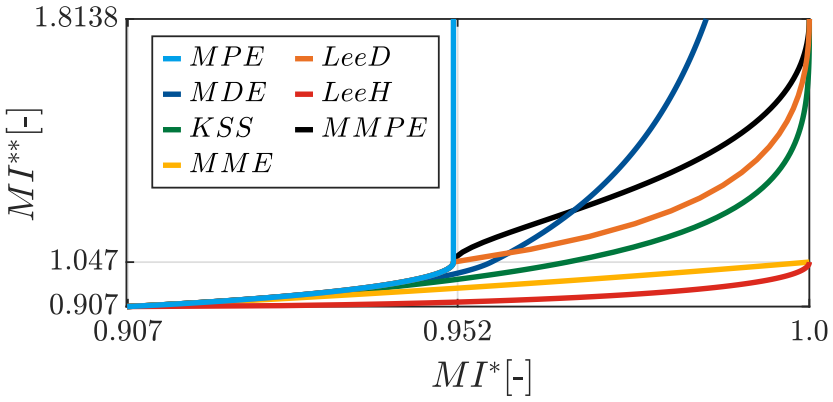


Figure 8.23: MI^* v.s. MI^{**}.

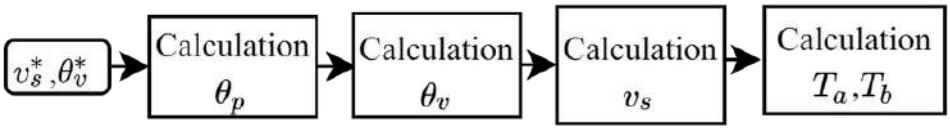


Figure 8.24: General execution flowchart of overmoulation.

be made equal to 1 for the entire modulation range. The data for MIL is obtained from Figure 8.23, which is reversed from Figure 8.20. Polynomial curve or lookup tables (LUTs) can be applied to implement MIL. From Figure 8.23, the slope of the MME curve varies slightly, and second order polynomial curve fitting is deemed sufficient. However, the slope of the other six methods varies dramatically over the entire modulation range. If polynomial curve fitting is applied in this case, a satisfactory performance is only achieved at the ninth order of polynomial curve fitting, which is computationally cumbersome. Instead, linear LUTs are more suitable for the other six methods. As such, MIL for MME is the simplest among the considered OVM methods.

Complexity of Execution

The general OVM execution process can be broken down into four steps, as shown in Figure 8.24. The first step is to calculate auxiliary theta θ_p. Based on θ_p, one base sector is divided into four segments. For each segment, v_s is set in second step and then θ_v is set by θ_v^* or θ_1 θ_5 in third step. In the last step, T_a and T_b for the two active vectors are calculated based on v_s and θ_v. The main calculation burden is on voltage magnitude and angle in Table 8.4. There is only one quantity to calculate in MME and LeeH. The execution burden is heaviest for MDE and KSS. On the other hand, MPE, LeeD and MMPE enjoy light execution burden. Considering Figure 8.18, MMPE is the simplest method to implement in practice.

Based on MI range, voltage THD, transition into six-step operation and complexity of execution, MMPE can be considered the best method.

8.4.3 Simulation Results and Discussion

The aforementioned OVM methods are validated using a 100 kW, 3 kRPM DTP-PMSM. The machine is modeled using FEA and controlled using FOC and VSD [30].

Table 8.4: Execution burden in overmodulation

Method	Voltage magnitude	voltage angle
MPE	v_1^*	θ_p
MDE	v_2^*	θ_1, θ_2, θ_p
KSS	v_2^*	θ_3, θ_4, θ_p
MME	—	θ_p
$LeeD$	v_3^*	θ_5, θ_p
$LeeH$	—	θ_p
$MMPE$	v_1^*	θ_p

The control scheme is shown in Figure 8.25. The DC-bus voltage is 350 V, and the simulation tests are conducted at a constant modulation frequency m_f of 50. The output of current controllers are d- and q-axis voltage reference $v^*_{d,q}$, and x- and y-axis voltage reference $v^*_{x,y}$. After applying the VSD transformation, two three-phase reference $v^*_{A1,B1,C1}$ and $v^*_{A2,B2,C2}$ are obtained. Two sets of $\alpha\beta$-axis voltage references are calculated using Clarke's transformation at the input of the two three-phase modulators. Finally, six-phase pulses are generated by the PWM blocks based on a duty ratio of one to six.

Open-Loop Performance

The v_{A1} waveform under the OVM techniques of MPE, MDE, KSS, MME, LeeD, and LeeH are shown in Figures 8.26 and 8.27. All six methods can be applied for DTP-PMSM drives as two modulators OVM. In order to show the difference on the same inputs, MIL is not enabled for pulses comparison of six methods.

At MI^* = 0.98, it can be noticed in Figure 8.26 that the switching pattern of MME and LeeH OVM is close to six-step operation, while the other four methods are far from six-step operation. This is attributed to the low modulation gain MI/MI^* in Figure 8.20. When MI^* is 0.98, the actual MI of MME and LeeH is very close

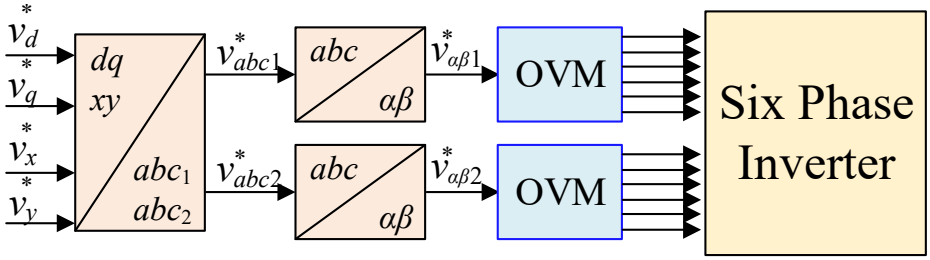
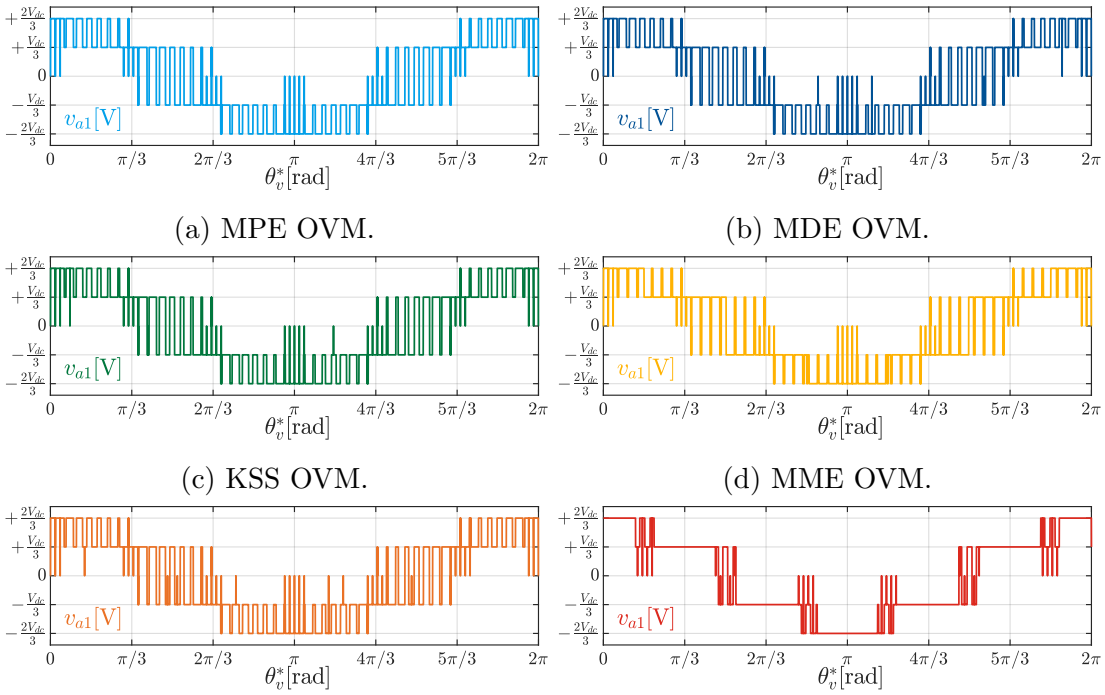


Figure 8.25: Control scheme of two modulators overmodulation in DTP-PMSM drives.



(a) MPE OVM. (b) MDE OVM.

(c) KSS OVM. (d) MME OVM.

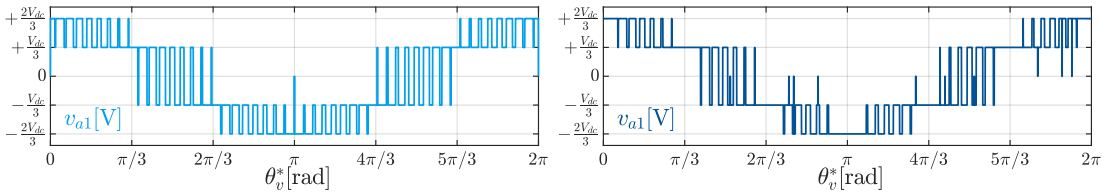
(e) LeeD OVM. (f) LeeH OVM.

Figure 8.26: Phase v_{A1} pulses at MI^* = 0.98.

to 1. For the other four methods, the difference between MI^* and actual MI is not significant at MI^* = 0.98. Also, the pulse difference among the four methods is small. Between $[2\pi/3,\ 4\pi/3]$ and $[-V_{dc}/3,\ 0]$, there are 9, 10, 11, and 12 small and narrow pulses in MPE, KSS, MDE, and LeeD OVM methods, respectively.

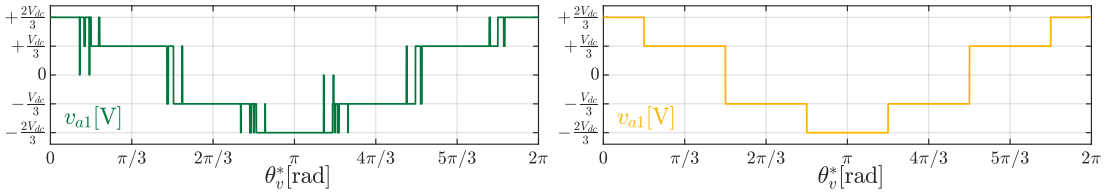
At MI^* = 1.4, LeeH and MME operate in six-step mode because MI^* is larger than the maximum effective limit of 1.047 in Table 8.3. The pulses of MPE are fixed as depicted in Figure 8.27a when MI^* exceeds the ceiling limit. The switching pattern of KSS and LeeD is close to six-step operation, while MDE is still far from six-step operation.

The v_{A1} pulses of MMPE are shown in Figure 8.28. MMPE operates normally for Mode I, Mode II and six-step operation. When MI^* is 0.98, Figure 8.28 a is



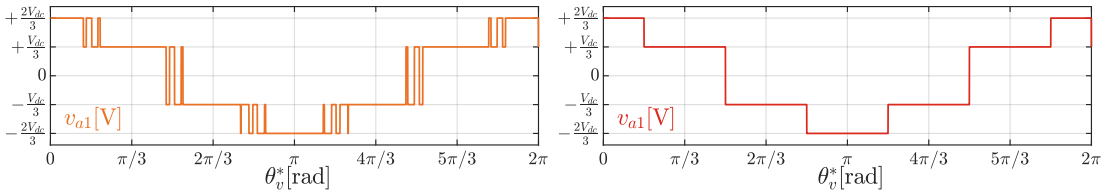
(a) MPE OVM.

(b) MDE OVM.



(c) KSS OVM.

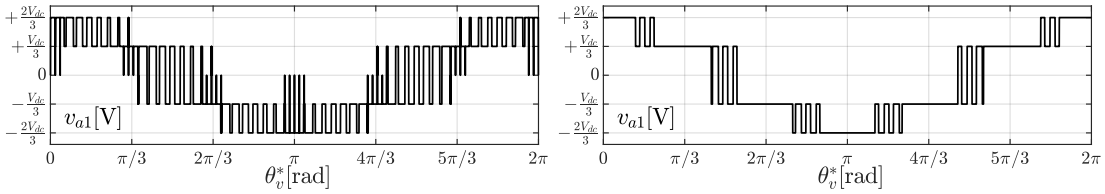
(d) MME OVM.



(e) LeeD OVM.

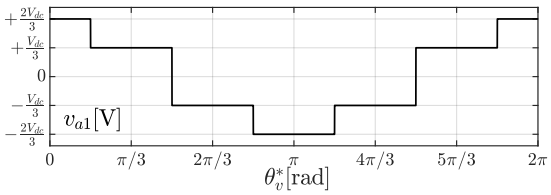
(f) LeeH OVM.

Figure 8.27: Phase v_{A1} pulses at MI^* = 1.4.



(a) Mode I: MI^* = 0.98

(b) Mode II: MI^* = 1.4



(c) Six-step operation: MI^* = 1.8138

Figure 8.28: Phase v_{A1} pulses in MMPE.

the same as Figure 8.26a. For $MI^* = 1.4$, MMPE (Figure 8.28b) is similar to LeeD (Figure 8.27e), but the pulses between $[V_{dc}/3,\ 2V_{dc}/3]$ and $[-2V_{dc}/3,\ -V_{dc}/3]$ are different. The performance of the DTP-PMSM drive, when using the different OVM methods, is investigated next.

PMSM Drive Performance

The studied OVM methods are tested over the torque-speed envelope of the DTP-PMSM drive to study their suitability for PMSM drive applications. Multiple points of operation in the OVM and FW regions are selected for this evaluation, as depicted in Figure 8.29. In OVM region in Figure 8.29, only MTPA control is applied and $MI^* \in [0.907,\ 1)$. In FW region, only FW control is applied and $MI^* \approx 1$. The VR-FW controller in Section 8.3 is adopted in this study for the DTP-PMSM drive. Since different controls are applied in those two regions, the drive performance from an OVM perspective is of a particular interest. Four metrics of drive performance are considered, namely DC-bus voltage utilization, voltage THD, current THD, and efficiency. Furthermore, the complexity of OVM methods is also considered.

The drive performance, in terms of the aforementioned metrics are recorded in

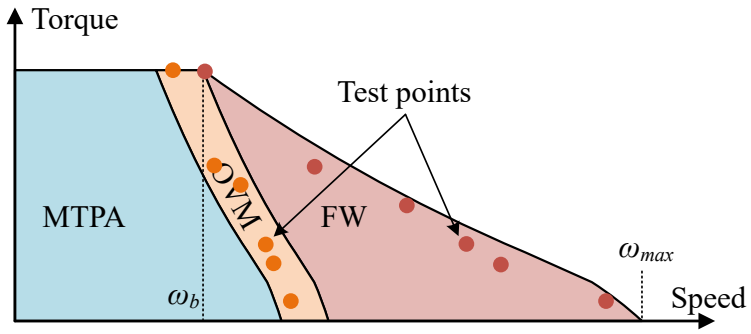


Figure 8.29: Torque-speed envelope of dual-three phase PMSM drive with OVM.

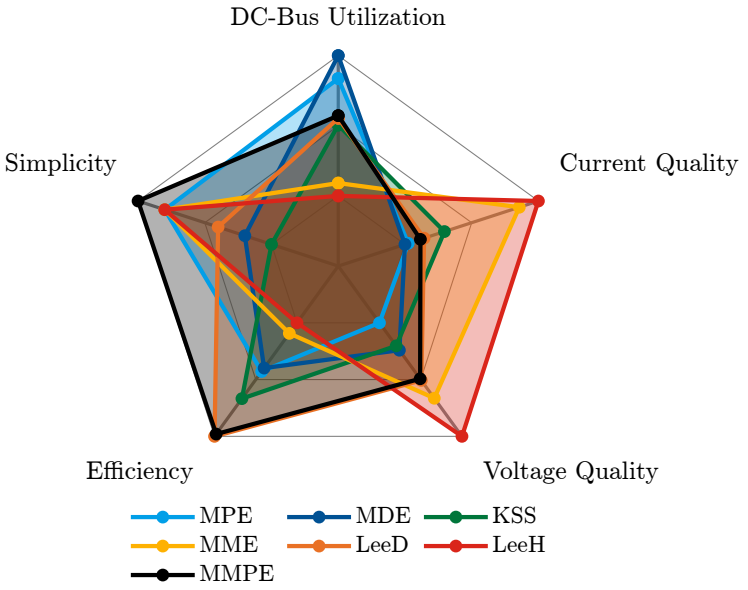


Figure 8.30: DTP-PMSM drive performance using the different OVM methods in OVM and FW regions.

steady-state for the test points highlighted in Figure 8.29. The overall performance of the DTP-PMSM drive is showcased in Figure 8.30. The values depicted in Figure 8.30 are merely the sum of the metrics at all test points. It can be observed from Figure 8.30 that MME and MMPE methods yields the highest drive efficiency, while LeeH method achieves the lowest voltage and current harmonics. Furthermore, the highest DC-bus voltage utilization by the PMSM drive was achieved when employing MDE and MPE methods. Due to the high degrees of freedom pertaining to performance metrics, drive control regions and number of test points, a decision matrix is sought to streamline the selection process of the optimum OVM method. A weighting factor is assigned to the drive performance metrics, with efficiency given the heaviest weight and DC-bus voltage utilization given the lightest weight. Voltage and current THD are assigned equal weights. Note that weight assignment is solely dependent on the designer and the desired drive performance. Based on the weighted-factor sum,

in addition to OVM implementation complexity, MMPE is deemed the best OVM method for the DTP-PMSM drive, followed by LeeD. On the other hand, MPE and MDE scored the lowest.

8.5 Summary

This chapter tackled the control aspects related to six-phase electric motor drives. Firstly, a comparative study for xy-current suppression, involving different controllers implemented in different reference frames, was conducted. It was found that the PR controller implemented in the asynchronous frame achieves the best suppression. Secondly, an adaptive voltage regulation flux-weakening controller that uses an adaptive control law to maintain stable performance in the deep flux-weakening region was proposed. The proposed controller was validated through simulations, and the obtained results demonstrated its superior performance compared to the non-adaptive flux-weakening controller. Thirdly, a comparative analysis of seven different overmodulation methods for DTP-PMSM drives was carried out. A four segmented formulae of the generalized form was presented based on the specific magnitude and angle calculation of the reference voltage vector. The comparison of the different overmodulation methods in terms of fundamental component and harmonic content, transition into six-step operation, modulation index linearization, and complexity of execution showed that MMPE yields the best DTP-PMSM drive performance. The preliminary validation was carried out in simulation.

Chapter 9

Conclusions and Future Work

9.1 Conclusions

This thesis focused on making the case for SiC-based six-phase traction inverters for automotive applications. To achieve this goal, this thesis adopted a two-pronged approach consisting of the theoretical and technological background covered in Chapters 1–5 and the applied design and development presented in Chapters 6–8. By integrating these two approaches, this thesis offers a well-rounded perspective on six-phase traction inverters, with a robust theoretical foundation supported by practical real-world applications.

The fundamentals of multiphase inverters, including modeling, topologies, switch selection, DC-capacitor sizing, modulation strategies, and future trends, were reviewed. The advantages of multiphase inverters were benchmarked against those of their conventional three-phase counterparts. It was found that multiphase inverters can achieve reduced cabling costs and smaller DC capacitors with greater control and fault-tolerant capabilities. However, they require an increased number of sensors and

gate-driver circuitry. Six-phase inverters were found to have the best trade-off among multiphase inverters in terms of per-phase power requirement and modularity as well as complexity and cost premium.

The use of SiC devices in multiphase inverters represents the intersection of two major trends in electrified powertrains. However, there has been a lack of thorough technological assessments of SiC-based multiphase inverters. Therefore, this thesis presents a case study of SiC-based multiphase inverters, which considers both quantitative and qualitative aspects of these systems in comparison to SiC-based three-phase traction inverters. The study found that multiphase traction inverters can complement the low current rating limitation of SiC devices, thanks to their lower per-phase current requirements. Specifically, when sized based on the minimum per-leg current handling, six-phase inverters employ the same total number of discrete devices as three-phase inverters, while maintaining the same efficiency. Furthermore, they reduce the capacitor volume and improve modularity and fault-tolerant capabilities. Given the competitiveness of six-phase systems among all multiphase systems, the scope of this thesis was narrowed to the former henceforth.

To further examine the benefits of using SiC devices in six-phase inverters compared to conventional Si IGBTs, a vehicle-level assessment was conducted. The efficiency of Si- and SiC-based 100 kW six-phase traction inverters in an 800 V powertrain was analyzed across the torque–speed envelope of an automotive-grade motor. The resulting data were then incorporated into the EV model. The analysis showed that the SiC-based six-phase inverter offers an 8% improvement in vehicle mileage and fuel economy compared to its Si-based counterpart.

The final theoretical contribution of this thesis involved the analysis of the DC-bus current and voltage ripples in six-phase inverters. For the first time, analytical formulas were developed to evaluate the voltage and current stresses on the DC-capacitor in six-phase inverters that supply both symmetric and asymmetric loads. The accuracy of the derived formulas was validated through simulations and experimental tests. Building upon these analytical formulas, this thesis proposed simple capacitor-sizing rules for symmetric and asymmetric six-phase VSIs. Additionally, the harmonic spectra of the DC-capacitor current in six-phase inverters were analyzed to identify the underlying reason for the reduction in the DC-bus current stress when compared to three-phase systems. It was found that the spatial distribution of the additional three phases in the six-phase inverters leads to the cancellation of the dominant carrier-sideband harmonics, resulting in a reduced current stress on the DC-capacitor.

Turning to the applied design and development aspect of this thesis, the foregoing fundamentals and theory of six-phase inverter design and operation were utilized to deliver a 100 kW/ 800 V SiC-based six-phase traction inverter, named MARC100. The proposed holistic design addressed the advantages and disadvantages inherent in a six-phase inverter. More specifically, a multi-objective optimization algorithm was proposed to find the most suitable capacitor bank, achieving the maximum reduction factor in the DC-capacitor size in six-phase systems. Similarly, cabling cost reduction was achieved by careful sizing of the AC cables used in the design. On the other hand, monolithic current sensor ICs were integrated into the power PCB to eliminate the need for bulky current sensors, thus effectively mitigating the drawback of the increased number of current sensors. The resultant inverter design from the proposed

electrical-thermal-mechanical design methodology was prototyped and experimentally tested. The peak power density of the prototype inverter is 70 kW/L, demonstrating a compact design. The MARC100 was made suitable for symmetric and asymmetric motor drives.

Finally, a traction inverter is used to power and control the electric drive motor. Accordingly, the control aspects of six-phase drives were investigated. Motor modeling, current control, and operation in all regions of the torque–speed envelope were analyzed. Special attention was given to operation at high speeds, where flux-weakening and overmodulation techniques are usually required to maximize the output power of the traction inverter. An adaptive flux-weakening technique was proposed to improve the dynamic performance of an electric drive operating at high speeds. The resulting increase in DC-bus voltage utilization was verified by simulations. Additionally, a comparative analysis of six existing overmodulation techniques, in addition to the proposed modified technique, is presented. The proposed MMPE overmodulation strategy yielded the best drive performance.

Overall, this thesis aimed to contribute to the body of knowledge on SiC-based six-phase traction inverters and provide a foundation for future research and development. The combination of theoretical and practical components was essential in providing a thorough and complete understanding of the topic, which can facilitate future research and advancements in the field.

9.2 Future Work

While this thesis has made significant contributions to the field of SiC-based six-phase traction inverters for automotive applications, there are several potential direction for future research that can push the boundaries of this technology and expand their potential benefits. Such directions include:

1. As the electrified powertrain field rapidly advances, scaling up the MARC100 design to 300 kW or 500 kW could increase the appeal of the SiC-based six-phase traction inverter. The ability to operate at such power levels opens up new opportunities for utilizing these inverters in light- to medium-duty trucks and buses.

2. In addition to the inverter losses, the six-phase motor losses should be analyzed as well. This will provide an overall powertrain efficiency benchmark against the conventional three-phase electric motor drives.

3. The lessons learned from the first generation of the MARC100 can be leveraged in developing a second generation that is more efficient and power dense. The prototyped inverter had provisions to enable easy testing and debugging, such as mating connector headers and receptacles between the PCBs. By directly soldering the power and gate driver PCBs, an 11% power density increase can be achieved. Besides, investigating the integration of the gate driver and control boards in a single board can further improve the power density and reduce manufacturing cost and moving parts.

4. More elaborate mechanical manufacturing and assembly techniques can be incorporated to improve the rugdness of the MARC100. For example, welding

techniques for the heat sink can reduce the risk of leakage encountered in the testing. Additionally, the investigation of more advanced heat sink designs, such as the staggered fin pin design, could yield a more efficient mechanical design and packaging of the MARC100.

5. The electromagnetic compatibility of the MARC100 was not explored given the limited time and resources at hand. Investigation of common mode and differential mode noises and their mitigation is imperative for commercial implementation.

6. Exploring advanced control and modulation techniques, such as model predictive control and space vector modulation, may further improve the performance of the SiC-based six-phase traction inverter. Additionally, the implementation of these techniques in hardware using digital signal processors or field-programmable gate arrays can be investigated to determine their feasibility and practicality in real-world applications.

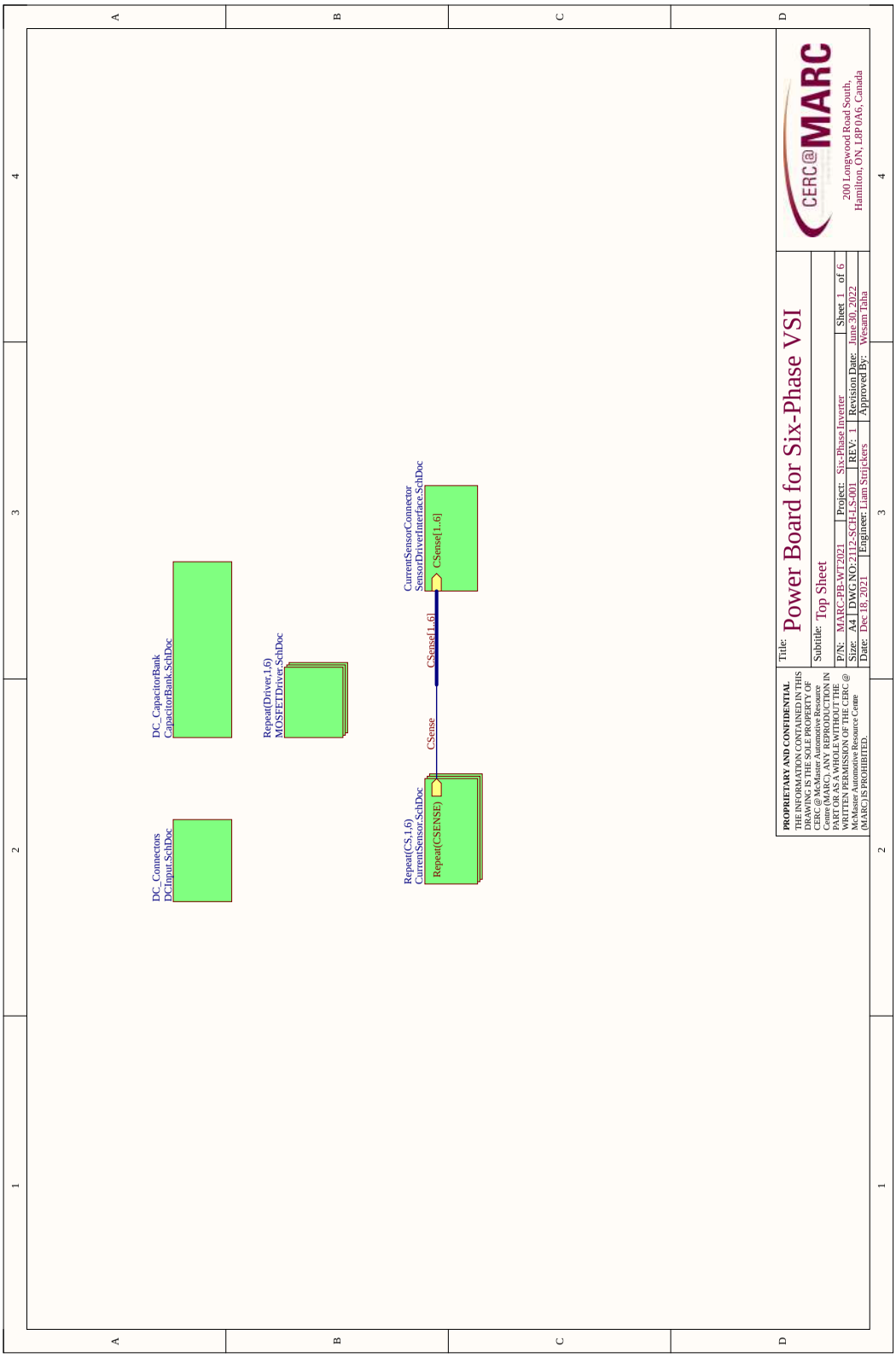
In conclusion, the suggested future work will pave the way for further advancements in the field of electrified powertrains and contribute to the development of more efficient and reliable powertrain systems.

Appendix A

Schematic Diagrams

This appendix includes the schematic diagrams of the designed circuits as part of the manufactured PCBs for the six-phase SiC-based inverter or as part of the built testing rig. Specifically, it includes:

1. Power PCB
2. Gate driver PCB
3. Control interface PCB
4. Low voltage connector interface PCB
5. Pre-charge/discharge and safety circuit


DC_CapacitorBank
CapacitorBank.SchDoc
Repeat(Driver,1,6)
MOSFETDriver.SchDoc
DC_Connectors
DCInput.SchDoc
CurrentSensorConnector
SensorDriverInterface.SchDoc
CSense[1..6]
CSense[1..6]
CSense
Repeat(CS,1,6)
CurrentSensor.SchDoc
Repeat(CSENSE)
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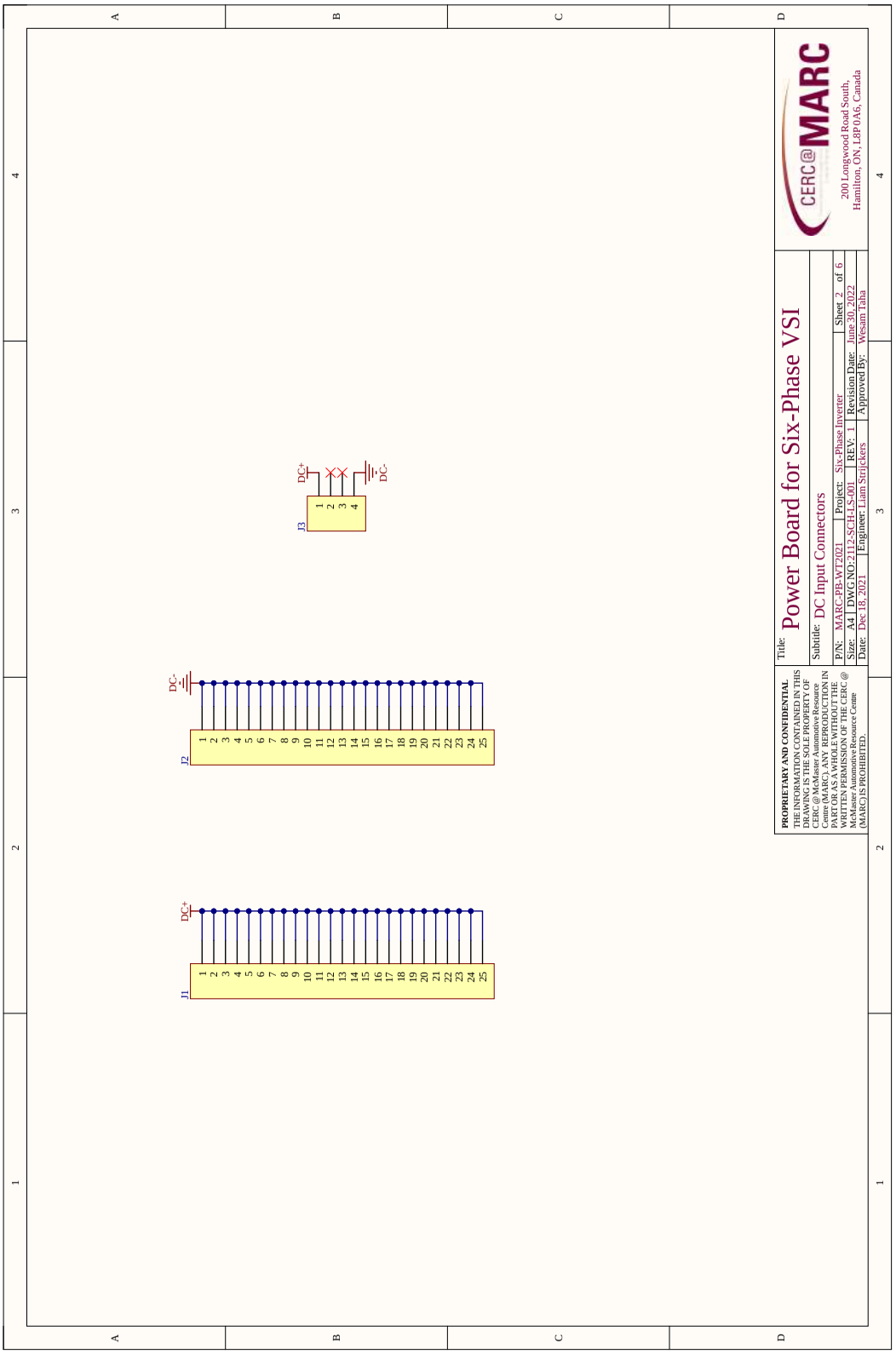
Title: Power Board for Six-Phase VSI
Subtitle: Top Sheet
P/N: MARC-PB-WT2021
Project: Six-Phase Inverter
Sheet 1 of 6
Size: A4
DWG NO: 2112-SCH-L-S-001
REV: 1
Revision Date: June 30, 2022
Date: Dec 18, 2021
Engineer: Liam Strijckers
Approved By: Wesam Taha
CERC@MARC
200 Longwood Road South,
Hamilton, ON, L8P 0A6, Canada


DC+
DC-
J3
DC-
J2
DC+
J1
Title: Power Board for Six-Phase VSI
Subtitle: DC Input Connectors
P/N: MARC-PB-WT2021
Project: Six-Phase Inverter
Sheet 2 of 6
Size: A4
DWG NO: 2112-SCH-LS-001
REV: 1
Revision Date: June 30, 2022
Date: Dec 16, 2021
Engineer: Liam Strickers
Approved By: Wesam Taha
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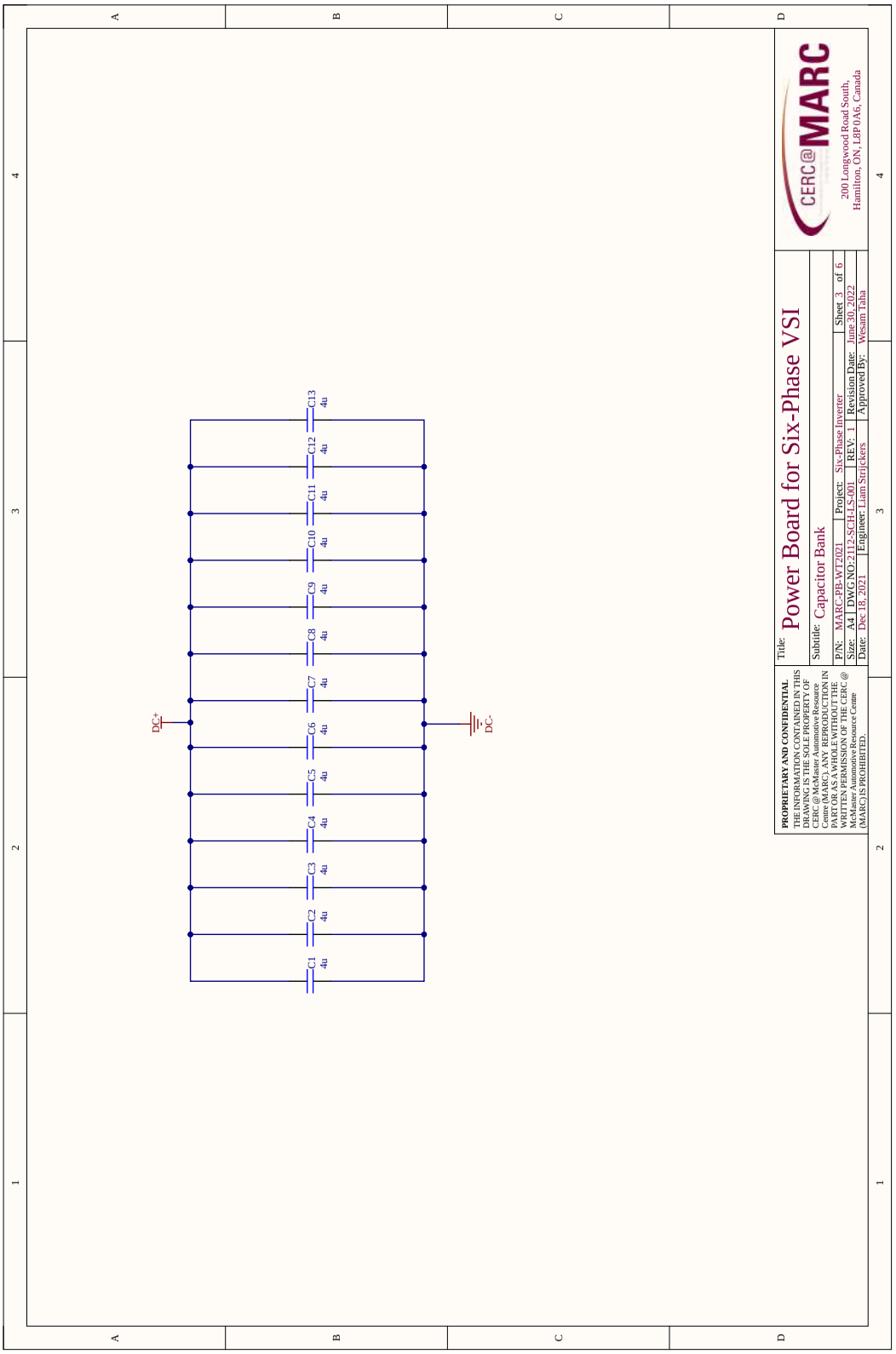
DC+
DC-
C1 4u
C2 4u
C3 4u
C4 4u
C5 4u
C6 4u
C7 4u
C8 4u
C9 4u
C10 4u
C11 4u
C12 4u
C13 4u
Title: Power Board for Six-Phase VSI
Subtitle: Capacitor Bank
P/N: MARC_PB_WT2021
Project: Six-Phase Inverter
Sheet 3 of 6
Size: A4
DWG NO: 2112-SCH-LS-001
REV: 1
Revision Date: June 30, 2022
Date: Dec 18, 2021
Engineer: Liam Strijckers
Approved By: Wesam Taha
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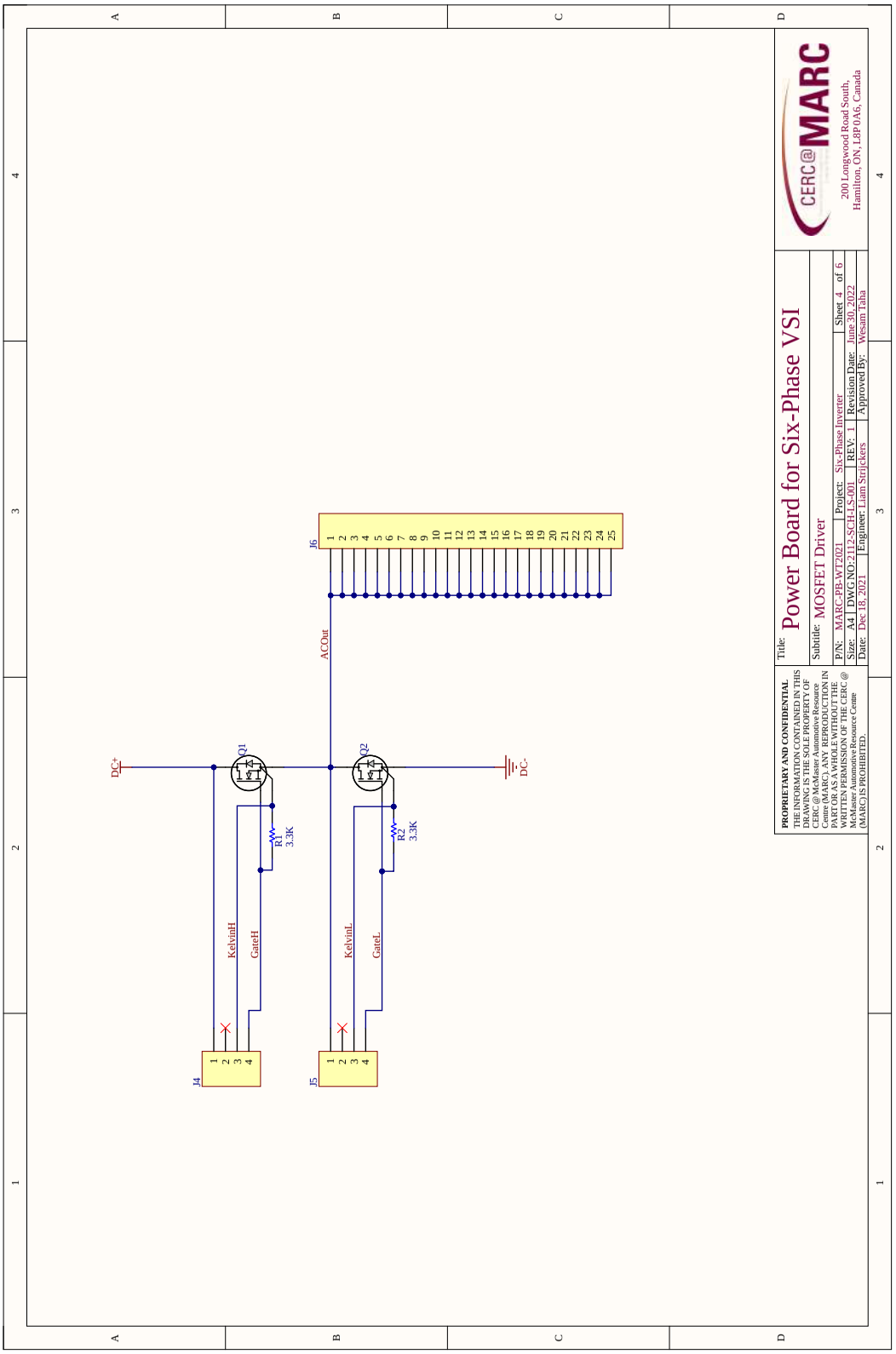
Power Board for Six-Phase VSI
MOSFET Driver
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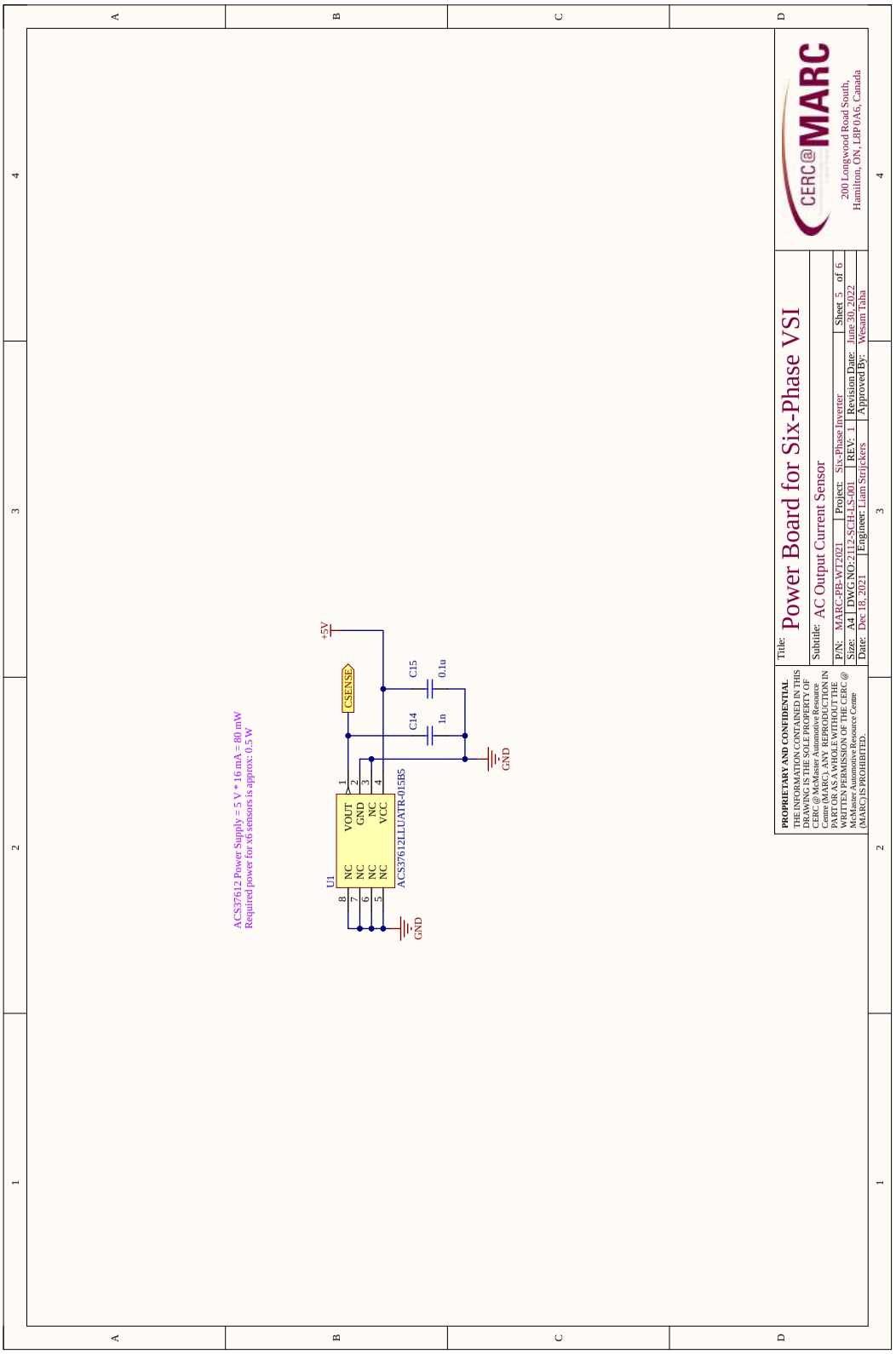
Title:
Subtitle:
P/N: MARC_PB_WT2021
Project: Six-Phase Inverter
Sheet 4 of 6
Size: A4
DWG NO: 2112-SCH-LS-001
REV: 1
Revision Date: June 30, 2022
Date: Dec 16, 2021
Engineer: Liam Strickers
Approved By: Wesam Taha
J6
ACOut
DC+
DC-
Q1
Q2
R1
3.3K
R2
3.3K
KelvinH
GateH
KelvinL
GateL
J4
J5


ACS37612 Power Supply = 5 V * 16 mA = 80 mW
Required power for x6 sensors is approx: 0.5 W
+5V
CSENSE
C15
0.1u
C14
1n
GND
U1
NC
NC
NC
NC
VOUT
GND
NC
VCC
ACS37612LLUATR-015B5
GND
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Title: Power Board for Six-Phase VSI
Subtitle: AC Output Current Sensor
P/N: MARC-PB-WT2021
Project: Six-Phase Inverter
Sheet 5 of 6
Size: A4
DWG NO: 2112-SCH-LS-001
REV: 1
Revision Date: June 30, 2022
Date: Dec 18, 2021
Engineer: Liam Strijckers
Approved By: Wesam Taha
CERC@MARC
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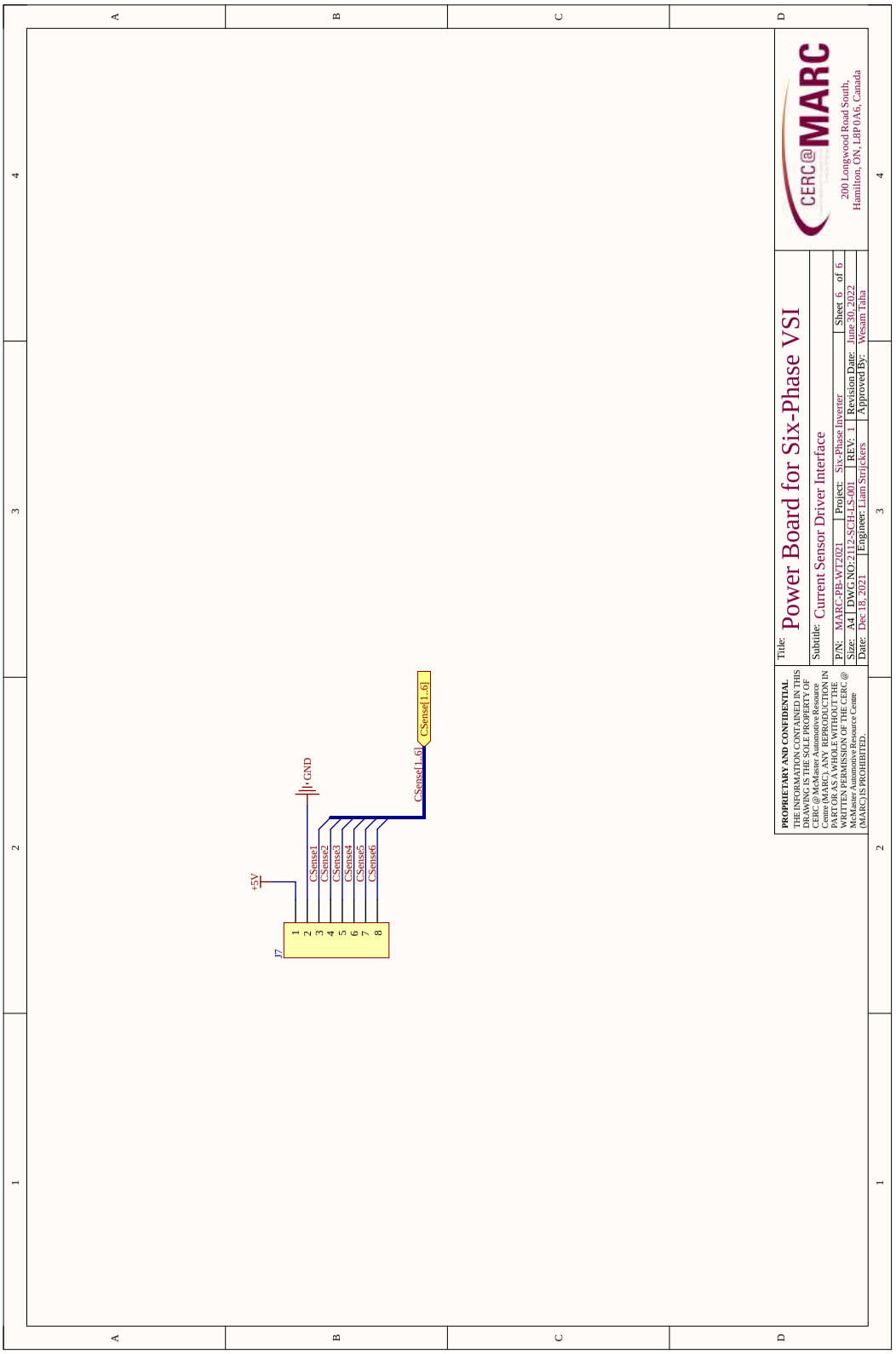
Hamilton, ON, L8P 0A6, Canada


A
B
C
D
1
2
3
4
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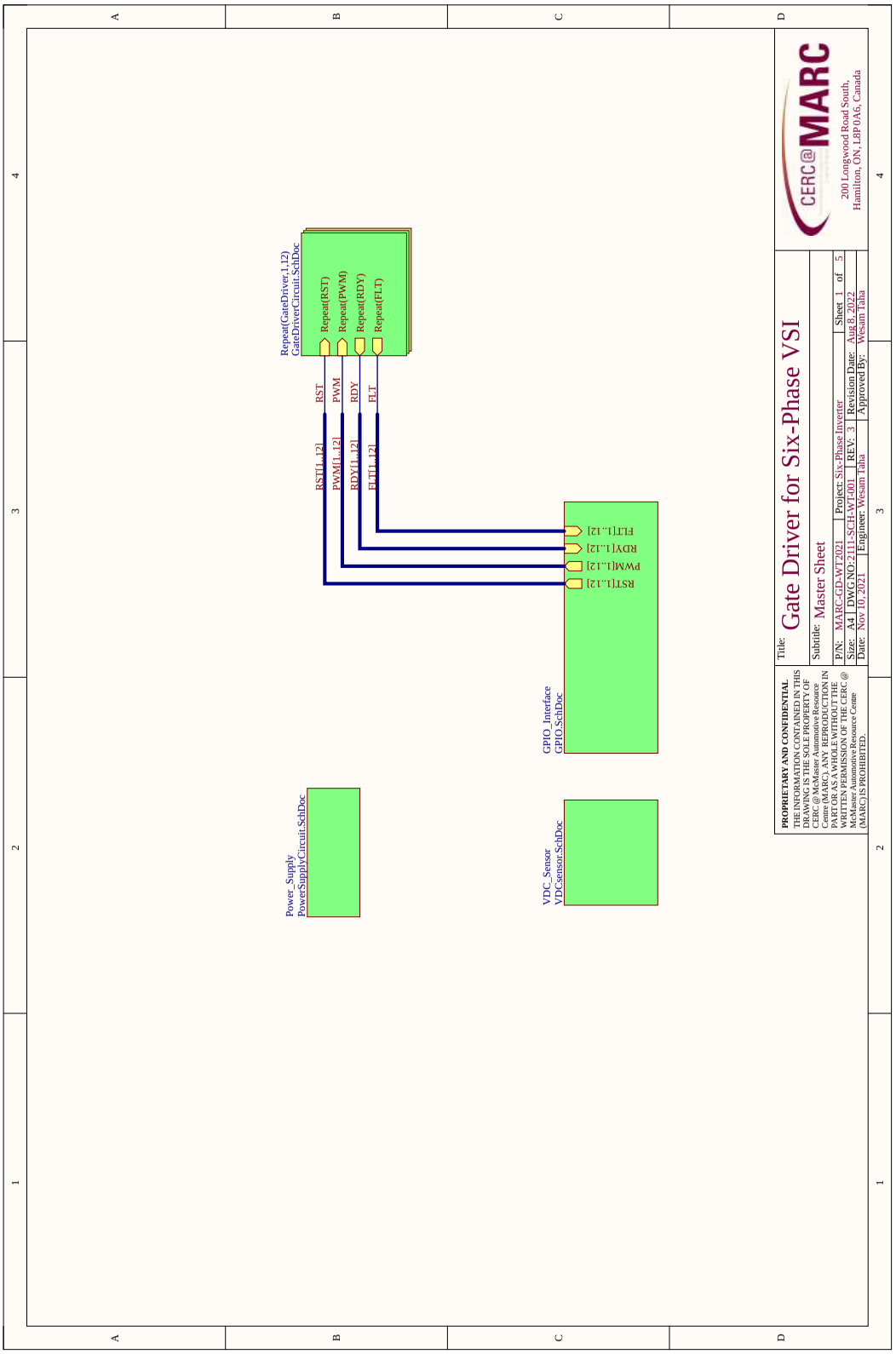
Title: Power Board for Six-Phase VSI
Subtitle: Current Sensor Driver Interface
P/N: MARC_PB_WT2021
Project: Six-Phase Inverter
Sheet 6 of 6
Size: A4
DWG NO: 2112-SCH-LS-001
REV: 1
Revision Date: June 30, 2022
Date: Dec 16, 2021
Engineer: Liam Strijckers
Approved By: Wesam Taha
CERC@MARC
200 Longwood Road South,
Hamilton, ON, L8P 0A6, Canada
+5V
GND
CSense1
CSense2
CSense3
CSense4
CSense5
CSense6
CSense[1..6]
CSense4[1..6]
J7
1
2
3
4
5
6
7
8


Repeat(GateDriver,1,12)
GateDriverCircuit.SchDoc
Repeat(RST)
Repeat(PWM)
Repeat(RDY)
Repeat(FLT)
RST
PWM
RDY
FLT
RST[1..12]
PWM[1..12]
RDY[1..12]
FLT[1..12]
FLT[1..12]
RDY[1..12]
PWM[1..12]
RST[1..12]
GPIO_Interface
GPIO.SchDoc
Power_Supply
PowerSupplyCircuit.SchDoc
VDC_Sensor
VDCsensor.SchDoc
CERC@MARC
200 Longwood Road South,
Hamilton, ON, L8P 0A6, Canada
Title: Gate Driver for Six-Phase VSI
Subtitle: Master Sheet
P/N: MARC-GD-WT2021
Project: Six-Phase Inverter
Sheet 1 of 5
Size: A4
DWG NO: 2111-SCH-WT-001
REV: 3
Revision Date: Aug 8, 2022
Date: Nov 10, 2021
Engineer: Wesam Taha
Approved By: Wesam Taha
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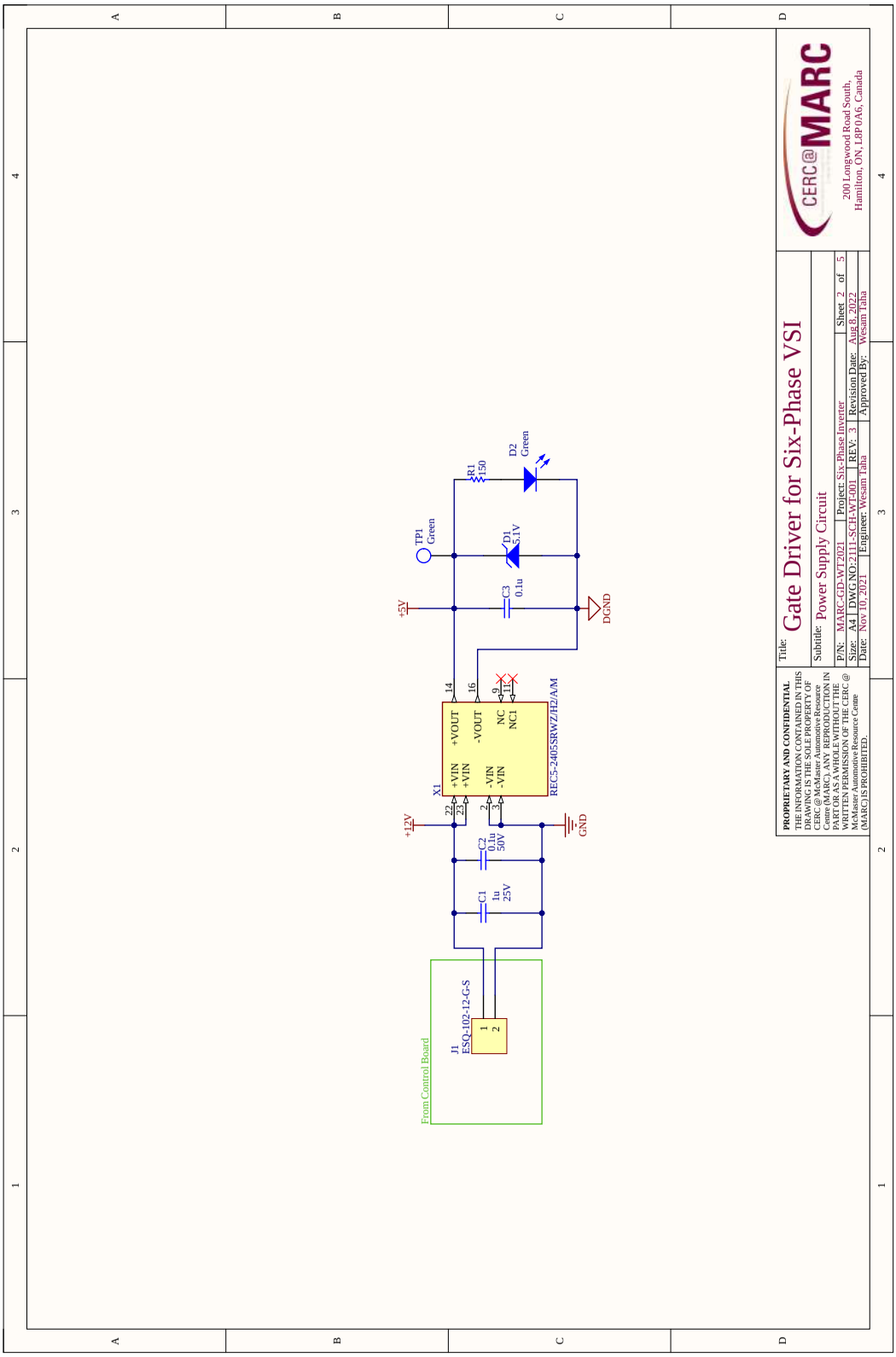
Title: Gate Driver for Six-Phase VSI
Subtitle: Power Supply Circuit
P/N: MARC-GD-WT2021
Project: Six-Phase Inverter
Sheet 2 of 5
Size: A4
DWG NO: 2111-SCH-wT-001
REV: 3
Revision Date: Aug 8, 2022
Date: Nov 10, 2021
Engineer: Wesam Taha
Approved By: Wesam Taha
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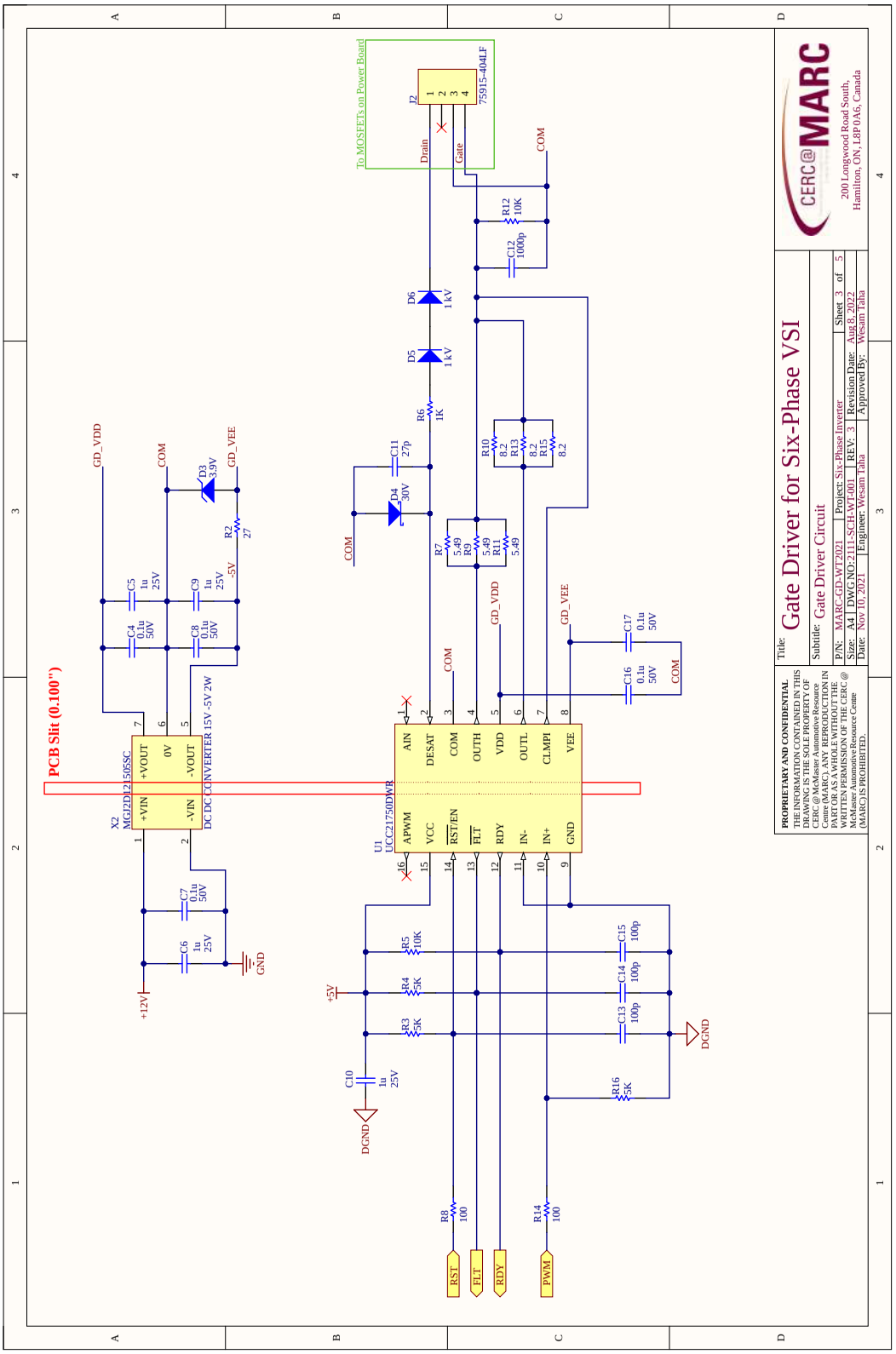
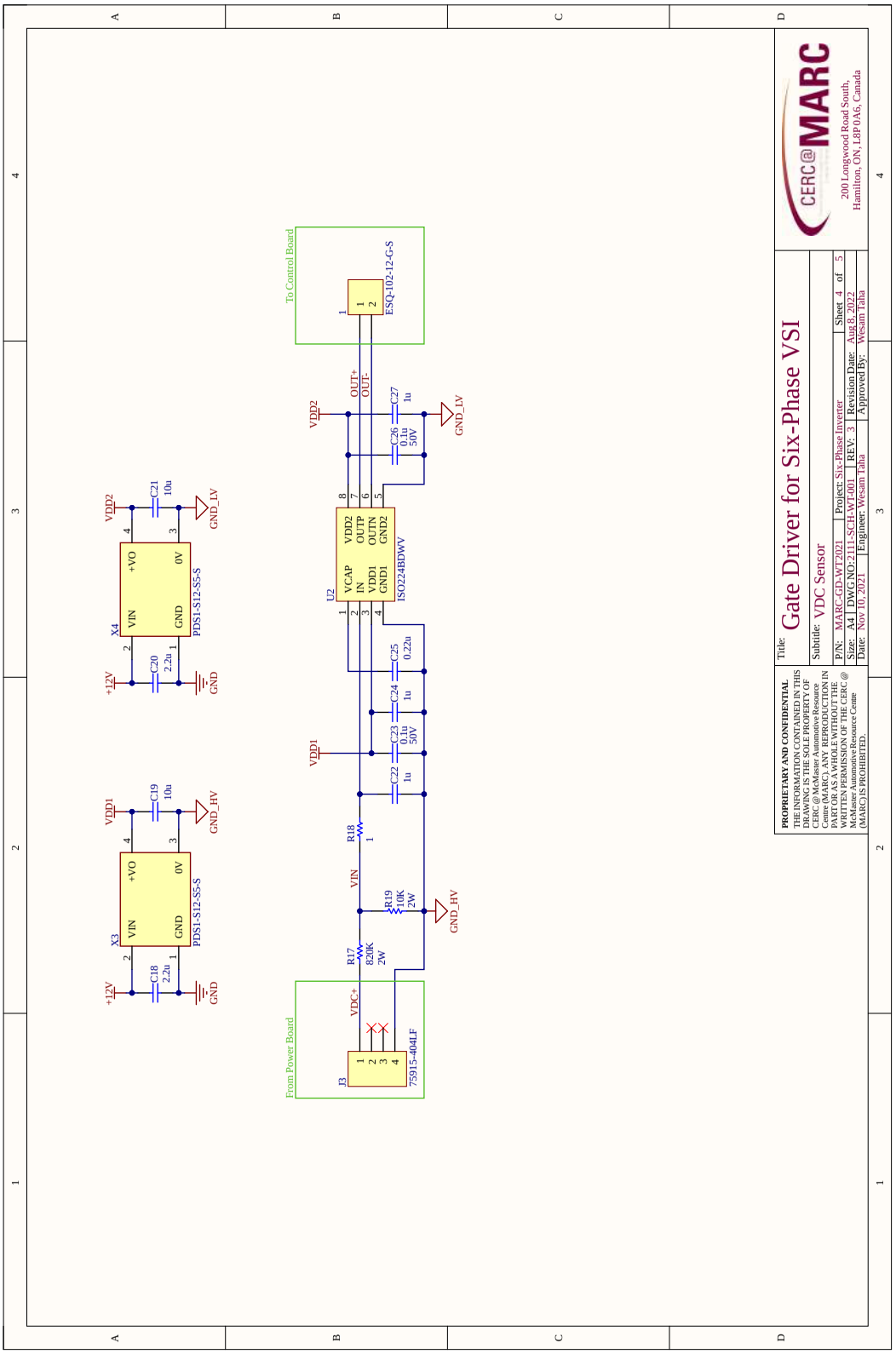
TP1 Green
R1 150
D2 Green
D1 5.1V
C3 0.1u
+5V
DGND
X1
REC5-2405SRWZ/H2/A/M
+VIN
+VIN
-VIN
-VIN
+VOUT
-VOUT
NC
NC1
+12V
GND
C2 0.1u 50V
C1 1u 25V
J1 ESQ-102-12-G-S
From Control Board


Gate Driver for Six-Phase VSI
Gate Driver Circuit
CERC@MARC
200 Longwood Road South,
Hamilton, ON, L8P 0A6, Canada
To MOSFETs on Power Board
PCB Slit (0.100")
DC-DC CONVERTER 15V -5V 2W
UCC21750DWR
GD_VDD
GD_VEE
COM
DGND
GND
+12V
+5V
RST
FLT
RDY
PWM


Gate Driver for Six-Phase VSI
Subtitle: VDC Sensor
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Hamilton, ON, L8P 0A6, Canada
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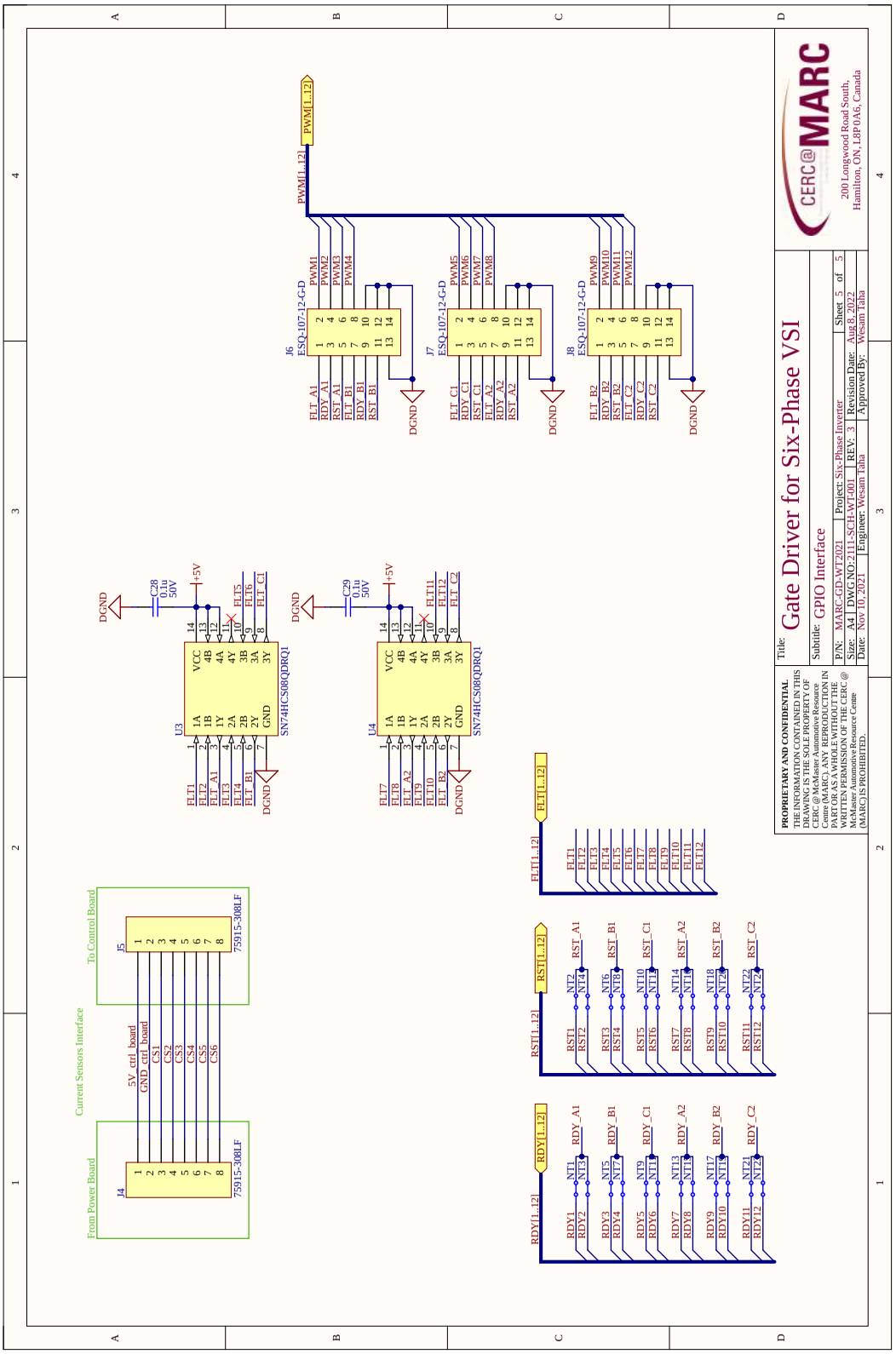
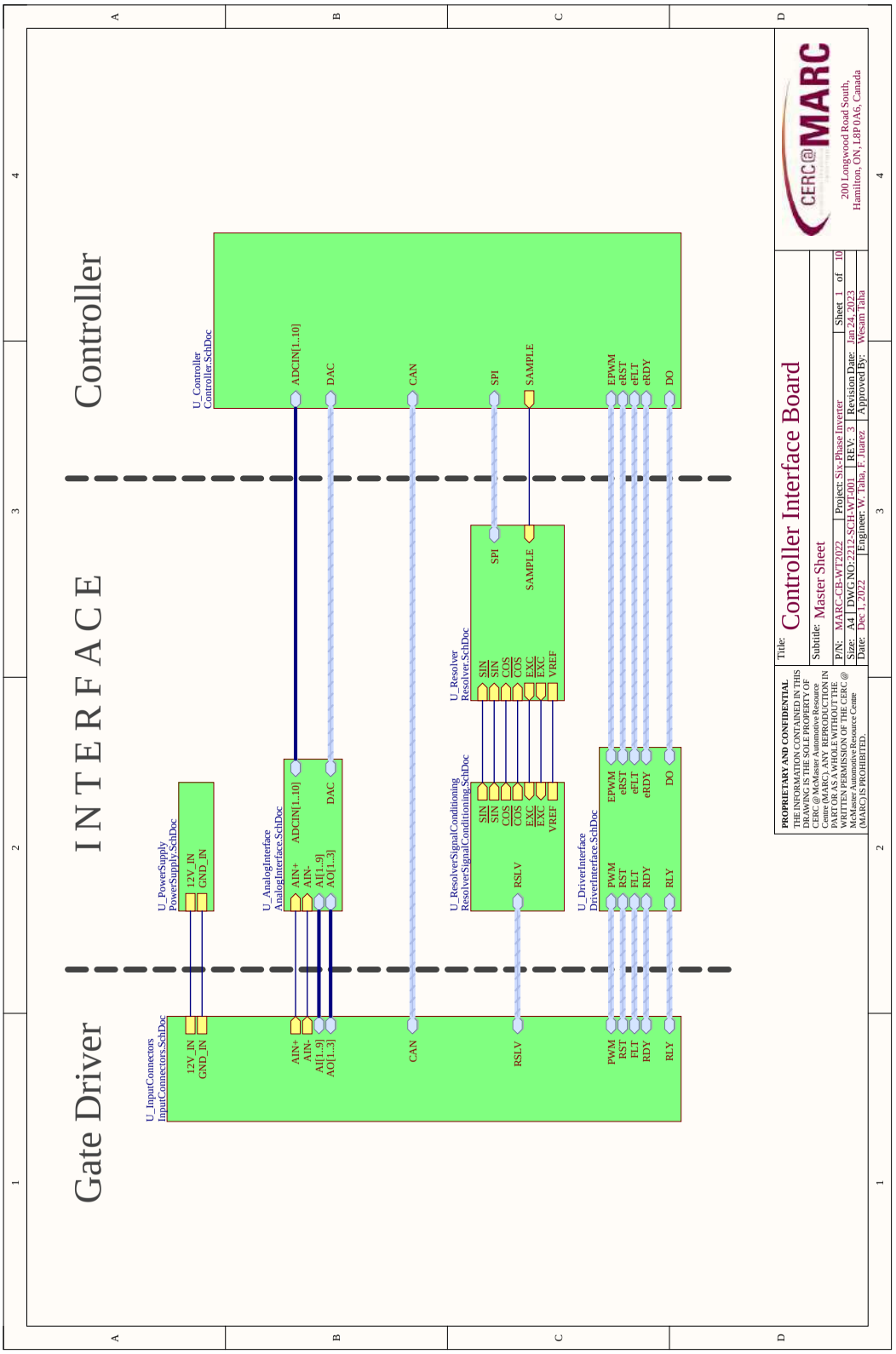
P/N: MARC-GD-WT2021
Project: Six-Phase Inverter
Sheet 4 of 5
Size: A4
DWG NO: 2111-SCH-WT-001
REV: 3
Revision Date: Aug 8, 2022
Date: Nov 10, 2021
Engineer: Wesam Taha
Approved By: Wesam Taha
From Power Board
To Control Board
J3
75915-404LF
ESQ-102-12-G-S
VDC+
VIN
R17
820K
2W
R18
1
R19
10K
2W
GND_HV
U2
ISO224BDWV
VCAP
IN
VDD1
GND1
VDD2
OUTP
OUTN
GND2
OUT+
OUT-
VDD1
VDD2
GND_LV
C22
1u
C23
0.1u
50V
C24
1u
C25
0.22u
C26
0.1u
50V
C27
1u
X3
X4
PDS1-S12-S5-S
VIN
+VO
GND
0V
+12V
GND
C18
2.2u
C19
10u
C20
2.2u
C21
10u


Gate Driver for Six-Phase VSI
GPIO Interface
CERC@MARC
200 Longwood Road South,
Hamilton, ON, L8P 0A6, Canada
PROPRIETARY AND CONFIDENTIAL
P/N: MARC-GD-WT2021
Project: Six-Phase Inverter
Sheet 5 of 5
Size: A4
DWG NO: 2111-SCH-wT-001
REV: 3
Revision Date: Aug 8, 2022
Date: Nov 10, 2021
Engineer: Wesam Taha
Approved By: Wesam Taha
PWM[1..12]
ESQ-107-12-G-D
SN74HCS08QDRQ1
5V_ctrl_board
GND_ctrl_board
75915-308LF
From Power Board
To Control Board
Current Sensors Interface


Gate Driver
INTERFACE
Controller
U_InputConnectors
InputConnectors.SchDoc
12V_IN
GND_IN
AIN+
AIN-
AI[1..9]
AO[1..3]
CAN
RSLV
PWM
RST
FLT
RDY
RLY
U_PowerSupply
PowerSupply.SchDoc
U_AnalogInterface
AnalogInterface.SchDoc
ADCIN[1..10]
DAC
U_ResolverSignalConditioning
ResolverSignalConditioning.SchDoc
U_Resolver
Resolver.SchDoc
SIN
COS
EXC
VREF
SPI
SAMPLE
U_DriverInterface
DriverInterface.SchDoc
EPWM
eRST
eFLT
eRDY
DO
U_Controller
Controller.SchDoc
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Title: Controller Interface Board
Subtitle: Master Sheet
P/N: MARC-CB-WT2022
Project: Six-Phase Inverter
Sheet 1 of 10
Size: A4
DWG NO: 2212-SCH-WT-001
REV: 3
Revision Date: Jan 24, 2023
Date: Dec 1, 2022
Engineer: W. Taha, F. Ibarez
Approved By: Wesam Taha
CERC@MARC
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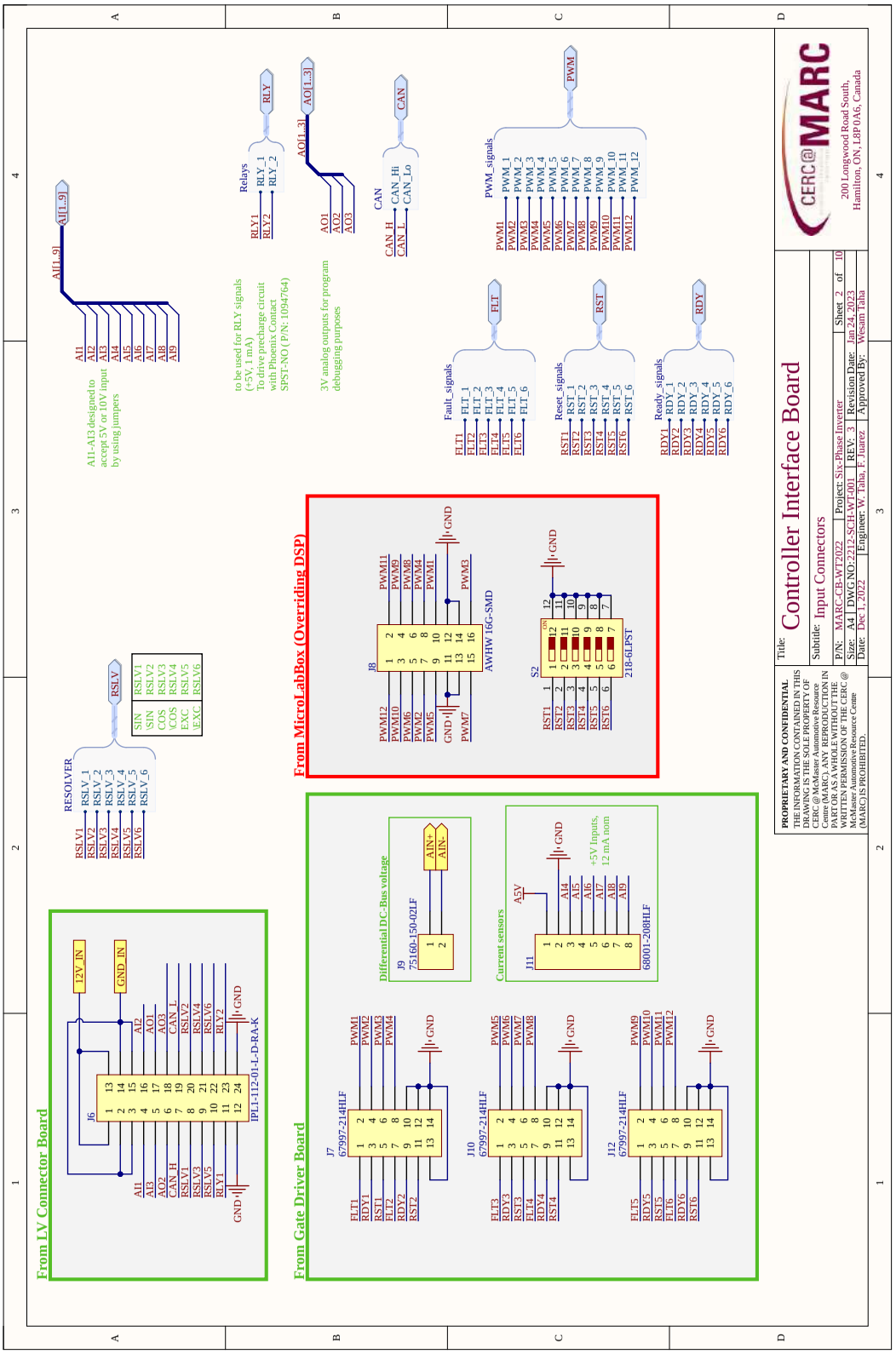
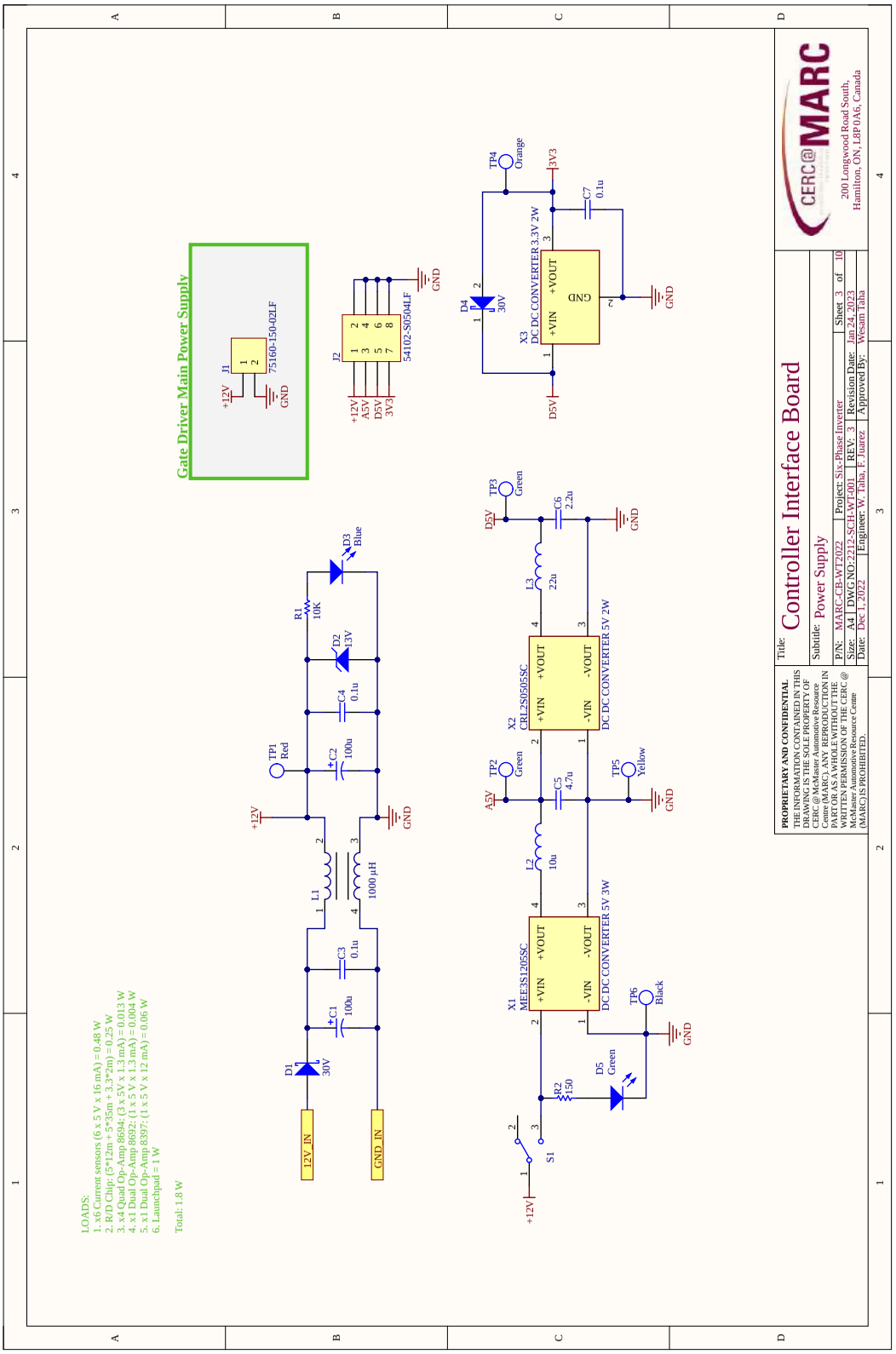
Hamilton, ON, L8P 0A6, Canada


Controller Interface Board
Input Connectors
From LV Connector Board
From Gate Driver Board
From MicroLabBox (Overriding DSP)
RESOLVER
Relays
CAN
Fault_signals
Reset_signals
Ready_signals
PWM_signals
Differential DC-Bus voltage
Current sensors
CERC@MARC
200 Longwood Road South, Hamilton, ON, L8P 0A6, Canada


Gate Driver Main Power Supply
J1
75160-150-02LF
+12V
GND
J2
54102-S0504LF
+12V
A5V
D5V
3V3
GND
TP4
Orange
3V3
D4
30V
X3
DC DC CONVERTER 3.3V 2W
+VIN
+VOUT
GND
C7
0.1u
D5V
TP3
Green
C6
2.2u
L3
22u
X2
CRL-2S0505SC
DC DC CONVERTER 5V 2W
TP2
Green
A5V
C5
4.7u
TP5
Yellow
L2
10u
X1
MEE3S1205SC
DC DC CONVERTER 5V 3W
TP6
Black
D5
Green
R2
150
S1
R1
10K
D3
Blue
D2
13V
C4
0.1u
TP1
Red
C2
100u
L1
1000 µH
C3
0.1u
C1
100u
D1
30V
12V_IN
GND_IN
LOADS:
1. x6 Current sensors (6 x 5 V x 16 mA) = 0.48 W
2. R/D Chip: (5*12m + 5*35m + 3.3*2m) = 0.25 W
3. x4 Quad Op-Amp 8694: (3 x 5V x 1.3 mA) = 0.013 W
4. x1 Dual Op-Amp 8692: (1 x 5 V x 1.3 mA) = 0.004 W
5. x1 Dual Op-Amp 8397: (1 x 5 V x 12 mA) = 0.06 W
6. Launchpad = 1 W
Total: 1.8 W
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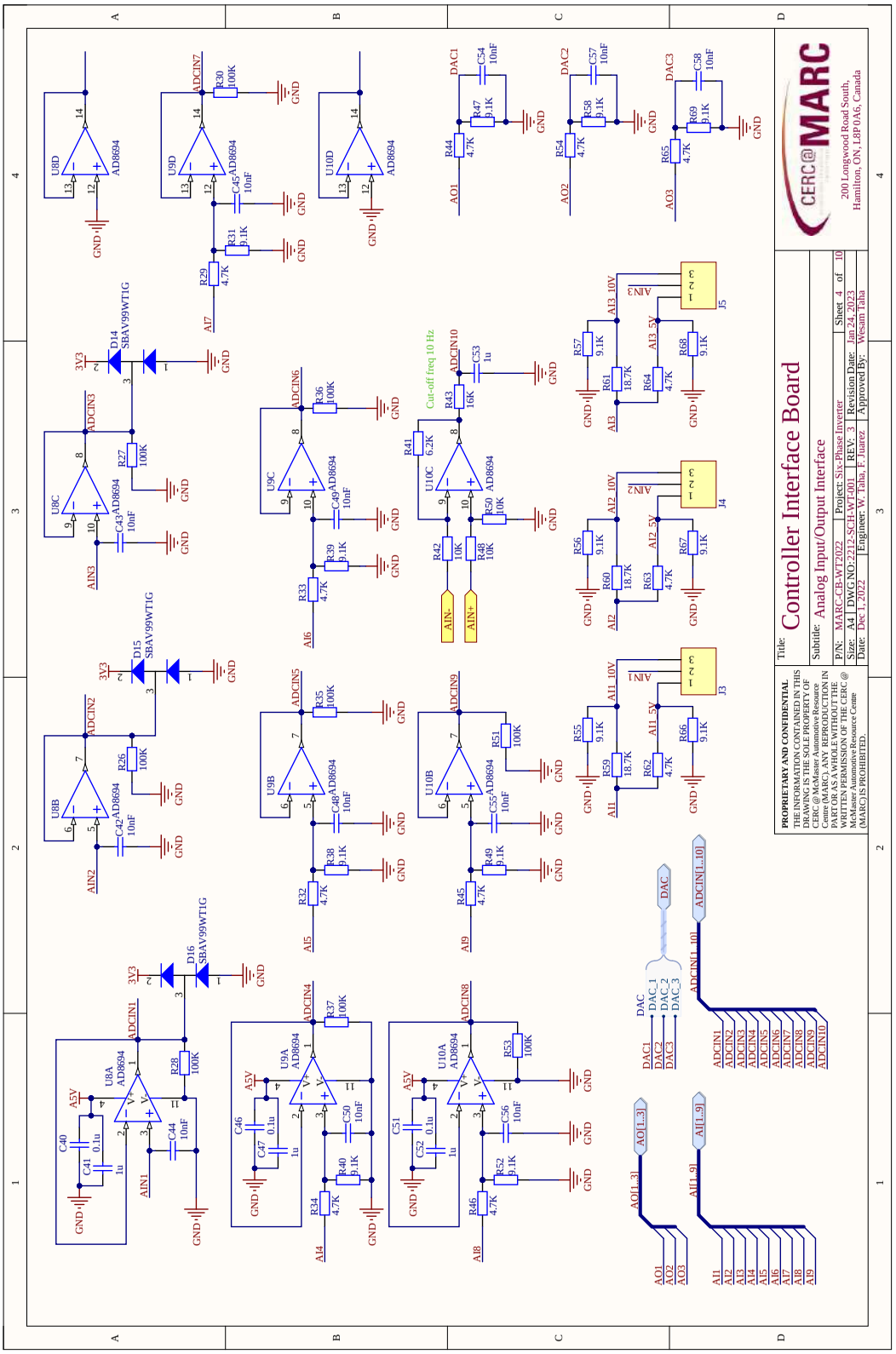
Title: Controller Interface Board
Subtitle: Power Supply
P/N: MARC-CB-WT2022
Project: Six-Phase Inverter
Sheet 3 of 10
Size: A4
DWG NO: 2212-SCH-WT-001
REV: 3
Revision Date: Jan 24, 2023
Date: Dec 1, 2022
Engineer: W. Taha, F. Juarez
Approved By: Wesam Taha
CERC@MARC
200 Longwood Road South,
Hamilton, ON, L8P 0A6, Canada


Title: Controller Interface Board
Subtitle: Analog Input/Output Interface
P/N: MARC-CB-WT2022
Project: Six-Phase Inverter
Sheet 4 of 10
Size: A4
DWG NO: 2212-SCH-WT-001
REV: 3
Revision Date: Jan 24, 2023
Date: Dec 1, 2022
Engineer: W. Taha, F. Ibarez
Approved By: Wesam Taha
CERC@MARC
200 Longwood Road South, Hamilton, ON, L8P 0A6, Canada
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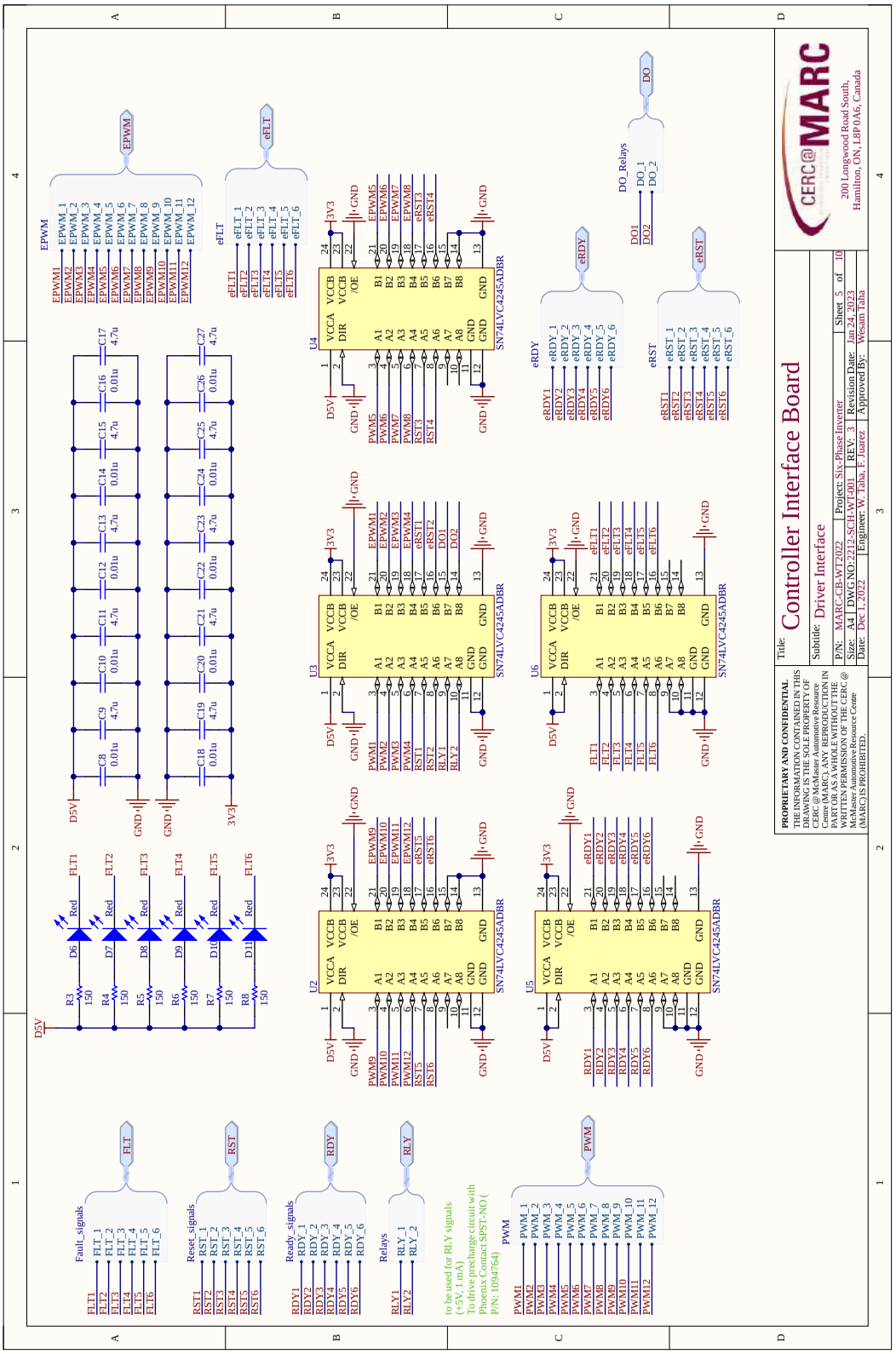
Cut-off freq 10 Hz


Controller Interface Board
Driver Interface
CERC@MARC
200 Longwood Road South, Hamilton, ON, L8P 0A6, Canada
PROPRIETARY AND CONFIDENTIAL
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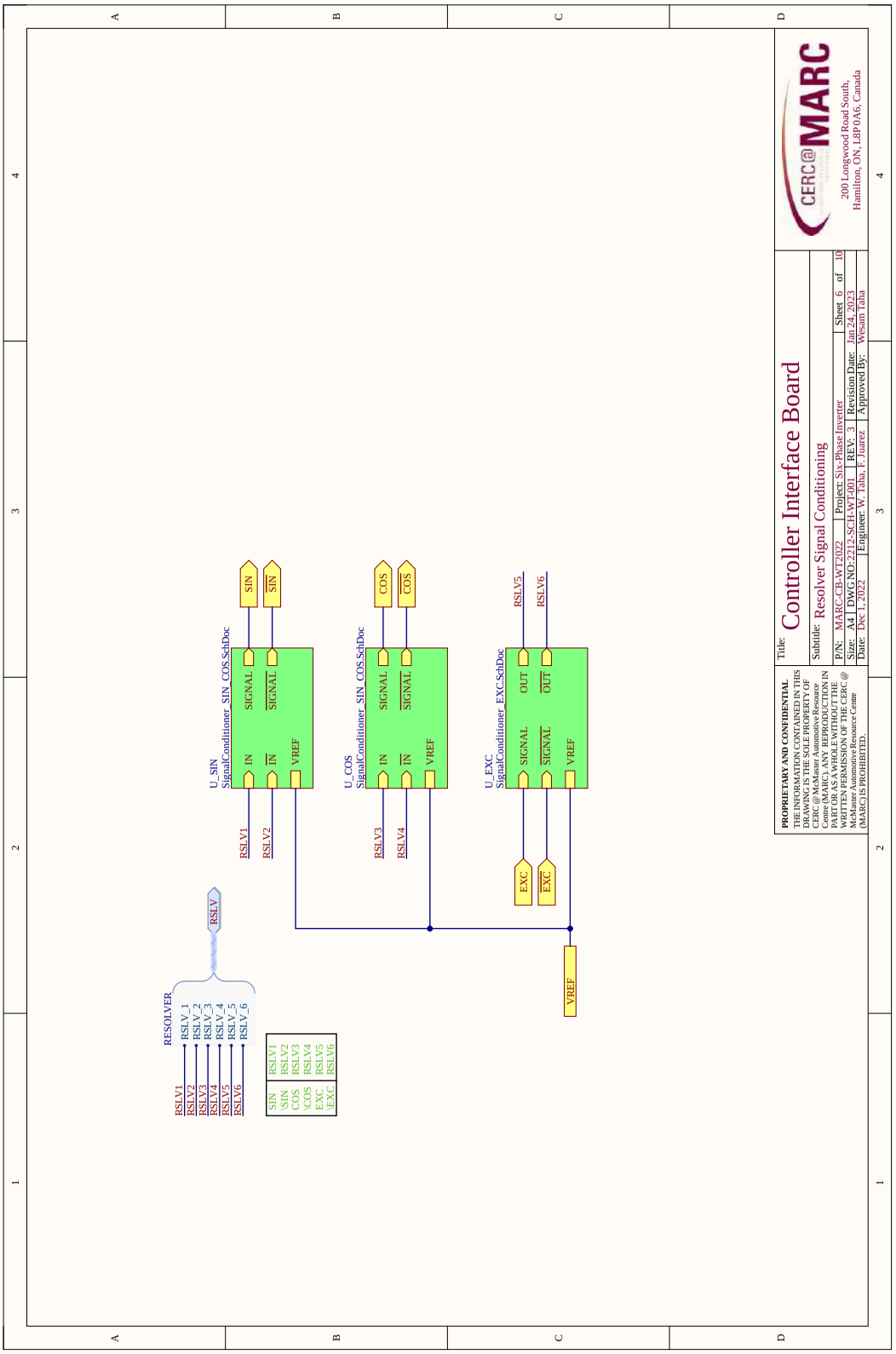
P/N: MARC-CB-WT2022
Project: Six-Phase Inverter
Size: A4
DWG NO: 2212-SCH-WT-001
REV: 3
Date: Dec 1, 2022
Engineer: W. Taha, F. Juarez
Revision Date: Jan 24, 2023
Approved By: Wesam Taha
SN74LVC4245ADBR
EPWM
eFLT
eRDY
eRST
DO
DO_Relays
Fault_signals
Reset_signals
Ready_signals
Relays
PWM
FLT
RST
RDY
RLY
D5V
3V3
GND
to be used for RLY signals (<5V, 1 mA)
To drive precharge circuit with Phoenix Contact SPST-NO (P/N: 1094764)


Controller Interface Board
Resolver Signal Conditioning
CERC@MARC
200 Longwood Road South,
Hamilton, ON, L8P 0A6, Canada
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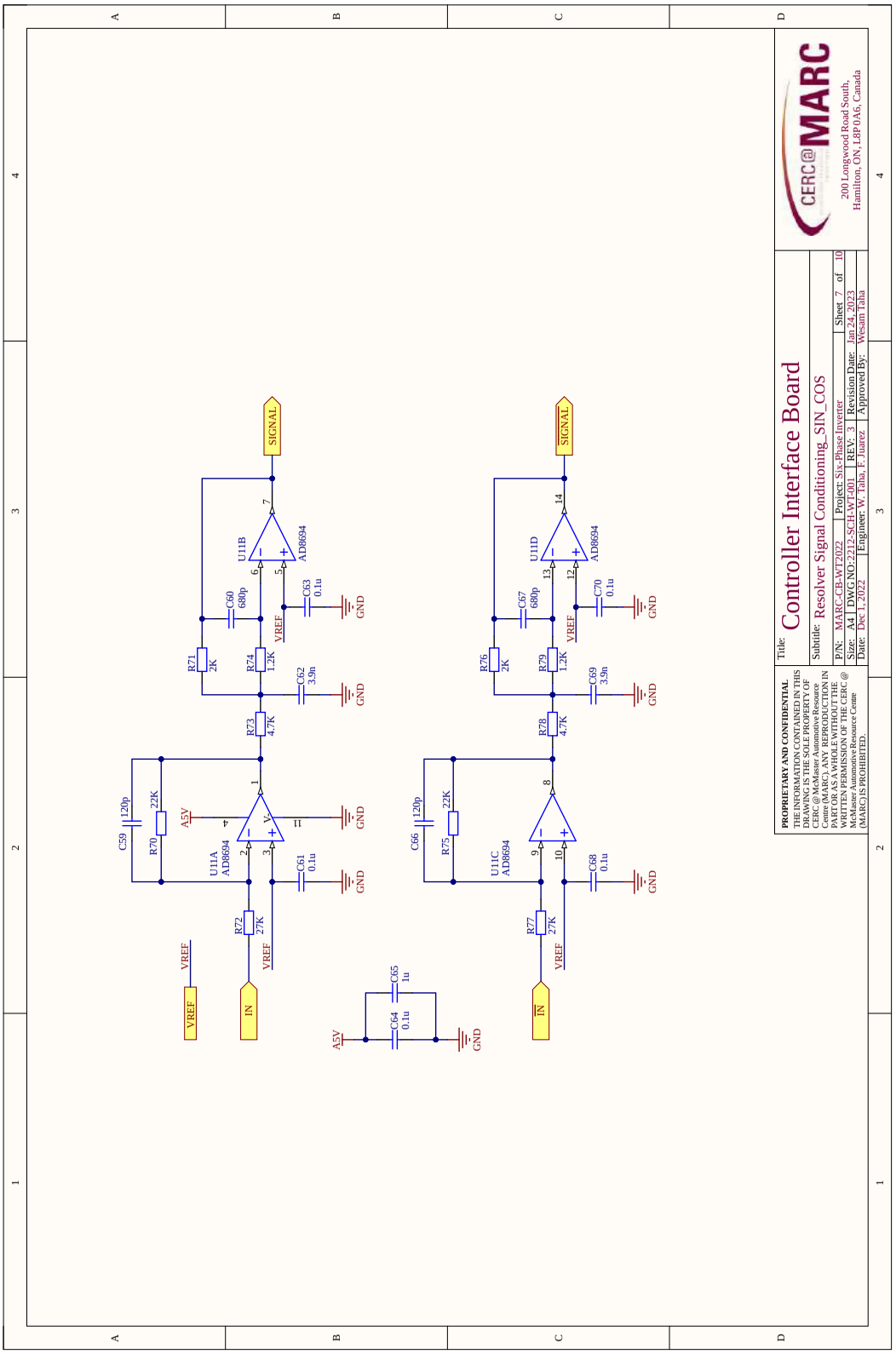
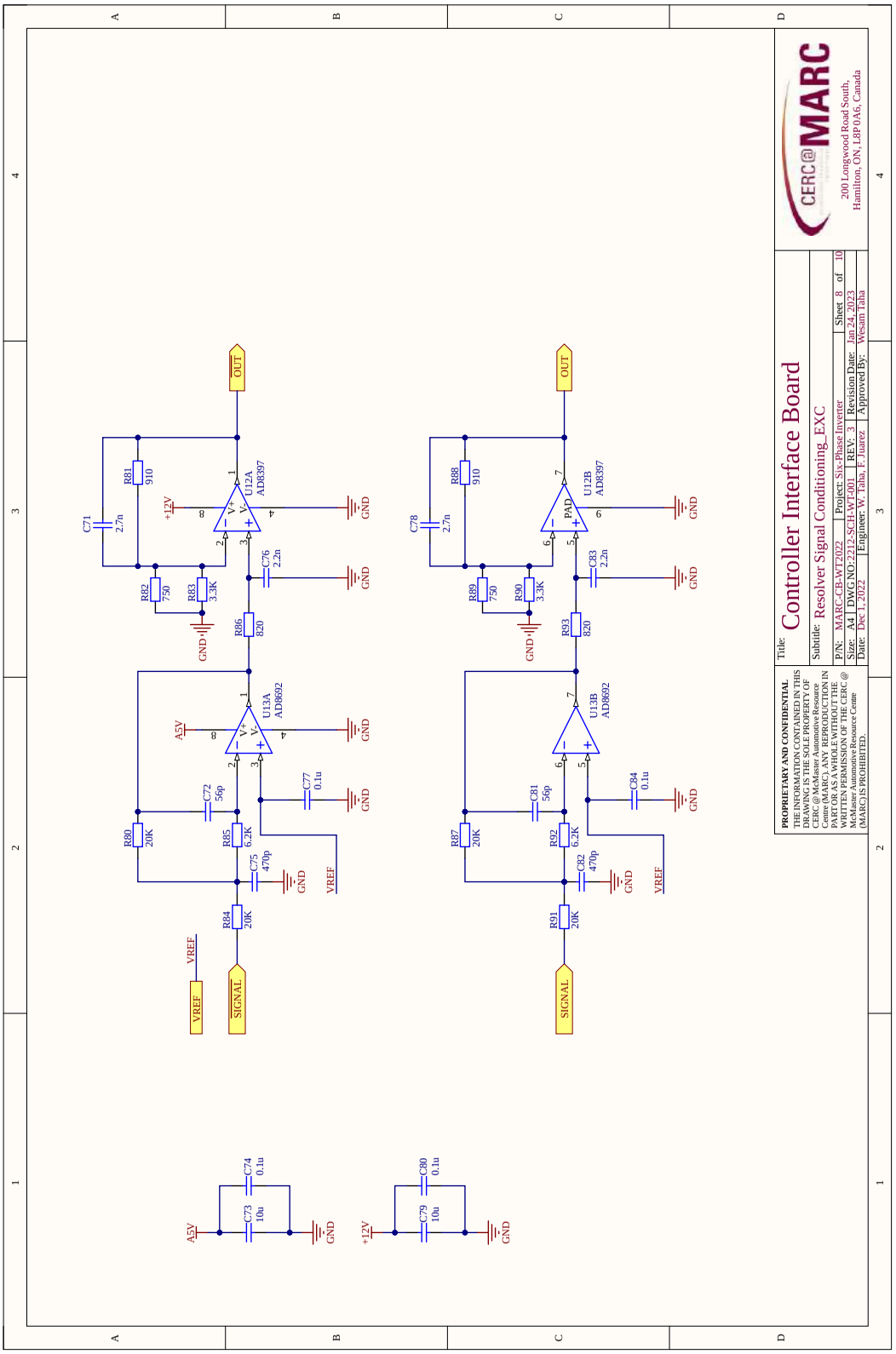
P/N: MARC-CB-WT2022
Project: Six-Phase Inverter
Size: A4
DWG NO: 2212-SCH-WT-001
REV: 3
Date: Dec 1, 2022
Engineer: W. Taha, F. Ibarez
Revision Date: Jan 24, 2023
Approved By: Wesam Taha
Sheet 6 of 10
U_SIN
SignalConditioner_SIN_COS.SchDoc
U_COS
SignalConditioner_SIN_COS.SchDoc
U_EXC
SignalConditioner_EXC.SchDoc
IN
SIGNAL
VREF
OUT
RSLV1
RSLV2
RSLV3
RSLV4
RSLV5
RSLV6
SIN
COS
EXC
VREF
RESOLVER
RSLV_1
RSLV_2
RSLV_3
RSLV_4
RSLV_5
RSLV_6


Controller Interface Board
Resolver Signal Conditioning_SIN_COS
CERC@MARC
200 Longwood Road South,
Hamilton, ON, L8P 0A6, Canada
SIGNAL
VREF
IN
A5V
GND
U11A AD8694
U11B AD8694
U11C AD8694
U11D AD8694
C59 120p
C60 680p
C61 0.1u
C62 3.9n
C63 0.1u
C64 0.1u
C65 1u
C66 120p
C67 680p
C68 0.1u
C69 3.9n
C70 0.1u
R70 22K
R71 2K
R72 27K
R73 4.7K
R74 1.2K
R75 22K
R76 2K
R77 27K
R78 4.7K
R79 1.2K


Title: Controller Interface Board
Subtitle: Resolver Signal Conditioning_EXC
P/N: MARC-CB-WT2022
Project: Six-Phase Inverter
Sheet 8 of 10
Size: A4
DWG NO: 2212-SCH-WT-001
REV: 3
Revision Date: Jan 24, 2023
Date: Dec 1, 2022
Engineer: W. Taha, F. Ibarez
Approved By: Wesam Taha
CERC@MARC
200 Longwood Road South,
Hamilton, ON, L8P 0A6, Canada
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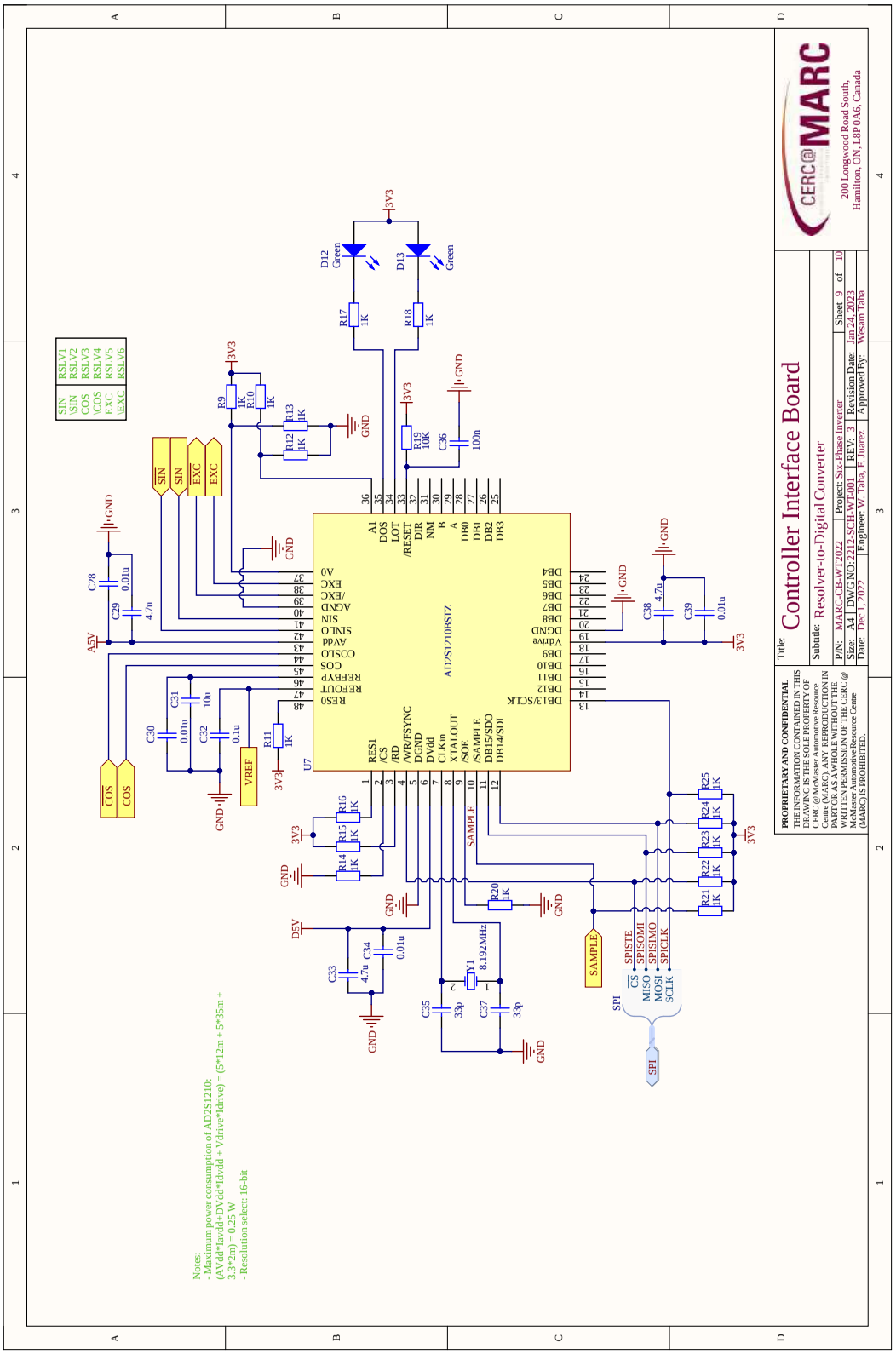
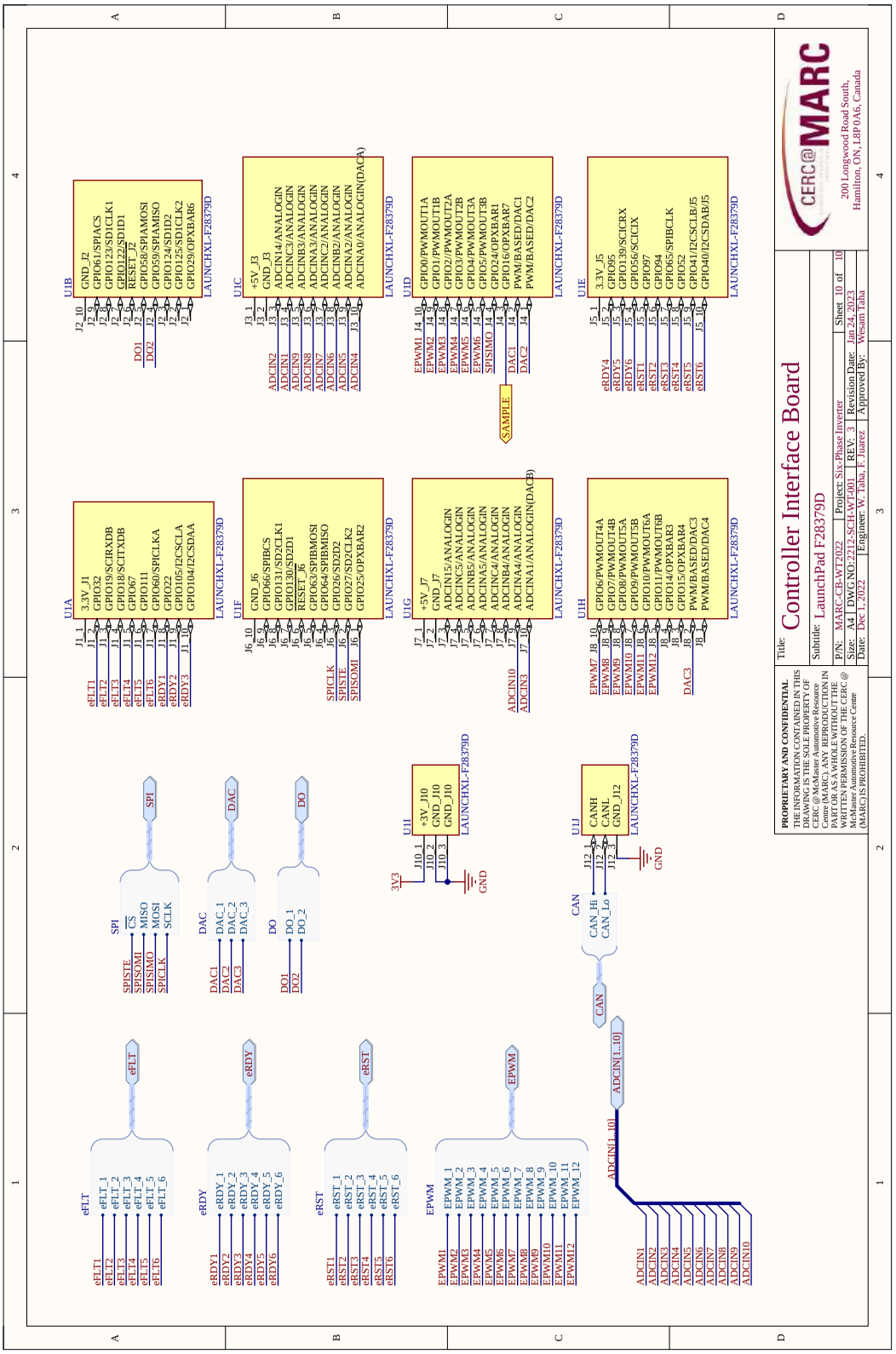
U12A AD8397
U12B AD8397
U13A AD8692
U13B AD8692
R80 20K
R81 910
R82 750
R83 3.3K
R84 20K
R85 6.2K
R86 820
R87 20K
R88 910
R89 750
R90 3.3K
R91 20K
R92 6.2K
R93 820
C71 2.7n
C72 56p
C73 10u
C74 0.1u
C75 470p
C76 2.2n
C77 0.1u
C78 2.7n
C79 10u
C80 0.1u
C81 56p
C82 470p
C83 2.2n
C84 0.1u
+12V
A5V
GND
VREF
SIGNAL
OUT


Controller Interface Board
Resolver-to-Digital Converter
CERC@MARC
200 Longwood Road South,
Hamilton, ON, L8P 0A6, Canada
AD2S1210BSTZ
U7
SIN
COS
EXC
SAMPLE
SPI
Notes:
- Maximum power consumption of AD2S1210:
(AVdd*Iavdd+DVdd*Idvdd + Vdrive*Idrive) = (5*12m + 5*35m + 3.3*2m) = 0.25 W
-Resolution select: 16-bit


Controller Interface Board
LaunchPad F28379D
CERC@MARC
200 Longwood Road South,
Hamilton, ON, L8P 0A6, Canada
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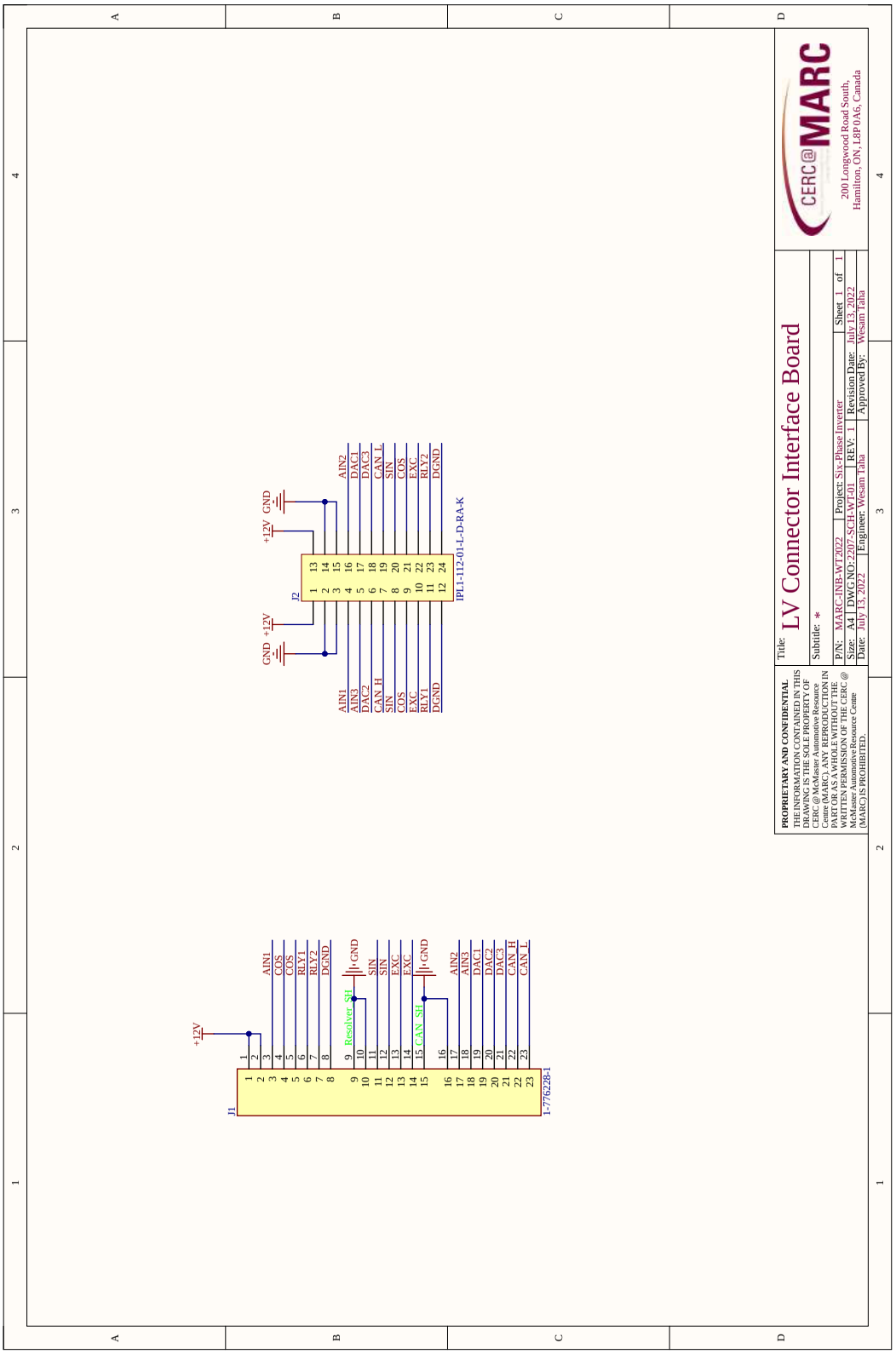
P/N: MARC-CB-WT2022
Project: Six-Phase Inverter
Size: A4
DWG NO: 2212-SCH-WT-001
REV: 3
Date: Dec 1, 2022
Engineer: W. Taha, F. Juarez
Revision Date: Jan 24, 2023
Approved By: Wesam Taha
Sheet 10 of 10
U1A
U1B
U1C
U1D
U1E
U1F
U1G
U1H
U1I
U1J
LAUNCHXL-F28379D
SPI
DAC
DO
CAN
SAMPLE
EPWM
eFLT
eRDY
eRST
ADCIN1..10
3V3
GND


Title: LV Connector Interface Board
Subtitle: *
P/N: MARC-INB-WT2022
Project: Six-Phase Inverter
Size: A4
DWG NO: 2207-SCH-WT-01
REV: 1
Date: July 13, 2022
Engineer: Wesam Taha
Revision Date: July 13, 2022
Approved By: Wesam Taha
Sheet 1 of 1
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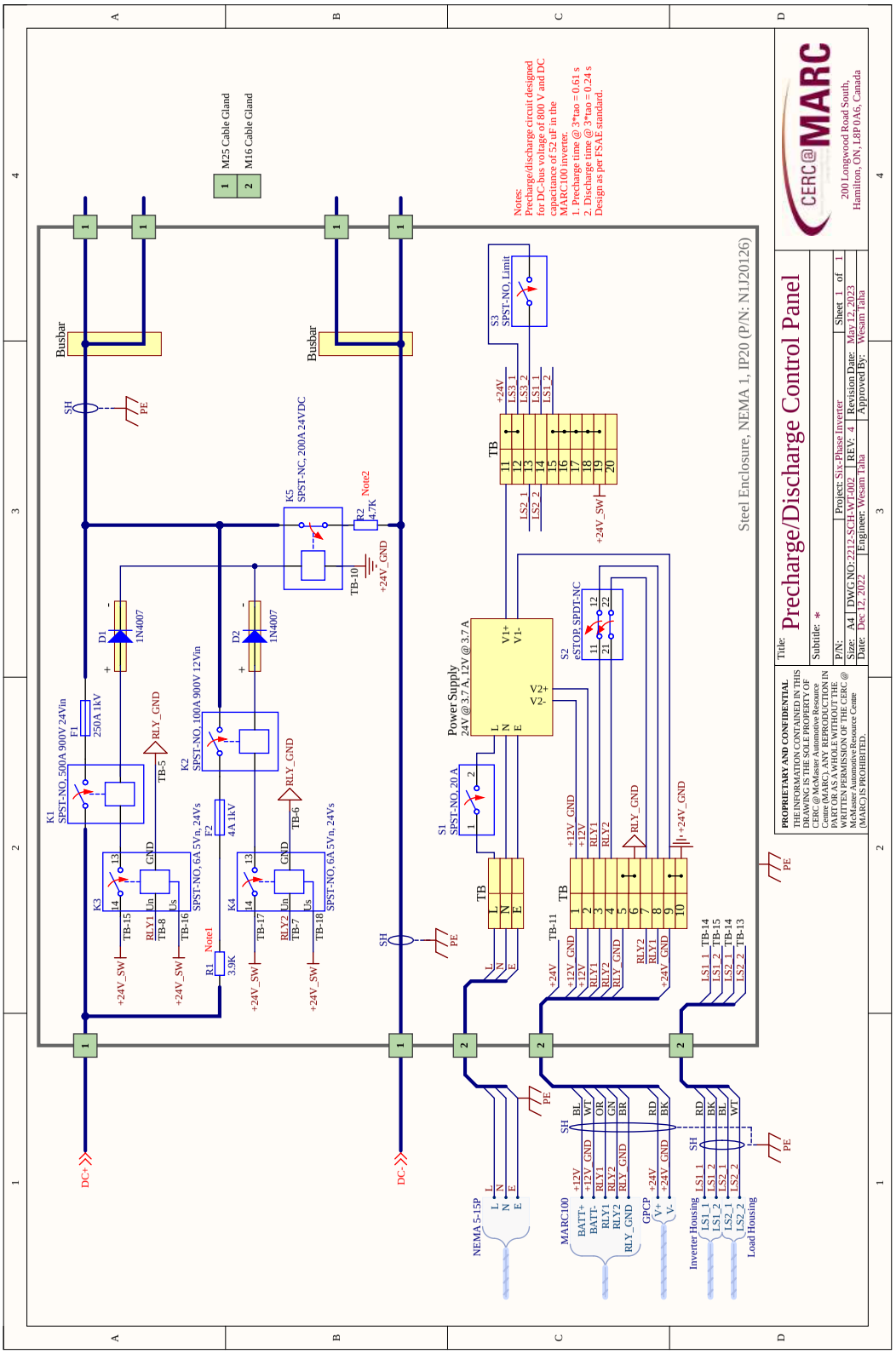
CERC@MARC
200 Longwood Road South,
Hamilton, ON, L8P 0A6, Canada
J1
1-776228-1
J2
IPL1-112-01-L-D-RA-K
+12V
GND
Resolver_SH
CAN_SH
AIN1
AIN2
AIN3
COS
SIN
EXC
RLY1
RLY2
DAC1
DAC2
DAC3
CAN_H
CAN_L
DGND


Precharge/Discharge Control Panel
Steel Enclosure, NEMA 1, IP20 (P/N: N1J20126)
CERC@MARC
200 Longwood Road South, Hamilton, ON, L8P 0A6, Canada
M25 Cable Gland
M16 Cable Gland
Busbar
Busbar
SH
PE
K1 SPST-NO, 500A 900V 24Vin
F1 250A 1kV
D1 1N4007
D2 1N4007
K2 SPST-NO, 100A 900V 12Vin
F2 4A 1kV
K3 SPST-NO, 6A 5Vn, 24Vs
K4 SPST-NO, 6A 5Vn, 24Vs
K5 SPST-NC, 200A 24VDC
R1 3.9K
R2 4.7K
Note1
Note2
RLY_GND
+24V_SW
+24V_GND
TB-5
TB-6
TB-7
TB-8
TB-10
TB-15
TB-16
TB-17
TB-18
S1 SPST-NO, 20 A
S2 eSTOP, SPDT-NC
S3 SPST-NO, Limit
Power Supply 24V @ 3.7 A, 12V @ 3.7 A
V1+ V1- V2+ V2-
TB
TB-11
+12V_GND
RLY1
RLY2
+24V
LS3_1 LS3_2 LS1_1 LS1_2 LS2_1 LS2_2
Notes:
Precharge/discharge circuit designed for DC-bus voltage of 800 V and DC capacitance of 52 uF in the MARC100 inverter.
1. Precharge time @ 3*tao = 0.61 s
2. Discharge time @ 3*tao = 0.24 s
Design as per FSAE standard.
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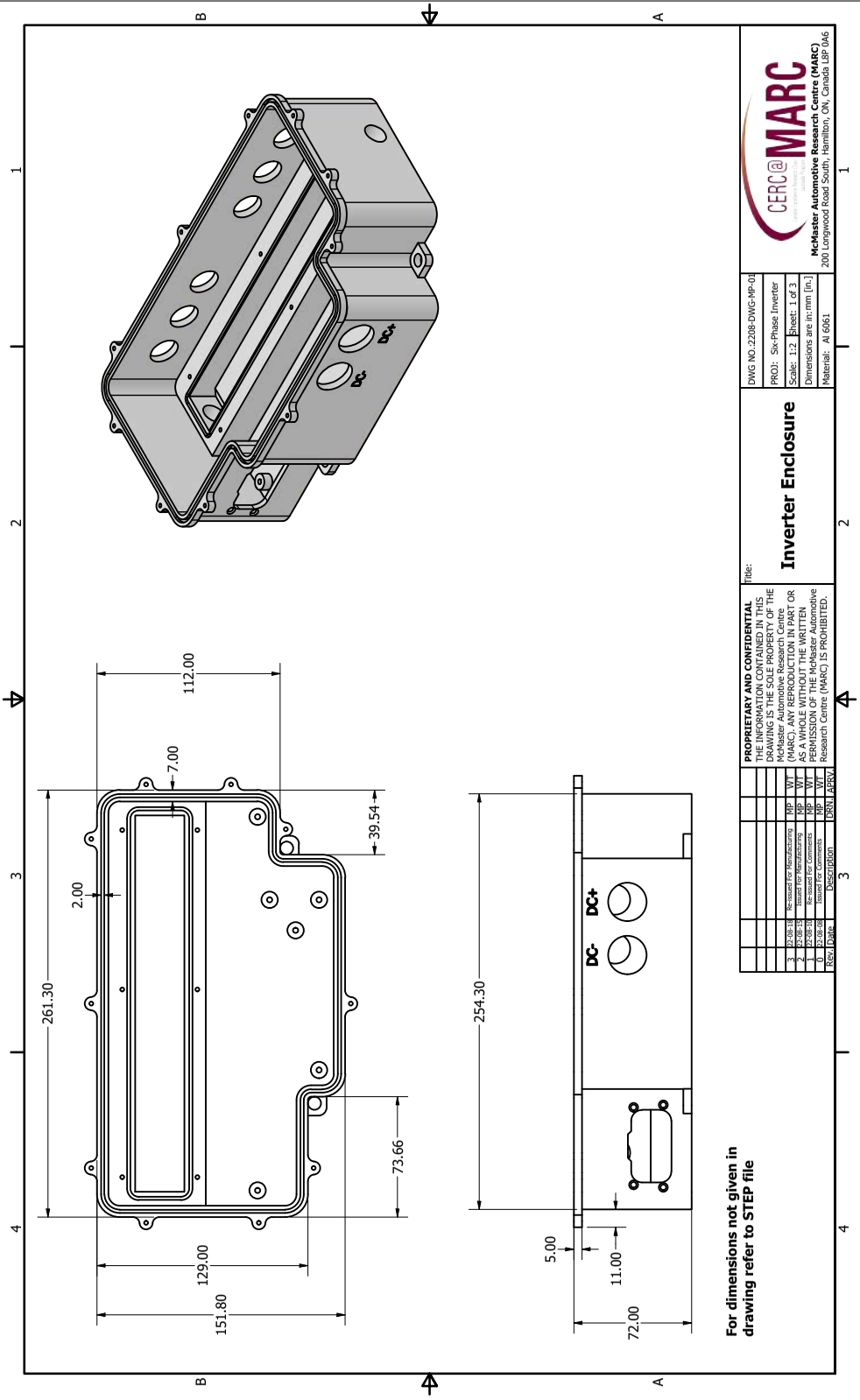
Title:
Subtitle: *
P/N:
Project: Six-Phase Inverter
Sheet 1 of 1
Size: A4
DWG NO: 2212-SCH-WT-002
REV: 4
Revision Date: May 12, 2023
Date: Dec 12, 2022
Engineer: Wesam Taha
Approved By: Wesam Taha
NEMA 5-15P
MARC100
GPCP
Inverter Housing
Load Housing
DC+
DC-

Appendix B

Engineering Drawings

This appendix includes the engineering drawings of the manufactured enclosure and heat sink and the experimental setup. Specifically, it includes:

1. Inverter enclosure
2. Inverter lid
3. Heat sink
4. High-voltage testing rig


DC-
DC+
112.00
7.00
39.54
2.00
261.30
73.66
129.00
151.80
254.30
DC- DC+
5.00
11.00
72.00
For dimensions not given in drawing refer to STEP file
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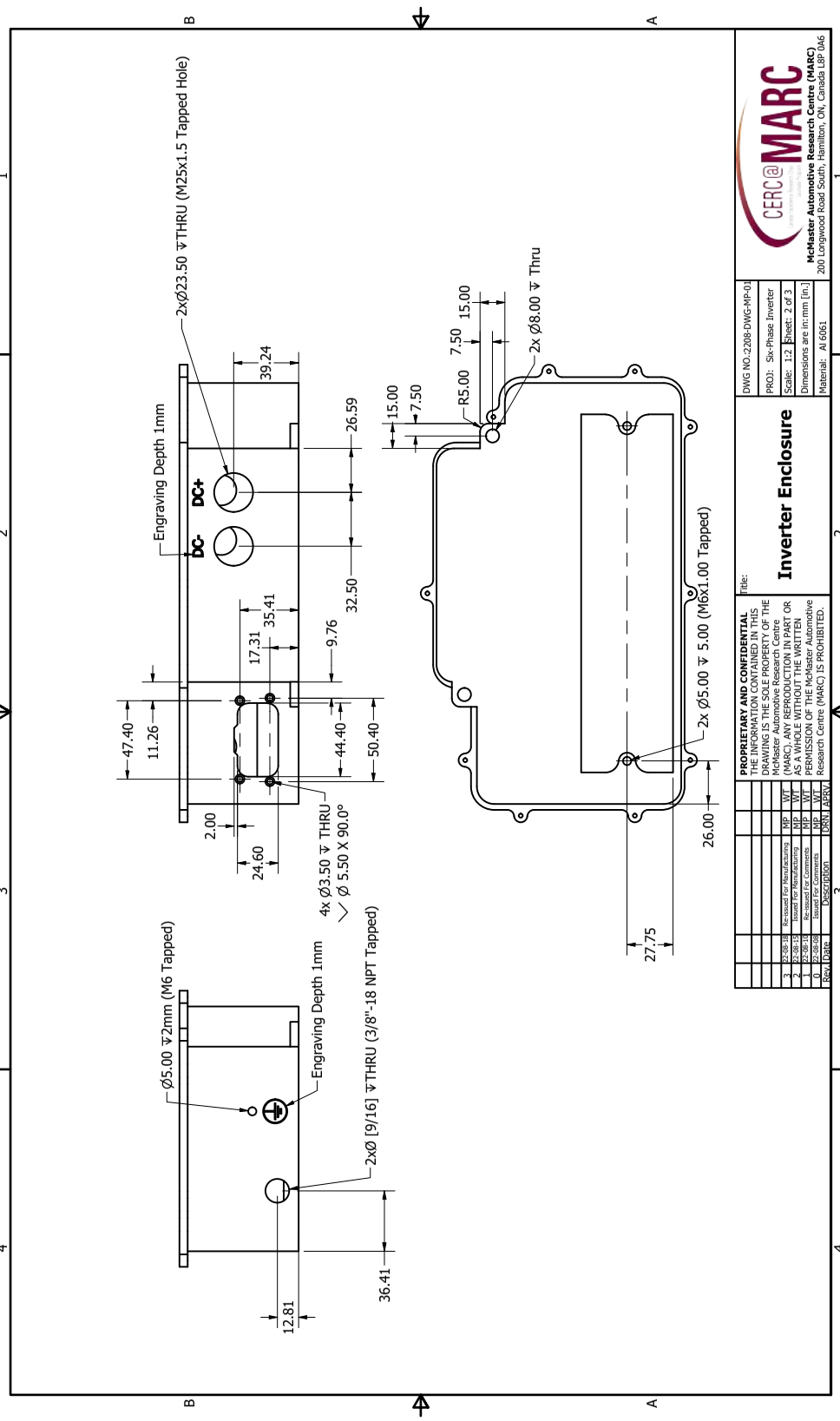
Title:
Inverter Enclosure
DWG NO.:2208-DWG-MP-01
PROJ: Six-Phase Inverter
Scale: 1:2 Sheet: 1 of 3
Dimensions are in:mm [in.]
Material: Al 6061
McMaster Automotive Research Centre (MARC)
200 Longwood Road South, Hamilton, ON, Canada L8P 0A6
Rev Date Description DRN APRV
3 22-08-31 Re-issued For Manufacturing MP WT
2 22-08-30 Re-issued For Manufacturing MP WT
1 22-08-29 Re-issued For Comments MP WT
0 22-08-09 Issued For Comments MP WT


2xØ23.50 ∓THRU (M25x1.5 Tapped Hole)
Engraving Depth 1mm
DC+
DC-
39.24
26.59
32.50
35.41
17.31
9.76
47.40
11.26
44.40
50.40
2.00
24.60
4x Ø3.50 ∓ THRU
⌵ Ø 5.50 X 90.0°
Ø5.00 ∓2mm (M6 Tapped)
Engraving Depth 1mm
2xØ [9/16] ∓THRU (3/8"-18 NPT Tapped)
36.41
12.81
15.00
7.50
R5.00
2x Ø8.00 ∓ Thru
2x Ø5.00 ∓ 5.00 (M6x1.00 Tapped)
26.00
27.75
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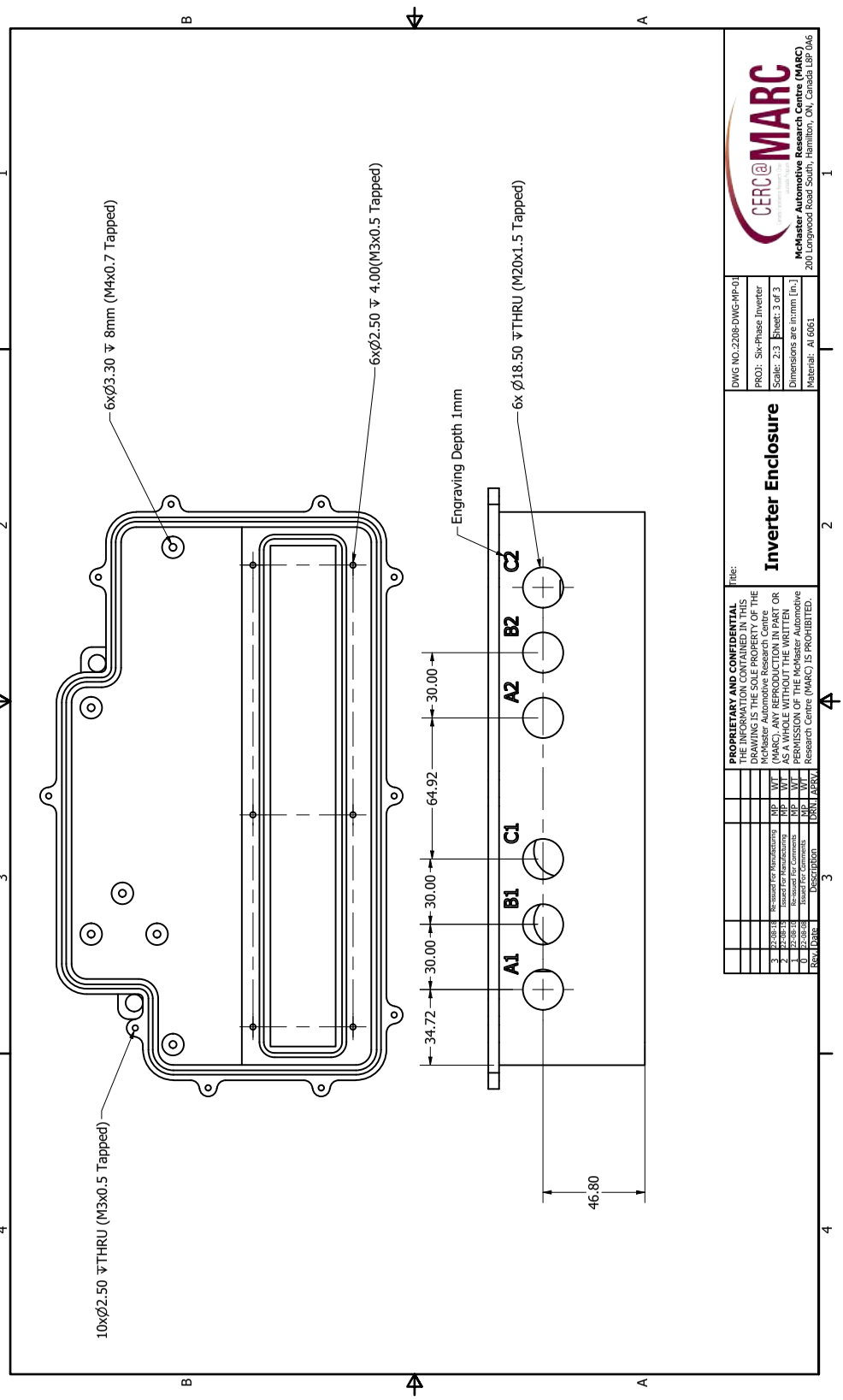
PERMISSION OF THE McMaster Automotive
Research Centre (MARC) IS PROHIBITED.
Title:
Inverter Enclosure
DWG NO:2208-DWG-MP-01
PROJ: Six-Phase Inverter
Scale: 1:2 Sheet: 2 of 3
Dimensions are in: mm [in.]
Material: Al 6061
CERC@MARC
McMaster Automotive Research Centre (MARC)
200 Longwood Road South, Hamilton, ON, Canada L8P 0A6
Rev Date Description DRN APPV
3 22-08-18 Re-issued For Manufacturing MP WT
2 22-08-15 Issued For Manufacturing MP WT
1 22-08-10 Re-issued For Comments MP WT
0 22-08-08 Issued For Comments MP WT


6xØ3.30 ∓ 8mm (M4x0.7 Tapped)
6xØ2.50 ∓ 4.00(M3x0.5 Tapped)
Engraving Depth 1mm
6x Ø18.50 ∓THRU (M20x1.5 Tapped)
10xØ2.50 ∓THRU (M3x0.5 Tapped)
A1
B1
C1
A2
B2
C2
34.72
30.00
30.00
64.92
30.00
46.80
PROPRIETARY AND CONFIDENTIAL
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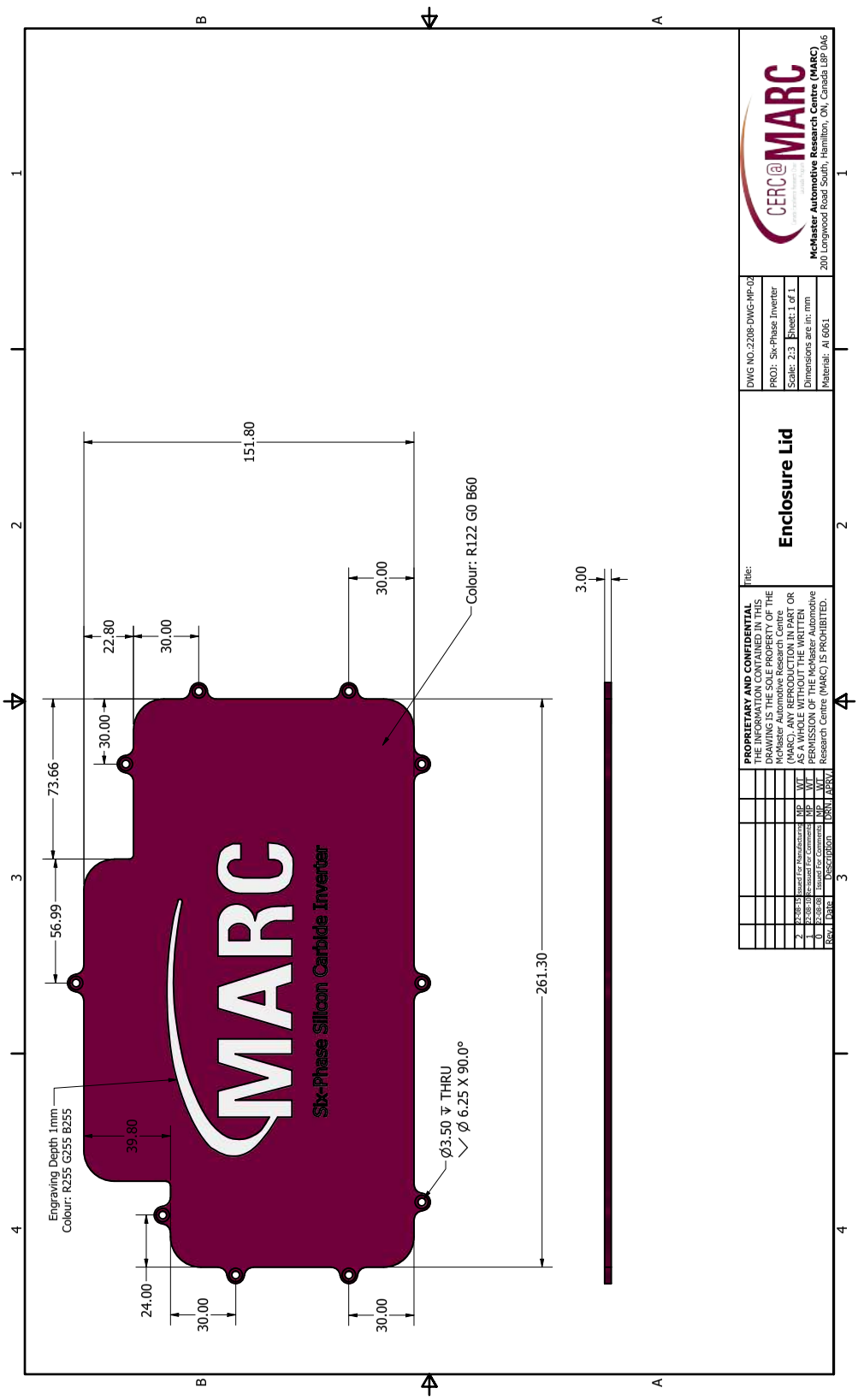
Title:
Inverter Enclosure
DWG NO.:2208-DWG-MP-01
PROJ: Six-Phase Inverter
Scale: 2:3 Sheet: 3 of 3
Dimensions are in:mm [in.]
Material: Al 6061
CERC@MARC
McMaster Automotive Research Centre (MARC)
200 Longwood Road South, Hamilton, ON, Canada L8P 0A6
Rev Date Description DRN APPV
3 22-08-19 Re-issued For Manufacturing MP WT
2 22-08-19 Issued For Manufacturing MP WT
1 22-08-18 Re-issued For Comments MP WT
0 22-08-08 Issued For Comments MP WT


151.80
22.80
30.00
30.00
30.00
73.66
56.99
39.80
24.00
30.00
30.00
261.30
3.00
Colour: R122 G0 B60
Engraving Depth 1mm
Colour: R255 G255 B255
Ø3.50 ∓ THRU
⌵ Ø 6.25 X 90.0°
MARC
Six-Phase Silicon Carbide Inverter
Enclosure Lid
DWG NO.2208-DWG-MP-02
PROJ: Six-Phase Inverter
Scale: 2:3 Sheet: 1 of 1
Dimensions are in: mm
Material: Al 6061
McMaster Automotive Research Centre (MARC)
200 Longwood Road South, Hamilton, ON, Canada L8P 0A6
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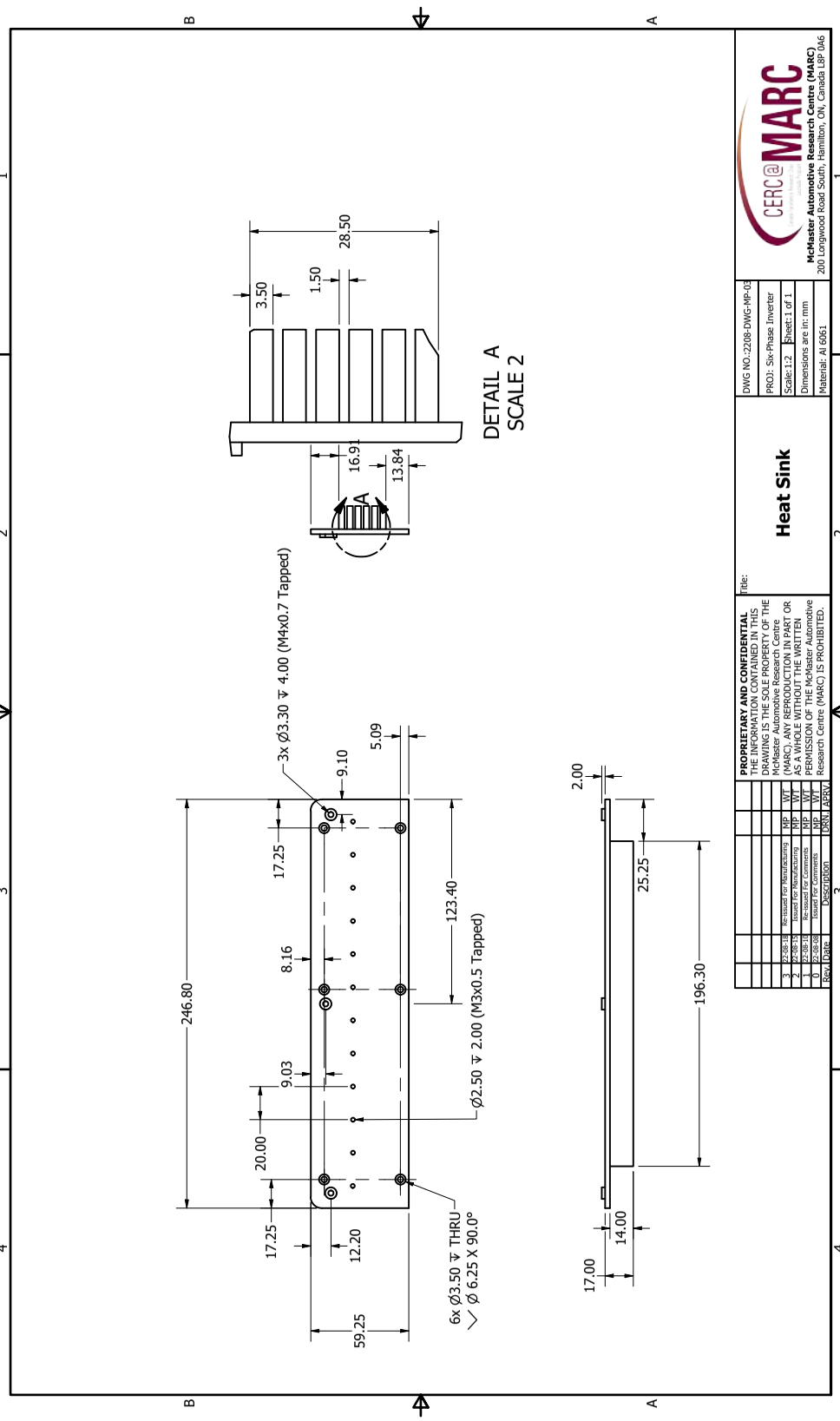
PERMISSION OF THE McMaster Automotive
Research Centre (MARC) IS PROHIBITED.
Rev. Date Description DRN APPV
2 24-08-15 Issued For Manufacturing MP WT
1 24-08-10 Reissued For Comments MP WT
0 24-08-08 Issued For Comments MP WT


DETAIL A
SCALE 2
28.50
3.50
1.50
16.91
13.84
3x Ø3.30 ↧ 4.00 (M4x0.7 Tapped)
9.10
5.09
246.80
17.25
8.16
123.40
9.03
20.00
Ø2.50 ↧ 2.00 (M3x0.5 Tapped)
17.25
12.20
59.25
6x Ø3.50 ↧ THRU
⌵ Ø 6.25 X 90.0°
2.00
25.25
196.30
17.00
14.00
PROPRIETARY AND CONFIDENTIAL
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AS A WHOLE WITHOUT THE WRITTEN
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Title:
Heat Sink
DWG NO.:2208-DWG-MP-03
PROJ: Six-Phase Inverter
Scale:1:2 Sheet: 1 of 1
Dimensions are in: mm
Material: Al 6061
CERC@MARC
McMaster Automotive Research Centre (MARC)
200 Longwood Road South, Hamilton, ON, Canada L8P 0A6
Rev Date Description DRN APPV
3 22-08-18 Re-issued For Manufacturing MP WT
2 22-08-15 Issued For Manufacturing MP WT
1 22-08-10 Re-issued For Comments MP WT
0 22-08-08 Issued For Comments MP WT


[96.000]
2438.40
[61.500]
1562.10
[36.000]
914.40
Si IGBT Inverter
MARC100 SiC Inverter
[8.819]
224.00
[29.547]
750.50
[33.071]
840.00
100A, 1mH
Inductive Load
Six-Phase Inverters
Precharge/Safety
TITLE:
Six-Phase Inverters
Testing Rig
McMaster Automotive
Research Centre (MARC)
DWG. NO.: 2212-WT-001
REV 1
PROJ.: Thesis
SCALE: 1:20
SHEET 1 OF 1
1 09-12-22 ISSUED FOR CONSTRUCTION WT
0 01-12-22 ISSUED FOR COMMENTS WT
REV DATE DESCRIPTION DRN CHKD APPR

Appendix C

MARC100 Low Voltage Connector Pin Out

This appendix outlines the pin out of the low voltage AMPSEAL 1-776228-1 (23-pin) header that is mounted on the inverter housing.

Pin #	Pin Name	Description	Notes
1	BATT+	12V Input	
2	BATT+	12V Input	Redundancy for increased current capability
3	AIN1	Analog Input 1	Configurable range (0–5V or 10V) via jumper J3 on control interface board

Continued on the next page

Pin #	Pin Name	Description	Notes
4	COS	Resolver COS winding	
5	/COS	Resolver COS return	
6	RLY1	High Side Driver	For pre-charge relay contactor output
7	RLY2	High Side Driver	For main relay contactor output
8	DGND	Digital Ground	Ground reference for digital inputs/outputs
9	R_SH	Resolver cable shield	
10	BATT_GND	12V Return	
11	SIN	Resolver SIN winding	
12	/SIN	Resolver SIN return	
13	EXC	Resolver excitation	

Continued on the next page

Pin #	Pin Name	Description	Notes
14	/EXC	Resolver excitation return	
15	CAN_SH	CAN cable shield	Connection of CAN cable shield
16	BATT_GND	12V Return	Redundancy for increased current capability
17	AIN2	Analog Input 2	Configurable range via jumper J4 on control interface board
18	AIN3	Analog Input 3	Configurable range via jumper J5 on control interface board
19	DAC1	Digital Output 1	0–3V
20	DAC2	Digital Output 2	0–3V
21	DAC3	Digital Output 3	0–3V
22	CAN_H	CAN Channel High	CAN communication channel
23	CAN_L	CAN Channel Low	CAN communication channel

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