Time-Domain Analysis and Optimization of a Three-Phase Dual-Active-Bridge Converter With Variable Duty-Cycle Modulation

Time-Domain Analysis and Optimization of a Three-Phase Dual-Active-Bridge Converter With Variable Duty-Cycle Modulation

by

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Abstract

The duty cycle control (DCC) modulation scheme for the three-phase dual-activebridge (3p-DAB) DC-DC converter is a promising three degree-of-freedom modulation scheme which can extend the converter's soft-switching range and reduce conduction losses under partial loading and wide voltage variations. However, the prior suggested methods to implement DCC in 3p-DABs have drawbacks such as requiring a multifrequency approximation and offline optimization process or achieving less than optimal efficiency. To overcome these challenges, this research first proposes an optimal DCC modulation strategy (OMS) for the 3p-DAB based on a novel piece-wise time-domain analysis (TDA) and optimization process that obtains the optimal control parameters for minimum RMS phase current. Secondly, this research proposes a novel closed-form minimum current stress optimization (MCSO) DCC scheme based on the theoretical findings of the TDA optimization. The MCSO reduces the transformer phase currents and extends soft-switching operation under partial loading and wide voltage variations. Experimental results via open-loop testing show that the proposed closed-form MCSO DCC scheme has virtually identical efficiency as the OMS, making this the first research to provide a closed-form DCC modulation scheme for a 3p-DAB that achieves efficiency results equivalent to a fully-optimized offline scheme, but without the drawbacks of the offline optimization process.

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Chapter 1

Introduction

1.1 Background and Motivations

With the increase in global attention towards electrified transportation, renewable power generation, and DC power distribution, the isolated bidirectional DC-DC converter (IBDC) is considered to be a key enabler in the development and integration of these technologies [1]-[4]. For example, in the AC/DC conversion stage of DC fast charging stations, IBDCs are an ideal power converter candidate capable of providing efficient power conversion across a wide range of battery voltages [2]. Furthermore in [3], IBDCs are shown to play an essential role in integrating battery energy storage systems into photovoltaic systems, thus making these renewable energy systems dispatchable in a supply and demand electricity market. Lastly, in [4], the future renewable electric energy delivery and management (FREEDM) system is proposed. In the FREEDM system, IBDCs are shown to be a key building block for solid state transformers (SST) which are a necessary component for routing electrical energy between distributed renewable energy devices and distributed energy storage devices thereby facilitating a green and sustainable energy-based society. The applications of IBDCs are widespread and deemed to be a key component in reducing the impact of carbon emissions on the environment.

The single-phase dual active bridge (1p-DAB) DC-DC converter is an attractive IBDC topology because of its high power density, galvanic isolation, and intrinsic softswitching ability [5], [6]. The three-phase dual active bridge (3p-DAB) IBDC, however, offers some additional advantages compared to the 1p-DAB, such as increased power transfer capability, reduced device current stress, and smaller DC-link capacitance, which all contribute to an increase in power density [5]. Based on these advantages, this research focuses on the 3p-DAB topology.

The 3p-DAB is composed of two three-phase active bridges connected together by a high-frequency transformer with turns ratio 1:n and leakage inductance L. For the conventional singe-phase-shift (SPS) modulation strategy, each switch in a leg has 50% complementary duty cycle and each leg is operated with a 120° phase-shift from another. By introducing a phase angle between the input and output bridges, power transfer can be controlled through the converter's leakage inductance. When a dual active bridge (DAB) converter is controlled using SPS modulation and is subject to partial loading with non-unity voltage gain d, its efficiency is reduced due to hard switching and increased back power flow [7]. However, when IBDCs operate as auxiliary power modules in electrified vehicles or interface with renewable energy sources and storage devices, operation under partial loading and non-unity voltage gain is unavoidable. Therefore, to maintain efficient converter operation under a wider operating range, alternative modulation strategies must be implemented.

For the 1p-DAB, there exist many alternative modulation strategies that improve the performance of the converter under partial loading and non-unity voltage gain. By increasing the degrees of freedom in the control by introducing inner phase-shift angles, the dual-phase-shift [7], extended-phase-shift [8], and triple-phase-shift (TPS) [9] modulation strategies can be implemented to help mitigate back power flow and extend the soft-switching range of the converter. The TPS modulation strategy, having three degrees of freedom, can achieve globally optimized control parameters for minimum current stress, minimum RMS current, minimum power loss, or maximum ZVS range [10]. These alternative modulation schemes, however, cannot be directly applied to the 3p-DAB because of the 120° phase-shift that exists between phase legs. Therefore, to add more flexibility to the 3p-DAB control, the duty cycles of the input and output bridges (D_1 , D_2) and phase-shift (D_{ps}) need to be modulated appropriately [11]-[15].

By implementing two degrees of freedom in the modulation of a 3p-DAB, [11] proposes an optimal simultaneous PWM control strategy which applies the same variable duty cycle to both active bridges to minimize the current stress. Although this control minimizes the peak current, it does not minimize the conduction losses or necessarily extend the soft-switching range, and since this control only employs two degrees of freedom, there is no guarantee that the current stress is globally minimized.

Allowing a different duty cycle on the input and output bridges (D_1, D_2) , as well as the phase-shift (D_{ps}) gives three degrees of freedom, commonly called duty-cycle control (DCC). DCC for the 3p-DAB is analogous to TPS modulation for the 1p-DAB and therefore globally optimized modulation strategies can be obtained. The 3p-DAB modulation strategies proposed in [5] and [11] can be considered as special cases of DCC.

In [12], a DCC strategy is proposed for the 3p-DAB with the goal of optimizing control parameters to minimize the converter's RMS phase current. The optimization process occurs offline, and the results are read from a look-up table (LUT) during converter operation. The 3p-DAB is modeled using the multi-frequency approximation method, resulting in expressions of average output power and transformer RMS currents that contain infinite series. To reduce the model's non-linearity and computational burden, the infinite

series must be truncated, which negatively affects the model accuracy, especially at light loads and non-unity voltage gain. Additionally, only a simplified block diagram of the novel optimization algorithm used to obtain the optimal parameters is provided in [12], which hinders its practical implementation. Furthermore, the multi-frequency approximation analysis in [12] is complicated and neglects to analyze the 3p-DAB boost operation, which is essential for many applications.

In [13], a phasor analysis approach is used in the proposed hybrid modulation scheme, which combines SPS and a novel zero-vector modulation scheme to target maximum 3p-DAB efficiency under wide voltage and power variations. The proposed modulation improves the efficiency of the converter compared to SPS during low to medium power and wide voltage gains, however, the modulation parameters (D_1 , D_2 , and D_{ps}) must be computed offline using a detailed loss model of the 3p-DAB which depends highly on component parameters that are sometimes difficult to determine such as the highfrequency transformer Steinmetz parameters and switch parasitic capacitances. In addition to the detailed loss model, an offline optimization process is required, and the resulting parameters are implemented in a LUT.

Considering the drawbacks of the multi-frequency approximation in [12] and the detailed loss modeling required in [13], the first contribution of this research is to propose a DCC strategy for the 3p-DAB based on a novel comprehensive piece-wise time-domain analysis (TDA) and an optimization process that obtains the optimal control parameters for minimum RMS phase current in buck and boost operation. By analyzing the phase voltage and inductor current waveforms, this research is the first to present the eighteen TDA

operating modes of a 3p-DAB with DCC defined by D_1 , D_2 , and D_{ps} . The non-linear optimization problem to obtain the optimal control parameters is solved using MATLAB's Optimization Toolbox, and the results show that many of the eighteen modes are not needed for optimal operation and can be eliminated, reducing the domain of the optimization problem, and simplifying its implementation. The theoretical results of this proposed TDA optimized modulation strategy (OMS) are validated experimentally.

The proposed straightforward TDA optimization, and the methods proposed in [12] and [13], rely on an offline optimization process with results being implemented in a LUT. Although optimal results can be obtained, downsides to this general approach include the fact that the optimization problem formulation and computation can be time-consuming, interpolation within a LUT can lead to error, and if a circuit parameter changes, the entire offline optimization process must be run again to generate a new LUT. A closed-form modulation scheme can overcome these drawbacks. A closed-form DCC modulation scheme for 3p-DAB, called asymmetrical DCC (ADCC), is proposed in [14]. By limiting the input and output bridge duty cycle range from 0 to 1/3 and adopting the triangular current mode and trapezoidal current mode, [14] proposes control that extends the softswitching range of the 3p-DAB under light loads. However, since the duty cycles are limited, this control strategy does not cover the entire operating range, thus, large hard switching regions still exist. Furthermore, [15] proposes a closed-form modulation scheme based on a TDA using four variables $(D_1, D_2, D_{ps}, and voltage gain)$, but this results in hundreds of operating modes, requiring simplifications and restrictions of the control mode; also, efficiency results are not provided to validate the resulting modulation scheme.

Thus, the second contribution of this research is the proposal of a novel closed-form DCC modulation scheme for the 3p-DAB, the minimum current stress optimization (MCSO) scheme, which is derived from the theoretical findings of the proposed TDA optimization method. The experimental results show that this closed-form modulation scheme performs nearly identically to the OMS, meaning this is the first research to provide a closed-form DCC modulation scheme for 3p-DAB that achieves efficiency results that are equivalent to a fully-optimized offline scheme, but without the drawbacks of the offline optimization process and LUT implementation.

1.2 Contributions

To summarize the contributions of this research, the first contribution is to propose a DCC strategy for the 3p-DAB based on a novel comprehensive piece-wise time-domain analysis and optimization process that obtains the optimal DCC control parameters for minimum RMS phase current in buck and boost operation. The second contribution is to propose a novel closed-form DCC modulation scheme for the 3p-DAB, the minimum current stress optimization (MCSO) scheme, which is derived from the theoretical findings of the proposed TDA optimization method that reduces the transformer RMS phase currents and extends the soft-switching region across a wide voltage and power range. The proposed MCSO control scheme is the first closed-form DCC scheme for the 3p-DAB to achieve equivalent efficiency performance to the offline optimized minimum RMS current DCC scheme, OMS. The research in this thesis has been submitted to the IEEE Transactions on Power Electronics as follows: G. Schulz and J. Bauman, "Time Domain Analysis and Optimization of a Three-Phase Dual-Active-Bridge Converter with Variable

Duty Cycle Modulation," submitted to IEEE Transactions on Power Electronics, February 2023.

1.3 Outline of the Thesis

The remainder of this thesis is organized as follows: Chapter 2 presents the TDA of the 3p-DAB with DCC, along with equations for the operating mode boundaries and their analytical expressions for average output power and RMS phase current. (The full set of analytic expressions for the selected optimal modes are given in Chapter 3 and those for the remaining sub-optimal modes are given in Appendix A.) Chapter 3 proposes the TDA optimization process and analyzes the results of the OMS for buck and boost operation. Chapter 4 presents the novel closed-form modulation scheme, MCSO, which builds upon the TDA fundamentals derived in Chapter 2. Chapter 5 presents the component selection and discusses the design considerations and challenges for the 3p-DAB experimental prototype. Chapter 6 presents the experimental results, verifying the exceptional performance of the proposed closed-form MCSO scheme compared to SPS, OMS, and the only other validated 3p-DAB closed-form DCC scheme from the literature, the ADCC [14]. Lastly, Chapter 7 concludes this research and provides motivations for future work.

Chapter **2**

Time-Domain Analysis of 3p-DAB with

Duty-Cycle Control

2.1 Overview of 3p-DAB with Duty-Cycle Control

Fig. 2-1(a) illustrates the circuit schematic of a 3p-DAB converter and Fig. 2-1(b) shows the corresponding equivalent circuit. V_I and V_2 are the input and output DC voltages, I_I and I_2 are the input and output DC currents and C_I and C_2 are the input and output filter capacitances. The input bridge is composed of switches S_{11} - S_{16} and the output bridge is composed of switches S_{21} - S_{26} . Connecting the two active bridges together is a balanced three-phase high-frequency Y-Y transformer with turns ratio I:n. Inductors L_a , L_b , and L_c are equal and represent the transformer leakage inductance. i_{La} , i_{Lb} , and i_{Lc} are the inductor currents, v_{1a} , v_{1b} , and v_{1c} are the primary side phase voltages and v_{2a} , v_{2b} , and v_{2c} are the secondary side phase voltages. The analysis carried out in this research assumes all components are ideal, thus parasitic resistances, inductances, and capacitances are not considered. Furthermore, due to the balanced and symmetrical nature of the 3p-DAB topology, only a single phase and power flow in the forward direction needs to be considered for a complete analysis.

The switch driving pulses and corresponding phase voltage and inductor current waveforms for the 3p-DAB with DCC are shown in Fig. 2-2. Fig. 2-2(a) shows that the driving pulses for each phase leg are complementary, and phase shifted by $T_s/3$, where T_s is the converter's switching period. The duration of a switching period that S_{11} , S_{12} , and S_{13} are ON is variable and denoted by D_1T_s . Similarly, the duration of a switching period that S_{21} , S_{22} , and S_{23} are ON is variable and denoted by D_2T_s . Lastly, the phase-shift between the rising edges of the driving pulses of the input and output bridges is variable and denoted by $D_{ps}T_s$. Thus, D_1 , D_2 and D_{ps} are the control parameters for the 3p-DAB under DCC and



Fig. 2-1. Circuit schematic and equivalent circuit of the 3p-DAB (a) Circuit schematic. (b) Equivalent circuit.



Fig. 2-2. Switch driving pulses and operating waveforms of the 3p-DAB with DCC. (a) Driving pulses. (b) Operating waveforms.

the range of values that they can take are given in (2-1). It is common practice with DAB converters to limit the range of D_{ps} because of the excessive reactive power that high magnitude phase-shift ratios create [16]. Thus, this research poses a practical limit of 1/6 on D_{ps} .

$$\begin{cases} 0 \le D_1 \le 1/2 \\ 0 \le D_2 \le 1/2 \\ 0 \le D_{ps} \le 1/6 \end{cases}$$
(2-1)

The phase voltages v'_{1a} (secondary referred) and v_{2a} are shown in Fig. 2-2(b). It is beneficial to define the switching function $S_{xy}(t)$ for the six phase legs of the 3p-DAB where (x = 1, 2, y = a, b, c). $S_{xy}(t)$ takes the value of 1 when a topside switch of a phase leg is ON and the value of 0 when a bottom side switch of a phase leg is ON. For example, referring to Fig. 2-2(a), $S_{2a}(t)$ is the switching function for phase leg A in the output bridge and it takes the value of 1 at time $D_{ps}T_s$ for the duration of D_2T_s and takes the value of 0 for the duration of $(1-D_2)T_s$. Since the switches in a phase leg are complementary, $S_{xy}(t)$ will either be 1 or 0, thus ambiguity in the function is avoided. Using $S_{xy}(t)$, the six-step phase voltage waveforms of the input and output bridge can be derived and are shown in (2-2) and (2-3).

$$\begin{cases} v'_{1a}(t) = \frac{nV_1[2S_{1a}(t) - S_{1b}(t) - S_{1c}(t)]}{3} \\ v'_{1b}(t) = \frac{nV_1[2S_{1b}(t) - S_{1a}(t) - S_{1c}(t)]}{3} \\ v'_{1c}(t) = \frac{nV_1[2S_{1c}(t) - S_{1a}(t) - S_{1b}(t)]}{3} \end{cases}$$
(2-2)

$$\begin{cases} v_{2a}(t) = \frac{ndV_1[2S_{2a}(t) - S_{2b}(t) - S_{2c}(t)]}{3} \\ v_{2b}(t) = \frac{ndV_1[2S_{2b}(t) - S_{2a}(t) - S_{2c}(t)]}{3} \\ v_{2c}(t) = \frac{ndV_1[2S_{2c}(t) - S_{2a}(t) - S_{2b}(t)]}{3} \end{cases}$$
(2-3)

During steady-state operation the phase voltages are periodic, and average to zero over a switching period. Using the equivalent circuit model in Fig. 2-1(b), the expression for the inductor current can be derived as,

$$i_{La}(t) = i_{La}(t_0) + \frac{1}{L_s} \int_{t_0}^t [v'_{1a}(\tau) - v_{2a}(\tau)] d\tau$$
(2-4)

where t_o denotes the beginning of the switching period and L_s is the series inductance in phase A. Assuming a balanced three phase transformer, the equations of RMS inductor current and total average transmission power can then be expressed using phase A quantities as,

$$I_{Lrms} = \sqrt{\frac{1}{T_s} \int_0^{T_s} i^2_{La}(t) dt}$$
 (2-5)

$$P_o = \frac{3n}{T_s} \int_0^{T_s} v_{1a}(t) i_{La}(t) dt$$
 (2-6)

2.2 Time-Domain Analysis – Operating Modes

The preceding analysis shows that the output power and phase current expressions of the 3p-DAB with DCC are piecewise-linear and dependent on the control parameters D_1 , D_2 , and D_{ps} . Consequently, this creates various modes of operation for the 3p-DAB



Fig. 2-3. Operating mode boundaries for the 3p-DAB with DCC. (a) Threedimensional illustration. (b) Cross section view of operating modes at fixed phase shift ratios.

within the domain of DCC described by (2-1). Since a TDA of the 3p-DAB with DCC has yet to be conducted in existing literature, Fig. 2-3 illustrates for the first time that there are

Mode	Limits on D ₁	Limits on D ₂
1	$0 < D_1 < D_{ps}$	$0 < D_2 < \left(-D_{ps} + \frac{1}{3} \right)$
2	$D_{ps} < D_1 < \left(D_2 + D_{ps}\right)$	$(D_1 - D_{ps}) < D_2 < (-D_{ps} + \frac{1}{3})$
3	$(D_2 + D_{ps}) < D_1 < \frac{1}{3}$	$0 < D_2 < \left(D_1 - D_{ps}\right)$
4	$\frac{1}{3} < D_1 < (D_{ps} + \frac{1}{3})$	$0 < D_2 < \left(-D_{ps} + \frac{1}{3} \right)$
5	$(D_2 + D_{ps} + \frac{1}{3}) < D_1 < \frac{1}{2}$	$0 < D_2 < \left(D_1 - D_{ps} - \frac{1}{3}\right)$
6	$(D_{ps} + \frac{1}{3}) < D_1 < (D_2 + D_{ps} + \frac{1}{3})$	$(D_1 - D_{ps} - \frac{1}{3}) < D_2 < (-D_{ps} + \frac{1}{3})$
7	$0 < D_1 < \left(D_2 + D_{ps} - \frac{1}{3}\right)$	$(D_1 - D_{ps} + \frac{1}{3}) < D_2 < \frac{1}{3}$
8	$(D_2 + D_{ps} - \frac{1}{3}) < D_1 < D_{ps}$	$(-D_{ps} + 1/3) < D_2 < (D_1 - D_{ps} + 1/3)$
9	$D_{ps} < D_1 < \frac{1}{3}$	$\left(-D_{ps} + \frac{1}{3}\right) < D_2 < \frac{1}{3}$
10	$\frac{1}{3} < D_1 < (D_2 + D_{ps})$	$(D_1 - D_{ps}) < D_2 < \frac{1}{3}$
11	$(D_2 + D_{ps}) < D_1 < (D_{ps} + \frac{1}{3})$	$(-D_{ps} + 1/3) < D_2 < (D_1 - D_{ps})$
12	$(D_{ps} + \frac{1}{3}) < D_1 < \frac{1}{2}$	$\left(-D_{ps} + \frac{1}{3}\right) < D_2 < \frac{1}{3}$
13	$0 < D_1 < D_{ps}$	$\frac{1}{3} < D_2 < \frac{1}{2}$
14	$D_{ps} < D_1 < (D_2 + D_{ps} - \frac{1}{3})$	$(D_1 - D_{ps} + \frac{1}{3}) < D_2 < \frac{1}{2}$
15	$(D_2 + D_{ps} - \frac{1}{3}) < D_1 < \frac{1}{3}$	$\frac{1}{3} < D_2 < (D_1 - D_{ps} + \frac{1}{3})$
16	$\frac{1}{3} < D_1 < (D_{ps} + \frac{1}{3})$	$\frac{1}{3} < D_2 < \frac{1}{2}$
17	$(D_2 + D_{ps}) < D_1 < 1/2$	$\frac{1}{3} < D_2 < (D_1 - D_{ps})$
18	$(D_{ps} + 1/3) < D_1 < (D_2 + D_{ps})$	$\left(D_1 - D_{ps}\right) < D_2 < \frac{1}{2}$
	For all operating mode	$ps: 0 < D_{ps} < \frac{1}{6}$

 TABLE 2-1

 Control Parameter Limits for Operating Modes

eighteen different operating modes for the 3p-DAB under DCC with control parameters D_1 , D_2 , and D_{ps} . Each operating mode is characterized by the set of control parameters that yield an inductor voltage waveform of the same step sequence. As a result, each operating mode requires a unique set of analytic expressions to model its operation. It is useful to visualize the operating modes as the three-dimensional regions of space that the intersections of eight boundary planes, shown in Fig. 2-3(a), create within the domain of (2-1). Table I presents a summary of the operating mode regions expressed mathematically

as inequalities of the control parameters D_1 , D_2 , and D_{ps} , which will be used to define the analytical expressions for each mode.

2.3 Time-Domain Analysis – Analytical Expressions

Fig. 2-4 illustrates examples of each operating mode's phase voltage and inductor current waveforms. To use piecewise modeling to describe the 3p-DAB with DCC, a TDA must be carried out for each of the eighteen operating modes to obtain expressions for P_{out} and I_{LRMS} . This section demonstrates the TDA for Mode 15 (M15), however, the same process can be applied to the other modes of operation. The analytical expressions of average output power and RMS phase current for the selected optimal operating modes are provided in Chapter 3 and the remaining sub-optimal modes in Appendix A.



Fig. 2-4. Operating waveforms during one switching period for the 18 operating modes of DCC. Blue: $v'_{1a}(t)$, Orange: $v_{2a}(t)$, Green: $i_{la}(t)$

To facilitate the analysis, Fig. 2-5 presents the switch driving pulses and operating waveforms for M15. Within the boundaries of all operating modes the phase current waveforms are asymmetric, periodic, and composed of twelve linear regions R1 to R12. The instances in a switching period where a switch turns ON or OFF are denoted by t_0 , t_1 , ... t_{11} and can be expressed using D_1 , D_2 and D_{ps} . Using (2-4), the piecewise time-domain expressions of the phase A current for M15 can be constructed, as shown in Table 2-2. Since the phase currents must average to zero over one switching period during steady state operation, the initial condition for the phase current $i_{La}(t_0)$ can be solved using (2-7). Table 2-3 shows the solved piecewise expressions for M15 phase current.



Fig. 2-5. Driving pulses and operating waveforms for a 3p-DAB operating with DCC.

	Operating Current Exp	pressions for Mode 15
Region	Interval Start Time	Expression of i_{La}
R1	$t_0 = t_{12} = 0$	$i_{La}(t_0) + k(2+d)(t-t_0)$
R2	$t_1 = D_{ps}$	$i_{La}(t_1) + k(2-d)(t-t_1)$
R3	$t_2 = D_2 + D_{ps} - 1/3$	$i_{La}(t_2) + 2k(1-d)(t-t_2)$
R4	$t_{3} = D_{1}$	$i_{La}(t_3) - 2kd(t-t_3)$
R5	$t_4 = 1/3$	$i_{La}(t_4) - k(1+2d)(t-t_4)$
R6	$t_5 = 1/3 + D_{ps}$	$i_{La}(t_5) - k(1+d)(t-t_5)$
R7	$t_6 = D_2 + D_{ps}$	$i_{La}(t_6) - k(1-d)(t-t_6)$
R8	$t_7 = 1/3 + D_1$	$i_{La}(t_7) + kd(t-t_7)$
R9	$t_8 = 2/3$	$i_{La}(t_8) - k(1-d)(t-t_8)$
R10	$t_9 = 2/3 + D_{ps}$	$i_{La}(t_9) - k(1-2d)(t-t_9)$
R11	$t_{10} = 1/3 + D_2 + D_{ps}$	$i_{La}(t_{10}) - k(1-d)(t-t_{10})$
R12	$t_{11} = 2/3 + D_1$	$i_{La}(t_{11}) + kd(t - t_{11})$
	where, $k = \frac{nV_1}{3L_s f}$	$\frac{1}{s}, d = \frac{V_2}{nV_1}$

TABLE 2-2Operating Current Expressions for Mode 15

$$\int_{t_0}^{t_{12}} i_L(\tau) d\tau = 0$$
 (2-7)

	TABLE 2-3
	SOLVED OPERATING CURRENT EQUATIONS FOR MODE 15
-n	Expression of L for Mode 15

Region	Expression of I_a for Mode 15
R1	$i_{La1}(t) = k(6t + d - 3D_1 + 3dt - 3dD_{ps})/3$
R2	$i_{La2}(t) = k(6t + d - 3D_1 - 3dt + 3dD_{ps})/3$
R3	$i_{La3}(t) = k(2t - D_1 - 2dt + dD_2 + 2dD_{ps})$
R4	$i_{La4}(t) = k(D_1 - 2dt + dD_2 + 2dD_{ps})$
R5	$i_{La5}(t) = k(1 - 3t + 3D_1 - 6dt + 3dD_2 + 6dD_{ps})/3$
R6	$i_{La6}(t) = k(1 - 3t - d + 3D_1 - 3dt + 3dD_2 + 3dD_{ps})/3$
R7	$i_{La7}(t) = k(1 - 3t - d + 3D_1 + 3dt - 3dD_2 - 3dD_{ps})/3$
R8	$i_{La8}(t) = k(3t - 1 - 3D_2 - 3D_{ps})/3$
R9	$i_{La9}(t) = k(2 - 3t - d + 3dt - 3dD_2 - 3dD_{ps})/3$
R10	$i_{La10}(t) = k(2 - 3t - 3d + 6dt - 3dD_2 - 6dD_{ps})/3$
R11	$i_{La11}(t) = k(2 - 3t - 2d + 3dt - 3dD_{ps})/3$
R12	$i_{La12}(t) = k(3dt - 2d - 3D_1 - 3dD_{ps})/3$
	where, $k = \frac{nV_1}{3L_sf_s}, d = \frac{V_2}{nV_1}$

The average output current expression for M15 can be constructed by analyzing the switching sequence of the output bridge switching functions $S_{2a}(t)$, $S_{2b}(t)$, and $S_{2c}(t)$ during 1/3 of a switching period i.e., regions R1 to R4 or equivalently, t_0 to t_4 as notated in Fig. 2-5. In region R1, only $S_{2c}(t)$ is ON, thus, the output current during this interval is $i_{Lcl}(t)$. So far, the phase current expressions developed in this research have been for phase A, however, it is possible to determine the phase B and phase C current expressions from phase A by delaying the phase A current waveform by 120° and 240°, respectively. Therefore, $i_{Lcl}(t)$ is equivalent to $i_{La5}(t)$. In R2, only $S_{2a}(t)$ and $S_{2c}(t)$ are ON, thus, the output current during this interval is the sum of $i_{La2}(t)$ and $i_{Lc2}(t) = i_{La6}(t)$. In R3 and R4, only $S_{2a}(t)$ is ON, thus, the output current during these intervals is equivalent to $i_{La3}(t)$ and $i_{La4}(t)$ respectively. The resulting expression for the average output current for M15 is provided in (2-8). Solving (2-8) and multiplying it with the output voltage $V_2 = ndV_1$, the average output power expression for M15 can be obtained as shown in (2-9). The equation for the RMS phase current of M15 can be derived by substituting the twelve piecewise equations from Table 2-3 into (2-5) and solving the integral. The result is shown in (2-10). It is worth mentioning that operating in M5 and M6 results in negative average power transfer, meaning that power flows from the output bridge to the input bridge because of the large difference between control parameters D_1 and D_2 . Because of this, M5 and M6 are not analyzed in detail.

$$I_{out_{M15}} = 3\left(\int_{t_4}^{t_5} i_{La5}(\tau)d\tau + \int_{t_1}^{t_2} i_{La2}(\tau)d\tau + \int_{t_5}^{t_6} i_{La6}(\tau)d\tau + \int_{t_2}^{t_3} i_{La3}(\tau)d\tau + \int_{t_3}^{t_4} i_{La4}(\tau)d\tau\right)$$
(2-8)

$$P_{out_{M15}} = \frac{V_1^2 n^2 d}{18L_s f_s} \left(-18D_1^2 + 18D_1 D_2 + 36D_1 D_{ps} - 9D_2^2 - 18D_2 D_{ps} + 6D_2 - 27D_{ps}^2 + 6D_{ps} - 1 \right)$$
(2-9)

$$I_{LRMS_{15}} = \frac{-V_1 n}{9\sqrt{3}L_s f_s} \left(9d^2 D_2^2 - 9d^2 D_2 + d^2 - 54dD_1^3 + 81dD_1^2 D_2 + 162dD_1^2 D_{ps} - 81dD_1 D_2^2 - 162dD_1 D_2 D_{ps} + 36dD_1 D_2 - 162dD_1 D_{ps}^2 + 27dD_2^3 + 81dD_2^2 D_{ps} - 27dD_2^2 + 81dD_2 D_{ps}^2 - 54dD_2 D_{ps} + 9dD_2 + 81dD_{ps}^3 - 27dD_{ps}^2 + 9dD_{ps} - d + 27D_1^3 - 18D_1^2\right)^{1/2}$$

$$(2-10)$$

2.4 Summary

This chapter provided an overview of DCC for the 3p-DAB and presented a novel time-domain analysis based on the DCC control parameters D_1 , D_2 , and D_{ps} . Resulting from the analysis, eighteen unique operating modes were defined and the process for deriving the analytical expressions for average output power and RMS phase current were carried out for M15.

Chapter **3**

Proposed Optimization Strategy

3.1 Optimization Problem Formulation

Optimizing the control parameters D_1 , D_2 , and D_{ps} for minimum conduction loss across all operating points (d, P_{ref}) means that the ohmic losses of the semiconductor devices, high-frequency transformer, and PCB traces are minimized. Since the ohmic losses for a 3p-DAB are proportional to the square of the RMS phase current (I_{Lrms}^2) it leads to the optimization problem given by (3-1). The nature of the objective and equality constraint functions are piecewise smooth across the domain of DCC; thus, an optimization problem must be defined for each operating mode using the expressions derived in Chapter 2. The objective function ensures that the ohmic losses are minimized, the non-linear equality constraint ensures that the operating point (d, P_{ref}) is satisfied, and the linear inequality constraints constrain D_1 , D_2 , and D_{ps} to the domain of the operating mode j that both the objective function and equality constraint belong to.

$$\min I_{LRMSj}^{2} (D_{1}, D_{2}, D_{ps}, d)$$

$$Subject to$$

$$P_{outj}(D_{1}, D_{2}, D_{ps}, d) - P_{ref} = 0$$

$$A_{j}X \leq b_{j}, where X = \begin{bmatrix} D_{1} \\ D_{2} \\ D_{ps} \end{bmatrix}, 1 \leq j \leq 18$$
(3-1)

3.2 Selection of Optimal Operating Modes

The active-set method from MATLAB's Optimization Toolbox was implemented to solve the non-linear optimization problem for each mode. Then, the global optimal control parameters were obtained by means of comparison to determine which mode's optimal control yielded the lowest RMS phase current for a given operating point (d, P_{ref}). Fig. 3-1

shows curves for each operating mode's locally minimized RMS phase current as a function of output power during buck operation (d = 0.6), where the optimal modes are shown in bold. For buck operation, operating in M2 during low-power, M15 during medium-power, and M16 during high-power achieves the globally minimized RMS phase currents across the entire output power range. A similar analysis for boost operation shows that globally minimized RMS phase current across the entire output power range can be achieved by operating in M3 during low-power, M10 during medium-power, and M16 during highpower. Fig. 3-2 illustrates the five optimal operating mode regions that contribute to the OMS as well as their turn-on soft-switching characteristics.



Fig. 3-1. Locally minimized RMS current curves for each DCC operating mode for buck operation (d = 0.6). M2, M15, and M16 achieve global minimum RMS phase current for entire output power range.



Fig. 3-2. Operating modes and turn-on soft-switching characteristics of OMS scheme in terms of voltage gain d and output power normalized to P_{base}.

3.3 Analysis of Optimal Operating Modes

The preceding section revealed that only five of the eighteen DCC operating modes contribute to the OMS, thus the remaining modes can be considered sub-optimal and are therefore redundant. The optimal control surfaces for D_1 , D_2 , and D_{ps} are shown in Fig. 3-3 where the voltage gain *d* ranges from 0.5 (buck) to 1.5 (boost) and the output power is normalized to $P_{base} = V_1^2 n^2 / (12L_s f_s)$. Fig. 3-4(a)-(b) shows curves of the control parameters for buck operation, where the voltage gain *d* is fixed to 0.6 and 0.8 respectively. Fig. 3-4(c)-(d) shows the corresponding RMS phase currents normalized to $I_{base} = V_1 n / (12L_s f_s)$, and highlights the theoretical improvement of the proposed OMS over SPS control through the significant reduction of RMS phase current during low to medium power transmission. Fig. 3-5 shows similar theoretical results for boost operation, with d = 1.2 and 1.4.



Fig. 3-3. Optimized control parameter surfaces to achieve minimum RMS phase current in buck and boost operation.



Fig. 3-4. (a)-(b) Two-dimensional curves of OMS control parameters with fixed buck voltage gain. (c)-(d) Comparison of RMS phase current - SPS vs. OMS.



Fig. 3-5. (a)-(b) Two-dimensional curves of OMS control parameters with fixed boost voltage gain. (c)-(d) Comparison of RMS phase current - SPS vs. OMS.

3.4 Optimal Operating Modes – Analytical Expressions

For completeness, this sub-section presents the analytical expressions for average output power (3-2)-(3-6) and RMS phase current (3-7)-(3-11) for the five optimal operating modes i.e., the objective functions and non-linear equality constraints respectively for the optimization problem. Considering only the optimal operating mode expressions provided by (3-2)-(3-11) when solving the optimization problem (3-1) streamlines its implementation by reducing the number of computations by not considering the sub-
optimal operating modes. However, the sub-optimal operating mode expressions are provided in Appendix A.

$$P_{outM2} = \frac{dV_1^2 n^2}{L_s f_s} \left(-D_1^2 + 2D_1 D_{ps} + D_2 D_1 - D_{ps}^2 \right)$$
(3-2)

$$P_{outM3} = \frac{dV_1^2 n^2 D_2}{L_s f_s} \left(D_2 - D_1 + 2D_{ps} \right)$$
(3-3)

$$P_{outM10} = \frac{-dV_1^2 n^2}{18L_s f_s} (18D_1^2 - 18D_1D_2 - 36D_1D_{ps} + 9D_2^2 + 18D_2D_{ps} - 6D_2 + 27D_{ps}^2 - 6D_{ps} + 1)$$
(3-4)

$$P_{outM15} = P_{outM10} \tag{3-5}$$

$$P_{outM16} = P_{outM10} \tag{3-6}$$

$$I_{LRMS_{M2}} = \frac{V_1 n}{3\sqrt{3}L_s f_s} \left(-3d^2 D_2^3 + 2d^2 D_2^2 + 6dD_1^3 - 9dD_1^2 D_2 - 18dD_1^2 D_{ps} + 9dD_1 D_2^2 + 18dD_1 D_2 D_{ps} - 4dD_1 D_2 + 18dD_1 D_{ps}^2 - 6dD_{ps}^3 - 3D_1^3 + 2D_1^2\right)^{1/2}$$
(3-7)

$$I_{LRMS_{M3}} = \frac{V_1 n}{3\sqrt{3}L_s f_s} \left(-3d^2 D_2^3 + 2d^2 D_2^2 + 9dD_1^2 D_2 - 9dD_1 D_2^2 - 18dD_1 D_2 D_{ps} - 4dD_1 D_2 + 6dD_2^3 + 18dD_2^2 D_{ps} + 18dD_2 D_{ps}^2 - 3D_1^3 + 2D_1^2\right)^{1/2}$$
(3-8)

$$I_{LRMS_{M10}} = \frac{-V_1 n}{9\sqrt{3}L_s f_s} \left(27d^2 D_2^3 - 18d^2 D_2^2 - 54dD_1^3 + 81dD_1^2 D_2 + 162dD_1^2 D_{ps} - 81dD_1 D_2^2 - 162dD_1 D_2 D_{ps} + 36dD_1 D_2 - 162dD_1 D_{ps}^2 + 27dD_2^3 + 81dD_2^2 D_{ps} - 27dD_2^2 + 81dD_2 D_{ps}^2 - 54dD_2 D_{ps} + 9dD_2 + 81dD_{ps}^3 - 27dD_{ps}^2 + 9dD_{ps} - d + 9D_1^2 - 9D_1 + 1\right)^{1/2}$$

$$(3-9)$$

$$I_{LRMS_{M15}} = \frac{-V_1 n}{9\sqrt{3}L_s f_s} \left(9d^2 D_2^2 - 9d^2 D_2 + d^2 - 54dD_1^3 + 81dD_1^2 D_2 + 162dD_1^2 D_{ps} - 81dD_1 D_2^2 - 162dD_1 D_2 D_{ps} + 36dD_1 D_2 - 162dD_1 D_{ps}^2 + 27dD_2^3 + 81dD_2^2 D_{ps} - 27dD_2^2 + 81dD_2 D_{ps}^2 - 54dD_2 D_{ps} + 9dD_2 + 81dD_{ps}^3 - 27dD_{ps}^2 + 9dD_{ps} - d + 27D_1^3 - 18D_1^2\right)^{1/2}$$
(3-10)

$$I_{LRMS_{M16}} = \frac{-V_1 n}{9\sqrt{3}L_s f_s} \left(9d^2 D_2^2 - 9d^2 D_2 + d^2 - 54dD_1^3 + 81dD_1^2 D_2 + 162dD_1^2 D_{ps} - 81dD_1 D_2^2 - 162dD_1 D_2 D_{ps} + 36dD_1 D_2 - 162dD_1 D_{ps}^2 + 27dD_2^3 + 81dD_2^2 D_{ps} - 27dD_2^2 + 81dD_2 D_{ps}^2 - 54dD_2 D_{ps} + 9dD_2 + 81dD_{ps}^3 - 27dD_{ps}^2 + 9dD_{ps} - d + 9D_1^2 - 9D_1 + 1\right)^{1/2}$$
(3-11)

3.5 Summary

This chapter presented a non-linear optimization process using the proposed TDA to obtain the optimal DCC parameters for minimum RMS current operation for buck and boost voltage gains. The optimization results revealed that only five of the eighteen DCC operating modes contribute to the OMS, thus simplifying its implementation. Furthermore, the analysis carried out in this section highlighted the theoretical improvement of the proposed OMS against SPS.

Chapter 4

Proposed Closed-Form Modulation Scheme

4.1 Overview and Motivation

Due to the significant offline calculations required every time a circuit parameter changes, and the potential interpolation errors or memory limits of LUT implementations, closed-form modulation schemes are often preferable to offline optimization-based schemes in many applications. However, until now, no closed-form 3p-DAB DCC modulation scheme had been proposed in the literature which can match the performance of optimization-based schemes. The purpose of the proposed MCSO closed-form scheme is to fill this gap. The novel TDA presented in Section II is used as the theoretical basis for this proposed MCSO scheme, and thus the MCSO stands apart from other closed-form schemes as it has a rigorous base which leads to converter efficiency equivalent to that of the OMS. To construct the closed-form MCSO scheme over the entire buck and boost operating range, each of the five operating modes in Fig. 3-2 is discussed and analyzed in the following subsections.

4.2 Low-Power Buck Operation in M2 (0.5 < d < 1.0)

According to the OMS, the 3p-DAB operates in M2 during low-power buck operation. Analyzing the numerical solutions of the optimized control parameters in M2 from Fig. 3-4(a)-(b) reveals that $D_{ps} = 0$, and $D_1 = dD_2$. Substituting these into the average output power expression for M2 (3-2) gives the closed-form expression for D_2 (4-1) in terms of P_{out} , d, and converter parameters to achieve minimum RMS phase current. The maximum power transfer while operating in M2 is presented in (4-2) and can be deduced from (3-2) by realizing that at the upper power boundary of M2, D_2 is always equal to 1/3.

$$\begin{cases} D_2 = \sqrt{\frac{P_{out}L_sf_s}{d^2V_1^2n^2(1-d)}} \\ D_1 = dD_2 \\ D_{ps} = 0 \end{cases}$$
(4-1)

$$0 < P_{out} < \frac{V_1^2 d^2 n^2 (1-d)}{9L_s f_s}$$
(4-2)

4.3 Low-Power Boost Operation in M3 (1.0 < d < 1.5)

Similarly, according to the OMS, the 3p-DAB operates in M3 during low-power boost operation. Analyzing the numerical solutions of the optimized control parameters in M3 from Fig. 3-5(a)-(b) reveals that $D_2 = D_{ps}/(d-1)$, and $D_1 = dD_2$. Substituting these into the average output power expression for M3 (3-3) allows derivation of the closed-form expression for D_{ps} (4-3) in terms of P_{out} , d, and converter parameters to achieve minimum RMS phase current. The maximum power transfer while operating in M3 is presented in (4-4) and can be deduced from (3-3) by realizing that at the upper boundary of M3, D_1 is always equal to 1/3.

$$\begin{cases} D_{ps} = (d-1) \sqrt{\frac{P_{out}L_s f_s}{dV_1^2 n^2 (d-1)}} \\ D_2 = \frac{D_{ps}}{(d-1)} \\ D_1 = dD_2 \end{cases}$$
(4-3)

$$0 < P_{out} < \frac{V_1^2 n^2 (d-1)}{9 dL_s f_s}$$
(4-4)

4.4 Medium-Power Buck Operation in M15 (0.5 < d < 1.0)

According to the OMS, the 3p-DAB operates in M15 during medium-power buck operation. Analyzing the numerical solutions of the optimized control parameters in M15 from Fig. 3-4(a)-(b) reveals no apparent parametrization of the optimal control variables, thus closed-form solutions for the control parameters in M15 cannot be obtained like they were for M2 and M3. Therefore, instead of using RMS phase current as the objective function, current stress is used to conveniently allow for an analytical optimization using the Global Optimal Conditions (GOC) proposed in [17] due to the linear nature of the peak current expressions of the 3p-DAB. The GOC for minimum current stress for a 3p-DAB with DCC is defined in (4-5),

$$\frac{\frac{\partial i_{p_{Mj}}}{\partial D_1}}{\frac{\partial P_{Mj}}{\partial D_1}} = \frac{\frac{\partial i_{p_{Mj}}}{\partial D_2}}{\frac{\partial P_{Mj}}{\partial D_2}} = \frac{\frac{\partial i_{p_{Mj}}}{\partial D_{ps}}}{\frac{\partial P_{Mj}}{\partial D_{ps}}}$$
(4-5)

where i_{PMj} is the expression for the peak current in Mode *j*, and P_{Mj} is the expression for average output power in Mode *j*. While operating in M15, the peak current and average output power expressions are given by (4-6) and (3-5) respectively. Computing their partial derivatives with respect to D_1 , D_2 , and D_{ps} and substituting them into the GOC (4-5) yields the system of equations given by (4-7). Solving (4-7) yields expressions for D_1 and D_2 in terms of D_{ps} and can be substituted into (3-5) to solve for the expression of D_{ps} in terms of P_{out} , *d*, and converter parameters. The resulting closed-form control parameters to achieve minimum current stress in M15 are given by (4-8). The upper power boundary of M15 as shown in Fig. 3-2 does not have a closed-form expression, thus a numerical solver is used, and a fourth order polynomial is fit to the numerical solution which accurately defines the upper power boundary of M15 (4-9).

$$i_{p_{M15}} = \frac{V_1 n}{3L_s f_s} \left(D_1 - 2dD_1 + dD_2 + 2dD_{ps} \right)$$
(4-6)

$$\frac{1-2d}{3d(D_2-2D_1+2D_{ps})} = \frac{1}{3D_1-3D_2-3D_{ps}+1} = \frac{2}{6D_1-3D_2-9D_{ps}+1}$$
(4-7)

$$\begin{cases} D_{ps} = \frac{1}{3} - \frac{\sqrt{d(V_1^2 n^2 d - 9L_s f_s P_{out})}}{3V_1 n d \sqrt{d^2 - d + 1}} \\ D_1 = (2 - d) D_{ps} + \frac{d}{3} \\ D_2 = D_{ps} + \frac{1}{3} \end{cases}$$

$$\frac{P_{out}}{P_{base}} < \begin{bmatrix} -2.779 & 4.526 & -3.891 & 2.319 & -0.175 \end{bmatrix} \begin{bmatrix} d^4_n \\ d^3_n \\ d^2_n \\ d^1_n \end{bmatrix}$$
(4-9)

4.5 Medium-Power Boost Operation in M10 (1.0 < d < 1.5)

Similarly, according to the OMS, the 3p-DAB operates in M10 during medium power boost operation. Analyzing the numerical solutions of the optimized control parameters in M10 from Fig. 3-5(a)-(b) reveals no apparent parametrization of the optimal control variables, thus closed-form solutions for the optimal control parameters in M10 cannot be obtained like they were for M2 and M3. Again, instead of using RMS phase current as the objective function, current stress is used to conveniently allow for an analytical optimization using the GOC. While operating in M10, the peak current and average output power expression are given by (4-10) and (3-4) respectively. Computing their partial derivatives with respect to D_1 , D_2 , and D_{ps} and substituting them into (4-5) yields the system of equations given by (4-11). Solving (4-11) yields expressions for D_1 and D_2 in terms of D_{ps} and can be substituted into (3-4) to solve for the expression of D_{ps} in terms of P_{out} , d, and converter parameters. The resulting closed-form control parameters to achieve minimum current stress in M10 are given in (4-12). The upper power boundary of M10 as shown in Fig. 3-2 does not have a closed-form expression, thus a numerical solver is used, and a fourth order polynomial is fit to the numerical solution which accurately defines the upper power boundary of M10 (4-3).

$$i_{p_{M10}} = \frac{V_1 n}{3L_s f_s} \left(-D_1 + dD_2 + 2D_{ps} \right)$$
(4-10)

$$\frac{-1}{3d(D_2 - 2D_1 + 2D_{ps})} = \frac{1}{3D_1 - 3D_2 - 3D_{ps} + 1}$$

$$= \frac{12}{d(36D_1 - 18D_2 - 54D_{ps} + 6)}$$

$$\begin{cases} D_{ps} = \frac{1}{3} - \frac{\sqrt{d(V_1^2 n^2 d - 9L_s f_s P_{out})}}{3V_1 n d\sqrt{d^2 - d + 1}} \\ D_1 = dD_{ps} - \frac{d}{3} + \frac{2}{3} \\ D_2 = (2d - 1)D_{ps} - \frac{2d}{3} + 1 \end{cases}$$
(4-11)
(4-12)

$$\frac{P_{out}}{P_{base}} < \begin{bmatrix} -2.779 & 15.748 & -34.469 & 35.706 & -14.229 \end{bmatrix} \begin{bmatrix} d^4 \\ d^3 \\ d^2 \\ d^1 \\ d^0 \end{bmatrix}$$
(4-13)

4.6 High-Power Buck and Boost Operation in M16 (0.5 < d < 1.5)

According to the OMS, the 3p-DAB operates in M16 during high power buck and boost operation. Analyzing the numerical solutions of the optimized control parameters in M16 from Fig. 3-4(a)-(b) and Fig. 3-5(a)-(b) reveals no apparent parametrization of the optimal control variables, thus closed-form solutions for the optimal control parameters in M16 cannot be obtained like they were for M2 and M3. However, close inspection of Fig. 3-4(c)-(d) and Fig. 3-5 (c)-(d)in the region of M16 reveals that the RMS phase current of SPS is almost equal to the RMS phase current of the OMS, and in fact the magnitude of the RMS phase current of the OMS converges to SPS when the voltage gain is close to unity or when the power transfer is large. Because of this, the proposed modulation scheme, MCSO, operates the 3p-DAB using SPS in M16. The closed-form control parameters for SPS modulation are provided in (4-14) and the upper power boundary is given in (4-15) when $D_{ps} = 1/6$.

$$\begin{cases} D_{ps} = \frac{1}{3} - \frac{1}{3} \sqrt{1 - \frac{9L_s f_s P_{out}}{V_1^2 n^2 d}} \\ D_1 = D_2 = \frac{1}{2} \end{cases}$$

$$P_{out} < \frac{V_1^2 n^2 d}{12L_s f_s}$$
(4-15)

4.7 Concluding Remarks on MCSO

The preceding subsections present the MCSO modulation scheme closed-form control and operating mode power boundary expressions to operate the 3p-DAB efficiently

using DCC under wide voltage and power variations. This sub-section discusses the notable features of the proposed MCSO scheme which contribute to its excellent performance.

When operating in M2 and M3, the phase current waveforms of the 3p-DAB are triangular and all switches experience either zero-current switching (ZCS) or zero-voltage switching (ZVS) at turn-on as proven in Appendix B. Operating the 3p-DAB with triangular phase currents during low power operation has been discussed previously in [14], [12], however, in [14] it was not concluded if in fact minimum RMS current operation was achieved and in [12] analysis of the low power boost operation was not considered (i.e., M3 of the proposed MCSO) and no closed-form expressions for the control parameters were provided.

During medium power transmission and wide voltage variation, the proposed MCSO modulation scheme operates in M15 for buck voltage gains and M10 for boost voltage gains. While operating in these modes, local minimum current stress (MCS) is achieved which reduces the magnitude of the RMS phase current when compared to SPS. Additionally, while operating in M15 and M10, all switches experience ZVS at turn-on as proven in Appendix B whereas if operating using SPS, hard-switching (HSW) would occur in either the primary or secondary bridge.

During high power transmission and buck or boost voltage gain, the proposed MCSO modulation scheme operates the 3p-DAB using SPS. In this region, SPS produces RMS phase currents very close to the global minimum and achieves ZVS at turn-on for the vast majority of the operating region except for the two small regions above M15 and M10. Fig. 4-1 summarizes the features of each MCSO operating mode. Combined, these features



Fig. 4-1. Annotated operating mode regions of the MCSO modulation scheme in terms of voltage gain d and output power normalized to P_{base}.

allow the proposed closed-form MCSO modulation scheme to achieve nearly identical efficiencies as the OMS under wide voltage and power variations.

4.8 Summary

This chapter proposed a novel closed-form DCC modulation strategy, MCSO, which was derived from the theoretical findings of the proposed TDA optimization method. The proposed MCSO scheme has five operating modes spanning a wide voltage and power range thereby extending the soft-switching region and greatly reducing the RMS phase currents of the 3p-DAB converter.

Chapter 5

3p-DAB Hardware Design

5.1 Design Methodology

A 500 W 3p-DAB experimental prototype was designed and built to verify the theoretical analysis presented in Chapters 2 to 5. The complete specifications of the prototype are listed in Table 5-1. Based on the defined rated power, input DC voltage, switching frequency, transformer turns ratio, and maximum allowable phase-shift ratio of 1/6, the required per-phase leakage inductance was calculated to be 83.33 uH using (5-1). It is worth mentioning that the converter was designed to achieve the rated power at unity voltage gain i.e., d = 1.0.

TABLE 5-1			
Parameters for 3p-DAB Prototype			
Parameter	Value		
Rated power (<i>P</i> _{rated})	500 W		
Input DC voltage (V ₁)	100 V		
Output DC voltage (V ₂)	60 V ~ 120 V		
Transformer turns ratio (1:n)	1:1		
Switching frequency (f _s)	20 kHz		
Leakage inductance (L _s)	83.33 μH		
Input capacitance (C _{in})	275 µF		
Output capacitance (Cout)	275 µF		

$$L_{s} = \frac{V_{1}^{2} n^{2} d}{9 f_{s} P_{rated}} \left(1 - \left(1 - 3 D_{ps} \right)^{2} \right)$$
(5-1)

5.2 Hardware Component Selection

To effectively build the 3p-DAB prototype according to the specifications outlined in Table 5-1, the hardware components had to be appropriately selected. This sub-section presents the hardware component selection process along with justifications for each component choice.

The Texas Instruments LaunchXL-F28379D development board was selected as the microcontroller for the 3p-DAB prototype because of its 200 MHz clock frequency, 16 ePWM modules, and ability to serially communicate to a host PC running MATLAB/Simulink.

One of the most important decisions made in regard to the hardware component selection process was the choice of the silicon switching devices. The switching frequency, rated power and operating voltage levels chosen for this prototype suggest the use of N-channel power MOSFETs as the switching device. However, to implement DCC accurately, it was important for the switch's dead-time to be small relative to the converter's switching period, thus, the switches needed to have extremely fast rise and fall times. Therefore, these requirements were satisfied by using twelve C3M0045065K Silicon Carbide (SiC) MOSFETs from Cree Wolfspeed because of their quick rise and fall times, suitable V_{DS} breakdown voltage and low on-state resistance. The C3M0045065K is a discrete 650V N-channel SiC MOSFET in a TO-247-4L package which allows for excellent power dissipation through the large drain tab and minimized gate-source loop inductance because of the added driver source lead.

Six Si823H half-bridge gate drive boards from Skyworks Solutions were paired with Wolfspeed's CGD12HB00D dual channel differential transceiver boards to effectively drive the twelve SiC MOSFETs with +15V/-3V powered signals. The half-bridge gate driver boards provide a 200 ns deadtime between each of the half-bridge MOSFETs as well

as isolate the power circuit from the control circuit, both of which ensure safe and reliable converter operation. Additionally, the dual channel differential transceiver boards protect the control signals from EMI generated from the power circuit by transmitting the microcontrollers single ended PWM signals as differential pairs.

A combination of film, ceramic and electrolytic capacitors were used in the power circuit to improve the transient performance of the prototype. The electrolytic capacitors were used to provide energy to the DC bus during transient operation between two steady states. Film and ceramic capacitors were used to mitigate the input and output DC bus ripple voltage and to reduce the length of high di/dt current loops in the circuit.

The three-phase high frequency transformer was designed and built from ecraftsmen, a custom magnetics company based out of Waterloo, Ontario. The three-phase transformer was implemented using three single-phase Y-Y connected high-frequency transformers with ETD49 cores. The leakage inductance was incorporated into each singlephase transformer for a more power-dense solution. Due to the possibility of magnetic-flux saturation of the transformer core resulting from DC-bias currents generated by the asymmetrical waveforms of the proposed MCSO modulation scheme, it is suggested to design the transformers with a small airgap in the core to ensure stable operation of the converter [4].

Thermal management was another important aspect to consider when determining the hardware for this prototype. Six half-bridge heatsinks were used to dissipate the heat generated from the losses of the twelve MOSFETs. Moreover, forced air convection via two small 12 Vdc BLDC fans (one for each three-phase H-Bridge) was implemented to further improve the thermal performance of the converter. Lastly, since TO-247-4L packaged MOSFETs have their drain terminals electrically connected to the backside of the package, an electrically insulating thermal interface material (TIM) was selected to ensure electrical isolation between MOSFETs mounted to the same heatsink.

5.3 PCB Design Considerations

Once all of the hardware components were selected, the PCB had to be meticulously designed to mitigate the parasitic effects that can arise due to improper PCB design and layout. The first step during the design was the component layout. Components of the input and output bridges were positioned symmetrically to ensure any introduced parasitic elements were balanced and minimized. Additionally, components were placed as close as possible to reduce the stray inductances and resistances that could affect the performance of the prototype. The symmetrical component layout is highlighted in Fig. 5-1.

Once the locations of all the components was finalized, the copper traces were formed using the EDA software's copper area tool. The complexity of the 3p-DAB power circuit required a 4-layer PCB with each layer having a copper weight of 2 oz. As shown in Fig. 5-2, traces belonging to the same power loop were overlapped as much as possible to increase their mutual inductance. Due to topology constraints in the layout, the overlapping of traces belonging to different power loops was unavoidable. Illustrated in Fig. 5-3, the overlap between the red phase traces and DC bus traces was minimized to reduce the capacitive coupling between them. The fast rise and fall times of the switching devices create high di/dt loops in the phase legs of the power circuit, which if not dealt with correctly in the PCB layout, would create large voltage transients across the switches during operation. Shown in Fig. 5-4, the trace length of these loops was minimized by adding film and ceramic capacitors close to each phase leg to ensure safe and reliable operation of the converter. Shown in Fig. 5-5, the traces connecting the outputs of the gate driver board to the MOSFET gate and driver source pins were made as short as possible and did not overlap with other traces in the power circuit in order to minimize stray inductances and capacitive coupling. Lastly, the complete PCB layout with traces is shown in Fig. 5-6.



Fig. 5-1. Symmetrical layout of components on 3p-DAB prototype PCB.



Fig. 5-2. Overlap of DC bus traces to increase mutual inductance in power loop



Fig. 5-3. Small overlap of phase traces (red) with DC bus trace (blue) to minimize their capacitive coupling.



Fig. 5-4. Addition of ceramic capacitors to reduce the high di/dt loop length.



Fig. 5-5. Short trace lengths to reduce parasitic inductance in the gate-source loop.



Fig. 5-6. Completed PCB layout

5.4 Summary

This chapter discussed the hardware design for the 3p-DAB prototype used in the proceeding chapter of this research. The 3p-DAB design methodology was presented and the specifications for the prototype were provided. Next the hardware component selection was discussed in detail in order to realize a converter with the defined specifications. Furthermore, the critical design choices made during the PCB layout were discussed.

Chapter 6

Experimental Verification

6.1 Overview of Experimental Setup

As discussed in Chapter 5, a 500 W 3p-DAB experimental prototype, shown in Fig. 6-1, was built and tested to validate the theoretical results. The proposed MCSO modulation scheme is experimentally compared to the traditional SPS modulation scheme [5], the proposed OMS using TDA (which is representative of the optimized modulation scheme given in [12], yet has the advantage of not requiring multi-frequency approximation), and the ADCC scheme [14] (which is the only prior validated closed-form scheme proposed for the 3p-DAB with DCC) through open-loop testing. During the experiments, the input bridge DC voltage V_1 was fixed to 100 V and the output bridge DC voltage V_2 varied depending on the desired voltage gain *d*. The input bridge DC-port was connected to a Sorenson SGX 600-25 power supply configured as a constant voltage source and the secondary bridge DC-port was connected to a Chroma 63800 electronic load configured in constant resistance mode.



Fig. 6-1. 3p-DAB experimental prototype and controller.

6.2 MCSO Operating Waveforms

Fig. 6-2. To Fig. 6-5. present the operating waveforms of the proposed closed-form MCSO modulation scheme compared to the SPS modulation scheme at various operating points. To highlight the differences between the two modulation schemes, each experiment measured the primary and secondary line voltages (V_{ab} , V_{ab}) and the output phase A transformer current (I_a) over four switching periods at identical operating points (P_{outb} , d). These waveforms capture the RMS phase current and switch turn-on events for both modulation schemes. If the body-diode of a particular switch is conducting at the turn-on instant, ZVS will be achieved [5]. Similarly, if the switch current is zero at the turn-on instant, ZCS will be achieved. Therefore, to experimentally determine whether a particular switch in a phase undergoes soft-switching at turn-on, the polarity of the phase current can be analyzed at the turn-on instant of that particular switch. Table V outlines the polarity requirements of the phase A current in order for a soft-switching event to occur in a phase A switch. The same requirements apply to phases B and C.

Fig. 6-2(a) presents the waveforms for low-power buck operation of the proposed MCSO modulation scheme and Fig. 6-2(b) shows the same for the SPS modulation scheme. In Fig. 6-2(a), the 3p-DAB operates in M2 of the MCSO thus the phase current is triangular. As a result, MCSO achieves soft-switching at turn-on for all phase A switches (S_{11} , S_{14} , S_{21} , and S_{24}) and leads to a substantial reduction in RMS phase current when compared to SPS. Fig. 6-2(b) shows that when using SPS at the same operating point, the phase A output bridge switches S_{21} and S_{24} undergo hard-switching at turn-on. Although these experimental waveforms are only for phase A, the balanced nature of this converter across

all phases means that the respective switches in phases B and C undergo the same switching stresses as in phase A. Fig. 6-3 presents similar results for low-power boost operation (M3 in MCSO), the difference being that for SPS modulation shown in Fig. 6-3(b), the phase A input bridge switches S_{11} and S_{14} undergo hard-switching at turn-on. Since the MCSO modulation scheme in the low-power range dramatically reduces the RMS phase current and achieves ZCS/ZVS for all switches, the total losses are much lower than when operating with SPS, thereby improving the converter's efficiency from 93.31% to 97.01% in M2 and 92.28% to 98.11% in M3.

Similarly, Fig. 6-4(a) presents the waveforms for medium-power buck operation of the proposed MCSO modulation scheme, and Fig. 6-4(b) shows the same for the traditional SPS modulation scheme. In Fig. 6-4(a), the 3p-DAB operates with the MCSO scheme in M15. As a result, this modulation scheme enables ZVS at turn-on for all phase A switches (S_{11} , S_{14} , S_{21} , and S_{24}) and leads to a small reduction in RMS phase current when compared to SPS. Fig. 6-4(b) shows that when using SPS at the same operating point, the phase A output bridge switches S_{21} and S_{24} undergo hard-switching at turn-on. Fig. 6-5 presents similar results for medium-power boost operation (M10 in MCSO), the difference being that for SPS modulation shown in Fig. 6-5(b), the phase A input bridge switches S_{11} and S_{14} undergo hard-switching at turn-on. Since the MCSO scheme in the medium-power range reduces the RMS phase current and achieves ZVS for all switches, the total losses are lower than when operating with SPS, thereby improving the converter's efficiency from 96.34% to 97.12% in M15 and 96.45% to 97.84% in M10.



Fig. 6-2. Comparison of MCSO and SPS operating waveforms for low-power buck operation, Pout = 50 W, d = 0.8. (a) Waveforms of MCSO in M2; (b) Waveforms of SPS



Fig. 6-3. Comparison of MCSO and SPS operating waveforms for low-power boost operation, Pout = 50 W, d = 1.2. (a) Waveforms of MCSO in M3. (b) Waveforms of SPS.



Fig. 6-4. Comparison of MCSO and SPS operating waveforms for medium-power buck operation, Pout = 150 W, d = 0.8. (a) Waveforms of MCSO in M15. (b) Waveforms of SPS.



Fig. 6-5. Comparison of MCSO and SPS operating waveforms for medium-power boost operation, Pout = 150 W, d = 1.2. (a) Waveforms of MCSO in M10. (b) Waveforms of SPS.

PHASE A TURN-ON SOFT-SWITCHING REQUIREMENTS			
Switch	$I_{La} < 0$	$I_{La} > 0$	$I_{La} = 0$
S ₁₁	ZVS	HSW	ZCS
S_{14}	HSW	ZVS	ZCS
S_{21}	HSW	ZVS	ZCS
S_{24}	ZVS	HSW	ZCS

TABLE 6-2

6.3 **Efficiency Performance**

The 3p-DAB efficiency and RMS currents are measured over a wide range of output voltages and power levels to assess the performance of the proposed closed-form MCSO modulation scheme. Fig. 6-6(a) shows the measured efficiency of all 4 compared modulation schemes at a constant output power of 150 W(0.3 p.u.) with the output voltage varying from 60 V (d = 0.6) to 120 V (d = 1.2). Fig. 6-6(b) shows the RMS current for the 4 modulation schemes over the same operating points. Fig. 6-6(a) shows that the efficiency of the 3p-DAB converter with SPS modulation decreases as the voltage gain deviates from unity because of the increase in RMS phase currents and loss of soft-switching operation. At this power level, the ADCC modulation scheme proposed in [14] operates in trapezoidal current mode and suffers from increased RMS phase currents, even at voltage gains close to unity. The proposed MCSO scheme overcomes these drawbacks by minimizing the current stress and extending the soft-switching operating region of the 3p-DAB, thereby reducing both the switching and conduction losses at wide voltage gains. This results in an efficiency performance that very closely follows OMS and either matches or outperforms SPS and ADCC at all voltage gains. To quantify, the average of the efficiency points in Fig. 6-6(a) for OMS is 97.376% and the same average for MCSO is 97.363%. Thus, the efficiency of the closed-form MCSO is nearly identical to that of the OMS with offline optimization.

Fig. 6-7(a)-(b) presents the efficiency and RMS phase current measurements, respectively, for all 4 modulation schemes over a wide output power range and fixed buck voltage gain (d = 0.8). In the low- and medium-power region, the OMS and MCSO efficiency curves match very closely and outperform the SPS and ADCC modulation schemes. In the high-power region, ADCC and MCSO adopt SPS modulation because of its ZVS and near optimal RMS phase current operation. To quantify, the average of the efficiency points in Fig. 6-7(a) for OMS is 96.452% and the same average for MCSO is 96.414%. Again, the efficiency of the closed-form MCSO is nearly identical to that of the OMS.

Fig. 6-8(a) -(b) presents similar measured efficiency and RMS current, respectively, for a fixed boost voltage gain (d = 1.2). In the low-power region, ADCC, OMS, and the proposed MCSO modulation schemes all operate with triangular phase currents thus they achieve the same superior performance over SPS. In the medium-power region the ADCC control operates using the trapezoidal current mode. Although operation in this mode achieves ZVS, the increased RMS phase currents lead to a significant increase in conduction losses which negatively affect its efficiency. In the high-power region, the ADCC and MCSO adopt SPS modulation because of its ZVS and near optimal RMS phase current operation. Fig. 6-8(a) shows that in the high-power region, the efficiency of OMS is slightly lower than that of SPS. This phenomenon can be attributed to errors generated in the offline optimized control due to slight differences in physical parameter values and modelled parameter values. Since the OMS produces RMS phase currents nearly identical to SPS in the high-power region, small errors in the OMS control parameters will result in performance slightly worse than SPS. This phenomenon has also been seen experimentally in [14] when comparing the OMS presented in [12] to SPS, and in [13] when comparing the efficiency-optimized zero-vector modulation scheme to SPS. To quantify, the average of the efficiency points in Fig. 6-8(a) for OMS is 97.151% and the same average for MCSO is 97.242%. The average efficiency of all points in Fig. 6-6(a), Fig. 6-7(a), and Fig. 6-8(a) is 97.008% for OMS and 97.021% for MCSO. Thus, the proposed closed-form MCSO modulation scheme has overall equivalent efficiency compared to the offline-optimized OMS, and near identical efficiency across the individual operating points.

6.4 Summary

This chapter presented the experimental results which compared the overall performance of the proposed closed-form MCSO modulation scheme against SPS, OMS, and ADCC. Additionally, operating waveforms at a variety of operating points were provided for MCSO and SPS to showcase the MCSO schemes increased soft-switching range and reduction of RMS phase currents. The results showed that the closed-form MCSO performed nearly identical to the offline optimized OMS and outperformed SPS and ADCC.



Fig. 6-6. Comparison of the SPS, proposed closed-form MCSO, OMS, and ADCC modulation schemes across wide voltage gain and fixed power level (Pout = 150 W). (a) Measured efficiency. (b) Transformer RMS current.



Fig. 6-7. Comparison of the SPS, proposed closed-form MCSO, OMS, and ADCC modulation schemes across large power range and fixed buck voltage gain (d = 0.8). (a) Measured efficiency. (b) Transformer RMS current.



Fig. 6-8. Comparison of the SPS, proposed closed-form MCSO, OMS, and ADCC modulation schemes across large power range and fixed boost voltage gain (d = 1.2). (a) Measured efficiency. (b) Transformer RMS current.

Chapter 7

Conclusions and Future Work

7.1 Conclusion

This research proposed a DCC modulation strategy for the 3p-DAB converter based on a comprehensive piece-wise TDA and an optimization process that obtains the optimal control parameters for minimum RMS phase current for buck and boost operation. Resulting from the TDA, eighteen operating modes were defined by D_1 , D_2 , and D_{ps} . A non-linear optimization problem was solved to obtain the optimal control parameters over a wide voltage and full power range. The results showed that only five of the eighteen operating modes contributed to the optimized control, thus simplifying its implementation. Then, a novel closed-form DCC modulation scheme was proposed, MCSO, which was derived from the theoretical findings of the proposed TDA optimization method. The proposed MCSO scheme extends the soft-switching region and greatly reduces the RMS phase currents during wide voltage and power variations thus improving the 3p-DAB's overall efficiency. The experimental results show that the proposed closed-form MCSO modulation scheme has equivalent efficiency to the OMS, making this the first research to provide a closed-form DCC modulation scheme for a 3p-DAB that achieves equivalent efficiency as a fully-optimized offline scheme, but without the drawbacks of the offline optimization process and LUT implementation.

7.2 Future Work

Future work should focus on further extending the soft-switching operation of the 3p-DAB with DCC, specifically in the small operating regions above M10 and M15 as shown in Fig. 4-1. Priority should be put on maintaining the closed-form nature of the control to
keep the implementation as simple as possible. Since the hard-switching regions of the MCSO scheme occur when operating with SPS as shown in Fig. 4-1, an alternative to SPS modulation should be investigated when operating in the hard-switching regions to overcome this.

Presently, there lacks research that focuses on the closed-loop control for a 3p-DAB operating with a closed-form DCC modulation strategy. The nature of calculating the DCC parameters at a particular operating point requires the knowledge (measurement) of input voltage, output voltage and output current. This means that three sensors are required for implementation which adds cost and complexity to the system. Future work can develop a closed-loop control strategy that leverages the proposed TDA and analytical expressions which allow for the computation of the output current. Being able to calculate the output current at a particular operating point using the measured voltages V₁ and V₂ and control parameters D₁, D₂, and D_{ps} may allow for a closed-loop control implementation using only two voltage sensors. The elimination of the output current sensor will reduce the cost and potentially the complexity of the system, making this an area of interest for future work.

When implementing the proposed closed-form MCSO modulation strategy in a 3p-DAB, the calculations of the optimal DCC parameters to meet the desired operating point are dependent on the converter's physical parameters such as leakage inductance, switching frequency, transformer turns ratio, and even measured values such as input and output voltage and current. Because of this, future work should perform a sensitivity analysis on the closed-form expressions of MCSO to determine how sensitive each of the DCC parameters are to changes in the converter's physical values. In this way, special attention can be put on ensuring that the most sensitive parameters are designed or measured to the necessary precision to allow for efficient and reliable operation of the converter.

Appendix A

Appendix A provides the analytical expressions for average output power and RMS phase current for the DCC operating modes that were not presented in the preceding chapters of this thesis.

$$P_{outM1} = \frac{dV_1^2 n^2 D_1 D_2}{L_s f_s}$$
(A-1)

$$P_{outM4} = \frac{dV_1^2 n^2 D_2}{L_s f_s} \left(D_2 - D_1 + 2D_{ps} \right)$$
(A-2)

$$P_{outM7} = \frac{dV_1^2 n^2 D_1}{6L_s f_s} (3D_1 - 6D_{ps} + 2)$$
(A-3)

$$P_{outM8} = \frac{-dV_1^2 n^2}{18L_s f_s} \left(18D_2 D_{ps} - 6D_{ps} - 18D_1 D_2 - 6D_2 + 9D_2^2 + 9D_{ps}^2 + 1 \right)$$
 (A-4)

$$P_{outM9} = \frac{-dV_1^2 n^2}{18L_s f_s} \left(18D_1^2 - 18D_1 D_2 - 36D_1 D_{ps} + 9D_2^2 + 18D_2 D_{ps} - 6D_2 + 27D_{ps}^2 - 6D_{ps} + 1 \right)$$
(A-5)

$$P_{outM11} = \frac{dV_1^2 n^2}{18L_s f_s} \left(6D_2 + 6D_{ps} - 18D_1 D_2 + 18D_2 D_{ps} + 9D_2^2 - 9D_{ps}^2 - 1 \right)$$
(A-6)

$$P_{outM12} = \frac{dV_1^2 n^2}{6L_s f_s} (D_2 - D_1 + 2D_{ps})(3D_2 - 3D_1 + 2)$$
(A-7)

$$P_{outM13} = P_{outM4} \tag{A-8}$$

$$P_{outM14} = \frac{dV_1^2 n^2}{6L_s f_s} \left(-3D_1^2 + 6D_1 D_{ps} + 2D_1 - 6D_{ps}^2 \right)$$
(A-9)

$$P_{outM17} = P_{outM12} \tag{A-10}$$

$$P_{outM18} = \frac{-dV_1^2 n^2}{6L_s f_s} (3D_1^2 - 6D_1D_2 - 6D_1D_{ps} + 2D_1 + 3D_2^2 + 6D_2D_{ps} - 2D_2 + 6D_{ps}^2 - 4D_{ps})$$
(A-11)

$$I_{LRMS_{M1}} = \frac{V_1 n}{3\sqrt{3}L_s f_s} \left(2D_1^2 - 3D_1^3 + 2d^2 D_2^2 - 3d^2 D_2^3 - 4dD_1 D_2 + 9dD_1 D_2^2 - 9dD_1^2 D_2 + 18dD_1 D_2 D_{ps}\right)^{1/2}$$
(A-12)

$$I_{LRMS_{M4}} = \frac{V_1 n}{9\sqrt{3}L_s f_s} \left(-27d^2 D_2^3 + 18d^2 D_2^2 + 81d D_1^2 D_2 - 81d D_1 D_2^2 - 162d D_1 D_2 D_{ps} - 36d D_1 D_2 + 54d D_2^3 + 162d D_2^2 D_{ps} + 162d D_2 D_{ps}^2 - 9D_1^2 + 9D_1 - 1\right)^{1/2}$$
(A-13)

$$I_{LRMS_{M7}} = \frac{-V_1n}{3\sqrt{3}L_s f_s} \left(3d^2 D_2^3 - 2d^2 D_2^2 + 3d D_1^3 - 9d D_1^2 D_{ps} + 3d D_1^2 \right)^{1/2}$$

$$I_{LRMS_{M8}} = \frac{-V_1n}{9\sqrt{3}L_s f_s} \left(27d^2 D_2^3 - 18d^2 D_2^2 + 81d D_1^2 D_2 - 81d D_1 D_2^2 \right)^{1/2}$$

$$I_{LRMS_{M8}} = \frac{-V_1n}{9\sqrt{3}L_s f_s} \left(27d^2 D_2^3 - 18d^2 D_2^2 + 81d D_1^2 D_2 - 81d D_1 D_2^2 \right)^{1/2}$$

$$I_{LRMS_{M8}} = \frac{-V_1n}{9\sqrt{3}L_s f_s} \left(27d^2 D_2^3 - 18d^2 D_2^2 + 81d D_1^2 D_2 - 81d D_1 D_2^2 \right)^{1/2}$$

$$I_{LRMS_{M9}} = \frac{-V_1n}{9\sqrt{3}L_s f_s} \left(27d^2 D_2^3 - 18d^2 D_2^2 - 54d D_1 D_2 + 27d D_{ps}^3 - 27d D_{ps}^2 \right)^{1/2}$$

$$I_{LRMS_{M9}} = \frac{-V_1n}{9\sqrt{3}L_s f_s} \left(27d^2 D_2^3 - 18d^2 D_2^2 - 54d D_1^3 + 81d D_1^2 D_2 \right)^{1/2}$$

$$I_{LRMS_{M9}} = \frac{-V_1n}{9\sqrt{3}L_s f_s} \left(27d^2 D_2^3 - 18d^2 D_2^2 - 54d D_1^3 + 81d D_1^2 D_2 \right)^{1/2}$$

$$I_{LRMS_{M9}} = \frac{-V_1n}{9\sqrt{3}L_s f_s} \left(27d^2 D_2^3 - 18d^2 D_2^2 - 54d D_1 D_2 D_{ps} + 36d D_1 D_2 \right)^{1/2}$$

$$I_{LRMS_{M11}} = \frac{V_1n}{9\sqrt{3}L_s f_s} \left(-27d^2 D_2^3 + 18d^2 D_2^2 + 81d D_1^2 D_2 - 81d D_1 D_2^2 \right)^{1/2}$$

$$I_{LRMS_{M11}} = \frac{V_1n}{9\sqrt{3}L_s f_s} \left(-27d^2 D_2^3 + 18d^2 D_2^2 + 81d D_1^2 D_2 - 81d D_1 D_2^2 \right)^{1/2}$$

$$I_{LRMS_{M11}} = \frac{V_1n}{9\sqrt{3}L_s f_s} \left(-27d^2 D_2^3 + 18d^2 D_2^2 + 81d D_1^2 D_2 - 81d D_1 D_2^2 \right)^{1/2}$$

$$I_{LRMS_{M11}} = \frac{V_1n}{9\sqrt{3}L_s f_s} \left(-27d^2 D_2^3 + 18d^2 D_2^2 + 81d D_2^2 D_{ps} - d \right)^{1/2}$$

$$I_{LRMS_{M11}} = \frac{V_1n}{9\sqrt{3}L_s f_s} \left(-27d^2 D_2^3 + 18d^2 D_2^2 + 81d D_1^2 D_2 - 81d D_1 D_2^2 \right)^{1/2}$$

$$I_{LRMS_{M11}} = \frac{V_1n}{9\sqrt{3}L_s f_s} \left(-27d^2 D_2^3 + 18d^2 D_2^2 + 81d D_2^2 D_{ps} - d \right)^{1/2}$$

$$I_{LRMS_{M11}} = \frac{V_1n}{9\sqrt{3}L_s f_s} \left(-27d^2 D_2^3 + 18d^2 D_2^2 + 81d D_2^2 D_2 - 81d D_1 D_2^2 \right)^{1/2}$$

$$I_{LRMS_{M11}} = \frac{V_1n}{9\sqrt{3}L_s f_s} \left(-27d^2 D_2^3 + 18d^2 D_2 + 27d D_2^3 + 81d D_2^2 D_{ps} \right)^{1/2}$$

$$I_{LRMS_{M11}} = \frac{V_1n}{9\sqrt{3}L_s f_s} \left(-27d^2 D_2^3 + 18d^2 D_2 + 27d D_2^3 + 81d D_2^2 D_{ps} \right)^{1/2}$$

$$I_{LRMS_{M11}} = \frac{V_1n}{9\sqrt{3}L_s f_s} \left(-27d^2 D_2^3 + 18d^2 D_2 + 27d D_2^3 + 81d D_2^2 D_{ps} \right)^{1/2}$$

$$I_{LRMS_{M11}} = \frac{V_1n}{9\sqrt{3}L_$$

$$I_{LRMS_{M12}} = \frac{V_1 n}{9\sqrt{3}L_s f_s} \left(-27d^2 D_2^3 + 18d^2 D_2^2 - 27d D_1^3 + 81d D_1^2 D_2 + 81d D_1^2 D_{ps} + 27d D_1^2 - 81d D_1 D_2^2 - 162d D_1 D_2 D_{ps} - 36d D_1 D_2 - 81d D_1 D_{ps}^2 - 54d D_1 D_{ps} - 9d D_1 + 27d D_2^3 + 81d D_2^2 D_{ps} + 27d D_2^2 + 81d D_2 D_{ps}^2 + 54d D_2 D_{ps} - 9d D_2 + 54d D_{ps}^2 + 2d - 9D_1^2 + 9D_1 - 1\right)^{1/2}$$

$$I_{LRMS_{M13}} = \frac{-V_1 n}{9\sqrt{3}L_s f_s} \left(9d^2 D_2^2 - 9d^2 D_2 + d^2 + 27d D_1^3 - 81d D_1^2 D_{ps} + 27d D_1^2 - 18d D_1 D_2 + 81d D_1 D_{ps}^2 - 54d D_1 D_{ps} + 9d D_1 + 27D_1^3 - 18D_1^2\right)^{1/2}$$

$$I_{LRMS_{M14}} = \frac{-V_1 n}{9\sqrt{3}L_s f_s} \left(9d^2 D_2^2 - 9d^2 D_2 + d^2 - 27d D_1^3 + 81d D_1^2 D_{ps} + 27d D_1^2 - 18d D_1 D_2 - 81d D_1 D_{ps}^2 - 54d D_1 D_{ps} + 9d D_1 + 54d D_{ps}^3 + 27D_1^3 - 18D_1^2\right)^{1/2}$$

$$I_{LRMS_{M17}} = \frac{V_1 n}{9\sqrt{3}L_s f_s} \left(-9d^2 D_2^2 + 9d^2 D_2 - d^2 - 27d D_1^3 + 81d D_1^2 D_{ps} + 27d D_1^2 - 81d D_1 D_{ps}^2 - 54d D_1 D_{ps} - 9d D_1 + 27d D_2^3 + 81d D_2^2 D_{ps} + 27d D_2^2 + 81d D_2 D_{ps}^2 - 54d D_1 D_{ps} - 9d D_1 + 27d D_2^3 + 81d D_2^2 D_{ps} + 27d D_2^2 + 81d D_2 D_{ps}^2 - 54d D_1 D_{ps} - 9d D_1 + 27d D_2^3 + 81d D_2^2 D_{ps} + 27d D_2^2 + 81d D_2 D_{ps}^2 - 54d D_1 D_{ps} - 9d D_1 + 27d D_2^3 + 81d D_2^2 D_{ps} - 36d D_1 D_2 - 81d D_1 D_{ps}^2 - 54d D_1 D_{ps} - 9d D_1 + 27d D_2^3 + 81d D_2^2 D_{ps} + 27d D_2^2 + 81d D_2 D_{ps}^2 - 54d D_1 D_{ps} - 9d D_1 + 27d D_2^3 + 81d D_2^2 D_{ps} - 27d D_1^2 - 81d D_1 D_2^2 - 162d D_1 D_2 D_{ps} - 9d D_2 + 54d D_{ps}^2 - 54d D_1 D_{ps} - 9d D_1 + 27d D_2^3 + 81d D_1^2 D_2 - 81d D_1 D_2^2 - 162d D_1 D_2 D_{ps} - 9d D_2 + 54d D_{ps}^2 - 27d D_2^2 + 81d D_2 D_{ps}^2 - 54d D_2 D_{ps} + 9d D_1 + 27d D_2^3 + 81d D_2^2 D_{ps} - 27d D_2^2 + 81d D_2 D_{ps}^2 - 54d D_2 D_{ps} + 9d D_1 + 27d D_2^3 + 81d D_2^2 D_{ps} - 27d D_2^2 + 81d D_2 D_{ps}^2 - 54d D_2 D_{ps} + 9d D_2 + 54d D_{ps}^2 - 54d D_2 D_{ps} - 54d D_2 D_{ps} - 9d D_2 + 54d D_{ps}^2 - 54d D_2 D_{ps} - 54d D_2 D_{$$

Appendix B

Appendix B derives the turn-on soft-switching conditions for the 3p-DAB operating with the proposed closed-form MCSO modulation scheme. The analysis only needs to be conducted for the switches of a single phase because each phase operates with the same DCC parameters, just 120° phase-shifted from each other. For consistency, phase A is chosen i.e., switches, S₁₁, S₁₄, S₂₁, and S₂₄. Table B-1 summarizes the turn-on instances of each phase A switch during a switching period and the phase current polarity requirement to achieve soft-switching. Zero-voltage switching of a MOSFET is achieved when the current is flowing through the body diode of the MOSFET at the turn-on instance. Zero-current switching of a MOSFET is achieved when the current through the MOSFET at the turn-on instance is zero. Therefore, the soft-switching conditions can be solved by checking to see if the polarity of the phase A current $i_a(t)$ at the turn-on instance of each switch meets the requirements outlined in Table B-1. The turn-on soft-switching conditions are presented in Tables B-2 to B-5 as inequality expressions of DCC parameters D_1 , D_2 , D_{ps} and voltage gain d.

PHASE A TURN-ON SOFT_SWITCHING REQUIREMENTS			
Phase A switch	Turn-on instance	Soft-switching requirement	
S_{11} – H.S. input bridge	t = 0	$i_a(t) \leq = 0$	
$S_{14} - L.S.$ input bridge	$t = D_1$	$i_a(t) >= 0$	
S_{21} – H.S. output bridge	$t = D_{ps}$	$i_a(t) >= 0$	
S_{24} – L.S. output bridge	$t = D_2 + D_{ps}$	$i_a(t) <= 0$	

TABLE B-1 PHASE A TURN-ON SOFT SWITCHING REQUIREMENTS

Switch	Expression for phase A current at switch turn-on	Soft-switching requirement from Table B-1	Simplified soft- switching requirement	Statement
S ₁₁	$i_a(t) = \frac{nV_1}{3L_s f_s} (2t - D_1 + dD_2)$	$i_a(t) \le 0$ $t = 0$	$dD_2 - D_1 \le 0$	ZCS for M2 since $D_1 = dD_2$
S_{14}	$i_a(t) = \frac{nV_1}{3L_s f_s} \left(D_1 - 2dt + dD_2 + 2dD_{ps} \right)$	$i_a(t) \ge 0$ $t = D_1$	$d(D_2 - dD_2) \ge 0$	ZVS for M2 since $d \le 1, D_2 > 0$
S ₂₁	$i_a(t) = \frac{nV_1}{3L_s f_s} \left(2t - D_1 - 2dt + dD_2 + 2dD_{ps}\right)$	$i_a(t) \ge 0$ $t = D_{ps}$	$dD_2 - D_1 \ge 0$	ZCS for M2 since $D_1 = dD_2$
S ₂₄	$i_a(t) = \frac{nV_1}{3L_s f_s} (D_1 - dD_2)$	$i_a(t) \le 0$ $t = D_2 + D_{ps}$	$dD_2 - D_1 \le 0$	ZCS for M2 since $D_1 = dD_2$

TABLE B-2 TURN-ON SOFT-SWITCHING CONDITIONS FOR M2

Therefore, in M2, S₁₁, S₂₁, S₂₄ achieve ZCS and S₁₄ achieves ZVS.

TURN-ON SOFT-SWITCHING CONDITIONS FOR M3				
Switch	Expression for phase A current at switch turn-on	Soft-switching requirement from Table B-1	Simplified soft-switching requirement	Statement
S_{11}	$i(t) = \frac{nV_1}{3L_s f_s} (2t - D_1 + dD_2)$	$i_a(t) \le 0$ $t = 0$	$dD_2 - D_1 \le 0$	ZCS for M3 since $D_1 = dD_2$
S_{14}	$i_a(t) = \frac{nV_1}{3L_s f_s} (D_1 - dD_2)$	$\begin{array}{l} i_a(t) \geq 0 \\ t \ = \ D_1 \end{array}$	$D_1 - dD_2 \ge 0$	ZCS for M3 since $D_1 = dD_2$
S ₂₁	$i_a(t) = \frac{nV_1}{3L_s f_s} \left(2t - D_1 - 2dt + dD_2 + 2dD_{ps}\right)$	$i_a(t) \ge 0$ $t = D_{ps}$	$D_{ps} \ge 0$	ZVS for M3 since $D_{ps} \ge 0$
S ₂₄	$i_a(t) = \frac{nV_1}{3L_s f_s} (2t - D_1 - dD_2)$	$i_a(t) \le 0$ $t = D_2 + D_{ps}$	$D_2 \le \frac{D_{ps}}{(d-1)}$	ZCS for M3 since $D_2 = \frac{D_{ps}}{(d-1)}$

TABLE B-3

Therefore, in M3, S_{11} , S_{14} , S_{24} achieve ZCS and S_{21} achieves ZVS.

Switch	Expression for phase A current at switch turn-on	Soft-switching requirement from Table B-1	Simplified soft- switching requirement	Statement
S_{11}	$i_a(t) = \frac{nV_1}{9L_s f_s} (6t + d - 3D_1 + 3dt - 3dD_{ps})$	$i_a(t) \le 0$ $t = 0$	$(1+d)D_{ps} \ge 0$	ZVS for M15 since $d, D_{ps} > 0$
S ₁₄	$i_a(t) = \frac{nV_1}{3L_s f_s} (D_1 - 2dt + dD_2 + 2dD_{ps})$	$i_a(t) \ge 0$ $t = D_1$	$D_{ps} + \frac{d}{3} + d^2 D_{ps}$ $\geq \frac{d^2}{3} + dD_{ps}$	ZVS for M15 since $d \le 1, D_{ps} > 0$
S ₂₁	$i_a(t) = \frac{nV_1}{9L_s f_s} (6t + d - 3D_1) - 3dt + 3dD_{ps})$	$i_a(t) \ge 0$ $t = D_{ps}$	$D_{ps} \ge 0$	ZVS for M15 since $D_{ps} > 0$
S ₂₄	$i_{a}(t) = \frac{nV_{1}}{9L_{s}f_{s}} (1 - 3t - d + 3D_{1} + 3dt - 3dD_{2} - 3dD_{ps})$	$i_a(t) \le 0$ $t = D_2 + D_{ps}$	$dD_{ps} \ge 0$	ZVS for M15 since $d, D_{ps} > 0$

TABLE B-4TURN-ON SOFT-SWITCHING CONDITIONS FOR M15

Therefore, in M15, S_{11} , S_{14} , S_{21} , S_{24} achieve ZVS.

Switch	Expression for phase A current at switch turn-on	Soft-switching requirement from Table 1	Simplified soft- switching requirement	Statement
S ₁₁	$i_a(t) = \frac{nV_1}{9L_s f_s} (3t - 1 + d) + 3dt - 3dD_{ps}$	$i_a(t) \le 0$ $t = 0$	$D_{ps} \ge \frac{(d-1)}{3d}$	*ZVS for M10 since $D_{ps} > \frac{(d-1)}{3d}$
S ₁₄	$i_{a}(t) = \frac{nV_{1}}{9L_{s}f_{s}} (1 - 3t + 3D_{1} - 6dt + 3dD_{2} + 6dD_{ps})$	$i_a(t) \ge 0$ $t = D_1$	$D_{ps} \ge \frac{(d-1)}{3d}$	*ZVS for M10 since $D_{ps} > \frac{(d-1)}{3d}$
S ₂₁	$i_a(t) = \frac{nV_1}{3L_s f_s} (2t - D_1) - 2dt + dD_2 + 2dD_{ps})$	$i_a(t) \ge 0$ $t = D_{ps}$	$D_{ps} \ge \frac{(d-1)^2}{3(d^2 - d + 1)}$	*ZVS for M10 since $D_{ps} > \frac{(d-1)}{3d}$

TABLE B-5TURN-ON SOFT-SWITCHING CONDITIONS FOR M10

S ₂₄	$i_a(t) = \frac{nV_1}{3L_s f_s} (1 - 3t + 3D_1 - 3dD_2)$	$i_a(t) \le 0$ $t = D_2 + D_{ps}$	$D_{ps} \ge \frac{(d-1)}{3d}$	*ZVS for M10 since $D_{ps} > \frac{(d-1)}{3d}$
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*The inequality expression for D_{ps} can be deduced by realizing that D_{ps} is a monotonically increasing function. In MCSO, M3 transitions into M10 as the output power increases. Since at the upper power boundary of M3, $D_{ps} = (d-1)/3d$ then know that in M10, D_{ps} will always be greater than (d-1)/3d.

Therefore, in M10, S₁₁, S₁₄, S₂₁, S₂₄ achieve ZVS.

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