SIC POWER MODULES WITH SILVER SINTERED MOLYBDENUM PACKAGING: MODELING, OPTIMAL DESIGN, MANUFACTURING, AND CHARACTERIZATION

SIC POWER MODULES WITH SILVER SINTERED MOLYBDENUM PACKAGING: MODELING, OPTIMAL DESIGN, MANUFACTURING, AND CHARACTERIZATION

BY

YUHANG YANG, B.Eng

A THESIS

SUBMITTED TO THE DEPARTMENT OF MECHANICAL ENGINEERING

AND THE SCHOOL OF GRADUATE STUDIES

OF MCMASTER UNIVERSITY

IN PARTIAL FULFILMENT OF THE REQUIREMENTS

FOR THE DEGREE OF

DOCTOR OF PHILOSOPHY

Doctor of Philosophy (2023) McMaster University

(Mechanical Engineering) Hamilton, Ontario, Canada

TITLE:	SIC POWER MODULES WITH SILVER SINTERED MOLYBDENUM PACKAGING: MODELING, OPTIMAL DESIGN, MANUFACTURING, AND CHARACTERIZATION
AUTHOR:	Yuhang Yang B.Eng. (Vehicle Engineering), Xi'an Jiaotong University, Xi'an, China
SUPERVISOR:	Prof. Ali Emadi
NUMBER OF PAGES:	xxii, 166

Abstract

This Ph.D. thesis carries out extensive and in-depth research on the packaging technology of silicon carbide (SiC) power modules, including new packaging structures, multi-physics modeling and optimal design methods for half-bridge power modules, manufacturing processes, and experimental validations.

A new packaging scheme, the Silver-Sintered Molybdenum (SSM) packaging, is proposed in this thesis. It contains a molybdenum (Mo) -based insulated-metal-substrate (IMS) structure, nano-silver sintering die-attachments, and planar interconnections. This technology has the potential to increase the operating temperature of SiC power modules to above 200^oC, and can greatly improve their lifetime. These advantages are verified by active power cycling and passive temperature cycling simulations.

Analytical modeling methods for half-bridge power modules with the SSM packaging are also studied. A decoupled Fourier-based thermal model is introduced. This model considers the decoupling effect between different heat source regions and can give a three-dimensional analytical solution for the temperature field of a simplified half-bridge power module structure. In addition, based on the partial inductance model for rectangular busbars, an analytical stray inductance model for half-bridge power modules is also proposed. The accuracy of these two models is estimated by

both numerical simulations and experiments.

With the proposed analytical models, an optimal design method for half-bridge power modules with the SSM packaging is proposed in this study, which uses the particle swarm optimization algorithm. This method is successfully applied in the design of a prototype power module and is able to minimize the stray inductance and volume while maintaining desired junction temperatures.

This thesis also introduces the manufacturing process of the prototype power module. Several new processes are proposed and validated, including a pressure-less nano-silver sintering process to bond SiC dies on Mo substrates, the formation of the Mo-based IMS structure, and the re-metallization of SiC dies.

Acknowledgements

I would like to express my sincere thanks to my supervisor, Dr. Ali Emadi, for providing me with such an invaluable opportunity to work at one of the best platforms in this field, McMaster Automotive Resource Centre (MARC), during the past four years and a half. With his support and encouragement, I had an enormous space to develop my abilities and carry out meaningful work that I found interesting. He also taught to be professional, considerate, and strategic.

I would like to thank my supervisory committee members, Dr. James Cotton and Dr. Saeid Habibi, for their helpful guidance and support of my thesis over the years. I would also like to thank Dr. Romina Rodriguez for her assistance during the early stage of my thesis, Dr. Mehdi Narimani and Omar Zayed for supporting thermal characterization experiments, Doris Stevanovic from Centre for Emerging Device Technologies (CEDT) at McMaster University for all the training and help with cleanroom work, Christopher Butcher and Jhoynner Martinez from Canadian Centre for Electron Microscopy (CCEM) for their assistance with scanning electron microscope examinations, and Dr. Yu-Chih Tseng from Natural Resources Canada-CanmetMATERIALS for his help with material manufacturing, Maryam Alizadeh and Linke Zhou for their contributions to the thermal modeling section. Besides, thank CREE Wolfspeed for technical supports and thank Mitsubishi Gas Chemical

for providing BT prepreg samples.

I want to thank all my colleagues from the industrial projects I participated in. Special thanks to Dr. Shamsuddeen Nalakath, Dr. Alan Callegaro, Dr. John Reimers, and Dr. Giorgio Pietrini for their leadership and mentorship. Also, I want to express my special appreciation to all members of the Eaton Aerospace Motor Drive team from both the McMaster and the Eaton sides for their support. I truly benefit a lot from working with these outstanding engineers.

My appreciation goes to all my dear friends for helping me and sharing so many wonderful moments with me. You are my family in Canada.

I would like to express my gratitude to my father, Guohua Yang, and mother, Guihua Xu. Their selfless love and cultivation is the reason why I am able to get to where I am today. The same thanks go to other family members who helped me, especially my aunt, Xiangqun Xu, and uncle, Zuopeng Zheng. Finally, I would like to thank my beloved wife, Yuqin Cao, for her support, understanding, and love.

This research was undertaken, in part, thanks to funding from the Canada Research Chair in Transportation Electrification and Smart Mobility and Natural Sciences and Engineering Research Council of Canada (NSERC).

Contents

List of Figures

List of Tables

Nomenclature

Abbreviations

1-D	One dimensional
3-D	Three dimensional
AMB	Active-metal-brazed
BT	Bismaleimide Triazine
CAD	Computer-aided design
CTE	Coefficient of thermal expansion
DBA	Direct-bond-aluminum
DBC	Direct-bond-copper
EDS	Energy-dispersive X-ray spectroscopy
EV	Electric vehicle
ESR	Equivalent series resistance

FEA	Finite element analysis
IGBT	Insulated Gate Bipolar Transistors
IMS	Insulated-metal-substrate
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NSGA-II	Non-Dominated-Sorting-Genetic-Algorithm II
PCB	Print-circuit-board
PSO	Partial swarm optimization
SAC305	Sn96.5Ag3Cu0.5 Solder
SEM	Scanning electron microscope
SSM	Silver-sintered molybdenum
TIM	Thermal interface material
TLPB	Transient liquid-phase bonding
TSP	Temperature-sensitive parameter
WBG	Wide band-gap

Main Symbols

C_P	Specific heat capacity under constant pressure
E	Elastic Modulus

f_o	Oscillation frequency
k	Thermal conductivity
L_s	Stray inductance
N_f	Cycle life
R_a	Averaged surface roughness
R_{th}	Thermal resistance
T	Temperature
T_j	Junction temperature
T_s	Sintering temperature
V_e	Volume of the power module
V_D	Body diode forward voltage
V_{DS-LS}	Low side drain-source voltage
γ	Relative electrical conductivity according to International Annealed Copper Standard
$\Delta\varepsilon_p$	Plastic strain difference during each cycle
ΔT_j	Junction temperature different between two dies in a half-bridge power module
ε	Strain

ε_p	Plastic strain
θ	Temperature rise from the coolant to a specific location in the power module
θ_j	Temperature-rise from the coolant to the junction
ν	Poisson‘s ratio
ρ	Mass density
σ	Stress

Chapter 1

Introduction

1.1 Background

Power semiconductor devices are the core components of power electronic systems. They usually contain one or more semiconductor dies, such as Insulated Gate Bipolar Transistors (IGBT) and Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Typically, devices with only one die are called discrete devices, while others with more dies are named power modules. Proper packaging design is necessary to construct a device from bare semiconductor dies. Currently, both discrete devices and power modules are widely adopted. Their basic packaging requirements are mostly similar, while the multi-die modules require extra attention to die spacing and circuit design. As a complex multi-physics system, the packaging of power modules should provide not only desirable electrical properties but also excellent thermal and mechanical properties.

Over the years, wide band-gap (WBG) devices have been regarded as the future of power electronics. The silicon carbide (SiC) MOSFETs, specifically, are suitable for

the next generation of traction applications due to their superior dielectric breakdown field intensity, switching speed, and temperature range. The application of SiC MOSFETs brings challenges to the packaging design. Compared with conventional silicon (Si) based IGBTs and diodes, SiC MOSFETs of the same rating can be 3x smaller in size, which increases concerns of temperature and stress concentration. Meanwhile, SiC MOSFETs can handle high temperatures over 200^{o}C (Liang *et al.*, 2013), while conventional packaging can barely match this range due to thermal stress concerns. Novel packaging technologies are needed to achieve a higher temperature range of SiC devices and improve thermal-mechanical reliability. In addition, SiC devices are more sensitive to stray inductance due to their faster switching speed. Thus, bond-wires should be replaced by low-inductance interconnections, such as planar leads.

A typical application of SiC power modules is the traction inverter in electric vehicles. This is because the voltage and current range of the SiC module is very suitable, and at the same time, its fast switching speed and high temperature-durability features also meet the needs of electric vehicles. SiC MOSFET modules are already used in mass-produced passenger cars. Starting in 2018, Tesla has been using SiC devices in inverters of their electric vehicle (EV) models, including Model 3, Model Y, and Model S Plaid. Chinese car maker, NIO, also introduced SiC inverters in their latest ET5 and ET7 models. In April 2022, Wolfspeed announced that their XM3 series SiC modules would be used in the high-performance EV, Lucid Air. The application of SiC MOSFET modules in the traction inverter of Tesla Model 3 is illustrated in Figure 1.1.

Mainly due to the advancement of electrified transportation, the power semiconductor industry is rapidly expanding. Yole Development forecasts that power modules

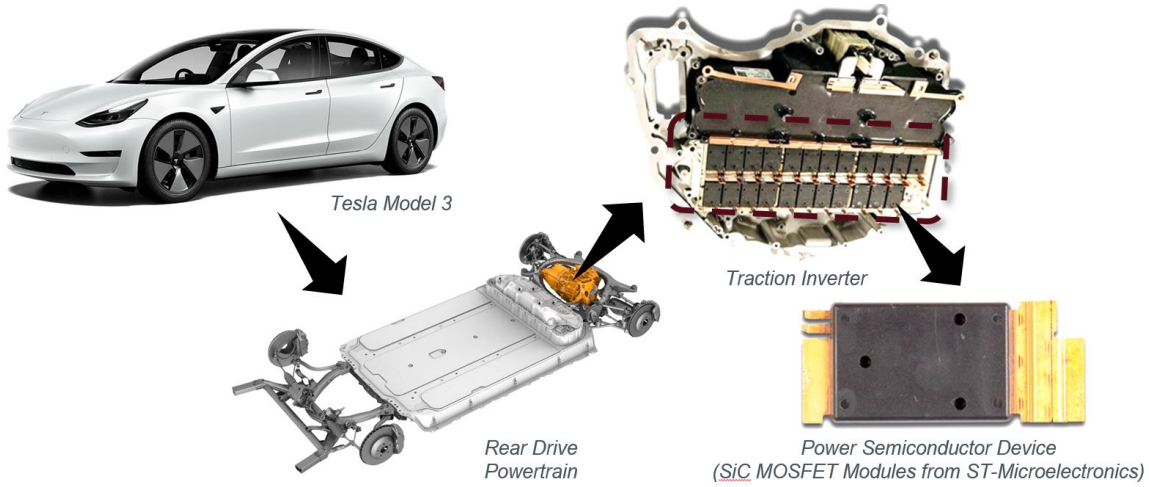


Figure 1.1: SiC MOSFET modules in the traction inverter of Tesla Model 3.

will have a total market of 7.6 billion US$ by 2025, with a 5-year compound annual growth rate of 9.1%. The largest part of the growth will be contributed by the electric vehicle industry (Yole.Developpement, 2020). The growing market and the need to save energy pose elevated challenges to the reliability, efficiency, power density, and cost of power modules. The U.S. Department of Energy has set targets for high-voltage power electronics, requiring reducing the cost to 2.7 US$/kW, doubling the lifetime, and increasing the power density to 100 kW/L by 2025 (U.S.Dept.Energy, 2017). The improvement in power modules is important to achieving these goals. Power modules are critical components in terms of cost and reliability, and their efficiency determines the size of the cooling system, which heavily affects the power density of a power electronics converter. However, the performance of power modules does not just rely on the semiconductor dies but is also affected by the packaging technology.

1.2 Motivations and Contributions

The conventional packaging technology is based on the metallized ceramic substrate and bond-wires. This technology has been applied in most of the existing modules and is still the most prevalent option in the market. However, the traditional packaging is facing challenges with growing performance requirements (Lee *et al.*, 2020). The large variations in the coefficient of thermal expansion (CTE) between the semiconductor, copper, and ceramic material cause significant thermal stress at high temperature. This will limit the advantages of high temperature-durability of SiC devices. Similarly, bond-wires introduce larger stray inductance. It can cause excessive voltage overshot for SiC devices that have fast switching speed (Yang *et al.*, 2020). Therefore, advanced packaging technologies need to be developed to take advantage of SiC's benefits. The mission of this thesis is to develop packaging structures, design methodologies, and manufacturing processes to help SiC power modules achieve high temperature-durability, enhanced reliability, low inductance, and simplified manufacturing. Specifically, this thesis has the following targets:

(1) Propose a novel packaging scheme to improve the temperature durability and reliability of SiC power modules.

(2) Propose multi-physics modeling and design methods for the proposed packaging scheme.

(3) Design a SiC prototype module based on the proposed packaging scheme and the design methods.

(4) Study the manufacturing process of the proposed packaging scheme.

(5) Manufacture and characterize the designed SiC prototype power module.

The process and methods to achieve these targets will be explained in detail in the

following chapters. This thesis brings solid contributions to the field of power module packaging and provides new directions for future research. The main contributions of this thesis include four parts:

(1) A new packaging scheme, the Silver-Sintered Molybdenum (SSM) packaging, for SiC power modules is proposed in this thesis. This new technology can remarkably improve power modules' reliability and temperature durability.

(2) This thesis proposes a thermal-electrical modeling and design method for power modules with the SSM packaging and other similar packaging schemes, including an analytical 3-D thermal model based on decoupled structures and the Fourier-series method, an analytical stray inductance model based on the partial-inductance method and the current density distribution, and a design optimization method based on the Particle Swarm Optimization algorithm.

(3) This thesis introduces a working process of bonding SiC dies on Molybdenum substrates with the pressure-less nano-silver sintering technology. The impact of the sintering temperature and the surface condition on the sintering quality are studied.

(4) A half-bridge prototype SiC power module with the SSM packaging scheme is designed, manufactured, and experimentally characterized, which validates the methodologies proposed in this thesis.

1.3 Thesis Overview

This thesis will conduct a broad and in-depth study to achieve the goals introduced above. The rest of this thesis is organized in the following order.

Chapter 2 introduces the common packaging methods of power modules in detail, and analyzes the existing technologies and future trends. Meanwhile, this chapter also

introduces the theoretical knowledge related to power modules' thermal-mechanical-related failures.

Chapter 3 proposes a new type of packaging scheme aiming at improving the reliability and temperature durability of power modules, and analyzes the selection of materials. The proposed packaging scheme is named Silver-Sintered Molybdenum (SSM) Packaging.

In Chapter 4, analytical modeling methods for SiC half-bridge power modules with the SSM packaging scheme are proposed, including a decoupled Fourier-based steady-state thermal model and an analytical stray inductance model. Their accuracy is validated by numerical simulations.

In Chapter 5, an optimal design method for SiC half-bridge power modules with the SSM packaging scheme is proposed. A half-bridge SiC MOSFET prototype power module is designed using this method, whose performances are estimated using numerical simulations.

Chapter 6 introduces the fabrication process of the prototype power module. Specifically, the key manufacturing step, the pressure-less nano-silver sintering, is studied in detail.

Chapter 7 presents experimental validations of the prototype power module. The double pulse test measures the module's switching behavior and calibrates the stray inductance. And the structural function analysis measures the power module's thermal resistance.

Chapter 8 discusses the reliability benefits of the SSM packaging scheme through passive temperature cycling and active power cycling simulations.

Chapter 9 concludes all work done in this thesis and discusses the future work.

Chapter 2

Power Module Packaging: Current Status and Future Trends

This chapter will provide an overview of power modules' packaging structure, materials, and failure modes. Motivations for proposing innovative solutions for improving the thermal-mechanical performance of the module will be further discussed.

2.1 Conventional Power Module Packaging Schemes

The layer stack-up of conventional power modules is shown in Figure 2.1, where semiconductor dies are mounted onto the metallized ceramic substrate with the chosen die-attachment technology and the electrical connections are formed through the use of bond-wires. The following will discuss the details in this design.

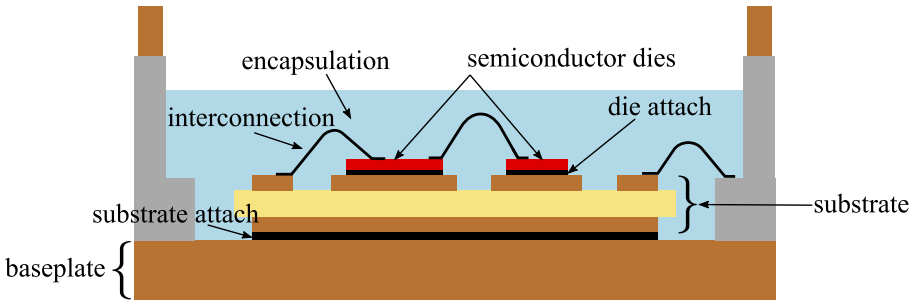


Figure 2.1: Layer stack-up of the conventional packaging scheme.

2.1.1 Semiconductors dies

Semiconductor dies are core components in power modules. Currently, Si IGBT dies are widely implemented in power modules for electrified transportation applications (Reimers *et al.*, 2019). Off-the-shelf products also include SiC MOSFET dies based power modules and discrete devices, with the latter being implemented in several mass-production vehicles as aforementioned. Gallium Nitride (GaN) dies are commercially available but are currently not prevalent for automotive traction applications (Amano *et al.*, 2018).

A shift from Si devices to WBG devices is expected to meet the exceeding demands for higher power density and efficiency in the automotive industry. The electrical and thermal properties for Si, SiC, and GaN materials are compared in Figure 2.2, where a high value is preferable for all the properties shown. As can be observed from Figure 2.2, the bandgap energy, breakdown voltage, saturation velocity, thermal conductivity, and maximum operating temperature of WBG materials far exceed Si (Masataka *et al.*, 2016; Morancho, 2008; Sun *et al.*, 2019). With a higher maximum operating temperature and thermal conductivity, WBG devices could potentially ease thermal management requirements. Generally, SiC power modules are foreseen to be implemented for high voltage applications over 1.2 kV, while GaN is typically used for

voltages below 650 V. The technical advantages of WBG devices have already been proven in many works, and the prices are forecasted to be decreased tremendously in the near future, mainly due to their application in the automotive industry.

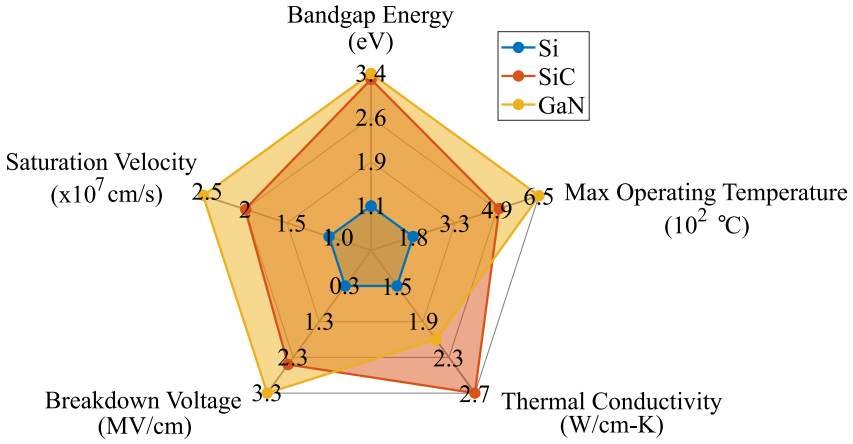


Figure 2.2: Electrical and thermal properties of Si, SiC, and GaN (Masataka *et al.*, 2016; Morancho, 2008; Sun *et al.*, 2019).

2.1.2 Die-attachment and interconnections

In power modules, semiconductor dies need to be attached to a substrate and connected with electrical interconnections to form the circuit. The major attachment technologies include solders (Xia *et al.*, 2002), silver-sintering (Wolfgang and Krebs, 2019), and transient liquid-phase bonding (TLPB) (Cook and Sorensen, 2011; Pahinkar *et al.*, 2018). Properties to consider during material selection include the melting temperature, thermal conductivity, as well as CTE since this will affect performance degradation during thermal cycling. In-depth reviews of each die attachment technology can be found in the literature. (Manikam and Cheong, 2011; Liu *et al.*, 2018; Yoon *et al.*, 2013; Gale and Butts, 2004; Siow and Lin, 2016).

Currently, Aluminum (Al) bond-wires are the predominant interconnection technology in power modules for electrified transportation. Bond-wires usually undergo fast and large-scale temperature cycling due to relatively high current density and low thermal capacity (Wang *et al.*, 2013). Consequently, cracking and fractures might occur due to high stress, and bond-wire lift-off might result due to accumulated elastic strain (Niu, 2017). In fact, failures of the wire bonding are the dominant failure modes in conventional power modules. Therefore, more advanced interconnection technologies have been investigated to mitigate the thermal-mechanical challenge, such as Al wire ribbons, Al-Copper (Al-Cu) wires, Al-Cu ribbons, and Cu wires/ribbons (Zhang *et al.*, 2007; Luechinger *et al.*, 2017; Ling *et al.*, 2012; Jacques *et al.*, 2015). The aforementioned technologies still use wires, and ultimately, planar interconnect technology, and pressure-based bondless connection will allow for higher reliability and lower parasitic inductance.

2.1.3 Substrate

Substrates include at least a conductive layer where the dies are placed and an electrically isolating layer. In conventional packaging, substrates are made with metallized ceramic boards. Direct-bond-copper (DBC) is the most commonly used metallized ceramic substrate in off-the-shelf power modules. It contains a ceramic layer with copper bonded on both sides. To achieve higher temperature cycling capability, the metallic material can be replaced by aluminum, which forms the direct-bond-aluminum (DBA) substrate. Active-metal-brazed substrate (AMB) is another metallized ceramic technology which normally works with Silicon Nitride (Si_3N_4) ceramic. Other commonly

used ceramic materials for the isolating layer include Aluminum Nitride (AlN), Aluminum oxide (Al_2O_3), and Beryllium oxide (BeO). A comparison of their properties is summarized in Bajwa's work (Bajwa, 2015). Other substrate technologies, such as insulated-metal-substrate (IMS) are studied in the literature. Their advantages and disadvantages are discussed in (Gurpinar *et al.*, 2020; Miyazaki *et al.*, 2018).

2.1.4 Baseplate and heatsink

The substrate is typically soldered onto a baseplate to ensure heat spreading and mechanical support. Usually, to attach a cooling solution to the baseplate, a thermal interface material (TIM) such as thermal paste needs to be applied to eliminate air gaps and reduce contact resistance. Baseplates are commonly made out of AlSiC or Cu. However, to mitigate their high CTE, metal matrix composites are created to achieve both a low CTE and high thermal conductivity (Luedtke, 2004). Typical examples are W-Cu, Mo-Cu, and Cu-Mo-Cu. The properties of these composites vary with the composition ratio.

A typical power module mounted onto a heat sink is shown in Figure 2.3. However, more advanced solutions include combining the heat sink and the baseplate are accepting by the industry. Circular pin-fins have been the predominant form implemented for direct cooling of the baseplate. Separate heat sink solutions for the power module still exist in the automotive industry predominantly include the horizontal-channel style type of cooling. Different types of fin configurations, from flat-plate fins to oval-shaped fins, have also been implemented. Micro-channels have been investigated but suffer from higher pressure drops.

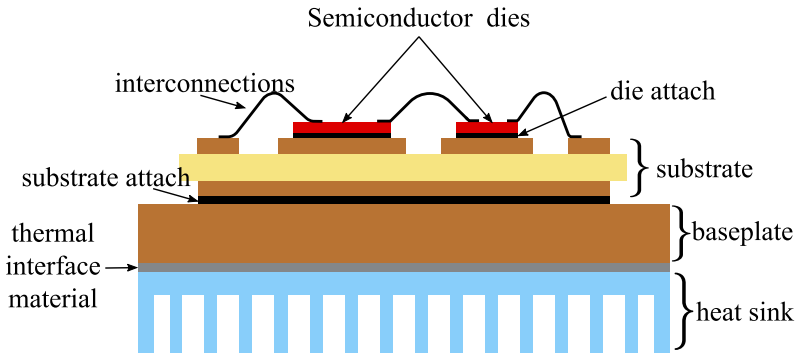


Figure 2.3: Power module mounted onto heat sink solution with TIM.

2.2 Thermal-Mechanical Related Failures and Reliability Assessment Methods

Thermal deformation and thermal stress are crucial for the power module's reliability. In order to understand this multi-physics problem, an one-dimensional linear analysis of the thermal-mechanical behavior between two structures (A and B) with different materials is discussed below. When a material is subjected to thermal deformation, the ε_a (actual strain) is the difference between the ε_{uc} (unconstrained thermal strain) and the ε_c (constrained strain), as shown in Equation (2.2.1) and (2.2.2). The ε_c will cause stress which can be expressed by Equation (2.2.3) for elastic materials. Derived from the above theories, the stress caused by structure A to another contacted structure B can be expressed as Equation (2.2.4) (Hu *et al.*, 2017).

$$\varepsilon_a = \varepsilon_{uc} - \varepsilon_c = \frac{L_T - L_{ref}}{L_{ref}} \tag{2.2.1}$$

$$\varepsilon_{uc} = CTE \times (T - T_{ref}) \tag{2.2.2}$$

$$\sigma = E \cdot \varepsilon_c \tag{2.2.3}$$

$$\sigma_B = \frac{E_B \cdot E_A \cdot \Delta CTE \cdot \Delta T}{E_B + E_A} \tag{2.2.4}$$

where E means the elastic modulus of the materials. T_{ref} is the deformation-free reference temperature which is typically the room temperature. L_{ref} is the length of the material at the reference temperature.

According to the analysis above, power modules' thermal-mechanical issues are mainly resulted from two reasons: the uneven temperature distribution and the mismatched CTE between materials, which are all heavily related to the packaging design. The uneven temperature distribution is natural to power modules since the heat is generated locally at semiconductor dies and spread through the packaging structure to the ambient, as shown in Figure 2.4. It could be improved by paralleling multiple dies to distribute heat sources. However, greater potentials lie in the structural design and the material selection to ease the concern of the CTE difference.

Typical thermal-related failure modes have been summarized in one of the author's articles (Jones-Jackson *et al.*, 2022). They can be categorized into three types, including cracking, metallurgic damage, and lift-off/delamination, as listed in Table 2.1. Cracking is mostly caused by thermal shock or residual warpage from the manufacturing of the power module. It could be prevented by improving the manufacturing and operation processes. Other failure modes mainly result from plastic behaviors of bonding interfaces under cyclic thermal loads. They can only be mitigated by improving the packaging design.

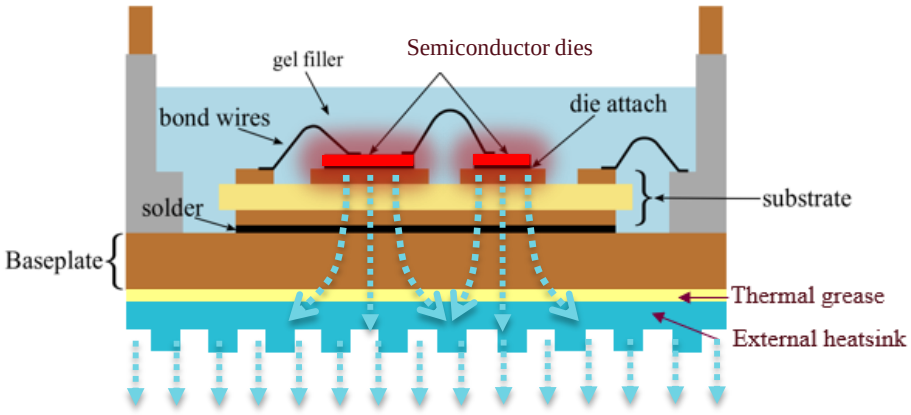


Figure 2.4: Heat generation and spreading in a power module.

Table 2.1: Primary thermal-related failure modes in power modules (Niu, 2017; Ciappa, 2002; Smet *et al.*, 2011; Qian *et al.*, 2018).

Failure Mode	Locations	Reasons
Brittle failures	Bond-wires heel region/Semiconductor die vertices/Ceramic layers	Thermal stress concentration/Thermal shock/Residual warpage
Metallurgic damage	Die metal pads/Bond-wire body	Plastic deformation and stress relaxing during thermal cycling
Lift-off/Delamination	Bond-wire joints/Attachment layers	Accumulated plastic strain and energy during thermal cycling/Pre-existing voids in attachment layers

Active power cycling and passive thermal cycling are standard ways to characterize the reliability of power modules. They can be achieved through both experiments and numerical simulations. According to the JEDEC standard (JEDEC, 2020), active power cycling emulates conditions when power modules withstand cyclic electrical

powers. Therefore, heat is generated at dies and the uneven temperature field changes repetitively. Typically, one cycle in active power cycling is a few seconds. As for passive thermal cycling, it represents environmental temperature variations. Thus, it is assumed that there is no temperature gradient within the module during passive thermal cycling. Also, each cycle is normally from 10 minutes to one hour.

There exist numerous empirical models for estimating power modules' lifetime during active power cycling based on cycling parameters, such as the peak temperature, duration of each cycle, temperature change during each cycle, etc. Here, the most renowned ones are summarized in the following equations.

$$N_f = Pa_1 \Delta T_{j-cycle}^{P_2} e^{(\frac{E_{act}}{k_B \times T_{j-mean-cycle}})} \tag{2.2.5}$$

$$N_f = Pa_1 \Delta T_{j-cycle}^{Pa_2} t_{on}^{Pa_3} I_{bon}^{Pa_4} V_{ra}^{Pa_5} Ar^{Pa_6} e^{(\frac{Pa_7}{T_{j-mean-cycle}+273})} \tag{2.2.6}$$

$$N_f = Pa_1 \Delta T_{j-cycle}^{Pa_2} Ar^{(Pa_3 \Delta T_{j-cycle}+Pa_4)} (\frac{Pa_5 + t_{on}^{Pa_6}}{Pa_7 + 1}) e^{(\frac{E_{act}}{k_B \times T_{j-mean-cycle}})} f_{diode} \tag{2.2.7}$$

In these equations, N_f is the estimated cycle life. $\Delta T_{j-cycle}$, $T_{j-mean-cycle}$, and t_{on} represent the temperature variation, the average temperature, and the heating time during one cycle. I_{bon} is the current per bond-wire. V_{ra} refers to the voltage range. Ar denotes the characteristic dimension of bond-wires. f_{diode} is the compensation factor of the diode effect. Pa_i are parameters to be calibrated using test data. The LSEIT model shown in Equation (2.2.5) is one of the earliest widely applied models, which was built for Al_2O_3 based conventional modules in the 1990s (Held *et al.*,

1999). In 2008, a more detailed model, the CIPS model (Bayerer *et al.*, 2008) was published, as shown in Equation (2.2.6). This model includes more cycling parameters and was also validated for Al_2O_3 based conventional modules. Around the same time, SEMIKRON introduced the lifetime model for power modules with their SKiM packaging (Scheuermann and Schmidt, 2013), as shown in Equation (2.2.7). This model is viewed as a bond-wire lifetime model since the SKiM packaging is solder-free.

Besides, there also exist physical-based models, which analyze the fatigue of power modules' critical structures based on physical assumptions. Well-known models include the Morrow model, the Coffin-Manson model, and Darveaux's model. The Morrow model (Riedel *et al.*, 2012) is defined in Equation (2.2.8), which was originally developed for solders in surface-mount-devices. It considers the cycle life of solders to be exponentially related to the accumulated deformation energy ($\Delta\omega$) per cycle. Similarly, the Coffin-Manson fatigue law uses the plastic strain range (ε_p) during each cycle to calculate N_f. This model has been validated for many metals, including Sn-Ag based solders, sintered nano-silvers, and Al bond-wires (Knoerr *et al.*, 2010). In addition, the Darveaux's energy-based model (Darveaux, 2002) focuses on describing the initiation and propagation of cracks in solders. In this model, both the number of cycles when the crack initiates (N_{f-0}) and the crack propagation rate ($\frac{dl_c}{dN_f}$) are modeled using the plastic energy density integrated during one cycle (ΔW). Here, l_c is the crack length. Compared with empirical models, these physical-based models can be used to estimate a new structure's reliability before building and testing it. Physical variables, such as $\Delta\omega$, ε_p, and ΔW can be obtained by either analytical calculation or numerical simulation. And other parameters are specific to materials,

which can be calibrated beforehand.

$$N_f = W_{cirt} \cdot \Delta\omega^{-n_1} \tag{2.2.8}$$

$$N_f = C_1 \Delta\varepsilon_p^{-C_2} \tag{2.2.9}$$

$$N_{f-0} = K_1 \cdot (\Delta W)^{K_2}; \frac{dl_c}{dN_f} = K_3 \cdot (\Delta W)^{K_4} \tag{2.2.10}$$

2.3 Current Status

Power modules have been implemented in the industry for decades. In this section, packaging technologies of several widely used products will be introduced. Compared with the very conventional packaging, they all have innovative designs in one way or another to improve the performance of the module.

CREE Wolfspeed has been leading the SiC device industry in recent years. Their power semiconductor devices, including discrete devices and modules, are popular. They also have their own packaging codes, such as XM3 and HM3. The XM3 packaging has been applied in their automotive-qualified high-performance modules. According to public information (McPherson and Lostetter, 2019), Wolfspeed's XM3 packaging mainly follows the conventional packaging scheme shown in Figure 2.1. However, there are two main improvements. First, the substrate is made of Si_3N_4-based AMB. Si_3N_4, as a ceramic material, has higher thermal conductivity and mechanical strength than Al_2O_3, which is the most common choice. In fact, Wolfspeed

announced that this substrate features high reliability and ensures mechanical robustness, which is also supported by Goetz's report (Manfred Goetz, 2018) that the Si_3N_4 substrate could survive 45 times more thermal cycles than the Al_2O_3 substrate. However, Si_3N_4 is not compatible in the DBC process. Only after the AMB process is mature is it feasible to use Si_3N_4 in power modules' substrate. Secondly, in the XM3 packaging, terminals are placed in a different and higher platform than the substrate, which largely shortens the length of bond-wires. This is meaningful for reducing the stray inductance. A photo of an opened XM3 module is shown in Figure 2.5.

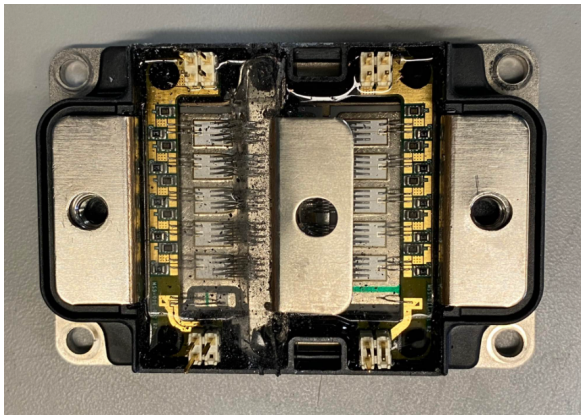
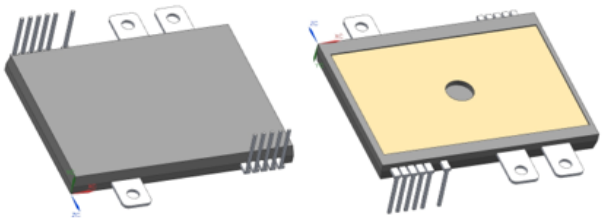


Figure 2.5: Opened XM3 power module from CREE Wolfspeed (photo taken by the author).

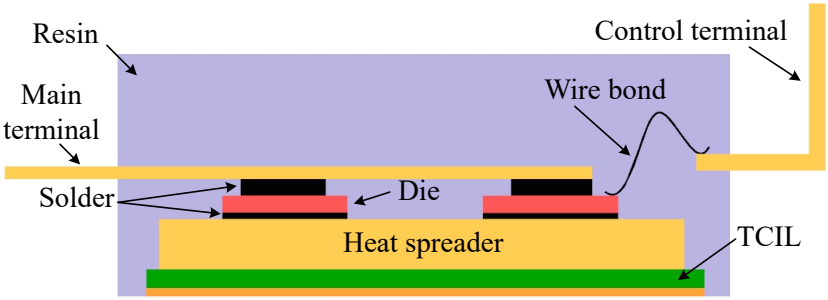
Mitsubishi Electric is another key supplier in the power module industry. They have developed high-power modules with various packages depending on different ratings. For applications up to 50 kW, Mitsubishi manufactured its J-series transfer-molded power module. It consists of two IGBT/diodes forming the half-bridge module (Han and Song, 2015). Instead of using traditional wire bonding, by applying direct-lead-bond technology, the power and thermal cycling capability are increased, while the internal inductance and lead resistance can be reduced. Al bond-wires are only

used for signals. A thermally-conductive-electrically-isolated layer is also added below the heat spreader to increase heat conduction. Directly soldering dies on the heat spreader enables better transient thermal performance. Besides, this module features embedded temperature and current sensors that facilitate fault detection and protection. This module has already been implemented in the Honda Insight (Yannou and Avron, 2012). For high-power traction inverters up to 190 kW, Mitsubishi developed a new family of 6-in-1 modules, called J1-series, that is composed of six IGBT/diode switches forming a voltage source inverter circuit (Spenke and Khalid, 2019). The IGBT dies have the 7_{th} generation carrier stored trench technology, which enables reducing power losses by more than 10% compared to previous generations. Similar to the J-series, the J1-series modules also feature the direct-lead-bond technology and embedded temperature and current sensors. The package layout has been improved by using direct liquid cooling where optimized pin-fins are integrated into the module and heatsink grease is no longer required. From experimental results, the thermal resistance is further reduced by 30% (Ishihara and Hiyama, 2015). The J1-series module is shown in Figure 2.7. With a 40% reduction of volume compared with J series, this module has a footprint of 120 mm×115.2 mm×31 mm.

Nissan designed its own customized semiconductors (Sato *et al.*, 2011) in its pure EV LEAF. This module investigated several packaging technologies to enhance heat dissipation and mitigate thermal stress, which could potentially improve reliability. Unlike a traditional structure, the die is directly soldered to a buffer plate made of Cu-Mo alloy, and the latter is soldered to the Cu busbar. This reduces the stress caused by a CTE mismatch between the die and the Cu busbar. The metallized ceramic substrate and the conventional baseplate are removed. Instead, a sheet made

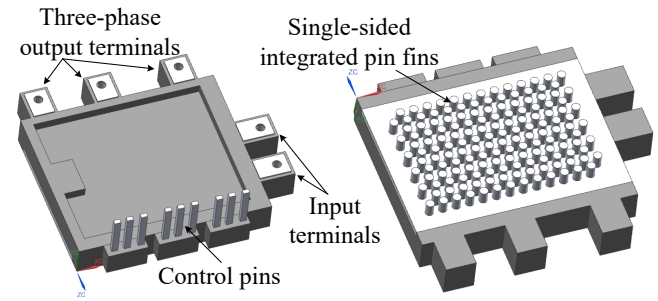


(a)

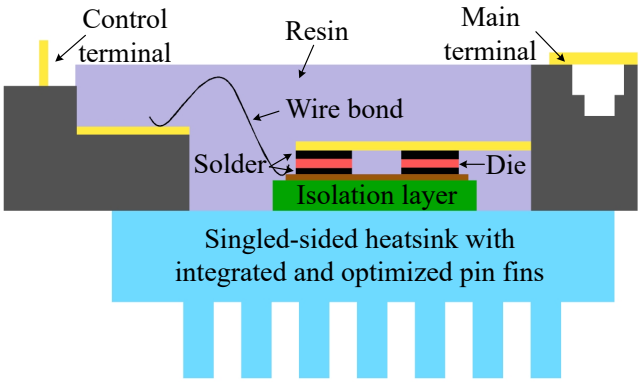


(b)

Figure 2.6: Mitsubishi J-series TPM power module: (a) CAD model (top and bottom views). (b) Internal cross-section.



(a)



(b)

Figure 2.7: Mitsubishi J1-series TPM power module: (a) CAD model (top and bottom views). (b) Internal cross-section.

of silicon with "special fillers" has been added between the busbar and the heatsink to provide thermal conduction and electrical insulation (Arai *et al.*, 2011). Figure 2.8 shows the internal cross-section of the module.

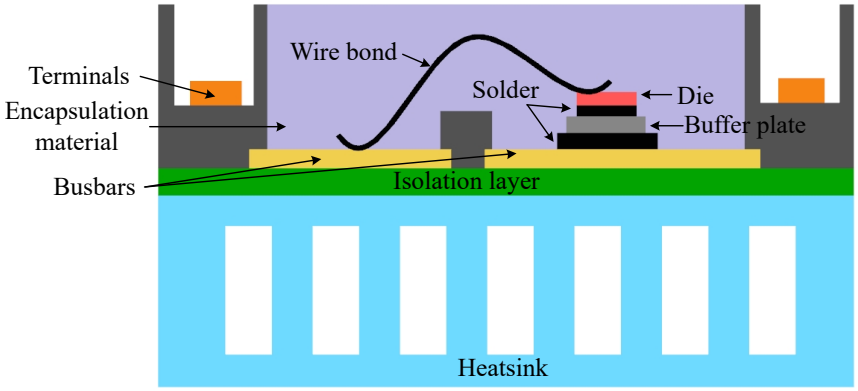


Figure 2.8: Cross-section of the power module in the Nissan LEAF.

More examples can be found in one of the author's published articles (Yang *et al.*, 2020). In general, the conventional packaging is still the mainstream. However, innovative structures have started to be applied in response to the higher demand for the next-generation of power electronics, mainly focusing on improving energy density and reliability, reducing losses and costs, etc.

2.4 Future Trends

As discussed above, the large-scale promotion of high-performance electric vehicles places higher requirements on power modules, including but not limited to cost, maximum rating, switching characteristics, heat dissipation performance, reliability, and

insulation. In the latest commercial vehicle power modules, there have been many innovative designs to improve the limitations of the conventional packaging technology in one or multiple aspects. However, there is still a long way to go before a design perfectly addresses most of the challenges, especially with the promotion of WBG devices. Recently, various novel packaging concepts and designs have been emerging in academia and industry. Each of them satisfies some of the requirements discussed above. However, they have not been widely implemented in the industry because of their limitations. In practice, these concepts are often combined to compensate for each other's shortcomings. A few examples are explained in detail in the following section.

In 2016, University of Applied Science Kempten (Sharma *et al.*, 2016) introduced a 1200 V/25 A power module, where semiconductor dies are packaged in a fashion of a printed-circuit-board (PCB). Its assembly process is illustrated in Figure 2.9. In fact, the so-called PCB embedded packaging has been applied in several projects (Parker *et al.*, 2015; Hou *et al.*, 2020; Löher *et al.*, 2016). The biggest advantage of PCB embedded packaging is the convenience of system integration, as explained above. Thus, it has most of the advantages of integrated packaging. When semiconductor dies are embedded in the PCB, the system volume could be further reduced, and the reliability could be improved. Due to the maturity of the PCB process, this technology reduces manufacturing difficulty and cost and improves system reliability. Thus, it is even more attractive for applications that require cost-effective and durable solutions. The selection of the embedding material is critical in this technology. First, a higher T_g is required to ensure high-temperature stability. Besides, proper thermal-mechanical and dielectric performances are necessary. A study from the Delft

University of Technology proposed that bismaleimide-triazine (BT) for embedding materials is a good selection for the embedding material (Hou *et al.*, 2018, 2019). BT is characterized to have a high T_g as 265^{o}C and a matched CTE of $5.3\times10^{-6}/^o$C.

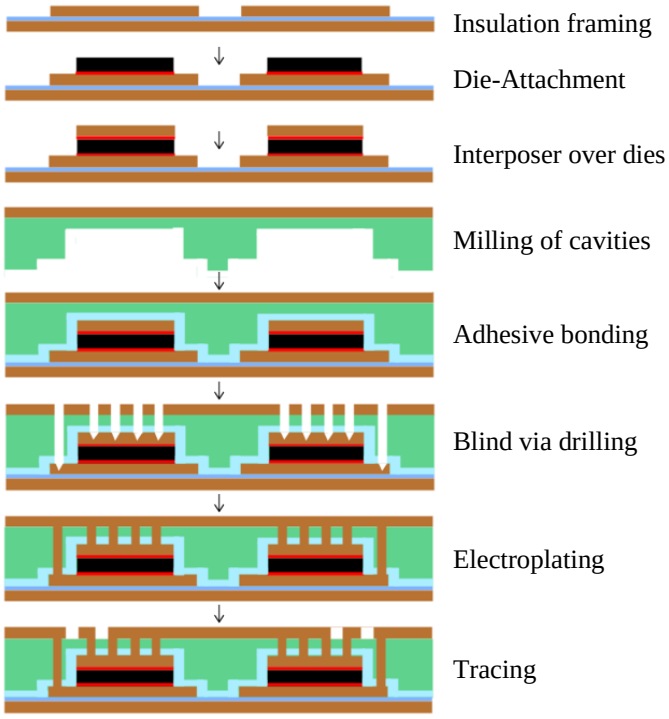


Figure 2.9: A PCB embedded packaging process (Sharma *et al.*, 2016).

In order to lower the risk of thermal-related failures, numerous designs have been proposed to enhance the heat dissipation capability of power modules. A typical example is the double-sided direct cooling technology. The idea is to largely decrease the thermal resistance from the semiconductor die to the ambient by providing two cooling paths from both the top and the bottom sides. The POL module from General Electric is shown in Figure 2.10, the interconnection is achieved by laser-drilled

vias on a polyimide/Cu layer, which forms flat surfaces at the top side. Two AMB substrates integrated with micro-channels are bonded to both sides to enhance cooling efficiency. The junction-to-fluid thermal resistance is reduced by around 50% compared with the single-sided cooling version (Yin *et al.*, 2017). Based on a similar concept, Oak Ridge National Laboratory (ORNL) developed an integrated power electronics building block (Chinthavali *et al.*, 2018). It achieves a 40% reduction of thermal resistance compared with single-sided cooling. The main challenge for double-sided direct cooling designs is the high complexity of their structures.

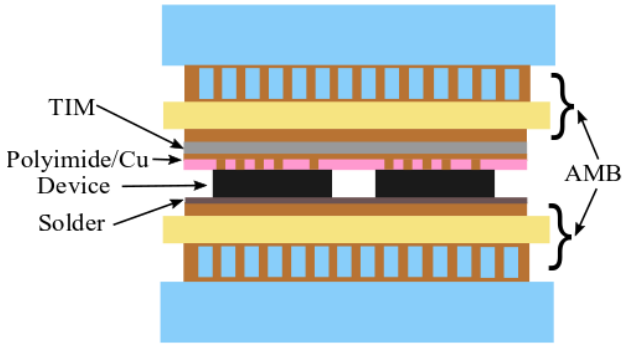


Figure 2.10: Double-side cooling POL module from GE (Yin *et al.*, 2017).

In addition, mitigating thermal reliability concerns can also be achieved by reducing the generation of thermal expansion. The most straightforward way to fulfill this purpose is selecting low-CTE materials, for example, the aforementioned BT material for PCB embedded packaging. Another example is the busbar-like press-pack module proposed by Grenoble Electrical Engineering Laboratory (Vagnon *et al.*, 2010), as shown in Figure 2.11, where molybdenum was used as contact pins which were placed near semiconductor dies. Molybdenum has a low CTE of $5.3\times10^{-6}/^{o}$C. Therefore, thermal deformation at these critical locations can be reduced.

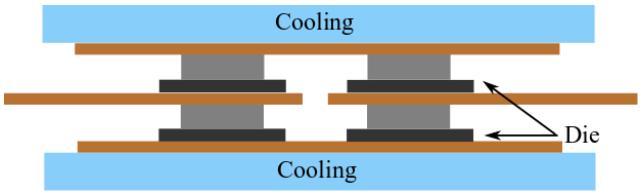


Figure 2.11: The busbar-like power module with Mo pins (Vagnon *et al.*, 2010).

Structural innovations have also been studied to achieve the same purpose, relieving thermal-mechanical concerns. In 2017, an innovative packaging structure was proposed by Zhu from Zhejiang Univeristy (Zhu *et al.*, 2017), whose layer stack-up is shown in Figure 2.12. A pressure contact interposer named "fuzz button" was introduced. It is a gold-plated beryllium (Be) copper wire that was reformed into a cylindrical pin. This structure not only allows a greater tolerance for clamping pressure distribution but also mitigates the thermal stress due to its excellent flexibility. Besides, massive usage of low-CTE materials, including Mo and the low-temperature co-fired ceramic, can be found in this design.

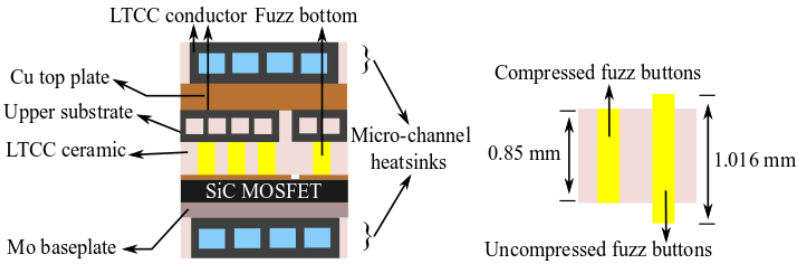


Figure 2.12: Press-pack structure with fuzzy bottom (Zhu *et al.*, 2017).

Examples shown in Figure 2.11 and Figure 2.12 can also be categorized into the press-pack packaging. In a conventional power module system, the most common failure modes are joint failures. In a press-pack power module, joints are formed by pressure-based bonding, which is simpler and more reliable compared to other connection methods, such as wire bonding, soldering, and sintering. Another example

is shown in Figure 2.13, where a Be-Cu spring is used to construct a press pack IGBT module (Xiaoyu *et al.*, 2006). This is another direction to eliminate thermal-related failures at joints. However, the electric and thermal conductivity of this type of joint is highly pressure-sensitive.

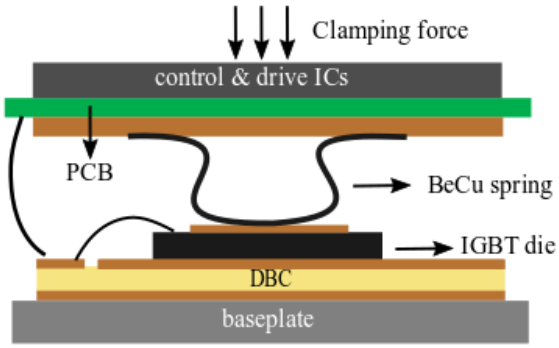


Figure 2.13: Press-pack structure with the BeCu spring (Xiaoyu *et al.*, 2006).

In general, new technologies that are expected to enhance the performance of power modules have been emerging in recent years. In terms of improving reliability, efforts have been made in different areas, including enhancing modules' heat dissipation capabilities, using suitable materials, and optimizing structures. However, most new designs have relatively complex structures. Simple and effective designs are still rare. In addition, the theoretical understanding of power modules' thermal-mechanical coupled performances still needs to be further investigated. Therefore, this thesis will focus on these directions.

Chapter 3

Silver-Sintered Molybdenum (SSM) Packaging Scheme for SiC Power Modules

This chapter will introduce the process of proposing the Silver-Sintered Molybdenum Packaging scheme for SiC power modules.

3.1 Motivations

Most of power modules' reliability issues are thermal-related. The dramatic differences in CTE between copper, aluminum, ceramic, and semiconductor materials are the primary reason for thermal-related failures in conventional modules. Meanwhile, the commonly-used solders and bond-wires are prone to failure when operating at a temperature higher than 150^{o}C.

In order to improve the reliability and temperature durability of SiC power modules, a new packaging scheme is proposed, whose layer stack-up is shown in Figure 3.1. Improvements are expected to be achieved by matching the CTE of materials and reducing the structural complexity.

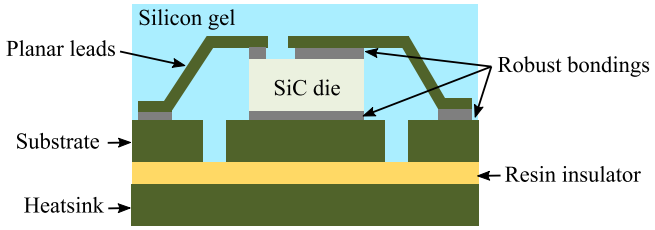


Figure 3.1: Layer configuration of the proposed structure.

The proposed scheme features a sandwiched stack-up, similar to the renowned IMS packaging. The SiC die is directly bonded to the substrate which not only forms the electric circuit but also works as a heat spreader. The substrate is bonded to the heatsink through the curing of the resin. And the resin layer also provides electrical insulation between the substrate and the heatsink. The top interconnections are achieved by planar leads which are expected to outperform the conventional bond-wires regarding reliability and stray inductance. Robust bonding will be applied at the joints between the die, leads, and substrate. The bonding technology will be discussed and selected in the following sections. Materials in this system are expected to have a similar CTE.

The system is encapsulated in silicone gel for environmental protection. Silicone gel is a very soft material whose modulus is 10^5 to 10^6 times smaller than other materials. Therefore, the effect of silicone gel on the mechanical behavior of other materials will be ignored in the following analysis.

It is worth mentioning that the heatsink can have enhanced liquid cooling features, like pin-fins. However, in this thesis, the heatsink is simplified as a flat plate, and a high equivalent convection coefficient will be applied at the bottom surface to represent the effect of enhanced liquid cooling designs in the following analysis.

3.2 Materials for Metal Layers

Metal layers have the greatest impact on the structural performance of the module, as they take up most of the mass. They are also in direct contact with weak points, the bonding layers. These metal layers are expected to have a similar CTE to that of SiC to reduce the risk of thermal failures. Meanwhile, they also serve as heat spreaders and electrical conductors. Therefore, they should have sufficient thermal and electrical conductivity.

A few candidate metals have been studied in the literature. Thanks to its low CTE, molybdenum (Mo) and its alloys are used in various innovative designs. In the press-pack module proposed by Zhu (Zhu *et al.*, 2017) and Vagnon (Vagnon *et al.*, 2010), Mo works as the buffer layer to mitigate the CTE difference within the module. Similarly, in the automotive industry, Nissan used Mo-Cu alloy as a buffer plate for the power module in their EV model, LEAF (Yang *et al.*, 2020). In addition, other potential materials have been reported by Jiang (Jiang *et al.*, 2013), including Tungsten (W) alloys and the Kovar alloy. Their major properties at room temperature (25^oC) are listed in Table 3.1 (Jiang *et al.*, 2013; AmericanElement, 2021; Plansee, 2022; ChemetalUSA, 2021).

Among these materials, pure Mo and Mo-Cu alloys have the most balanced properties. Their CTE is much lower than Cu and Al, and is close to that of SiC. They

Material	ρ (g/cm^3)	γ (% IACS)	k (W/m-K)	CTE ($10^{-6}/^o$C)
SiC	3.1	-	120	4
Pure Mo	10.2	0.32	140	5.3
Mo-Cu alloys (15% - 60% Cu)	9.4-10	0.37-0.65	170-260	6.8-11.5
Pure W	19.27	0.31	170	4.6
W-Cu alloys (10% - 50% Cu)	11.7-16.75	0.27-0.56	>170	7.4-13
Kovar alloy	8.3	-	17	5.9

Table 3.1: Properties of thermal management metals at 25^{o}C.

also have sufficient thermal and electrical conductivity. Thus, they are selected as candidates for all the metal layers in the proposed scheme. Further analysis is needed to determine the ratio of Cu in Mo-Cu alloys. On the contrary, other materials have unbalanced properties. The advantages of the Kovar alloy are its low CTE and mass density. However, its thermal conductivity is insufficient for the thermal management of power modules. Tungsten (W) and W-Cu alloys have slightly higher thermal conductivity than Mo-Cu alloys. However, they have higher CTE and mass density. In addition, W series are extremely hard to be manufactured.

3.3 Materials for Bonding Layers

In conventional modules, semiconductor dies are soldered on the substrate. The lead-free solder, SAC305 (Sn96.5Ag3Cu0.5), is one of the most common bonding materials. However, its melting temperature is only around 220^{o}C, leading to a high fatigue rate when the T_j is higher than 150^{o}C. Two advanced bonding technology, TLPB and nano-silver bonding, have been introduced in Chapter 2. As discussed,

nano-silver sintering is very suitable for power module applications. It exhibits great thermal and electrical conductivity. Meanwhile, its melting temperature (961^{o}C) is much higher than the operating temperature range of power modules. The superior reliability of nano-silver sintering bonding has been proved in a wide range of conditions. Therefore, it is selected as the material of the bonding layers for the proposed packaging.

3.4 Materials for the Resin Layer

The resin layer attaches the substrate to the heatsink and acts as the electrical insulator. Resin materials usually have low thermal conductivity. Thus, its thickness should be minimized. However, it should be thick enough to provide proper insulation. Epoxy resins are common-used in PCBs. However, they normally have a low glass transient temperature (T_g), lower than 150^{o}C, and a high CTE, higher than $20\times10^{-6}/^o$C in all directions. For the proposed packaging, the resin layer is expected to have a high temperature-durability (>200 ^{o}C) and a low CTE. Hou (Hou *et al.*, 2019) applied a BT resin in a PCB-embedded SiC power module. This material is provided by Mitsubishi Gas Chemical Company, INC. (MGC, 2022), with a part number of HL832NSF. BT resin has been proved to have a high glass-transient temperature (>250 ^{o}C) and a low CTE ($5.5\times10^{-6}/^o$C in x and y directions). Therefore, HL832NSF is suitable for the proposed packaging.

3.5 Material Properties

This section will provide all necessary material properties for following thermal-electrical-mechanical analysis. Properties of SiC, Cu, Al, BT HL832NSF resin, and Si_3N_4 are unpublished data provided by suppliers. Others are referenced from the literature.

3.5.1 Thermal Properties

The thermal conductivity (k) and specific heat capacity (C_P) of involved materials at 25^{o}C are listed in Table 3.2 (AmericanElement, 2021; Plansee, 2022; Munro, 1997; Zhang, 2014).

Material	k (W/m·K)	C_P (J/(g·K))
SiC	314	552
Si_3N_4	85	690
Al_2O_3	33	755
Mo	143	249
Mo85Cu15	170	-
Mo70Cu30	190	-
Mo60Cu40	230	-
Mo40Cu603	290	-
BT HL832NSF	0.7	900
TIM	0.7	1100
Silicone gel	0.2	-
Al	237	892
Cu	387	383
Sintered nano-silver (30% porosity)	200	168
SAC305 solder	58.7	236

Table 3.2: Thermal properties at 25^{o}C.

3.5.2 Elastic Properties

The mass density (ρ), elastic modulus (E), Poisson ratio (ν), and CTE of elastic materials at 25^{o}C are listed in Table 3.3 (MGC, 2022; Plansee, 2022; Munro, 1997; AmericanElement, 2021; Yang *et al.*, 2020; Zhang, 2014). The TIM is the THERM-A-GAP T630 Gels family from PAEKER. The silicon gel for encapsulation is the SEMICOSIL 915HT from WACKER.

Material	ρ (g/cm^3)	E (Gpa)	ν	CTE ($10^{-6}/^o$C)
SiC	3.21	410	0.14	3.3
Si_3N_4	3.20	300	0.3	3.3
Al_2O_3	3.98	416	0.231	4.6
Mo	10.28	330	0.31	5.3
Mo85Cu15	10.00	280	0.31	6.8
Mo70Cu30	9.80	230	0.31	7.5
Mo60Cu40	9.66	210	0.32	8.7
Mo40Cu60	9.40	170	0.33	11.5
BT HL832NSF	2.00	32	0.19	5.5 in $-y$ 20 in z
TIM	2.25	-	-	-
Silicone gel	0.98	$<10^{-6}$	-	300
Sintered nano-silver (70% relative density)	7.9	20	0.37	19.6
SAC305 solder	7.49	45	0.37	14.8

Table 3.3: Properties of elastic materials at 25^{o}C.

3.5.3 Elasto-Plastic Properties

Copper and aluminum have elasto-plastic mechanical behavior. Their main properties at 25^{o}C are listed in Table 3.4. The bi-linear elasto-plastic model is used.

Material	ρ (g/cm^3)	E (Gpa)	ν	CTE (10^{-6}/ ^{o}C)	Yield Strength (Mpa)	Tangent Modulus(Mpa)
Al	2.69	69	0.34	23.2	28	95.9
Cu	8.94	110	0.34	16.7	280	1192

Table 3.4: Properties of elasto-plastic materials at 25^{o}C.

3.5.4 Visco-Plastic Properties

The solder and sintered nano-silver are visco-plastic materials. They are commonly described using Anand visco-plastic model in the literature (Brown *et al.*, 1989; Siow, 2019). Anand model is usually used for materials that exhibit large, isotropic, visco-plastic deformations, and small elastic deformations. Therefore, it is very suitable for solders and sintered nano-silvers. A single-scalar internal variable, the deformation resistance (s), is used to construct the model. Anand model also requires no clear yield condition. The model is shown in Equation (3.5.1), which describes the relationship between stress (σ) and the plastic strain rate ($\dot{\varepsilon_p}$). Here, the plastic strain includes the creep strain. The evaluation of s is achieved in Equation (3.5.2) and Equation (3.5.3).

$$\dot{\varepsilon_p} = A \cdot e^{-\frac{Q}{TR}} \cdot [sinh(\xi \frac{\sigma}{s})]^{1/m} \tag{3.5.1}$$

$$\dot{s} = [h_0 \cdot |1 - \frac{s}{s^*}|^a \cdot sign(1 - \frac{s}{s^*})] \cdot \dot{\varepsilon_p} \tag{3.5.2}$$

$$s^* = \hat{s}[\frac{\dot{\varepsilon_p}}{A} \cdot e^{\frac{Q}{RT}}]^n \tag{3.5.3}$$

In these equations, T is the absolute temperature in the unit of K. s^* is the saturation value of s. Other involved parameters are shown in Table 3.5 (Basit *et al.*, 2016; Yu *et al.*, 2009). Basit reported the Anand parameters of re-flow soldered SAC305 solder with aging effects (Basit *et al.*, 2016). Parameters of the sintered nano-silver were experimentally obtained by Yu (Yu *et al.*, 2009) based on a material with 82% relative density (Chen *et al.*, 2008).

Parameters	Sintered nano-silver	SAC305 solder
S_0 (Mpa)	2.77	21
Q/R (1/K)	5709	9320
A (1/s)	9.81	3501
ξ	11	4
m	0.657	0.25
h_o (Gpa)	15.8	180
$\hat{S}$ (Mpa)	67.4	30.2
n	0.003	0.01
a	1	1.78

Table 3.5: Anand model parameters.

3.5.5 Temperature Dependent Properties

Accurate modeling of materials' temperature dependencies is the key to perform meaningful temperature-related analysis. The following paragraphs introduce material properties that vary noticeably over the concerning temperature range (from -40^{o}C to 200^{o}C).

Temperature dependent k of Al_2O_3, Cu, Al, SiC, Si_3N_4, and Mo are shown in Figure 3.2 (Munro, 1997; Plansee, 2022).

Temperature dependent CTE of Al_2O_3, Cu, Al, SiC, and SAC305 solder are shown

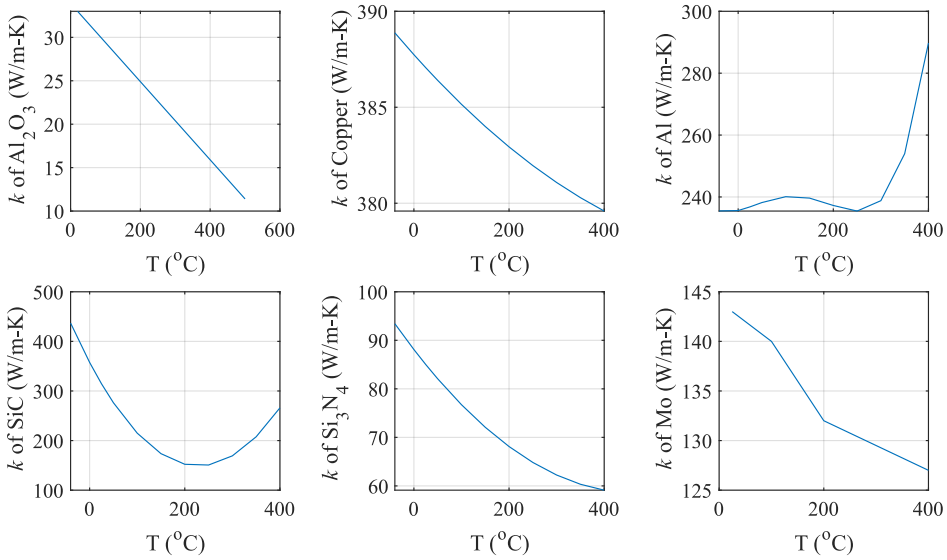


Figure 3.2: Temperature dependent k.

in Figure 3.3 (Munro, 1997; Plansee, 2022; Hasnine and Bozack, 2018).

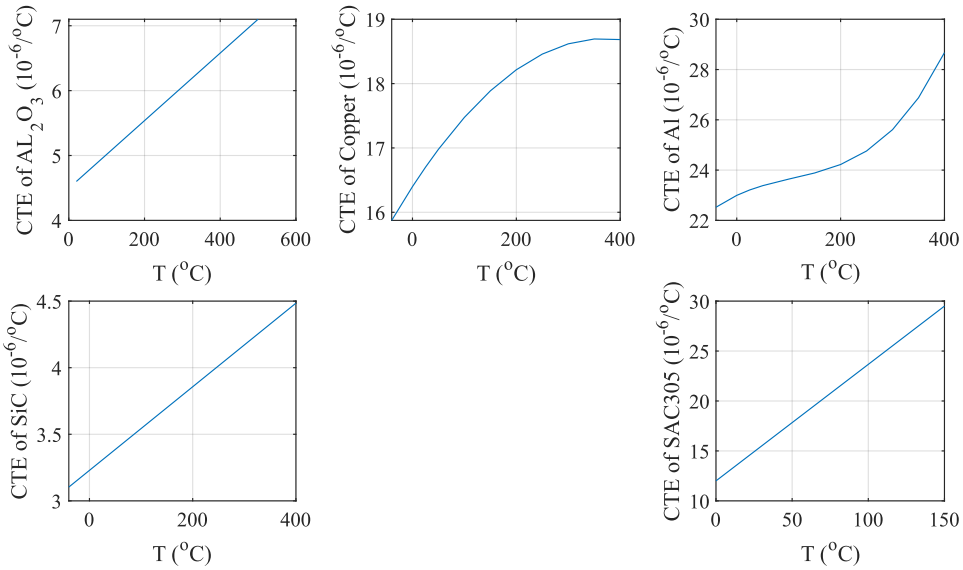


Figure 3.3: Temperature dependent CTE.

Temperature dependent C_P of Al_2O_3, Cu, Al, SiC, and Mo are shown in Figure

3.4.

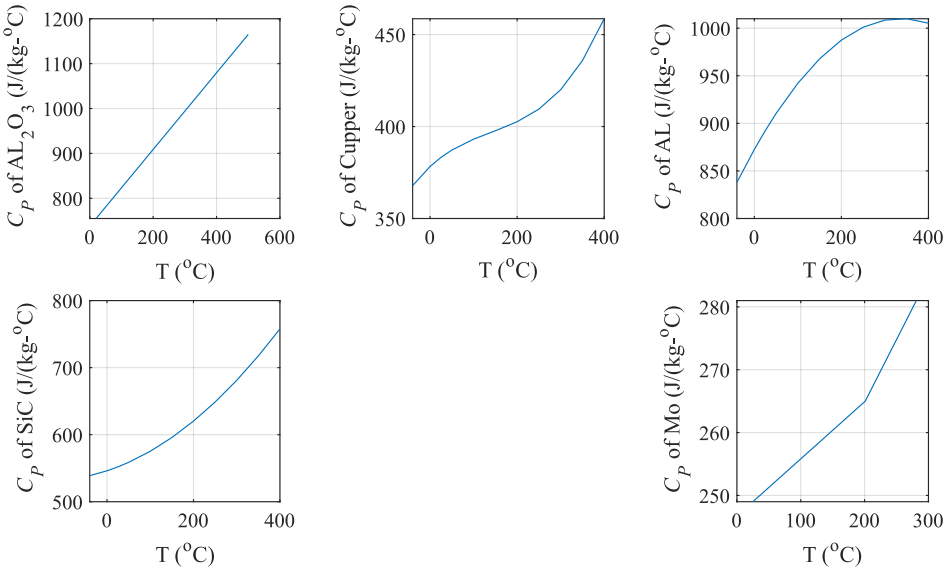


Figure 3.4: Temperature dependent C_P.

Temperature dependent E of Al_2O_3, Al, and Cu, SAC305 solder, and BT HL832NSF resin are shown in Figure 3.5 (Munro, 1997; Hasnine and Bozack, 2018; Alam *et al.*, 2016).

3.6 Evaluation of Candidate Materials for Metal Layers

As discussed above, Mo-Cu alloys are selected as candidate materials for metal layers due to their balanced properties. In this section, their performances will be evaluated by steady-state thermal-mechanical simulations through numerical tools. The results of this comparative study will guide the finalization of this material selection.

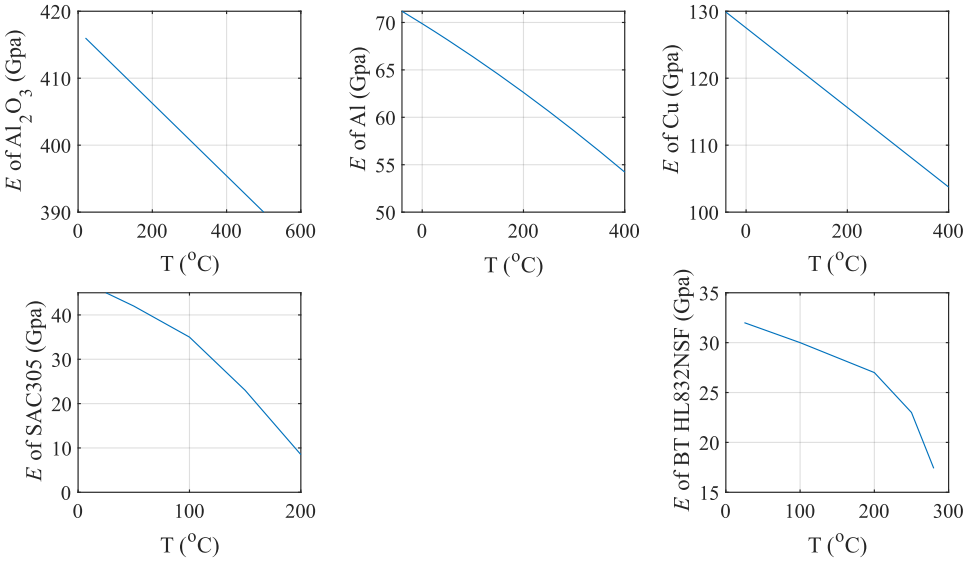


Figure 3.5: Temperature dependent elasticity.

3.6.1 Partial Structures

Power modules have complicated structures. In numerical simulations, it is common to just consider a partial structure around the critical location, in order to reduce the simulation complexity, which is essentially suitable for evaluating performance differences in comparative studies. This study considers a quarter of a symmetric cubic-shaped structure with the die located at the center. Partial structures based on the proposed packaging and the conventional packaging (benchmark) based on metallized Si_3N_4 substrate are shown in Figure 3.6 and Figure 3.7. The conventional packaging performs as a benchmark in this analysis. For a more valuable comparison, the high performance-ceramic, Si_3N_4, is used in the conventional packaging. Also, these two partial structures have the same footprint. Moreover, they all use nano-silver sintering as the die-attachment. The thickness of layers can be found in Table 3.6, determined according to common practices. The silicone gel is ignored in this

study due to its extremely low elastic modulus.

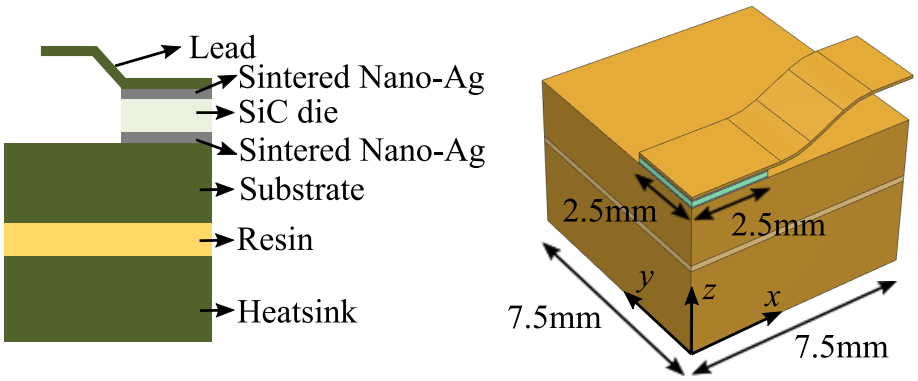


Figure 3.6: Partial structure of the proposed packaging: (a) layer configuration (b) 3D CAD model.

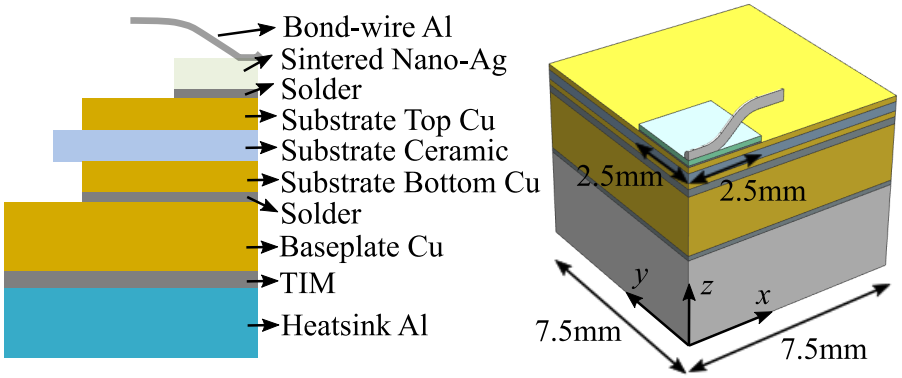


Figure 3.7: Partial structure of the conventional packaging: (a) layer configuration (b) 3D CAD model.

3.6.2 Comparative Study on Steady-State Thermal-Mechanical Performances

This study is to evaluate the steady-state thermal-mechanical performances of different packaging schemes and materials. Specifically, the temperature and stress profiles

Proposed packaging			Conventioanl packaging		
Layer	Description	Thickness (mm)	Layer	Description	Thickness (mm)
1	Lead	0.1	1	Bond-wire	d=0.38
2	Sintered nano-Ag	0.05	2	SiC	0.18
3	SiC	0.18	3	Sintered nano-Ag	0.05
4	Sintered nano-Ag	0.05	4	Substrate top Cu	0.2
5	Substrate	2	5	Substrate ceramic (Si_3N_4)	0.32
6	Resin	0.2	6	Substrate bottom Cu	0.2
7	Heatsink	3	7	Solder	0.25
			8	Baseplate Cu	2
			9	TIM	0.16
			10	Heatsink Cu	3

Table 3.6: Layer thicknesses of partial structures.

will be analyzed. Simulations are conducted in coupled Steady-State Thermal and Static Structural units of the ANSYS Mechanical, as shown in Figure 3.8. Simulations are subject to several assumptions: (1) As discussed above, the silicone gel is ignored. (2) The heat generation in the die is volumetrically uniform. (3) Except for the bottom of the heatsink, other surfaces are adiabatic. (4) For the conventional packaging, the bottom surface of the baseplate has no movement in the z direction. Thus, the thermal grease and the heatsink have no impact on mechanical performance. (5) For the proposed module, the bottom of the heatsink has no movement in the z direction. (6) The expansion-free temperature is 25^oC.

Identical thermal-mechanical boundary conditions are applied on both structures,

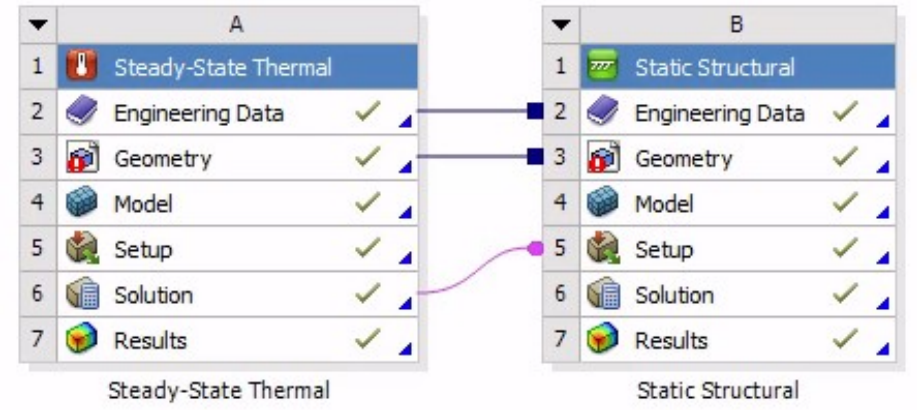


Figure 3.8: Coupled steady-state thermal and static structural units in ANSYS Mechanical packaging.

including: (1) A volumetric heat generation of 7.33×10^9 W/m^3 (equivalent to 33 W for each die) is set on the dies. (2) An effective convection coefficient of 5000 W/m-K is set at the bottom of heatsinks with a coolant temperature of 25 ^{o}C. (3) Frictionless supports are assigned to $x-z$ and $y-z$ planes in both structures. (4) A frictionless support is assigned at the bottom of the heatsink in the proposed packaging. (5) A frictionless support is assigned at the bottom of the baseplate in the conventional packaging.

A mesh of 1336349 elements is assigned to the partial structure with the proposed packaging. Critical locations, including the die, die-attachment, bond-wire, and their contacted surfaces, are modeled with finer elements, as shown in Figure 3.9. Mesh sensitive studies show that differences of critical results (stress, strain, deformation at the die and the die attach) are less than 5% when reducing the element size by 50%. Therefore, the configured mesh is adequate for this problem. The structure of the conventional packaging is meshed in a similar fashion.

Under identical heat losses and cooling boundary conditions, the two packaging

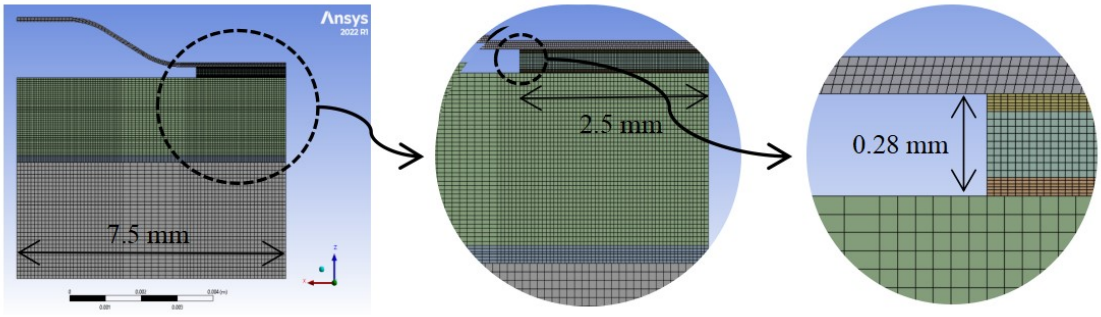


Figure 3.9: Mesh of the partial structure with the proposed packaging.

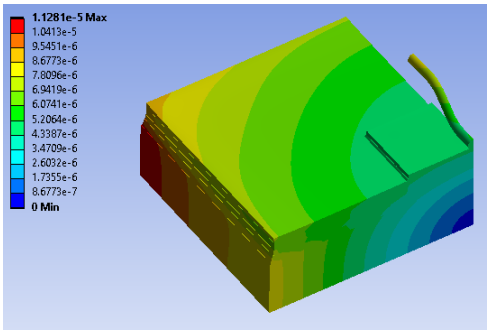
schemes with various material selections exhibit different temperature profiles. Table 3.7 illustrates the T_j and the calculated junction-to-fluid thermal resistance ($R_{th(j-f)}$). It is assumed that T_j equals the maximum temperature at the die.

Packaging schemes	T_j(^{o}C)	$R_{th(j-f)}$(K/W)
Conventional packaging	104.4	2.41
Proposed packaging with Mo40Cu60	109.2	2.55
Proposed packaging with Mo60Cu40	112.2	2.64
Proposed packaging with Mo70Cu30	115.2	2.73
Proposed packaging with Mo85Cu15	117.2	2.79
Proposed packaging with Pure Mo	121.2	2.92

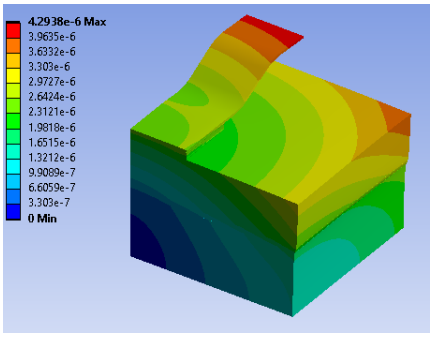
Table 3.7: Steady-state thermal results.

In the proposed packaging, a higher Cu ratio in the Mo-Cu alloy leads to a lower T_j and $R_{th(j-f)}$, due to the increase of k. For the DBC packaging, although it has more layers, the massive application of Cu results in better heat spreading, thus, a lower $R_{th(j-f)}$ is observed. It is worth mentioning that, in the proposed packaging, the temperature durability of materials can exceed 220^{o}C, which is much higher than the typical maximum operating temperature of power modules (150^{o}C to 175^{o}C).

As aforementioned, the thermal-mechanical reliability of power modules is not



(a) Deformation of the conventional packaging with Si_3N_4 (69x)



(b) Deformation of the proposed packaging with pure Mo (160x)

Figure 3.10: Steady state deformation.

only affected by the temperature but also by the mechanical properties of materials, such as CTE and elastic modulus. In other words, a proper selection of material could reduce the risk of failure despite the possible increase of $R_{th(j-f)}$ and T_j. The temperature gradient and CTE difference cause uneven expansion between layers. Figure 3.10 illustrates the deformation of two cases at steady-states. In the conventional packaging, due to the large CTE of Cu, the baseplate expands extensively, pulling other layers, while the Si_3N_4 layer buffers the expansion and reduces the transferring of expansion from Cu layers to the die and die-attachment layers. While in the proposed packaging, since the entire system shares a very close CTE, the difference of expansion is mainly generated by temperature gradient. Overall, the proposed packaging with pure Mo reduces the maximum deformation by 62% compared with the benchmark.

In steady-state thermal-mechanical simulations, stresses are viewed as the indicator of reliability. Lower thermal stress could prevent cracking and usually improve the resistance against fatigue. Table 3.8 lists the stress at different components in

conventional packaging. Table 3.9 elaborates on the stress in the proposed packaging with different Mo-Cu alloys. The brittle materials, including SiC and Si_3N_4, are evaluated using Maximum Principle Stress, while other materials use Von-Mises Equivalent Stress.

	Die	Ag	Bond-wire	Substrate top Cu	Substrate bottom Cu	Si_3N_4	Substrate solder	Baseplate
DBC Packaging	161.2	45.4	29.7	151.8	160.7	299.1	33.8	83.9

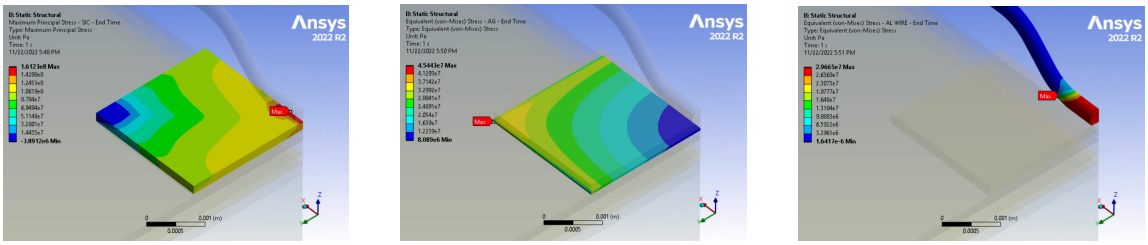
Table 3.8: Steady-state σ (Mpa) of the conventional packaging.

	Die	Ag top	Ag bottom	Lead	Substrate	Resin	Heatsink
Mo40Cu60	127.9	36.8	36.8	94.1	77.3	110.3	121.7
Mo60Cu40	88.1	30.4	28.7	72.5	69.9	103.9	117.5
Mo70Cu30	70.0	26.8	22.8	61.2	66.9	98.0	111.6
Mo85Cu15	60.7	24.3	18.8	58.4	72.7	108.8	125.1
Pure Mo	34.1	17.9	15.3	39.8	69.0	100.5	116.6

Table 3.9: Steady-state σ (Mpa) of the proposed packagings.

Typically, the stress at the die, die-attachment, bond-wires are the most concerned because they are related to major failure modes. Since the proposed packaging has no bond-wire, therefore, only the stress at the die and die-attachment are viewed as critical results.

In Table 3.9, results show that the proposed packaging could reduce the stress at the die by 20.7% to 78.8% compared with the conventional packaging, while the



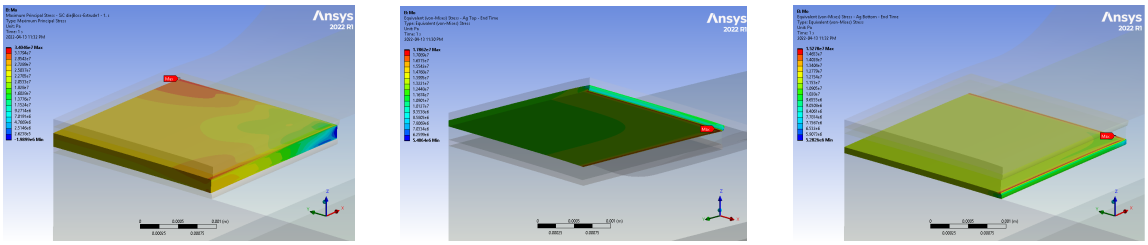
(a) Die. (b) Die-attachment. (c) Bond wire.

Figure 3.11: Stress - conventional packaging.

stress at die-attachment layers could be reduced by 18.9% to 66.3%. Among all the candidate Mo-Cu alloys, pure Mo exhibits the lowest critical stresses despite a higher junction temperature. This indicates that balancing CTE plays a decisive role in improving reliability. Therefore, pure Mo is selected for all metal layers in the proposed packaging. And the proposed scheme is named Silver-Sintered Molybdenum (SSM) packaging.

As seen in Figure 3.11, in the conventional packaging, the maximum stress of the die locates at the edge contacted with the bond-wire, due to the large CTE mismatch between Al and SiC. Correspondingly, the maximum stress point of the bond-wire locates at the heel point where cracks are likely to initiate. The die-attachment (sintered nano-silver) is constrained by SiC die from its top and the Cu layer at its bottom. Apparently, the bottom contact surface of the die-attach is subjected to a larger deformation, and the maximum stress is located at the far-end corner.

The critical stresses of the SSM packaging are shown in Figure 3.12. There are two die-attachment layers at the top and the bottom of the die. For both attachment layers, the maximum stress points are shown at the edges near the far-end of the surface contacted with the die. This is due to the CTE difference between SiC and Ag being larger than that between Mo and Ag.



(a) Die. (b) Top die-attachment. (c) Bottom die-attachment.

Figure 3.12: Stress - SSM packaging.

3.7 Summary

This chapter proposed an advanced packaging scheme based on CTE-matched materials. Steady-state thermal-mechanical analyses were conducted to evaluate different candidate materials for the core metal in the proposed packaging scheme. The comparative study demonstrated that pure Mo results in the lowest stress at critical locations, which indicates enhanced reliability. Therefore, pure Mo is selected as the core metal. The finalized layer configuration of the proposed packaging scheme is shown in Figure 3.13, which is named as Silver-Sintered Molybdenum (SSM) packaging. The design, prototyping, and characterization of a power module based on the SSM packaging will be introduced in the following chapters.

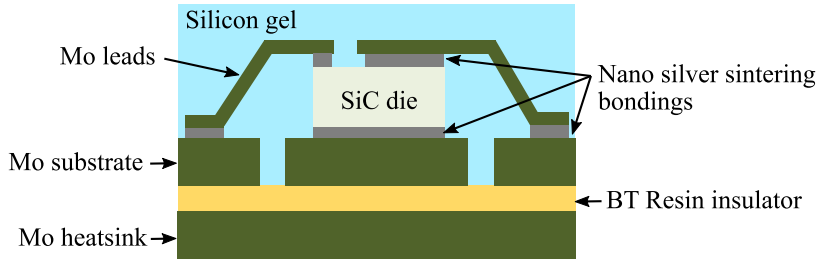


Figure 3.13: Layer configuration of the proposed SSM packaging.

Chapter 4

Thermal-Electrical Analytical Modeling of Power Modules with SSM Packaging

Analytical modeling methods for designing power modules are proposed in this chapter, including thermal modeling and stray inductance modeling. They are suitable for the proposed SSM packaging and other similar packaging schemes. Numerical simulations to verify the accuracy of these models are also presented in this chapter.

Power modules usually refer to power semiconductor devices composed of multiple dies to form a specific circuit. Electrical, thermal, and mechanical coupled multi-physics must be considered during their design. In terms of thermal management, T_j of semiconductor dies should be maintained within a safety threshold to ensure good reliability. On the electrical side, the most important concern is the stray inductance of the main switching loop (L_s). It should be minimized to reduce the switching loss and overvoltage during switching. There exist several methods to

evaluate T_j and L_s of power modules. Numerical methods, such as finite-element-analysis (FEA), are accurate but time-consuming, which are mostly used in simulating a fixed structure. Instead, analytical models are more suitable for rapid calculations during an optimization process.

Generally, there are two types of analytical thermal models, the lumped thermal network model and the physical-based model. The thermal network varies from one-dimensional (1-D) structures (Bouguezzi *et al.*, 2016; Yang *et al.*, 2021) to three-dimensional (3-D) structures (Chang *et al.*, 2019; Bahman *et al.*, 2018). However, since the network parameters need to be extracted from numerical simulations, this method can only be used for a fixed geometry, making it impractical to optimize geometric variables. Some studies reported physical-based thermal networks. However, they are only verified to be accurate with 1-D simplified geometries (Yang *et al.*, 2021). Masana (Masana, 1996) introduced a simplified physical-based thermal resistance model, the constant spreading angle model. Nevertheless, this model is only verified to be accurate with a single-layer geometry. Bouguezzi (Bouguezzi *et al.*, 2016) integrated the constant spreading angle model with a 1-D thermal network. Although, the thermal coupling between different heat sources still requires FEA calibration. Fourier-based models are another type of analytical model. They directly solve the heat transfer equations, such as Laplace's equation for the steady-state conduction, in the form of finite Fourier series (Swan *et al.*, 2012; Choudhury and Rogers, 2019; Culham *et al.*, 2000; Monier-Vinard *et al.*, 2013). The challenge is to determine the Fourier constants using boundary conditions. Thus, the geometry needs to be simplified. Monier-Vinard (Monier-Vinard *et al.*, 2013) and Culham (Culham *et al.*, 2000) proposed Fourier-based solutions for PCBs with embedded heat sources.

Swan (Swan *et al.*, 2012) and Choudhury (Choudhury and Rogers, 2019) derived the temperature field of conventional power modules based on this method and obtained a good accuracy of 96.5%. Generally, the Fourier-based models exhibit improved accuracy than other analytical models and are suitable for optimization.

Similarly, conductors' L_s can be estimated by numerical methods and analytical models. Numerical tools, such as ANSYS Q3D, are now convenient and accurate, but again, impractical for optimizing complex geometries. The analytical expression of L_s has been studied for decades. There exist extensively validated equations for simple conductors, such as wires and coils, which have been summarized by Grover (Grover, 1962) and Leferink (Leferink, 2002). However, power modules have complicated internal conductors. Wada (Wada *et al.*, 2013) introduced a partial-inductance model for busbars, which is also suitable for power module conductors.

The proposed SSM packaging belongs to the category of IMS packaging. Therefore, directly applying conventional modules' design methods would be inadequate. Specific models are developed in this chapter for designing modules with the SSM packaging.

Half-bridge modules containing two dies are studied in this chapter. The layout of this module is shown in Figure 4.1, where several geometric parameters are defined and will be considered as variables in the optimization.

4.1 Analytical Thermal Model

Thermal management is essential in power module design. The temperature distribution, especially T_j at dies, affects the reliability of the module.

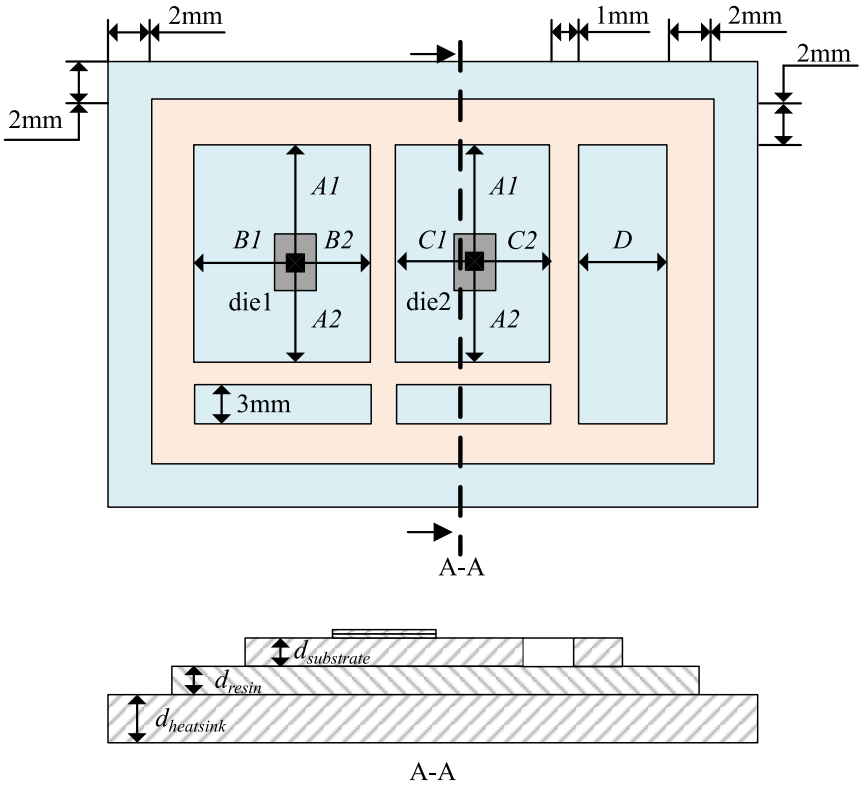


Figure 4.1: Geometrical layout of half-bridge SSM module.

4.1.1 Fourier-Based Model for a Three-Layer Simplified Geometry

The internal structure of power modules is similar to a stack of cuboid layers with a unified section area. On top of the first layer, several rectangular areas receive the heat flux, representing the corresponding areas on the substrate, and are equal to the area of semiconductor dies. The simplified geometry is illustrated in Figure 4.2. If multiple heat sources exist, the total temperature field is the summation of fields when considering each heat source individually due to the linearity of this heat transfer problem.

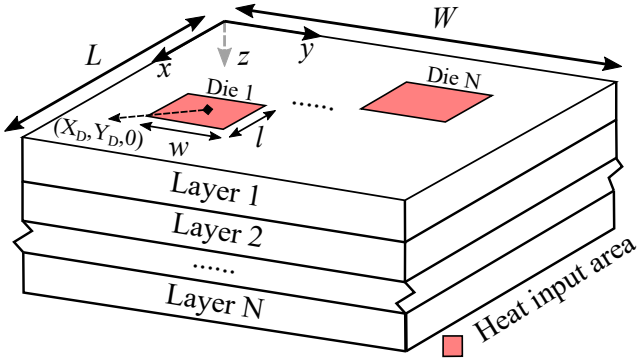


Figure 4.2: Simplified power module with cuboid layers.

The governing equation for the steady-state 3-D heat transfer is Equation (4.1.1), where θ is the temperature rise from the coolant to a specific location inside the structure.

$$\frac{\partial^2\theta}{\partial x^2} + \frac{\partial^2\theta}{\partial y^2} + \frac{\partial^2\theta}{\partial z^2} = 0 \tag{4.1.1}$$

Boundary conditions for the geometry in Figure 4.2 are summarized in Equation (4.1.2), (4.1.3), and (4.1.4). Specifically, in the SSM packaged module, there are only

three layers to be considered: the substrate layer, the resin layer, and the heatsink layer.

On top of layer 1 (the substrate layer):

$$\begin{cases} \frac{\partial\theta}{\partial z}|_{z=0} = -\frac{P}{k_1 lw} \text{ (Inside die areas)} \\ \frac{\partial\theta}{\partial z}|_{z=0} = 0 \text{ (Outside of die areas)} \end{cases} \tag{4.1.2}$$

At interfaces between layers:

$$\begin{cases} k_i \frac{\partial\theta_i}{\partial z}|_{z=z_i} = k_{i+1} \frac{\partial\theta_{i+1}}{\partial z}|_{z=z_i} \\ \theta_i(x, y, z_i) = \theta_{i+1}(x, y, z_i) \end{cases} \tag{4.1.3}$$

At the bottom of layer 3 (the heatsink layer):

$$k_3 \frac{\partial\theta_3}{\partial z}|_{z=z_3} = -h \cdot \theta_3|_{z=z_3} \tag{4.1.4}$$

where k_i denotes the thermal conductivity of the i_{th} layer. z_i refers to the bottom of the i_{th} layer, which equals $\sum_{j=1}^{i} d_j$, where d_i is the thickness of the i_{th} layer. P is the heat flow at each heat input area. h is the effective convection coefficient at the bottom. The geometrical variables, including X_D, Y_D, l, w, L, and D, can be found in Figure 4.2.

This problem can be solved by the Separation of Variables method (Wendl, 2012; Choudhury and Rogers, 2019). And the general solution is given in (4.1.5).

$$\begin{aligned}\theta(x,y,z) = A_{i0} + B_{i0}z + \sum_{m=1}^{\infty} cos(a_m x)[A_{im}cosh(a_m z) \\ + B_{im}sinh(a_m z)] \\ + \sum_{n=1}^{\infty} cos(b_n y)[A_{in}cosh(b_n z) \\ + B_{in}sinh(b_n z)] \\ + \sum_{m=1}^{\infty}\sum_{n=1}^{\infty} cos(a_m x)cos(b_n y)[A_{imn}cosh(c_{mn} z) \\ + B_{imn}sinh(c_{mn} z)]\end{aligned} \tag{4.1.5}$$

where $a_m{=}\frac{m\pi}{L}$, $b_n{=}\frac{n\pi}{W}$, $c_{mn}{=}\sqrt{a_m + b}$. A_{i0}, B_{i0}, A_{im}, B_{im}, A_{in}, B_{in}, A_{imn}, and B_{imn} are parameters to be determined by integral and differential operations of boundary conditions. Choudhury (Choudhury and Rogers, 2019) proposed an iterative method to derive those parameters.

The SSM packaging scheme has a three-layer configuration. Although, only the temperature distribution of the first layer is needed to calculate the junction temperature. The required parameters are solved and elaborated from Equation (4.1.6) to (4.1.18). With those parameters, the temperature field can be easily expressed using Equation (4.1.5) and (4.1.19).

$$B_{10} = -\frac{P}{k_1 LW} \tag{4.1.6}$$

$$A_{10} = \frac{P}{LW}[\frac{d_1}{k_1} + \frac{d_2}{k_2} + \frac{d_3}{k_3} + \frac{1}{h}] \tag{4.1.7}$$

$$B_{1m} = \frac{-4Pcos(a_m X_D)sin(a_m l/2)}{LWlk_1 a_m^2} \tag{4.1.8}$$

$$B_{1n} = \frac{-4Pcos(b_n Y_D)sin(b_n w/2)}{LWlk_1 b_n^2} \tag{4.1.9}$$

$$B_{1mn} = \frac{B_{1m}B_{1n}a_m b_n LWk_1}{c_{mn}} \tag{4.1.10}$$

$$A_{1m} = -\frac{B_{1m}}{V_{1m}} \tag{4.1.11}$$

$$A_{1n} = -\frac{B_{1n}}{V_{1n}} \tag{4.1.12}$$

$$A_{1mn} = -\frac{B_{1mn}}{V_{1mn}} \tag{4.1.13}$$

A few intermediate parameters are needed in the expressions above. They are listed below.

$$V_{1p}(p = m, n, mn) = \frac{(\frac{V_{3p}U_{2p}-I_{2p}}{V_{3p}I_{2p}-O_{2p}})U_{1p} - I_{1p}}{(\frac{V_{3p}U_{2p}-I_{2p}}{V_{3p}I_{2p}-O_{2p}})I_{1p} - O_{1p}} \tag{4.1.14}$$

$$V_{3p} = \frac{\delta sinh(\delta z_3) + \frac{hcosh(\delta z_3)}{k_3}}{\delta cosh(\delta z_3) + \frac{hsinh(\delta z_3)}{k_3}} \tag{4.1.15}$$

$$U_{ip} = cosh^2(\delta \sum_{j=1}^{i} d_j) - \frac{k_i}{k_{i+1}} sinh^2(\delta \sum_{j=1}^{i} d_j) \tag{4.1.16}$$

$$I_{ip} = sinh(\delta \sum_{j=1}^{i} d_j) cosh(\delta \sum_{j=1}^{i} d_j)(1 - \frac{k_i}{k_{i+1}}) \tag{4.1.17}$$

$$O_{ip} = sinh^2(\delta \sum_{j=1}^{i} d_j) - \frac{k_i}{k_{i+1}} cosh^2(\delta \sum_{j=1}^{i} d_j) \tag{4.1.18}$$

(if $p = m$, $\delta = a_m$; if $p = n$, $\delta = b_n$; if $p = mn$, $\delta = c_{mn}$)

Finally, T_j needs to include the coolant temperature ($T_{coolant}$) and the temperature-rise at the die bonding layer and the die layer, as shown in Equation (4.1.19).

$$T_j = \theta(X_D, Y_D, 0) + \frac{Pd_{Ag}}{lwk_{Ag}} + \frac{Pd_{die}}{lwk_{die}} + T_{coolant} \tag{4.1.19}$$

A brief introduction of the solving process of Fourier parameters is given in the following paragraphs, which is based on the iterative process proposed by Chourdhury (Choudhury and Rogers, 2019).

STEP1: Obtain B_{1m}, B_{1n}, B_{1mn}, and B_{10}:

Substitute Equation (4.1.5) into Equation (4.1.2) and solve it. Then, Equation (4.1.6), (4.1.8), (4.1.9), and (4.1.10) are obtained.

STEP2: Obtain A_{10}:

Assume a two-layer structure. Use the bottom surface boundary condition (Equation (4.1.4)) and Equation (4.1.5), Equation (4.1.20) can then be obtained. Use the interface boundary conditions (Equation (4.1.3)) and Equation (4.1.5), Equation (4.1.21) and (4.1.22) can be then obtained. Then, Equation (4.1.23) can be obtained by combining Equation (4.1.6) and (4.1.21). Use Equation (4.1.20), (4.1.22), and (4.1.23), A_{10} for the assumed two-layer structure can be obtained, as shown in Equation (4.1.24). Therefore, A_{10} for a three-layer structure (SSM packaging) can be

written in the same pattern, as shown in Equation (4.1.7).

$$-(h/k_2)A_{20} = B_{20}(1 + \frac{h(d_1 + d_2)}{k_2}) \tag{4.1.20}$$

$$k_1 B_{10} = k_2 B_{20} \tag{4.1.21}$$

$$A_{10} + B_{10}d_1 = A_{20} + B_{20}d_1 \tag{4.1.22}$$

$$B_{20} = -\frac{P}{k_2 LW} \tag{4.1.23}$$

$$A_{10} = \frac{P}{LW}(\frac{d_1}{k_1} + \frac{d_2}{k_2} + \frac{1}{h}) \tag{4.1.24}$$

STEP3: Obtain A_{1m}, A_{1n}, and A_{1mn}:

Substitute Equation (4.1.5) into Equation (4.1.4) and solve it. Then, Equation (4.1.15) is obtained. Combining with Equation (4.1.3), the following equation can be obtained.

$$V_{1p}(p = n, m, mn) = -\frac{B_{1m}}{A_{1m}} = \frac{V_{2p}U_{1p} - I_{1p}}{V_{2p}I_{1p} - O_{1p}} \tag{4.1.25}$$

$$V_{2p}(p = n, m, mn) = -\frac{B_{2m}}{A_{2m}} = \frac{V_{3p}U_{2p} - I_{2p}}{V_{3p}I_{2p} - O_{2p}} \tag{4.1.26}$$

Substitute Equation (4.1.14) into Equation (4.1.25) and (4.1.26), then A_{1m} can be solved. A_{1n} and A_{1mn} can be obtained in a same fashion.

4.1.2 Decoupled Fourier-Based Model for IMS-type Power Modules

The aforementioned original Fourier-based method has two major limitations. First, areas of all layers are assumed equal, which is unrealistic. For example, the heatsink layer is usually larger than the substrate layers. Thus, it is necessary to assign an equivalent area for all layers. Defining the equivalent area is essential to achieve accurate estimation using Fourier based thermal models. In practice, the equivalent area should be defined based on the thermal-coupling and heat spreading. In another word, the equivalent area should represent where the main heat flux pass through horizontally. Second and more importantly, all layers are assumed to be a single and united body. However, in power modules, some layers are separated into segments, such as the conductor layer of the substrate. This assumption does not have a noticeable effect on conventional power modules with metallized ceramic substrate, because their tracing layer is very thin and has an unremarkable impact on the heat spreading. However, this assumption could lead to significant errors when applied in IMS-type modules.

IMS-type packaging is featured with a sandwich structure. Unlike the conventional packaging, where the baseplate is the main heat spreader, the heat spreading in IMS-type modules mostly occurs at the thick substrate layer. Also, because of the extremely low k of the resin layer, the thermal coupling between different substrate segments is very minimum. The horizontal heat flux commuting between different segments are extremely low and neglectable. Therefore, each segment should be considered individually.

To capture the unique heat transfer characteristics of IMS-type modules, a decoupling method is proposed. The decoupling of a half-bridge module with two dies is given in Figure 4.3 as an example. There are two substrate segments that are receiving the heat flux. The volume under each segment is considered as an individual heat transfer unit, which is utilized to calculate the T_j of the corresponding die using the Fourier-based method. The equivalent area for each individual calculation equals to the area of the corresponding Mo substrate due to aforementioned reasons.

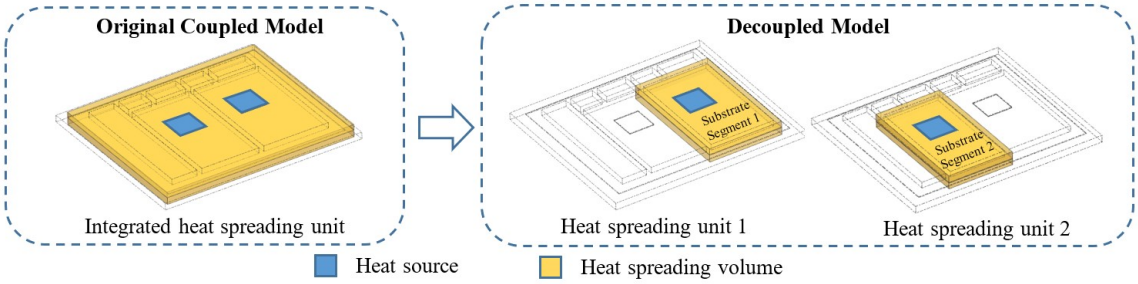


Figure 4.3: Decoupling of heat spreading in a half-bridge IMS-type module.

4.1.3 Simulation evaluation

To evaluate the accuracy of the decoupled Fourier-based method for IMS-type power modules, thermal performances of six different designs are estimated using the original coupled model, the decoupled model, and FEA simulations (conducted in ANSYS Mechanical). Their geometrical topology follows the schematic shown in Figure 4.1, and their dimensions are listed in Table 4.1. Other dimensions remain constants, specifically, A1=A2=10mm; D=5mm; $d_{substrate}$=1mm; d_{resin}=0.2mm. These cases covered symmetric and asymmetric designs with different footprints.

In simulations, h is 5000 W/m^2·^{o}C at 105^{o}C coolant temperature. P_{loss} is 41 W for each die. T_j results of die 1 (located on substrate segment 1) are illustrated in

Table 4.1: Dimension of cases for thermal model evaluation.

Dimensions	Case A	Case B	Case C	Case D	Case E	Case F
B1 (mm)	10	10	10	15	10	15
B2 (mm)	10	10	10	15	10	15
C1 (mm)	5	10	15	10	5	5
C2 (mm)	15	10	5	10	5	5

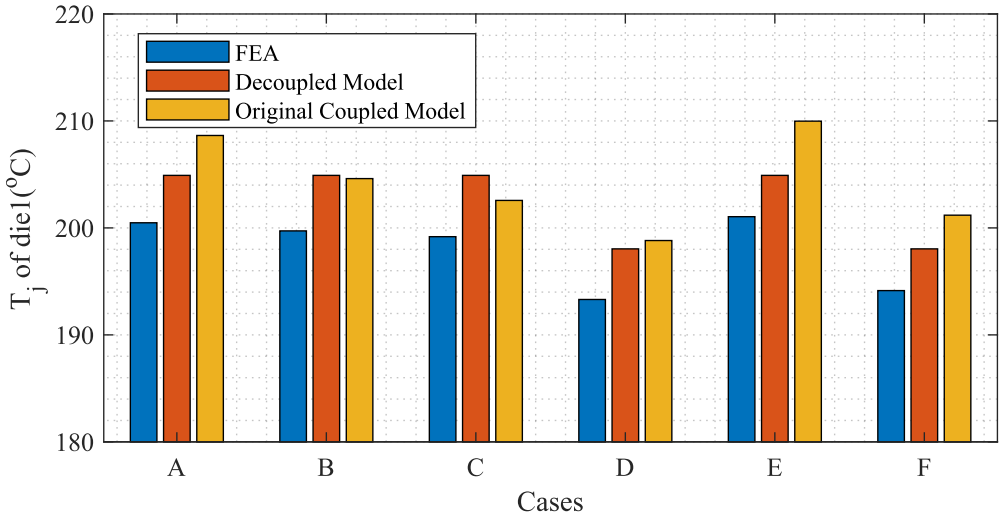


Figure 4.4: T_j of die 1.

Figure 4.4. FEA results of cases A, B, and C show that T_j of die 1 is not affected by the area of segment 2, which is also found in results from the decoupled model. Although, the original coupled model fails to capture this trend. Figure 4.5 shows T_j of die 2. The original coupled model shows significantly larger errors in cases E and F, where segment 1 is several times larger than segment 2. Overall, when estimating the temperature-rise (T_j-$T_{coolant}$) for symmetric layouts, average errors are 3.7% and 4.7% for the decoupled model and the original coupled model, respectively. While for asymmetric layouts, they are 3.2% and 9.5%, respectively.

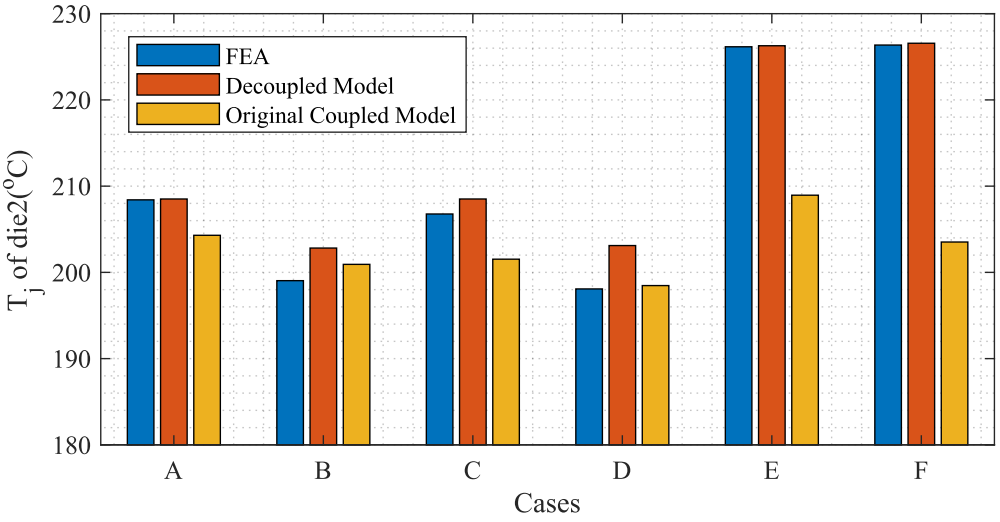


Figure 4.5: T_j of die 2.

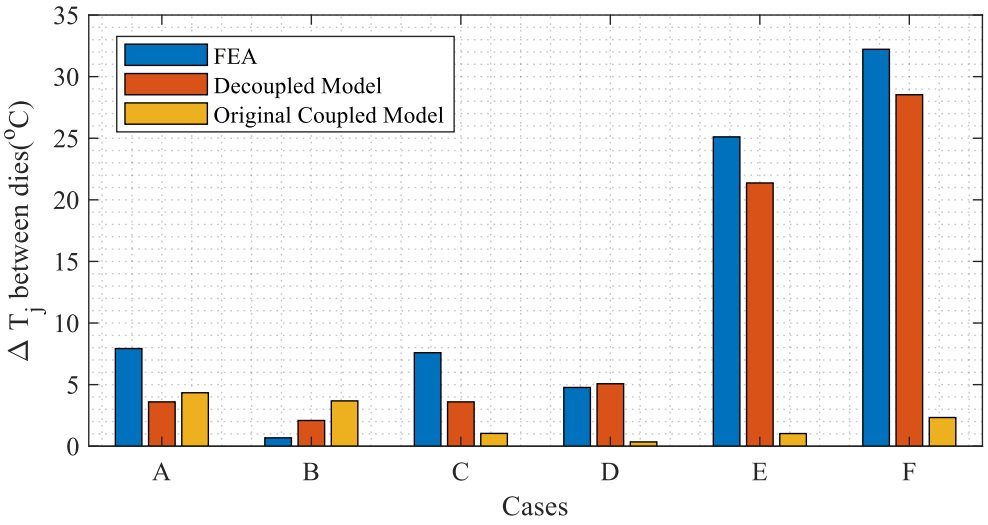


Figure 4.6: ΔT_j between dies.

More importantly, as can be seen in Figure 4.6, when using the original coupled model, the estimations of ΔT_j between two dies are very inaccurate for asymmetric cases (D, E, and F). Only in case A does the original coupled model show a slightly smaller error. This is because that die 2 is located closer to die 1 instead of at the

center of segment 2, which strengthens the coupling effect between the two segments. Overall, the decoupled model reduced the average error of ΔT_j estimation from 93.8% to 10.9% for asymmetric layouts. As expected, the proposed decoupled model exhibits significant benefits for IMS-type modules by considering the barrier effect between the substrate segments and the low thermal spreading at the resin layer. Therefore, it will guarantee accurate calculations during the design optimization.

4.2 Analytical Stray Inductance Model

Stray inductance leads to overvoltage and contributes to the switching loss of power modules. Therefore, it needs to be minimized. Power modules have busbar-like internal conductors. Therefore, a method called the partial inductance model is adopted in this work, which was initially developed for estimating the L_s of laminated busbars.

The total inductance of the power modules' main commutation loop (L_s) is of the greatest concern, for the reason that it contributes to the drain-source voltage overshot during switching. Therefore, minimizing L_s is desired when designing power modules. As highlighted in Figure 4.7, L_s is a combination of several inductance segments. Since there is no overlapping between these corresponding conductors, mutual-inductance can be ignored. Therefore, the total L_s is the summation of self-inductances of all conductor segments, as given in (4.2.1).

$$\begin{aligned} L_s = L_{P-Tr} + L_{P-HD} + L_{HS-O} + L_{O-LD} \\ + L_{LS-N} + L_{N-Tr} \end{aligned} \tag{4.2.1}$$

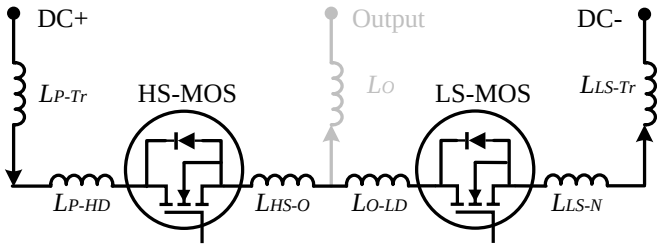


Figure 4.7: Main commutation loop in a half-bridge module.

4.2.1 Partial Inductance Model for Rectangular Conductors

The partial inductance model for rectangular conductors is introduced by Wada (Wada *et al.*, 2013). In this theory, a wide conductor can be separated into N sets of thin conductors in parallel with a square cross-section, as shown in Figure 4.8. Furthermore, thin rectangular conductors can be simplified as circular wires whose radius (r) equals half of the thickness (t). The empirical equation of the self-inductance of a single wire (L_w) is obtained in Equation (4.2.2). And the mutual-inductance between the i_{th} and j_{th} wires (M_{w-ij}) are given in Equation (4.2.3).

$$L_w = \frac{\mu_0 l}{8\pi} + \frac{\mu_0}{2\pi}\left(l \ln \frac{\sqrt{r^2+l^2}+l}{r} - \sqrt{r^2+l^2} + r\right) \tag{4.2.2}$$

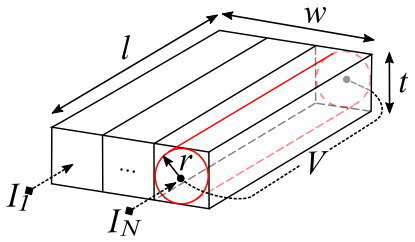


Figure 4.8: Partial-inductance scheme of a rectangular conductor.

$$M_{w-ij} = \frac{\mu_0}{2\pi}(l \ln \frac{\sqrt{(d_{ij}+2r)^2+l^2}+l}{d_{ij}+2r} - \sqrt{(d_{ij}+2r)^2+l^2} + (d_{ij}+2r)) \tag{4.2.3}$$

where μ_0 (free space permeability) is $4\pi\times10^{-7}$ H/m, l is the length of the wire, d_{ij} is the center-to-center distance between the i_{th} and j_{th} wires.

The L_s of the wide conductor can be obtained by the combination of the partial inductances of these paralleled wires. The voltage and current of these conductors are subjected to Equation (4.2.4). The matrix is inversed in Equation (4.2.5). The total current is the summation of all wires' current, as written in Equation (4.2.6). Therefore, the total inductance L_s is given in Equation (4.2.7).

$$\begin{bmatrix} V \\ ... \\ V \end{bmatrix} = jw \begin{bmatrix} L_w \ ... \ M_{w-1n} \\ ... \ ... \ ... \\ M_{w-n1} \ ... \ L_w \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ ... \\ I_n \end{bmatrix} \tag{4.2.4}$$

$$\begin{bmatrix} I_1 \\ ... \\ I_n \end{bmatrix} = \frac{1}{jw} \begin{bmatrix} L_w \ ... \ M_{w-1n} \\ ... \ ... \ ... \\ M_{w-n1} \ ... \ L_w \end{bmatrix}^T \cdot \begin{bmatrix} V \\ ... \\ V \end{bmatrix} \tag{4.2.5}$$

$$I = I_1 + ... + I_n = \frac{1}{jw} \times sum(\begin{bmatrix} L_w \ ... \ M_{w-1n} \\ ... \ ... \ ... \\ M_{w-n1} \ ... \ L_w \end{bmatrix}^T) \times V \tag{4.2.6}$$

$$L_s = (sum(\begin{bmatrix} L_w \ ... \ M_{w-1n} \\ ... \ ... \ ... \\ M_{w-n1} \ ... \ L_w \end{bmatrix}^T))^{-1} \tag{4.2.7}$$

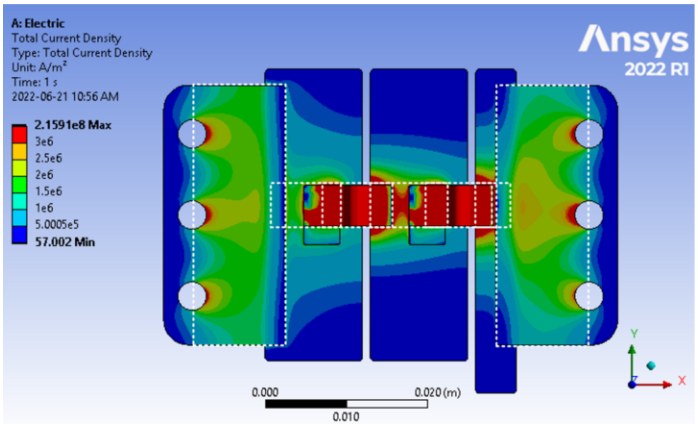


Figure 4.9: Current density distribution in a SSM half-bridge module.

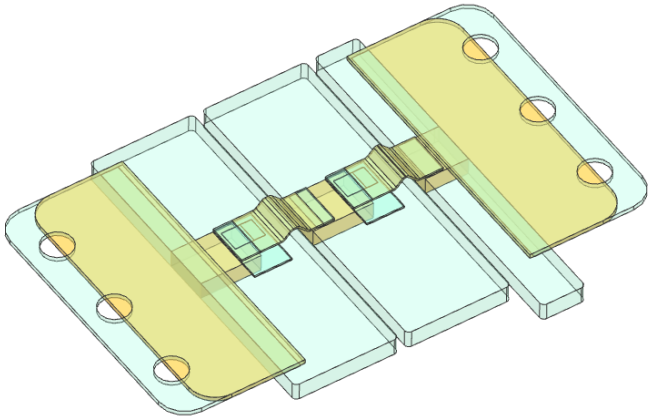


Figure 4.10: Effective conductor layout for stray inductance calculation.

The conduction trace of half-bridge modules consists of several components, including terminals, substrates, and leads. When the module is conducting the main power, the current density is usually uneven, as shown in Figure 4.9. Therefore, only

the high-density portions are considered as effective conductors in the calculation of L_s, which are the highlighted parts in Figure 4.10.

4.2.2 Simulation evaluation

Numerical simulations in ANSYS Q3D parasitic extractor are performed to evaluate the accuracy of the analytical model proposed above. First, single rectangular conductors with various l, w, and t are simulated using both Q3D and the analytical model. The frequency is 60 MHz in all simulations, which refers to the common switching speed of SiC MOSFETs. Results of the parametric comparisons are shown in Figure 4.11, which shows that errors of the partial-inductance model are less than 11%.

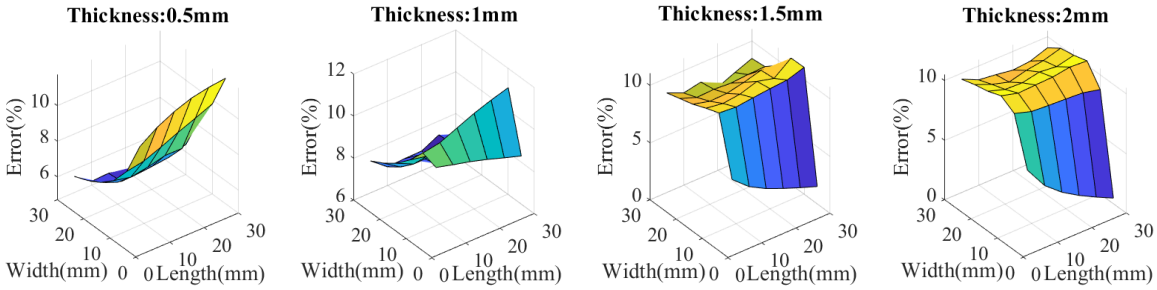


Figure 4.11: Parametric evaluation on errors of the partial inductance model on rectangular conductors with various dimensions.

In order to evaluate the model's accuracy when applied in half-bridge SSM power modules, numerical simulations are again conducted on five example cases, as shown in Table 4.2. Here, $d_{substrate}$ is 2 mm, d_{lead} is 0.1 mm. D is 5 mm. C1 equals B1. C2 equals B2. These five cases cover half-bridge SSM modules with different footprints

and conditions of symmetry. Results from the analytical model and numerical simulations are compared in Table 4.3. It can be seen that the maximum error of simulated cases is 12.1%, which indicates that the proposed model has a good accuracy.

Table 4.2: Dimension of cases for stray inductance model evaluation.

Dimensions	Case A	Case B	Case C	Case D	Case E
A1 (mm)	10	15	15	20	20
A2 (mm)	10	15	15	20	20
B1 (mm)	10	10	10	10	10
B2 (mm)	10	10	5	10	5

Table 4.3: Comparison between the analytical stray inductance model and numerical simulations.

Results	Case A	Case B	Case C	Case D	Case E
$L_s - FEA$ (nH)	28.3	25.2	18.8	23.2	17.2
$L_s - Model$ (nH)	26.2	24.9	16.6	24.2	15.8
Error	7.4%	1.2%	12.1%	4.3%	8.1%

4.3 Summary

This chapter proposed and validated analytical models for estimating power modules' thermal and electrical performances. These models are essentially suitable for half-bridge power modules with IMS-type packaging. First, a decoupled Fourier-based thermal model was proposed, which showed improved accuracy compared with the original Fourier-based thermal model when estimating T_j and ΔT_j, where errors are less than 4% and 11%, respectively. Then, to estimate L_s, a model combining the

partial inductance model and effective current conduction region analysis was proposed, whose errors were less than 12.1% on sample modules. Analytical models will be combined with optimization algorithms to design a prototype power module with SSM packaging, which will be introduced in the next chapter.

Chapter 5

Optimal Design of a Half-Bridge SiC Power Module with SSM Packaging

When designing power modules, there is always a trade-off between the thermal performance, power density, and L_s. Generally, a larger footprint could reduce the T_j, but also reduce the power density and increase the L_s. Therefore, co-optimization is needed to ensure balanced performances. Evolutionary algorithms have been widely applied in this field. Ji (Ji *et al.*, 2015) introduced an optimization process using the Non-Dominated-Sorting-Genetic-Algorithm II (NSGA II) for power module design, which shows promising performance in dealing with multi-objective optimizations. The same algorithm has been used in the development of the PowerSyth Software (Evans *et al.*, 2019) for the co-optimization of conventional planar power modules. Another practical and effective algorithm is the Particle Swarm Optimization (PSO) algorithm. Alavi (Alavi *et al.*, 2017) used PSO in optimizing the thermal design of a

power module. Similarly, Alizadeh (Alizadeh *et al.*, 2020) applied this algorithm in designing SiC converters.

5.1 Optimal Design Using PSO Algorithm

5.1.1 Problem Statement

The target is to design a SiC half-bridge module based on the SSM packaging scheme. The layout of the half-bridge module was defined in Figure 4.1. Dimensions of each layer and locations of dies are to be designed. However, as discussed above, trade-offs exist between improving the power density, minimizing the L_s of the module, and maintaining suitable T_j of dies. Therefore, design variables need to be optimized to achieve expected performances.

In this problem, thermal considerations are set as design constraints:

(1) T_j of two dies should be lower than 200^{o}C, due to the temperature durability of materials in the SSM packaging. This constraint is considered under certain power loss and cooling conditions. Based on simulating the half-bridge module as a phase leg in a three-phase inverter, it is found that each die will generate a 41 W power loss when the inverter operates at 800 Vdc/25 kVA. Details of the simulation are introduced in Appendix A. Regarding cooling boundary conditions, the effective convection coefficient at the bottom of the heatsink layer is set as 5000 W/m$^{2\cdot o}$C, which is based on assuming a pin-fin heatsink with an enlarged surface area. And the coolant temperature is 105^{o}C, according to the worst-case scenario in electrified vehicle applications, the hybrid-electric vehicles with shared coolant between the engine and power electronics.

(2) The ΔT_j between two dies should be less than 5^oC under the same thermal boundary conditions. This is to ensure that two dies to share a close lifetime expectation.

The minimization targets include the L_s and the volume (V_e) of the module. They are combined using defined weights (po_1 and po_2). Therefore, this optimization is reduced to a single objective problem. Furthermore, to scale these two criteria, reference values based on off-the-shelf power modules with similar ratings are used. Specifically, L_{s-ref} equals 10 nH, V_{e-ref} equals 1.9×10^{-5} m^3. Constraints and the cost function are shown in Equation (5.1.1) to (5.1.3). In this problem, F is to be minimized. po_1 and po_2 are set to be 0.3 and 0.7, respectively.

$$Constriants - 1 : max(T_{j1}, T_{j2}) < 200^oC \tag{5.1.1}$$

$$Constriants - 2 : |T_{j1} - T_{j2}| < 5^oC \tag{5.1.2}$$

$$CostFunction : F = po_1 \times \frac{V_e}{V_{e-ref}} + po_2 \times \frac{L_s}{L_{s-ref}} \tag{5.1.3}$$

5.1.2 Particle Swarm Optimization Algorithm

The Particle Swarm Optimization algorithm is a well-known evolutionary algorithm. First introduced in 1995 by Kennedy and Eberhart (Kennedy and Eberhart, 2002), it has been applied in seeking the global optimal of multi-variable problems, such as the thermal design of power electronics (Alavi *et al.*, 2017; Alizadeh *et al.*, 2020). PSO algorithm is constructed by simulating social interactions. A swarm of particles is

searching for the optimal position in the defined search space. The update of particle velocity considers the particle's self-inertial, the influence from the historical best position of that particle, and the influence from the current global best position, as shown in Equation (5.1.4). $v_i(it)$ means the velocity of the i_{th} particle at the it_{th} iteration. $x_{ibsest}\ (it)$ is the historical best position of this particle. $x_{global}\ (it)$ is the global best position. we is the inertia weight factor. c_1 is the self-learning factor. c_2 is the self-learning factor. The position update is obtained in Equation (5.1.5).

$$\begin{aligned} v_i(it+1) = we \times v_i(it) + c_1 r_1(x_{ibest}(it) - x_i(it)) \\ + c_2 r_2(x_{gbest}(it) - x_i(it)) \end{aligned} \tag{5.1.4}$$

$$x_i(t+1) = x_i(t) + v_i(t+1) \tag{5.1.5}$$

These parameters are critical for ensuring stabilized results and a proper convergence, which are the literature review (Trelea, 2003; Dai *et al.*, 2011) and parametric studies, as shown in Table 5.1. v_{i-max} is the max allowed velocity of particles, x_{max} and x_{min} are the boundaries of the searching space. N is the swarm population.

Table 5.1: PSO parameters

we	c_1	c_2	v_{i-max}	N
0.7298	1.4962	1.4962	0.02 $\times(x_{max} - x_{min})$	30

5.1.3 Optimized Design

Analytical models proposed in Chapter 4 are combined with the PSO algorithm to form a complete design methodology. The design process is illustrated in Figure 5.1. A half-bridge module with the SSM packaging scheme is designed using this method. There are two SiC MOSFET dies in this module, working as the upper switch and the lower switch in the half-bridge circuit. The die is CPM3-1200-0013A from Wolfspeed, whose specifications are listed in Table 5.2.

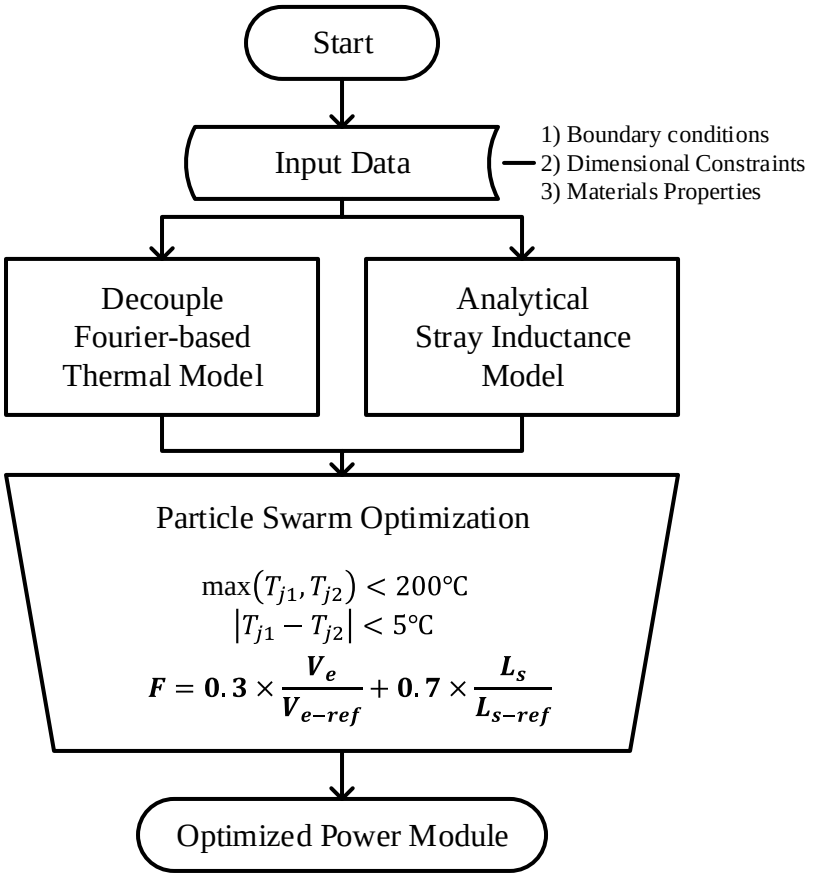


Figure 5.1: Design process.

Table 5.2: Specifications of CPM3-1200-0013A.

Parameter	Information
Semiconductor type	N-Channel Enhancement SiC MOSFET
Maximum V_{DS}	1200 V
Maximum I_{DS} at T_C=25^{o}C	149 A
$R_{DS(on)}$ at T_j=175^{o}C	21 mΩ
Die dimensions (L x W)	4.36 mm x 7.26 mm
Die thickness	180 μm ($\pm$10%)

In this design, some dimensions are defined symmetric for simplification purposes, as shown in Figure 4.1. Specifically, A1 equals A2. B1 equals C1, B2 equals C2. In addition, several dimensions are fixed due to limitations in manufacturing. Specifically, D is 5 mm, d_{lead} is 0.1 mm, d_{resin} is 0.2 mm, $d_{heatsink}$ is 2 mm. Additionally, the length and width of the DC terminals are 15 mm and (A1+A2-4) mm, respectively.

The search space and optimized results are summarized in Table 5.3. When calculating the performance of the optimized design in analytical models, they output a T_j of around 180^{o}C for both dies and a L_s of 16.17 nH. It is worth noting that off-the-shelf devices could have a lower inductance due to die paralleling. However, the target of this study is to validate of proposed methodologies. Thus, die paralleling is avoided to simplify the fabrication process.

The optimized design is shown in Figure 5.2. Its thermal-electrical performances will be evaluated by numerical simulations.

Table 5.3: Optimization variables.

Variables	A1/A2 (mm)	B1/C1 (mm)	B2/C2 (mm)	$d_{substrate}$ (mm)
Upper Limit	20	10	10	2
Lower Limit	15	7	5	0.2
Optimized	18	7	5	2

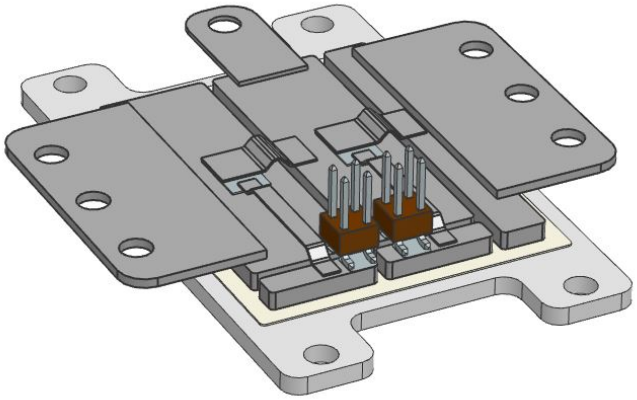


Figure 5.2: CAD model of the optimized SSM half-bridge module.

5.2 Simulation Evaluation

Performances of the optimized design are evaluated by numerical simulations. In order to obtain the L_s of the module, conductors of the main loop are simulated in Ansys Q3D, as shown in Figure 5.3.

Results of a frequency sweep from 10 kHz to 100 Mhz are shown in Figure 5.4, in which the L_s value of the typically concerning frequency of SiC MOSFET (60 MHz) can be extracted, which is 16.0 nH. Overall, L_s decreases with the frequency due to the skin effect of conductors. However, it is stabilized after reaching the mega-hertz

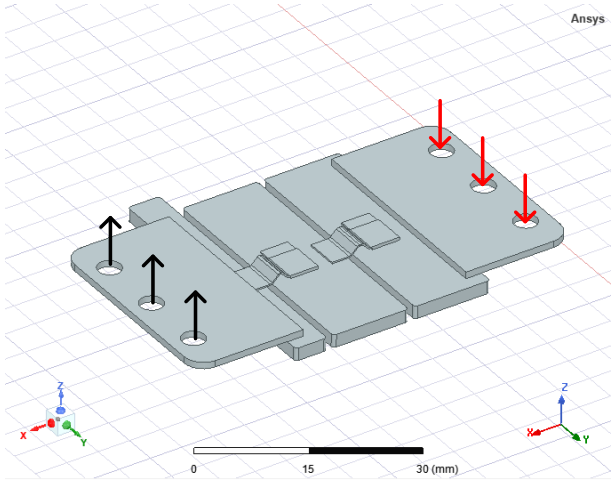


Figure 5.3: Q3D simulation of the main conductors of the optimized half-bridge module.

range. It is worth noting that the analytical L_s model also assumes a high-frequency application with a fully developed skin effect.

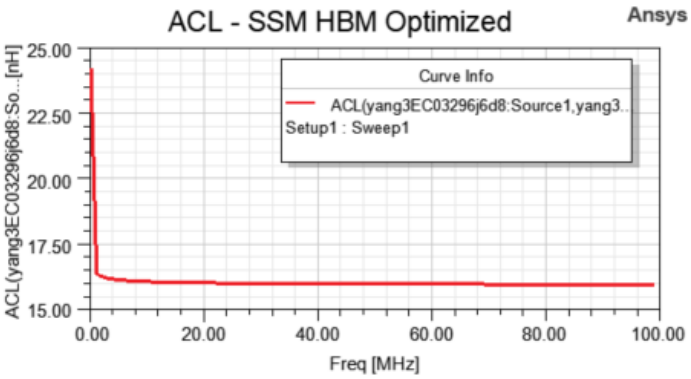
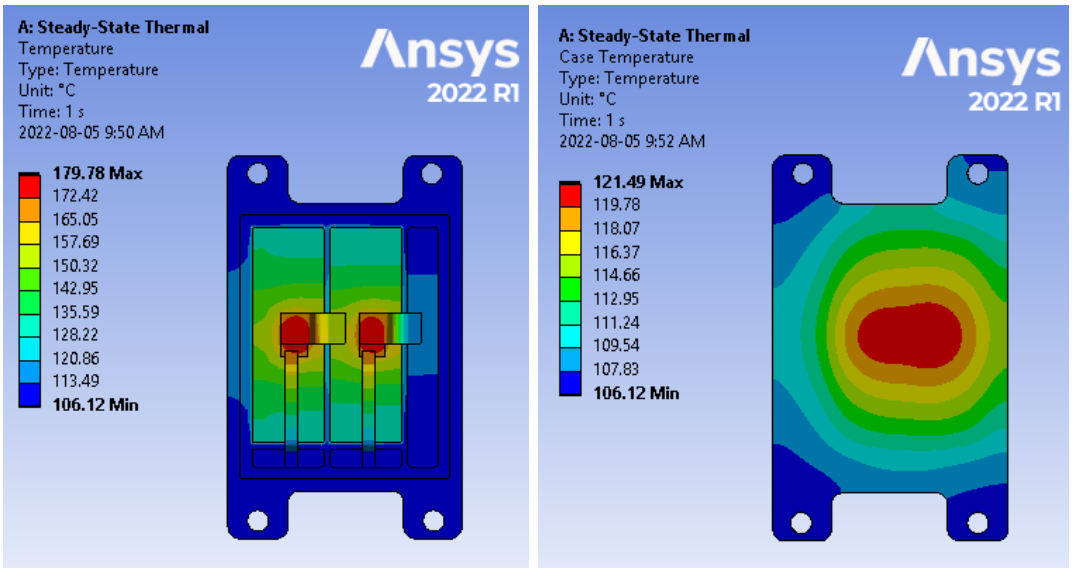


Figure 5.4: Frequency sweep of L_s of the designed module.

The module is also simulated using the Steady-State Thermal Unit in ANSYS Mechanical with the same power losses and cooling boundary conditions. The temperature profile is shown in Figure 5.5, from which T_j of dies can be measured. Here,

the influence of terminals is ignored.



(a) (b)

Figure 5.5: Thermal profile of the optimized half-bridge module: (a) top. (b) bottom.

The comparison between analytical estimations and numerical simulations is summarized in Table 5.4. The analytical models exhibit good accuracy with errors less than 4.6% and 8.3% for θ_j and L_s estimations, respectively. θ_j is the temperature-rise from the coolant to the junction.

Table 5.4: Comparison between the analytical model and the numerical simulations.

Results	θ_j (^{o}C) of the left die	θ_j (^{o}C) of the right die	L_s (nH) at 60 MHz
Analytical model	77.8	77.8	17.3
Numerical simulation	74.8	74.4	16.0
Error (%)	4.1	4.6	8.3

5.3 Summary

In this chapter, the process of optimizing a half-bridge power module based on the SSM packaging was presented. The design method included analytical thermal and stray inductance models and the PSO algorithm. With considerations of practical boundary conditions and dimension limits, an optimized prototype module was designed with SiC MOSFETs (CPM3-1200-0013A) as switches. T_j and L_s of the prototype module were verified by numerical simulations. Compared with calculated values from analytical models, simulation results showed an error of less than 5% for θ_j estimation and an error of 8.3% for L_s estimation, which validated again that analytical models have a decent accuracy.

Chapter 6

SiC Power Module Prototype Manufacturing

A half-bridge SSM module was designed in Chapter 5. In this chapter, the manufacturing process of the prototype module will be presented. The key step, nano-silver sintering, will be discussed in detail.

6.1 Pressure-less Nano-Silver Sintering Technology for Bonding SiC Dies on Molybdenum Substrate

As aforementioned, nano-silver sintering has obvious advantages over conventional Sn-Ag solders and was selected as the die-attachment method for the SSM packaging. Previous works have been done to investigate suitable processes to bond semiconductor dies with nano-silver sintering in power semiconductor devices. A simple

pressure-less profile was proposed by a renowned material supplier, NBE.Inc, in which the temperature is increased to 260 ^{o}C continuously with a speed of 5-7^{o}C/min and then held for 5-30 min (NBE, 2019). Other studies recommended different sintering temperatures between 160^{o}C to 350^{o}C (Atelge, 2016; Yan *et al.*, 2012). It was also demonstrated that applying pressure could improve the sintering quality but also complicate the process. Meanwhile, several studies have revealed that preheating the silver paste is essential to ensure complete evaporation of the organic matter in the paste, which could help reduce large pores in the final result. A double-stage preheating profile was introduced by Buttay (Buttay *et al.*, 2011), which resulted in a good sintering quality. The majority of these studies focused on applying nano-silver sintering in the conventional packaging with metallized ceramic substrates. However, studies on bonding SiC dies on Mo substrates via nano-silver sintering have not been reported. Therefore, investigating this process is necessary to validate the manufacturability of the proposed SSM packaging scheme.

6.1.1 Nano-Silver Sintering Mechanism

Nano-silver sintering is a solid-state powder metallurgy technology (Atelge, 2016). In the sintering process, the surface energy of materials is reduced by decreasing the surface area. There are three major stages during silver sintering. First, adjacent silver particles are joined with each other by surface atomic diffusion at the initial necking stage. Initial bonding lines are formed while large vacancies still exist in this stage. Then, the densification happens due to viscous flow or grain boundary diffusion. The bond lines extend, and small vacancies and pores start to appear. And finally, pores shrink until eliminated due to the same mechanism (Siow, 2019). A

dense silver bonding is then achieved. The mass transport path and stages are shown in Figure 6.1.

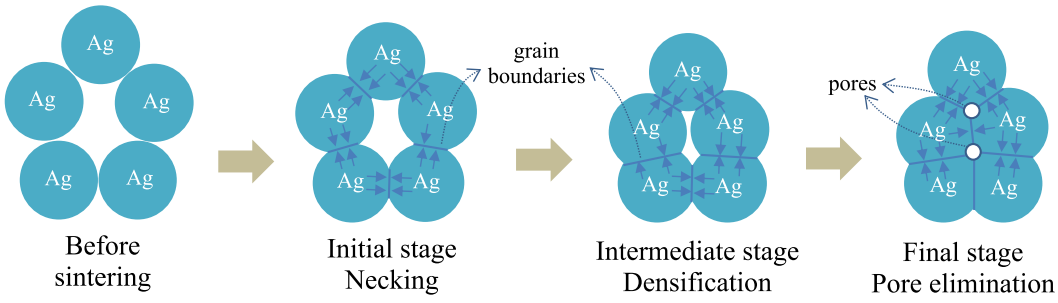


Figure 6.1: Mass transport path and sintering stages.

6.1.2 Critical Parameters and Considerations for the SSM Packaging

According to previous studies, there are several key parameters that affect the sintering quality, including particle size, surface condition, sintering temperature (T_s), time duration, and pressure. Due to the manufacturability issue explained above, this work will be only focused on pressure-less sintering. Early technologies of silver sintering used micro-scale silver particles (Schwarzbauer and Kuhnert, 1989) under a pressure of 9-40 MPa. With the recent development of nano-materials, it is found that a superior sintering quality can be achieved by using nano-scale ($\leq$100 nm) silver particles, even without applying pressure. This is because the total surface area and energy increase with the reduction of particle size. Therefore, the driving force of diffusion sintering is enhanced.

A higher T_s enhances the diffusivity. However, an excessive temperature could result in damage to semiconductor dies. Generally, a range of 160^{o}C to 350^{o}C (Atelge,

2016; Yan *et al.*, 2012) was recommended. A profile featured with a T_s of 275^{o}C was introduced by Knoerr (Knoerr *et al.*, 2010), which resulted in a relative density of 75%-85%. It was also proven that this process could lead to an extended lifetime compared with the SAC305 solder. The sintering time needs to be long enough to complete the diffusion. Studies indicated that improvement would be unnoticeable when the sintering time exceeds 30 minutes (Bai *et al.*, 2006; Wang *et al.*, 2007; Zou *et al.*, 2014). It is necessary to identify the minimum T_s that can achieve a satisfactory bonding quality. First, a lower T_s can reduce the manufacturing cost. More importantly, in the SSM packaging, the BT-resin insulator needs to be assembled before sintering. However, its glass transient temperature is around 265^{o}C (Hou *et al.*, 2019). A T_s high than that could affect its properties.

Silver sintering could exhibit selective results with different contact surfaces. The bare copper surface in the conventional packaging has been proven not ideal for silver sintering. This is because that Cu could get oxidized at the sintering temperature, and the formed CuO/Cu_2O structures will prevent the inter-diffusion between Ag and Cu and decrease the bonding strength, especially the power-like Cu_2O particles. Moreover, these oxidation structures will degrade the lifetime of the bonding. It is recommended in the literature that the contact material should have a similar lattice structure to Ag and is not prone to oxidation. Therefore, Ag and Au are the most commonly adopted options. In the SSM packaging, SiC dies are sintered on Mo substrates. However, Mo has a different lattice structure from Ag, and it could be oxidized at T_s. Therefore. it is necessary to study if bare Mo is compatible with nano-silver sintering. Lastly, the surface roughness (Ra) of contact surfaces could also affect the sintering quality. According to the literature, Ra of contact surfaces

should be noticeably larger than the silver particle size (8-12 nm) to allow silver particles to form mechanical interlocks with the contact surface (Wang *et al.*, 2018). However, they should also be much smaller than the thickness of the bond-line. In this study, contact surfaces were finely polished, and their Ra are within the suitable range. Thus, Ra is not considered in this study.

Last but not least, applying pressure during the sintering process could potentially improve the result, especially for bonding large-size dies. However, it requires sophisticated set-ups for alignment and pressure balance purposes, which will especially increase the process costs of packaging schemes that involve multiple sintering steps, like the SSM packaging. In fact, pressure-less sintering has been proven to have similar excellent performance for small-sized dies, and can greatly reduce process costs. In this study, the selected SiC MOSFET die has a small size. Meanwhile, the applied silver paste, nanoTach from NBE, is designed for pressure-less processes. In the following contents, key process parameters, including T_s and the surface finishing of Mo substrates, of pressure-less sintering bonding of SiC MOSFET dies on Mo substrates will be studied.

6.1.3 Experiment

According to the discussion above, this paper will focus on studying the effect of the T_s and surface finishing of Mo. A temperature profile is proposed in Figure 6.2. Samples need to be pre-heated first to evaporate organic matter in the nano-silver paste, including solvent, thinner, binder, and surfactant. A two-stage (50^oC and 100^oC) pre-heating temperature profile was introduced by Wang (Wang *et al.*, 2007), where the thermo-gravimetric-analysis (TGA) showed that the two-stage pre-heating

could slow down the evaporation process, which could reduce the influence on silver-particle's densification from outgassing. It was also reported in Yoon's TGA work that the evaporation completes at around 125^{o}C (Yoon *et al.*, 2018). Therefore, in this study, a two-stage pre-heating profile is applied, where samples are held at 50^{o}C and 125^{o}C. After pre-heating stages, samples are sintered at the T_s for 30 minutes. According to Atelge's survey (Atelge, 2016), the increase in sintering quality with sintering time becomes insignificant when the sintering time is longer than 30 minutes. Different T_s will be studied. The entire process is taken place in the air since oxygen is necessary for the evaporation of organics in the nano-silver paste.

As shown in Table 6.1, four cases are compared in this study, which features different T_s and surface conditions of Mo substrates. Considering the reference profile (Knoerr *et al.*, 2010) and the glass-transition temperature of the BT resin, T_s varies from 240^{o}C to 275^{o}C. Except in case D, other cases use Mo substrates with Ni(0.8μm)/Au(0.1μm) coating. These coatings are achieved by the e-beam evaporation technique.

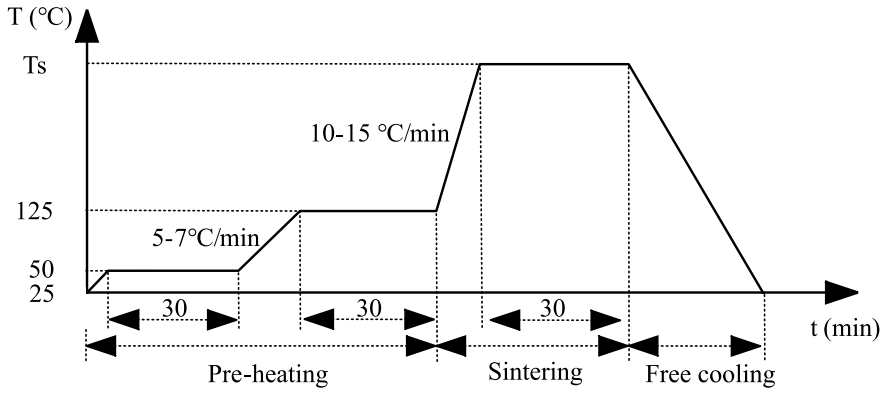


Figure 6.2: Sintering profile.

Dummy SiC dies with a size of 5 mm×5 mm×0.18 mm are used in this study.

Table 6.1: Sintering trials.

Cases	T_s (^{o}C)	Surface condition of Mo
A	240	Ni/Au coated
B	250	Ni/Au coated
C	275	Ni/Au coated
D	275	Bare Mo

Their surfaces are finished with Ni(0.6 μm)/Pd(0.2 μm)/Au(0.1 μm). The nano-silver paste is the nanoTach-X from NBE (NBE, 2019), in which nano-silver particles with sizes of 8-12 nm are mixed with organic matter to form the paste of 82 wt.%. Mo substrates are cuboid samples with a size of 15 mm×15 mm×3 mm. Mo substrates are manufactured by the supplier, Standford Advanced Materials. . All samples are cleaned with Acetone, Methanol, and deionized water before sintering. Figure 6.3 shows the nano-silver paste and samples on the heating station.

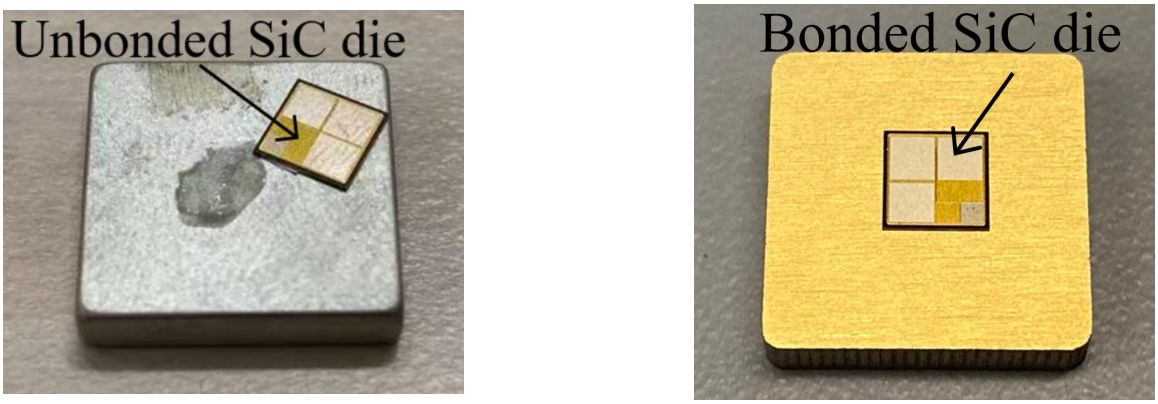
(a) (b)

Figure 6.3: Material and set-ups: (a) nanoTach-X paste from NBE.Inc. (b) samples on the heating station.

Generally, a thinner thickness of the bond-line leads to better thermal and electrical conductivity. However, it should also be thick enough to mitigate the surface roughness. In this study, the nano-silver pastes are applied on Mo substrates using stencil printing. The pre-sintered thickness is 50 μm. According to the supplier (NBE), it will result in an end thickness of 20-30 μm.

6.1.4 Analysis of Sintering Quality

Two sintered samples are shown in Figure 6.4. In case D, the SiC die was not securely attached to the bare Mo substrate. The bare Mo surface was also partially oxidized. Therefore, a bare Mo surface is not suitable for nano-silver sintering bonding. On the contrary, all other cases (A, B, and C) achieved proper bonding. Thus, applying Ni/Au coating makes Mo compatible with nano-silver sintering.



(a) (b)

Figure 6.4: Sintered samples: (a) case D with bare Mo. (b) case B with Ni/Au coated Mo.

Successfully bonded samples were then prepared for microscopy examination. Figure 6.5 shows the resin-mounted samples for scanning electron microscope (SEM) and

energy-dispersive X-ray spectroscopy (EDS) analysis. First, samples were cut by low-speed sawing to expose the cross-section. Then, samples are polished carefully to remove scratches caused by the sample preparation process.

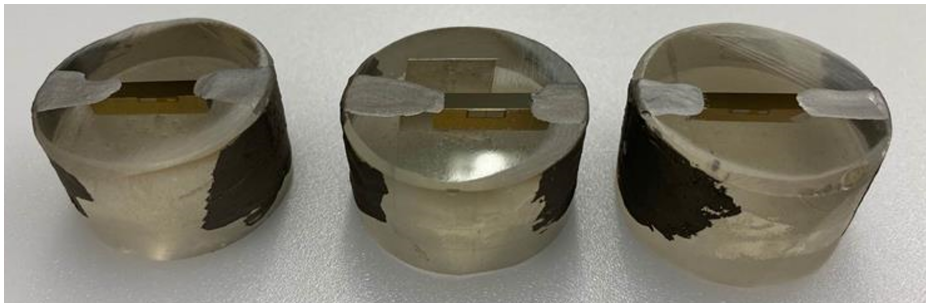


Figure 6.5: Cross section samples for SEM and EDS.

The sintering quality is described using a parameter called relative density. Relative density refers to the ratio of the volume occupied by silver to the total volume. In cross sections, it can be represented by the ratios of areas. Relative density is the key parameter in evaluating the quality of sintered nano-silver. A higher relative density means fewer pores and vacancies, therefore, less opportunity for cracking initiation and propagation. Meanwhile, it also guarantees better thermal and electrical conductivities. The manufacturer (NBE) indicates that this material could achieve a good relative density, higher than 70%. In literature, a relative density of 80% marks an excellent overall performance, especially an enhanced reliability (Knoerr *et al.*, 2010; Yang *et al.*, 2021; Yu *et al.*, 2009). Therefore, in this paper, 80% is also viewed as the baseline for satisfactory bonding.

SEM images of samples were obtained in the JEOL JSM-7000F machine, as shown in Figure 6.6. From these figures, the relative density of different spots can be calculated. Results are summarized in Figure 6.7. The relative distance refers to the ratio of the distance from a point to the left edge and the total length of the bonding

line. Clearly, the left and right edges have lower relative density. This is likely because the mismatched thermal-expansion between materials causes uneven internal pressure during the pressure-less sintering process. According to our previous study (Yang *et al.*, 2021), when external pressure is applied during the sintering process, this uneven distribution of relative density is less noticeable, which indicates the advantage of pressure-based sintering. As aforementioned, a higher T_s could enhance the diffusion bonding between particles. Therefore, it will also mitigate the uneven distribution of relative density, which is verified in Case B and Case C in Figure 6.7. It is essential to find the suitable T_s for pressure-less sintering, which could result in a satisfactory bond-line.

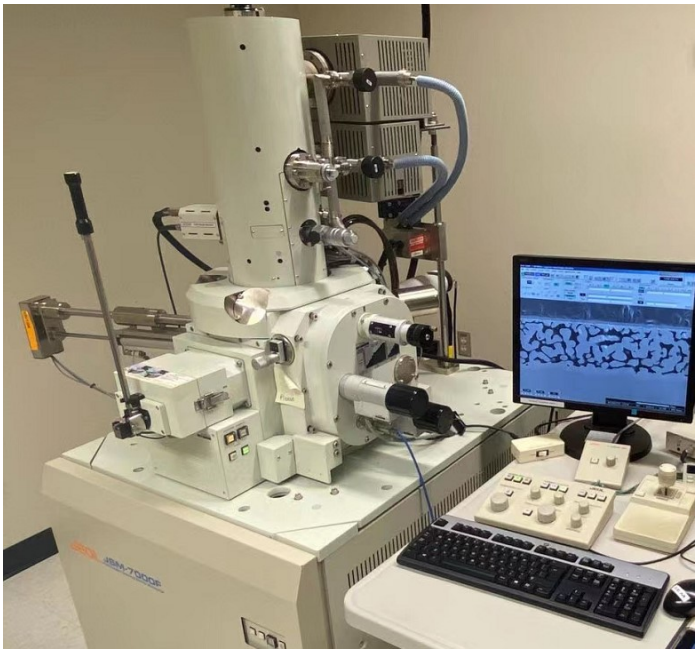


Figure 6.6: SEM set-up:JOEL JSM-7000F.

Peak relative density values of all three cases are higher than 95%. And the average relative densities are all above 80%. Also, the majority of bonding lines

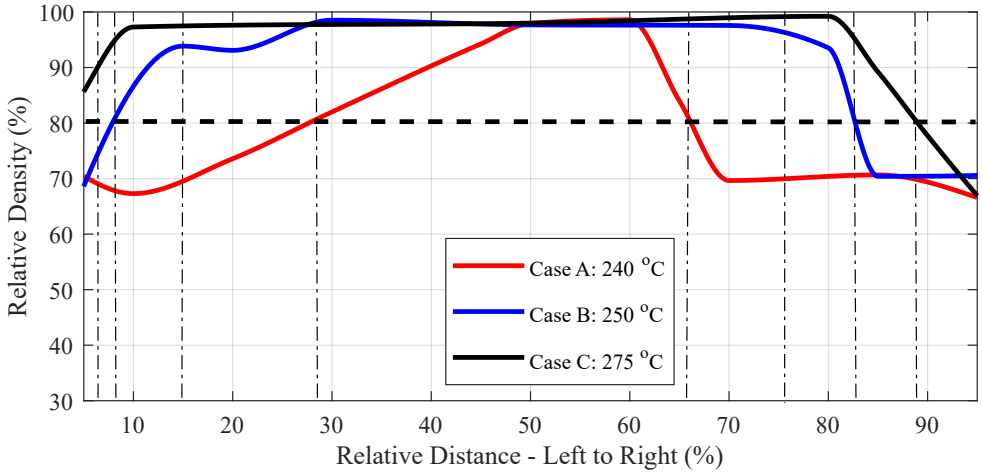


Figure 6.7: Relative density distribution.

are denser than 70% except for some minor regions in case A. This indicates that all three cases result in an acceptable bonding quality. However, due to the uneven distribution discussion above, case A has a large portion of length whose relative density is lower than 80%. Therefore, the reliability of this case can be remarkably worse than the other two cases. Case B and case C exhibit a similar distribution. Thus, their bonding qualities are close.

For the SSM packaging, T_s is expected to be as low as possible to avoid damaging the BT resin. Therefore, case B with a T_s of 250^{o}C is more suitable. It has an average relative density of 91.36%, and 75% of the total length has a relative density higher than 80%. The bonding quality of this case is better than benchmarks from the literature (Knoerr *et al.*, 2010; Yu *et al.*, 2009).

Microstructures of case B at different relative distances are shown in Figure 6.8. The bond-line thickness is between 20-30 μm, which agrees with the supplier's assumption. The left side is slightly thinner than the right side due to imperfect manual placement. The variation of relative density across the total length can be clearly seen.

The left and right edges contain larger pores and vacancies, while the middle region is denser, which agrees with the trend in Figure 6.7. The transition regions are located at around 10% and 85% relative distance, where vacancies start to be eliminated. The maximum dimension of vacancies is larger than 10 μm at the edges. At transition regions, it shrinks to around 5 μm. At the middle region, only a few small pores with a maximum dimension of less than 1 μm exist. As discussed above, this is likely due to the uneven internal pressure distribution at edges, especially during pressure-less sintering, which lacks external driven force. Another notable phenomenon is that vacancies on the lower side of the bonding-line are eliminated before those on the upper side, which can be seen at figures of 20% and 80% relative distances. This is because samples are only heated from the bottom.

Microstructures of contact-lines are elaborated in Figure 6.9. A three-layer stack-up of Ni-Pd-Au is seen at the contact-line between the SiC chip and the silver. The total thickness is measured as 0.952 μm, which is close to the values announced in the datasheet of the SiC chip, 0.9 μm. At the contact-line between the Ag layer and the Mo substrate, a two-layer stack-up of Ni-Au can be found. The total thickness is measured as 0.889 μm, close to the designed value during the e-beam evaporation, 0.9 μm. These two contact-lines are further analyzed by EDS.

EDS line-scan analysis detects the elemental composition at contact-lines, as illustrated in Figure 6.10. The desired inter-diffusion between silver and the contact surfaces is observed. Specifically, at the contact line between the SiC die and the Ag layer, mixed regions of Ag-Au and Ag-Au-Pd are formed. Meanwhile, at the contact line between the Mo layer and the Ag layer, there is a well-mixed region of Ag-Au. Also, The diffusion barrier effect of Ni and Pd is effective, since there is no

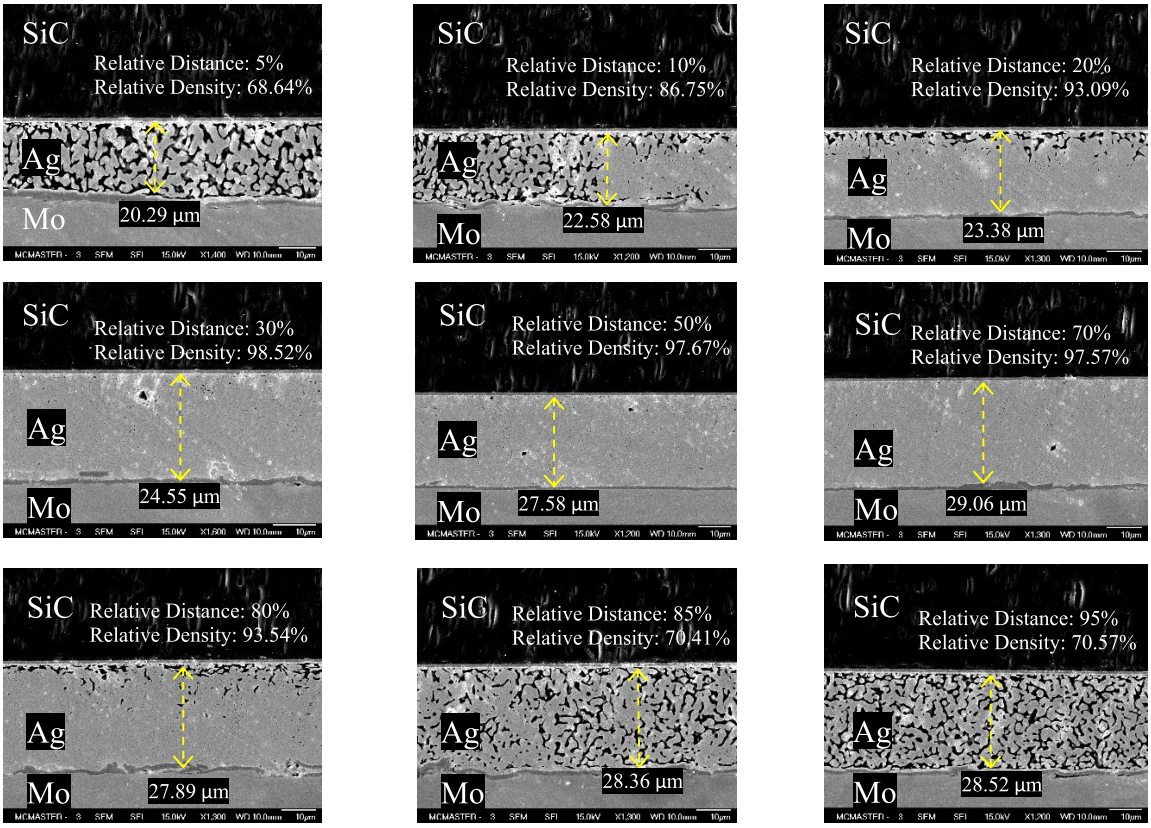


Figure 6.8: Bond-line microstructure of case B.

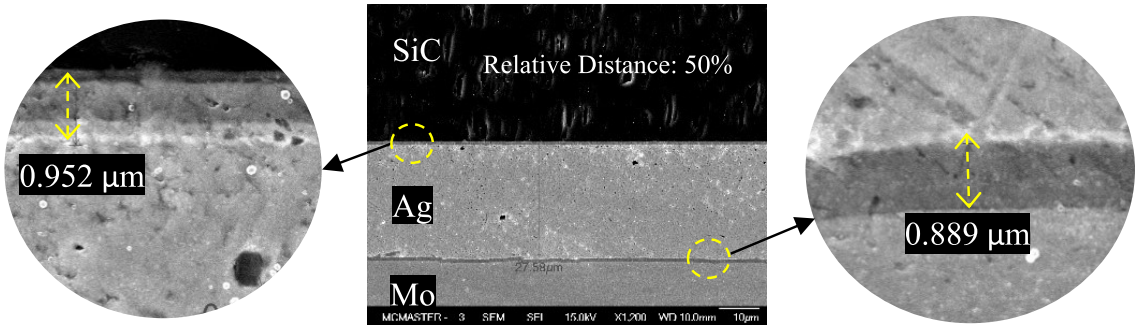
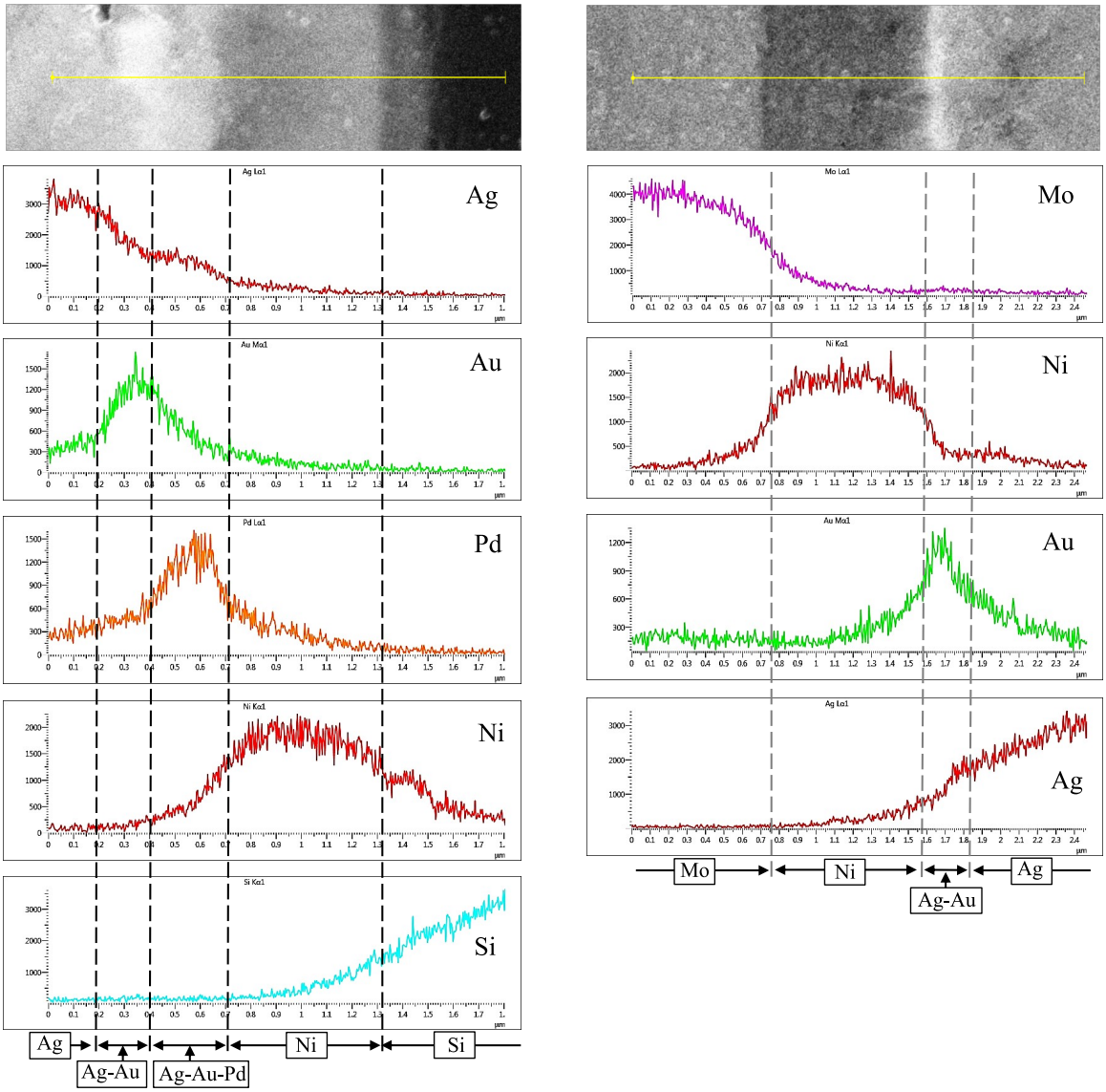


Figure 6.9: Contact-line microstructure of case B.

Ag penetrating into SiC or Mo. This analysis demonstrates that proper inter-metallic joints were formed in case B. Therefore, Case B (T_s=250^{o}C) is validated as the most suitable process and will be used in the assembly of the prototype module.



(a) (b)

Figure 6.10: Contact line microstructure of case B: (a) contact line between the silver bond-line and the SiC chip. (b) contact line between Mo and the silver bond line.

6.2 Assembly of the Prototype Half-Bridge Power Module

A prototype half-bridge power module based on the SSM packaging was designed in Chapter 5. In this section, the complete assembly process of the prototype module will be introduced, and each manufacturing step will be elaborated in detail. In general, there are four main parts, including the preparation of SiC dies (re-metallization of pads), the vacuum curing of the BT resin, the die attaching, and the terminal assembly. It should be noted that materials (SiC dies, Mo pieces, BT resin pieces, and nano-silver paste) are prepared beforehand. Specifically, Mo pieces are custom manufactured by the material supplier, Stanford Advanced Materials.

Original gate and source pads on SiC MOSFET dies (CPM3-1200-0013A) are made with Al, which is designed for Al wire bonding. In the SSM packaging, top interconnections are silver-sintered Mo leads. Thus, the first step is to re-metallize gate and source pads, making them compatible with silver sintering bonding. As aforementioned, contact surfaces should be coated with Ni(0.05μm)/Au(0.1μm). Meanwhile, the clearance distance between the new gate and source pads should be enlarged to make it feasible to apply silver paste.

The re-metallization process is illustrated in Figure 6.11. In Step 1, a 0.25 μm SiO_2 layer was coated uniformly on top of the original dies by Plasma Enhanced Chemical Vapor Deposition (PE-CVD). This layer covers the original gate and source pads, providing insulation against new metal layers to be coated. In Step 2, a layer of photo-resist was coated on top of SiO_2. Then, in Step 3, areas for new pads were exposed by photolithography using dedicated masks. After removing the exposed

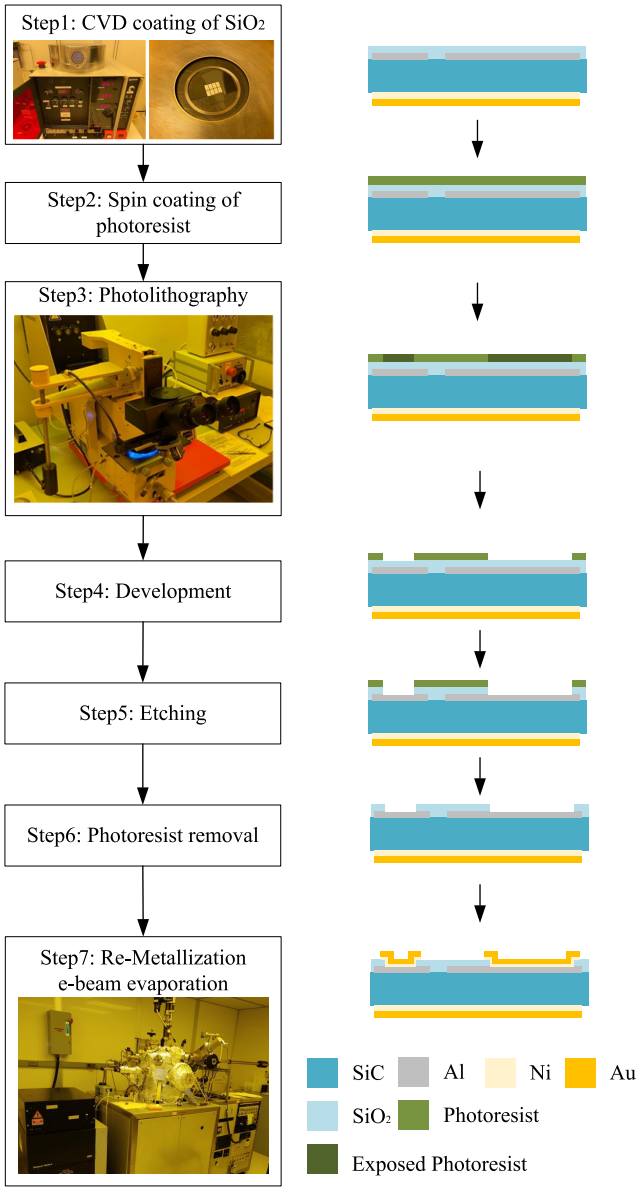
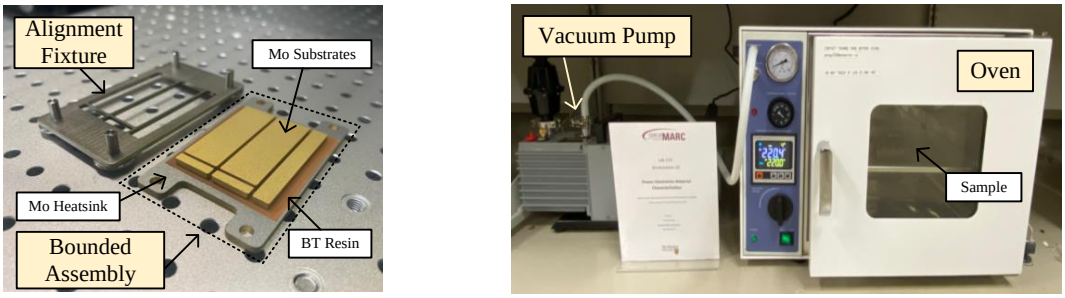


Figure 6.11: Re-metallization process of SiC dies.

photo-resist using the development solution in Step 4, the SiO_2 within the exposed area was then etched off by Hydrofluoric acid solution in Step 5, which made the original Al metal layer accessible again. Then, tunnels to connect the original pads

and new pads are formed. Finally, after removing the rest of the photo-resist in Step 6, new Ni/Au layers were metalized on exposed areas by UHV-Electron-Beam Evaporation. Details of this process are introduced in Appendix B.

Then, the next step was forming the Mo-based IMS structure, where substrate pieces were bonded with the heatsink by vacuum curing of the BT-resin prepreg. The BT prepreg is HL832NSF from Mitsubishi Chemical (MGC, 2022). A dedicated alignment fixture was applied to position each substrate piece precisely, as can be seen in Figure 6.12a. The curing profile is recommended by the supplier, as shown in Figure 6.13. The curing process was achieved by holding the materials at 220 ^{o}C for more than one hour. Meanwhile, the vacuum environment enhances the flow of resin, helping the formation of micro-mechanical joints between the resin and the metal surfaces. This process was taken place in a vacuum oven, as shown in Figure 6.12b.



(a) (b)

Figure 6.12: Set-ups for assembling the substrate-resin-heatsink sandwiched structure (a) alignment fixture and assembled parts. (b) vacuum oven.

After that, SiC dies were attached to Mo substrates by nano-silver sintering. First, the nano-silver paste (nanoTach-X from NBE (NBE, 2019)) was screen-printed on the substrate with stencils. Components with printed silver paste were illustrated

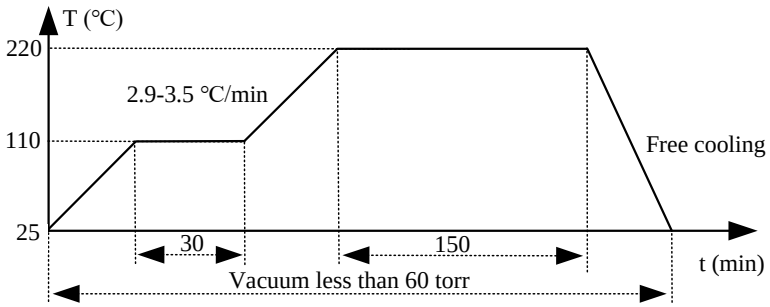
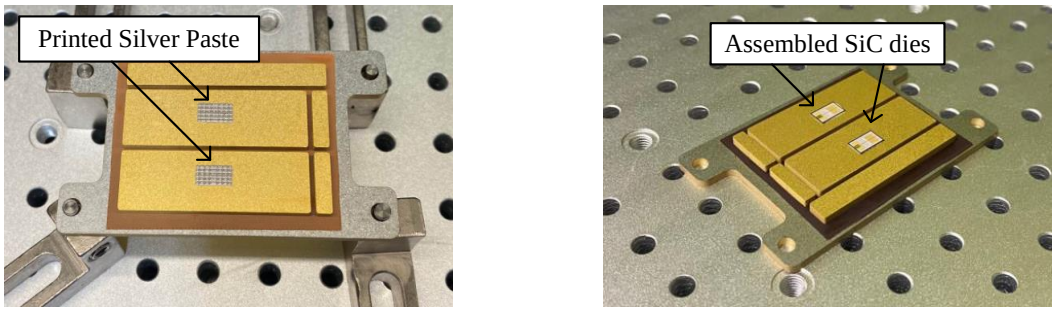


Figure 6.13: Curing profile of BT resin.

in Figure 6.14a. Then, the SiC dies were placed on pastes and aligned with dedicated fixtures. The sintering process follows case B (T_s=250^{o}C) introduced in Chapter 6. Assembled SiC dies on Mo substrates are shown in Figure 6.14b.



(a) (b)

Figure 6.14: Die attachment process: (a) printed nano-silver paste. (b) assembled SiC dies.

A similar approach is implemented in assembling Mo leads and terminals. It is worth noting that all Mo parts are also coated with Ni(0.8 μm)/Au(0.1 μm).

The entire assembly process is summarized in Figure 6.15.

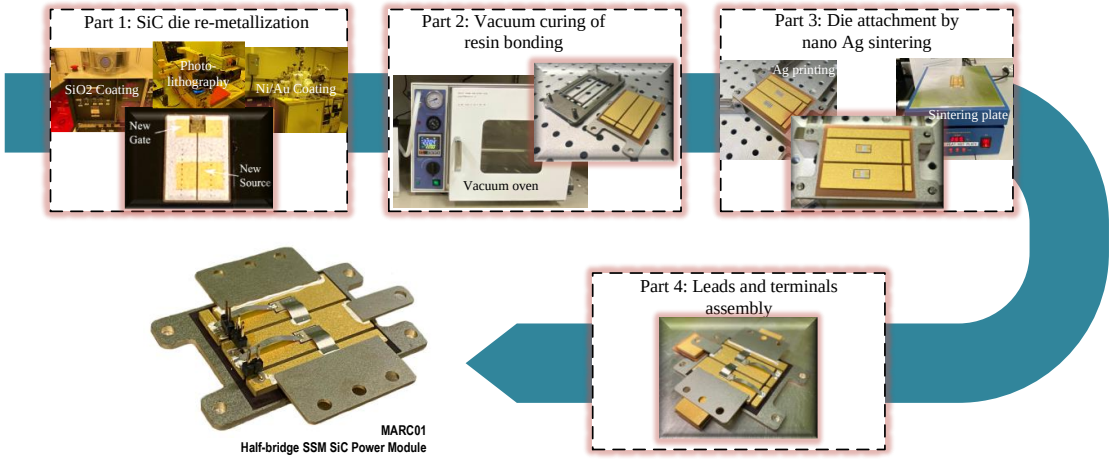


Figure 6.15: Fabrication process of the prototype module.

6.3 Summary

In this chapter, a prototype power module with the proposed SSM packaging was fabricated. The complete process was elaborated. And the key step, nano-silver sintering between Mo parts and SiC dies, was studied in detail.

The fabrication process includes four parts: the re-metalization of the gate and source pads on SiC dies, the assembly of Mo-based IMS by vacuum curing of the BT resin, die attaching, and the formation of interconnections, where the last two parts were achieved by nano-silver sintering. Specifically, nano-silver sintering with various Mo surface conditions and T_s were investigated in detail. By analyzing micro-structures and the material composition of samples, a pressure-less sintering profile was recommended, where Mo surfaces are coated with Ni(0.8 μm)/Au(0.1 μm), and T_s is 250^{o}C.

Chapter 7

Thermal-Electrical Characterization

This chapter will introduce experimental characterizations of the prototype power module, including the double pulse test and the thermal impedance characterization. These tests evaluate the accuracy of analytical models proposed in Chapter 4 and validate the fabrication process introduced in Chapter 6.

7.1 Double Pulse Test

The double pulse test is a standard method to characterize the switching behaviors of power modules. The schematic of testing a half-bridge module is shown in Figure 7.1, where the low-side MOSFET is the active device under test. During the test, the high-side MOSFET is kept off by clamping its gate-source voltage (V_{GS}) at -4V, which is according to the datasheet. As for the V_{GS} of the low-side MOSFET, two -4V to 15V square-wave pulse signals are generated to turn it on and off. In this

circuit, the DC-link capacitor works as the stabilized voltage source, which has its own equivalent series resistance ($ESR - C$) and stray inductance (L_{s-Cap}). Moreover, all components are connected through a PCB. Therefore, the ESR and stray inductance of the PCB are included, which are $ESR - PCB$ and L_{s-PCB} in the schematic. Additionally, an external gate resistance (R_{G-EXT}) is added to the gate-source loop of the low-side MOSFET to control its switching speed. The $HS - L_s$ and $LS - L_s$ are stray inductance values of the high-side and low-side of the power module, while the $HS - ESR$ and $LS - ESR$ are equivalent series resistance values. Finally, L_{Load} is the load inductor.

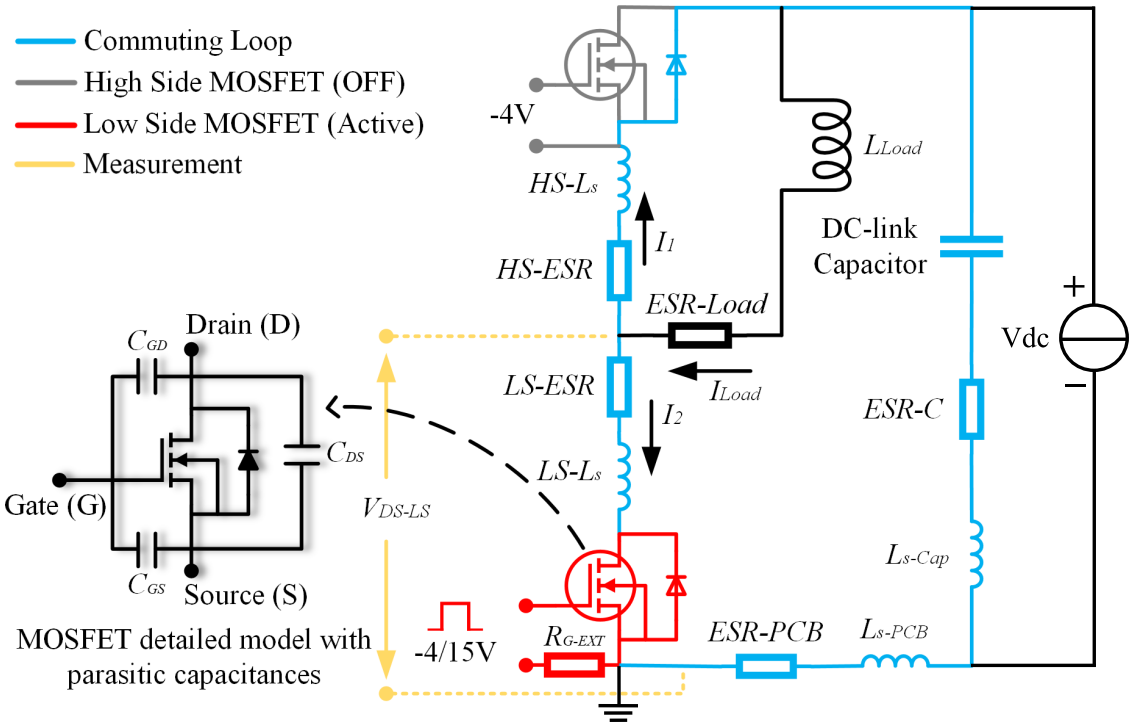


Figure 7.1: Double pulse test schematic.

Ideal waveforms of the low-side MOSFET are shown in Figure 7.2. During the on-time of the first pulse, the load current (I_{load}) increases until it reaches the desired

value, and the turn-off transient under this current will be captured at the falling edge of the first pulse. I_{load} keeps constant during the gap between two pulses due to the existence of the load inductor. Similarly, at the rising edge of the second pulse, the turn-on transient will be measured.

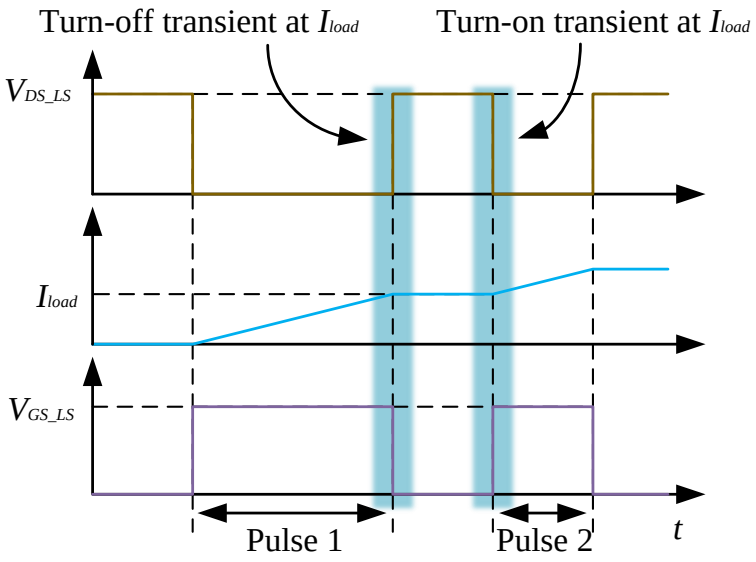


Figure 7.2: Ideal waveforms of double pulse test.

The turn-off transient is useful for characterizing parasitic parameters in the circuit. According to the schematic shown in Figure 7.1, when the low-side MOSFET is turning off, I_2 will decrease, and I_1 will increase to provide a path for the I_{Load} to stay a constant. Therefore, a current commutation loop is formed. After turning-off, the V_{DS} of the low side MOSFET will oscillate, whose frequency (f_o) is determined by the output capacitance of the MOSFET (C_{oss}) and the total stray inductance of the commuting loop (L_{s-loop}), as explained in Equation (7.1.1) and (7.1.2). C_{GD} and C_{DS} are parasitic capacitance of the MOSFET as shown in Figure 7.1. Equation

(7.1.1) is commonly used to calculate L_{s-loop}.

$$f_o = \frac{1}{2 \times \pi \times \sqrt{C_{oss} \times L_{s-loop}}} \tag{7.1.1}$$

$$C_{oss} = C_{GD} + C_{DS} \tag{7.1.2}$$

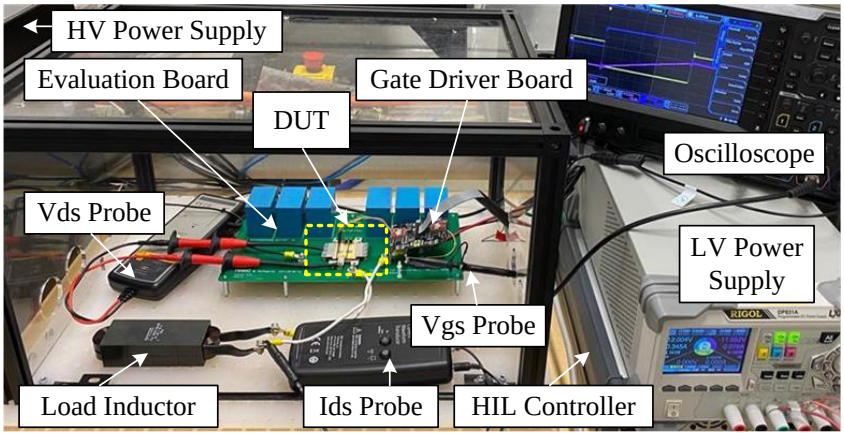


Figure 7.3: Double pulse test set-up.

The experimental set-up is illustrated in Figure 7.3. Figure 7.4 shows experimentally measured V_{DS-LS} during turn-off of the low side MOSFET at a DC voltage of 300 V and a I_{Load} of 60 A.

The identical circuit is also simulated in the PSIM software. In the simulation, the DC-link capacitor is a bank of six single units (B32778G8606 from TDK) connected in parallel. $ESR-C$ and L_{s-Cap} are cited from the datasheet, which are 0.85 mOhm and 2.5 nH, respectively. The stray inductance value of the test circuit is obtained by simulations in ANSYS Q3D. The CAD model used for the simulation is shown in Figure 7.5, where the PCB, the DC-link capacitor, and the power module are

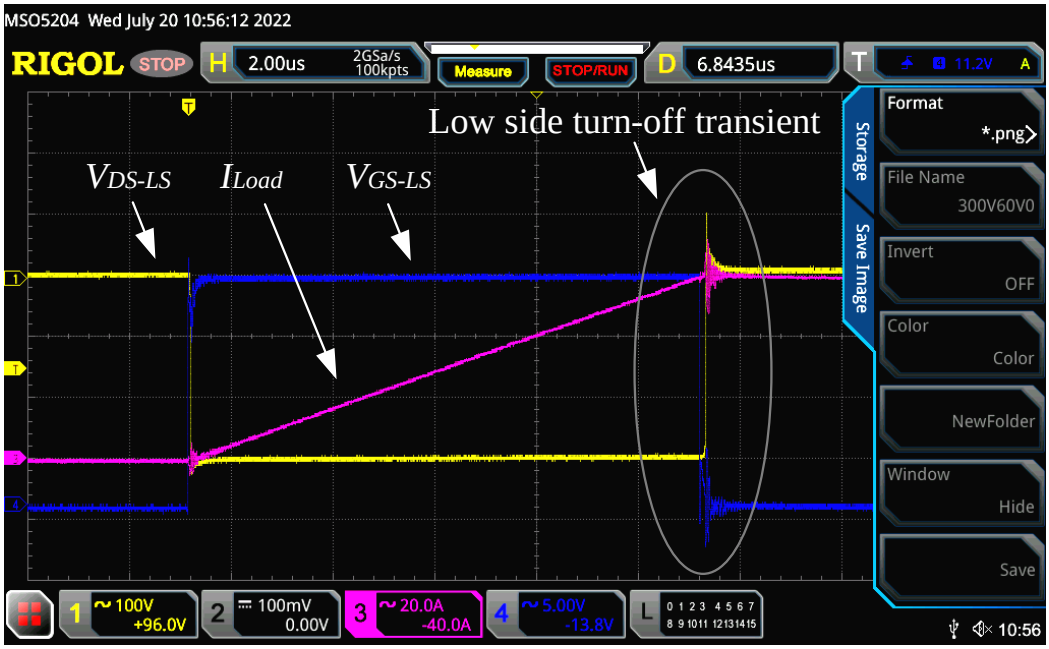
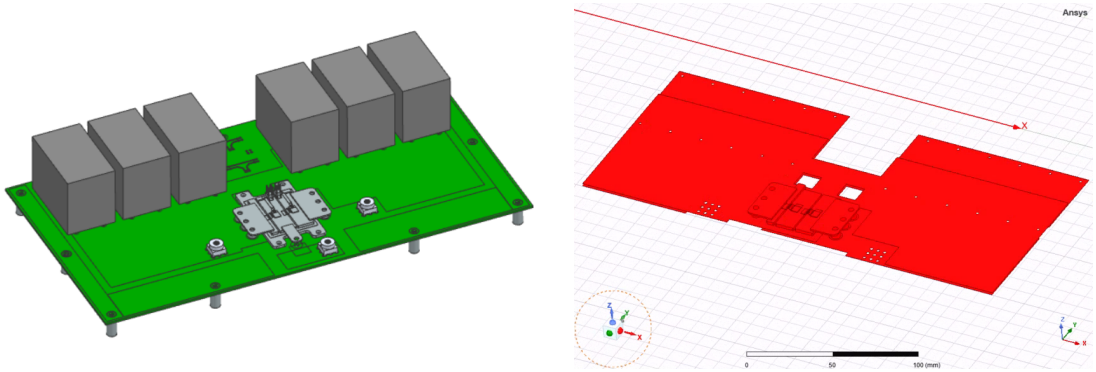


Figure 7.4: Low side MOSFET waveform during turn-off at 300 Vdc/60 A.

included. The L_{s-PCB} is 7.15 nH. $HS - L_s$ and $LS - L_s$ equal to half of the total L_s of the power modules estimated by the analytical model. It is worth mentioning that the mutual-inductance (also obtained in the ANSYS Q3D) between conductors are also considered and subtracted from self-inductances. In this work, an indirect validation method is applied to evaluate the accuracy of the proposed inductance model. Assuming inductance values obtained from Q3D simulations and the datasheet are trust-worthy, then the accuracy of the power module's inductance can be evaluate by comparing waveforms form both PSIM simulations and experiments, which could then prove the accuracy of the analytical inductance model proposed in this study.

Figure 7.6 compares the V_{DS} curves during the turn-off of the low-side MOSFET. It can be seen that the simulation result matches with the measured waveform.



(a) (b)

Figure 7.5: Double pulse test models: (a) 3D CAD of the double pulse set-up. (b) 3D CAD of conduction traces in ANSYS Q3D.

Results are further summarized in Table 7.1. And L_{s-loop} from experiments are calculated using Equation (7.1.1).

According to the datasheet, the C_{oss} of the MOSFET equals 383 pF at 300 V. Using Equation (7.1.1), the experimentally characterized L_{s-loop} can be obtained. It can be seen in Table 7.1 and Figure 7.6 that the inductance obtained from Q3D simulation matches with the experimental results well. In previous sections, the analytical L_s model has been proven accurate compared with the Q3D simulation. Thus, it is reasonable to conclude that the analytical L_s model has decent accuracy.

Table 7.1: Comparison of the switching characteristics.

Results	f_o (MHz)	L_{s-loop} (nH)
Experiment	55.1	21.8 (Calculated)
Simulation	54.8	21.9 (Q3D)
Error (%)	0.5	0.4

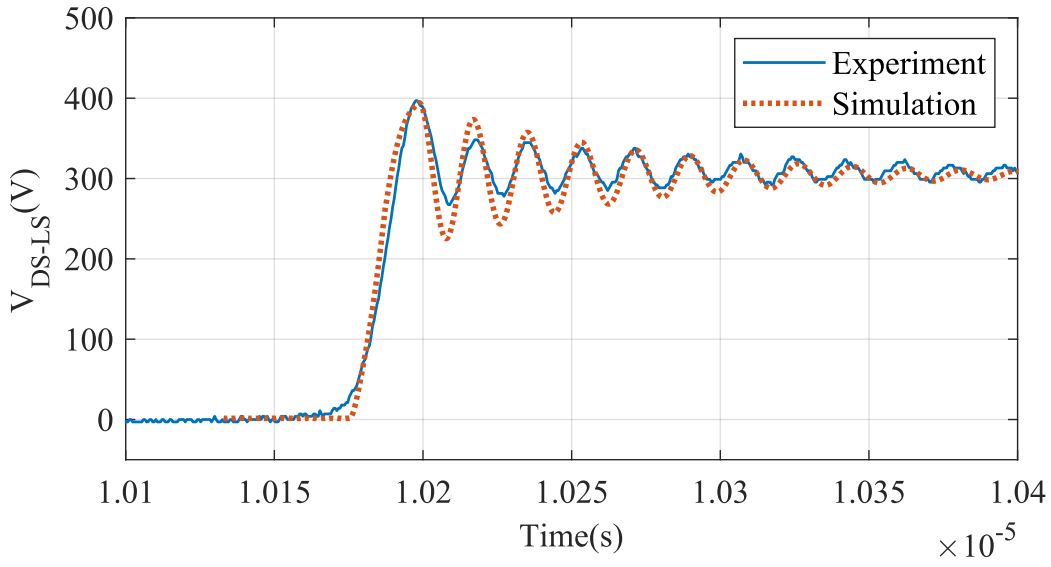


Figure 7.6: Comparison of V_{DS-LS} during turn-off at 300 Vdc/60 A.

7.2 Thermal Impedance Characterization

In order to experimentally validate the thermal design and evaluate the manufacturing quality of the prototype module, the junction-to-case thermal resistance ($R_{th(j-c)}$) is measured. $R_{th(j-c)}$ is the most important parameter to describe heat conduction within a power module. It is expressed in the form of the difference between the junction temperature (T_j) and the case temperature (T_b) over the power loss of the heat source (P_{die}), as shown in Equation (7.2.1). In the SSM packaging, the maximum temperature at dies is considered as T_j, while T_b refers to the temperature at the closest point to the center of the corresponding die, at the bottom surface of the heatsink, as illustrated in Figure 7.7. For a power module, the largest $R_{th(j-c)}$ of all dies is viewed as the per-die value of the module.

$$R_{th(j-c)} = \frac{T_j - T_b}{P_{die}} \tag{7.2.1}$$

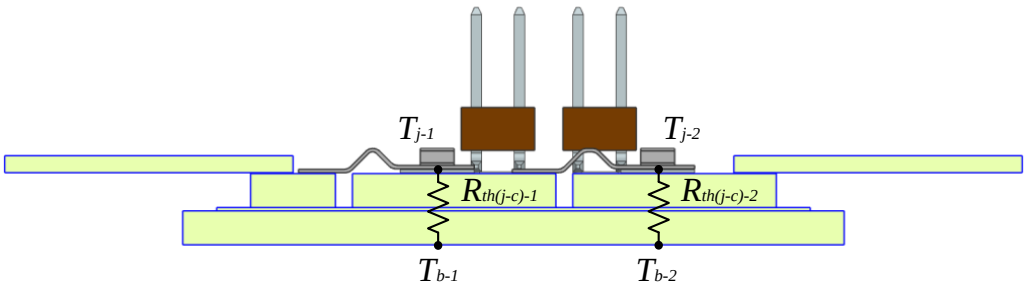


Figure 7.7: Measurement points for calculating the $R_{th(j-c)}$.

In the thermal characterization of power modules, one main challenge is the T_j measurement. As aforementioned, T_j refers to the maximum temperature of the semiconductor die. It is not possible to capture it with direct measurement tools, such as thermal-couples. As for indirect measurement tools, like infrared thermal-meter, it is also hard to get a good resolution due to the small size of the die. Meanwhile, this method lacks the capability to reveal heat transfer behaviors of different layers inside power modules.

Indirect measurement of T_j can be accurately achieved by correlating T_j with a temperature-sensitive parameter (TSP). TSP refers to electrical parameters of semiconductors that have a clear relationship with temperature and can be easily measured. These relationships can be calibrated using the thermal equilibrium method in advance. During the calibration, an external heater will heat up the entire system to a set temperature, including the coolant, the coldplate, and the power module. Then, the TSP value at this specific temperature will be measured. After running a series of measurements, the relationship can be determined through curve-fitting of data points. For SiC MOSFET, a commonly used TSP is the forward voltage of the

body-diode (V_D). When V_{GS} of the MOSFET is clamped to 0 V, V_D can be measured through conducting a small sensing current from source to drain through the body diode. This method can avoid instabilities in gating control of SiC MOSFETs and has good linearity. The T_j to V_D relationship of the prototype SSM power module is calibrated using the method, as depicted in Equation (7.2.2). The calibration equipment is the SIEMENS Power T3ster (PWT-1500A).

$$T_j = -348.2042 \times V_D + 974.1909 \tag{7.2.2}$$

There are several ways to characterize $R_{th(j-c)}$. The conventional method is to measure T_b and T_j during the thermal steady-state of power modules, then, use Equation (7.2.1) to calculate $R_{th(j-c)}$. However, apart from difficulties in the T_j measurement mentioned above, it is also hard to measure T_b precisely. Normally, structural modifications are needed for inserting a thermal-couple near the concerned location. Therefore, the accuracy of this method is highly dependent on the set-up.

Instead, structural function analysis is another method that numerically derived thermal network parameters of power modules based on their transient temperature response. It can reveal the heat transfer physics of power modules' internal layers and obtain the $R_{th(j-c)}$ without adding interference to the system. The principle to characterize power modules' transient thermal response is specified in the IEC 60747-9 standard. The module will be heated by a power loss (P_h) until it reaches a thermal steady-state. Then, P_h will be removed, and the transient response during the cooling down process will be recorded and represented as $Z_{th}(t)$, as shown in Equation (7.2.3). The process to derive the structural function from the transient thermal response is illustrated in Figure 7.8. As can be seen, the end goal is to

form a Cauer thermal network. Cauer thermal network reflex the physical-based thermal impedance accumulated from the sink to the source. Each unit in this network represents a vertical portion of the physical structure in the power module. However, it is necessary to clarify that the number of units in the thermal network is much larger than the number of packaging layers, since it is determined by the resolution of the discretization process. In other words, each packaging layer is separated as multiple "sub-layers", and each "sub-layer" is represented by a unit in the Cauer network. Detailed mathematics of numerical derivation and deconvolution can be found in literature (Székely, 1998; Schweitzer *et al.*, 2008).

$$Z_{th}(t) = \frac{T_j(t) - T_b(t)}{P_h} \tag{7.2.3}$$

The structural function analysis discussed above reveals thermal impedance accumulation from the coolant to the junction. However, in order to isolate the portion between junction to case. The Transient Dual Interface Methods (specified in JEDEC 51-14 standard) is applied. In this method, the power module is characterized under two conditions: 1) The module is mounted on the cold-plate without TIM. 2) The module is mounted on the cold-plate with TIM. Theoretically, structural function curves of these two conditions should overlap with each other from the junction to case and diverge afterward. Then, the case point is determined.

The structural function analysis of the prototype SSM module is also performed on the SIEMENS Power T3ster (PWT-1500A). The calibrated V_D to T_j relationship is utilized. The heating current, I_h, is supplied by the main power source from the source to the drain through the body diode. The sensing current, I_s, is sent from the measurement equipment to sense the V_D during this thermal transient. I_s should be

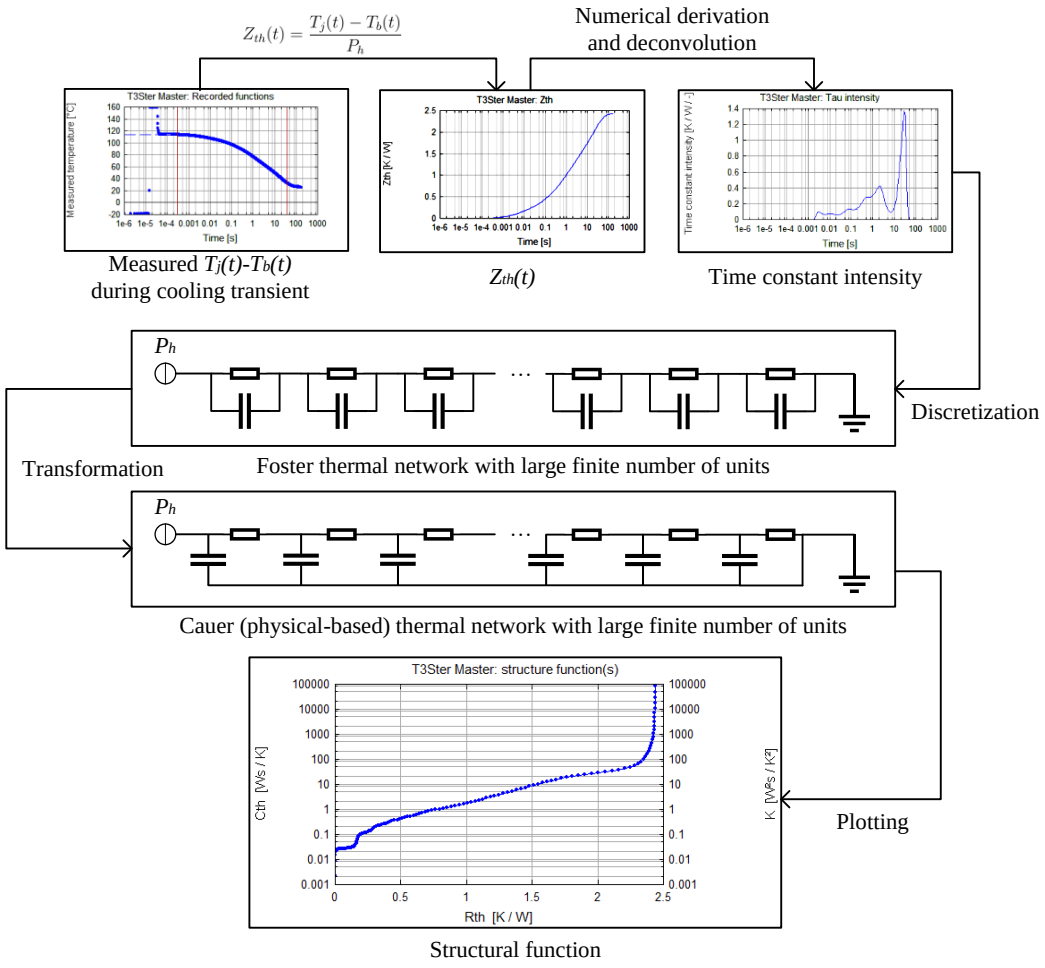


Figure 7.8: Process of deriving the structural function plot from the thermal transient response.

low enough to avoid introducing additional thermal losses but high enough to achieve stable measurements. In this test, I_s is set to be 200 mA, where the system noise is less than 0.1%. The testing circuit is illustrated in Figure 7.9. And Figure 7.10 shows the testing set-up.

Characterized structural function curves are combined in Figure 7.11, describing

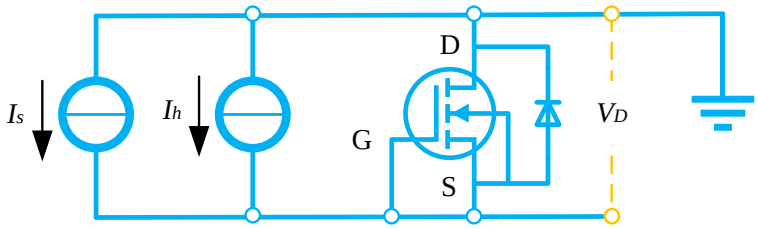
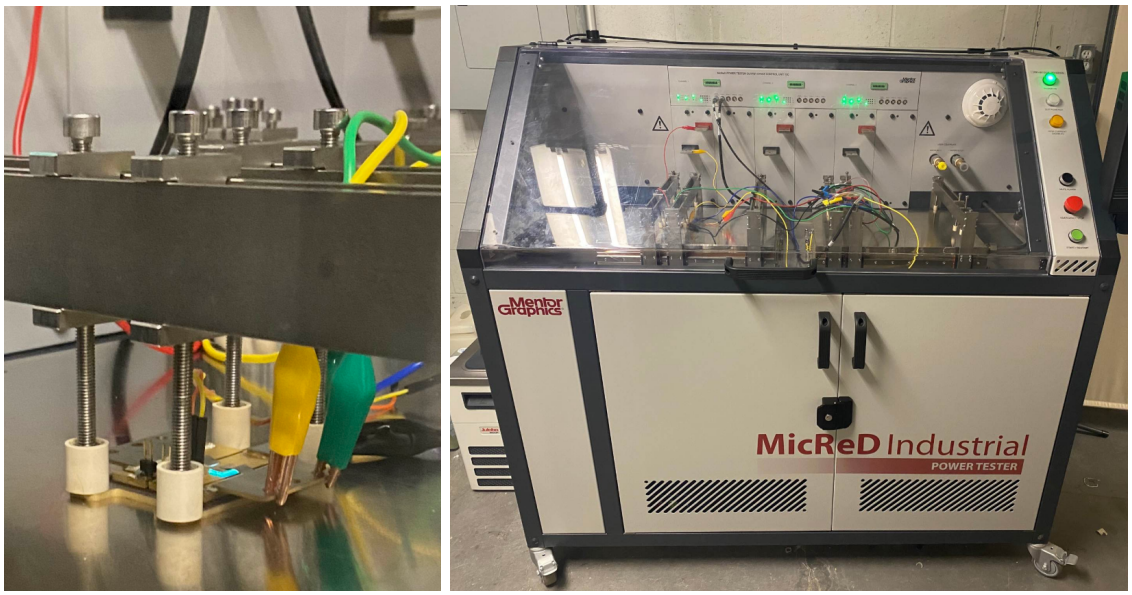


Figure 7.9: Concept schematic of the diode mode for MOSFET structural function analysis.



(a) (b)

Figure 7.10: Thermal characterization set-up: (a) device under test. (b) SIEMENS Power T3ster.

the accumulation of thermal impedance from the die junction to the ambient. The intersection point refers to the impedance values between the junction to case, in which $R_{th(j-c)}$ equals 1.46 K/W. It can be seen in Table 7.2 that both the analytical thermal model and the ANSYS simulation exhibit a very good accuracy. It is worth noting that off-the-shelf devices could have a lower $R_{th(j-c)}$ due to die paralleling.

However, the target of this study is to validate the proposed methodologies.

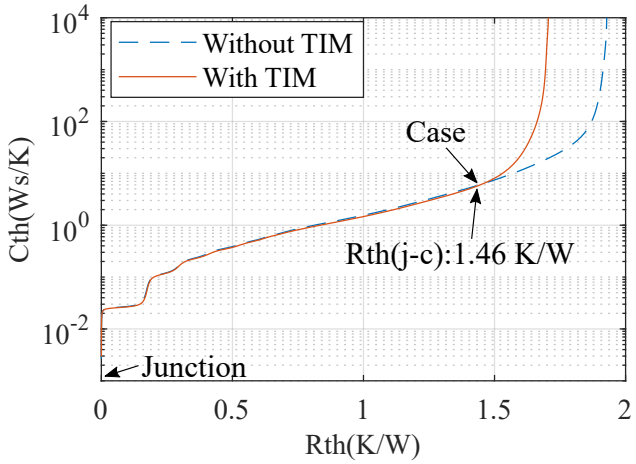


Figure 7.11: $R_{th(j-c)}$ characterization by structural function.

Table 7.2: Comparison of $R_{th(j-c)}$.

Results	Experiment	ANSYS simulation	Analytical model
$R_{th(j-c)}$ (K/W)	1.46	1.42	1.51
Error (%)	-	2.7	3.4

7.3 Summary

In this chapter, experimental characterizations of the prototype half-bridge SSM module were reported. First, the double pulse test was performed to capture the switching behavior of the module, in which the turn-off transient was used to calculate the L_s. It was found that the experimentally obtained L_s matches with the estimated value from the analytical model nicely with an error of only 0.4%. Next, the prototype

module's thermal impedance was measured using structural function analysis. The measured $R_{th(j-c)}$ agreed with the analytical estimation and the numerical simulation very well with errors less than 3.4%. Overall, experimental results validated that analytical thermal and L_s models proposed in Chapter 4 have good accuracy. Meanwhile, it also proved that the manufacturing methods introduced in Chapter 6 can successfully prototype SSM power modules with desired performances.

Chapter 8

Reliability Assessment of the Proposed SSM Packaging Scheme

This chapter will evaluate SSM packaging's reliability advantage through passive thermal cycling and active power cycling.

Power modules are subjected to multiple failures and fatigue modes, among which the fatigue at die-attachment layers and bond-wires are viewed as the most critical ones. Since the bond-wires are eliminated in the SSM packaging, the only mode to be discussed is the fatigue at die-attachment layers.

As introduced in Chapter 2, the Coffin-Manson model (Knoerr *et al.*, 2010; Zhang, 2014) is a widely used method for analyzing the lifetime of metallic or solder materials under cyclic-plastic deformation. Many studies have verified it as valid for power module die-attachment materials. This model considers that the lifetime of the material has an exponential relationship with the plastic strain difference ($\Delta\varepsilon_p$) during each cycle. Its governing equation is shown again here in Equation (8.0.1).

$$N_f = C_1 \Delta \varepsilon_p^{-C_2} \tag{8.0.1}$$

N_f denotes the cycle life, C_1 and C_2 are material constants. The parameter characterization of the specific sintered nano-silver materials (nanoTach from NBE) has been reported in Knoerr's work (Knoerr *et al.*, 2010) through experiments, in which C_1 equals 0.16, and C_2 is -2.96. Sintered nano-silver's properties are largely dependent on its relative density (or porosity) (Siow, 2019). The nanoTach material in Knoerr's work has a relative density of 75%-85%, which is similar to the material used in obtaining the Anand visco-plastic model. Also, the manufacturing process proposed in Chapter 6 achieves similar results. Therefore, it is reasonable to use these values in following analysis. Similary, parameters of the benchmark material, SAC305 solder, are also characterized by Knoerr, where C_1 and C_2 are 0.075 and -1.79, respectively. Coffin-Manson characterization curves of these two materials are shown in Figure 8.1.

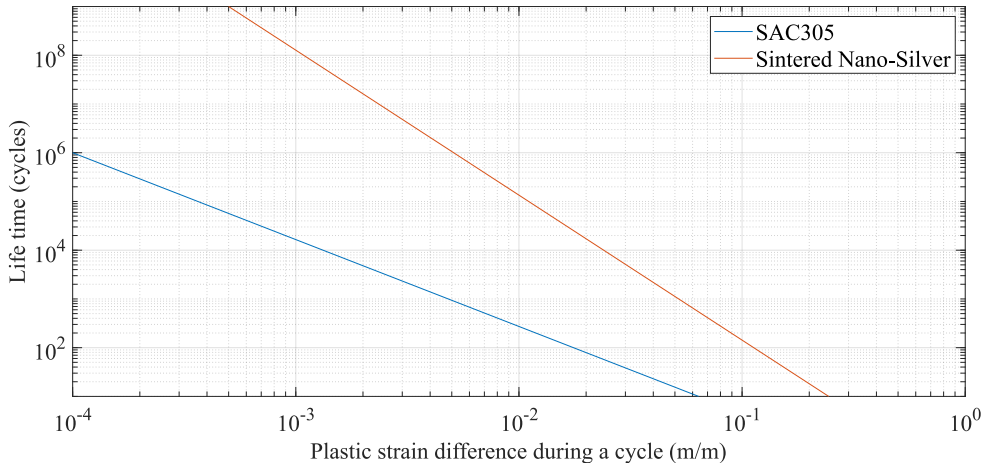


Figure 8.1: Coffin-Manson lifetime characterization of SAC305 solder and sintered nano-silver (Knoerr *et al.*, 2010).

8.1 Passive Temperature Cycling Simulations of Partial Structures

Passive temperature cycling is a standard approach to assess the lifetime of power modules, which emulates ambient temperature change. Several cycling profiles based on JEDEC standard (JEDEC, 2020) are applied in this analysis, which is generalized in Figure 8.2. All profiles simulated in this study have a T_{min} of -40^{o}C.

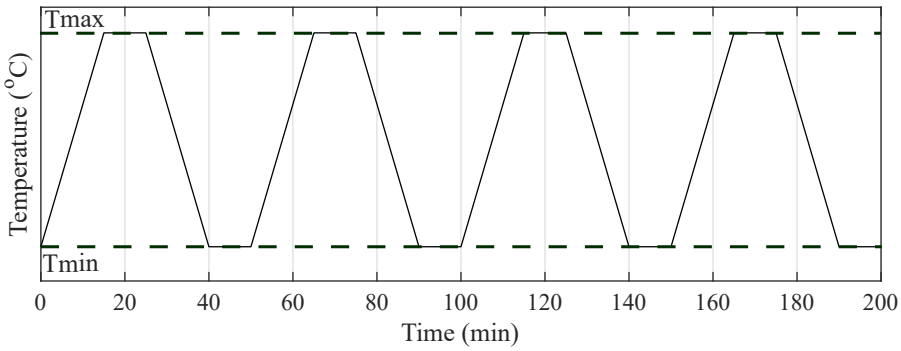
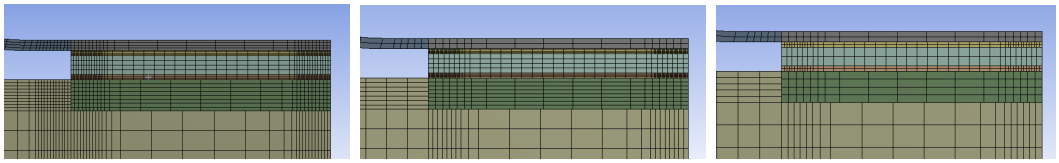


Figure 8.2: JEDEC temperature cycling profiles (JEDEC, 2020).

Thermal cycling simulations are carried out in the Static Structural Unit of the ANSYS Mechanical. Since it is assumed that there is no temperature gradient within the entire body during the passive thermal cycling, it is preferred to use partial structures defined in Chapter 3 to simplify the work. In thermal cycling simulations, the temperature of the partial structure is defined based on the cycling profile. Mechanical boundary conditions remain the same as those of the steady-state simulations in Chapter 3.

A mesh-sensitive study is conducted to determine the suitable mesh size that guarantees reliable results with limited computational cost. As shown in Figure 8.3, three different meshes with 0.5x, 0.75x, and 1x element sizes at critical regions are

compared.



(a) (b) (c)

Figure 8.3: Different sizes for mesh sensitive study: (a) 0.5x mesh size. (b) 0.75x mesh size. (c) 1x mesh size.

Figure 8.4 shows that simulation results remain unchanged with the meshes with both 0.75x and 0.5x element sizes. Therefore, 0.5x element size is selected.

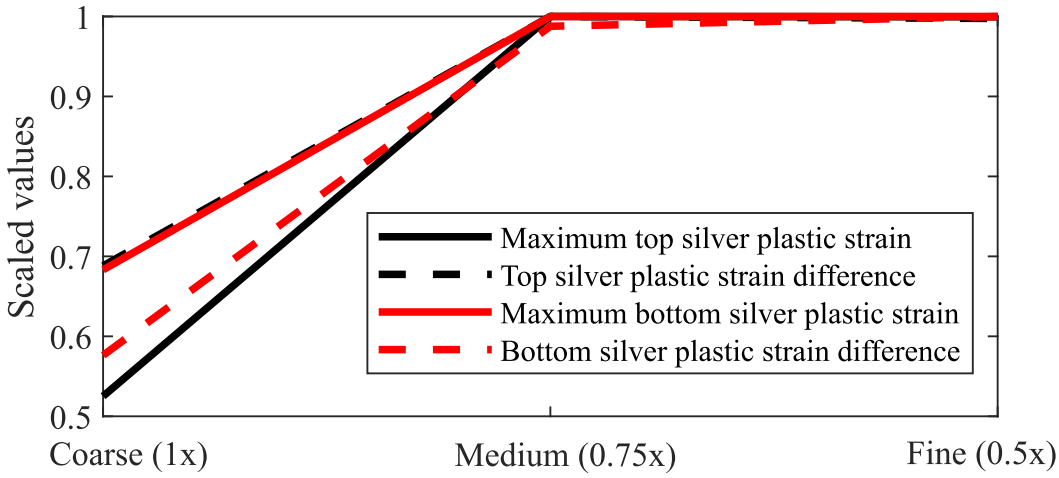


Figure 8.4: Mesh sensitive study.

The confidence level of this simulation model can be further evaluated by convergence analysis. Figure 8.5 shows the force and displacement convergence plots. It can be seen that the model converged quickly after 1 to 3 iterations for each simulation step, which indicates that this model is properly defined.

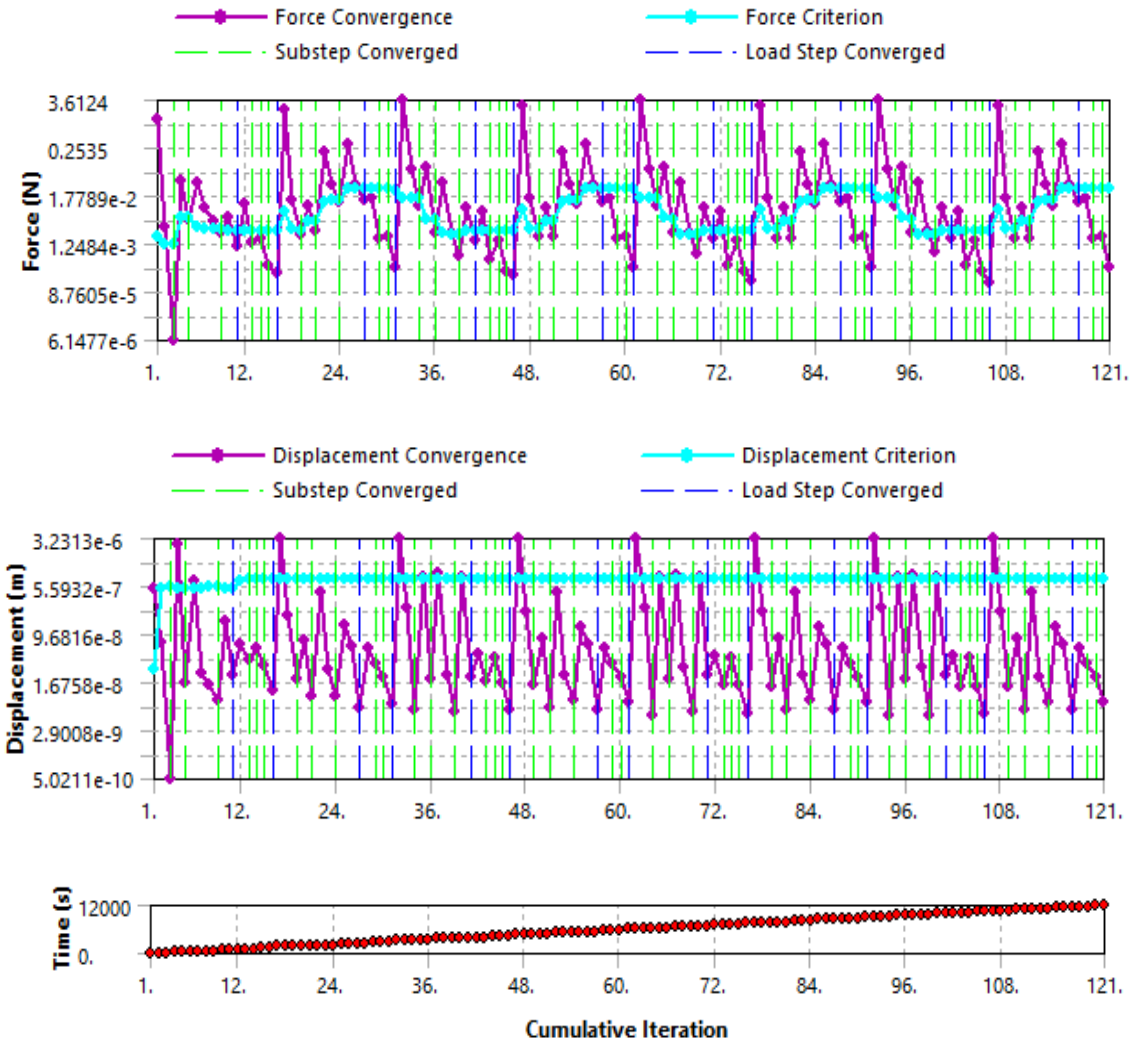


Figure 8.5: Convergence analysis of passive temperature cycling simulation.

8.1.1 SSM module under -40^{o}C to 125^{o}C temperature cycling

The temperature cycling between -40^{o}C and 125^{o}C is explained in detail here. The total deformation of the module at the 175_{th} minute is shown in Figure 8.6. Obviously, the maximum deformation appears at the farthest end. Figure 8.7 illustrates the maximum deformation of bonding (Ag) layers, which is located at corners. Apparently, contact surfaces between Ag and Mo are subjected to larger deformation.

This is because the CTE of Mo is larger than that of SiC, as can be seen in Table 3.3 and Figure 3.3.

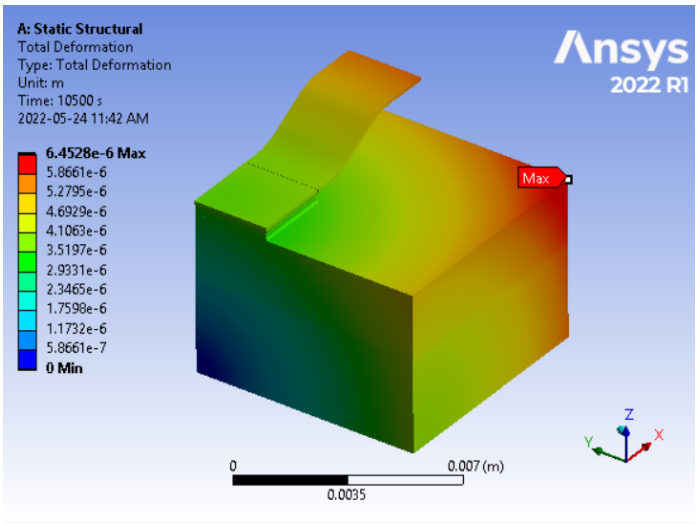
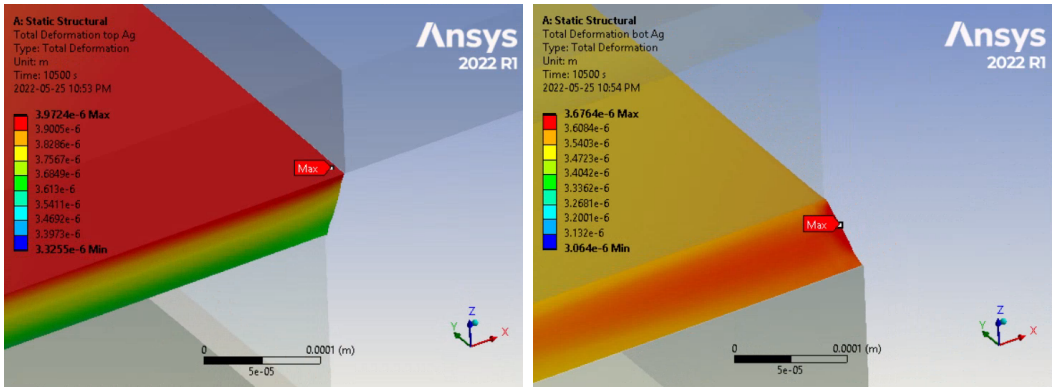


Figure 8.6: Total deformation (153x) of SSM module under -40^{o}C to 125^{o}C cycling.



(a) (b)

Figure 8.7: Maximum deformation at corners of Ag layers under -40^{o}C to 125^{o}C cycling: (a) top. (b) bottom.

As discussed above, fatigue at die-attachment layers is the concerned failure mode in this study. For the SSM packaging, two attachment layers (sintered nano-silver) are located at both the die's top and the bottom. Stress fluctuation curves of these two

layers during this cycling are shown in Figure 8.8. In general, these two layers went through similar stress changes. The maximum stress at the top silver layers (49.65 Mpa) is very close to that of the bottom silver layer (49.19 Mpa). Stress relaxation can be observed during this process. Take the first cycle of the top Ag layer as an example. From A to B, the stress decreases because the temperature approaches 25^{o}C (the stress-free temperature) from -40^{o}C. From B to C, the temperature continues to increase until it reaches 125 ^{o}C. However, the stress from thermal expansion is compensated by the stress relaxation, which allows the actual stress to first increase and then decrease slightly. From C to D, when the temperature load is fixed at 125^{o}C, the stress is brought down by stress relaxation only. During the cooling process from (D to E), the stress elevates fast due to compression. Then, the stress relaxation is dominant again during the second constant temperature region (E to F). Specifically, the stress relaxation is caused by the creep of the sintered nano-silver, which has rate-dependent visco-plastic properties. The creep of the material relaxes the strain, which releases the elastic stress at the contacted surfaces. Consequently, stress at the sintered nano-silver is reduced as well. Intrinsically, these creep and stress relaxation is due to mechanisms such as dislocation glide, dislocation creep, and diffusional flow (Nabarro creep) in the sintered nano-silver (Siow, 2019).

The stress profiles of these two layers at the end of the cycling are exhibited in Figure 8.9. For both layers, the maximum stress is located at the corners. First of all, stress concentration can always happen at sharp edges. Meanwhile, the edges and corners are subjected to the mismatch of thermal expansion by different materials. Therefore, they are typically the most critical locations. Similar behaviors have been reported by Zhang (Zhang, 2014) and Cao (Cao *et al.*, 2012). In fact, it is found that

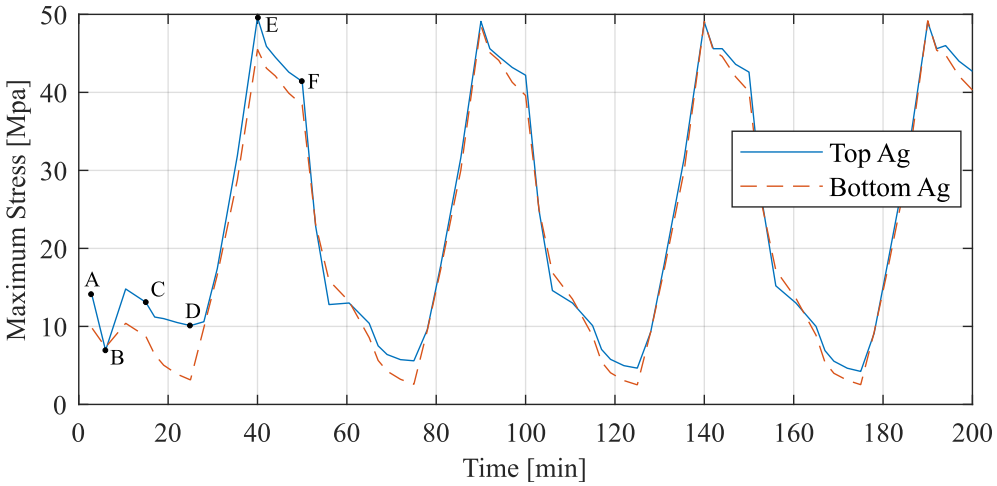
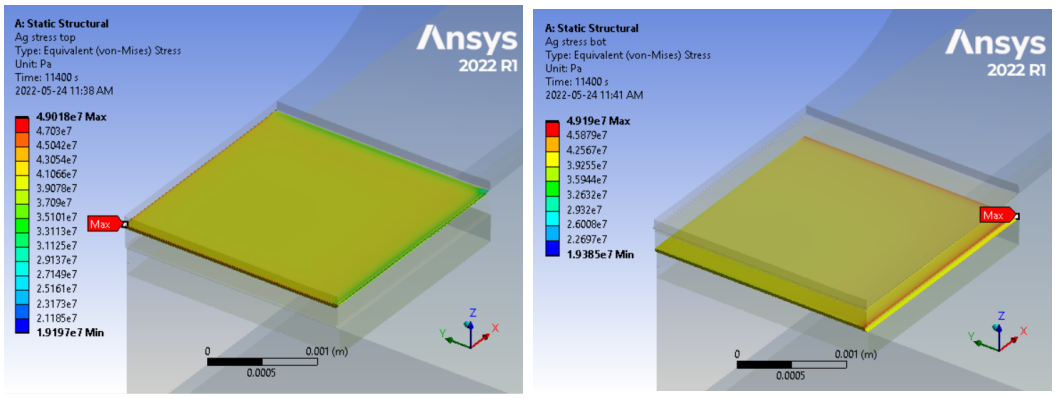


Figure 8.8: Stress fluctuation of Ag layers under -40^{o}C to 125^{o}C cycling.

corners of die-attachment layers are usually where cracks initiate (Cao *et al.*, 2012; Hung *et al.*, 2013), which brings failures and fatigue eventually.



(a) (b)

Figure 8.9: Stress profiles at Ag layers under -40^{o}C to 125^{o}C cycling: (a) top. (b) bottom.

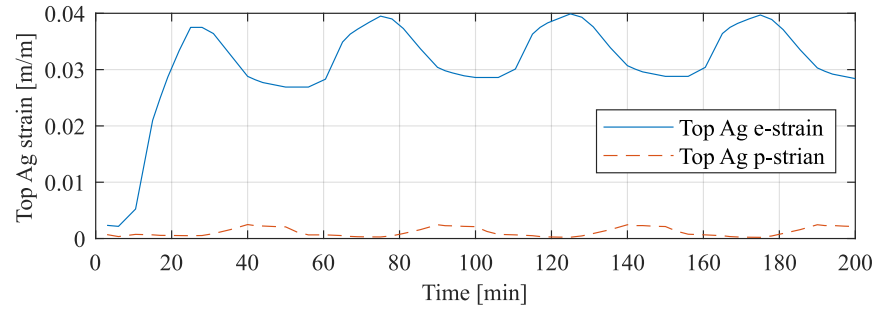
According to the Coffin-Manson model, the plastic strain variation during cycling is directly related to fatigue. Figure 8.10 illustrates strain fluctuation curves under this cycling condition, including both the elastic and plastic strains. Overall, the

strain curves get stabilized after two cycles. For both the top and the bottom layers, the elastic strain is much smaller than the plastic strain, demonstrating again that this is a plastic-dominant deformation. The bottom Ag layer is clamped by the SiC die and the constrained Mo substrate. In contrast, the top Ag layer is clamped by the SiC and the thin Mo lead which is free to move. Consequently, the bottom Ag layer undergoes smaller deformation. The maximum plastic strain (0.0397 m/m) of the top Ag layer is also nearly 3x larger than that of the bottom Ag layer (0.0126 m/m). More importantly, the $\Delta\varepsilon_p$ of the top layer (0.0109 m/m) is much larger than that of the bottom layer (0.00406 m/m). Thus, the top silver layer is subjected to a higher fatigue risk. The plastic strain distributions of these two layers are shown in Figure 8.11. Critical points are also located at corners.

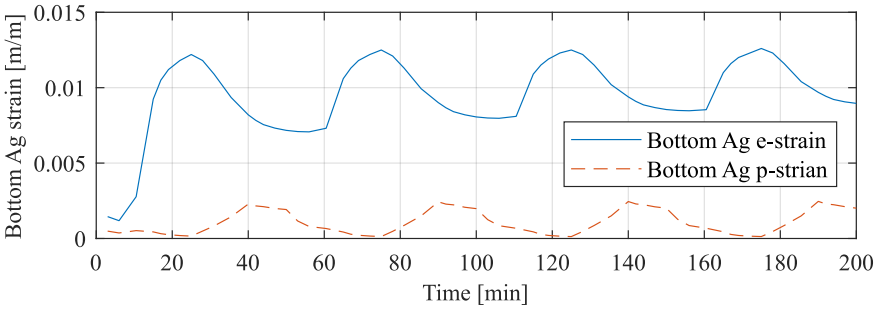
8.1.2 Comparative studies and lifetime analysis

A few more temperature cycling processes are simulated following the same procedure introduced above. Performances of die-attachment layers in the partial structures with both the SSM packaging and the Si_3N_4 based conventional packaging are compared.

Two most commonly used temperature cycling processes from JEDEC, -40^{o}C to 85^{o}C and -40^{o}C to 125^{o}C, are simulated in this comparative study, whose results are shown in Figure 8.12. The higher T_{max} apparently leads to higher stress and plastic strain difference, causing a shorter lifetime for both modules. However, the differences between the two modules are significant. The SSM module has over 16.7% lower maximum stress at the bonding, over 10 times lower plastic strain difference, and over 1000 times longer lifetime. Results demonstrated that the proposed SSM

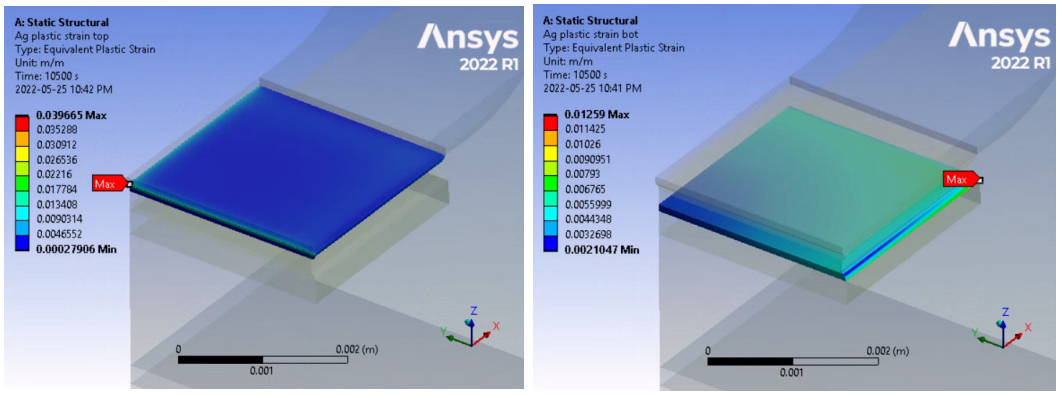


(a)



(b)

Figure 8.10: Strain fluctuation of Ag layers under -40^{o}C to 125^{o}C cycling: (a) top. (b) bottom.



(a) (b)

Figure 8.11: ε_p at Ag layers under -40^{o}C to 125^{o}C cycling: (a) top. (b) bottom.

packaging has a significantly better performance in fatigue and lifetime than the conventional packaging.

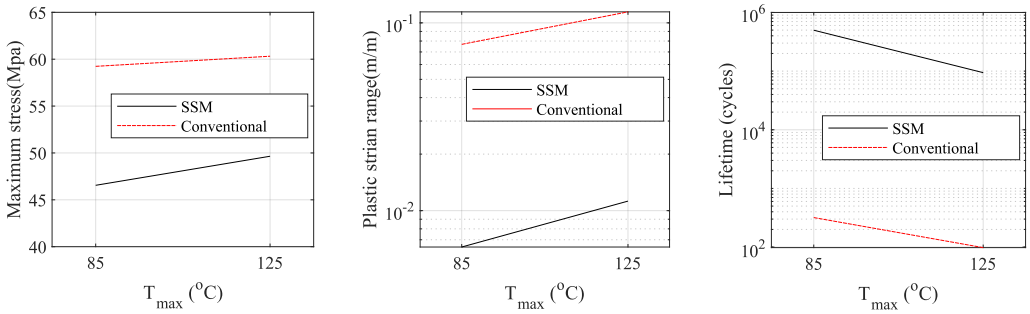


Figure 8.12: Comparative study: (a) maximum stress at Ag layers. (b) $\Delta\varepsilon_p$ at Ag layers. (c) lifetime.

In Table 8.1, results of this study are compared with Knoerr's experiments (Knoerr *et al.*, 2010) (case A, B, C, and D), where the Coffin-Manson parameters are cited. Here, t_{dwell} is the dwell time at T_{max} and T_{min} in each cycle. Regarding the conventional packaging, it has been proved that the case (case C and D) using sintered nano-silver as die-attachments has a much longer lifetime compared with cases with SnAg solders (case A and B). Comparing case C, D, E, and F, which feature metallized ceramic substrates and sintered nano-silver bonding, cases from this study (case E and F) are predicted to have a slightly longer lifetime than cases from the literature. It is mainly due to the smaller temperature range during thermal cycling. Also, different die sizes (Si Diode vs. SiC MOSFET) and ceramic materials (Al_2O_3 vs. Si_3N_4) affect performances. Overall, all lifetime results are in the same magnitudes, indicating that simulations in this work have a decent confidence level. Case G and H are results using the SSM packaged structures, which have remarkably longer lifetimes than others. This is mainly due to the low $\Delta\varepsilon_p$ during each cycle (around 4×10^{-3} m/m and 8×10^{-3} m/m, respectively). As discussed before, the CTE difference between the SiC die and the Mo substrate is significantly smaller than that

Table 8.1: Lifetime comparison with benchmarks from the literature (Knoerr *et al.*, 2010)

Cases	Packaging type	Die-attachment material	Method	Temperature cycling profile	Lifetime (cycles)
A	Si Diode with Al_2O_3 substrate	SnAg solder	Experiment	-5^{o}C to 175^{o}C (t_{cycle}=60 min, no t_{dwell})	87
B	Si Diode with Al_2O_3 substrate	SnAg solder	Experiment	-55^{o}C to 175^{o}C (t_{cycle}=60 min, no t_{dwell})	51
C	Si Diode with Al_2O_3 substrate	Sintered nano-silver	Experiment	-5^{o}C to 175^{o}C (t_{cycle}=60 min, no t_{dwell})	790
D	Si Diode with Al_2O_3 substrate	Sintered nano-silver	Experiment	-55^{o}C to 175^{o}C (t_{cycle}=60 min, no t_{dwell})	105
E	SiC MOSFET with Si_3N_4 substrate	Sintered nano-silver	Conffin-Manson model	-40^{o}C to 85^{o}C (t_{cycle}=50 min, t_{dwell}=10 min)	316
F	SiC MOSFET with Si_3N_4 substrate	Sintered nano-silver	Conffin-Manson model	-40^{o}C to 125^{o}C (t_{cycle}=50 min, t_{dwell}=10 min)	98
G	SiC MOSFET with SSM	Sintered nano-silver	Conffin-Manson model	-40^{o}C to 85^{o}C (t_{cycle}=50 min, t_{dwell}=10 min)	498225
H	SiC MOSFET with SSM	Sintered nano-silver	Conffin-Manson model	-40^{o}C to 125^{o}C (t_{cycle}=50 min, t_{dwell}=10 min)	94132

between the SiC die and the metallized ceramic substrate. Therefore, the advantage is expected. In fact, similar to case H, a case with a $\Delta\varepsilon_p$ of 8×10^{-3} m/m is also reported in Knoerr's work (Knoerr *et al.*, 2010). The experimentally measured lifetime

of this case is around 2×10^5 cycles, which agrees with case H very well. Thus, it is safe to conclude that the SSM packaging has a tremendous advantage in its lifetime over the conventional packaging.

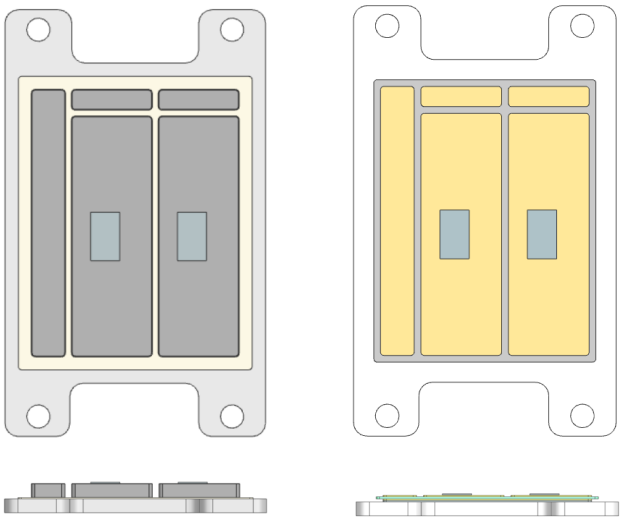
8.2 Active Power Cycling Simulations of Half-bridge Power Modules

8.2.1 Simulation models

Active power cycling is another way to characterize the reliability of power modules, which is also specified in the JEDEC standard (JEDEC, 2020). Since power cycling represents thermal loads caused by cyclic electrical power, it is more meaningful to study actual power modules instead of partial structures. In this study, the SSM half-bridge module and a Si_3N_4 based conventional module are simulated. The layer definition and thicknesses of the conventional module stay the same as what was shown in Figure 3.7 and Table 3.6. In order to achieve a reasonable comparison, the conventional module has the same layout and footprint as the SSM module.

The concerned failure mode in this study is the fatigue at die attachment layers beneath semiconductor dies in both modules. Therefore, leads, bond-wires, and terminals are ignored. CAD models of these two modules are illustrated in Figure 8.13.

Simulations are again conducted in ANSYS Mechanical, as shown in Figure 8.14. First, power modules' temperature response under cyclic power loads is simulated in the Transient Thermal Unit. Then, the temperature profile is fed into the Static Structural Unit to evaluate modules' mechanical response. In the Transient Thermal



(a) (b)

Figure 8.13: CAD models for active power cycling simulations: (a) SSM half-bridge module. (b) Si_3N_4 based conventional half-bridge module.

Unit, repetitive power losses (P_{loss}) are equally assigned on two semiconductor dies in a half-bridge module. P_{loss} is adjusted for different modules for achieving a desired T_j profile. This work intends to study the extreme cycling condition, where the power module operates between the off-state and the full-power-state. Therefore, the T_j variation is expected to be from 30^{o}C to 155^{o}C, which is normally the T_j at full power for off-the-shelf power modules in the market. As for the cooling condition, an effective convection coefficient of 5000 W/m·K is assigned at the bottom of both modules. In general, T_j variations of both modules are tuned as identical as possible. Profiles of the assigned P_{loss} and the expected T_j are shown in Figure 8.15, which is according to the JEDEC standard (JEDEC, 2020) and the Infineon's power cycling instruction (Infineon Technologies AG, 2019).

Mesh quality is essential in these simulations. Therefore, it should be carefully

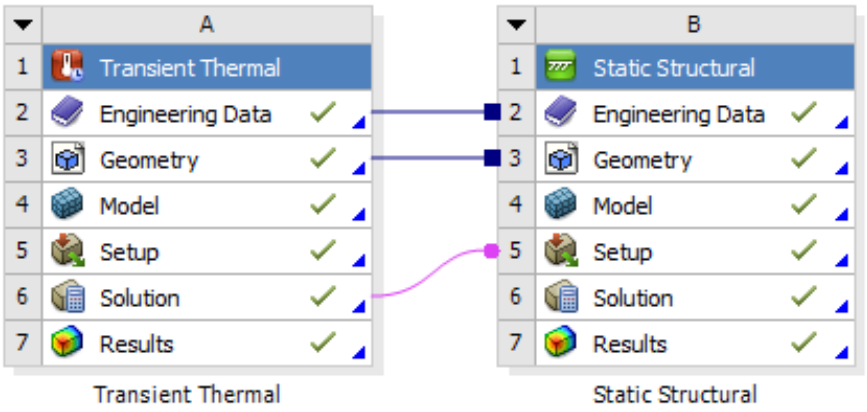


Figure 8.14: ANSYS Mechanical simulation environment for active power cycling.

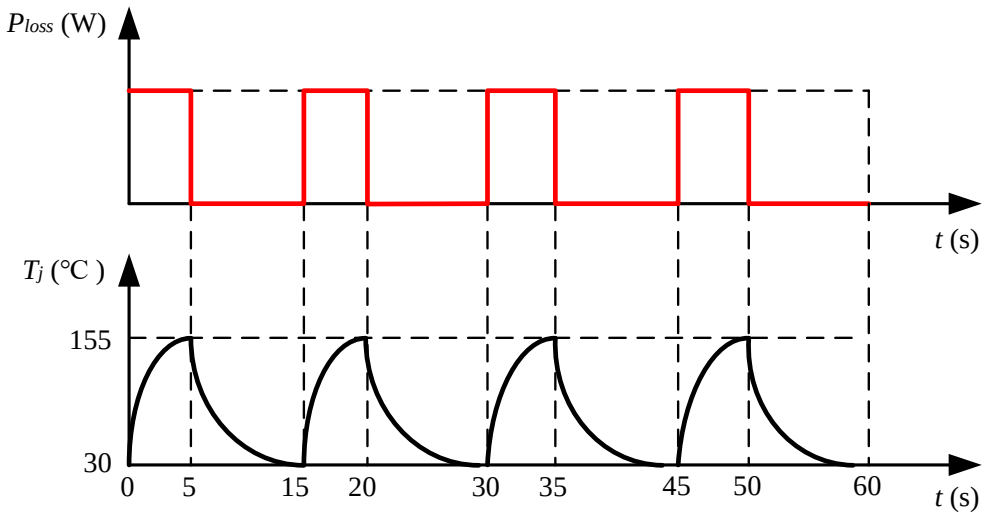


Figure 8.15: The assigned P_{loss} and the expected T_j profiles during active power cycling (4 cycles).

designed. Take the SSM half-bridge module as an example. A mesh containing 744136 elements was applied, as shown in Figure 8.16. It can be seen that extremely fine mesh was assigned around critical locations, die-attachment layers.

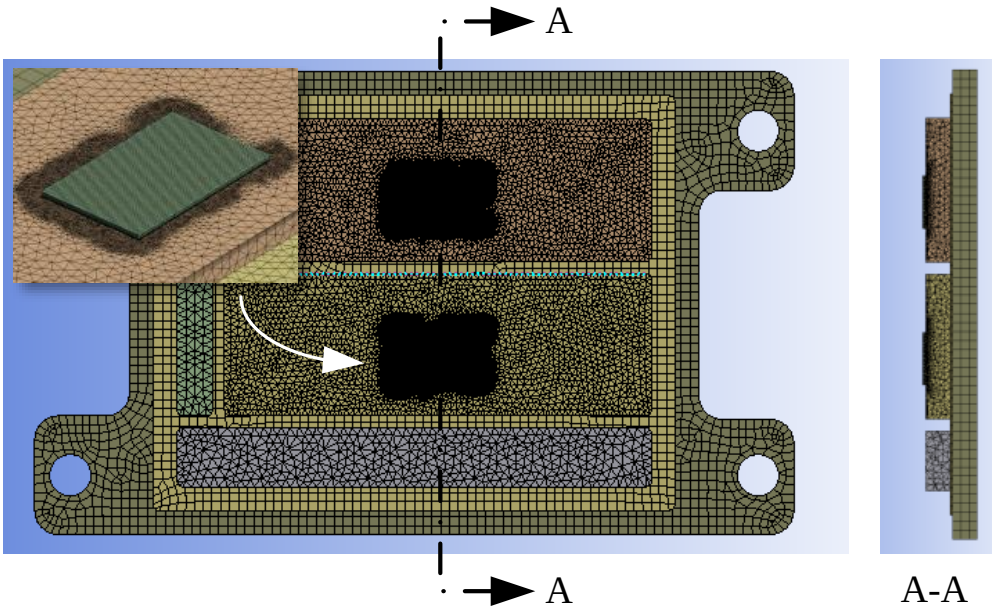


Figure 8.16: Mesh of the SSM half bridge-power module.

Convergence plots obtained from the static structural analysis of the SSM module can be found in Figure 8.17. They show that each simulation step can reach a proper convergence after less than two iterations, which indicates that the simulation model is properly defined.

8.2.2 Comparative studies and lifetime analysis

Active power cycling simulations (30^{o}C to 155^{o}C) were conducted on both modules, and this comparative study can be used to evaluate the reliability advantage of the SSM packaging. Temperature profiles of two modules at the instant (the 50_{th} second) of when T_j reaches 155^{o}C during the 4_{th} cycle are shown in Figure 8.18. As discussed

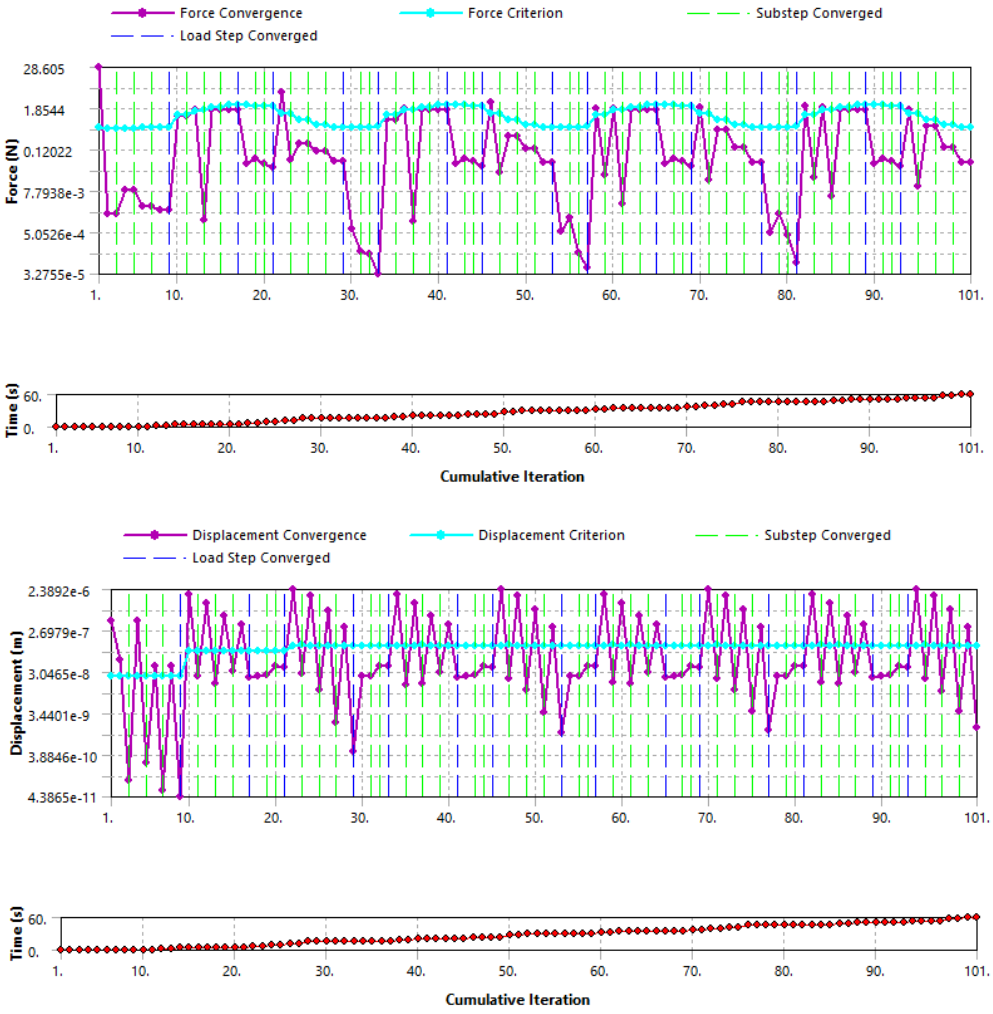
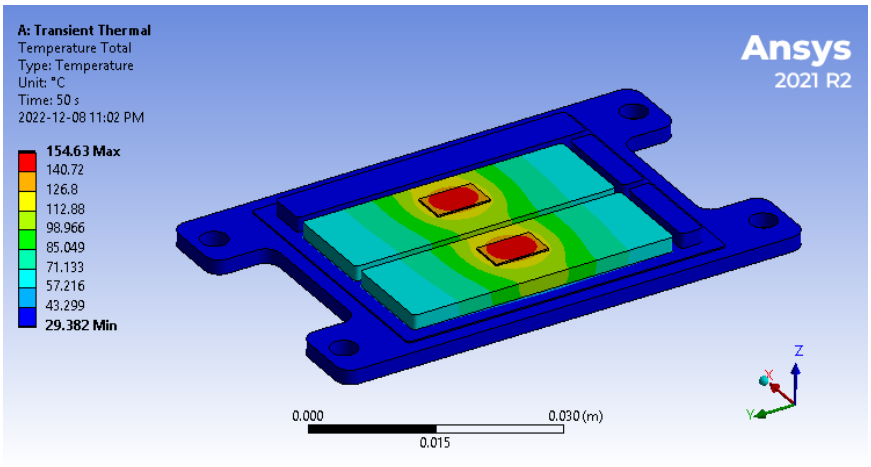


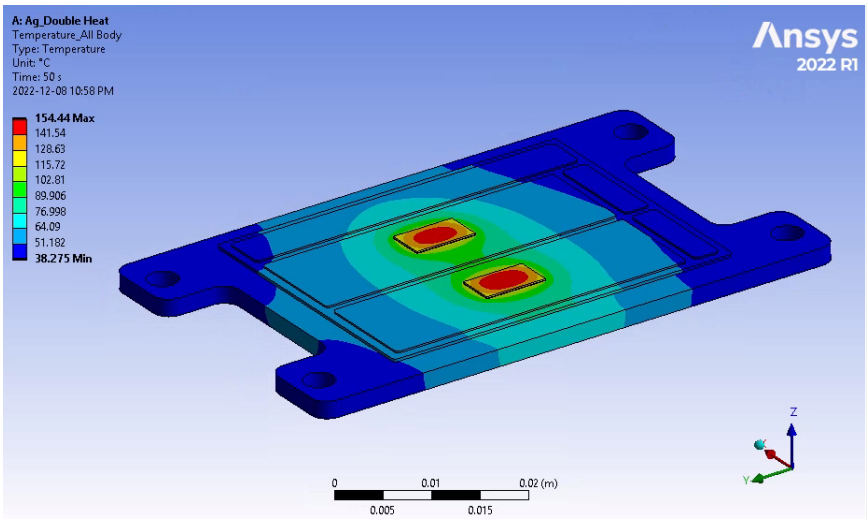
Figure 8.17: Convergence analysis from the structural simulation for the SSM half-bridge power module.

above, the critical failure mode is fatigue at die-attachment layers. Therefore, the deformation of these critical locations at the same instant is displayed in Figure 8.19. Clearly, the die-attachment layer in the SSM module has a much smaller deformation than that in the conventional module, which indicates that the SSM packaging has a

lower risk of failure than the benchmark.



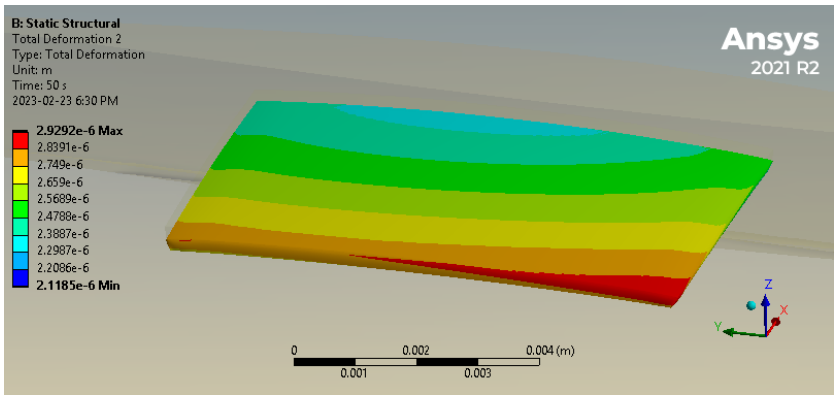
(a)



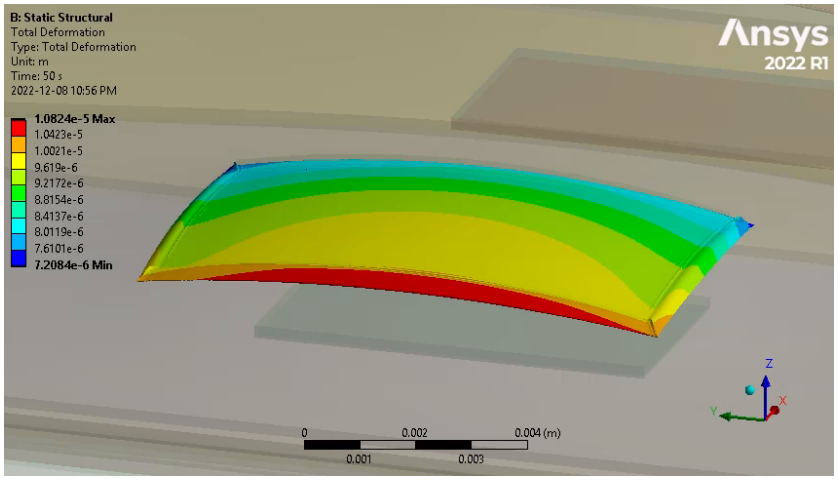
(b)

Figure 8.18: Temperature profiles of power modules at the 50_{th} second: (a) SSM half-bridge module. (b) Si_3N_4 based conventional half-bridge module.

Similar to the passive temperature cycling analysis, fatigue at die-attachment layers can be evaluated by using the Coffin-Manson model, which requires the $\Delta\varepsilon_p$ as the fatigue indicator. Figure 8.20 displays T_j and ε_p fluctuation curves of dies in two modules, from which the $\Delta\varepsilon_p$ can be extracted. Key results are summarized in



(a)



(b)

Figure 8.19: Deformation (500x) of die-attachment layers at the 50_{th} second: (a) SSM half-bridge module. (b) Si_3N_4 based conventional half-bridge module.

Table 8.2.

As designed, both dies in the SSM module have similar performances. However, these in the conventional module behave differently. The right die is clearly subjected to a higher risk of fatigue. It can be seen that, with the same layout and dimensions, the SSM packaging is able to reduce the maximum $\Delta\varepsilon_p$ during cycling by a factor of six compared with the conventional packaging, which results in a 190 times increase of expected N_f and lifespan. Thus, the tremendous advantage of improving power

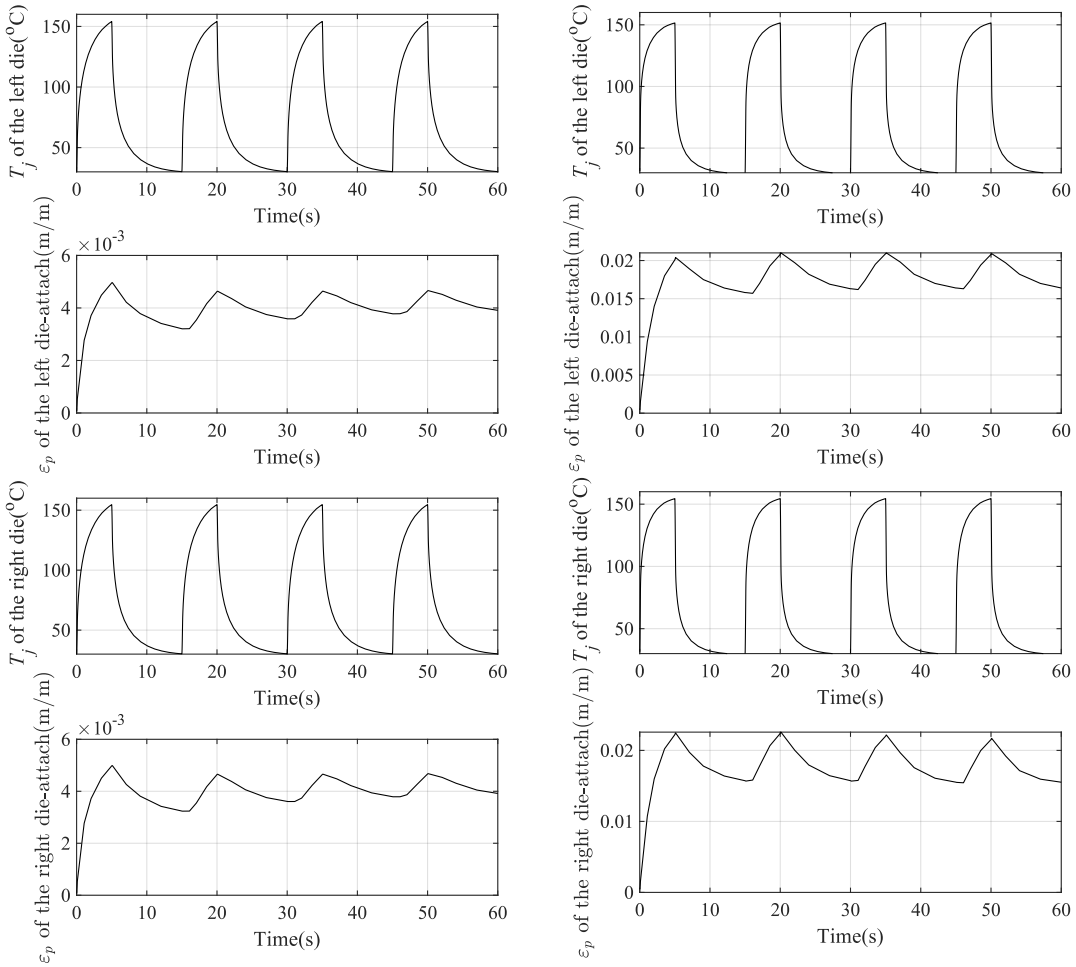


Figure 8.20: T_j and ε_p fluctuation curves of dies in two modules: (a) SSM half-bridge module. (b) Si_3N_4 based conventional half-bridge module.

modules' reliability by using the SSM packaging is proven.

Results	SSM module (left die)	SSM module (right die)	Conventional module (left die)	Conventional module (right die)
Maximum T_j (^{o}C)	154.1	154.6	151.5	154.4
$\Delta\varepsilon_p$ (m/m)	0.011	0.011	0.049	0.066
N_f (cycles)	86265200	86744781	1099359	455203
Lifespan (hours)	359438	361436	4581	1897

Table 8.2: Key results from active power cycling simulations.

8.3 Summary

In this chapter, the reliability advantage of the proposed SSM packaging was assessed by means of passive thermal cycling and active power cycling simulations. Partial structures were used in the passive temperature cycling analysis, which emulates the ambient temperature change. Results showed that the SSM packaging could improve the reliability of the module to a large extent. For example, in the case of -40^{o}C to 125^{o}C thermal cycling, the $\Delta\varepsilon_p$ was reduced by 10 times, and the cycle life was increased by a factor of over 1000 by using the SSM packaging. Results were also compared with previous works from the literature to prove their credibility. As for the active power cycling, since it represents the actual operation of power modules, half-bridge modules were simulated. Similarly, it is found that the SSM module leads to a 190 times longer lifespan than the conventional module. Therefore, the SSM packaging's reliability advantage is proven.

Chapter 9

Conclusions and Future Work

9.1 Conclusions

This thesis completed a systematic study of a packaging technology suitable for SiC power modules, the SSM packaging. The main contents and contributions are summarized here.

Chapter 2 provided an overview of power modules' packaging structure, materials, and failure modes. An in-depth review of the current status and future trends of power module packaging was also presented.

Chapter 3 proposed an advanced packaging scheme based on CTE-matched materials. Steady-state thermal-mechanical analyses were conducted to evaluate different candidate materials for the core metal in the proposed packaging scheme. The comparative study demonstrated that pure Mo results in the lowest stress at critical locations, which indicates enhanced reliability. Therefore, pure Mo is selected as the core metal. And the proposed technology is named as Silver-Sintered Molybdenum (SSM) packaging.

In Chapter 4, analytical models for estimating power modules' thermal and electrical performances were proposed and validated. These models are essentially suitable for half-bridge power modules with IMS-type packaging. First, a decoupled Fourier-based thermal model was proposed, which showed improved accuracy compared with the original Fourier-based thermal model when estimating T_j and ΔT_j, where errors are less than 4% and 11%, respectively. Then, to estimate L_s, a model combining the partial inductance model and effective current conduction region analysis was proposed, whose errors were less than 12.1% on sample modules.

In Chapter 5, the process of optimizing a half-bridge power module based on the SSM packaging was presented. The design method included analytical thermal and stray inductance models and the PSO algorithm. With considerations of practical boundary conditions and dimension limits, an optimized prototype module was designed with SiC MOSFETs (CPM3-1200-0013A) as switches. T_j and L_s of the prototype module were verified by numerical simulations. Compared with calculated values from analytical models, simulation results showed an error of less than 5% for θ_j estimation and an error of 8.3% for L_s estimation, which validated again that analytical models have a decent accuracy.

In Chapter 6, a prototype power module with the proposed SSM packaging was fabricated. The complete process was elaborated. And the key step, the pressure-less nano-silver sintering between Mo parts and SiC dies, was studied in detail. The fabrication process includes four parts: the re-metalization of gate and source pads on SiC dies, the assembly of Mo-based IMS by vacuum curing of the BT resin, die attaching, and the formation of interconnections, where the last two parts were achieved by nano-silver sintering. Specifically, nano-silver sintering with various Mo surface

conditions and T_s were investigated in detail. By analyzing micro-structures and the material composition of samples, a pressure-less sintering profile was recommended, where Mo surfaces are coated with Ni(0.8 μm)/Au(0.1 μm), and T_s is 250^{o}C.

Chapter 7 presented experimental characterizations of the prototype half-bridge SSM module. First, the double pulse test was performed to capture the switching behavior of the module, in which the turn-off transient was used to calculate the L_s. It was found that the experimentally obtained L_s matches with the estimated value from the analytical model nicely with an error of only 0.4%. Next, the prototype module's thermal impedance was measured using structural function analysis. The measured $R_{th(j-c)}$ agreed with the analytical estimation and the numerical simulation very well with errors less than 3.4%. Overall, experimental results validated that analytical thermal and L_s models proposed in Chapter 4 have good accuracy. Meanwhile, it also proved that the manufacturing methods introduced in Chapter 6 can successfully prototype SSM power modules with desired performances.

In Chapter 8, the reliability advantage of the proposed SSM packaging was assessed by means of passive thermal cycling and active power cycling simulations. Partial structures were used in the passive temperature cycling analysis, which emulates the ambient temperature change. Results showed that the SSM packaging could improve the reliability of the module to a large extent. For example, in the case of -40^{o}C to 125^{o}C thermal cycling, the $\Delta\varepsilon_p$ was reduced by 10 times, and the cycle life was increased by a factor of over 1000 by using the SSM packaging. Results were also compared with previous works from the literature to prove their credibility. As for the active power cycling, since it represents the actual operation of power modules, half-bridge modules were simulated. Similarly, it is found that the SSM module leads

to a 190 times longer lifespan than the conventional module. Therefore, the SSM packaging's reliability advantage is proven.

9.2 Future Work

In the future, this research can also be continued in multiple directions. First of all, the SSM package proposed in this study can be applied to other types of devices, such as discrete devices, three-phase full-bridge devices, etc. In addition, the modeling and design methods proposed in this thesis can also be modified and extended to design other types of devices. Meanwhile, SSM packaging technology's advantages in improving power modules' reliability can also be further investigated. What's more, it will be exciting to apply power modules with the SSM packaging in power electronic systems. In a word, this research provides a new direction for SiC power module packaging. The outcomes of this work will help the power module industry advance in directions of high performance and high reliability, promote the transportation electrification process, and realize energy saving and emission reduction.

Appendix A

Power Loss Simulation of the Half-Bridge SiC Power Module in a Three-Phase Inverter

In Chapter 5, a power loss of 41W per die was used during the design optimization of the prototype power module. It was briefly mentioned that this value is based on an assumed application in a three-phase inverter. Here, details are given.

Hal-bridge power modules are often used as phase legs in three-phase inverters, as shown in Figure A.1. The selected SiC MOSFET die, CPM3-1200-0013A, has a breakdown voltage of 1200 V, making it normally used in 800 V systems. An example inverter based on common engineering practices is designed and its main parameters are shown in Table A.1.

In theory, total power loss (P_{tot}) of a SiC MOSFET, as shown in Equation (A.0.1), consists of the conduction loss of the MOSFET (P_{MOS-c}), the switching loss of the

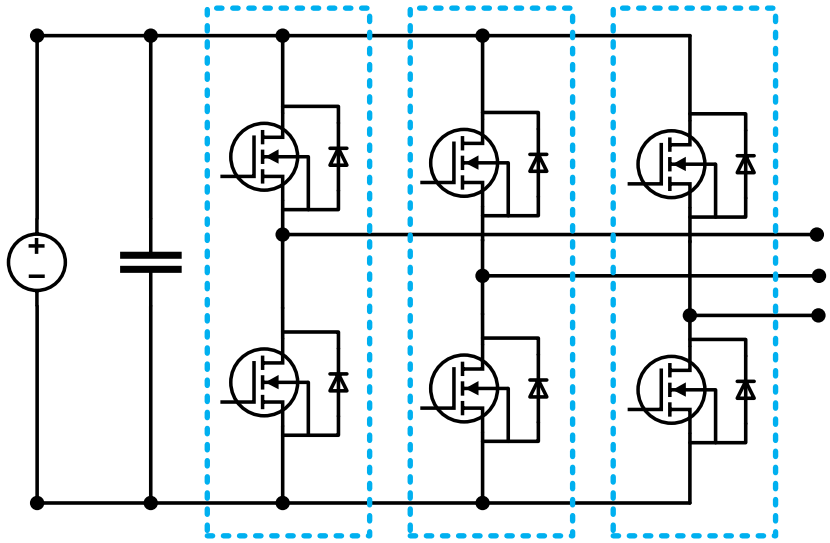


Figure A.1: Schematic of a three phase inverter with SiC MOSFET half bridge modules.

Table A.1: Specifications of the example inverter

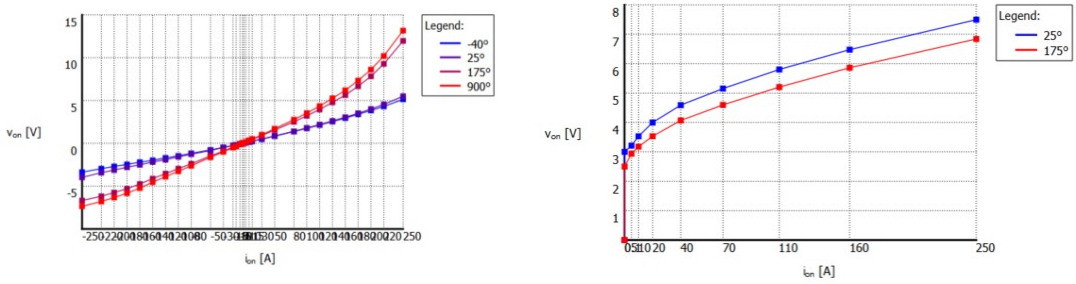
DC-link Voltage	Peak Power	Switching Frequency	External Gate Resistance	Norminal Fundamental Frequency	Maximum T_j	Modulation Scheme
800 V	25 kVA	15 kHz	1 Ohm	400 Hz	175 ^{o}C	SVPWM

MOSFET (P_{MOS-s}), and the conduction loss of the body diode ($P_{Diode-c}$) (Jones-Jackson *et al.*, 2022). The switching loss of the body diode is ignored due to its ultra-fast reverse recovery speed. P_{MOS-c} and $P_{Diode-c}$ are determined by the on-state characteristics of the MOSFET and the body diode, respectively. P_{MOS-s} is calculated using the switching frequency (f_{sw}) and switching energy, including the turn-on energy (E_{on}) and the turn-off energy (E_{off}), as depicted in Equation (A.0.2).

On-state characteristics are shown in Figure A.2. And the switching energy is illustrated in Figure A.3. These parameters are cited from the datasheet of a discrete SiC MOSFET device, C3M0016120D (CREE WolfSpeed, 2019), which contains similar dies as the one selected in this study. The difference between using two discrete devices and using the SSM half-bridge module is ignored since the target here is just to obtain a reasonable estimation of the power loss.

$$P_{tot} = P_{MOS-c} + P_{MOS-s} + P_{Diode-c} \tag{A.0.1}$$

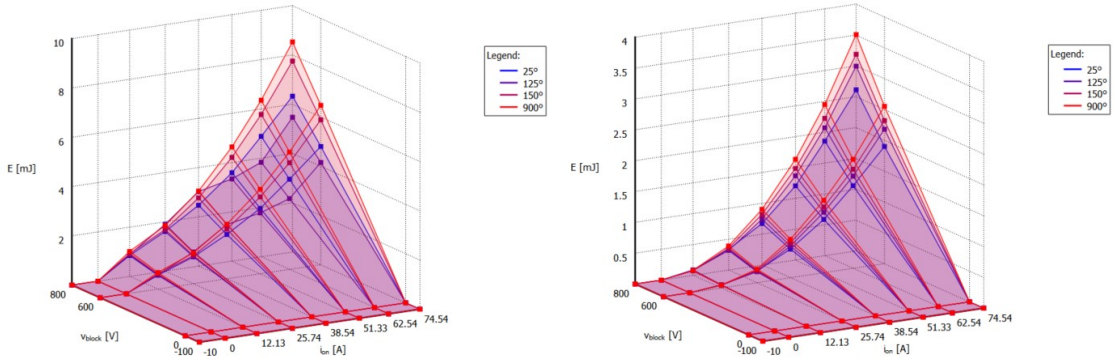
$$P_{MOS-s} = (E_{on} + E_{off}) \times f_{sw} \tag{A.0.2}$$



(a) (b)

Figure A.2: On-state characterizations: (a) MOSFET. (b) body diode.

The example inverter is simulated in the PLECS software using the standard space vector pulse width modulation, in which power losses of devices can be extracted. The aforementioned parameters are imported into the PLECS simulation as look-up tables. The simulation model is shown in Figure A.4. At the operating condition listed in Table A.1, the output line-line voltages and phase currents are shown in



(a) (b)

Figure A.3: MOSFET switching energy: (a) E_{on}. (b) E_{off}.

Figure A.5, which result in the P_{tot} curve shown in Figure A.6. The stabilized value of P_{tot} is 41 W for each die, which was used in design optimizations in Chapter 5.

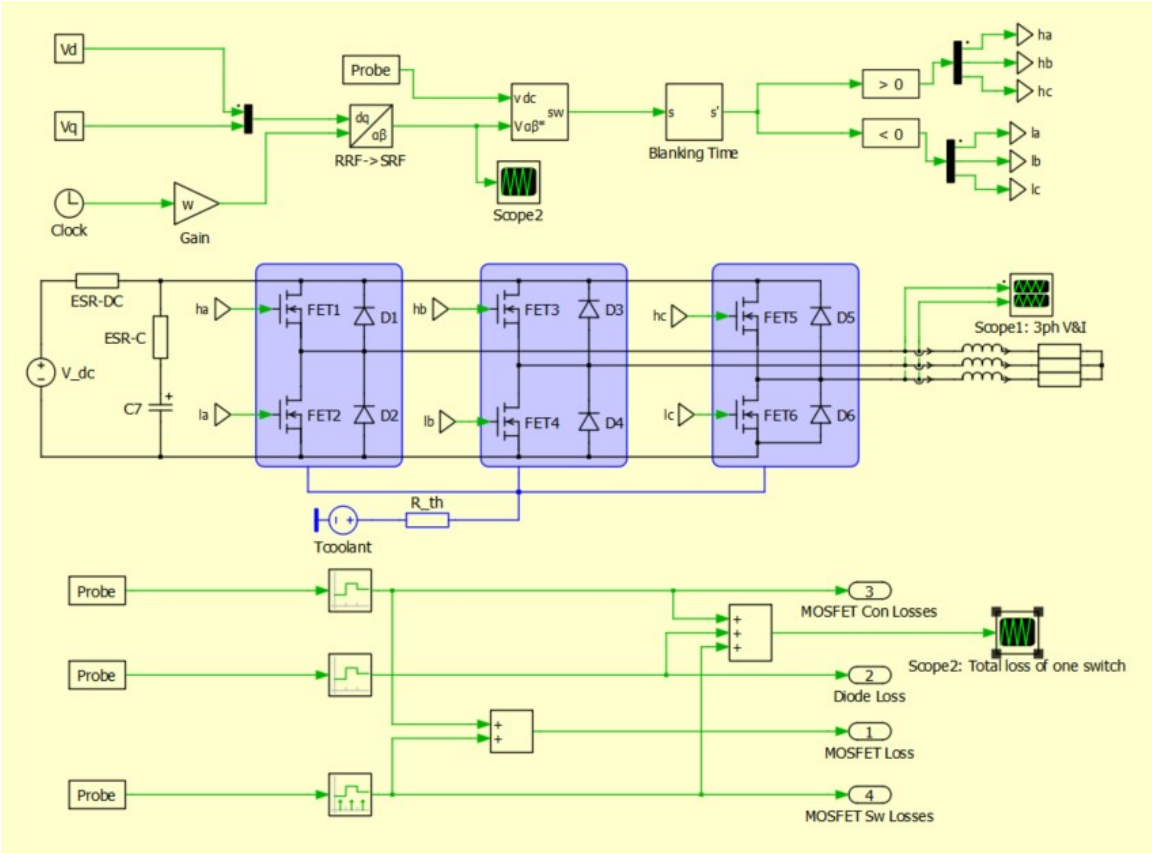


Figure A.4: Simulation model of the three-phase inverter in PLECS.

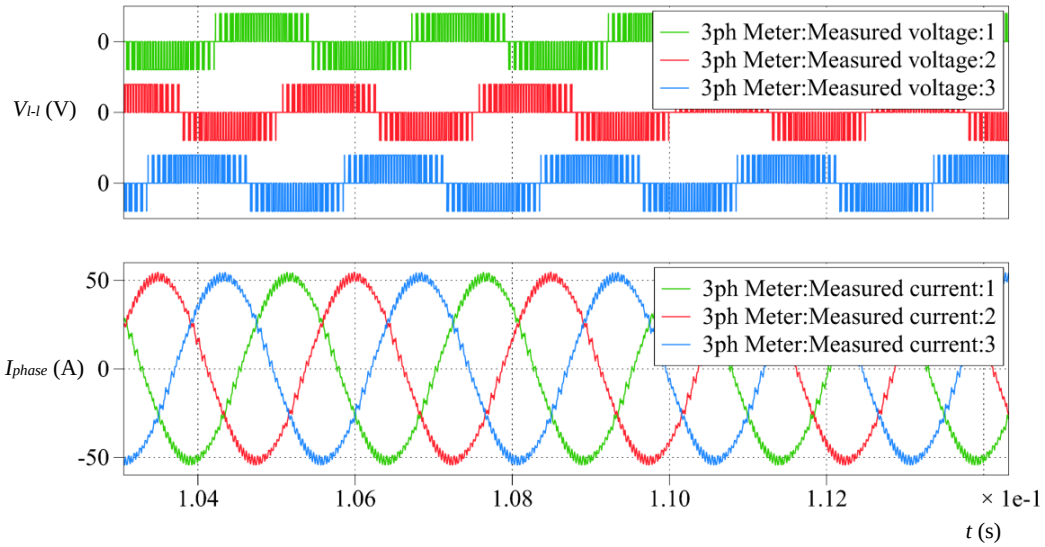


Figure A.5: Output line-line voltages and phase currents.

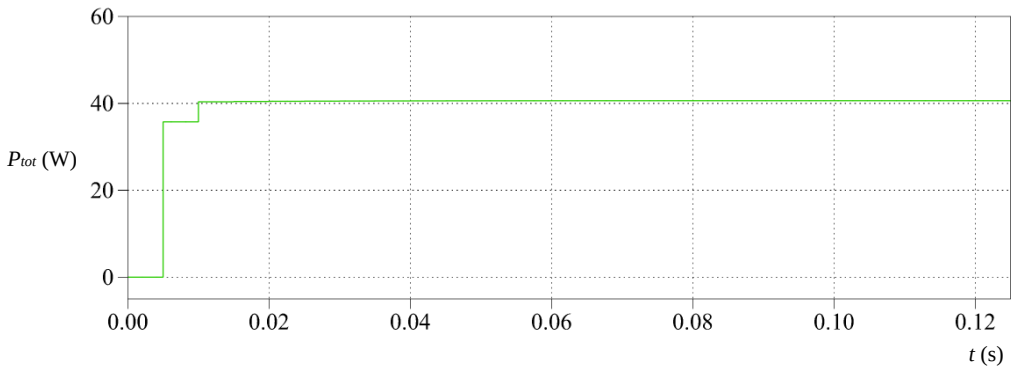


Figure A.6: Total loss of a single die.

Appendix B

SiC MOSFET Die Re-metallization Process

It was discussed in Chapter 6 that re-metallization of the SiC die is essential to achieve nano-silver bondings during the prototyping process of SSM power modules. For the top pads (gate and source) of MOSFETs, the expected new metallization is Ni(0.05 μm)/Au(0.1 μm). A brief introduction of this process was explained in Figure 6.11. Here, details are given. The whole process was taken place in a class 10000 clean-room with ultraviolet light (UV) free lights.

The first step was adding an additional insulation layer to cover the original top surface of the die. Here, a new layer of SiO_2 (0.25 μm) was created through PECVD coating. The equipment was the Technics Micro-PD Series PECVD, as shown in Figure B.1. The main process parameters are listed in Table B.1. And the coated dies are shown in Figure B.2.

The next step was to cover the surface of the die with photoresist by spin coating. Photoresist will protect useful SiO_2 areas from being removed during the following

Figure B.1: Technics Micro-PD Series PECVD.

Table B.1: Process parameters of PECVD

Parameters	Values
Growth conditions (Gas flow)	89 sccm SiH_4 + 69 sccm N_2O (sccm: standard cubic centimeters per minute)
Power	50 W
Total pressure	650 mTorr
Temperature	300^{o}C
Duration	4 min 55 seconds

etching process. The die was first bonded to a Si substrate with a larger surface area, and then they were fixed onto the spinner. This bonding was also achieved by curing the photoresist. After the die was fixed on the spinner, its top surface was spin-coated with a layer of photoresist of about 2.7 μm. Detailed procedures are explained in Table B.2. The spin-coating set-up is shown in Figure B.3.

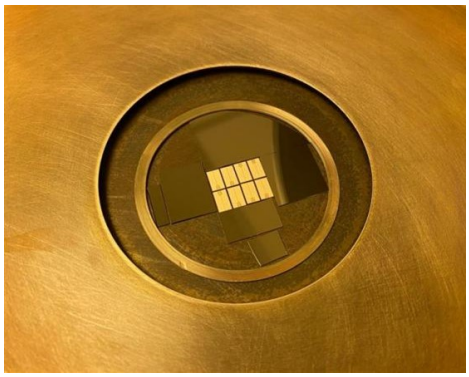


Figure B.2: MOSFET Dies with SiO_2 Coating.

Table B.2: Application notes of spin coating of the photoresist

Procedure	Application Notes
Bond the die on the Si substrate	1) Clean the substrate with Acetone, Methanol, and Deionized (DI) water. And then dry it. 2) Mount the Si substrate on the spinner. 3) Use a syringe to drop S1808 photoresist to cover the entire Si substrate. Make sure all bubbles in the syringe are removed first. 4) Spin it at 500 rpm for 5 seconds for achieving a thin and uniformed coating. 5) Place the die at the center on the substrate. 6) Hard bake the assembly on a hotplate at 130^{o}C for 5 minutes to cure the photoresist bonding.
Coat the die with photoresist	1) Mount the assembly on the spinner again. 2) Use a syringe to drop S1827 photoresist to cover the entire die. Make sure all bubbles are removed in the syringe first. 3) Spin it at 4000 rpm for 30 seconds. 4) Soft bake the assembly on a hotplate at 110^{o}C for 2 minutes to cure the photoresist.

Then, the next part was creating tunnels through to photoresist and SiO_2 layers for accessing the original gate and source pads, as explained in Figure B.4. This part was achieved by three steps: exposure, development, and etching.

As for the localized exposure of the photoresist, the mask aligner photolithography

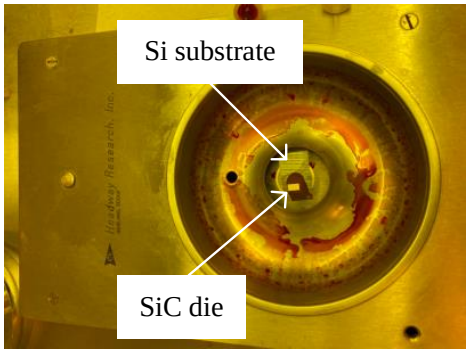


Figure B.3: The SiC die and spinner.

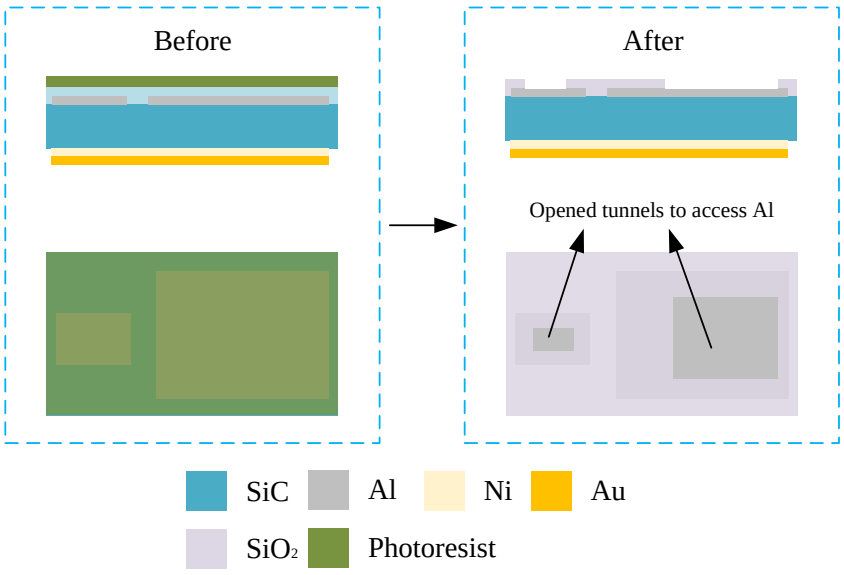


Figure B.4: The concept of creating tunnels through the photoresist and the SiO_2 layers to access original Al pads.

set-up (the Karl Suss MJB-3) was used, as shown in Figure B.5. Dedicated masks were placed on the die to create desired patterns. It was verified that an energy of

150 mJ/cm^2 is required to achieve a complete exposure. Therefore, the sample was exposed under a power of 9.2 mW/cm^2 for 16.3 seconds.

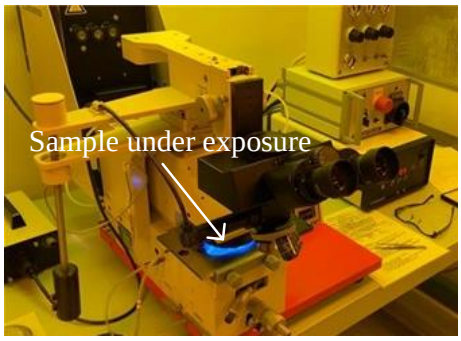


Figure B.5: Sample under exposure in the Karl Suss MJB-3 mask aligner photolithography set-up.

After exposure, the next step was the development, where the photoresist within exposed areas got removed. During the process, the sample was submerged in a beaker containing the development solution (AZ 400K 1:4) for 60 seconds. Then, the sample was cleaned with running DI water. After removing the exposed photoresist, the thickness of the photoresist layer was measured using the Alpha Step Profiler, which verified that the thickness was 2.7 μm, as shown in Figure B.6. And finally, the sample was hard bake at 130^{o}C for 2 minutes to further harden the remaining photoresist.

When the exposed photoresist was removed, the SiO_2 layer in these areas became open. Therefore, to access Al pads beneath them, opened SiO_2 was etched off. During the etching process, the sample was submerged in the etching solution (buffered HF 1:10) for 3.5 minutes. Then, the sample was cleaned with running DI water. After this step, the original Al gate and source pads became accessible. The remaining

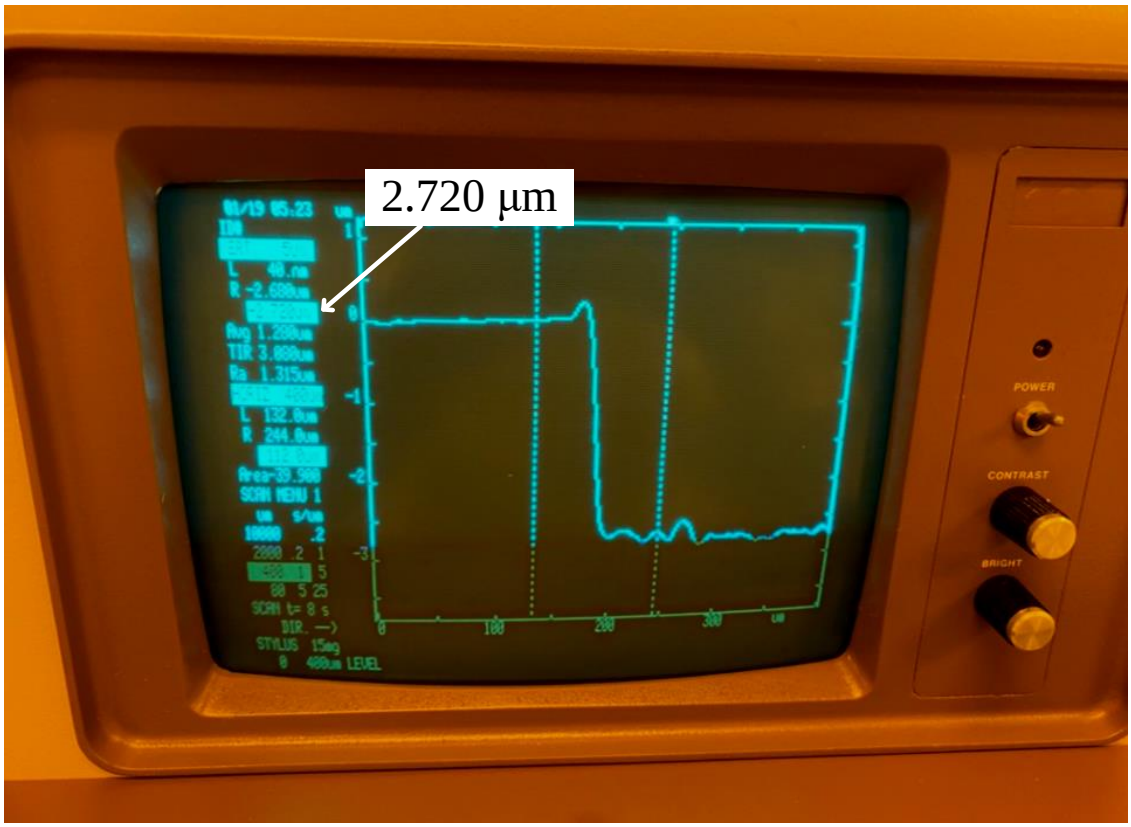


Figure B.6: Photoresist thickness measurement using the Alpha Step Profiler.

photoresist was then fully removed with Acetone, making the sample ready for the following metallization process. The sample was observed under the microscope, where opened areas on top of the original gate pad can be clearly seen, as shown in Figure B.7.

New metallizations (0.05 μm Ni/0.1 μm Au) of the gate and source pads were deposited on the die in the e-beam evaporator, as shown in Figure B.8. Again, the die was covered by a mask during the deposition, so that only certain areas were metallized. After the metallization, the die was separated from the Si substrate by removing the photoresist bonding. Figure B.9 shows the finished sample.

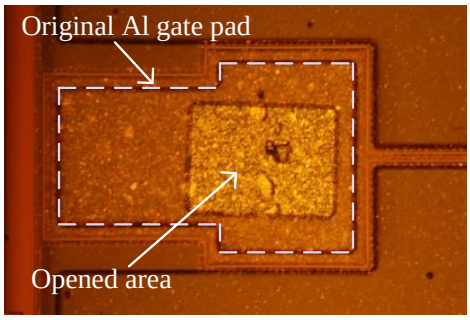


Figure B.7: Opened area on the gate pad.

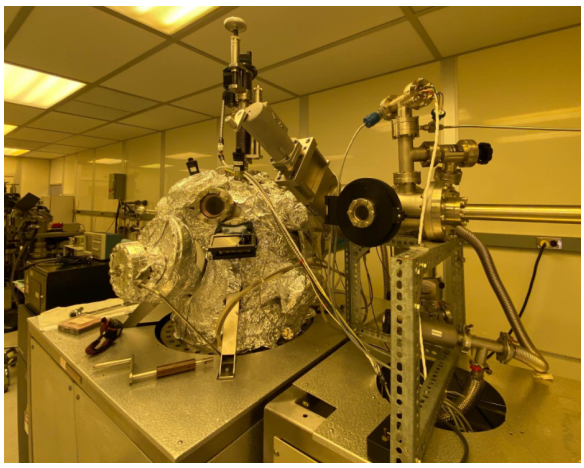


Figure B.8: The UHV e-beam evaporator.

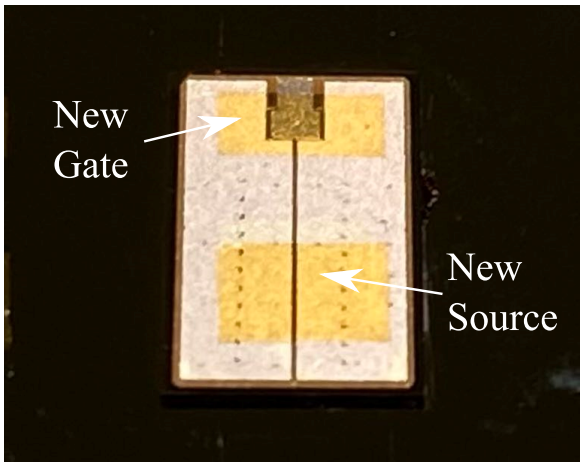


Figure B.9: The finished die.

References

Alam, M. S., Basit, M., Suhling, J. C., and Lall, P. (2016). Mechanical characterization of sac305 lead free solder at high temperatures. In *Proceedings of the 15th InterSociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, ITherm 2016*, pages 755–760, Las Vegas, NV, USA.

Alavi, O., Abdollah, M., and Viki, A. H. (2017). Thermal optimization of igbt modules based on finite element method and particle swarm optimization. *Journal of Computational Electronics*, **16**, 930–938.

Alizadeh, M., Rodriguez, R., Bauman, J., and Emadi, A. (2020). Optimal design of integrated heat pipe air-cooled system using tlbo algorithm for sic mosfet converters. *IEEE Open Journal of Power Electronics*, **1**, 103–112.

Amano, H., Baines, Y., Beam, E., Borga, M., Bouchet, T., Chalker, P. R., Charles, M., Chen, K. J., Chowdhury, N., Chu, R., Santi, C. D., Souza, M. M. D., Decoutere, S., Cioccio, L. D., Eckardt, B., Egawa, T., Fay, P., Freedsman, J. J., Guido, L., Häberlen, O., Haynes, G., Heckel, T., Hemakumara, D., Houston, P., Hu, J., Hua, M., Huang, Q., Huang, A., Jiang, S., Kawai, H., Kinzer, D., Kuball, M., Kumar, A., Lee, K. B., Li, X., Marcon, D., März, M., McCarthy, R., Meneghesso, G., Meneghini, M., Morvan, E., Nakajima, A., Narayanan, E. M., Oliver, S., Palacios,

T., Piedra, D., Plissonnier, M., Reddy, R., Sun, M., Thayne, I., Torres, A., Trivellin, N., Unni, V., Uren, M. J., Hove, M. V., Wallis, D. J., Wang, J., Xie, J., Yagi, S., Yang, S., Youtsey, C., Yu, R., Zanoni, E., Zeltner, S., and Zhang, Y. (2018). The 2018 gan power electronics roadmap. *Journal of Physics D: Applied Physics*, **51**.

AmericanElement (2021). Mo-cu alloy.

Arai, K., Higashi, K., Iiyama, T., Murai, H., Ishikawa, S., and Okubo, T. (2011). High power density motor and inverter for rwd hybrid vehicles. In *SAE 2011 World Congress and Exhibition*, Detroit, MI, USA.

Atelge, M. R. (2016). Power module packaging in automotive applications.

Bahman, A. S., Ma, K., and Blaabjerg, F. (2018). A lumped thermal model including thermal coupling and thermal boundary conditions for high-power igbt modules. *IEEE Transactions on Power Electronics*, **33**, 2518–2530.

Bai, J. G., Calata, J. N., Lei, G., and Lu, G. Q. (2006). Thermomechanical reliability of low-temperature sintered silver die-attachment. *IEEE Transactions on Device and Materials Reliability*, **2006**, 1126–1130.

Bajwa, A. A. (2015). New assembly and packaging technologies for high-power and high-temperature gan and sic.

Basit, M., Ahmed, S., Motalab, M., Roberts, J. C., Suhling, J. C., and Lall, P. (2016). The anand parameters for sac solders after extreme aging. In *Proceedings of the 15th InterSociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, ITherm 2016*, pages 440–447, Las Vegas, NV, USA.

Bayerer, R., Herrmann, T., Licht, T., Lutz, J., and Feller, M. (2008). Model for power cycling lifetime of IGBT modules – various factors influencing lifetime. In *CIPS 2008 - 5th International Conference on Integrated Power Electronics Systems, Proceedings*, pages 37–42, Nuremberg, Germany.

Bouguezzi, S., Ayadi, M., and Ghariani, M. (2016). Developing a simplified analytical thermal model of multi-chip power module. *Microelectronics Reliability*, **66**, 64–77.

Brown, S. B., Kim, K. H., and Anand, L. (1989). An internal variable constitutive model for hot working of metals. *International Journal of Plasticity*, **5**, 95–130.

Buttay, C., Masson, A., Li, J., Johnson, M., Lazar, M., and Raynaud, C. (2011). Die attach of power devices using silver sintering - bonding process die attach of power devices using silver sintering - bonding process optimization and characterization.

Cao, X., Lu, G. Q., and Ngo, K. D. (2012). Planar power module with low thermal impedance and low thermomechanical stress. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **2**, 1247–1259.

Chang, Y., Li, W., Luo, H., He, X., Iannuzzo, F., Blaabjerg, F., and Lin, W. (2019). A 3d thermal network model for monitoring imbalanced thermal distribution of press-pack igbt modules in mmc-hvdc applications. *Energies*, **12**.

ChemetalUSA (2021). Copper tungsten.

Chen, X., Li, R., Qi, K., and Lu, G. Q. (2008). Tensile behaviors and ratcheting effects of partially sintered chip-attachment films of a nanoscale silver paste. *Journal of Electronic Materials*, **37**, 1574–1579.

Chinthavali, M., Wang, Z. J., Campbell, S., Wu, T., and Ozpineci, B. (2018). 50-kW 1kV DC bus air-cooled inverter with 1.7 kV SiC MOSFETs and 3D-printed novel power module packaging structure for grid applications. In *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, pages 133–140, San Antonio, TX, USA. IEEE.

Choudhury, K. R. and Rogers, D. J. (2019). Steady-state thermal modeling of a power module: a n-layer fourier approach. *IEEE Transactions on Power Electronics*, **34**, 1500–1508.

Ciappa, M. (2002). Selected failure mechanisms of modern power modules. *Microelectronics Reliability*, **42**(4-5), 653–667.

Cook, G. O. and Sorensen, C. D. (2011). Overview of transient liquid phase and partial transient liquid phase bonding. *Journal of Materials Science*, **46**, 5305–5323.

CREE WolfSpeed (2019). C3M0016120D Datasheet.

Culham, J. R., Yovanovich, M. M., and Lemczyk, T. F. (2000). Thermal characterization of electronic packages using a three-dimensional fourier series solution. *Journal of Electronic Packaging*, **122**, 233–239.

Dai, Y., Liu, L., and Li, Y. (2011). An intelligent parameter selection method for particle swarm optimization algorithm. In *Proceedings - 4th International Joint Conference on Computational Sciences and Optimization, CSO 2011*, pages 960–964, Kunming and Lijiang City, China.

Darveaux, R. (2002). Effect of simulation methodology on solder joint crack growth correlation and fatigue life prediction. *Journal of Electronic Packaging, Transactions of the ASME*, **124**(3), 147–154.

Evans, T. M., Le, Q., Mukherjee, S., Razi, I. A., Vrotsos, T., Peng, Y., and Mantooth, H. A. (2019). Powersynth: A power module layout generation tool. *IEEE Transactions on Power Electronics*, **34**, 5063–5078.

Gale, W. F. and Butts, D. A. (2004). Transient liquid phase bonding. *Science and Technology of Welding and Joining*, **9**, 283–300.

Grover, F. W. (1962). *Inductance calculations: working formulas and tables*. Dover Publication.

Gurpinar, E., Ozpineci, B., and Chowdhury, S. (2020). Design, analysis, comparison, and experimental validation of insulated metal substrates for high-power wide-bandgap power modules. *Journal of Electronic Packaging, Transactions of the ASME*, **142**.

Han, H. and Song, G. (2015). Automotive power module solution for ev inverter application. In *2015 PCIM Asia*, pages 1–6, Shanghai, China.

Hasnine, M. and Bozack, M. J. (2018). Effects of isothermal aging on the thermal expansion of several sn-based lead-free solder alloys. *Journal of Materials Engineering and Performance*, **27**, 1274–1280.

Held, M., Jacob, P., Nicoletti, G., Scacco, P., and Poech, M. H. (1999). Fast power cycling test for insulated gate bipolar transistor modules in traction application. *International Journal of Electronics*, **86**(10), 1193–1204.

Hou, F., Guo, X., Wang, Q., Wang, W., Lin, T., Cao, L., Zhang, G. Q., and Ferreira, J. A. (2018). High power-density 3D integrated power supply module based on panel-level PCB embedded technology. In *2018 IEEE 68th Electronic Components and Technology Conference (ECTC)*, pages 1365–1370, San Diego, CA, USA. IEEE.

Hou, F., Wang, W., Lin, T., Cao, L., Zhang, G. Q., and Ferreira, J. A. (2019). Characterization of pcb embedded package materials for sic mosfets. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **9**, 1054–1061.

Hou, F., Wang, W., Ma, R., Li, Y., Han, Z., Su, M., Li, J., Yu, Z., Song, Y., Wang, Q., Chen, M., Cao, L., and Zhang, G. (2020). Fan-out panel-level PCB-embedded SiC power MOSFET packaging. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, **8**(1), 367–380.

Hu, B., Ortiz Gonzalez, J., Ran, L., Ren, H., Zeng, Z., Lai, W., Gao, B., Alatise, O., Lu, H., Bailey, C., and Mawby, P. (2017). Failure and reliability analysis of a SiC power module based on stress comparison to a Si device. *IEEE Transactions on Device and Materials Reliability*, **17**(4), 727–737.

Hung, T. Y., Huang, C. J., Lee, C. C., Wang, C. C., Lu, K. C., and Chiang, K. N. (2013). Investigation of solder crack behavior and fatigue life of the power module on different thermal cycling period. *Microelectronic Engineering*, **107**, 125–129.

Infineon Technologies AG (2019). AN2019-05 PC and TC Diagrams. Technical report, Infineon.

Ishihara, M. and Hiyama, K. (2015). Next-generation power module for automotive applications - j1-series. **149**, 7–9.

Jacques, S., Leroy, R., and Lethiecq, M. (2015). Impact of aluminum wire and ribbon bonding technologies on d2pak package reliability during thermal cycling applications. *Microelectronics Reliability*, **55**, 1821–1825.

JEDEC (2020). Power and temperature cycling.

Ji, B., Song, X., Sciberras, E., Cao, W., Hu, Y., and Pickert, V. (2015). Multiobjective design optimization of igbt power modules considering power cycling and thermal cycling. *IEEE Transactions on Power Electronics*, **30**, 2493–2504.

Jiang, G., Diao, L., and Kuang, K. (2013). *Advanced thermal management materials*, volume 53. Springer.

Jones-Jackson, S., Rodriguez, R., Yang, Y., Lopera, L., and Emadi, A. (2022). Overview of current thermal management of automotive power electronics for traction purposes and future directions. *IEEE Transactions on Transportation Electrification*, **8**(2), 2412–2428.

Kennedy, J. and Eberhart, R. (2002). Particle swarm optimization. In *Proceedings of ICNN'95 - International Conference on Neural Networks*, volume 4, pages 1942–1948, Perth, WA, Australia. IEEE.

Knoerr, M., Kraft, S., and Schletz, A. (2010). Reliability assessment of sintered nanosilver die attachment for power semiconductors. In *2010 12th Electronics Packaging Technology Conference, EPTC 2010*, pages 56–61, Singapore.

Lee, H., Smet, V., and Tummala, R. (2020). A review of sic power module packaging technologies: challenges, advances, and emerging issues. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, **8**, 239–255.

Leferink, F. (2002). Inductance calculation: methods and equations. In *Proceedings of International Symposium on Electromagnetic Compatibility*, pages 16–22, Atlanta, GA, USA.

Liang, Z., Ning, P., and Wang, F. (2013). Advanced packaging of sic power module for automotive applications. In *2013 IEEE Energy Conversion Congress and Exposition, ECCE 2013*, pages 2884–2891, Denver, CO, USA.

Ling, J., Xu, T., Chen, R., Valentin, O., and Luechinger, C. (2012). Cu and al-cu composite-material interconnects for power devices. In *Proceedings - Electronic Components and Technology Conference*, pages 1905–1911, San Diego, CA, USA.

Liu, W., An, R., Wang, C., Zheng, Z., Tian, Y., Xu, R., and Wang, Z. (2018). Recent progress in rapid sintering of nanosilver for electronics applications. *Micromachines*, **9**, 1–17.

Löher, T., Allee, G. M., Karaszkiewicz, S., Böttcher, L., and Ostmann, A. (2016). Compact power electronic modules realized by PCB embedding technology. In *2016 IEEE CPMT Symposium Japan (ICSJ)*, pages 2–5, Kyoto, Japan.

Luechinger, C., Chen, R., Fu, J., Poncelet, B., Valentin, O., Walker, T. J., and Xu, T. (2017). Aluminum-copper ribbon interconnects for power devices. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **7**, 1567–1577.

Luedtke, A. (2004). Thermal management materials for high-performance applications.

Manfred Goetz (2018). Silicon Nitride Substrates for Improved Performance in Power Electronics.

Manikam, V. R. and Cheong, K. Y. (2011). Die attach materials for high temperature applications: A review. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **1**, 457–478.

Masana, F. N. (1996). A closed form solution of junction to substrate: thermal resistance in semiconductor chips. *IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part A*, **19**, 539.

Masataka, H., Kohei, S., Hisashi, M., Yoshinao, K., Akinori, K., Akito, K., Takekazu, M., and Shigenobu, Y. (2016). Recent progress in ga2o3 power devices. *Semiconductor Science and Technology*, **31**, 34001.

McPherson, B. and Lostetter, A. (2019). High power multilayer module having low inductance and fast switching for paralleling power devices.

MGC (2022). Non-haloganated low cte bt resin laminate for ic plastic packages.

Miyazaki, H., Zhou, Y., Iwakiri, S., Hirotsuru, H., Hirao, K., Fukuda, S., Izu, N., and Hyuga, H. (2018). Improved resistance to thermal fatigue of active metal brazing substrates for silicon carbide power modules using tough silicon nitrides with high thermal conductivity. *Ceramics International*, **44**, 8870–8876.

Monier-Vinard, E., Laraqi, N., Dia, C. T., Nguyen, M. N., and Bissuel, V. (2013). Analytical thermal modelling of multilayered active embedded chips into high density electronic board. *Thermal Science*, **17**, 695–706.

Morancho, F. (2008). State of the art and trends in power semiconductor devices for optimized power management.

Munro, R. G. (1997). Evaluated material properties for a sintered-alumina. *Journal of the American Ceramic Society*, **80**, 1919–1928.

NBE (2019). Applications of nbe's nanotach.

Niu, H. (2017). A review of power cycle driven fatigue, aging, and failure modes for semiconductor power modules. In *2017 IEEE International Electric Machines and Drives Conference, IEMDC 2017*, Miami, FL, USA.

Pahinkar, D. G., Puckett, W., Graham, S., Boteler, L., Ibitayo, D., Narumanchi, S., Paret, P., DeVoto, D., and Major, J. (2018). Transient liquid phase bonding of aln to alsic for durable power electronic packages. *Advanced Engineering Materials*, **20**, 1800039(1–9).

Parker, E., Narveson, B., Alderman, A., and Burgyan, L. (2015). Embedding active and passive components in PCBs and inorganic substrates for power electronics. In *IEEE International Workshop on Integrated Power Packaging, IWIPP 2015*, pages 107–110, Chicago, IL, USA. IEEE.

Plansee (2022). Molybdenum properties.

Qian, C., Gheitaghy, A. M., Fan, J., Tang, H., Sun, B., Ye, H., and Zhang, G. (2018). Thermal management on IGBT power electronic devices and modules. *IEEE Access*, **6**, 12868–12884.

Reimers, J., Dorn-gomba, L., Mak, C., and Emadi, A. (2019). Automotive traction inverters: current status and future trends. *IEEE Transactions on Vehicular Technology*, **68**, 3337–3350.

Riedel, G. J., Schmidt, R., Liu, C., Beyer, H., and Alaperae, I. (2012). Reliability of large area solder joints within IGBT modules: numerical modeling and experimental results. In *2012 7th International Conference on Integrated Power Electronics Systems, CIPS 2012*, volume 1, pages 1–6, Nuremberg, Germany.

Sato, Y., Ishikawa, S., Okubo, T., Abe, M., and Tamai, K. (2011). Development of high response motor and inverter system for the nissan leaf electric vehicle. In *SAE 2011 World Congress and Exhibition*, Detroit, MI, USA.

Scheuermann, U. and Schmidt, R. (2013). Impact of load pulse duration on power cycling lifetime of Al wire bonds. *Microelectronics Reliability*, **53**(9-11), 1687–1691.

Schwarzbauer, H. and Kuhnert, R. (1989). Novel large area joining technique for improved power device performance. In *Conference Record of the IEEE Industry Applications Society Annual Meeting*, San Diego, CA, USA.

Schweitzer, D., Pape, H., and Chen, L. (2008). Transient measurement of the junction-to-case thermal resistance using structure functions: chances and limits. In *Annual IEEE Semiconductor Thermal Measurement and Management Symposium*, pages 191–197, San Jose, CA, USA.

Sharma, A. B., Paul, D., Kreck, M., Rahmoun, Y., Anders, P., Gruber, M., and Huesgen, T. (2016). PCB embedded power package with reinforced top-side chip contacts. In *2016 6th Electronic System-Integration Technology Conference (ESTC)*,

pages 1–5, Grenoble, France. IEEE.

Siow, K. S. (2019). *Die-attach materials for high temperature applications in microelectronics packaging: Materials, processes, equipment, and reliability*. Springer International Publishing.

Siow, K. S. and Lin, Y. T. (2016). Identifying the development state of sintered silver (ag) as a bonding material in the microelectronic packaging via a patent landscape study. *Journal of Electronic Packaging, Transactions of the ASME*, **138**, 020804(1–13).

Smet, V., Forest, F., Huselstein, J. J., Richardeau, F., Khatir, Z., Lefebvre, S., and Berkani, M. (2011). Ageing and failure modes of IGBT modules in high-temperature power cycling. *IEEE Transactions on Industrial Electronics*, **58**(10), 4931–4941.

Spenke, R. and Khalid, H. (2019). Automotive high capacity power module.

Sun, Y., Kang, X., Zheng, Y., Lu, J., Tian, X., Wei, K., Wu, H., Wang, W., Liu, X., and Zhang, G. (2019). Review of the recent progress on gan-based vertical power schottky barrier diodes (sbds). *Electronics*, **8**.

Swan, I., Bryant, A., Mawby, P. A., Ueta, T., Nishijima, T., and Hamada, K. (2012). A fast loss and temperature simulation method for power converters, part ii: 3-d thermal model of power module. *IEEE Transactions on Power Electronics*, **27**, 258–268.

Székely, V. (1998). Identification of RC networks by deconvolution: chances and

limits. *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, **45**(3), 244–258.

Trelea, I. C. (2003). The particle swarm optimization algorithm: convergence analysis and parameter selection. *Information Processing Letters*, **85**, 317–325.

U.S.Dept.Energy (2017). Us drive electrical and electronics technical team roadmap.

Vagnon, E., Jeannin, P. O., Crébier, J. C., and Avenas, Y. (2010). A bus-bar-like power module based on three-dimensional power-chip-on-chip hybrid integration. *IEEE Transactions on Industry Applications*, **46**, 2046–2055.

Wada, K., Hino, A., and Ando, M. (2013). High-speed analysis of bus bar inductance for a laminated structure. *IEEJ Journal of Industry Applications*, **2**, 189–194.

Wang, H., Liserre, M., and Blaabjerg, F. (2013). Toward reliable power electronics: challenges, design tools, and opportunities. *IEEE Industrial Electronics Magazine*, **7**, 17–26.

Wang, M., Mei, Y., Li, X., Burgos, R., Boroyevich, D., and Lu, G. Q. (2018). How to determine surface roughness of copper substrate for robust pressureless sintered silver in air. *Materials Letters*, **228**, 327–330.

Wang, T., Chen, X., Lu, G. Q., and Lei, G. Y. (2007). Low-temperature sintering with nano-silver paste in die-attached interconnection. *Journal of Electronic Materials*, **36**, 1333–1340.

Wendl, M. C. (2012). *Theoretical foundations of conduction and convection heat transfer*. The Wendl Foundation.

Wolfgang, S. and Krebs, T. (2019). Adjust the mechanical properties of sintered silver layers using additives. In *CIPS 2016 - 9th International Conference on Integrated Power Electronics Systems*, pages 1–7, Nuremberg, Germany.

Xia, Z., Shi, Y., and Chen, Z. (2002). Evaluation on the characteristics of tin-silver-bismuth solder. *Journal of Materials Engineering and Performance*, **11**, 107–111.

Xiaoyu, H., Xiangjun, Z., Xu, Y., and Zhaoan, W. (2006). A hybrid integrated power electronic module based on pressure contact technology. In *PESC Record - IEEE Annual Power Electronics Specialists Conference*, Jeju, South Korea.

Yan, J., Zou, G., Wu, A. P., Ren, J., Yan, J., Hu, A., and Zhou, Y. (2012). Pressureless bonding process using ag nanoparticle paste for flexible electronics packaging. *Scripta Materialia*, **66**, 582–585.

Yang, Y., Dorn-Gomba, L., Rodriguez, R., Mak, C., and Emadi, A. (2020). Automotive power module packaging: current status and future trends. *IEEE Access*, **8**, 160126–160144.

Yang, Y., Hefny, M., Noronha, K., Callegaro, A., Goykhman, M., Baronian, A., and Emadi, A. (2021). A fast and accurate thermal-electrical coupled model for sic traction inverter. In *2021 IEEE Transportation Electrification Conference and Expo, ITEC 2021*, pages 496–501, Chicago, IL, USA.

Yannou, J.-M. and Avron, A. (2012). Analysis of innovation trends in packaging for power modules. In *7th European Advanced Technology Workshop on Micropackaging and Thermal Management*, pages 22–25, San Diego, CA, USA.

Yin, L., Nagarkar, K., Kapusta, C., Tuominen, R., Gowda, A., Hayashibe, S., Ito, H., and Arai, T. (2017). POL-kW modules for high power applications. In *Proceedings - Electronic Components and Technology Conference*, pages 1497–1503, Orlando, FL, USA. IEEE.

Yole.Developpement (2020). Power module packaging : Ev / hev changes the rules of game.

Yoon, J. W., Back, J. H., and Jung, S. B. (2018). Effect of surface finish metallization on mechanical strength of ag sintered joint. *Microelectronic Engineering*, **198**, 15–21.

Yoon, S. W., Glover, M. D., Mantooth, H. A., and Shiozaki, K. (2013). Reliable and repeatable bonding technology for high temperature automotive power modules for electrified vehicles. *Journal of Micromechanics and Microengineering*, **23**, 015017(1–12).

Yu, D., Chen, X., Chen, G., quan Lu, G., and qiang Wang, Z. (2009). Applying anand model to low-temperature sintered nanoscale silver paste chip attachment. *Materials and Design*, **30**, 4574–4579.

Zhang, H. (2014). High temperature ltcc based sic double-sided cooling power electronic module.

Zhang, H., Yang, H., Zhou, M., and Tsui, A. C. (2007). Aluminum ribbon bonding technology in a new package of high power and thermal performance. In *Proceedings of the Electronic Packaging Technology Conference, EPTC*, volume 00, pages 25–27, Shanghai, China.

Zhu, N., Mantooth, H. A., Xu, D., Chen, M., and Glover, M. D. (2017). A solution to press-pack packaging of sic mosfets. *IEEE Transactions on Industrial Electronics*, **64**, 8224–8234.

Zou, G., Yan, J., Mu, F., Wu, A., Ren, J., and Hu, A. (2014). Low temperature bonding of cu metal through sintering of ag nanoparticles for high temperature electronic application. *The Open Surface Science Journal*, **3**, 70–75.