Power Electronic Architectures for Solar-Charged Electric Vehicles

Power Electronic Architectures for Solar-Charged Electric Vehicles

by

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Abstract

Anthropogenic climate change, resulting from drastic exploitation of fuel sources like gas and oil, has caused global warming as the most evident sign of releasing greenhouse emissions. One of the possible solutions is employing renewable energies. Renewable energy sources like photovoltaic (PV) cells and wind are emission free during operation. Electric vehicles (EVs) are the leading solution to the rising air pollution from the transportation sector; however, their deployment has been slow due to cost, range, and charging issues. One promising solution is to use the solar panel as an on-board source to partially charge the EV's battery. However, there are some obstacles in developing on-board solar generation for EVs, mainly the PV-steel integration process, including concerns of cost, mass, efficiency, and durability, and the power electronic architecture cost, efficiency, and size/mass. This thesis focuses on designing optimal power electronic architectures for on-board solar generation. One main challenge is that the PV voltage is often low, and thus a high voltage gain is required to step up this voltage to that of the high-voltage EV traction battery.

The first contribution of this thesis the proposal of a high step-up DC-DC converter with low input voltage ripple. This feature is important because having lower current ripple from solar cells helps to improve their reliability and performance. An experimental prototype validates the circuit theory. The second contribution is the proposal of a novel generalized methodology for switched-capacitor high step-up converters including coupled inductors and voltage multiplier cells, which are applicable in solar-charged EVs that do not require electrical isolation between the solar array and the high voltage battery. The

generalized method can be used to design for the voltage gain required of any application with a minimum number of components. To illustrate the method, a novel high step-up converter is designed, built, and tested. The third contribution is the design of an integrated on-board solar charger including a flying capacitor active rectifier. The active rectifier is a reconfigurable topology which can act as the inverter for the motor drive when the EV is driving. This concept reduces the size and the number of components compared to a non-integrated approach.

Next, the thesis considers how to best incorporate electrical isolation in the solar-charged EV power electronic architecture, if it is desired. Firstly, two power electronics interfaces for a solar-charged EV are simulated and investigated, one isolated and the other non-isolated, so that efficiency and component count can be compared. A model of a solar-charged Chevrolet Bolt is created to use as a simulation platform for comparing the isolated and non-isolated power electronics designs. Lastly, a novel isolated three-port converter is proposed for interfacing the solar arrays, low voltage battery, and high voltage battery. Electrical isolation is present between the high voltage battery and the other two ports. The performance of the converter is improved by employing differential power processing converters which will process only the power difference between the solar arrays. The proposed circuit has a low component count compared to a non-integrated approach. Overall, this thesis presents four novel power electronic topologies that can be used in solar-charged EVs. Though the focus in this thesis is the solar-charged EV application, the first two contributions can be applied to a variety of applications and represent general advances in the field of high step-up converters.

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Chapter 1

Introduction

1.1 Background and Motivations

Anthropogenic climate change, resulting from drastic exploitations of fuel sources like gas and oil, has caused global warming as the most evident sign of releasing greenhouse emissions. About 22% of global greenhouse gas emissions are caused by transportation (37% in the US, 28% in Canada) [1]. One of the possible solutions is employing renewable energy generation. Renewable energy like photovoltaic (PV) and wind are emission free during operation and thus more environmentally friendly. Development of these resources can improve the situation for the environment, and also, they can be a sustainable energy source for humankind, for all traditional fuel sources are exhaustible [1-2].

As mentioned, a great portion of air pollution is related to the transportation sector. Electric vehicles (EVs) are the leading solution to this problem; however, their deployment has been slow due to cost, range, and charging issues. Although EVs are more efficient than internal combustion engine (ICE) vehicles, they can produce nearly as much pollution as ICE vehicles do if the electricity is generated by coal. In addition, EV charging during peak hours adds demand to the grid; by doing so, it can decrease the lifetime of distribution transformers in neighborhoods with high EV penetration rates [3-7].

One potential solution to these EV challenges is to add on-board solar generation to the vehicle, where the EV traction battery acts as the built-in energy storage often needed for intermittent renewable energy sources like solar. At the system level, it is proposed to integrate thin PV cells onto all upward-facing vehicle body panels (hood, roof, and trunk). This is a game-changing difference from a small vehicle roof-top PV panel because this much larger PV area can produce enough electricity to significantly increase EV range and

reduce grid recharging power. Figure 1-1 shows an example of on-board solar generation in a prototype Toyota Prius Prime [8]. There are two main challenges for developing on-board solar generation: 1) the PV-steel integration process (efficiency, cost, mass, durability, etc.), and 2) developing an optimal power electronic architecture to transfer the low-voltage solar power to the high-voltage traction battery. This thesis focuses on the power electronic architecture challenge, with the goals of low component count and high efficiency.

Figure 1-1: Prototype EV with on-board solar generation [8]

There are two main advancements that have paved the way for the development of integrating solar arrays on electric vehicles: high-speed power switches and high efficiency solar arrays. Regarding the first advancement, with the advent of high speed and highly efficient power semiconductors, power conversion can be done with higher efficiency and smaller size. Silicon Carbide (SiC) and Gallium Nitride (GaN) power transistors can operate at high frequency, so the size of inductors and capacitors reduce considerably [10]. With small capacitors the use of film/thin-film capacitors are possible, which results in more reliable structures and a higher lifetime of capacitive storage.

In addition, there has been a great improvement in photovoltaic (PV) cell technology which can provide an energy conversion efficiency of 26.7% for the highest efficiency silicon monocrystalline cells [11], with record 1-sun efficiencies of 38.8% for laboratory demonstrations of multijunction cells [12]. Most notably for EVs, the recent advances have created flexible thin-film cells with efficiencies in excess of 20% [13]. Solar deployment has been increasing worldwide, particularly in utility-scale deployments; however, its impact at the individual level (residential rooftop solar) has been slow due to the large upfront cost for installation (e.g., $23 000 for a 7.5-kW system) [14].

As an example of recent developments in this area, the Toyota Prius Prime and the Karma Revero both have solar cells integrated into the roof, which charge the propulsion battery [15], [16]. Hyundai introduced the Ioniq5 in 2022, an EV with a solar-powered range extender and claims extra solar range of ~2000Km per year [17]. Furthermore, the Sion EV, manufactured by Sono Motors GmbH, has solar panels fixed onto all vehicle body panels to provide electric range extension [18]. A detailed modeling study in [19] has shown that the annual net energy reduction of a large-scale SEV (with solar arrays on the upwards-facing vehicle surfaces of the hood, roof, and truck) would be 21.5% in Los Angeles and 17.5% in Detroit.

With regards to electricity transmission and distribution for EV charging, the losses and load limitations must be considered. There is an average of 12% loss in energy from large generating stations to local residential loads [20], so for EV charging, it means that the EV is actually consuming 12% more generated energy than the energy used to drive the vehicle. Furthermore, most of the grids present today were not designed for EV charging. Much

research has investigated this issue, and a primary concern of having an increasing number of EVs plugging into the grid to charge is the overloading of distribution transformers [21]–[22]. Large-scale SEVs can help with both these problems, as the solar energy is generated very close to where it is required, and grid EV charging can be reduced. According to [19], for large-scale SEVs, in average cloud conditions, the annual vehicle energy consumption is reduced by 21.5% in LA and 17.5% in Detroit.

In terms of EV range extension, the full-scale SEV concept can be considered as a type of wireless charging solution, using free and clean solar energy to charge the battery when driving or parked anywhere outside. Although much research has been conducted on dynamic wireless charging through the road, obstacles remain including enormous infrastructure investment needed to retrofit roads, and peak driving times often coincide with afternoon peak grid loads [23], [24], meaning that new generation could be needed, local grid generation mix might not guarantee low CO_2 driving, and grid transmission losses (about 12%) still exist. In [19], simulation is done on the average daily per-driver solar range extension for Los Angeles (LA) and Detroit. Results shows, in average cloud conditions, a solar range extension of at least 15 km in LA can be seen yearly. Also, for a northern city like Detroit, in average cloud conditions, 8 months of the year give a solar range extension of at least 15 km. On an annual average, the daily solar range extensions for LA are 30 km for full sun, 26 km for average cloud conditions. On an annual average, the daily solar range extensions for Detroit are 29 km for full sun, 20 km for average cloud conditions.

From the perspective of vehicle efficiency, automotive engineers spend much effort to increase EV efficiencies by a few percentages: aerodynamic improvements, more efficient motors, and power electronics, and there are diminishing returns in these areas for the current generation of highly efficient EVs. However, the proposed full-scale SEV can reduce charging needs by about 20% on average, depending on driving scenarios, which is analogous to an increase in efficiency of 20% [19].

1.2 Contributions

This thesis investigates the power electronics interface of SEVs. The efficiency, power density and cost are the prominent factors which are being investigated in the system. Different isolated and non-isolated topologies are investigated for these purposes, as isolated topologies may be desired for safety concerns with respect to the high voltage battery, yet non-isolated topologies offer advantages of lower cost and size, and potentially higher efficiency due to the lack of a transformer. Since there is not yet industry agreement on whether isolation is required, both options are investigated in this thesis.

The first contribution of this thesis is a novel non-isolated high step-up converter with low input current ripple [25]. The characteristics of low input current ripple and high voltage step-up are well-matched to the needs of a SEV, since high PV current ripple can negatively affect PV performance and maximum power point tracking algorithms. The improved input current ripple reduces additional filtering needs for PV or fuel cell sources. Also, the circuit provides a high voltage gain of 8-11 (for a 450 V battery pack) at high efficiency, and low component count. Furthermore, the integration of the secondary side

winding of the coupled inductor with the switch-capacitor (SC) cell prevents high voltage spikes on the switch during turn-off.

The second contribution of this thesis is a novel generalized methodology for designing high step-up converters [26]. The paper presents a novel generalized method to derive the voltage gain of boost-based converters using switch capacitor (SC), couple inductor (CI), and voltage multiplier cells (VMC) techniques. The proposed generalized method uniquely reveals the unifying theory underlying boost-based converters with any variation of SC/CI/VMC (with one switch and one CI core) and requires only four equations for gain. No previously published theories can describe the gain of such a wide variety of converter topologies with so few equations. The proposed generalized method provides a deeper comprehension of these applied techniques, allowing for improved designs that make the best possible use of their active and passive devices to achieve the highest voltage gain. Thus, this paper's new perspective on high step-up converter design can lead to more optimal converters in terms of cost and efficiency. As an example of this process, this research presents a novel integrated SC-CI converter designed using the proposed generalized method and compares it to other high step-up converters from the literature using a loss breakdown analysis and component stress factor (CSF) analysis. The high step-up converters designed using the generalized method can be used in SEVs or in other applications that require high voltage gain.

The third contribution of this thesis is the design of an integrated on-board solar charger [28]. This research proposes a novel integrated electric architecture for SEVs which relies on a flying capacitor topology for both battery charging and driving the motor. The

on-board solar energy is used to solve the common problem of balancing the flying capacitors, which at the same time helps the solar voltage boost problem since the solar power no longer needs to be boosted to the full battery voltage.

The fourth contribution of this thesis is the investigation of the efficiency and cost of two proposed electrical architectures for use in SEVs using four different converters, two which are isolated, and two which are non-isolated [29]. Detailed PLECS efficiency results are added to a vehicle model to investigate the efficiency during a real drive cycle with multiple solar radiation profiles. Also, the efficiency of these structures are compared for the same operating condition, and a cost analysis is performed to ease the choosing of the best structure based on a cost-efficiency tradeoff.

The fifth contribution of this thesis is the proposal of a SC-based multiport converter with integrated differential power processing (DPP) for solar power processing during partial shading, which also has electrical isolation in the path to a high voltage load, suitable for an EV traction battery [27]. The third port connects to a nominal 12 V load, representing the vehicle's low voltage electrical accessories. Furthermore, the proposed topology achieves zero-voltage switching (ZVS) at the primary side and zero-current switching (ZCS) at the secondary side even at low load, resulting in high efficiency.

1.3 Publications

This thesis is written in the "Sandwich Thesis" format, where each of chapters three to seven are based on a conference or journal paper. These papers keep the main content intact but have a slightly modified structure to comply with the format of the thesis. Chapters 3,

4, and 7 are related to three journal papers [25] – [27] and Chapters 5 and 6 are related to two conference papers [28], [29].

1.3.1 Journal Publications

[25] D. Sadeghpour and J. Bauman, "High-Efficiency Coupled-Inductor Switched-Capacitor Boost Converter with Improved Input Current Ripple," in IEEE Transactions on Industrial Electronics, vol. 69, no. 8, pp. 7940-7951, Aug. 2022.

[26] D. Sadeghpour and J. Bauman, "A Generalized Method for Comprehension of Switched-Capacitor High Step-Up Converters Including Coupled Inductors and Voltage Multiplier Cells," in IEEE Transactions on Power Electronics, vol. 37, no. 5, pp. 5801-5815, May 2022.

[27] D. Sadeghpour and J. Bauman, “Integrated Three-Port Converter for PEV Applications," submitted to IEEE Transactions on Industrial Electronics, December 2022.

1.3.2 Conference Publications

[28] D. Sadeghpour, and J. Bauman, " Novel Integrated Electrical Architecture for Solar-Charged Electric Vehicles," IEEE Transportation Electrification Conference & Expo, California, USA, 2022

[29] D. Sadeghpour and J. Bauman, "Investigation of Power Electronic Architectures for Solar Electric Vehicles," IEEE Transportation Electrification Conference & Expo, Chicago, USA, pp. 1227-1233, 2020.

An additional conference publication, not directly related to this thesis, is:

[30] J. Dong, D. Sadeghpour, and J. Bauman, " High Efficiency GaN-based Non-isolated Electrical Vehicle On-board Charger with Active Filtering," IEEE Transportation Electrification Conference & Expo, California, USA, 2022.

1.4 Outline of the Thesis

This thesis is organized into eight chapters. Chapter 1 has given the background and motivation for the design of power electronic architectures for SEVs. Chapter 2 reviews basic power electronic converters that can be of use in developing SEV power electronic architectures. The topologies are analyzed based on advantages and disadvantages, or potential for improvements. Some of the topologies have shown superior performance over others and have been used as part of the proposed topologies in this thesis. Chapter 2 also includes a review of some of the DPP techniques to extract the PV maximum power in case of PV module shading.

Chapter 3 proposes a high step-up topology with low current ripple at the PV side. The converter shows high efficiency and power density. A pulsating current drawn from PV arrays will negatively affect the PV performance, so the proposed circuit reduces the need for additional filtering to be added. Experimental results validate the theory of the circuit.

Chapter 4 proposes a generalized methodology of designing high step-up DC-DC converters. Different methodologies are investigated in the literature. The methodology starts from basic switched-capacitor structures and continues in coupled-inductor techniques and voltage multiplier cell characteristics and their respective effects on the voltage gain and cost of the converters. Also, in this chapter a proposed converter is

investigated, and the experimental results are presented. The efficiency analysis, design process, and dynamic behavior of this converter are presented.

Chapter 5 proposes an integrated non-isolated solar charged on-board charger and completes topology validation in PLECS (electronic circuit simulation software) and Simulink. The electrical component models have been modified to match the real components, especially the GaN E-HEMTs. Simulation results including efficiency, power factor (PF), and total harmonics distortion (THD) are presented.

Chapter 6 investigates the performance of the well-known isolated and non-isolated DC-DC converters applicable for the large-scale SEV concept. In this study, two design option are proposed and investigated, and the state of charge (SOC) of the traction battery for a certain driving pattern and daily solar radiation is closely monitored to see the effect of the different converters in a SEV.

Chapter 7 focuses on an isolated design and proposes a novel integrated isolated three-port converter for use in SEVs. The design process and control scheme are presented. In addition, different modes are devised and discussed in detail. The experimental design and results are shown, and different features such as efficiency, zero voltage switching, and decoupled control of all ports are validated through experimental results. Chapter 8 gives the summary and future work and provides a path for future research and challenges for this topic.

1.5 References

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Chapter 2

Review of Power Electronic Converters Applicable in Solar Charged Vehicles

In a SEV, a path needs to be created to charge the high voltage traction battery (HVB) which varies from 250-400V, or low voltage battery (LVB), which has a nominal voltage of 12V, from the solar arrays integrated on the surface of the EV. In electric vehicles, the onboard charger (OBC) has the role of charging the HVB from the grid. The OBC generally contains an ac-dc converter for interfacing the grid and another high gain dc-dc converter for interfacing the battery. The most general topologies for OBCs may consist of three stages. The front stage consists of a diode rectification, the second stage is the power factor correction (PFC), and the third stage comprises of the dc–dc conversion. The first step in designing an optimum solar assisted charger will be a deep understanding of OBCs.

2.1 DC-DC Converter

The DC-DC stage converts the incoming DC link voltage to a specific DC voltage to charge the battery of an EV. The DC-DC converter must be capable of delivering rated power to the battery over a wide range with the capability of charging the battery at constant current and at constant voltage mode, depending on the state of charge (SOC) of the battery.

In a SEV, the harvested power from the solar arrays must be employed to charge the battery over a wide voltage range. The solar charger can be added to EVs by adding it as a separate modular system to charge the HVB, without changing the existing systems, or integrating with the existing EV chargers. This can be done by integrating with the rectifier stage or DC-DC stage. The following sections review isolated and non-isolated converters that can be considered for use in SEV power electronic architectures.

2.2 Non-Isolated DC-DC Converters

2.2.1 High Step-up Converters

When connecting PV cells to a higher voltage level a significant voltage boost is required. The conventional boost converter is not suitable for high step-up applications because parasitic losses at high duty cycles degrade the output voltage and efficiency. Also, switch and diode voltage stress are high which increases the cost and degrades the efficiency. To tackle this, different high step-up techniques are proposed in the literature [1-6]. Among which, switched capacitor structures are a promising solution as they increase the power density of the converter and reduce the switch/diode voltage stress. But this technique suffers from high diode reverse recovery losses, high number of components and cost. Integrating with coupled inductors reduces the high number of switched-capacitor pairs for achieving high step-up voltage gains and alleviates the reverse recovery losses [7-8].

2.2.2 Differential Power Processing Converters

Other than voltage conversion requirements for solar modules, maximum power harvesting is another point that needs to be addressed. The current produced by a solar module is dependent on the irradiance and the temperature of the surrounding environment. The solar panels can have a MPPT DC-DC converter per module [9-11]. These configurations, which are called “DC optimizer” structures can be implemented with DC-DC converters. In addition to the extra cost and complexity, it introduces additional losses to the system as these converters process the entire solar power. Differential power

processing converters are introduced to improve the cost and efficiency of DC optimizers. These converters are placed in parallel with each two modules in a string and only process the differential power between two ports at a time. Accordingly, the number of components and power losses are reduced, and efficiency is improved [12-14]. Based on the literature, there are four different types of DPP converters: 1- Buck-Boost converter 2- Multistage choppers 3- Switched capacitor 4- Multi-winding flyback converters [12-14]. These converters are shown in Figure 2-1.

Converters proposed in [15-19] are the DPP converters investigated for MPPT and tackling of the shading effects. Scalability, high power density, and high efficiency of switched capacitor structures motivates DPP designers to use SC converters. [9,12] use the SC voltage multiplier structure with LLC resonant converter to achieve MPPT and regulation of the output voltage. High efficiency and high-power density of the structure makes it a prominent candidate for solar based topologies. [13] uses the same structure as [9,12] added by a voltage divider stage to make it applicable for curved PV modules on rooftop electric vehicle systems. In addition to other advantages, it can find the global MPP. Another approach is investigated in [10]. A SC voltage multiplier structure followed by Quasi-Z-Source inverter structure (qSI) is proposed. Although the boost ratio is increased, the shoot through state of qSI introduces freewheeling current which can increase the conduction losses and lower the efficiency. [11] propose a multi-stacked buck-boost structure.

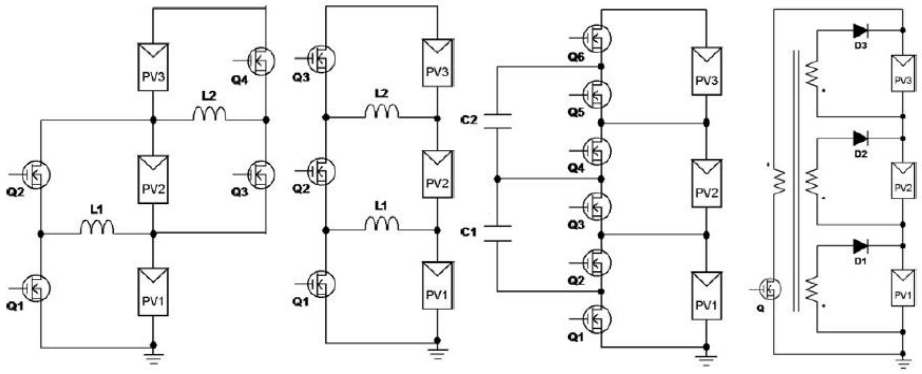

Figure 2-1: Different DPP Topologies a) Buck-Boost Converter b) Multistage choppers c) Switched Capacitor d) Multi-winding Flyback [9]

2.3 Isolated Converters

This section explores four different topologies of high-power DC-DC converters: namely the LLC resonant converter, the Phase-shifted Full Bridge (PSFB), Single-phase Dual-Active Bridge (DAB) and the Dual-Active, Bridge in CLLC mode (DAB – CLLC).

2.3.1 PSFB

Figure 2-2 shows the basic topology of the phase shifted full bridge converter. The phase shifted full bridge belongs to the family of Dual Active Bridge converters where the active switches on the secondary are replaced with diodes. Due to this, it allows only unidirectional power transfer.

The power transfer between the primary and secondary is controlled by varying the phase between the switch legs of the primary bridge. As a result, it is possible to obtain ZVS turn on of one leg and low voltage turn on of the other leg minimizing losses. The passive diodes on the secondary can experience hard switching and result in more conduction losses which can reduce the efficiency of this converter.

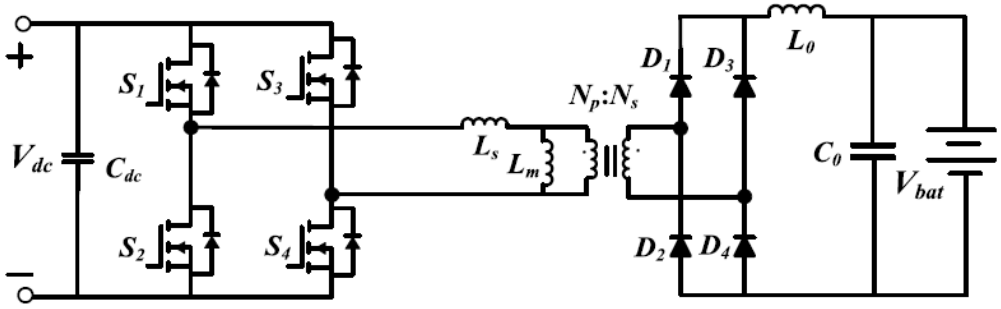

Figure 2-2: Phase-shifted full-bridge converter [20]

This converter suffers non ZVS turn on loss at light load condition and non ZVS turn off. Typically burst mode of operation is used to maintain ZVS at light load condition. This converter is also modular, and it can be paralleled to obtain higher power throughput in EV charging stations [20]. In PSFB, dithering can be easily implemented to reduce the conducted EMI signature. This topology requires a DC blocking capacitor which is needed to block DC voltage offset saturating the transformer in voltage mode control. This converter often requires an additional shim inductor which is needed for ZVS operation, and it can make the converter bulky and can hamper power density. Also, circulating current in the top and bottom switches allows energy stored in the leakage inductance to charge/discharge switch output capacitance and achieve zero voltage switching (ZVS), but it leads to potentially higher conduction losses of switches. The inductor at the secondary side although smooth the charging current of the battery, the inductor sets high reverse voltages on the diodes, which will be proportional and inversely proportional to the duty cycle, and therefore, depending on the operating conditions, reverse voltages on the diode in excess of two and three times the output voltage might arise [21].

2.3.2 DAB

Figure 2-3 depicts the basic topology of the Dual Active Bridge converter. It consists of full bridge with active switches on both the primary and secondary sides connected by a high-frequency transformer. Because of the inherent lagging current in one of the bridges, the current discharges the output capacitance of switches of one bridge (say secondary side) and some switches of the primary side thereby enabling ZVS turn on. In addition to these lossless capacitive snubbers can be used across the switches to reduce turn-off losses. The main advantages of this converter are its inherent bidirectional capability which is achieved by controlling the phase angle between the two bridges and its modularity that allows for it to be scaled to higher power levels.

The control of the DAB ranges from simple (or single-phase shift modulation) to complex (for extended, dual and triple phase shift modulation). This topology can be used to cover a wide variation of battery voltages with single phase shift modulation but circulating currents in the transformer increase which drastically reduces efficiency.

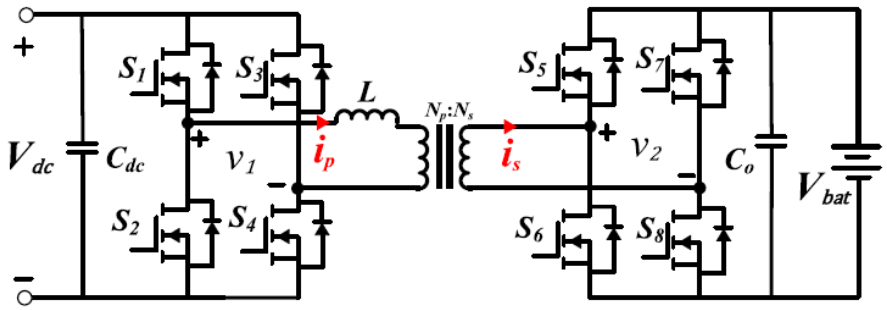

Figure 2-3: Dual active bridge converter [20]

But with advanced modulation schemes like triple phase shift, the converter can theoretically achieve ZVS over the entire operating range. The utilization of the output

power to the transformer kVA rating is high for this topology. The required output capacitor to handle the ripple currents is also low for this converter. This converter with the relatively fewer number of devices, soft-switching commutations, low cost, and high efficiency is used in applications where the power density, cost, weight, isolation, and reliability are critical factors. Another limiting feature is that the converter often requires an additional shim inductor which is needed for ZVS operation, and it can make the converter bulky and can hamper power density [22-23].

2.3.3 LLC

The gain of this converter is a function of switching bridge gain, resonant tank gain and transformer turns ratio. The output voltage regulation is achieved by varying the switching frequency of operation. There are three modes/regions of operation in the LLC resonant converter namely the operation at resonant frequency, above resonant frequency, and below resonant frequency. During below resonant frequency operation, the resonant half cycle inductor current reaches the value of magnetizing current within the switching cycle and leads to soft switching across secondary rectifier diodes but on the other hand leads to more conduction losses due to more circulating energy. Above resonant frequency operation leads to increased switching losses and hard commutation of secondary rectifier diodes but leads to lower conduction losses due to reduced circulating energy. Hence the best performance of these converters is obtained when operated close to resonance frequency where ZVS turn on and ZCS turn off is possible. This converter provides unidirectional power flow and is generally used in applications less than 5 kW [20-24]. Figure 2-4 shows the topology of the LLC resonant converter.

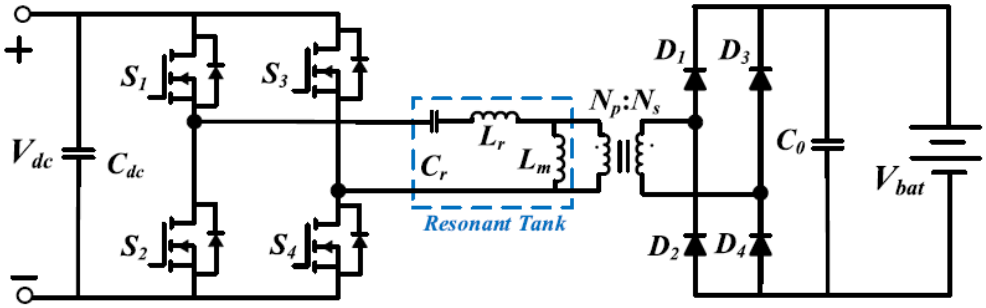

Figure 2-4: Full bridge LLC converter [20]

Paralleling and synchronization of multiple LLC converter modules to increase the power throughput is difficult and often requires external control logic for safe implementation. Low di/dt in high-output-voltage designs (greater than 400 V) makes implementation of synchronous rectification in LLC converter quite tricky. The ripple current and peak voltage stress across the active and passive devices is significantly high, hence higher output capacitance is needed for handling high ripple. Since this converter soft switches during turn on and turn off, the EMI performance is better when compared to other hard switched topologies previously discussed.

2.3.4 DAB in CLLC Mode

The CLLC incorporates all the functionalities of the LLC described before, but a major advantage of this topology is that with the use of active switches across the secondary, we can obtain bidirectional power transfer as Figure 2-5 shows. The ZVS/ZCS operation of this converter results in increased efficiency. When there is room to vary the bus voltage by a margin of 10%, this converter can cater to wide varying battery voltage with good efficiency performance, but with a fixed bus voltage this has a very limited range of operation. With capacitors in the primary and secondary side of the transformer, the

problem of saturation of the core of the transformer is prevented. This converter is primarily suited for onboard charger applications but can be used at higher power levels up to 10 kW. But scaling to higher power levels and paralleling can be difficult as it requires a highly symmetrical tank structure and synchronization of multiple modules which can be quite difficult [25].

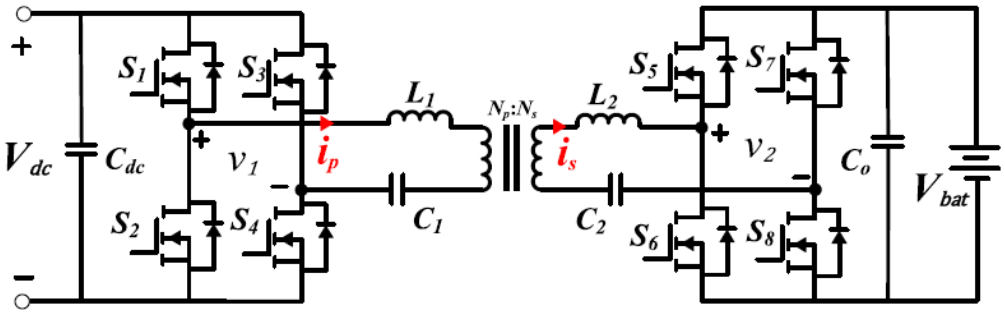

Figure 2-5: Dual active bridge converter with CLLC resonant tank [20]

2.3.5 Comparisons

Table 2-1 compares and summarizes the previously discussed DC-DC topologies.

2.4 Three Port DC-DC converters

Three port converters play a major role in integrating solar arrays to existing power conversion systems. This makes it more efficient as the result of processing power in just one stage. Also, the power density of the system increases significantly by sharing active and passive components between SISO converters [26], which is important for SEVs. As an example, in [27], a three-port converter regulating the solar arrays, grid, and high voltage battery is introduced. The converter is shown in Figure 2-6.

Table 2-1: Summarized Features of isolated DC-DC converters

	LLC Converter	Phase Shift Full Bridge (PSFB)	Dual Active Bridge (DAB)	DAB in CLLC Mode
Transformer kVA rating	High	Mild	Low	High
Power output to transformer kVA rating	Low	Mild	High	Mild
Input and output capacitor rms current	High	Mild	Low	High
Operation	Unidirectional	Unidirectional	Bidirectional	Bidirectional
Conduction losses	High	Mild	Low	Mild
Switching losses	Low	High	High	Low
Total Losses	Low	Highest	Mild	Low
Control Complexity	Moderate	Simple	Moderate	Moderate
Wide Battery Voltage handling	No, Needs additional DC-DC converter	Yes, With reduced efficiency	Yes, With reduced efficiency	Limited Range
Paralleling modules	Intensive	Easy	Easy	Intensive

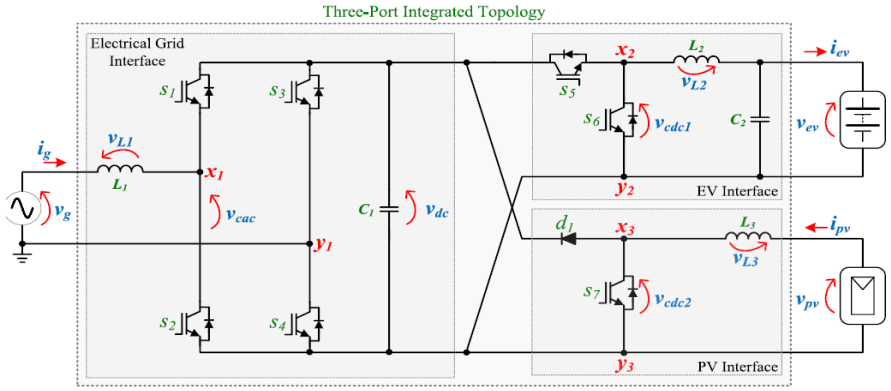

Figure 2-6: Basic three-port converter interfaces EVs and RE with Electrical grid [27]

Three port converters are divided into three categories: 1- non-isolated 2- fully isolated 3- partly isolated. Partly isolated three port converters can provide a high voltage gain and isolation between two ports. However, they have limited power flow options due to partially shared devices. Isolated three port converters can achieve high voltage gain, high

power operation and provide galvanic isolation while offering single-stage power conversion between any two ports. However, the three-winding transformer and many switches increases the converter size and cost [28].

2.4.1 Isolated Three Port Converters

[29-34] presents isolated topologies. [30-31], [33-34] are the three winding topologies which are applicable in plug-in electric vehicles to interface the battery, fuel cell, and DC-bus required for driving the motor. The isolated converter is shown in Figure 2-7. They use phase-shift and PWM control for decoupling the power flow between ports to achieve power balance between ports.

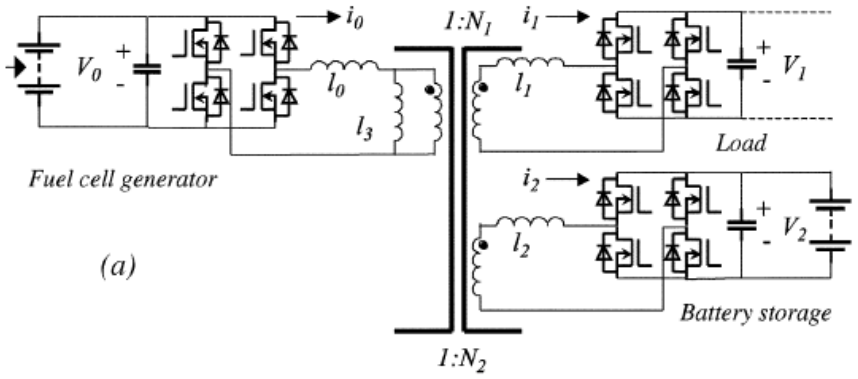

Figure 2-7: Basic Three winding isolated three port converters [30]

[32] is a three port DC-DC converter to interface renewable energy sources with bidirectional load and a battery as an energy storage. It uses the series-resonant structure to achieve soft switching for the switches. It adopts a novel phase shift control to control the flow between ports and achieve soft switching for all full bridges.

2.4.2 Partially Isolated Three Port Converters

[35-44] propose the partially isolated topologies. In these structures, only one port is isolated from others. A high frequency transformer can be used to provides the isolation and wide voltage regulation of the output port. An attractive structure is achieved by integrating two interleaved buck-boost converters (IBBC) and a secondary side phase shift (SSPS) full bridge converter to interface the renewable energy sources, storage element, and load. This converter can be controlled by PWM and Phase-Shift (PS) method to control the power flow between voltage source and battery and regulate output voltage respectively. Another approach is to employ an LLC converter instead of the DAB structure, which can be controlled by frequency modulation. [36] proposes an IBBC+SSPS structure which interfaces the hybrid battery and fuel cell and load in a hybrid electric vehicle.

In [37-38],[40], [42-43] the renewable energy sources and battery share two switching legs which reduces the number of components and cost. And the output port is isolated on the secondary side. The secondary side full bridge, which plays the rectifier role, can vary based on the voltage conversion requirement. [39] uses the phase shift in primary legs to control the power flow to output port and battery. The converter is presented in Figure 2-8.

All [35,41], and [44] are fly back structures which can regulate the output voltage by the either two PWM variable [44] or PWM+PFM [41] or PWM+PS [35]. The converter proposed in [41] is illustrated in Figure 2-9.

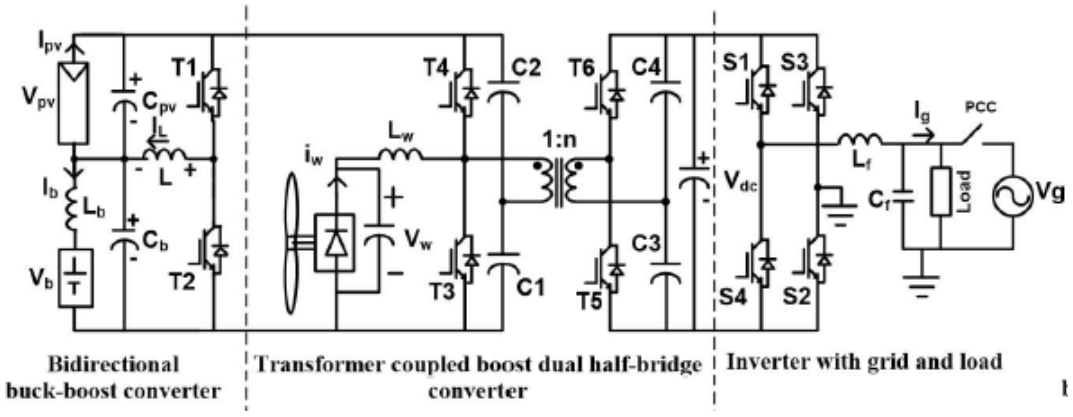

Figure 2-8: Multi-port Buck-boost +IBBC+SSPS converter [39]

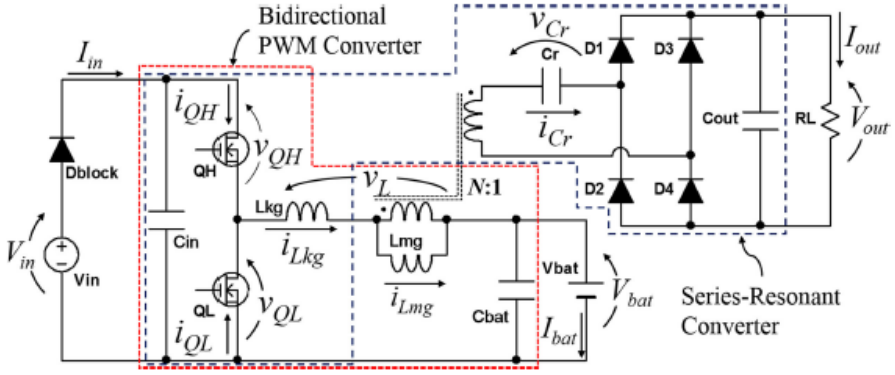

Figure 2-9: PWM + PFM converter [41]

2.4.3 Non-isolated Three Port Converters

Attractive advantages of the non-isolated converters make them suitable for many applications, where the isolation is not required. Recently, considerable research has tried to synthesize three port converters and find a general solution for integrating controlled voltage sources and controlled current sources with each other and created new converters. [45-49] investigates the different approaches to design and control the novel three port converters. [50-53] presents the non-isolated three port converters designed for interfacing

renewable energies or grid as input energy sources, storage elements such as battery and supercapacitors, and load.

[50] is an IBBC which interfaces the battery and supercapacitor with a DC-bus. The supercapacitor can handle the high power and high number of charge/discharges of the battery and help to increase the lifespan of the battery. It regulates the output voltage by controlling the duty cycle of the two IBBC leg and half bridge placed at output port.

[51] is the integration of two boost converter which share the output diode. The converter is designed to interface the fuel cell and supercapacitors. The phase shift and duty cycle of the boost switches can regulate the output voltage and power flow between the fuel cell and supercapacitors. [52] presents a four-port converter for interfacing the PV, fuel cell, battery, and load. It uses the non-inverting buck-boost converter integrated with a boost converter. MPPT tracking of the PV source, adjusting the fuel cell power, controlling battery power flow, and calibrating the output voltage can be performed by controlling duty ratios of the switches. [53] is simply two interleaved boost converters where each one is being fed by battery and renewable energy sources.

2.5 References

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Chapter 3

High-Efficiency Coupled-Inductor Switched-Capacitor Boost Converter with Improved Input Current Ripple

A novel single-switch coupled-inductor switched-capacitor (CISC) high step-up converter is proposed which has a boost-type input structure allowing an improved input current ripple compared to other leading CISC converters. This is important for sustainable energy applications such as photovoltaic (PV) cells and fuel cells where high current ripple can degrade performance or lifetime. Though large input filters can be added between the energy source and the boost converter to smooth a pulsed converter input current, the proposed converter naturally has a more moderate current ripple, reducing the need for additional filtering. With regards to the coupled inductor, the leakage inductor energy is recycled without using an extra clamped circuit, and core utilization is high. The detailed theoretical operation is presented and an experimental prototype (200 W, 36 V to 48 V input, 400 V output) achieves a maximum efficiency of 97.1%.

3.1 Introduction

High step-up DC-DC converters are increasingly in demand for a variety of applications, including sustainable energy, lasers, X-rays, and radar [1]. For example, when connecting photovoltaic (PV) cells or fuel cells (both lower-voltage devices) to micro- or nano-grids, significant voltage boost is required. Further, the recent concept of adding on-board PV cells to electric vehicles also requires a high-efficiency, high-power density, high-step-up converter to boost the PV voltage to the traction battery voltage [2-3]. However, reducing the input current ripple for PV-connected converters is also important, as high current ripple can lead to poor maximum power point tracking performance, decreasing PV system efficiency [4-5]. For fuel cell systems, current ripple has been shown experimentally to accelerate cell degradation [6]. If the structure of the converter creates a

pulsed input current, then significant additional filtering components are required, increasing system size and cost. Therefore, the goal of this work is to develop a high step-up converter with low component count, low cost, and high efficiency, that also allows for an improved input current ripple compared to the pulsed input current often seen in other similar converters. An improved input current ripple will reduce the size of the additional input filters required, or even preclude their need altogether with the choice of a larger converter input inductor – this will maximize power density for the whole system.

The conventional boost converter is not generally used for high step-up applications because parasitic losses at high duty cycles degrade the output voltage and efficiency. Furthermore, switch and diode voltage stress are equal to the high output voltage, meaning high voltage rated devices are required, which increases cost and $R_{ds(on)}$, leading to higher conduction losses [7]. Thus, numerous voltage multiplier cells have been proposed in the literature to increase voltage gain and reduce device voltage/current stress, such as quadratic converters [8], quasi-resonant converters [9], switched-capacitor (SC) cells [10], switched-inductor cells [11], and active networks [12]. Quadratic and quasi-resonant converters can provide high gain at lower duty cycles, though control can be complex. Furthermore, the second stage of the quadratic converter suffers from high voltage stress, and quasi-resonant converters have high current stress. Thus, both suffer from low power density and efficiency [13]. The main advantage of SC cells is the reduction of voltage stress on the switch and diodes, which reduces the size and cost of these devices. However, a large number of these cells should be placed in series to achieve high voltage gain, which can instead increase the cost and volume of the converter, and also increases diode reverse

recovery losses. Integrating a coupled inductor with SC cells (CISC converters) has become a popular way to improve the performance of SC converters [14], [15]. The leakage inductance can help reduce the reverse recovery losses of the diodes, which increases converter efficiency. Also, increasing the turns ratio, *n*, of the coupled inductor will increase voltage gain, meaning less series SC cells are required.

In the literature, some high step-up converters [16] – [19] use multiple switches, which require multiple gate drive circuits, increasing complexity and cost. Furthermore, [16] – [18] also have high input current ripple and relatively low efficiencies. Due to the cost and complexity of using multiple switches, this literature review will focus on single-switch converters.

Interleaved SC converters [19][20] give the lowest input current ripple, but use 2 or 3 inductor cores, have low voltage gain, and achieve low or moderate efficiency. Using multiple inductor cores has the disadvantages of increasing component cost, and worsening efficiency and power density. With moderate input current ripple, quasi-z source [21], and CI quadratic [8], [22] converters offer high voltage gain, but use 2 or 3 inductor cores and also have low peak efficiencies (87.0% to 93.1%). SC converters also have moderate input current ripple [23], [24], [11], but [23] has only moderate voltage gain and relatively low peak efficiency, and [24] and [11] have low gain with moderate efficiency. Some CISC converters achieve moderate input current ripple [25], [10], [26], but have only moderate voltage gain. Furthermore, [10] requires 2 inductor cores. The quasi-resonant converter in [9] also has moderate current ripple, but has low gain, low peak efficiency, and requires 2 inductor cores. References [27] and [28] propose CISC converters where the drain of the

switch is connected to both sides of the coupled inductor, meaning there is always inductance in the switch current path which results in high voltage spikes on the switch during turn-off. This fundamental problem limits their efficiency (93.7% and 92.8% at full load, respectively), and thus their practical usefulness. The authors of [28] have worked to remedy this problem in [29] by adding an additional switch and diode as an active clamp, but this now has the complexity and cost of being a two-switch converter. Many other CISC converters are available with high gain, moderate or high efficiency, and the use of only one inductor core, but these all have pulsating input currents [30] – [34]. These converters are best suited to applications where very high voltage gain is required and input current ripple is not a concern.

This chapter proposes a CISC converter that is designed for a PV or fuel cell input with typical input voltage range of 36 to 50 V, and an output voltage of 400 V to represent a DC microgrid or an electric vehicle battery. The primary design goal is to achieve an improved input current ripple to reduce additional filtering needs for PV or fuel cell sources. Other requirements include: a high voltage gain of approximately 8-11, high efficiency, and low component count. The proposed converter for this application uses one switch, one coupled inductor core, 5 diodes, and 5 capacitors, exhibits high efficiency (peak 97.1% for a 100 kHz 200 W prototype), and has a moderate input current ripple due to its boost-type input structure. This is in contrast to other CISC converters that have pulsed or near-pulsed input current ripple resulting from their basic input structure. Furthermore, the integration of the secondary side winding of the coupled inductor with the SC cell prevents high voltage spikes on the switch during turn-off. The remainder of the chapter is organized as follows:

Section 3.2 describes the proposed converter and its operational modes. Section 3.3 and 3.4 provide detailed converter analysis including the voltage gain derivation, an efficiency analysis, DCM operation, a small signal analysis, and design considerations. Section 3.5 presents the experimental results, and Section 3.6 performs a detailed comparison of the proposed converter to other topologies in the literature. Section 3.7 summarizes the chapter.

3.2 Proposed Topology and Operation

3.2.1 Proposed Topology

The proposed converter is shown in Figure 3-1 (a). It has one switch (S_1) and a coupled inductor at the input (giving the boost-type input structure) with a turn ratio of $n=n_s/n_p$, where n_s is the number of secondary turns and n_p is the number of primary turns. The proposed topology can also be extended for higher voltage gain by cascading more voltage multiplier cells, as shown in Figure 3-1 (b). The voltage multiplier cell consists of two back-back diodes (D_1, D_2) and two capacitors (C_1, C_3). The topology has low switch voltage stress and increases voltage gain four times more than the basic boost converter for n=1.

The leakage inductance energy is recuperated to the load as follows: in the switch ON state the primary side of the coupled inductor is being charged by the input. The leakage inductance will be charged in this interval. Also, C_1, C_2, and C_3 are being charged by the secondary side of coupled inductor and by C_4. In the switch OFF state, C_1 and C_2 release their energy to the load along with the energy from the primary side of the coupled inductor. The energy stored in the leakage inductance through D_1 will be transferred to C_4.

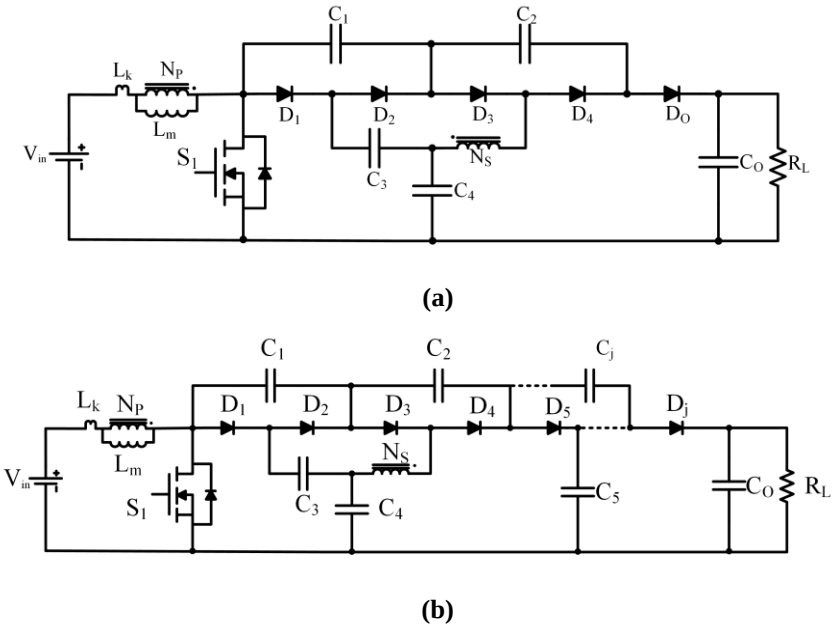


Figure 3-1: (a) Proposed converter (b) General proposed converter for j cells.

Also, leakage inductance smooths the input current ripple and reduces diode reverse recovery loss. The proposed converter uses the series clamping circuit (D_1, C_3, and C_4) to absorb the energy from the leakage inductance and recycle this energy to the output capacitor. In contrast, [17,19,20,21] use a parallel clamping circuit, which means the input current is the sum of the capacitive current and the leakage inductor current, which causes a pulsating input current, by the nature of the topology. In the proposed converter, the input current is equal to the current in the primary inductor, so proper choice of inductance will reduce the input current ripple. A larger inductance will reduce the input current ripple but adds to the volume and cost. With the proposed converter, the designer can choose the inductance to balance these factors based on the application.

3.2.2 Detailed Operation

The proposed converter has six operating intervals during one switching cycle. The typical waveforms for steady state operation of the converter are shown in Figure 3-2, where T_s represents the switching period.

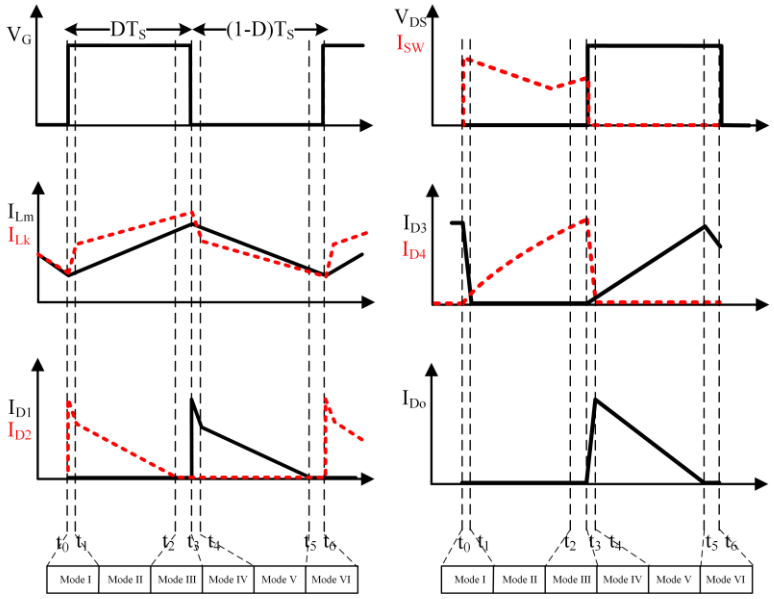


Figure 3-2: Key waveforms of the proposed converter in CCM Operation

The coupled inductor is modeled by the magnetizing inductance L_m, leakage inductance L_{lk}, and an ideal transformer where the coupling factor, k, is defined as,

$$k = \frac{L_m}{L_m + L_{lk}} \tag{1}$$

where L_1 and L_2 are the self-inductance of the primary and secondary sides, and M is the mutual inductance between the primary and secondary sides.

Figure 3-3 and the following discussion provide a comprehensive analysis of the proposed converter in CCM mode where magnetizing current is continuous. CCM mode is recommended because discontinuous current mode (DCM) makes the input current ripple

worsen, leading to lower efficiency, poor MPPT performance, and higher filtering requirements.

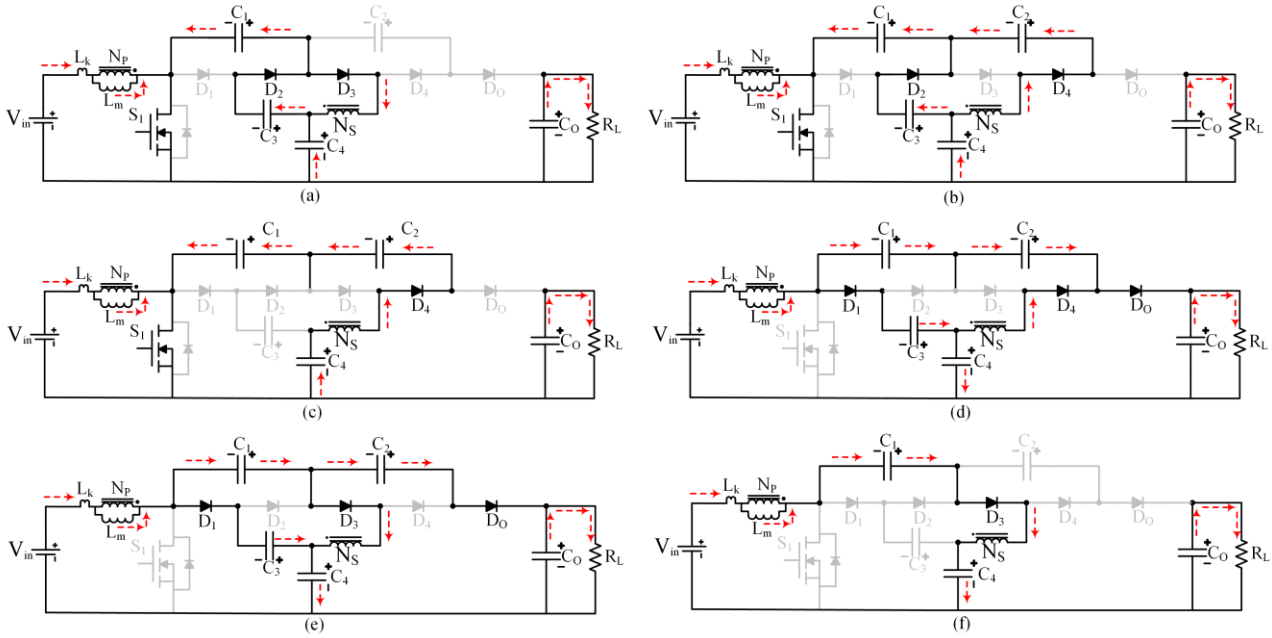


Figure 3-3: **Equivalent circuit of proposed converter (a) Mode I (b) Mode II (c) Mode III (d) Mode IV (e) Mode V (f) Mode VI**

Mode I [t_0,t_1]: In this interval, shown in Figure 3-3(a), the switch turns on and the inductor voltage is equal to the input DC voltage, V_{in}. Therefore, the current of L_m and L_{lk} begin to increase at t_0. For leakage inductance,

$$i_{Llk} = \frac{1}{L_{lk}} \int_o^{t_1} (1-k) V_{in} dt \tag{2}$$

and having a small L_{lk} results in a fast increase in the leakage inductance's current. D_3 provides a path for the secondary side current, as given by (3).

$$i_{D_3}(t) = \frac{i_{Lm}(t) - i_{Llk}(t)}{n} \tag{3}$$

At the end of interval, the L_{lk} current reaches the L_m current and D_3 turns off. D_1 has negative polarity so it stays off. In this interval, the output diode, D_O, is off so the output

capacitor, C_O, provides the power to the load. Based on the opposite polarity of L_1 and L_2, a negative voltage is placed on L_2, so the current decreases from an initial positive value.

Mode II [t_1,t_2]: In this interval, shown in Figure 3-3(b), D_2 and D_4 are conducting and D_1, D_3, and D_O are off. As a result, C_1 and C_2 are charged by the secondary side and by C_3. The current for D_4 is given in (4). Writing a KVL on the primary side and using (4) for calculating i_{Lk} based on i_{sec} results in (5),

$$i_{D_4}(t) = i_{C_2}(t) = i_{\sec}(t) = \frac{i_{Llk}(t) - i_{Lm}(t)}{n} \tag{4}$$

$$\frac{di_{\sec}(t)}{dt} = \frac{v_{L2}}{n^2}(L_{lk} \| L_M) - \frac{v_{in}}{nL_{lk}} \tag{5}$$

Consequently, C_4 will be discharged, and L_m is still being charged by the input, so its current is increasing. In this mode, the leakage current is higher than the magnetizing current, as shown in Figure 3-2.

The current flowing through D_4 and C_2 can be calculated by solving the equivalent circuit shown in Figure 3-4. Solving the differential equations for i_{c3} and i_{D4} gives (6) and (7), where $k_1 = V_{C4(0)} - V_{C3(0)} - V_{C1(0)}$.

$$i_{D_4}(t) = I_{D_4(peak)} \sin(\omega_r t) \rightarrow \omega_r = \frac{\sqrt{5}}{\sqrt{3CL_{lk}}} \tag{6}$$

$$i_{C_3}(t) = -\frac{2}{3} I_{D_4(peak)} \sin(\omega_r t) + \frac{k_1}{3R_C} e^{\frac{-t}{RC}} \tag{7}$$

From the input side, the L_{lk} current can be described as a sinusoidal waveform as shown in (8).

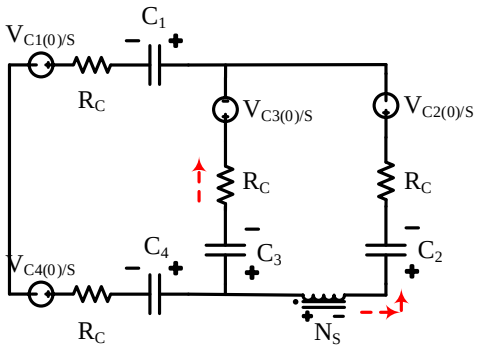


Figure 3-4: Equivalent circuit of Mode II with parasitic elements

$$i_{Llk}(t) = I_{Lm} + I_{D_4(peak)} \sin(\omega_r t) \tag{8}$$

Based on (3), when the current of C_1 and C_3 are equal, the current of D_2 becomes zero, which provides a zero-current turn off for this diode, making turn off losses negligible.

Mode III [t_2,t_3]: At t_2, D_2 turns off and D_4 is still conducting. Therefore, C_3 is no longer being discharged. Still, C_1 and C_2 are being charged by the secondary side and by C_4. L_m and L_k are also being charged by the same current. This interval, shown in Figure 3-3(c), continues until the switch turns off at t_3. In this mode the current through D_4 is given by (9). Compared to (6), the resonant frequency and amplitude are not the same, but they are very close. Therefore, for simplifying the procedure, the current through D_4 will be shown with (9) for all the time switch is on. The duration of Mode II and Mode V are defined as d_1 and d_2 respectively. After d_1, the current goes to zero. Also, the average current of D_4 is I_O so d_1 can be derived as,

$$i_{D_4}(t) = I_{D_4(peak)} \sin(\omega_r t) \rightarrow \omega_r = \frac{\sqrt{3}}{\sqrt{CL_{lk}}} \tag{9}$$

$$d_1 = \frac{1}{\omega_r T_s} \sin^{-1}(\alpha) + \frac{\tan^{-1}(R_s \omega_r)}{\omega_r T_s} \tag{10}$$

where,

$$\alpha = \frac{1}{4\sqrt{1+R^2{}_C C^2 \omega_r^2}}[4 + 3D\omega_r T_s - \frac{kC\omega_r D}{I_O}] \tag{11}$$

The peak current for D_2 is,

$$I_{D_2(peak)} = \frac{k_1}{3R_s} = \frac{(V_{C_4(0)} - V_{C_3(0)} - V_{C_1(0)})}{3R_C} \tag{12}$$

Based on Figure 3-2, the average current of D_4 is equal to I_O. As a result,

$$\frac{1}{T_s}\int_0^{DT_s} I_{D_4(peak)} \sin(\omega_r t)dt = I_O \longrightarrow I_{D_4(peak)} = \frac{I_O \omega_r T_s}{1-\cos(\omega_r D T_s)} \tag{13}$$

Considering the ideal condition where C is very large, meaning ω_r is very small, the peak value for I_{D4}, with the help of the Maclaurin series expansion, is,

$$I_{D_4(peak)} = \frac{2I_O}{D} \tag{14}$$

Mode IV [t_3, t_4]: When the switch is off, D_1 starts to conduct to provide a path for the primary side current. Meanwhile, D_4 is still on to provide the path for the secondary side current. The voltage across L_2 is positive so the secondary side current starts to decrease from a negative value. At t_4, the current of L_m will equal that of L_{lk}. As a result, the current of the secondary side and D_4 reaches to zero, and D_4 will be turned off. In this interval, shown in Figure 3-3(d), C_4 is being charged by the input and C_3. The output diode is turned on and the output capacitor is being charged by C_1 and L_1 as well as the input voltage.

Mode V [t_4,t_5]: As shown in Figure 3-3(e), with D_4 off, C_1 and C_2 are discharged to C_O. C_4 is charged by the secondary side, the input voltage, and C_3. The current of L_m is higher than that of L_{lk}. The current of D_O and D_1 are equal in this interval. At t_5, the secondary side

current (i_{sec}) is equal to i_{Lk}, as shown in (15). As a result, D_1 turns off at zero current, which results in zero turn-off losses for the diode.

$$i_{\sec}(t_5) = i_{Llk}(t_5) = \frac{I_{Lm}}{n+1} \tag{15}$$

Also, the average current for D_1 and D_O are I_O. Considering a linear approximation for discharging C_3 in Mode V,

$$I_{D_O(peak)} = I_{D_1(peak)} = \frac{2I_O}{d_2} = \frac{I_{Lm_{(peak)}}}{2} \tag{16}$$

The peak value for magnetizing current can be expressed as,

$$I_{Lm_{(peak)}} = I_{Lm} + \frac{\Delta I_{Lm}}{2} \tag{17}$$

where the ripple current of L_m and L_{lk} can be obtained based on the existing voltage across the inductor when the switch is on,

$$\frac{\Delta I_{Lm}}{2} = \frac{kV_{in}D_s}{2f_sL_m} \tag{18}$$

$$\frac{\Delta I_{L_{lk}}}{2} = \frac{(1-k)V_{in}D_s}{2f_sL_{lk}} \tag{19}$$

Using (15)-(19) results in (20), where $Q = \frac{kR_LD}{2f_sL_m}$.

$$d_2 = \frac{4}{\frac{n+3}{1-D}\left[1+\left(\frac{1-D}{n+3}\right)^2 Q\right]} \tag{20}$$

Mode VI [t_5,t_6]: As in Figure 3-3(f), at t_5, D_1 and D_O are turned off. As a result, the voltages of C_3 and C_2 remain constant. In this interval, having the primary side and

secondary side in series results in a constant current for L_m and L_k which is equal to the value calculated in (15). The output is being charged by C_O. D_O turns off in this mode which reduces the turn off losses of D_O at t_6. In addition, L_k provides a very smooth turn-on for D_3 and D_4 which makes the turn on losses negligible for these diodes. Also, the energy of this inductor is fully recovered at the end of the period. For D_3, the peak current is equal to the peak current of the secondary side which accrues at t_5.

$$I_{D_3(peak)} = \frac{I_{Lm}}{n+1} = \frac{I_O}{1-D} \times \frac{n+3}{n+1} \tag{21}$$

3.3 Detailed Converter Analysis

3.3.1 Voltage Gain Derivation

For the voltage gain derivation, it is assumed that all semiconductor devices are ideal, so the voltage drop on diodes and the switch are ignored. In Mode II, the switch is on, and by using KVL for both primary and secondary side, (22) – (25) are obtained. For the primary inductor,

$$v_{L_1} = -kV_{in} \tag{22}$$

$$V_{C_1} = V_{C_4} - V_{C_3} \tag{23}$$

$$v_{L_2} = V_{C_3} - V_{C_2} = -nkV_{in} \tag{24}$$

$$V_{C_2} = V_{C_3} + nkV_{in} \tag{25}$$

In Mode V, the switch is off, and by using KVL for both primary and secondary side, (26) – (28) are obtained. Based on this,

$$v_{L_2} = nv_{L_1} = \frac{kn(V_{C_1} - V_{C_4} + V_{in})}{n+1} \tag{26}$$

$$v_{L_1} = k(V_{C_4} - V_{C_3} - V_{in}) \tag{27}$$

$$v_{L_2} = V_{C_3} - V_{C_1} = V_{C_4} + V_{C_2} - V_O \tag{28}$$

Solving for V_O in (28) results in (29).

$$V_O = V_{C_1} + V_{C_2} + V_{C_4} - V_{C_3} \tag{29}$$

By applying the volt–second balance to the primary inductor L_1 in one switching period using (22)-(24),

$$\int_0^{Ts} v_{L_1} dt = D(-kV_{in}) + d_2 k(V_{C_4} - V_{C_3} - V_{in}) + [1 - D - d_2]k(\frac{V_{in} - V_{C_3}}{n+1}) = 0$$

and defining Δ as,

$$\Delta = \frac{1 - D - d_2}{n+1} T_s \rightarrow kV_{in}(D + d_2 - \Delta) = (V_{C_4} - V_{C_3})d_2 k - V_{C_3}\Delta k \tag{30}$$

By applying the volt–second balance to the secondary inductor L_2 in one switching period using (26)-(29),

$$\int_0^{Ts} v_{L_2} dt =$$
$$d_1(-nkV_{in}) + (D - d_1)(V_{C_1} + V_{C_2} - V_{C_4}) + d_2(V_{C_3} - V_{C_1}) + n\Delta k(V_{in} - V_{C_3}) = 0$$

$$\begin{aligned} &-nkV_{in}(d_1 - \Delta) + V_{C_1}(D - d_1 - d_2) + V_{C_2}(D - d_1) + \cdots \\ &\cdots + V_{C_3}(d_2 - nk\Delta) - V_{C_4}(D - d_1) = 0 \end{aligned} \tag{31}$$

Using (30), (31), (23), and (25), V_{C3} and V_{C4} are given as,

$$V_{C_3} = \frac{[(D - \Delta)(n+1) + d_2]kV_{in}}{d_2 - \Delta(nk+1)} \tag{32}$$

$$V_{c_4} = \frac{[(D-2\Delta)(n+1)+2d_2+D+\Delta]kV_{in}}{d_2-\Delta(nk+1)} \tag{33}$$

By inserting (33) and (32) into (23), the voltage of C_1 is shown in (34).

$$V_{c_1} = \frac{[(-\Delta)(n+1)+d_2+D+\Delta]kV_{in}}{d_2-\Delta(nk+1)} \tag{34}$$

Inserting (32) into (25) results in the voltage of C_2 given by (35).

$$V_{c_2} = \frac{[D(n+1)+d_2(nk+1)+k^2n^2\Delta]kV_{in}}{d_2-\Delta(nk+1)} \tag{35}$$

With the voltages of all the capacitors calculated, the output voltage gain is found by inserting (32-35) into (29) to get,

$$M = \frac{V_O}{V_{in}} = \frac{3+nk}{1-D}\left(\frac{1-\frac{4n+3}{n+3}k^2\Delta}{1-\frac{2n+2}{1-D}k^2\Delta}\right) \tag{36}$$

In an ideal condition where the capacitor time constant RC is large enough compared to ω_r so that Mode III and Mode VI can be neglected (which results in $d_2 = 1 - D$ and $\Delta = 0$), the voltage gain can be simplified to,

$$M_{l\,\mathrm{arg}eRC} = \frac{3+nk}{1-D} \tag{37}$$

If the effect of leakage inductance is also ignored, the voltage gain equation further simplifies to,

$$M_{l\,\mathrm{arg}eRC,ignoreL_{lk}} = \frac{3+n}{1-D} \tag{38}$$

Based on (38), the high step-up gain can be achieved with a low duty cycle and turns ratio, which leads to lower voltage stress on capacitors and lower current stress on

inductors. Also, the voltage rating of capacitors is low and working at high frequency results in lower required values of these capacitors. As a result, smaller capacitors like film capacitors can be used, that have better reliability and longer lifetimes than electrolytic capacitors.

Parasitic losses should also be considered, as they will affect the voltage gain, especially at higher duty cycles. Figure 3-5 shows an equivalent circuit with the main parasitic elements considered: capacitor resistance (R_c), switch on-resistance ($R_{ds,on}$), diode resistance (R_d) and voltage drop (V_F), and resistance of the primary and secondary sides of the CI (R_p and R_s). An analysis of the circuit with these parasitic components gives the non-ideal voltage gain shown in (39) as an extension of (38).

$$M_{parasitics} = \frac{3+n}{1-D} \times \frac{1}{1+\lambda} \tag{39}$$

where,

$$\lambda = \frac{R_C}{R_L}\left(\frac{10}{D(1-D)} + \frac{(1-D-\sqrt{D})^2}{1-D}\right) + \frac{4R_{ds,on}}{R_L}\left(\frac{(1-D)}{D} + \frac{1}{4}\left(\frac{3+n}{1-D}\right)^2 + \frac{3+n}{\sqrt{D(1-D)}}\right) + \frac{R_d}{R_L}\left(\frac{5D}{D(1-D)}\right) + 5\frac{V_D}{V_O} + \frac{1}{R_L}\left(\frac{R_s}{D(1-D)} + R_p\left(\frac{3+n}{1-D}\right)^2\right)$$

Figure 3-6 shows the converter voltage gain from (39) for the case of P_{out} = 100 W, V_{out} = 400 V, V_F = 0.44 V, R_d=5 mΩ, R_c = 8 mΩ, switch $R_{ds,on}$ = 5 mΩ, and R_p = R_s = 50 mΩ. The results show that the gain considering parasitic is very close to the ideal gain up to about 80% duty cycle.

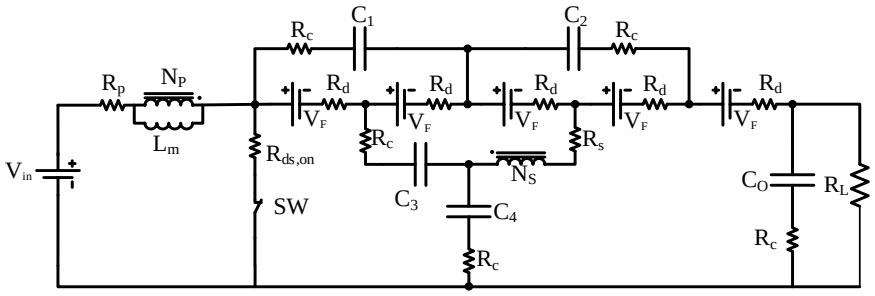


Figure 3-5: Equivalent **circuit including conduction losses of the proposed converter.**

3.3.2 Voltage and Current Stress

The voltage component stresses with respect to V_O are summarized in Table 3-1. Based on Table I, the maximum switch voltage stress is 25% of the output voltage when n = 1, which allows the use of lower voltage rated devices, reducing cost and $R_{ds(on)}$. Figure 3-7 presents the voltage stress of the capacitors and semiconductor devices.

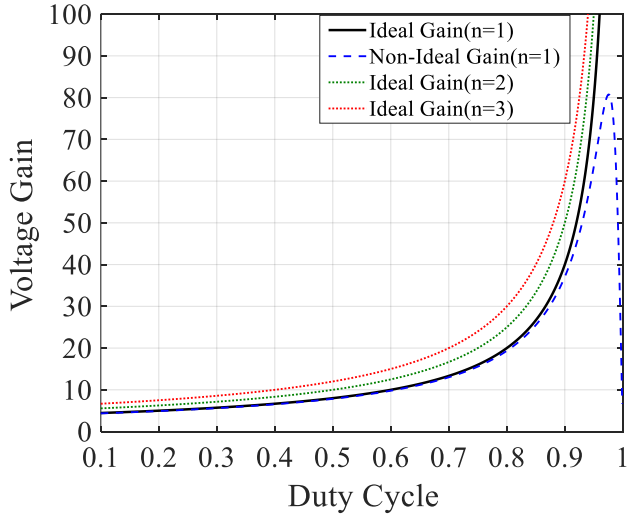


Figure 3-6: The voltage gain considering parasitic conduction losses.

Based on the analysis presented in the previous section, the average current of all diodes is equal to I_O. The rms value can be estimated as shown below.

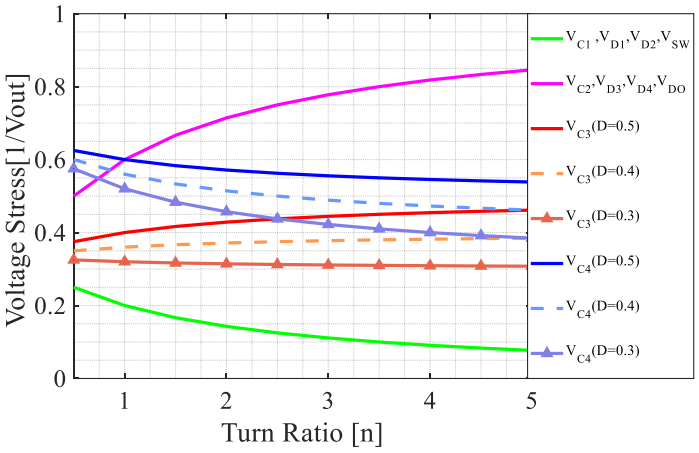


Figure 3-7: Voltage stress of switch, diodes, and capacitors

Table 3-1: Capacitor and Semiconductor Voltage Stresses

Component	Rated Voltage	Component	Rated Voltage
C_1	$\frac{V_O}{3+n}$	D_1	$\frac{V_O}{3+n}$
C_2	$\frac{(1+n)V_O}{3+n}$	D_2	$\frac{V_O}{3+n}$
C_3	$\frac{(1+nD)V_O}{3+n}$	D_3	$\frac{V_O}{3+n}$
C_4	$\frac{(2+nD)V_O}{3+n}$	D_4	$\frac{(n+1)V_O}{3+n}$
Switch	$\frac{V_O}{3+n}$	D_O	$\frac{V_O}{3+n}$

$$I_{D_1(rms)} = I_{D_O(rms)} = \sqrt{\frac{1}{T_s}\int_0^{d_2T_s}\left(\frac{2I_O}{d_2} - \frac{2I_O}{d^2{}_2T_s}t\right)^2 dt} = \frac{2}{\sqrt{3}}\frac{I_O}{\sqrt{d_2}} \tag{40}$$

$$I_{D_2(rms)} = \sqrt{\frac{1}{T_s}\int_0^{d_1T_s}\left(-\frac{2}{3}i_{D_4}(t) + \frac{k_1}{3R_s}e^{\frac{-t}{RC}}\right)^2 dt} \approx \frac{4I_O}{\sqrt{3D}} \tag{41}$$

$$I_{D_3(rms)} = \frac{I_O}{1-D}\cdot\frac{n+3}{n+1}\sqrt{3(1-D)+4d_2} \approx \frac{\sqrt{7}I_O}{\sqrt{(1-D)}}\cdot\frac{n+3}{n+1} \tag{42}$$

$$I_{D_4(rms)} \approx \sqrt{\frac{1}{T_s}\int_0^{DT_s}\left(\frac{I_{D_4(peak)}}{DT_s}t\right)^2 dt} = \frac{2I_O}{\sqrt{3D}} \tag{43}$$

The rms value of the magnetizing inductor current is,

$$I_{Lm(rms)} = (\frac{2\sqrt{3}+1}{2\sqrt{3}})(\frac{n+3}{1-D})I_O - \frac{kV_{in}D}{2\sqrt{3}L_m f} \quad (44)$$

The input current in each mode is found by summing the currents of the other connected components. From this, the rms value can be calculated as shown in (45).

$$I_{Llk(rms)} = \sqrt{[1+(1-D)(\frac{1+(n+1)^2}{(n+1)^2})]I^2{}_{Lm(rms)} + I^2_{D_4(rms)} + I^2_{D_O(rms)}} \quad (45)$$

3.3.3 Efficiency Analysis

The efficiency analysis considers many non-idealities in the circuit, such as switching and conduction loses, diode forward voltage drops, and losses in the inductor and capacitors. The analysis is performed for the following operating conditions and parameters: P_{out} = 100 W, V_{in} = 40 V, V_{out} = 400 V, D = 60%, capacitor equivalent series resistance ESR = 8 mΩ, switch $R_{ds\text{-}on}$ = 5 mΩ, R_L = 1600 Ω, $I_{in(avg)}$ = 2.5 A. The current RMS and average values of passive and active components are extracted by simulation.

1) *Switch Losses:* The conduction and switching losses are:

$$P_{sw} = R_{ds-on}I^2{}_{sw(rms)} + \frac{1}{2}V_{ds}I_{sw(on)}(t_r + t_f)f_{sw} = 1.603W \quad (46)$$

2)Diode Losses: Three diodes (D_1, D_3, and D_O) have average conducting currents of 0.623 A with D = 40%, and the diode forward conducting voltage, V_F, for these is estimated at 0.8 V from the datasheet. The other two diodes (D_2, D_4) have average conducting currents of 0.415 A with D = 60%, with estimated V_F at 0.75 V. Thus, the conduction losses for the diodes can be expressed as (47), where *i* represents each diode number,

$$P_D = \sum_{i=1}^{5} V_{F,i}I_{on,i}d_i = 3\left(0.8\times 0.623\times 0.4\right) + 2(0.75\times 0.415\times 0.6) = 0.97W \quad (47)$$

3)Capacitor Losses: For capacitors, the conduction losses are,

$$P_C = ESR\sum_{i=1}^{6} I^2_{i,rms(cap)} = 64mW \tag{48}$$

4)Inductor Losses: Core losses, in (49), and winding conduction losses, in (50), constitute the inductor losses.

$$P_{core} = Kf_{sw}^{\alpha}(B_{\max})^{\beta} A_c l_c \tag{49}$$

B_{max} is the maximum flux density, A_c is the cross-sectional area of the core, and l_c is the average path length of the core. K, α, and β are dependent on the core type and are available in the datasheet. In (50), R_p and R_s are the parasitic resistances in the primary and secondary sides.

$$P_{cond} = R_p I^2_{p(rms)} + R_s I^2_{s(rms)} \tag{50}$$

The winding and core losses are calculated by the manufacturer using the Coilcraft online calculator and are shown in (51).

$$P_L = P_{winding} + P_{core} = 700mW \tag{51}$$

The efficiency of the converter can be calculated from (52),

$$\eta = 100\% \times \frac{P_{out}}{P_{out} + P_D + P_C + P_{sw} + P_L} = 96.78\% \tag{52}$$

The measured efficiency of the prototype at this operating point is 96.7%, which is very close to the calculated efficiency. The detail loss breakdown is presented in Figure 3-8.

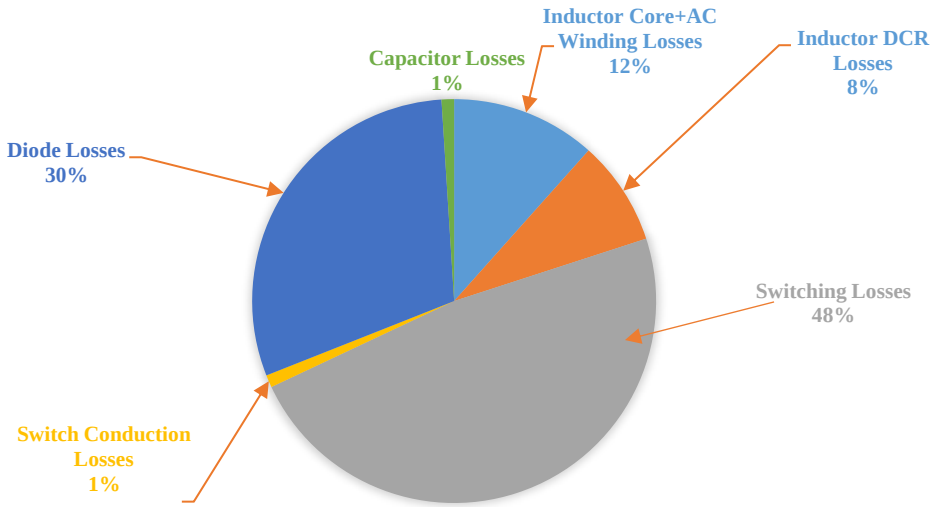


Figure 3-8: Detailed power loss breakdown

3.3.4 DCM Operation

Although CCM is preferable for lowering input current ripple, analysis of DCM operation is useful to determine the CCM/DCM boundary. A similar approach as used for calculating CCM voltage gain is used here to calculate the gain for DCM, which is given by (53).

$$M_{DCM} = \frac{1}{2}(n+3)\left(1+\sqrt{1+\frac{2D^2}{\tau(n+3)^2}}\right) \tag{53}$$

τ is the magnetizing inductance time constant and is defined as,

$$\tau = \frac{L_m}{R_L T_s} \tag{54}$$

At the boundary condition when the voltage gain of CCM operation and DCM operation are equal, the boundary magnetizing inductance time constant can be obtained by,

$$\tau_{L_{mb}} = \frac{D(1-D)^2}{4(n+3)^2} \tag{55}$$

Figure 3-9 shows the boundary magnetizing inductance time constant for different duty cycles for *n=1*. For a specific power and frequency, this curve can be used to calculate the inductor value which will make the time constant higher than the boundary value shown by the blue line, putting the converter in CCM. For example, in the prototype, the lowest power is 100 W at 400 V output (R_L = 1600 Ω), T_s = 10 μs, and L_m is selected as 48 μH, meaning τ = 0.003 and the prototype is in CCM for all duty cycles. At higher powers, it will remain in CCM.

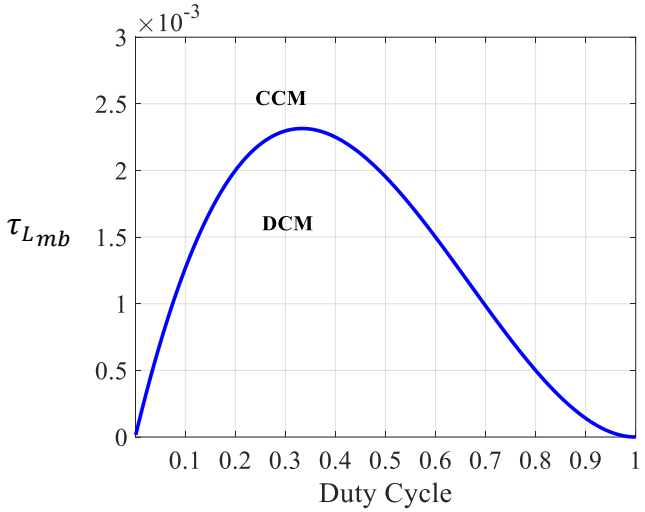


Figure 3-9: Curve of the CCM/DCM boundary of magnetizing inductance time constant of the inductor with respect to the duty cycle

3.3.5 Small Signal Analysis

The goal of small signal modeling is to predict how low-frequency variations in duty cycle induce low frequency variations in the converter voltages and currents. In the small signal analysis, the switching ripples and their complicated harmonics and sidebands are ignored. A complete steady-state analysis is performed for the proposed converter. The CI

and five capacitors are the energy storing components. By considering the leakage inductance, three state variables are assigned to the current of the primary (x_1), secondary (x_3), and input (x_2). The other five state variables are assigned to the five capacitors, for a total of eight state variables, as shown in (56).

$$\begin{aligned} &x_1 = i_{Lm}, x_2 = i_{Llk}, x_3 = i_{\text{sec}ondary}, x_4 = v_{C1}, x_5 = v_{C2}, \\ &x_6 = v_{C3}, x_4 = v_{C4}, x_8 = v_O \end{aligned} \tag{56}$$

The equations in the first state when the switch is on are defined in (57).

$$\begin{cases} \dfrac{dx_1}{dt} = \dfrac{(v_g + x_4 + x_5 - x_8)k}{L_m} - \dfrac{k(R_{on} + r_p)}{L_m} x_2 \\ \dfrac{dx_2}{dt} = \dfrac{(v_g + x_4 + x_5 - x_8)(1-k)}{L_{lk}} - \dfrac{(1-k)(R_{on} + r_p)}{L_{lk}} x_2 \\ \dfrac{dx_3}{dt} = \dfrac{x_4 - x_6}{L_2} \end{cases} \begin{cases} \dfrac{dx_4}{dt} = \dfrac{-(x_2 + x_3)}{2C} \\ \dfrac{dx_5}{dt} = \dfrac{(x_3 - x_2)}{2C} \\ \dfrac{dx_6}{dt} = \dfrac{(x_3 - x_2)}{2C} \\ \dfrac{dx_7}{dt} = \dfrac{(x_3 + x_2)}{2C} \\ \dfrac{dx_8}{dt} = \dfrac{(x_2 - x_3)}{2C_O} + \dfrac{-x_8}{RC_O} \end{cases} \tag{57}$$

When the switch is off, the equations are defined in (58). In the next step, the averaging method is adopted for the calculated equations to combine the on and off modes.

$$\begin{cases} \dfrac{dx_1}{dt} = \dfrac{kv_g}{L_m} - \dfrac{k(R_{on} + r_p)}{L_m} x_2 \\ \dfrac{dx_2}{dt} = \dfrac{(1-k)v_g}{L_{lk}} - \dfrac{(1-k)(R_{on} + r_p)}{L_{lk}} x_2 \\ \dfrac{dx_3}{dt} = \dfrac{x_5 - x_6}{L_2} \end{cases} \begin{cases} \dfrac{dx_4}{dt} = \dfrac{-x_3}{C} \\ \dfrac{dx_5}{dt} = \dfrac{-x_3}{C} \\ \dfrac{dx_6}{dt} = 0 \\ \dfrac{dx_7}{dt} = \dfrac{x_3}{C} \\ \dfrac{dx_8}{dt} = \dfrac{-x_8}{RC_O} \end{cases} \tag{58}$$

The linearization for small signal values for each state variable can be defined as $x_i = \hat{x}_i + x_{0i}$, where x_{0i} is the DC value of the state variable and $\hat{x}_i$ is the small signal component. Using the standard linearized small-signal state equations and the Laplace transform, the transfer function is calculated by MATLAB, and the approximated second order result is in (59).

$$G(s) = \frac{\hat{v}(s)}{d(s)} = \frac{(s-\alpha)}{s^2 + 2\xi\omega_n + \omega^2{}_n} \tag{59}$$

where,

$$\begin{cases} \omega_n = \dfrac{(1-D)}{3+n} \cdot \dfrac{1}{\sqrt{L_m C_O}}, \quad \alpha = \dfrac{R_{ds(on)} D I_{load}}{L_m} s \\ \xi = \left(\left(\dfrac{k R_{ds(on)} D}{L_m}\right) \dfrac{3+n}{(1-D)} + \dfrac{1}{R_{load} C_O}\right) \dfrac{1}{2\omega_n} \end{cases}$$

Figure 3-10 shows the small signal analysis result (59) of a 1% change in duty cycle as the blue line.

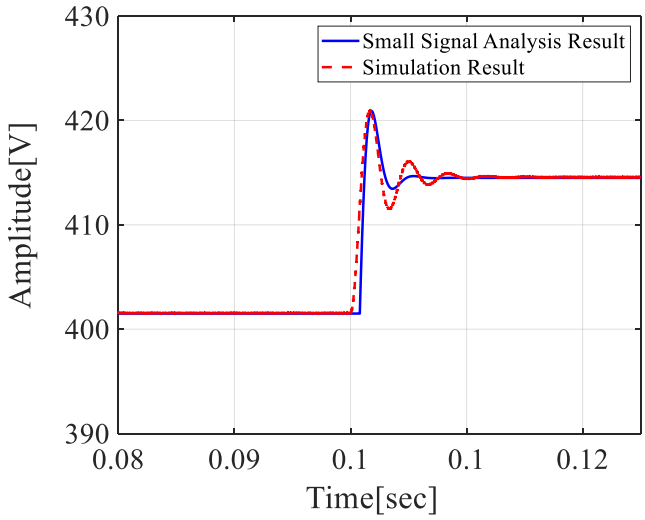


Figure 3-10: Small signal modeling results compared to simulation result.

The simulated result of the switching circuit is shown as a red dashed line. The small signal result predicts the peak voltage overshoot very accurately, which is important for control. There is some variation between the model and the simulation after the peak due to the second order approximation of the transfer function.

3.4 Design Considerations

3.4.1 Coupled Inductor Design

In order to operate in CCM condition, the magnetizing inductance's current should be higher than the boundary current,

$$L_m \geq \frac{kV_{in}D(1-D)}{2(3+n)I_{O(\min)}f_{sw}} \tag{60}$$

$$n = \frac{V_O}{V_{in}}(1-D)-3 \tag{61}$$

Based on the acceptable input current ripple (ΔI), the leakage inductance can be calculated as,

$$L_{lk} \geq \frac{(1-k)V_{in}D}{(\Delta I)f_{sw}} \tag{62}$$

3.4.2 Capacitor Design

The capacitors store energy in some portion of the switching period and release that energy to the load in the rest of the period. In general, capacitance is related to voltage ripple by,

$$C_x \geq \frac{I_{c_x}\Delta t}{\Delta V_O f_{sw}} \tag{63}$$

where x is related to each capacitor. For the output capacitor, the voltage ripple is affected by capacitance and ESR as,

$$\Delta V_O \geq \frac{I_{C_O(\max)} D}{C_O f_{sw}} + \left(\frac{(n+3) I_{out(\max)}}{d_2} - \frac{\Delta I_{Lm}}{2} \right) \left(ESR + \frac{ESL}{t_r} \right) \tag{64}$$

In (64), ESR = 8mΩ, ESL is approximated as 42.5nH from the datasheet based on lead distance, transient time t_r is defined in the diode datasheet as 50ns, V_O = 400V, and the maximum power is 200W. For maximum 1% (4V) ripple on C_O, (64) requires $C_{O(min)}$>13μF. Two R46KW510050P0M capacitors of 10μF are used in parallel in the prototype to provides enough safety margin for the output capacitor. For C_1, C_2, C_3, and C_4 based on the period they release energy to load,

$$C_1 \geq (n+3)(1+\frac{1-D}{d_2}) \frac{P_{out(\max)}}{\Delta V_O \times V_O \times f_{sw}} \tag{65}$$

$$C_2 \geq \frac{n+3}{n+1} \frac{P_{out(\max)}}{\Delta V_O \times V_O \times f_{sw}} \tag{66}$$

$$C_3 \geq \frac{n+3}{1+nD} \frac{P_{out(\max)}}{\Delta V_O \times V_O \times f_{sw}} \tag{67}$$

$$C_4 \geq \frac{n+3}{2+nD} (1+\frac{1-D}{d_2}) \frac{P_{out(\max)}}{\Delta V_O \times V_O \times f_{sw}} \tag{68}$$

3.5 Experimental Results

Figure 3-11 shows the experimental prototype and setup and Table 3-2 summarizes the specifications. The prototype is rated for 200 W and a 400 V output voltage, with the input varied from 36 V to 48 V. According to the nominal power, the programmable load is set to a constant R_L = 800 Ω. Based on (37), for the desired voltage gain (M = 10), duty cycle

D = 0.6 is required. The minimum magnetizing inductance for working in CCM can be calculated with (60), giving (69). Two inductors JA4590-AL (24 μH each) are used in series to provide the minimum inductance to provide continuous current for the input current. This value is used in the prototype to minimize the size of the converter; however, to improve the input current ripple further, a larger inductance can be used. Table 3-2 provides detailed information of components employed in the prototype.

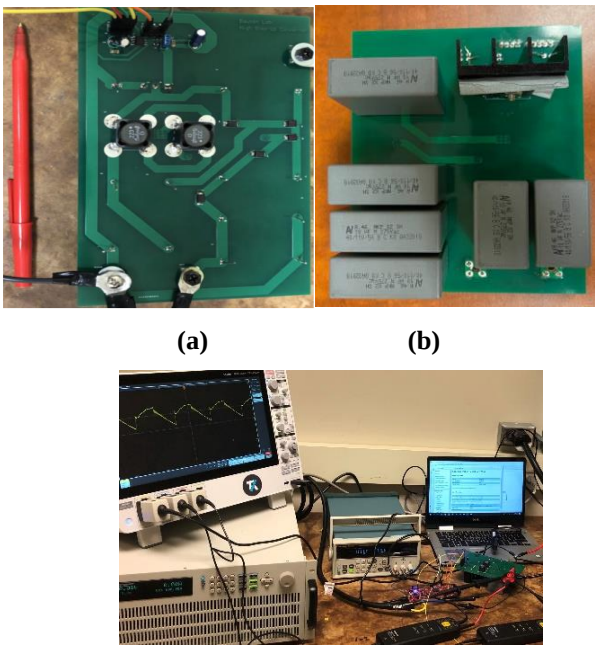
$$L_m \geq \frac{kV_{in}D(1-D)}{(3+n)I_{O(\min)}f_{sw}} = \frac{1\times 40\times 0.6\times(1-0.6)}{(3+1)0.5\times 100k} = 48\mu H \tag{69}$$

Experimental results for 200 W operation are presented in Figure 3-12 to Figure 3-14. Based on Figure 3-13, the output voltage of 405.4 V is obtained from an input voltage of 37.4 V. The output voltage has ripple of 4 V which results in 1% voltage ripple. The capacitor voltages are constant during the switching period and the voltage across them is consistent with (65)-(68).

For the 200 W test, the average input current is 5.71A which results in the efficiency of 96.2% at this power. Figure 3-12(a) shows the input current shape for the 200 W test. The input current ripple is 1.1 A at the average current of 5.71 A which is 18.5% input current ripple. This is greatly improved from a pulsating current, which reduces the size of the input filter, due to the boost-type input structure of the proposed converter.

Figure 3-13 presents the output voltage dynamics with a small variation in the load from 0.5 A to 0.3 A. An overshoot of 4 V accrues due to the load variation, which is 1% of the output voltage. Figure 3-14 shows the experimental efficiency curves of the proposed converter for different input voltages in the range of 100 – 200 W. High efficiency is achieved, at 96.1% to 97.1%, over all tested operating points. For very low power levels,

when the solar radiation is low, the converter enters the DCM region, so current stress at the diodes, inductors, and switch increases, degrading the efficiency. Thus it is not ideal to operate the converter at very low powers below 100 W.



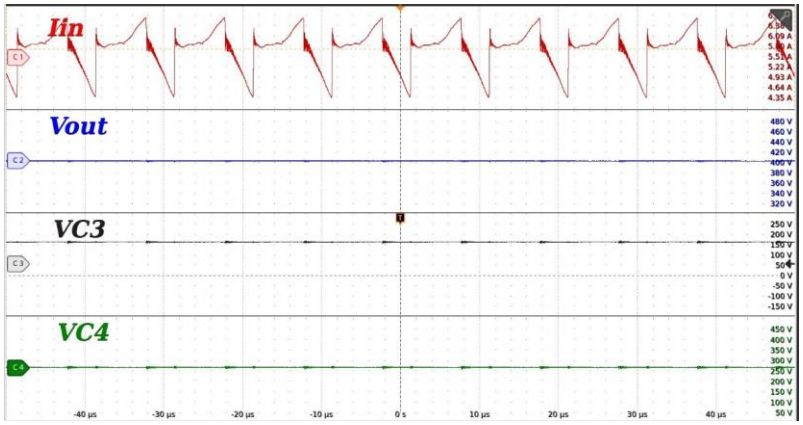
(a) **(b)**

(c)

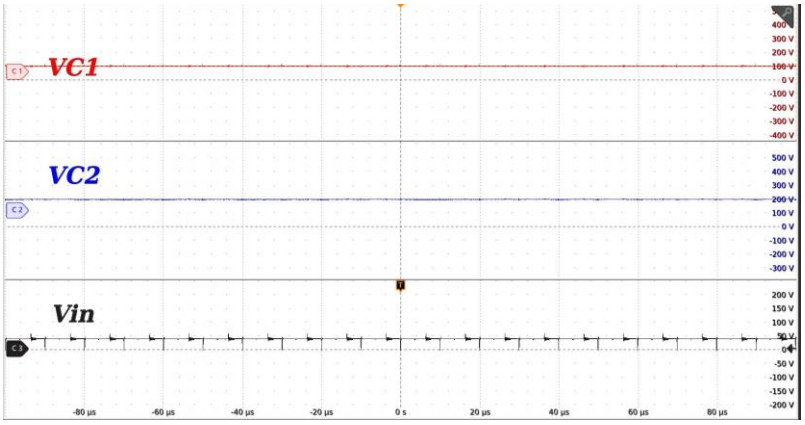
Figure 3-11: Prototype converter (a) top side (b) bottom side (c) measurement setup

Table 3-2: Experimental Prototype Specifications

Parameter	Value
Input Voltage	36-50 V
Output Voltage	400 V
Nominal Power	200 W
Switching Frequency	100 kHz
Switch	IXFK300N20X3, N-Channel 200V
Diodes	5 × HS3FB R5G, 300V, 3A
$C_{1\text{-}4}$	4 × R46KW510050P0M, 10µF Film Capacitor 275V 560V Polypropylene (PP)
C_O	R46KW510050P0M, 20µF
Inductor	2 × JA4590-AL Series of 1:1 coupled power inductor, L_m=50µH, L_{lk}=1µH



(a)



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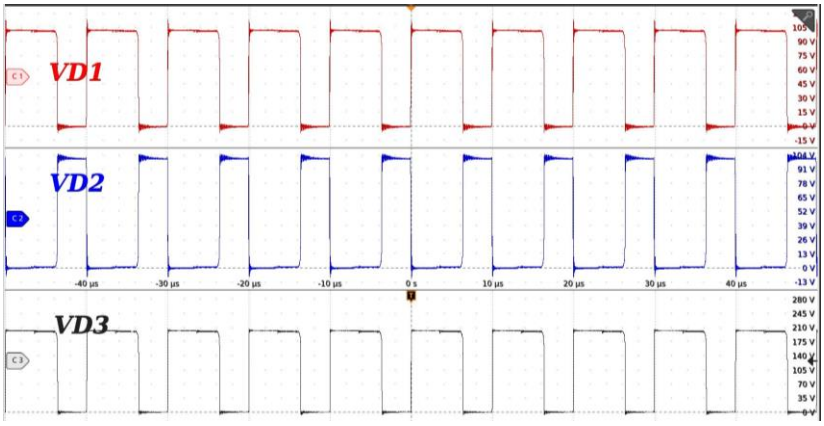
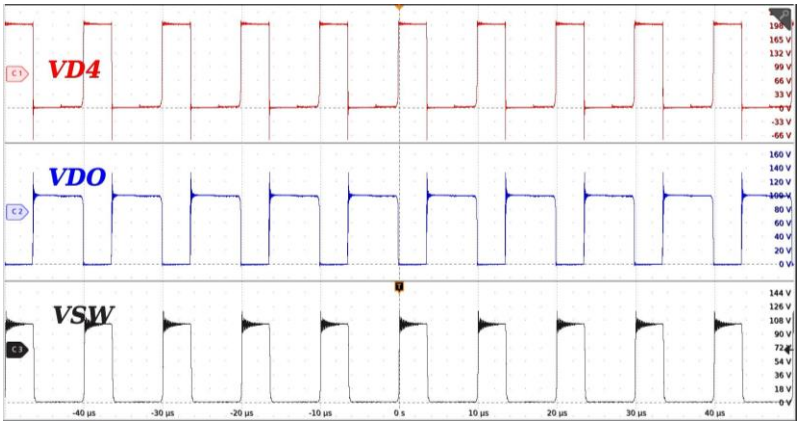


(c)



(d)

Figure 3-12: Experimental results for P_{out}=200W, V_{in}=36V, and V_{out}=400V

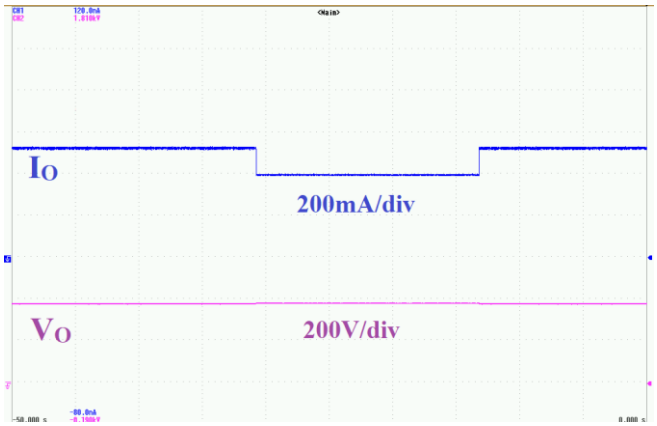


Figure 3-13: Dynamic response of the proposed converter

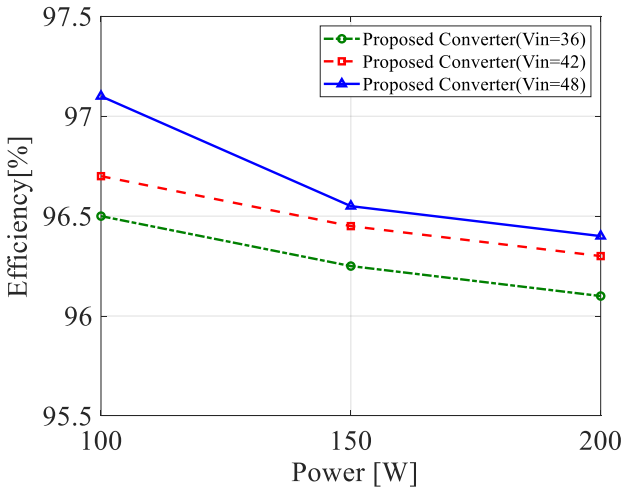


Figure 3-14: Efficiency curve versus power for 400 V output voltage

3.6 Comparison to Other Converters

Table 3-3 compares the proposed converter to other high step-up converters with one switch from the literature with the goal of identifying the best topology for achieving improved input current ripple while attaining high efficiency, high gain, and a low component count, especially a minimum of coupled inductor cores. In Table 3-3, converters are ordered first in terms of input current ripple category (low, moderate, pulsating) and then in terms of voltage gain for D = 0.5, n = 1. N_S is the number of switches, N_D is the number of diodes, N_C is the number of capacitors, and N_L is the number of coupled inductor cores. Though it is difficult to precisely compare efficiencies of prototypes built by different researchers, Table 3-3 shows both the maximum reported efficiency and the full load reported efficiency to give the clearest understanding of each converter. Furthermore, critical factors that affect efficiency are noted in resistance, and converter switching frequency. This is important because the prototype of the proposed converter operates at 100 kHz, only 4 other converters in Table 3-3 operate at 100 kHz, and 12 of the other 14 converters operate at 50 kHz or less, which reduces switching losses. All converters use silicon MOSFETS and most fall within the power rating range of 100 – 300 W. Thus, though variation will exist in the different prototypes, the color-coded efficiency ratings help to group the converters into approximate categories of low (<94%), moderate (<96%), and high (>96%) efficiency.

Table 3-3 shows that the interleaved SC converters that offer low input current ripple at the top of the table have low gain, need multiple inductor cores, and have moderate efficiency, so are not suitable for the target application. The next three rows describe

converters with moderate current ripple and high gain, but they all have multiple inductor cores (3 for those with the highest gain) and low efficiency. The proposed converter lies next in the table with moderate current ripple, high gain, a single inductor core, and high peak and full load efficiency. All other moderate current ripple converters lower in the table have lower gain than the proposed converter, and many have low or moderate efficiency, with some requiring 2 inductor cores. Thus, considering converters with low or moderate current ripple and one inductor core, the proposed converter has the highest gain along with efficiency approximately equal to the other highest-efficiency converters. Figure 3-15 shows the voltage gain of the proposed converter compared to other converters with low or moderate current ripple and one inductor core. Overall, the proposed converter stands out from prior work as a well-rounded candidate for many cost-sensitive applications, including PV and fuel cells, where improved input current the table, including switch rise and fall times, switch on-ripple is required, along with high voltage gain, low component count, and high efficiency.

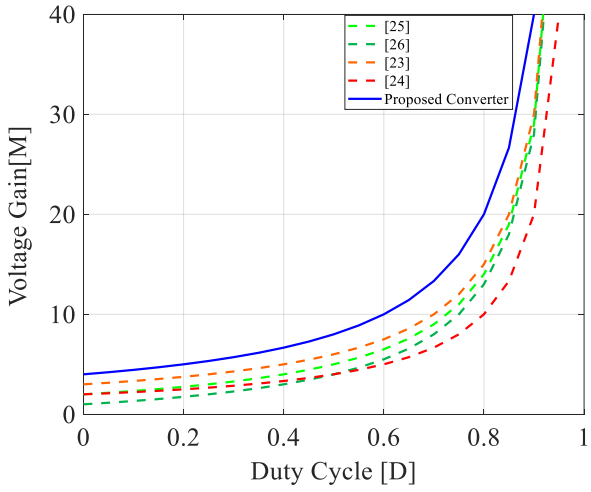


Figure 3-15: Voltage gain comparison of converters with low or moderate input current ripple and one inductor core

3.7 Summary

This chapter presents a high-efficiency, high-gain DC-DC converter that utilizes a single switch and a single coupled inductor core. Most importantly, it has a boost-type input structure that allows for improved input current ripple compared to similar converters with a pulsed input current. This reduces the need for extensive input filters in current-ripple-sensitive applications, thus improving overall power density and reducing system cost. Experimental results from the 200 W prototype show an average efficiency of 96.5% and a maximum efficiency of 97.1%, even with 100 kHz switching frequency.

High step-up converters are crucial in many power electronics interfaces, including for renewable energy sources. As the result of topological variation of high step-up converters, many topologies share similar characteristics. To have a clear understanding of an optimized design that makes the best use of components to achieve high gain, it is necessary to devise a generalized comprehension method for high step-up converters. This chapter presents a novel generalized method for analyzing single-switch step-up converters that can include switched capacitor (SC) cells, a coupled inductor (CI), and/or voltage multiplier cells (VMC). The proposed method is not dependent on the position of the CI nor the structure of the VMC and is not tied to a specific topology. Thus, the proposed generalized method uniquely reveals the unifying theory underlying high step-up converters with any variation of SC/CI/VMC. In order to verify the theoretical analysis, many examples from the literature are investigated. Then, using design tips from the generalized method, a new high step-up converter is designed. A 150 W prototype of the converter shows 97.5% peak

efficiency. The proposed converter also compares favorably to other topologies in both a power loss breakdown analysis and a component stress factor analysis.

Table 3-3: Comparison of High Step-Up Converters with One Switch

Converter	Converter Type	Input Current Ripple	Voltage Gain	Voltage Gain (D=0.5, n=1)	Voltage Gain (D=0.5, n=2)	Switch Voltage Stress	N_S	N_D	N_C	N_L	Maximum Reported Efficiency	Full Load Efficiency	T_{rise}/T_{fall} (ns)/$R_{ds,on}$(mΩ)	f_{sw} (kHz)	Power V_{in}/V_{out}
[19]	Interleaved SC	Low	$\frac{3}{1-D}$	6	6	$\frac{V_O}{3}$	1	8	5	3	94.8%	94%	16/45/25.5	20	800 W 100/400 V
[20]	Interleaved SC	Low	$\frac{2}{1-D}$	4	4	$\frac{V_O}{2}$	1	4	4	2	95.21%	92%	28/30/33	50	1000 W 50/400 V
[21]	Quasi-Z Source	Moderate	$\frac{(2+D)}{(1-2D)}$	25*	25*	$\frac{V_O}{2+\mathrm{D}}$	1	5	7	3	92.8%	91.2%	17/48/40	40	150 W 24/365 V
[8]	CI Quadratic	Moderate	$\frac{n+2}{(1-D)^2}$	12	16	$\frac{\mathrm{V_O}}{n+2}$	1	5	5	3	87.0%	84%	17/48/40	50	72 W 11/120 V
[22]	CI Quadratic	Moderate	$\frac{n(3D+2)+2-D}{2(1-D)^2}$	10	17	$\frac{2(1-D)^2V_o}{n(3D+2)+2-D}$	1	6	5	2	93.14%	92.96	17/48/40	50	250 W 24/400 V
Proposed Topology	CISC	Moderate	$\boldsymbol{\frac{3+n}{1-D}}$	8	10	$\boldsymbol{\frac{V_O}{3+n}}$	1	5	5	1	97.1%	96.3%	43/13/5	100	200 W 36/400 V
[23]	SC	Moderate	$\frac{3}{1-D}$	6	6	$\frac{V_O}{3}$	1	5	5	1	93.85%	93%	15/5.5/150	50	75 W 30/200 V
[25]	CISC	Moderate	$\frac{n(D+1)+1}{(1-D)}$	5	8	$\frac{V_O}{n(1+D)+1}$	1	4	4	1	97%	97%	36/57/14.5	50	150 W 35/400 V
[10]	CISC	Moderate	$\frac{1+(\mathrm{D}+1)\mathrm{n}}{1-D}$	5	8	$\frac{V_O}{n(1+D)+1}$	1	4	5	2	97.1%	96.2%	26/78/5.6	88	200 W 25/400 V
[9]	Quasi-resonant	Moderate	$\frac{(1+n)}{(1-D)}$	4	6	$\frac{V_O}{1+\mathrm{n}}$	1	3	4	2	93.8%	89%	18/56/52	100	100 W 18/200 V
[26]	CISC	Moderate	$\frac{1+(\mathrm{n}+1)\mathrm{D}}{1-D}$	4	5	$\frac{V_o}{1+D+nD}$	1	5	4	1	95.15%	93.6%	20/55/4.8	15	150W 18V/200V
[24]	SC	Moderate	$\frac{2}{1-D}$	4	4	$\frac{V_O}{2}$	1	4	3	1	94.45%	90%	24/25/40	20	300 W 40/300 V
[11]	SC	Moderate	$\frac{2-\mathrm{D}}{1-D}$	3	3	$\frac{2V_O}{2+\mathrm{D}}$	1	2	2	2	94.5%	94%	30/65/8	100	100 W 30/90 V
[30]	CISC	Pulsating	$\frac{3+2n}{1-D}$	10	14	$\frac{V_O}{2n+3}$	1	5	5	1	96.7%	95.5%	15/17/2.3	100	200 W 30/380 V
[31]	CISC	Pulsating	$\frac{4+n(2-D)-D}{(1-D)}$	10	13	$\frac{V_O}{4+n(2-D)-D}$	1	8	8	1	97%	94%	41/74/8	40	200 W 30/400 V
[32]	CISC	Pulsating	$\frac{2+n(3-D)}{1-D}$	9	14	$\frac{V_O}{2+n(3-D)}$	1	5	5	1	96.5%	91.8%	41/74/8	50	200 W 24/400 V
[33]	CISC	Pulsating	$\frac{n(1+D)+2}{(1-D)}$	7	10	$\frac{V_o}{2+n+nD}$	1	4	4	1	96.9%	96%	17/48/40	60	300W 40/400V
[34]	CISC	Pulsating	$\frac{n+2}{(1-D)}$	6	8	$\frac{V_o}{n+2}$	1	3	3	1	96.4%	96.1%	35/9/9.2	100	100 W 45/380 V

* D=0.4, since D=0.5 is not feasible for these converters ** Color-coding for comparison: (1) Gain: gain < total components/2 is red, gain < (total components/2)+1 is yellow, gain > (total components/2)+1 is green. (2) Efficiency: Eff>= 96% is green, 94%<Eff<96% is yellow, Eff<94% is red.

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Chapter 4

A Generalized Method for Comprehension of High Step-Up Converters with Switched Capacitors, Coupled Inductors, and Voltage Multiplier Cells

High step-up converters are crucial in many power electronics interfaces, including for renewable energy sources. As the result of topological variation of high step-up converters, many topologies share similar characteristics. In order to have a clear understanding of an optimized design that makes the best use of components to achieve high gain, it is necessary to devise a generalized comprehension method for high step-up converters. This chapter presents a novel generalized method for analyzing single-switch step-up converters that can include switched capacitor (SC) cells, a coupled inductor (CI), and/or voltage multiplier cells (VMC). The proposed method is not dependent on the position of the CI nor the structure of the VMC and is not tied to a specific topology. Thus, the proposed generalized method uniquely reveals the unifying theory underlying high step-up converters with any variation of SC/CI/VMC. In order to verify the theoretical analysis, many examples from the literature are investigated. Then, using design tips from the generalized method, a new high step-up converter is designed. A 150 W prototype of the converter shows 97.5% peak efficiency. The proposed converter also compares favorably to other topologies in both a power loss breakdown analysis and a component stress factor analysis.

4.1 Introduction

High step-up converters are increasingly in demand for a variety of applications, including sustainable energy, lasers, X-rays, and radar [1]. For example, in the growing solar energy sector, a high voltage step-up is needed between the solar modules, which often operate in the range of 15 – 50 V [2], and the grid or storage battery. For vehicle on-board solar generation, the voltage must be boosted to the traction battery voltage, usually 300 – 450 V [3], [4].

The conventional boost converter requires a high duty cycle to provide high gain, but the achieved voltage boost and the efficiency are degraded at high duty cycles due to parasitic losses, including high conduction losses and high switching losses that are proportional to the output voltage. Furthermore, since the switch voltage rating is equal to the output voltage, a high voltage-rated switch is required, which increases converter cost and reduces efficiency due to the high $R_{ds(on)}$.

In order to achieve a high step-up voltage ratio, high efficiency, and low voltage and/or current stress of active and passive devices, different techniques have been proposed in the literature, such as switched capacitor (SC) cells, coupled inductor (CI) cells, voltage multiplier cells (VMC), active networks, and quadratic converters. Coupled inductors are often useful when cascading two or more converters to achieve high gain. Many articles in the literature present novel topologies and compare them with well-known converters. While these contributions are useful, most do not provide a more generalized understanding of the circuit. As a result, some papers may even present circuits which are a topological variation of others presented in past years, without knowing they symbolized the same concept.

Some prior work has focused on the design methodology, review, and comprehension methods of high step-up converters [5]-[8]. However, some of these focuses more on classification and none give a unified generalized view of methods applied to a wide range of topologies. For example, [5] reviews different variations of CI structures combined with SC cells. As an example, a Cockcroft-Walton VMC is combined with a CI. The voltage gain derivation is presented for upstream and downstream growth based on the position of

the dot point of the CI. However, the position of the CI is considered fixed in the converter. Also, [5] only considers specific formulas for specific topologies, and a generalized terminology is not presented.

In [6], a graph with four nodes and 11 branches is defined. Each branch can represent a passive or active device or be a short or open circuit. Twelve possible high step-up converters are proposed based on varying the position of the switches, capacitors, inductors, and diodes. A topology is then selected for voltage gain and stress analysis, but a general voltage gain derivation is not given for the proposed graph. Conversely, in [7], a more generalized basic gain cell including 7 branches is proposed. Different structures are proposed by cascading or integrating the basic gain cell, and a design guideline is given based on the proposed graph. However, this research only investigates the classic voltage step-up methods, so excludes CI and VMC techniques, and does not present a generalized gain derivation. Reference [8] investigates the basic boost CI converter with different VMCs. It assigns two parameters to each VMC for calculating the voltage gain achieved over that of the conventional boost converter, but it does not present a generalized method for obtaining these parameters. Reference [9] provides a synthesis methodology for developing high step-up converters using three step-up techniques: CIs, VMCs, and diode VMCs. In [9], numerous different combinations of these methods are presented, and a formula is given for each converter, yet it does not give a generalized view for all converters. The converters can be cascaded with more VMCs or diode VMCs. However, in all cases, the position of the CI is predetermined. By doing so, many variations are not covered.

This chapter presents a novel generalized method to derive the voltage gain of boost-based converters using SC, CI, and VMC techniques. Compared to the synthesis analysis in [9], the proposed generalized method has the following advantages: (1) Based on the design rules, the CI can be placed in any position in the converter, (2) The equations are related to the general architecture (integrated or cascaded), not the specific topology, and are extracted according to the main loop within the converter; also, the method does not differentiate between cascaded or stacked topologies, (3) It is not specific to the Cockcroft–Walton VMC, and can be used with all VMC cells investigated in the literature, (4) It includes integrated topologies, providing the voltage gain in a generalized approach, and (5) It leads to an underlying understanding of how the gain is achieved, meaning design tips can be extracted to understand how to use the least number of capacitors and diodes to achieve the highest gain. Accordingly, [9] provides formulas for existing topologies, but the proposed generalized method can be used to design new topologies. Thus, the proposed generalized method uniquely reveals the unifying theory underlying boost-based converters with any variation of SC/CI/VMC (with one switch and one CI core), and requires only four equations for gain. No previously published theories can describe the gain of such a wide variety of converter topologies with so few equations.

The proposed generalized method provides a deeper comprehension of these applied techniques, allowing for improved designs that make the best possible use of their active and passive devices to achieve the highest voltage gain. Thus, this chapter's new perspective on high step-up converter design can lead to more optimal converters in terms of cost and efficiency. As an example of this process, this chapter presents a novel

integrated SC-CI converter designed using the proposed generalized method and compares it to other high step-up converters from the literature using a loss breakdown analysis and component stress factor (CSF) analysis.

4.2 Proposed Generalized Method

The proposed generalized method is introduced gradually using each main converter technique, starting with the simplest type and moving in order of increasing complexity: SC, CI, cascaded/stacked structure with SC/CI, integrated structure with SC/CI, and then the addition of VMCs. First, some assumptions and definitions are required for the proposed generalization concept, as follows: (1) All semiconductor devices are ideal, so the voltage drop across diodes and the switch are ignored; (2) All capacitors have equal capacitance (C) and are large enough to hold voltage constant during the switching period; (3) All diodes and the switch have the clamping voltage feature, meaning they should be placed in the converter so that voltage spikes at turn-on and turn-off are avoided; (4) The energy of the leakage inductance should be recycled in one switching period; (5) In order to focus on converters with minimum cost and complexity, only one magnetic core and one switch are considered. However, the proposed generalized method is also applicable to converters with one active switch and other synchronous switches used in place of diodes since the basic operation modes remain the same whether synchronous switches are used or not. The choice of using synchronous switches in place of diodes will vary with the application, since this practice will reduce losses, but increase gate driver cost and control complexity.

To give a better understanding of the proposed generalized method, a conventional boost converter is first analyzed, as shown in Figure 4-1. The boost converter can be considered as a graph consisting of four nodes and seven branches. In the proposed generalized method, all nodes are not the same. Two kinds of nodes are defined: (1) constant voltage (CV) nodes and (2) switching (SW) nodes. CV nodes are connected to a constant voltage, either by capacitors or by direct connection to a voltage source. SW nodes are connected directly to the switch or are connected to the switch via a capacitor. Therefore, in Figure 4-1, nodes 1, 3, and 4 are CV nodes and node 2 is a SW node. Based on this, two types of capacitors can also be defined: (1) capacitors between two CV nodes, or (2) capacitors between two SW nodes, as shown in Figure 4-2. As mentioned earlier, in both cases the voltage across the capacitor remains constant during one switching period. Based on this definition, the capacitor C_O in Figure 4-1 is a CV capacitor.

In this method, the basic gain cell consists of three nodes and two branches, which includes one diode and one capacitor, as shown in Figure 4-3(a). Considering the fact that voltage across capacitors is always constant during one period, if one terminal node of the capacitor is CV/SW, the other terminal node must also be a CV/SW node. Thus, four possible scenarios are considered in Figure 4-3(b)-(e). Scenario (c) is not physically possible due to the natural commutation of the diode. Scenario (e) creates voltage spikes on the diode, leading to the use of higher voltage-rated diodes and the associated higher losses and cost. Therefore, in the generalized design procedure, scenarios (b) and (d) are preferred. Based on this, diodes act as a block that transform a SW node to a CV node or vice versa. Diodes can conduct either at the same time (in sync) as the switch or with the

opposite state of the switch. If a diode is connected directly to a SW node or via a capacitor (switching capacitor) it will conduct in sync with the switch. Otherwise, it will conduct in the opposite state of the switch.

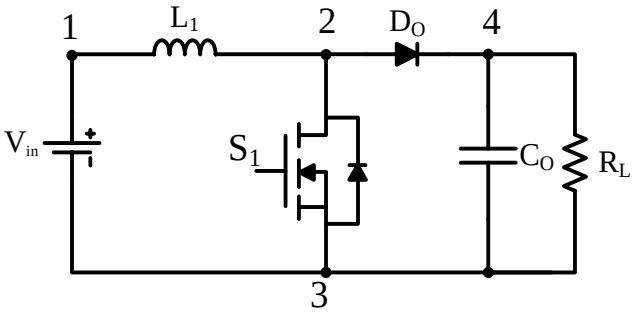


Figure 4-1: Conventional boost converter

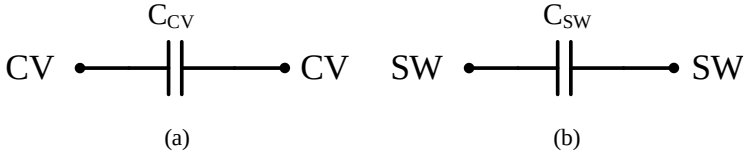


Figure 4-2: (a) Constant voltage capacitor (b) Switching voltage capacitor

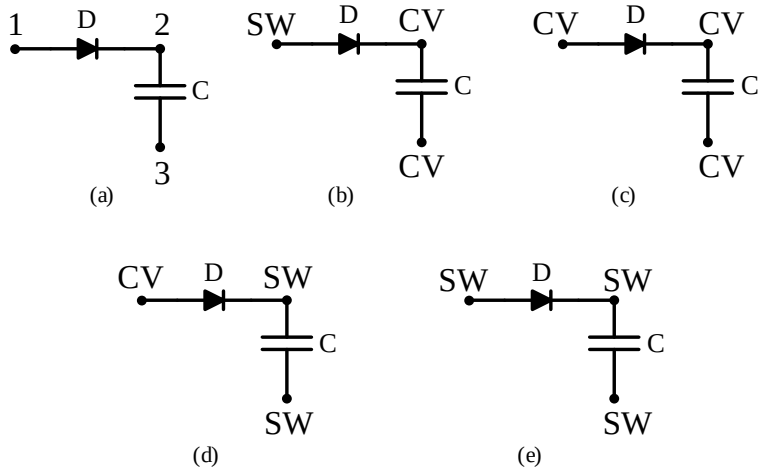


Figure 4-3: Different diode-capacitor structure (a) general three port network (b) SW-CV diode (c) CV-CV diode (d) CV-SW diode (e) SW-SW diode

4.2.1 Switched Capacitor

For switched capacitor step-up converters, the proposed generalized method gives the voltage gain, *M*, as (1),

$$M = \frac{1 + K_1 - K_2 D}{1 - D} \tag{1}$$

where *D* is the switch duty cycle, K_1 is the number of switching capacitors, and calculating K_2 requires a further discussion of SW nodes, as follows. Starting from the traditional boost converter, a SW node in the network can be made by one of two methods: (1) Using a diode with its anode connected to a constant voltage (like the input voltage source in Figure 4-4 (a)), and its cathode connected to a capacitor which makes it a switching capacitor type. In Figure 4-4(a) and (c), the switching capacitor C_1 (named lift capacitor), is created by this method. The voltage on this capacitor clamps on input voltage due to the use of this diode. As a result, it creates a (-D) factor in the gain cell. In this case, $K_2 = 1$; (2) Using a capacitor which is connected to a SW node, for example the main SW node, node 2 in Figure 4-1, and the other node also will be a SW point based on the fact that the capacitor voltage is constant during one switching period. In Figure 4-4(b), C_2 is generated by this method. In this case, $K_2 = 0$.

Figure 4-4 presents multiple SC converter examples [9]-[12], where red dots show SW nodes and SW capacitors are circled by a red dashed line. Table 4-1 summarizes the gain expression of each converter as derived from (1), which matches the gain expressions given in [9]-[12]. Cascading from a basic SC converter, it can be deduced that the number of diodes after the main switching node is always an odd number and the number of diodes before the main switching node is always even. Based on the requirements of the

application, power density, and cost, more SCs can be added to the design to increase voltage gain. However, SC cells can also be used with a CI and VMC, generating positive coupling, as investigated in the next sections.

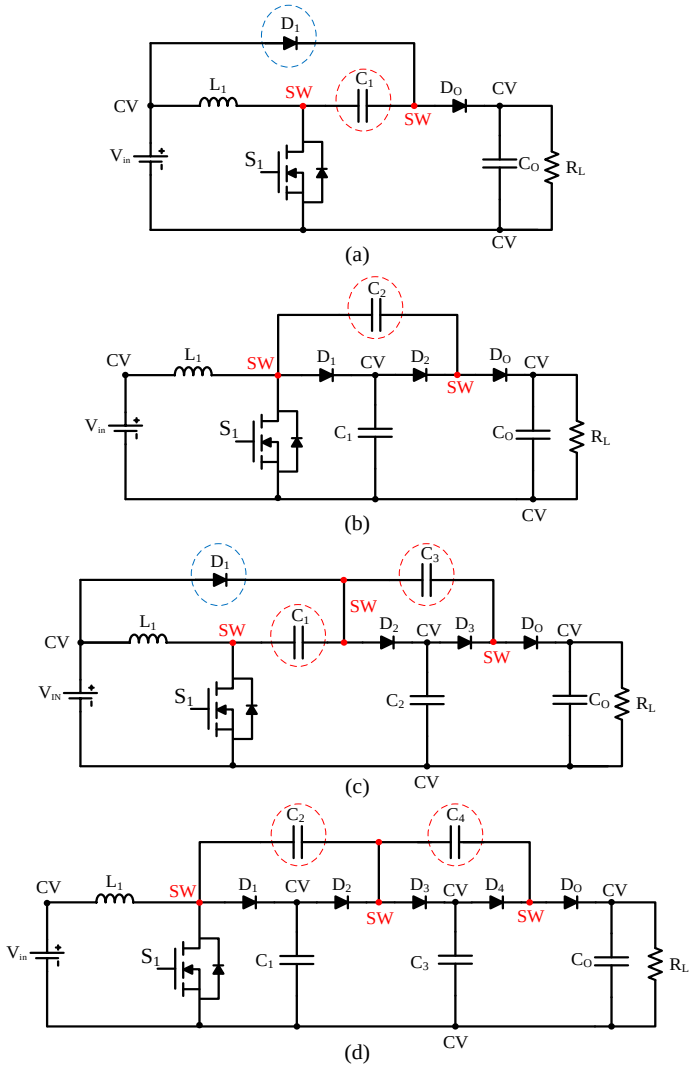


Figure 4-4: Switched-capacitor (SC) converter examples (a) 2D-2C converter [10], (b) 3D-3C converter [11], (c) 4D-4C converter [11], (d) 5D-5C converter [12]

4.2.2 Coupled Inductor

A similar approach will be adopted with some adjustment for the CI technique. Figure 4-5 shows the basic CI converter. A CI can increase the voltage gain without the

need for cascading two or more stages to achieve high step-up gain. However, CIs can increase the output diode voltage stress and cause more winding losses. The energy stored in the leakage inductance is naturally recycled by a SC cell, which prevents severe voltage spikes on the switch after turn-off.

Table 4-1: Characteristics of Basic SC Converters

	K_1	K_2	M
Fig. 1	0	0	$\frac{1}{1-D}$
Fig. 4 (a)	1	1	$\frac{2-D}{1-D}$
Fig. 4 (b)	1	0	$\frac{2}{1-D}$
Fig. 4 (c)	2	1	$\frac{3-D}{1-D}$
Fig. 4 (d)	2	0	$\frac{3}{1-D}$

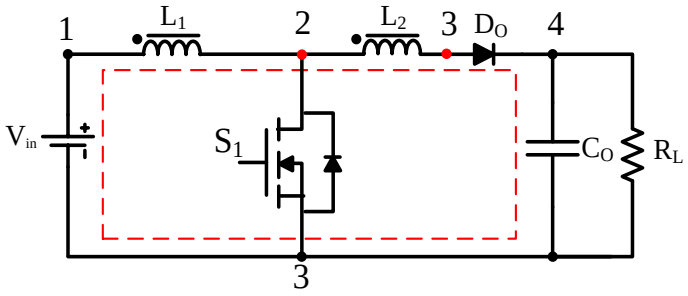


Figure 4-5: Basic coupled inductor (CI) converter [13]

However, after turning on the switch, this inductance starts to resonate with the parasitic capacitance of the diodes, resulting in overvoltage spikes on the diodes and switch, which creates a need to use more clamping circuits. Two clamping methods are shown in Figure 4-6. Diodes which are conducting at the same time as the switch are shown in gray.

In the proposed generalized method, the main loop is defined as a loop which consists of the CI primary and secondary and diodes which turned on in the opposite state of the switch. If there is no path including primary and secondary, only primary can be considered. The CIs can be placed between two SW nodes or one SW and one CV node as a result of the volt-second balance of the inductor. The main loop is shown in Fig. 6 by a red dashed line. As can be seen in Figure 4-6, the clamp circuits do not change the main loop structure so they will not change the gain of the simple CI presented in Figure 4-5.

The CI technique can be used in two more advanced ways: cascaded/stacked with SC converters or integrated with SC converters. In the integrated technique, the secondary side is a part of the SC cell. However, in the cascaded/stacked version, the secondary side is separate from the SC cell, and can be placed either before or after the SC cell.

4.2.3 Cascaded/Stacked Structure

In a cascaded structure the secondary side of the CI is cascaded with the boost gain cell. Figure 4-7 presents the general structure of a cascade CI topology. The proposed generalization method gives the voltage gain of a SC+CI cascaded converter as (2), which has the extra term +ND over (1),

$$M = \frac{1 + K_1 - K_2 D + ND}{1 - D} \tag{2}$$

where N is the turns ratio of the CI. The factor of ND is the effect of the secondary side voltage added to the gain of the SC cell.

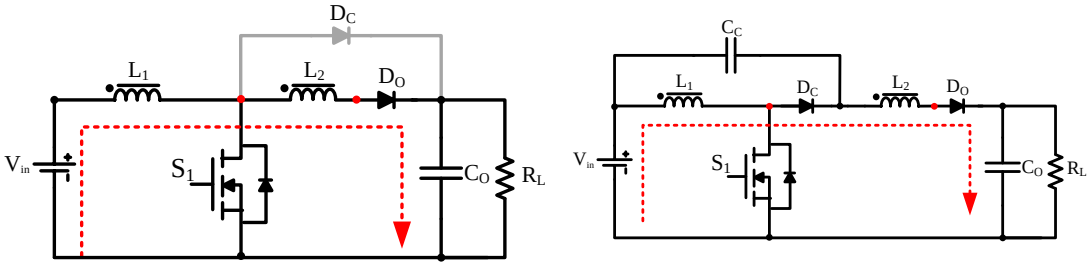


Figure 4-6: Basic CI converter with clamp circuit (a) [14] (b) [15]

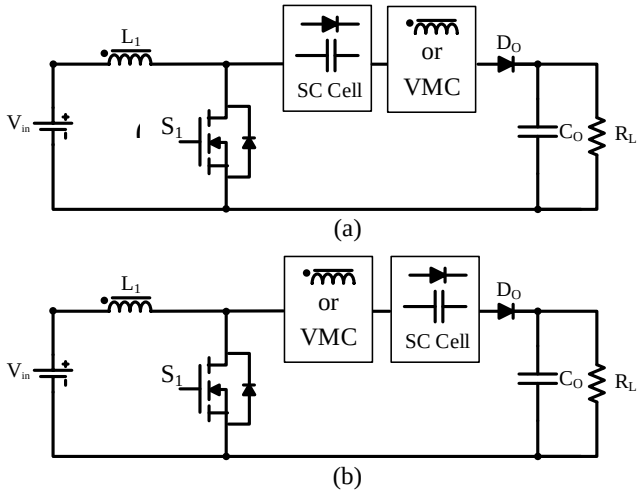


Figure 4-7: General cascade structure (a) SC+CI (b) CI+SC

Figure 4-5 represents the most basic cascade structure as it does not have a SC cell. Based on the analysis, there is no switching capacitor in the structure so $K_1 = 0$. Also, the lift capacitor doesn't exist, so $K_2 = 0$. As a result, the voltage gains for Fig. 5 based on (2) can be expressed as,

$$M = \frac{1 + ND}{1 - D} \tag{3}$$

A basic SC+CI cascaded converter is shown in Figure 4-8[16]. The SC cell consists of D_1, D_2, C_1, and C_2. The secondary side inductor is cascaded after the SC cell. The main

loop is shown as a red dashed line. There is only one switching capacitor so $K_1 = 1$. Also, the lift capacitor does not exist so $K_2 = 0$. Thus, using (2), the voltage gain can be expressed as (4), which agrees with the gain given in [16].

$$M = \frac{2 + ND}{1 - D} \tag{4}$$

When the cascaded SC cell comes after the CI secondary, as in Figure 4-7(b), the voltage gain of the CI+SC converter can be expressed as (5),

$$M = \frac{1 + K_1 - K_2 D + ND + K_1 N}{1 - D} \tag{5}$$

Comparing with (2), (5) has an extra $+K_1N$. As an example, the converter proposed in [17] is investigated, as shown in Figure 4-9. Figure 4-9 shows that the symmetrical SC structure comes after the CI secondary. In this structure, there are two switching capacitors which are both in the main loop, C_2 and C_3. Thus, $K_1 = 2$ and there is no lift capacitor so $K_2 = 0$. As a result, the voltage gain is calculated using (5) to obtain (6), which is consistent with the voltage gain presented in [17].

$$M = \frac{3 + 2N + ND}{1 - D} \tag{6}$$

The difference between (2) and (5) comes from the fact that the switching capacitors in a CI+SC converter, for example in Figure 4-9, will charge with both primary and secondary side in series with each other. As a result, these capacitors will charge to higher voltages. However, for SC+CI, for example in Figure 4-8, the switching capacitor will charge only with primary side voltage. Thus, at a fundamental level, CI+SC converters can achieve higher voltage gains than SC+CI converters with similar component counts.

The basic stacked CI structure is shown in Figure 4-10. The only difference is that the output capacitor now consists of C_{O1} and C_{O2}, and consequently the main loop consists of two loops on the primary and secondary sides. The voltage gain is the same as the general SC+CI cascaded converter, as shown in (2). By substituting $K_1 = 0$ and $K_2 = 0$, the gain simplifies to (3), which is consistent with the voltage gain presented in [18].

4.3 Integrated Structure

In this structure, the CI is integrated directly into the SC cell. Figure 4-11 illustrates the general form of this topology. In general, the voltage gain of an integrated structure using CI and/or SC can be expressed as,

$$M = \frac{1 + K_1 - K_2 D + (K_3 - K'_2)ND}{1 - D} + NK_3 \tag{7}$$

where K_3 is the number of switching capacitors in the main loop, and K_2' = 1 only if the lift capacitor exists and is placed in the main loop. It should be noticed the multiplier of ND only depends on capacitors that exist in the main loop. It can be used as a factor to increase the core utilization in design procedures.

A basic integrated SC+CI is shown in Figure 4-12 [19]. In this topology, the secondary side inductor is integrated with the SC cell, in series with capacitor C_2. The only switching capacitor, C_2, is placed in the main loop. Based on the proposed generalization method, $K_1 = 1$, $K_2 = 0$, $K_2' = 0$, and $K_3 = 1$. Thus, based on (7), the voltage gain for the converter in Fig. 12 is derived as (8), which agrees with the gain given in [19].

$$M = \frac{2 + ND}{1 - D} + N = \frac{2 + N}{1 - D} \tag{8}$$

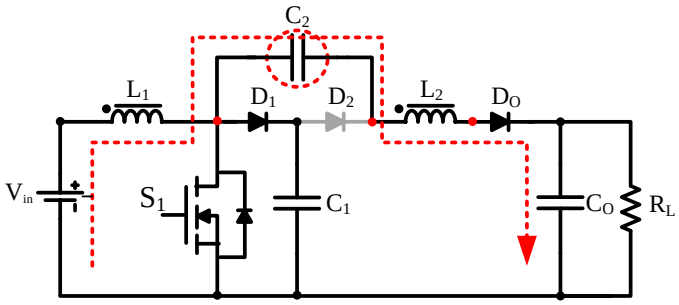


Figure 4-8: Basic SC+CI cascade structure [16]

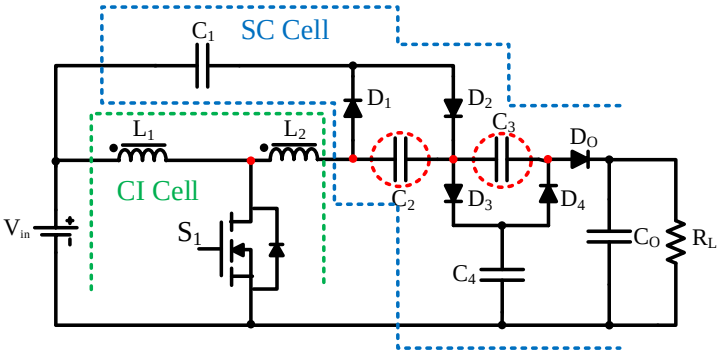


Figure 4-9: Basic CI +SC cascaded structure [17]

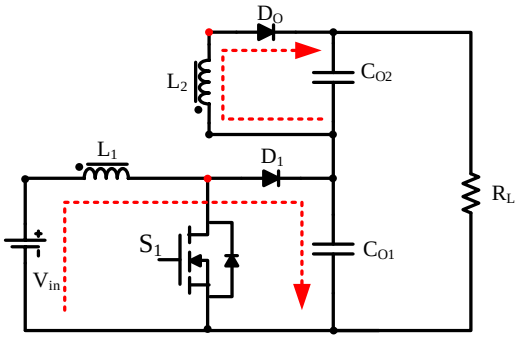


Figure 4-10: Basic SC+CI stacked structure [18]

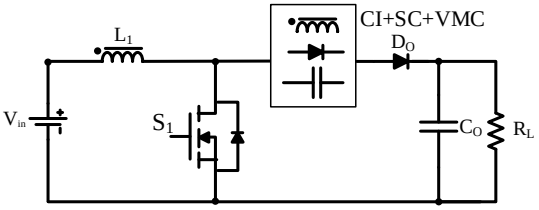


Figure 4-11: General integrated structure

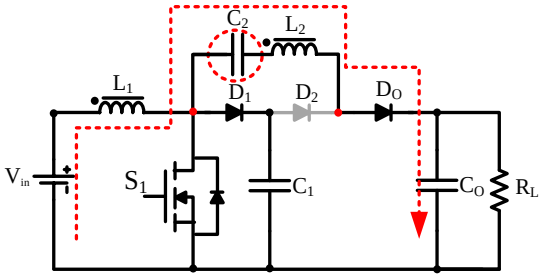


Figure 4-12: Basic SC+CI integrated structure [19]

In some cases, the CI structure is integrated with VMCs. Some of the most well-known VMCs are presented in Figure 4-13 [6]. In order to have a simple analysis of VMCs, they can be replaced with a simple CI in the position of their CI, considering the gain cell as an additional circuit. Then, they can be solved as cascaded/stacked or integrated based on the position of their secondary side inductance. The voltage gain of a converter with a VMC cell can be expressed as (9),

$$M = M_{without-VMC} + K_4 N \tag{9}$$

where K_4 is the number of capacitors that the VMC introduces to the circuit. It should be noticed that these capacitors should be counted even if they are not switching capacitors (C_a in Figure 4-13(d)). Table 4-2 summarizes the K parameters used in the generalized gain equations.

Figure 4-14 (a) shows a basic VMC integrated with a CI [20]. Based on the proposed method, replacing the VMC with a simple CI result in the circuit in Fig. 5, with the voltage gain as expressed as (3). Only one capacitor is added by the VMC (C_1) so $K_4 = 1$. According to (9), the voltage gain can be expressed as (10), which agrees with the gain given in [20].

$$M = \frac{1+ND}{1-D} + N = \frac{1+N}{1-D} \tag{10}$$

In Figure 4-14 (b), a VMC is integrated with an integrated SC+CI converter. Replacing the VMC with a CI result in the simple integrated CI converter shown on the left side of Figure 4-14 (c). The integrated converter in Figure 4-14 (c) has one switching capacitor in the main loop (C_2) so $K_1 = 1$, $K_2 = 0$, $K_3 = 1$. Based on (7) the gain can be expressed as $M_{without\text{-}VMC}$ and since the VMC on the right side of Figure 4-14 (c) only introduces one capacitor in the main loop, the voltage gain based on (9) is,

$$M = M_{without-VMC} + N = \frac{2+N}{1-D} + N = \frac{2+2N-ND}{1-D} \tag{11}$$

For a stacked converter, the same rule applies. Figure 4-15 shows a VMC stacked with a conventional boost converter including a CI. Based on the proposed generalized method, replacing the VMC by a simple CI result in the circuit in Figure 4-10, which has voltage gain expressed by (3). Then, based on (9), and since there are two capacitors in the original VMC, the gain can be expressed as (12), which agrees with the gain given in [22].

$$M = \frac{1+ND}{1-D} + 2N = \frac{1+2N-ND}{1-D} \tag{12}$$

In summary, the generalized method proposes three main equations to express voltage gain: (2) for cascaded/stacked SC+CI, (5) for cascaded/stacked CI+SC, and (7) for integrated SC/CI. Equation (1) for SC converters can be derived from (2), (5), or (7) by setting N = 0 since there is no CI. Furthermore, a fourth equation, (9) is introduced to allow for the analysis of converters with VMCs using (2), (5), or (7) depending on the converter structure.

Table 4-2: Summary of K Parameters in Generalized Gain Equations

Parameter	Definition
K_1	Number of switching capacitors
K_2	= 1 if lift capacitor exists, = 0 otherwise
K_2'	= 1 if lift capacitor exists in the main loop, = 0 otherwise
K_3	Number of switching capacitors in the main loop
K_4	Number of capacitors in VMC

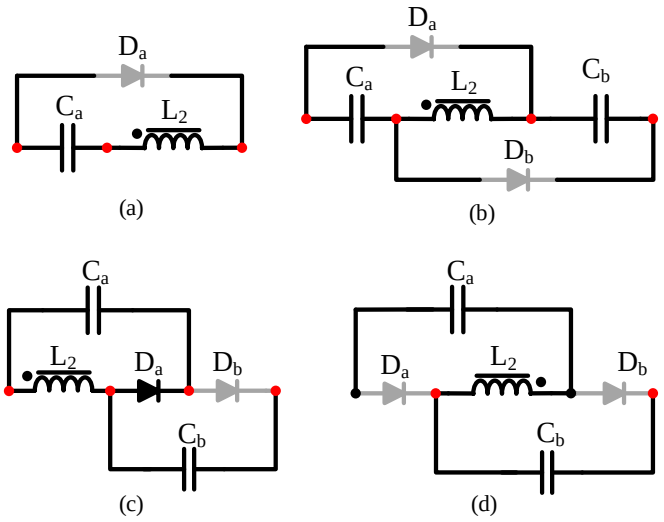


Figure 4-13: Different VMCs integrated with the CI technique [6]

4.4 Circuit Application Examples

In this section, three converters which have been published recently are analyzed using the proposed generalized method. An integrated high step-up SC-CI converter is designed in [23]. This converter is presented in Figure 4-16. This converter employs a SC structure and a VMC which is cascaded after the SC cell. This structure is successful in creating many SW points. However, having only one switching capacitor in the main loop decreases the cost efficiency of integrating with CI and VMC. Also, D_a and D_b are placed

between two switching points which creates severe voltage spikes when turning off the diodes.

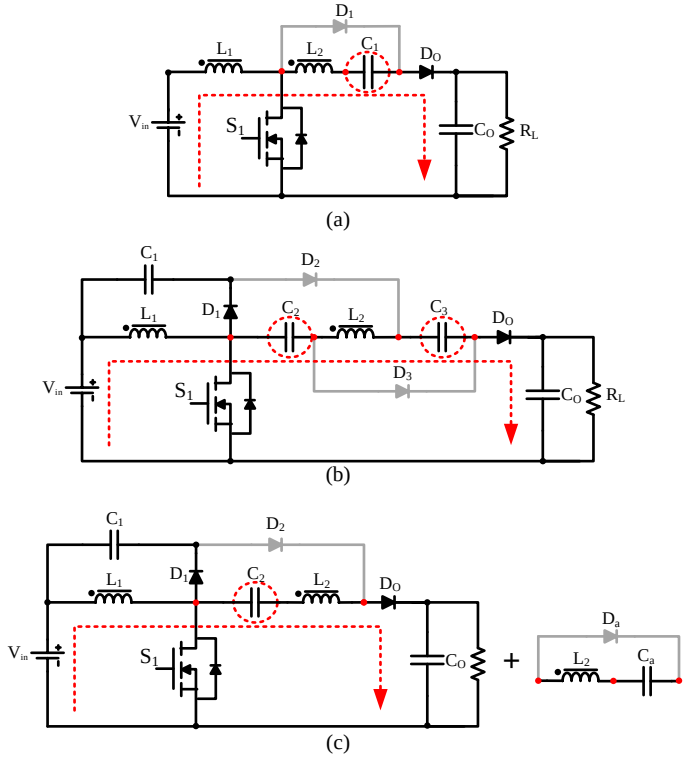


Figure 4-14: Basic integrated VMC+CI [20] (b) integrated SC+CI+VMC [21] (c) simplified circuit after replacing VMC.

According to the proposed generalized method, the VMC can be replaced with a simple CI which is cascaded with the SC converter, making a cascaded SC+CI converter. Based on this, there are three switching capacitors in the converter and a lift capacitor is one of them (K_1=3, K_2=1). As a result, the voltage gain of the simplified cascaded SC+CI converter based on (2) can be expressed as,

$$M_{without-VMC} = \frac{4 - D + ND}{1 - D} \tag{13}$$

Considering the VMC adds two capacitors which increases the voltage gain by 2N, the total gain of the circuit in Figure 4-16: First example from [23] based on (9) is given by (14), which agrees with the gain given in [23].

$$M = \frac{4 - D + ND}{1 - D} + 2N = \frac{4 - D + 2N - ND}{1 - D} \tag{14}$$

As a design exercise, consider if instead of using the VMC, the designer used the integrated method and put the secondary side inductance with positive polarity in series with C_3. Based on (7) for integrated converters, there are three switching capacitors in the converter ($K_1 = 3$). Also, only C_3 among the switching capacitors exists in the main loop so $K_3 = 1$. The lift capacitor exists ($K_2 = 1$), but it is not placed in the main loop ($K'_2 = 0$). As a result, the voltage gain can be derived as (15) using (7),

$$M = \frac{4 - D + ND}{1 - D} + N = \frac{4 - D + N}{1 - D} \tag{15}$$

Although the integrated version in this design exercise provides less voltage gain, it uses only 6 diodes and capacitors instead of 8 diodes and 8 capacitors in the original design. Also, all of the diodes are between SW and CV points which guarantees the absence of severe voltage spikes when diodes turn off.

The second example is an integrated SC+CI converter published in [24], as shown in Figure 4-17. It uses the symmetrical SC cell. There are two switching capacitors in the structure ($K_1 = 2$) and both of them are in the main loop ($K_3 = 2$). Also, no lift capacitor is used in the structure ($K_2 = 0$, $K'_2 = 0$). Thus, the voltage gain from (7) is calculated as shown in (16), which agrees with the gain derived in [24].

$$M = \frac{3 + 2ND}{1 - D} + 2N = \frac{3 + 2N}{1 - D} \tag{16}$$

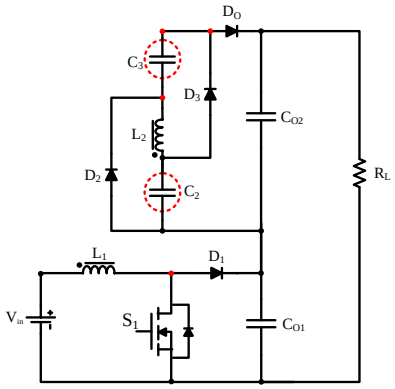


Figure 4-15: Basic Stacked VMC+CI [22]

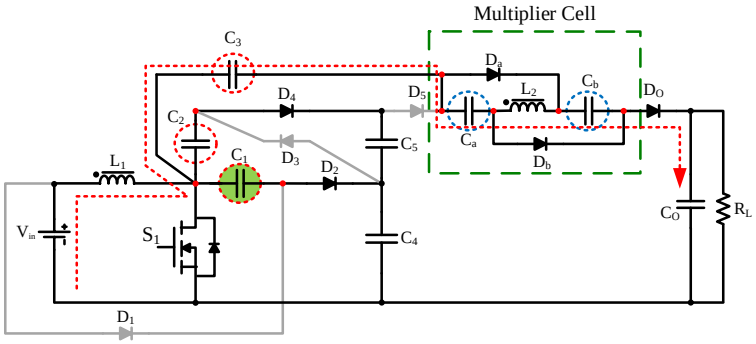


Figure 4-16: First example from [23]

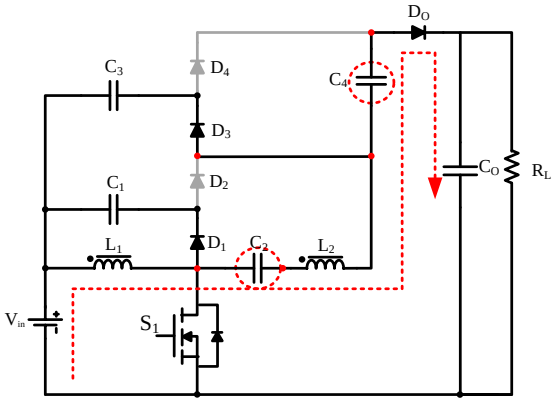


Figure 4-17: Second example from [24]

This converter uses 5 diodes and provides the same gain (at N = 1, D = 0.5) as the integrated converter in Figure 4-16. Although the converter in Figure 4-17 has fewer switching capacitors than the converter in Figure 4-16, it employs both of them in the main

loop. However, in this converter capacitor current will be injected into the input source, making the input current discontinuous.

The third example is a Dickson VMC integrated with CI from [25]. This converter, which is shown in Figure 4-18, can be grown in both upward and downward directions in order to achieve higher voltage gain. Replacing the VMC with its CI, the voltage gain of the equivalent converter results in (3). The VMC introduces two capacitors in the main loop, so the voltage gain based on (9) is shown in (17), which agrees with the gain presented in [25].

$$M = \frac{1+ND}{1-D} + 2N = \frac{1+2N-ND}{1-D} \tag{17}$$

4.5 Proposed Converter Using Generalized Method

4.5.1 Topology and Operation

For some renewable energy sources, an average voltage gain of 12 or higher may be needed. However, operating at higher duty cycles leads to higher losses, and using a higher N lead to higher current stress, higher copper losses, and higher cost. Thus, the design goal is to achieve high gain with moderate D while using a low number of components. The converter analyzed in the first example of Section III has a gain of 10.6 when N = 1.2 and D = 0.5 and uses 8 diodes and capacitors [23]. The converter from the second example has a gain of 10.8 when N = 1.2 and D = 0.5 and uses 5 diodes and capacitors [24]. To increase gain further, both converters would require 2 more diodes and capacitors, as the symmetrical switched capacitor structure uses two diodes and two capacitors, increasing cost and complexity. However, the proposed generalization method shows that by adding

a lift capacitor instead, only one extra diode and one extra capacitor are required to increase gain. Thus, the design of the proposed integrated converter follows these guidelines: (1) Use at least three switching capacitors so $K_1 = 3$; (2) Place all switching capacitors in the main loop so $K_3 = 3$; (3) Use a lift capacitor as one of the switching capacitors to reduce component count compared to using a symmetrical switched capacitor structure so $K_2 = 1$ and $K'_2 = 1$. The resulting proposed topology is shown in Figure 4-19 and the converter can be grown upward for higher gain by adding further capacitor-diode pairs. D_1 and C_1 act as a snubber circuit to absorb the energy of the switch drain-to-source capacitance, dampening the voltage spikes on the switch. The voltage gain is found using (7) for the integrated converter, with the result shown in (18). For N = 1.2 and D = 0.5, the voltage gain is 13 and the converter uses 6 diodes and capacitors.

$$M = \frac{4 - D + 2ND}{1 - D} + 3N = \frac{4 - D + 3N - ND}{1 - D} \tag{18}$$

Figure 4-20 shows the waveforms for analysis of the proposed converter. For simplicity, only Modes II and IV are considered in the analysis below.

Mode II: When the switch is on, D_1, D_3, and D_5 are conducting and D_2, D_4, and D_O are off. Consequently, the primary and secondary sides of the CI are being charged in parallel. At the same time, C_1 is being charged by the secondary side and input source. Also, C_2 and C_3 are being charged by C_4 and C_5.

Mode IV: When the switch is off, D_2, D_4, and D_O are conducting and D_1, D_3, and D_5 are off. As a result, C_1, C_2 and C_3 are in series with the output capacitor C_O and charge the load. C_4 and C_5 are being charged by the secondary side simultaneously.

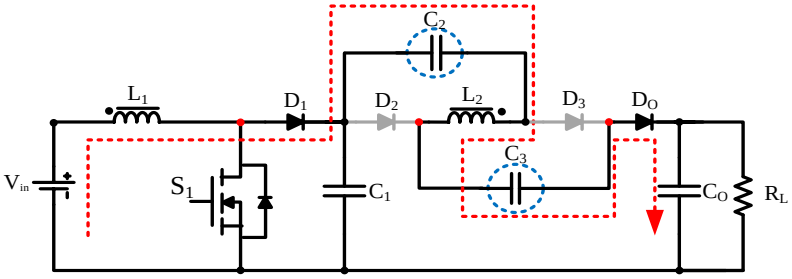


Figure 4-18: Third example from [25]

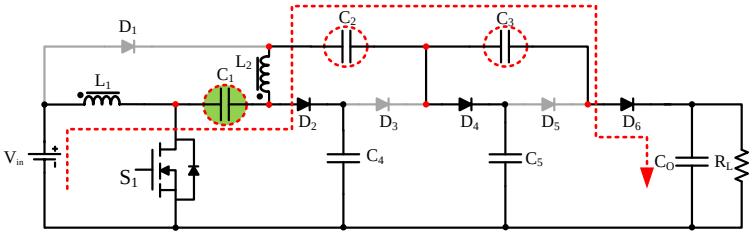


Figure 4-19: The proposed converter

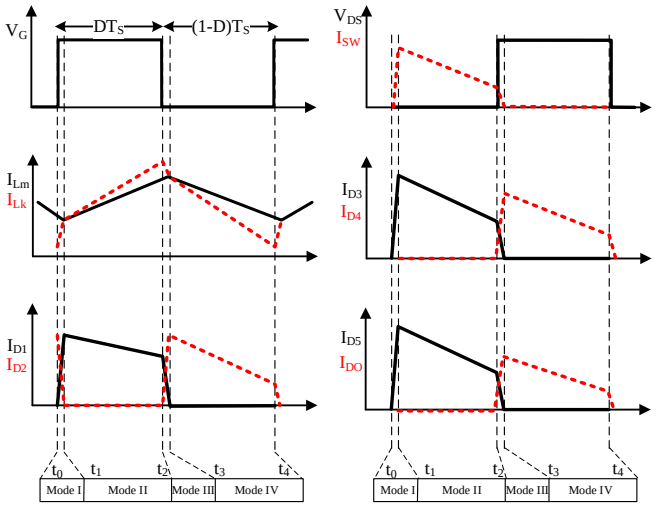


Figure 4-20: Waveform analysis of the proposed converter

4.5.2 Gain Derivation

Based on the assumptions in the previous sections, when the switch is on,

$$v_{L_1} = \frac{v_{L_2}}{N} = kV_{in} \tag{19}$$

where *k* is the coupling factor of the CI. Applying Kirchhoff's voltage law (KVL) at the secondary side results in (20) – (21).

$$V_{C_1} = V_{in} + v_{L_2} = (Nk+1)V_{in} \tag{20}$$

$$V_{C_5} = V_{C_1} + V_{C_2} + V_{C_3} - v_{L_2} \tag{21}$$

Applying (20) in (21) results in,

$$V_{C_5} = V_{in} + V_{C_2} + V_{C_3} \tag{22}$$

In addition, based on the fact that the series connection of C_3 and C_4 are in parallel with C_5,

$$V_{C_5} = V_{C_4} + V_{C_3} \tag{23}$$

At t=DT$_s$ the switch turns off and using KVL for both primary and secondary sides results in (24) – (26) in Mode IV.

$$v_{L_1} = V_{C_1} - V_{C_4} + V_{in} = (Nk+2)V_{in} - V_{C_4} \tag{24}$$

$$V_O = V_{C_3} + V_{C_5} \tag{25}$$

$$v_{L_2} = V_{C_4} + V_{C_2} - V_{C_5} \tag{26}$$

By applying the volt–second balance to L_1 over one switching period using (19) and (24),

$$\int_0^{Ts} v_{L_1} dt = D(kV_{in}) + (1-D)[(Nk+2)V_{in} - V_{C_4}] = 0 \rightarrow V_{C_4} = \frac{[(Nk+2)(1-D)+kD]V_{in}}{1-D} \tag{27}$$

By applying the volt–second balance to L_1 over one switching period using (19) and (26),

$$\int_0^{Ts} v_{L_2} dt = D(NkV_{in}) + (1-D)[V_{C_4} + V_{C_2} - V_{C_5}] = 0 \rightarrow V_{C_5} = V_{C_2} + \frac{[Nk+2+D(2-K))]V_{in}}{1-D} \tag{28}$$

By inserting (22) into (28),

$$V_{C_3} = \frac{1 + Nk + kD - D}{1 - D} V_{in} \tag{29}$$

Based on (29), (27), and (23),

$$V_{C_5} = \frac{2Nk + 3 - D(Nk + 3 - 2k)}{1 - D} V_{in} \tag{30}$$

By inserting (28)-(30) and (20) into (24), the gain in (31) is achieved, which simplifies to the gain given in (18) from the proposed generalized method when k=1.

$$M = \frac{V_O}{V_{in}} = \frac{3Nk + 4 - D(Nk + 4 - 3k)}{1 - D} \tag{31}$$

Figure 4-21 illustrates the gain variation based on changing the duty cycle for different turns ratios compared to that of other state-of-the-art CISC converters. The results show that the proposed converter achieves the highest gain for a given duty cycle and turns ratio. Also, the voltage rating of the capacitors is low and working at high frequency results in lower required values of these capacitors.

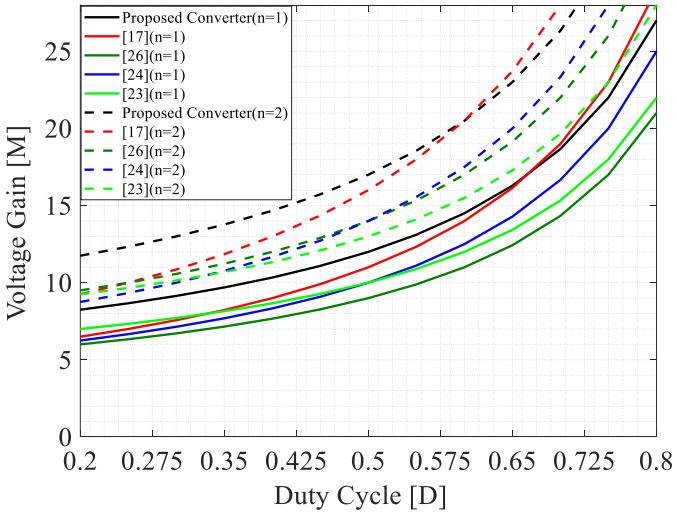


Figure 4-21: Voltage gain versus duty cycle and turns ratio

As a result, smaller capacitors like film capacitors can be used, that have better reliability and longer lifetimes than electrolytic capacitors. Table 4-3 shows the voltage stress of capacitors, diodes, and the switch. The maximum switch voltage stress is 16% of the output voltage when N = 1 and D = 0.5, which allows for the use of lower voltage rated devices, reducing cost and $R_{ds(on)}$.

Table 4-3: Capacitor, Switch, and Diode Voltage Stresses

Component	Rated Voltage	Component	Rated Voltage
C_1	$\frac{(1-D)(N+1)V_O}{4+3N-D(N+1)}$	D_1	$\frac{(N+1)V_O}{4+3N-D(N+1)}$
C_2	$\frac{(1+N-ND)V_O}{4+3N-D(N+1)}$	D_2	$\frac{V_O}{4+3N-D(N+1)}$
C_3	$\frac{(N+1)V_O}{4+3N-D(N+1)}$	D_3	$\frac{(N+1)V_O}{4+3N-D(N+1)}$
C_4	$\frac{(2+N-ND-D)V_O}{4+3N-D(N+1)}$	D_4	$\frac{(N+1)V_O}{4+3N-D(N+1)}$
C_5	$\frac{(2N+3-D(N+1))V_O}{4+3N-D(N+1)}$	D_5	$\frac{(N+1)V_O}{4+3N-D(N+1)}$
Switch	$\frac{V_O}{4+3N-D(N+1)}$	D_O	$\frac{(N+1)V_O}{4+3N-D(N+1)}$

4.6 Experimental Results

Figure 4-22 shows the experimental prototype of the proposed converter. The prototype is rated for 150 W and a 420 V output voltage, with the input varied from 30-42 V. Based on (31), for a desired voltage gain of M = 14, and considering a CI with N = 1, a duty cycle of D = 0.58 is required.

Table 4-4 shows the prototype specifications. The output capacitor is selected to allow 1% voltage ripple at the output. Three inductors MSD1514-123MEB (24μH) are used in series to provide enough inductance for continuous input current. According to the power rating, the programmable load is set to a constant resistance of 1176 Ω.

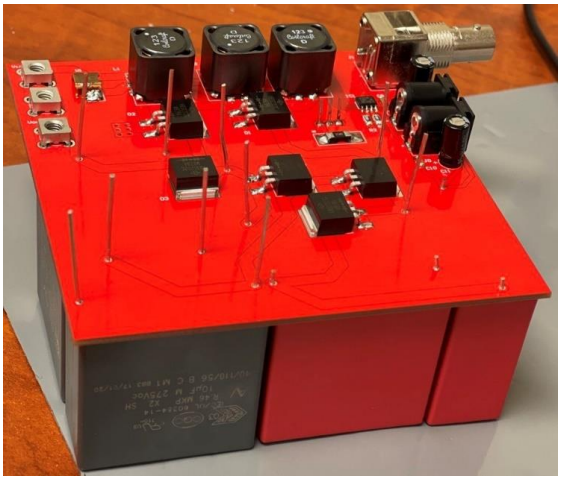


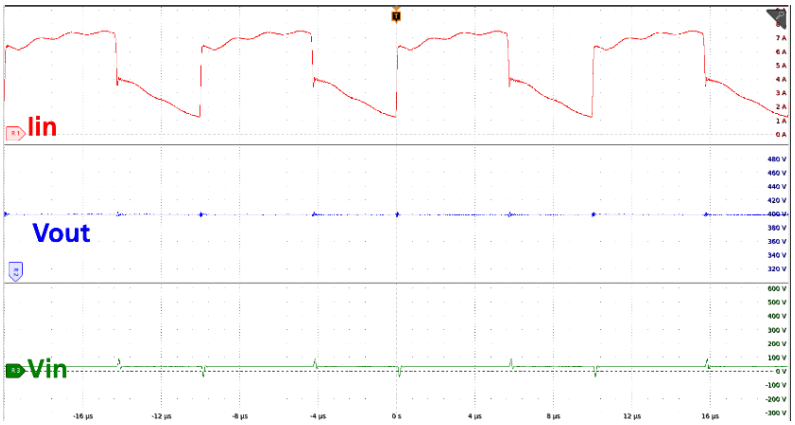
Figure 4-22: Prototype converter

Table 4-4: Experimental Prototype Specifications

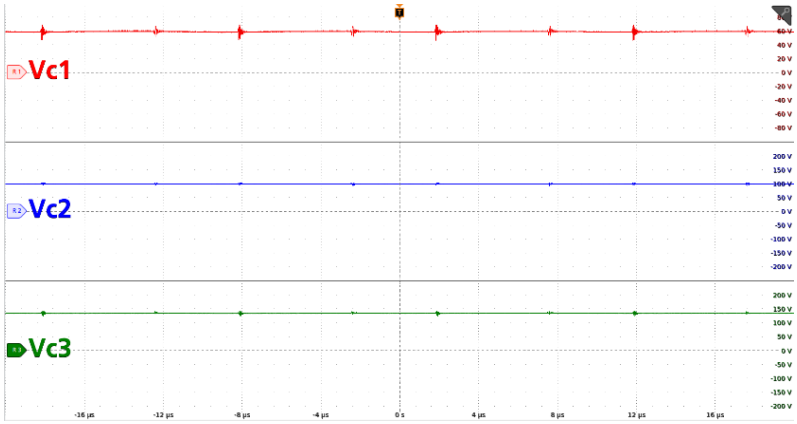
PARAMETER	Value
Input Voltage	30-42 V
Output Voltage	420 V
Nominal Power	150 W
Switching Frequency	100 kHz
Switch	IPP041N12N3 G, N-Channel 120V
Diodes	6 ×VB30202C-M3/8W, 200V, 3A
$C_{1\text{-}4}$	5 × R46KW510050P0M, 10µF Film Capacitor 275V 560V Polypropylene (PP)
C_O	2*B32776E5256K000, 27µF
Inductor	3 × MSD1514-123MEB Series of 1:1 coupled power inductor, L_m=72µH, L_k=1.2µH
Output Voltage Ripple	<1%

Measurements are obtained using Tektronix current and differential voltage probes. Experimental results for V_{in} = 30V, V_{out} = 420 V, and P_{out} = 150 W are shown in Figure 4-23. The output voltage of 420.05 V is achieved with the input voltage of 30.3 V. The output voltage ripple is 3.2 V which results in less than 1% voltage ripple. Figure 4-23 shows that the capacitor voltages are constant during the switching period and are consistent with the capacitor voltage ratings calculated in Table 4-3. Also, the switch voltage stress is 65 V, as seen in Figure 4-23(c). Figure 4-24 shows the measured

experimental efficiency curves for different input voltages and V_{out} = 420 V. The lowest measured efficiency, 96.5%, occurs at maximum power (150 W) and the highest voltage step up (V_{in} = 30V, V_{out} = 420 V), and peak measured efficiency is 98.2%.



(a)



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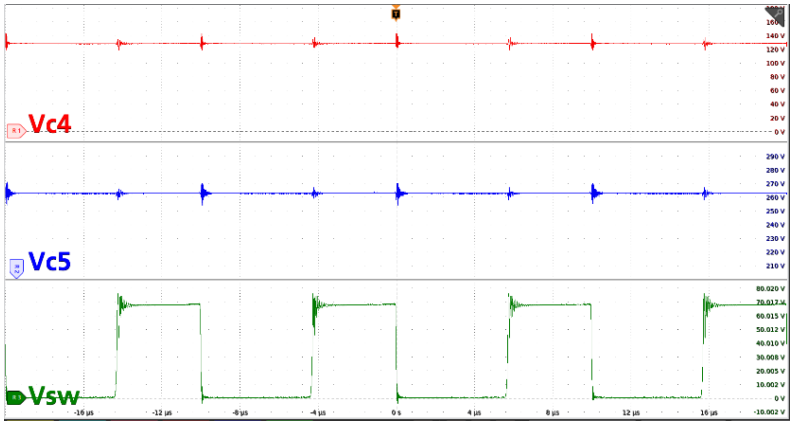

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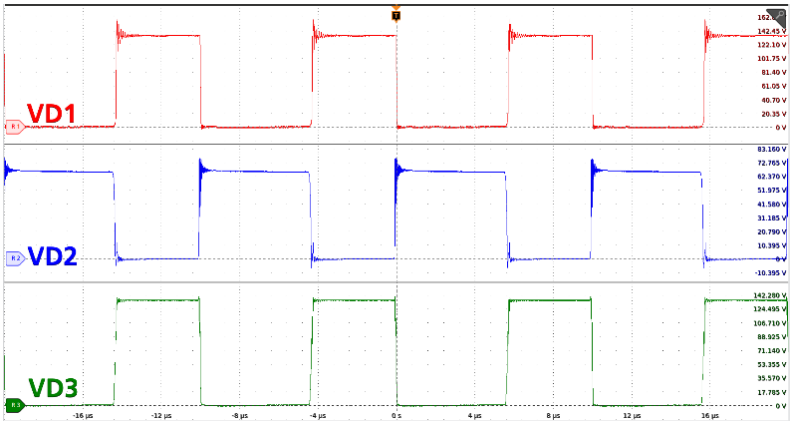
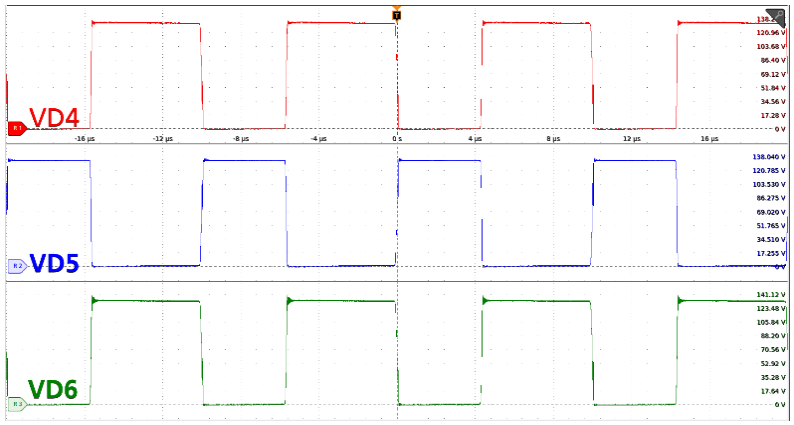


(d)



(e)

Figure 4-23: Measurement results for 150W, V_{in} = 30V, V_{out}= 420V (a) I_{in}, Vout, V_{in} (b) V_{C1},V_{C2},V_{C3} (c) V_{C4},V_{C5},V_{SW} (d) V_{D1},V_{D2},V_{D3} (d) V_{D4},V_{D5},V_{DO}

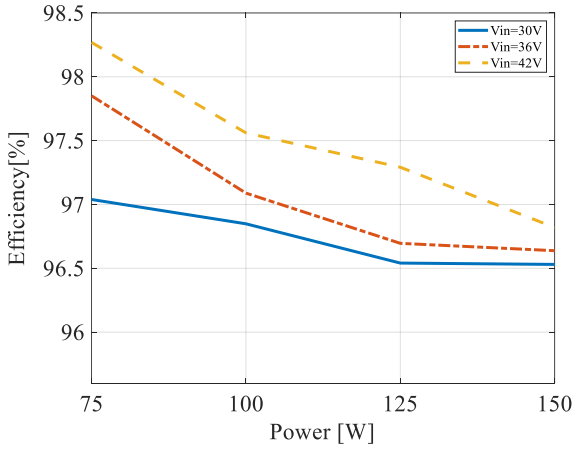


Figure 4-24: Efficiency measurement for Vout = 420 V

4.7 Comparison with Other Converters

In this subsection, the proposed converter is compared to four other promising CISC converters from the literature with one switch and one CI core: (1) [17] cascades a CI with two SC cells, but the leakage inductance doesn't have a path to release its stored energy when the switch turns off, so high turn-off switch voltages occur (Figure 4-9), (2) [23] is a VMC cascaded with three SC cells, two of which are symmetrical, and one that is a super lift cell (Figure 4-16), (3) [24] has three symmetrical SC cells integrated with a CI (Figure 4-17), and (4) [26] has one VMC cascaded with a symmetrical SC cell. Both [17] and [24] have pulsating input currents, meaning larger input filters are required if a smooth input current is desired.

Since it can be inaccurate to compare efficiencies and power densities of converters built by different researchers in different labs (due to different choices of components, switching frequencies, operating points, and measurement equipment) this comparison utilizes a detailed LTSpice simulation of each compared converter, using the same components and operating points, to compare the converters in a fair way. The LTSpice simulations are used to obtain component voltages and currents, which are used for both a loss breakdown analysis and a component stress factor (CSF) analysis. The CSF analysis provides a numerical score for each component type and is a common way to compare converters [9], [27-29], as the CSF is a general indicator of efficiency, cost, and power density since components with lower voltage and current stresses will be more efficient, lower cost, and smaller, while also requiring smaller thermal management systems.

For the loss breakdown analysis all main parasitic losses are considered. All converters are created in LTSpice using IRF6644 switches, RF201LS diodes, C = 33 μF, C_O = 100 μF, N = 1.2, magnetizing inductance L_m = 100 μH, leakage inductance L_k = 1 μH, and capacitor equivalent series resistance (R_{ESR}) is 5mΩ. The operating point is P_{out} = 100 W, V_{in} = 24 V, V_{out} = 400 V, and f_{sw} = 100 kHz. The simulated currents and voltages for each component are used in the loss breakdown and CSF analyses. Diode and capacitor losses are calculated using (32) and (33) respectively where N_D is the number of diodes, N_C is the number of capacitors, and V_F is the forward conducting voltage of the diode.

$$P_D = V_F \sum_{i=1}^{N_D} I_{D,i(avg)} \tag{32}$$

$$P_C = R_{ESR} \sum_{i=1}^{N_C} I_{C,i(rms)}^2 \tag{33}$$

The switch losses are given by (34),

$$P_S = R_{ds(on)} I_{S(rms)}^2 + \frac{1}{2} V_{ds} I_{S(on)} (t_r + t_f) f_{sw} \tag{34}$$

where rise time t_r and fall time t_f are given in the device datasheet. The CI winding and core losses are calculated by the manufacturer using the Coilcraft online calculator for the MSD1514-123MEB series of coupled inductors, and used in (35) to get the total inductor losses, P_L.

$$P_L = P_{winding} + P_{core} \tag{35}$$

The power loss breakdown results are shown in Figure 4-25. The proposed converter has significantly lower switch losses than the other converters, which will reduce the switch heating.

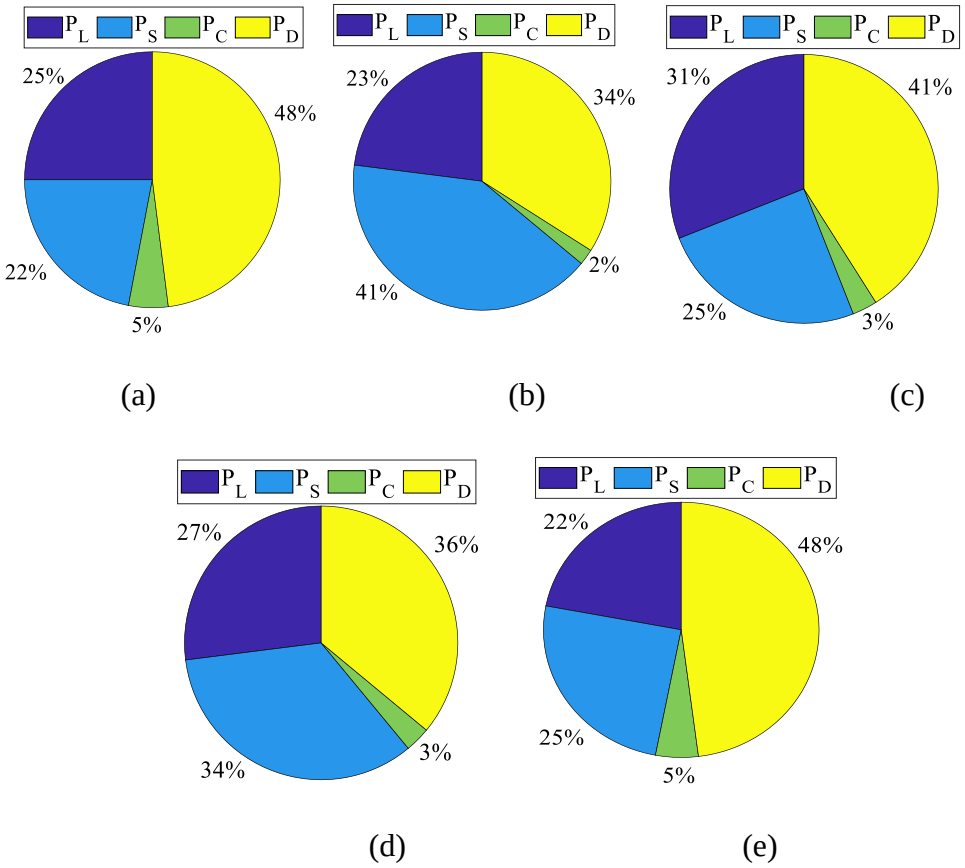


Figure 4-25: Power loss breakdown (a) proposed (Total loss=2.49W, Efficiency=97.6%) (b) [17] (Total loss=3.01W, Efficiency=97.20%) (c) [24] (Total loss=2.47W,Efficiency=97.6%) (d) [26] (Total loss=2.81W, Efficiency= 97.26%) (e) [23] (Total loss=2.34W,Efficiency=96.7%)

These low switch losses occur because the switch has relatively low current stress, and the switch voltage stress is effectively clamped by the series clamp circuit of C_1 and D_2. [17] has the highest switch loss because the topology does not have an effective path for discharging the leakage inductance energy at turn off, and thus there is a high voltage spike on the switch during turn off (120 V experimentally from [17] and 140 V in the LTSpice simulation). However, the proposed converter has higher diode losses than [17], [24], and [26] because of the extra diode. Overall [24] and the proposed converter have the lowest total losses and thus the highest calculated efficiency.

CSF is calculated for all components in (36) – (39), where CSF_S is for the switch, CSF_D is for the diodes, CSF_W is for the inductor windings, and CSF_C is for the capacitors. Also, N_S is the number of switches (one for all converters considered) and N_W is the number of inductor windings. Equation (40) gives the total converter CSF, CSF_T.

$$CSF_S = \sum_{i=1}^{N_S} \frac{V_{S,i(\max)} \times I_{S,i(rms)}}{P_{out}} \tag{36}$$

$$CSF_D = \sum_{i=1}^{N_D} \frac{V_{D,i(\max)} \times I_{D,i(rms)}}{P_{out}} \tag{37}$$

$$CSF_W = \sum_{i=1}^{N_W} \frac{V_{L,i(\max)} \times I_{L,i(rms)}}{P_{out}} \tag{38}$$

$$CSF_C = \sum_{i=1}^{N_C} \frac{V_{C,i(\max)} \times I_{C,i(rms)}}{P_{out}} \tag{39}$$

$$CSF_T = CSF_S + CSF_D + CSF_W + CSF_C \tag{40}$$

The CSF results are summarized in Figure 4-26. Based on the analysis, the proposed converter is best in term of total CSF. Although it uses two more components than [17], [24], and [26], it lowers the voltage stress on the switch and diodes, and the current stress on the switch. In addition, the increased diode-capacitor components increase the CSF_D and CSF_C insignificantly as the voltage stress of the diodes and capacitors reduces. Table 4-5 summarizes the important features of the considered converters, where N_L is the number of CI cores. By using the design tips from the generalized method, a very promising high step-up converter has been developed, which achieves high gain at moderate duty cycles, very high efficiency, and the lowest total CSF of all converters compared, indicating it is comparatively low cost, highly efficient, and power dense.

4.8 Summary

This chapter presented a novel generalized method for analyzing high step-up converters utilizing switched capacitors, coupled inductors, and voltage multiplier cells. The method has proposed three main equations, one for each of cascaded/stacked SC+CI, cascaded/stacked CI+SC, and integrated CISC.

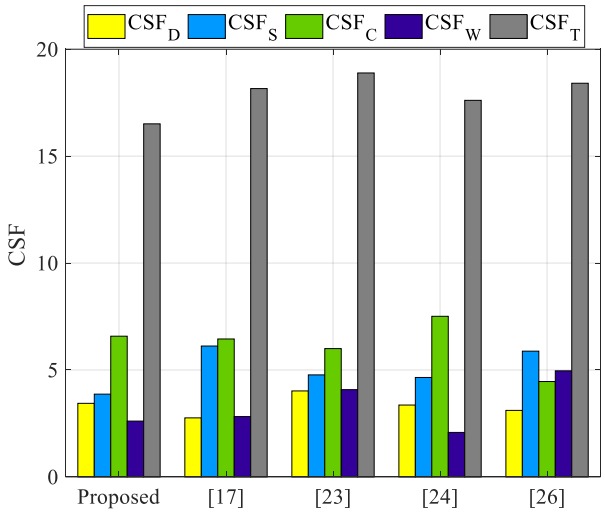


Figure 4-26: CSF breakdown calculation

All of these simplify correctly for a SC converter. Furthermore, a fourth equation is proposed to allow converters with VMCs to be analyzed using one of the three main equations. No prior research in the area of high step-up converters has been able to describe the gain of such a wide variety of converters with so few equations. The proposed generalized method provides insight into the underlying theory unifying these high step-up converters, and thus reveals numerous design strategies to maximize gain for a given number of components. For example, the analysis shows that at a fundamental level, a cascaded/stacked CI+SC converter can achieve higher gain than a cascaded/stacked SC+CI converter because in the latter, the switching capacitor only charges with the primary side

voltage. Furthermore, gain is increased by using more switching capacitors (to increase the value of K_1), and by placing the switching capacitors in the main loop (to increase the value of K_3). Lastly, by employing a lift capacitor as one of the switching capacitors, component count can be reduced compared to using symmetrical switched capacitor structures. Future work will focus on developing further new converter designs utilizing the new understanding provided by the proposed generalized method.

Table 4-5: Summary of CISC Converters with One Switch and One Inductor Core

Converter	Voltage Gain	Duty Cycle (M=16.6, N=1.2)	Switch Voltage Stress	Switch Voltage Stress (M=16.6, N=1.2)	$N_S/N_D/N_C/N_L$	Total CSF
Proposed	$\frac{3\mathrm{N}+4-\mathrm{D}(\mathrm{N}+1)}{1-D}$	0.63	$\frac{V_O}{3\mathrm{N}+4-\mathrm{D}(\mathrm{N}+1)}$	$\frac{V_O}{6.21}$	1/6/6/1	16.51
[17]	$\frac{N(2+D)+3}{(1-D)}$	0.64	$\frac{V_O}{N(2+D)+3}$	$\frac{V_O}{6.17}$	1/5/5/1	18.16
[24]	$\frac{3+2N}{1-D}$	0.685	$\frac{V_O}{2N+3}$	$\frac{V_O}{5.4}$	1/5/5/1	17.61
[23]	$\frac{4+\mathrm{N}(2-D)-D}{(1-D)}$	0.72	$\frac{V_O}{4+N(2-D)-D}$	$\frac{V_O}{4.82}$	1/8/8/1	18.9
[26]	$\frac{2+N(3-D)}{1-D}$	0.73	$\frac{V_O}{2+N(3-D)}$	$\frac{V_O}{4.74}$	1/5/5/1	18.41

4.9 References

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Chapter 5

Novel Integrated Electrical Architecture for Solar-Charged Electric Vehicles

Electric vehicles with on-board solar generation can offer extended driving range and lower grid charging needs than their standard electric vehicle counterparts. The main power electronic challenge in solar-charged electric vehicles (SEVs) is efficiently boosting the low solar voltage to the much higher traction battery voltage. This chapter proposes a novel integrated electric architecture for SEVs which relies on a flying capacitor topology for both battery charging and driving the motor. The on-board solar energy is used to solve the common problem of balancing the flying capacitors, which at the same time helps the solar voltage boost problem since the solar power no longer needs to be boosted to the full battery voltage. Simulation results are presented for a 2.2 kW charging system with 150 V rms input voltage and maximum of 600 W available solar power. The current total harmonics distortion (THD) reduces from 1.37% to 0.36% when the PV structure integrates with the flying capacitor topology.

5.1 Introduction

Electric vehicles (EVs) are a promising solution to help reduce greenhouse gas emissions and air pollution from the transportation sector. However, EVs still face some obstacles such as limited driving range, high battery cost, and long charge times. Therefore, advances that help make EVs more efficient can help society transition to EVs. Adding on-board solar generation to an EV is one way to increase the net efficiency over the day. In the past, low solar generation efficiency was a main obstacle to the concept of solar-charged electric vehicles (SEVs). However, recent advancements have opened new possibilities. For example, current thin-film photovoltaic (PV) cells have a peak efficiency of 23.35% [1]. By integrating PV cells onto all upwards-facing body panels of EVs, large-scale SEVs

offer benefits such as increased driving range and requiring less grid charging electricity. On average, the grid charging demand for a SEV can be reduced by about 20% [2] compared to a standard EV. Some automotive manufacturers are working on on-board PV generation [3] – [5] though most focus on vehicle rooftop solar generation only.

The main power electronic challenge of SEVs is to transfer the solar energy efficiently from the lower voltage PV panel (< 50 V for safety reasons) to the high voltage battery (up to 450 V) when the vehicle is parked or to the high voltage motor inverter while driving. Reference [6] explores two such architectures: (i) a direct high-step up converter from PV to battery and (ii) a step-down converter to the 12 V auxiliary bus with reuse of the isolated bidirectional auxiliary power module. Though the direct high-step up converter achieved higher efficiency of the two, the high voltage gain (9 or more) requires many components, leading to less-than-optimal efficiency. Furthermore, if in the future excess solar energy may be sent back to the grid (if the battery is fully charged and the vehicle is plugged in during the day) [7], consideration of using the on-board charger (OBC) is warranted, to maximize this efficiency path.

OBCs can be galvanically isolated or non-isolated. Conventional isolated OBCs consist of an ac-dc rectifier, a power factor correction (PFC) stage, and an isolated dc-dc converter stage [7]. General Motors (GM) has used a typical isolated OBC structure in the second-generation Chevrolet Volt [8]. Isolated dc-dc converters with relatively low efficiency affect the overall performance of OBCs, as even with 98-99% efficiency in the PFC stage, significant losses come from the transformer. Therefore, non-isolated OBC topologies can be considered instead to increase efficiency. Ford discusses the safety risks from the

leakage current for non-isolated OBCs in different grounding systems in [9] and GM explains the ground-fault current in non-isolated OBCs in [10]. Both Ford and GM suggest as a solution to add a ground fault circuit interruption (GFCI) circuit to the off-board charging circuit as the protection layer. The GFCI will be triggered if the ground-fault current exceeds the threshold, normally 4~6 mA [11].

Several non-isolated OBC topologies are compared in [11], including diode rectifiers with conventional buck-boost, SEPIC, and CUK converters, all with PFC. However, the semiconductor switches and diodes are under high voltage stress in these topologies since they tolerate the summation of the input voltage and the output voltage during operation. This leads to higher switching losses and the use of higher voltage rated devices, leading to higher conduction losses. Furthermore, the diode rectifier introduces significant conduction losses.

Thus, the totem-pole front end with PFC has been extensively researched for OBCs [12], [13]. Since the totem-pole circuit naturally provides a voltage boost, this chapter first suggests an OBC with a totem-pole front end for rectification and PFC cascaded with a synchronous buck converter for battery charging, as shown in Figure 5-1, as a traditional approach for comparison. The solar power from two large PV panels (i.e., vehicle hood and roof) goes through a high step-up boost converter to the DC bus in the OBC for battery charging. In high step-up converters, there is generally a trade-off between voltage gain and efficiency. With a PV voltage range of 40 – 50 V and a maximum battery voltage of 450 V, these converters must provide voltage gain of 9 to 11.

The main contribution of this chapter is the proposal of a novel SEV architecture where the solar energy is used to balance the capacitors in the flying capacitor front end, which improves upon the more conventional architecture from Figure 5-1. Section 5.2 presents the details of the proposed SEV integrated architecture, Section 5.3 presents its associated control, and Section 5.4 presents detailed simulation results. Section 5.5 performs a comparison of the two architectures and Section 5.6 summarizes the chapter.

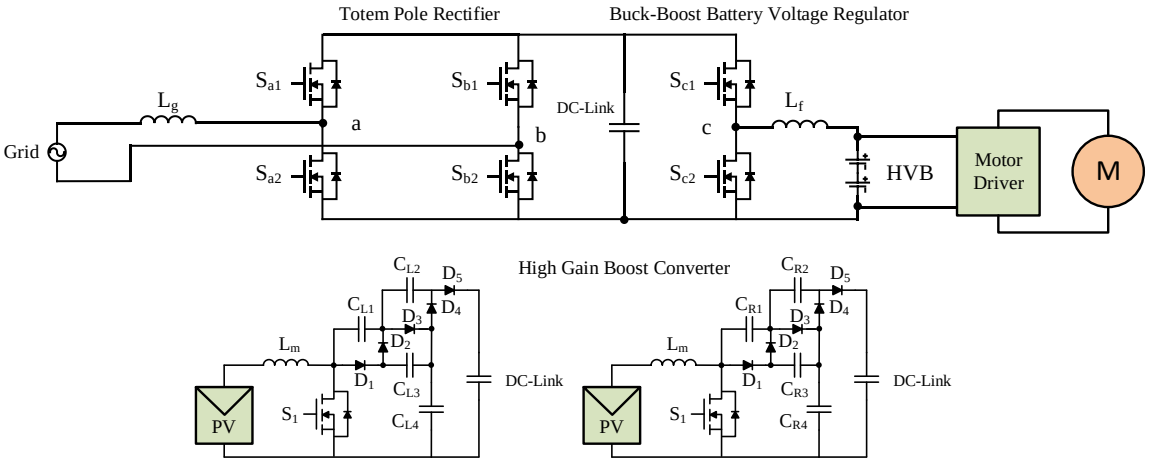

Figure 5-1: Traditional approach with three separate converters

5.2 Proposed SEV Electrical Architecture

The main contribution of this chapter is the proposed novel integrated flying capacitor SEV architecture shown in Figure 5-2. In this architecture, the flying capacitor topology is used for both battery charging and driving the motor to reduce component count, hence the name “integrated”. The main benefits of flying capacitor converters are lower switch voltage stress and improved total harmonics distortion (THD). Yet, balancing the flying capacitors is generally a challenge. However, in the proposed architecture, the solar energy from the PV panels is used to balance the capacitors when solar energy is available.

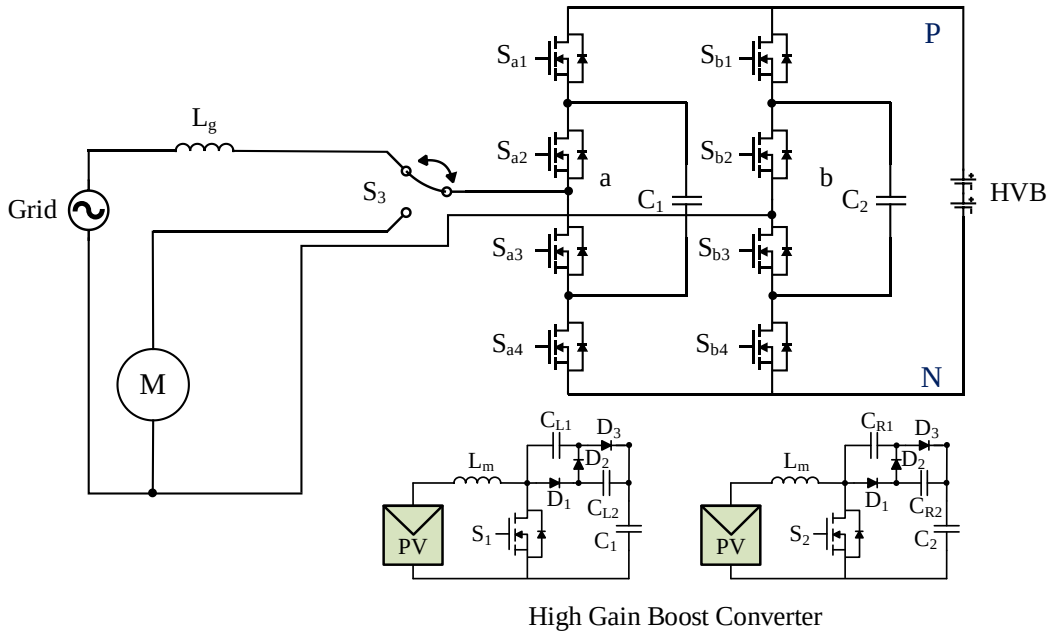

Figure 5-2: Proposed SEV architecture

The top and bottom circuits in Figure 5-2 are connected via the flying capacitors C_1 and C_2. Thus, this SEV architecture solves the capacitor balancing problem and the need for a high step-up solar converter, since the PV voltage no longer needs to be stepped up to the full battery voltage. In the proposed structure, the flying capacitor converter acts as an active rectifier when the high voltage battery (HVB) is being charged by the grid (*charging* mode). By using the reconfigurable switch S_3, the flying capacitor converter also acts as a 3-level inverter when the vehicle is driving, to drive the motor (*motoring* mode). A simpler step-up converter can be used to process the solar power, since the required voltage gain is now around 4.5 to 5.5. Figure 5-2 shows a single-phase motor to illustrate the basic idea, but often the motor is a 3-phase motor. The proposed converter can be extended to a 3-phase rectifier/inverter. In this case, the flying capacitor rectifier will have another leg which will add four switches and one flying capacitor to the circuit. The d-q method of

analysis will be also applicable for the 3-phase converter, and only the Table 5-1 will be updated according to the newly added leg. For the simplicity of analysis, a single phase rectifier/inverter is analyzed in the following subsections, which describe the three operating modes of the proposed architecture.

5.2.1 Mode A (Charging the Battery or Driving at night)

Mode A covers charging or driving when no solar power is available (e.g., overnight or parked inside). In charging mode, the grid will charge the HVB, but solar power is not available for balancing the flying capacitors. Thus, the energy required for charging and discharging the capacitors will only be supplied by the grid. The flying capacitor converter acts as an active rectifier which is being controlled by the d-q frame method. For the motoring mode, the HVB provides power through the converter to drive the motor. In both conditions, the harmonics introduced to the grid or motor will be controlled by the modulation scheme. Also, a balancing method is employed to keep the capacitors balanced.

5.2.2 Mode B (Charging the Battery or Driving the Motor with Solar and HVB)

Mode B covers charging or driving when solar power is available (e.g., most daytime hours). For this mode, the solar high boost converters have two roles. First, they help to balance the flying capacitors. Secondly, and most importantly, they provide solar power to the HVB to reduce the ac charging power required from the grid. By using this configuration, the voltage of the capacitors will be kept at the half of the DC link, reducing the gain requirement of the converters.

5.2.3 Mode C (Charging the Battery with only PV at Parking)

Mode C covers the common case of the vehicle being parked and charging the HVB with solar energy only. In this mode, the two capacitors will be in series with each other and will charge the HVB. The ac side of the flying capacitor converter is not connected to either motor or grid motor and grid. As shown in Figure 5-3, S_{a1}, $\underline{S}_{a2}$, S_{b2}, and $\underline{S}_{b1}$ are on providing the path for making the two capacitors in series to charge the HVB. In this mode, each capacitor should provide half of the DC link voltage, as compared to the full DC link voltage for the more conventional totem-pole topology in Figure 5-1.

5.3 Analysis and Control Scheme

At first, the active rectifier control and balancing method for both mode A and B is described. Then the equivalent circuit from the point ab is shown in Figure 5-4. Writing the equation for the circuit results in (1) – (4).

$$L\frac{di_{as}}{dt} = V_{as} - V_{ab} \tag{1}$$

$$C\frac{dV_c}{dt} = \frac{V_{ab}}{V_{dc}} i_{as} - \frac{V_{dc}}{R} \tag{2}$$

$$V_{ab} = V_d \,\mathrm{Cos}(\omega_0 t) + V_q \,\mathrm{Sin}(\omega_0 t) \tag{3}$$

$$i_{as} = I_d \,\mathrm{Cos}(\omega_0 t) + I_q \,\mathrm{Sin}(\omega_0 t) \tag{4}$$

Implementing (1) – (4) results a d-q system which can be shown in Figure 5-5. It should be mentioned that the system is single phase. Therefore, an imaginary phase with the 90-degree phase shift to reference voltage which is $V_{as} = V_m \mathrm{Cos}(w_0 t)$ is considered [15].

In this modulation there are two loops which control the dc link voltage and the power factor of input current for rectifying mode and motor input current in inverting mode. The reference for this current loop will be provided by the outer loop which regulates the output voltage. The result will produce the desired V_q and V_d for the $V_{ab.}$ The next step will be converting the d-q value of the V_{ab} to alpha-beta frame. The result will be used as the modulation scheme for the sinusoidal pulse width modulation (SPWM) system (5) which will produce the desired level for V_{ab}.

$$m = (n-1)(1+\frac{\sqrt{V_d^{\,2}+V_q^{\,2}}}{V_{dc}}\mathrm{Sin}(\omega_0 t - \tan^{-1}(\frac{V_q}{V_d}))) \tag{5}$$

In the next step, based on the desired voltage level (V_{ab}), the gate drive signals will be determined in a way that both capacitor voltages are balanced. To balance the capacitors, there are 4 switches in each leg, where lower switches have the complementary gate signals of the above switches. Therefore, there are 16 different switch state combinations. According to the direction of the current and current state of the capacitors charges a set of gates will be chosen (6) – (9). In this regard, a redundancy states table is developed (Table 5-1) [16]. Then, for balancing the capacitors a *Goodness* factor is defined. Among the possible switches a set with higher *Goodness* factor will be chosen. The higher the *Goodness* factor means that the greater number of capacitors are being balanced in the circuit. In the simulation, for the 3-level converter the maximum goodness is equal to number of capacitors which is two. Comparing to [16], in the proposed modulation in the equal circumstances for both capacitors (goodness capacitors=1) the set with more severe state will be chosen to be tackled with the undercharged or overcharged situations. Also, in

Mode B, when the PV power is available the Table 5-1 will be updated and reduced to 6 states which makes the control system much more simple comparing to [16]. The table of all possible sets of gate signals is shown in Table 5-1.

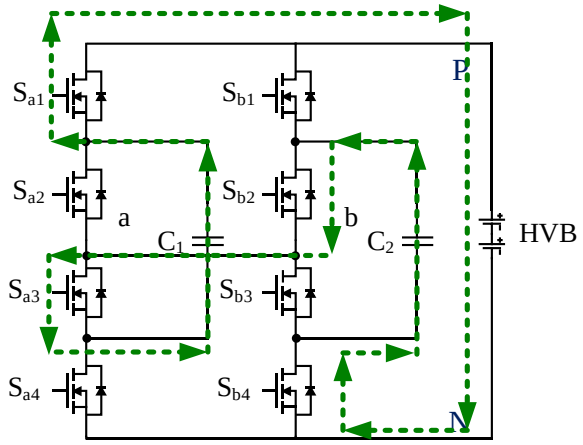

Figure 5-3: Mode C of the proposed converter (two capacitors are in series)

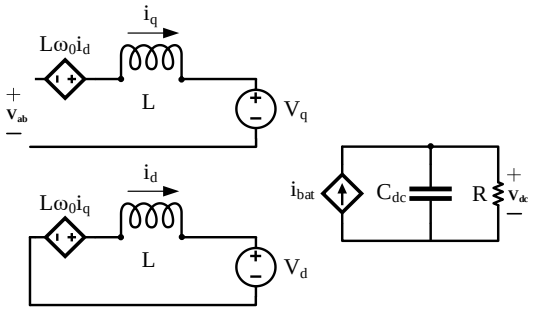

Figure 5-4: Equivalent circuit of the flying capacitor

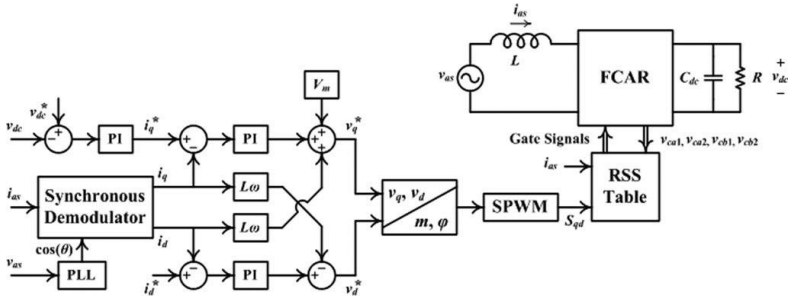

Figure 5-5: Control scheme [15]

$$V_{ab} = \begin{cases} 1\left(V_{C_1} < V_{C_1}^{*}\right) \\ -1\left(V_{C_1} > V_{C_1}^{*}\right) \end{cases} \tag{6}$$

$$I_{C_1} = (S_{a_1} - S_{a_2}) sign(i_{as}) \tag{7}$$

$$I_{C_2} = (S_{b_2} - S_{b_1}) sign(i_{as}) \tag{8}$$

$$Goodness_{Factor} = V_{C_1} I_{C_1} + V_{C_2} I_{C_2} \tag{9}$$

Table 5-1: RSS Offline Configuration

Levels	$[S_{a1}, S_{a2}, S_{b1}, S_{b2}]$					
2E	[1100]					
E	[0100]	[1000]	[1101]	[1110]		
0	[0000]	[0101]	[1001]	[1010]	[1111]	[0110]
-E	[0010]	[0111]	[1011]	[0001]		
-2E	[0011]					

5.4 Simulation Results

With regards to SEVs, a 20% efficient thin-film copper indium gallium selenide (CIGS) is assumed to be used for acquiring the solar energy. Solar data is extracted from [2] for Los Angeles with sunny and cloudy conditions. As an example, for a Chevrolet Bolt, considering the tilted surfaces have an approximately 18° angle, the effective horizontal area for installing the solar panels is about 3.3 m^2. By using the solar data from [2], in every hour the amount of solar power generated by the PV arrays is determined.

5.4.1 Mode A

All simulations are performed in MATLAB/Simulink and PLECS. For Mode A, the solar power is not available at night, and balancing of the capacitors is the challenge. Simulation results for Mode A in the charging mode are implemented for 2.2 kW and input voltage 150 V. Detailed information is given in Table 5-2. The simulation results for when

the grid is charging the HVB for the input current and output voltage are shown in Figure 5-6 and Figure 5-7, respectively. As can be seen in Figure 5-6 and Figure 5-7, the power factor (PF) and output voltage are adjusted with respect to their reference created in Figure 5-5(v_d, i_d), respectively. In order to observe the THD, a Fast Fourier Transform (FFT) analysis has been performed, and the result is shown in Figure 5-8. The THD 1.37% in charging mode.

The capacitor's voltages are balanced at half of the DC link. The SPWM levels generated between point a and b is produced in a way to assure unity power factor. The result is presented in Figure 5-10. To compare with the motor drive mode (when the vehicle is driving), the FFT analysis for the AC side is reported as 2.58%, which shows the THD in charging mode is 1% better than in motor drive mode.

Table 5-2: Simulation Parameters

Line Frequency	60Hz	V_g (peak)	210 V
Power	2.2 kW	C_1, C_2	2 mF
Switching Frequency	5 kHz	V_{Batt}	350 V
Grid Inductance	0.01 (units)	C_{out}	3 mF

5.4.2 Mode B

In this mode, the solar panels and the grid will charge the HVB or the HVB and the solar panels will feed the induction motors. In this section, the battery is 380V and is being charged by both the grid and solar panels, where the solar panels provide a moderate power level of 210 W each. The simulation results for when PV panels and the grid are charging the HVB are shown in Figure 5-11 and Figure 5-12 for input current and output voltage, respectively. Again, the PF and output voltage are adjusted in the desired range. To observe the THD, a FFT analysis has been performed, with the results shown in Figure 5-13, with

the THD being 0.36%. The THD has been improved by 1% compared to Mode A, and that is because having a tight regulation on capacitors with a PI controller for the dc-dc converters leads to smoother V_{ab} and consequently the THD and the PF improve. The results for capacitor voltages and V_{ab} are shown in Figure 5-14 and Figure 5-15.

The fundamental current value of grid current without PV power is 21.08 A and for the situation with PV the current is 17.23 A, which shows an 18.2% reduction in grid demand when the vehicle is being charged with PV as well as better THD. PF for all cases is around 0.99 which is acceptable for the requirements of the system.

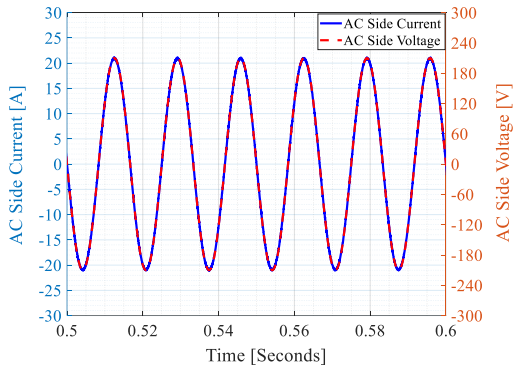

Figure 5-6: AC side current and voltage in charging state for mode A

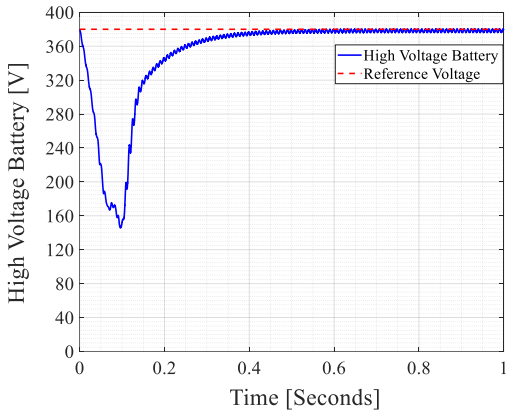

Figure 5-7: High voltage battery voltage for Mode A

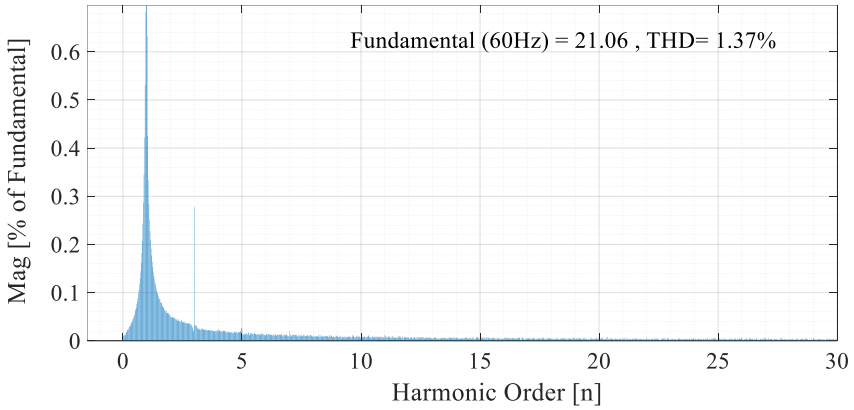

Figure 5-8: FFT analysis of input current for integrated topology in Mode A

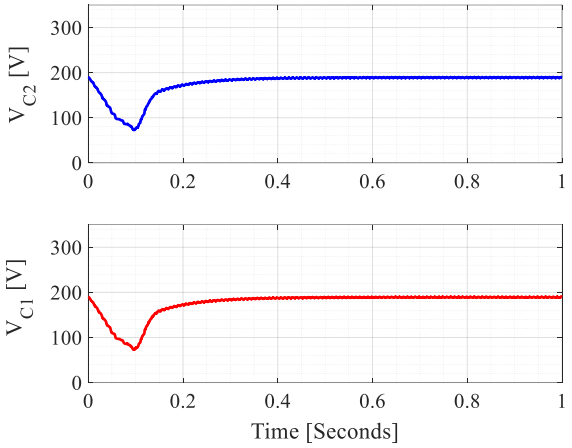

Figure 5-9: Flying capacitor voltages balanced in Mode A

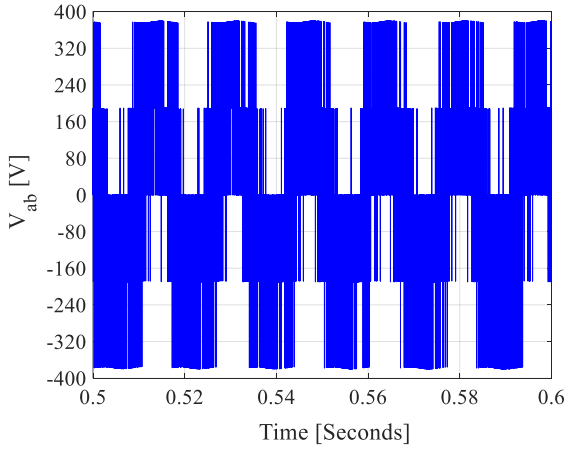

Figure 5-10: Vab in Mode A with only capacitor balancing method applied

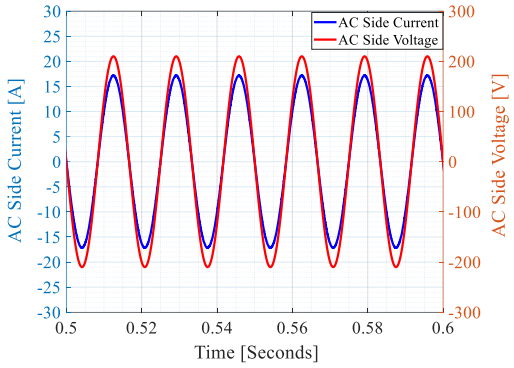

Figure 5-11: AC side current and voltage in charging state for mode

5.4.3 Mode C

In this mode both dc-dc converters will be in series with each other to charge the HVB. In this subsection, the third order boost converter is simulated. Based on [6], a simulation model is developed for this converter. A 200V GaN device is considered for the switch and Wolf speed SiC Schottky diodes have been selected. Table 5-3 shows the simulation model details.

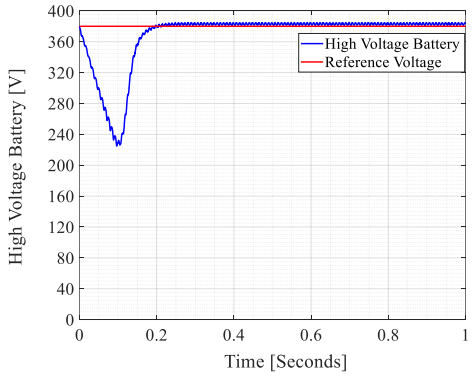

Figure 5-12: High Voltage Battery Voltage for mode B

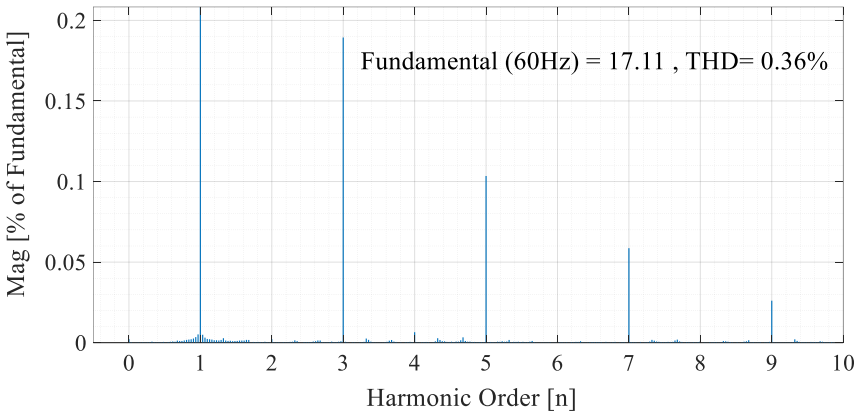

Figure 5-13: FFT analysis of input current for integrated topology in Mode B

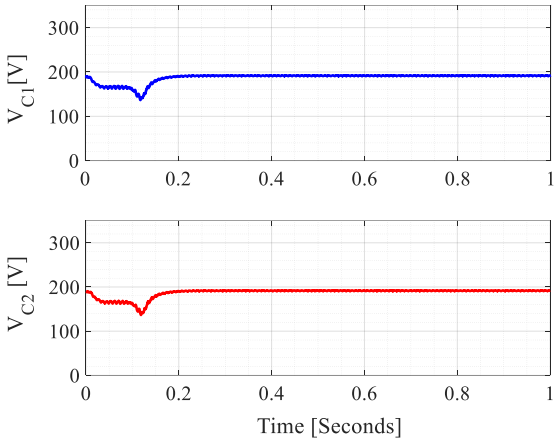

Figure 5-14: Flying Capacitor voltages Balanced in Mode B

Based on the results, with the change of voltage and power the efficiency of the converter remains more than 90% which is an acceptable result for a boost converter working at lower powers. For this simulation the voltage of the battery is considered to change from 240-380 V. Also, based on the PV curves and available solar power the power will change from 50-600W. The efficiency map result is presented in Figure 5-16.

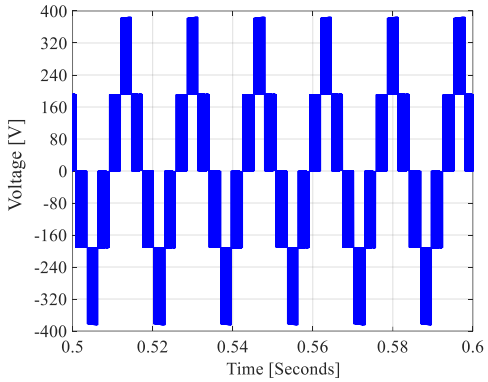

Figure 5-15: Vab in Mode B with capacitor balancing method and PI control of high step-up converter.

Table 5-3: Simulation Characteristics of the High Step-Up DC-DC converter

Switch	GS61008_v3
Diode	5*C3M0015065D
Inductance	300uH
$C_{1\text{-}4}$ / C_{out}	4*5uF(270V) 27uF(450V)

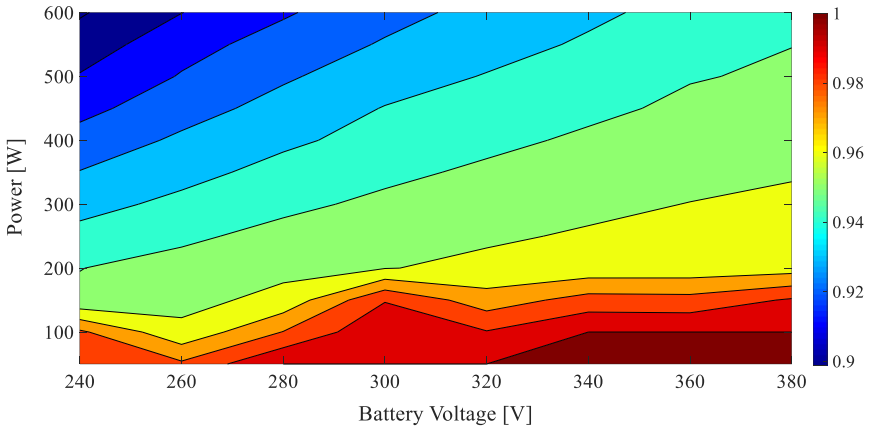

Figure 5-16: Simulated efficiency map of the high step-up converter

To have a more comprehensive view of the system, a simulation is done for a Chevrolet Bolt vehicle model altered to be a SEV, which is developed in MATLAB/Simulink. The system is simulated with and without PV for different months and different sky conditions. The simulated battery state of charge (SOC) result is presented in Figure 5-17 for a sunny day in June in LA. In these simulations the initial SOC of the battery is 95%. For different

solar radiation conditions and months, the battery ending SOC for each situation is presented in Table 5-4.

Table 5-4: Summary of the SEV Driving Simulation Results

Month	June		February	
Solar Conditions	Sunny	Cloudy	Sunny	Cloudy
Ending SOC (%)	53.14	51.78	47.10	45.53

5.5 Comparison

In order to compare the proposed integrated architecture with the more traditional approach in Figure 5-1, a simulation is performed for the Figure 5-1 circuit for the same rated voltage and current with two control loops of voltage and current [14]. The results for the input current and output voltage for this circuit are shown in Figure 5-18.

The simulated THD result is 4.13% which is almost three times higher than that of the proposed integrated system, as shown in Figure 5-19. The flying capacitor topology is a 3-level converter, and the totem pole converter from Figure 5-1 is a 2-level converter, so it is expected the 3-level converter would have a better THD in the proposed architecture.

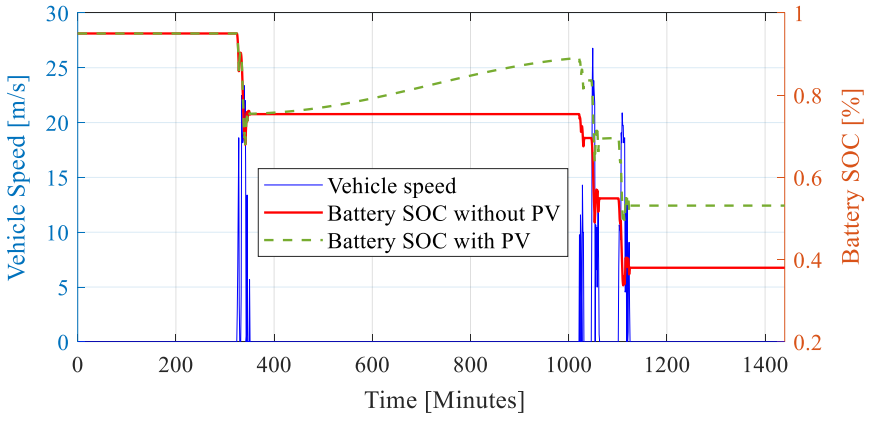

Figure 5-17: Vehicle battery SOC simulation results in June on a sunny day in LA

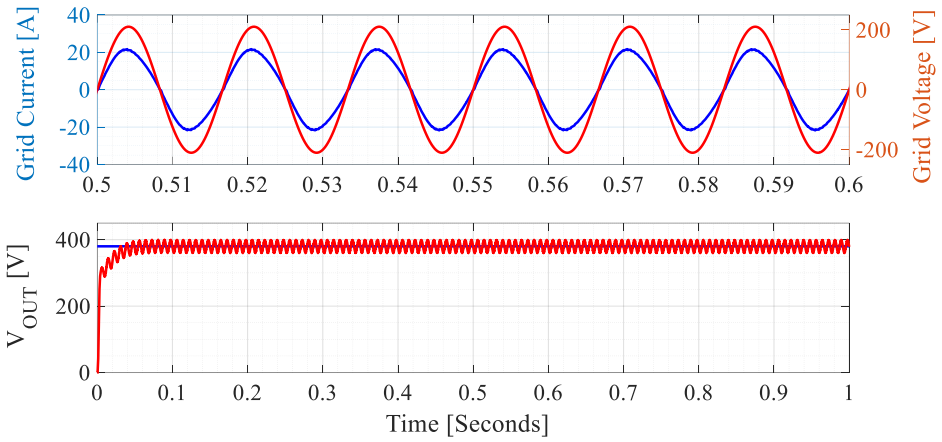

Figure 5-18: a) Input AC current and voltage b) output voltage

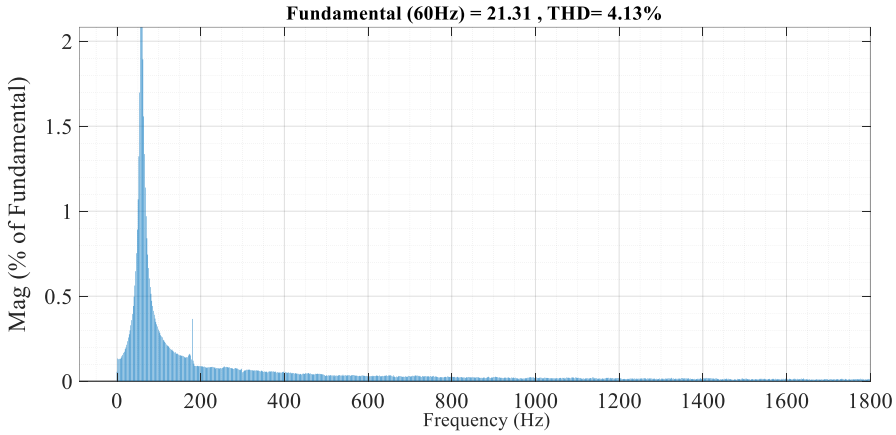

Figure 5-19: FFT analysis of input current for totem-pole circuit

Compared to the circuit in Figure 5-1, the proposed structure has a lower number of components, as summarized in Table 5-5, where N_{SW} is the number of switches, N_D is the number of diodes, N_C is the number of capacitors, and N_L is the number of inductors. The switch number for the Figure 5-1 circuit includes the 8 switches shown in Figure 5-1 and Figure 5-4 switches in a 2-level voltage source inverter used for the motor drive. This highlights an important advantage of the proposed architecture, in that the proposed converter can play the role of the charger or the motor drive, through the reconfigurable switch S_3. Since more simple boost converters can be used in the proposed architecture, the

number of diodes reduces by 4 and the number of capacitors reduces by 3. This is because a third order switched-capacitor dc-dc boost converter should be used to meet the high gain needs of the system in Figure 5-1, but a second-order boost converter provide enough gain in the proposed architecture.

Table 5-5: Comparison Between Topologies

	THD	V_{SW}	N_{SW}	N_D	N_C	N_L
Figure 5-1 circuit	4.13%	$V_{DC}/3$	12	10	9	3
Proposed	0.37% (with PV), 1.37% (without PV)	$V_{DC}/4$	10	6	6	2

A further benefit is that the voltage stress of the boost converter switch is reduced from 0.333 to 0.25 of the rated battery voltage. It should also be mentioned that with the proposed topology, the need for the dc-link capacitor is satisfied. This capacitor is large and adds significantly to the volume of the circuit in Figure 5-1. Overall, the proposed architecture achieves significantly better THD with a lower component count, compared to the more traditional approach of the Figure 5-1 circuit.

5.6 Summary

This chapter proposes a reconfigurable integrated flying capacitor architecture for a SEV. Different modes of operation based on the availability of sunlight and the vehicle operation are explained in detail. In addition, simulation results using MATLAB/Simulink are presented to justify the circuit theories presented. The proposed architecture achieves a significantly better THD while also reducing component count compared to a more traditional separate circuit approach, which means costs can be reduced.

5.7 References

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Chapter 6

Investigation of Power Electronic Architectures for Solar Electric Vehicles

Solar electric vehicles (SEVs) can play a role in the move towards sustainable transportation, as a portion of the vehicle's traction power is generated directly from on-board photovoltaic cells rather than relying on the generation mix of the local electricity supply for all charging. Other potential benefits include range extension, reducing charging load on the grid, and reduced charging costs. However, it is critical to design a high-efficiency electrical architecture to maximize the solar energy captured. This chapter investigates the efficiency and cost of two investigated electrical architectures for use in SEVs using four different converters. Detailed PLECS efficiency results are added to a vehicle model to investigate the efficiency during a real drive cycle with multiple solar radiation profiles. The results show that the best high step-up boost converter yields 9.9% higher efficiency than the best converter in the architecture utilizing the existing bidirectional converter results but has 2.8 times the cost.

6.1 Introduction

Electric vehicles (EVs) have the potential to significantly reduce harmful emissions from the transportation sector. However, to maximize the environmental benefits, the electricity used to power EVs should be generated in a sustainable way, such as from solar or wind. Due to the intermittent nature of most renewable energy generation, energy storage is often required, increasing the system cost. With the increasing efficiency of thin-film photovoltaic (PV) cells (23.35% [1]), it is becoming realistic to consider integrating the PV cells directly onto the EV, so that the built-in battery can act as the energy storage needed to deal with solar power intermittency. This concept of a solar EV (SEV) has additional

benefits such as increasing driving range and reducing charging needs from the grid, which can also reduce distribution transformer aging [2].

Some automotive companies are now starting to develop passenger vehicles with integrated PV cells: the Toyota Prius Prime and the Karma Revero both have solar cells integrated into the roof which charge the propulsion battery [3], [4]. Audi plans to integrate Gallium Arsenide (GaAs) solar cells, with efficiencies around 30% [5] on the roof of its 2020 EV line, and Sono Motors GmbH is currently developing the Sion EV, which has monocrystalline silicon PV modules fixed onto all vehicle body panels [6]. Recent research also shows increasing interest in PV on vehicles: [7] proposes EV battery balancing powered by vehicle-rooftop solar panels, [8] proposes reconfigurable PV arrays for on-vehicle use to deal with partial shading, and [9] analyses the benefits of adding monocrystalline silicon PV cells to internal combustion engine vehicles.

Reference [10] proposes an electrical architecture using a switch matrix to charge small groups of battery cells from onboard PV panels yet requires extensive switch connections between the PV output and the internal cells of the battery pack, meaning the design is not modular. On-board solar has also been investigated for other modes of transportation: [11] presents the design of a solar-assisted electric rickshaw and [12] presents a silicon carbide-based converter with differential power processing for a solar powered aircraft. In [12], the PV voltage is very high (352 V) due to the large PV area available on the aircraft, and thus the voltage boost challenges are much different than in a passenger vehicle with lower PV voltages due to a smaller vehicle surface area.

This chapter simulates and compares four power electronic architecture options for SEVs to investigate the efficiency and cost of each option. It is assumed that the solar energy should be delivered to the high-voltage battery pack terminals for a modular design that does not require redesign of the battery pack for adding complex interconnections between the solar output and the individual battery cells. Section 6.2 describes the requirements and challenges of designing SEV electrical architectures and presents two architectures, each with two circuit options. Section 6.3 presents simulation results which compare the efficiency of each architecture within a vehicle model and discusses the cost implications of each architecture. Section 6.4 summarizes the chapter.

6.2 SEV Electrical Architectures

6.2.1 SEV Architecture Options

This analysis is based on a large-scale SEV concept with 20% efficient thin-film copper indium gallium selenide (CIGS) integrated onto the roof, hood, and trunk of an electric vehicle. The Chevrolet Bolt is used as a reference model. The Bolt has approximately 2.3 m^2 of near-horizontal surface area including the combined roof and trunk, and approximately 1.05m^2 of surface area tilted by about 18°. To approximate the horizontal equivalent area of the tilted area, cosine is applied to 18°. Thus, the estimated total equivalent horizontal area is 3.3 m^2. To generalize the results, it is assumed that this area is divided into three 1.1 m^2 solar panels, with a maximum power point tracking (MPPT) converter connected to each 1.1 m^2 panel. For peak solar radiation of 1000 W/m^2, about 220 W can be generated on each surface for a total of 660 W in ideal non-shaded conditions.

Though the peak solar generated power of 660 W is low compared to traction power needs, the value of SEVs is to obtain solar power over long periods of the day, while driving and parked, to amount to significant solar energy storage.

This study considers the average daily solar radiation in July and in January in Los Angeles, California. Figure 6-1 shows the daily solar radiation for both months for both full sun and average cloud conditions [13]. One crucial aspect of the electrical design is to maximize conversion efficiency at both low and high loads, due to the changing solar radiation over a day. Furthermore, the power electronic design is interrelated with the PV cell connection scheme, which complicates the task of determining the overall optimal architecture. The size of PV cells, number of PV cells in series, and number of PV cells in parallel will affect the power electronic design by influencing the input voltage and current.

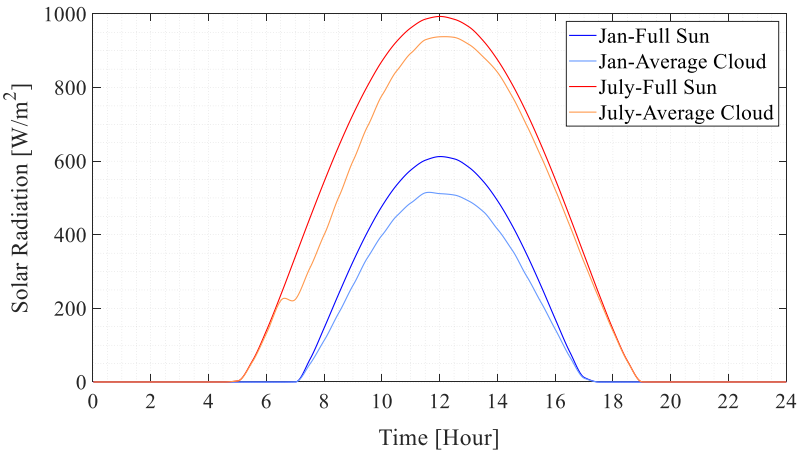


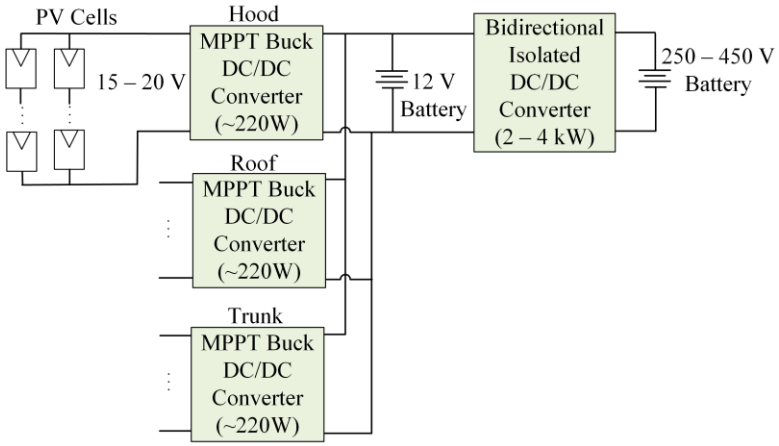
Figure 6-1: Average solar radiation power profiles in Los Angeles [13]

This research presents and analyses two potential power electronic architectures for transferring solar power to the traction battery of an EV (250 V to 450 V), as shown in Figure 6-2. Option 1 utilizes the bidirectional isolated 12 V DC-DC converter already present in EVs to perform the main voltage boost from the 12 V bus to the traction battery.

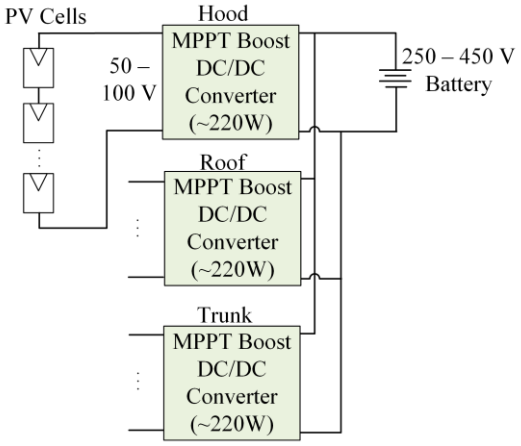
Also, low cost and high efficiency MPPT buck converters are used to transfer the solar power to the 12 V battery bus, where it is later transferred through the bidirectional converter to the traction battery. The advantages of Option 1 are: (i) PV cell arrangement with less cells in series makes it more immune to partial shading, (ii) low cost since only low-voltage MPPT buck converters are added and the bidirectional converter already present in the vehicle is utilized, and (iii) solar energy can first be used to power low-voltage accessories while driving and charge the 12 V battery, and only be transferred to the traction battery when the 12 V battery is fully charged. The disadvantages of Option 1 are: (i) there will be higher circulating currents for a given solar power level due to the lower PV voltage, (ii) the solar power must pass through two power electronic converters to get to the traction battery, lowering the efficiency of this path, and (iii) the bidirectional charger is rated for higher power (2 to 4 kW) and thus will have lower efficiency at the lower solar power levels.

Option 2 uses more cells connected in series to achieve higher solar voltage, then boosts the voltage directly to the traction battery voltage using dedicated MPPT boost converters. The main advantage of Option 2 is that higher conversion efficiency can likely be obtained because: (i) solar power is processed by only one converter, (ii) a high-efficiency non-isolated boost converter is used, and (iii) due to higher PV voltages, there will be lower PV currents. The potential disadvantages of Option 2 are: (i) since more PV cells are required in series to create a higher PV voltage, there could be more negative effects from partial shading, and (ii) since a voltage boost of up to 9 times is required, and higher voltage rated

devices are required, the MPPT boost converters will be higher cost than the MPPT buck converters in Option 1.



(a) Option 1



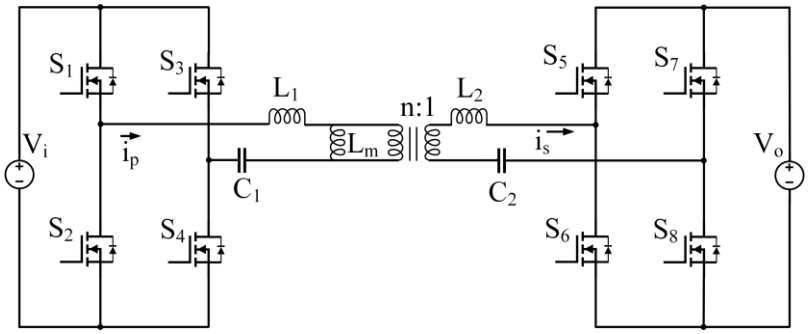
(b) Option 2

Figure 6-2: Two investigated SEV architecture options

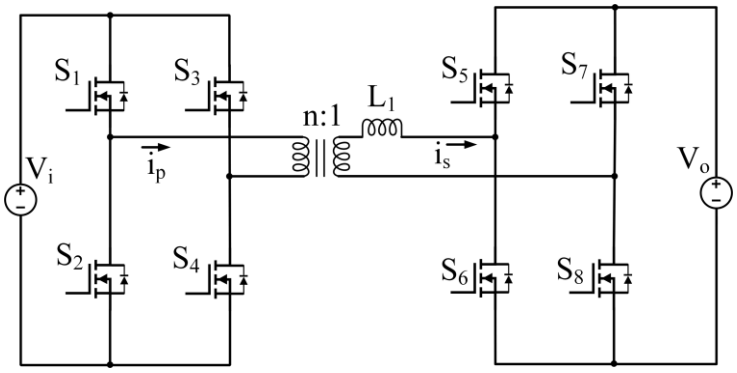
6.2.2 SEV Power Electronic Converter Options

For Option 1, it is recommended to use a simple non-isolated buck converter to process the solar power to the 12 V bus. Low voltage rated devices can be used to reduce cost. With regards to the bidirectional isolated DC-DC converter, the CLLC converter and the dual

active bridge (DAB) converter are considered. These bidirectional converters can achieve high power density, high efficiency, wide gain range, and galvanic isolation [14]. Both architectures have zero voltage switching (ZVS) which can lead to higher efficiency [14], [15]. Reference [15] proposed a 500 W CLLC converter with ZVS and ZCS features to minimize the switching losses, as shown in Figure 6-3(a). The highest efficiency of the experimental results is 96%. Reference [16] uses a DAB for converting the 12 V battery voltage to the traction battery voltage. Reference [17] analyzes and investigates the performance of the DAB. Intrinsic ZVS features with a reduced number of passive components are the advantages of using this converter. Figure 6-3 (b) illustrates the typical DAB converter, which will be considered in this study.



(a)



(b)

Figure 6-3: Isolated bidirectional converter options for SEV architecture Option 1 (a) CLLC converter [15] (b) Dual Active Bridge converter

For Option 2, a high efficiency, high step-up non-isolated boost converter is required. Over the last decade, many potential converters meeting these requirements have been proposed [18-21]. For the SEV application, the converters proposed in [18] and [19] are considered, as shown in Figure 6-4. The circuit in Figure 6-4(a) [18] uses the switched capacitor method to achieve high voltage gain, which can reduce voltage stress on the switches and diodes by 66% in comparison to the conventional boost converter. It is capable of achieving 95% efficiency for a voltage gain ratio of 8. The converter proposed in [19], as shown in Figure 6-4(b), is a SEPIC-based boost converter with adapting fly back/forward coupled inductors for achieving a high gain voltage ratio. However, due to high current stress of the inductors, the efficiency decreases at higher power. This converter has reported the efficiency of 97.5% in a 100W converter with the voltage gain ratio of 14.

6.3 Simulation Results

6.3.1 Simulation Framework

Detailed models of each converter are designed and then simulated in PLECS. The DAB and CLLC isolated bidirectional converters in Option 1 are designed for 3 kW peak power, as they are intended to represent the auxiliary power converter used in a typical EV. The high step-up converters for Option 2 are designed for 250 W each, as they only process solar power from one array each. The PLECS models are run at numerous operating points so that converter efficiency can be extracted overall operating points of interest to create look-up tables for use in a system-level vehicle model.

In this study, it is assumed that each surface (hood, roof, trunk) has a solar array consisting of four strings. Table 6-1 shows the parameters used to model each string in MATLAB/ Simulink.

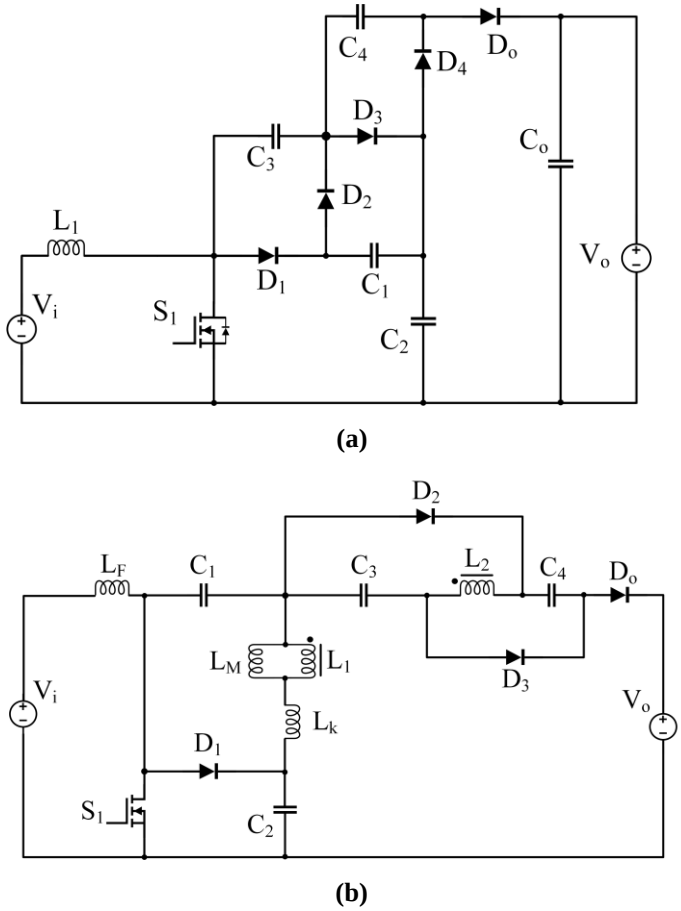


Figure 6-4: High step-up converters for SEV architecture Option 2 (a) Boost converter proposed in [18] (b) Boost converter proposed in [19]

For the Option 1 architecture, the four strings are connected in parallel to create a lower voltage to be stepped down to the 12 V bus. For the Option 2 architecture, the four strings are connected in series to create a higher voltage to minimize the step-up required by the boost converter. Figure 6-5 shows the simulated I-V and P-V characteristics of each array. These results show that for Option 1, the maximum power point (MPP) is around 15 V and

thus 15 V is used as the input voltage to the buck MPPT converters. The buck converters step the voltage down to 12 V, and then the DAB or CLLC converters boost to the traction battery voltage (250 V to 450 V). For Option 2, the MPP is around 60 V, and thus 60 V is used as the input voltage to the boost MPPT converters. The converters from [18] and [19] boost this 60 V directly to the traction battery voltage. Based on these respective input voltages, each converter is designed, and the converter parameters are shown in Table 6-2. For the DAB and CLLC converters, the primary low voltage sides use GaN switches with low $R_{ds\text{-}on}$ values to reduce conduction losses. The CLLC converter uses 3 of these switches in parallel on the low side to reduce conduction losses from circulating current. On the secondary sides, silicon carbide (SiC) MOSFETs are employed. GaN switches and SiC diodes are used in the boost converters from [18] and [19] as well. PLECS simulation results considering switching, conduction, and magnetic losses are used to make efficiency look-up tables, as shown in Figure 6-6 to Figure 6-9. For reference, the operating points for a cloudy day in January are marked on top of the efficiency maps. A buck converter is also simulated in PLEC for use with Option 1, to step down the solar voltage to 12 V.

Table 6-1: Modeled Solar String Parameters

Parameter	Value
Maximum power (W)	51.45
Open circuit voltage, V_{oc} (V)	18
Voltage at maximum power point, V_{mpp} (V)	15
Temperature coefficient of V_{oc} (%/°C)	-0.361
Short-circuit current, I_{sc} (A)	3.6
Current at maximum power point, I_{mpp} (A)	3.43
Temperature coefficient of I_{sc} (%/°C)	0.102

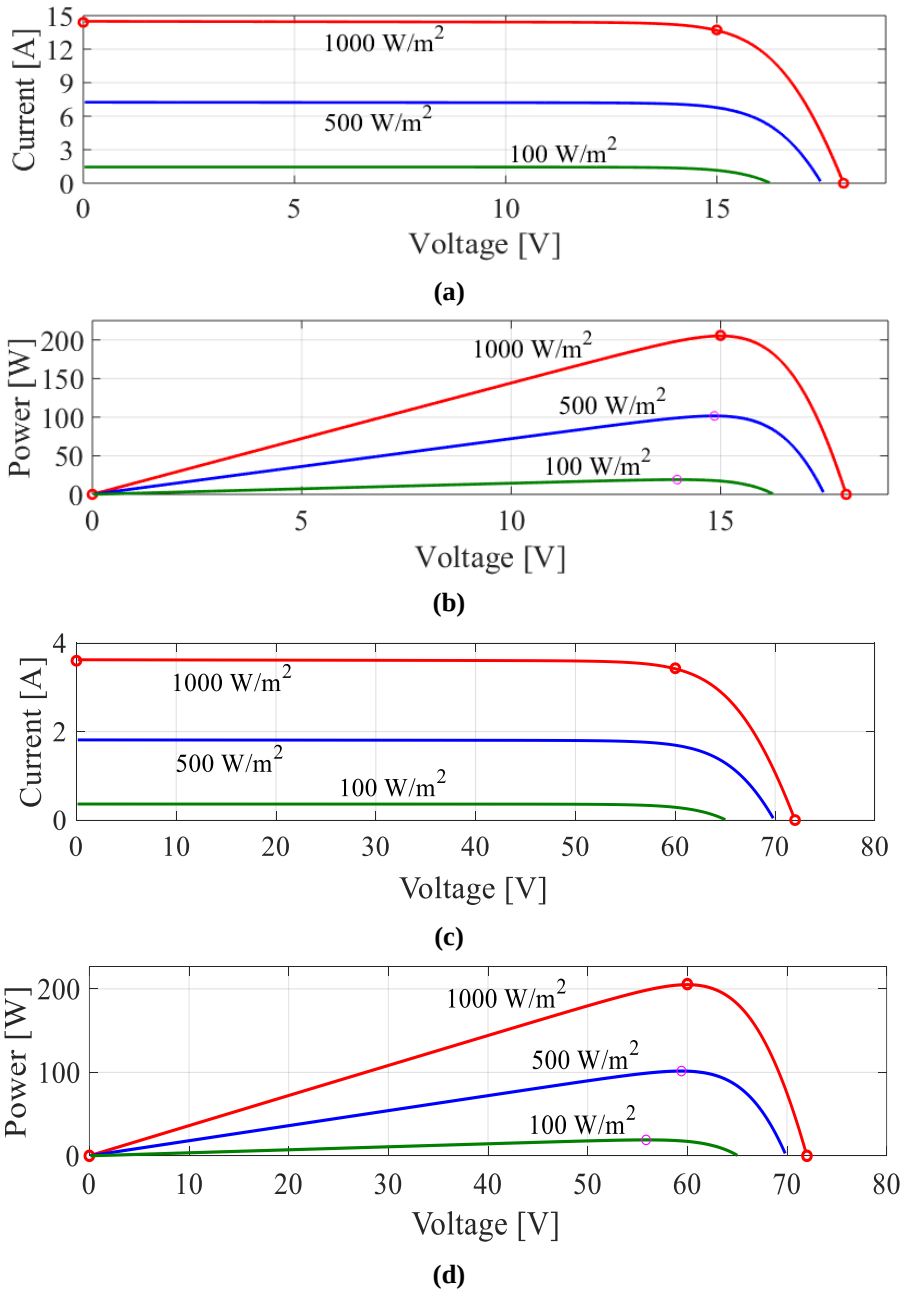


Figure 6-5: I-V and P-V characteristics of simulated solar arrays to generate input voltage for both options (a) The I-V curve for four solar strings in series (b) The P-V curve for four solar strings in series options (c) The I-V curve for four solar strings in parallel (d) The P-V curve for four solar strings in parallel

Table 6-2: Converter Design Details

Component	DAB	CLLC	Boost Converter [18]	Boost Converter [19]
Switches	4×GS61008, 4×C3M00-65090D	12×GS61008, 4×C3M00-65090D	GS61008	GS61008
Diodes	-	-	5× C3M00-15065D	4× C3M00-15065D
Transformer, Coupled Inductor	Payton T250 AC P.N. 501044	Payton T250-4-16	-	Payton T80 AC P.N. 500510
Inductors	-	100uH	300uH	300uH
Capacitors	10uF/450V	33nF/180V, 33uF/180V	4×5uF/270V, 27uF/450V	47uF/47V, 2×10uF/90V, 6.6uF/90V, 100uF/380V
Switching Frequency	80 kHz	80 kHz	40 kHz	40 kHz

The efficiency map for this buck converter is shown in Figure 6-10. A system-level EV model is created in MATLAB/Simulink as described in [22], based on the Chevrolet Bolt. This model is modified to have the solar energy source and the efficiency look-up tables for each converter. For Option 1, the buck converter efficiency map is used with the DAB or CLLC converter map.

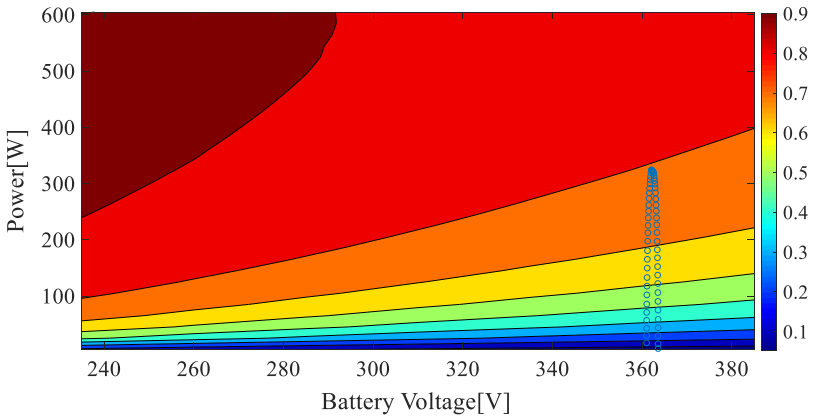


Figure 6-6: Simulated efficiency map for DAB

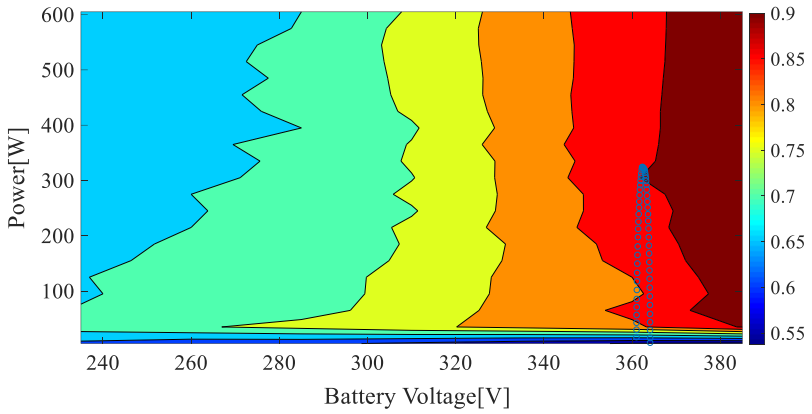


Figure 6-7: Simulated efficiency map for CLLC

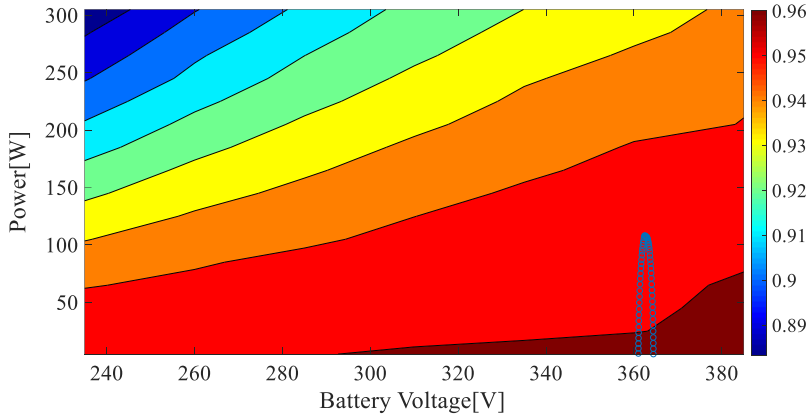


Figure 6-8: Simulated efficiency map for boost converter from [18]

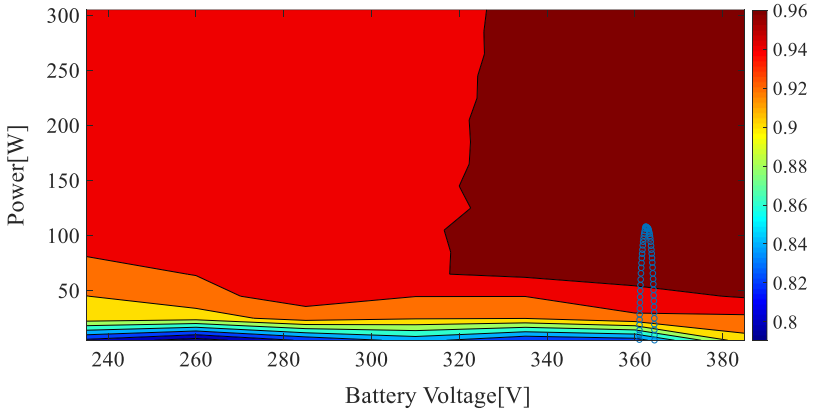


Figure 6-9: Simulated efficiency map for boost converter from [19]

6.3.2 Efficiency Results

One full day of real-world logged driving data is used as the test case in this study. Figure 6-11 shows the vehicle speed over 24 hours of the day, as well as the battery state-of-charge (SOC) over the day for a non-solar EV, for comparison purposes. The initial battery SOC is set to 95%. All SEV architecture options are simulated for both a sunny and average cloud day in July and January to investigate the efficiency of each converter at the highest and lowest projected solar power levels. The vehicle battery SOC for each tested case is shown in Figure 6-12 to Figure 6-15, and the detailed converter efficiency results are shown in Table 6-3.

The results show that Option 2 with the high step-up boost converters exhibits much higher average daily efficiency than Option 1 (buck converter and isolated bidirectional converter). Within Option 2, the converter from [19] gives slightly higher efficiency than that from [18]. Within Option 1, the CLLC converter is more efficient than the DAB converter for the case studied. However, if a lower traction battery voltage is used, the CLLC efficiency will decrease, possibly below that of the DAB, as shown in Figure 6-7. The relatively low efficiency of the DAB and CLLC converters is partly due to the fact that the converters are designed for the required 3 kW auxiliary power load, and the low solar powers often mean the converters are operating at low efficiency points. Also, it is encouraging that the rank of ordering converters by efficiency is the same in January and July, meaning a good choice of converter in one part of the year will also be a good choice in the opposite part of the year.

For the non-solar EV, the ending SOC is 62.4%, meaning the vehicle consumed 19.56 kWh over the day (battery capacity is 60 kWh). For the average cloud case in July with the highest efficiency converter (from [19]), the ending SOC is 69.9%, meaning 15.06 kWh was used over the day, or 23% less energy than the non-solar EV. For the same conditions, the lowest efficiency converter (buck + DAB), gave an ending SOC of 68.5%, and used only 18.7% less energy than the non-solar EV.

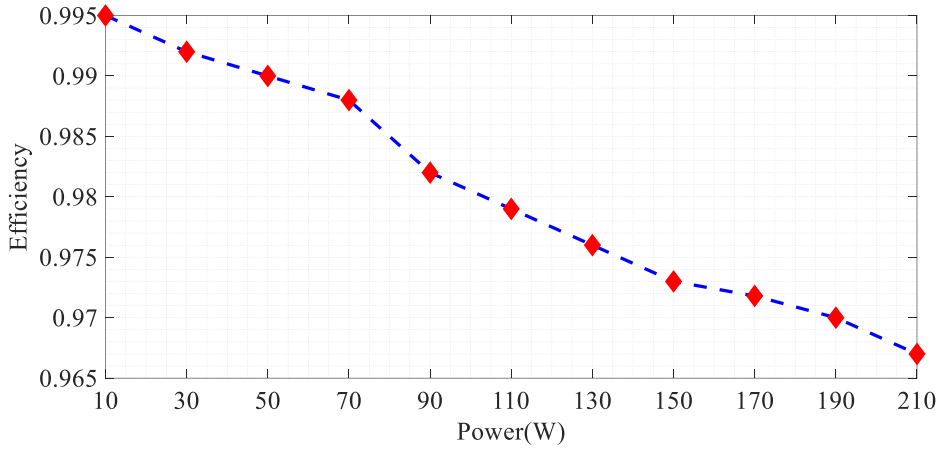


Figure 6-10: Simulated efficiency map for buck converter (V_{in}=15V, V_{out}=12V)

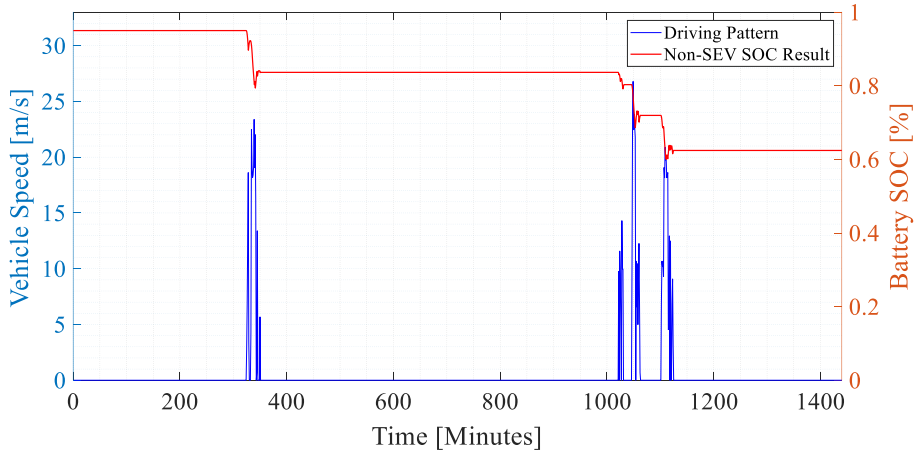


Figure 6-11: Driving profile and simulated SOC for non-solar EV

These results show that it is critical to design a high efficiency solar architecture, or the full advantages of on-board solar will not be realized. These results also show that less grid charging will be required for the solar EV and thus it is possible that battery life may be extended due to less daily depletions of battery energy (since depth of discharge is related to battery life).

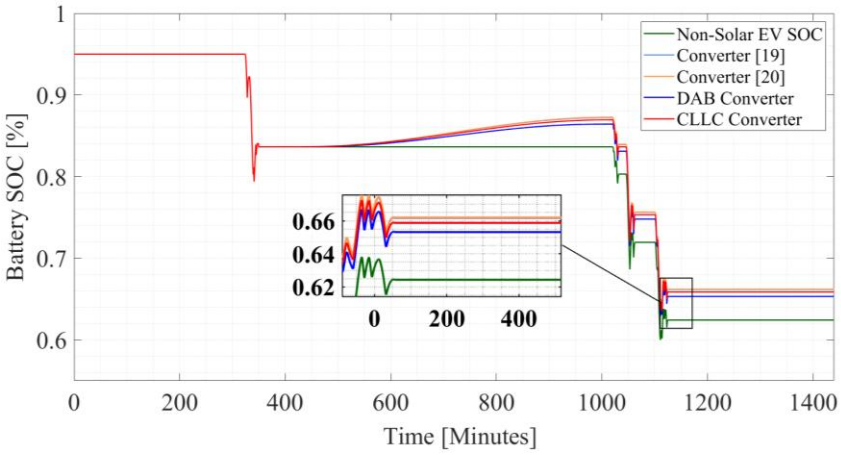


Figure 6-12: Simulated SOC for each converter in January (full sun)

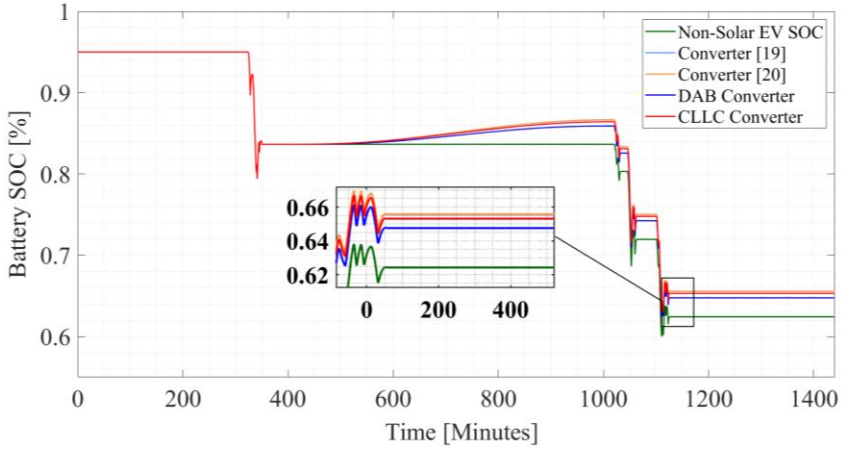


Figure 6-13: Simulated SOC for each converter in January (average cloud)

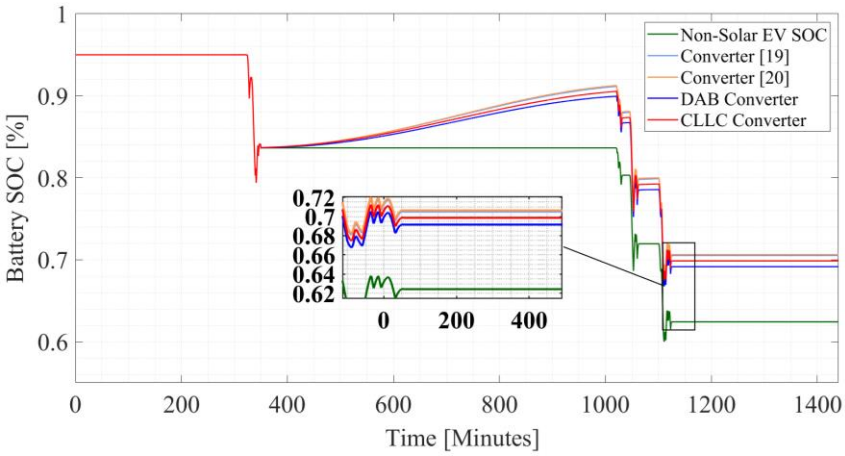


Figure 6-14: Simulated SOC for each converter in July (full sun)

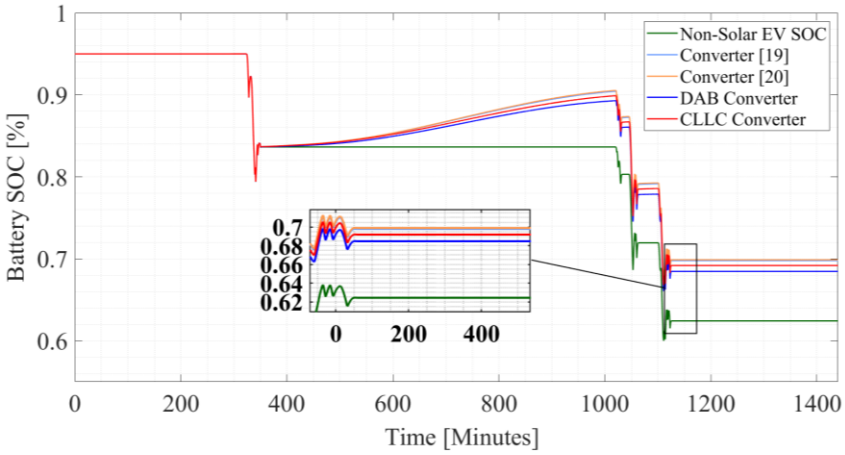


Figure 6-15: Simulated SOC for each converter in July (average cloud)

6.4 Cost Analysis

Though Option 2 yielded the highest average efficiencies, Option 1 is attractive due to being able to re-use the isolated bidirectional converter already utilized in EVs. Thus, the extra cost for Option 2 is only related to the buck converters. Since precise costs can vary based on the quantity purchased, this cost analysis calculates active device ratings (*ADR*) (relative to power throughput) and passive device ratings (*PDR*) as metrics for comparing costs. The equations used here for *ADR* and *PDR* are shown in (1) and (2) respectively.

Table 6-3: Summary of Simulated Efficiencies

		Daily Energy from Solar Panels (E_{in}) (KWh)	Converter	Daily Energy into HV Battery (E_{out}) (KWh)	Battery Ending SOC (%)	Average Converter Efficiency (E_{out}/E_{in}) (%)
Jan.	Full Sun	2.3670	[18]	2.2649	66.2	95.69
			[19]	2.2888	66.2	96.70
			Buck+DAB	1.7515	65.3	74.00
			Buck+CLLC	2.0881	65.9	88.22
	Average Cloud	1.9767	[18]	1.8936	65.5	95.80
			[19]	1.9085	65.6	96.55
			Buck+DAB	1.4101	64.8	71.34
			Buck+CLLC	1.7459	65.3	88.30
July	Full Sun	5.1666	[18]	4.9225	70.5	95.27
			[19]	5.0014	70.6	96.80
			Buck+DAB	4.0910	69.2	79.18
			Buck+CLLC	4.5237	69.8	87.56
	Average Cloud	4.688	[18]	4.4718	69.8	95.37
			[19]	4.5374	69.9	96.77
			Buck+DAB	3.6847	68.5	78.28
			Buck+CLLC	4.1085	69.2	87.63

$$ADR = \frac{1}{P_{out}}\left(\sum_{i=1}^{N_S} V_{switch\_i} I_{switch\_i} + \sum_{j=1}^{N_D} V_{diode\_j} I_{diode\_j}\right) \quad (1)$$

$$PDR = \left(\sum_{i=1}^{N_L} L_i I_i^2 + \sum_{j=1}^{N_C} C_j V_j^2\right) \quad (2)$$

In (1) and (2), N_s and N_D are the numbers of switches and diodes in each converter and N_L and N_C are the numbers of inductors and capacitors. Also, I_i and V_j are the RMS current of inductors and voltage rating of capacitors, respectively. The active and passive device ratings can be combined into one device rating metric, *DR*, using weighting factors α_1 and α_2, which can be chosen to weight the priority of *ADR* and *PDR* in the design of the system, as shown in (3). In this case, $\alpha_1 = 1, \alpha_2 = 4$ are used to make the *ADR* and *PDR* in the same range.

$$DR = \alpha_1 ADR + \alpha_2 PDR \quad (3)$$

Table 6-4 summarizes the device ratings and average efficiency for average cloud conditions in the two months analyzed. Though the only extra power electronic cost for Option 2 is for the three buck converters, the device ratings for Option 2 including the DAB and CLLC are also shown in Table 6-4 for completeness. However, the *DR* for the DAB and CLLC cannot be directly compared to the those of the buck and boost converters for a cost comparison due to the different power ratings (see (1)). However, the power ratings of the buck and boost converters are the same, so can be compared as a direct metric for cost. Figure 6-16 plots the average efficiency against *DR* for the four main cases, excluding the device ratings for the DAB and CLLC, as these would be existing on the vehicle anyways. For Option 2, the converter from [19] is 1.1% more efficient than the converter from [18] for the test cases chosen but has a 3.2% higher cost. Comparing the highest efficiency converter in Option 2 (converter from [19]) to the highest efficiency converter in Option 1 (CLLC) shows that the boost converter from [19] is 9.9% more efficient than the CLLC, but costs nearly 2.8 times more. However, when considering the system-level design, it should be pointed out that the additional cost of the on-board solar cells will likely be best utilized by choosing the highest efficiency architecture (Option 2), even at a higher cost.

6.5 Summary

This research investigates two SEV power electronic architectures and considers four known power converters within the two options. PLECS simulations are carried out to analyze efficiency and device ratings for the SEV use case.

Table 6-4: Summary of Device Ratios

	ADR	PDR	DR	Average Efficiency (%)
3×Converter from [18]	10.98	0.333	12.31	95.58
3×Converter from [19]	11.22	0.3725	12.71	96.66
Device Ratings: 3×Buck Efficiency: Buck+DAB	3.48	0.268	4.55	74.81
Device Ratings: 3×Buck+DAB Efficiency: Buck+DAB	8.03	1.685	14.77	
Device Ratings: 3×Buck Efficiency: Buck+CLLC	3.48	0.268	4.55	87.97
Device Ratings: 3×Buck+CLLC Efficiency: Buck+CLLC	7.18	2.145	15.76	

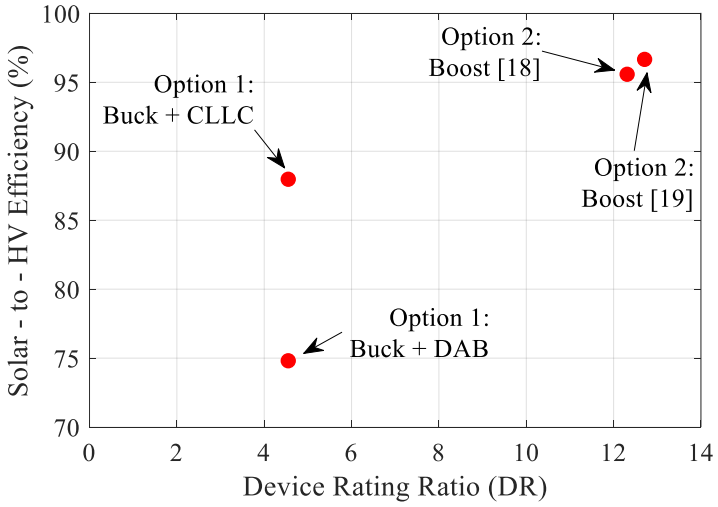


Figure 6-16: Efficiency and device ratings of the four topologies

A system-level vehicle model is used with the converter efficiency maps to investigate the impact on battery SOC of using the four different converters. The results show that the high step-up boost converter architecture (Option 2) is much more efficient than using buck converters with the 12 V bus and re-using the isolated bidirectional DC-DC converter already in the vehicle (Option 1). However, Option 1 has significantly lower device ratings, implying a lower cost. Although the decision of efficiency versus cost will be unique for each design scenario, it is recommended that a high priority be placed on efficiency since

the cost of adding the on-board solar arrays is best utilized when less solar power is lost in the power electronic converters transferring this power to the traction battery.

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Chapter 7

Integrated Three-Port Converter for PEV Applications

Adding on-board solar generation to electric vehicles (EVs) is one way to help reduce their charging needs and/or increase their driving range. To maximize the potential benefit, differential power processing (DPP) converters can be implemented to maximize solar energy capture in partial shading conditions. Furthermore, an isolated high-step up converter is required to transfer solar energy to the high-voltage battery, and a buck converter is useful to create an efficient direct path from the solar cells to the low-voltage accessory bus. If implementing these power electronic requirements with separate converters, the component count is high and power density can suffer. Thus, this chapter proposes the first multiport converter with solar DPP, an isolated high-voltage output port, and a low-voltage port, which is uniquely suited for solar-charged EVs. The switch count is low, and a simple control strategy is proposed to allow separate control of the two output ports. A 200 W experimental prototype is built and tested and shows a peak efficiency of 96.7% when solar power is flowing to both the high-voltage and low-voltage ports.

7.1 Introduction

Electric vehicles (EVs) are a promising solution to reduce fossil fuel use and emissions. However, some obstacles to EV uptake include limited driving range, high battery costs, and long charging times. Furthermore, the effect of increased charging loads on the generation, transmission, and distribution systems must be considered. Adding on-board solar generation to an EV is one way to help deal with these issues. Recent advancements have pushed the peak lab-measured efficiency of thin-film photovoltaic (PV) cells to 23.35% [1]. By modeling the effect of adding PV cells to all upwards-facing vehicle surfaces, [2] showed that on average, such a large-scale solar electric vehicle (SEV) could

reduce annual net vehicle energy consumption by 21.5% in Los Angeles and 17.5% in Detroit.

The development of an optimal large-scale SEV requires a power electronic architecture that can transfer solar power to both the high-voltage battery (HVB) and low-voltage bus (LVB) to power accessory loads with very high efficiency [3]. In general, when the vehicle is parked, all generated solar energy will be sent to the HVB for storage. While driving, it is most efficient to send the required solar power directly to the LVB (to avoid additional losses through the auxiliary power module) and send any excess power to the HVB. Additionally, the power electronic topology must provide maximum power point tracking (MPPT) to maximize solar power generated during partial shading conditions and should have a low component count to reduce size and cost. Further design constraints may include keeping the PV voltage < 60 V and providing electrical isolation between the PV panels and the HVB, both for safety reasons.

Another design consideration is how to deal with partial shading over the solar vehicle surfaces. The simplest solution is to use bypass diodes across a number of solar modules, but power is lost from all modules in series connected across the diode, even if only some of those modules are shaded. To reduce power loss, distributed MPPT systems [4] can be used instead, where each module is connected to a micro-converter; however, the cost and complexity of this solution is high [5].

An alternative that has been well-researched is differential power processing (DPP) converters [5]– [11]. These converters are placed in parallel with PV modules in a string and only process the differential power between two ports. Thus, a portion of generated

solar power from the unshaded modules is transferred to the shaded ones, so all modules can operate at the same voltage [12]. Accordingly, the number of components and power losses are reduced [12]. DPP converters can be categorized into several groups based on power redistribution scenarios: 1) buck-boost converters, 2) multistage choppers, 3) switched-capacitor (SC) converters, and 4) multi-winding flyback converters [12]. Among these, SC-based DPP converters are gaining significant attention as a prominent solution to minimize the effects of partial shading [13]– [15]. The energy density of discrete capacitors is 100-1000 times higher than similarly scaled inductors, resulting in increased power density of the converter [7].

However, the poor voltage regulation of SC converters requires this structure to integrate with another stage of a DC-DC converter to properly regulate the voltage for the desired load. For the SEV application, the main load is the HVB, so electrical isolation is required in the DC-DC converter for safety reasons. In SEVs, the LVB is a secondary load, since it is most efficient during driving to send generated solar power directly to the LVB to power the electrical accessories. Figure 7-1(a) shows a possible design for the described system including a DPP converter for the solar cells, an isolated DC-DC converter for the HVB, and a non-isolated DC-DC converter for the LVB. This system is complex and costly as three separate converters are required. Thus, the focus of this chapter is to develop an integrated SEV architecture that can perform all these functions with a lower component count. The conceptual diagram of an integrated SEV architecture with DPP is shown in Figure 7-1(b).

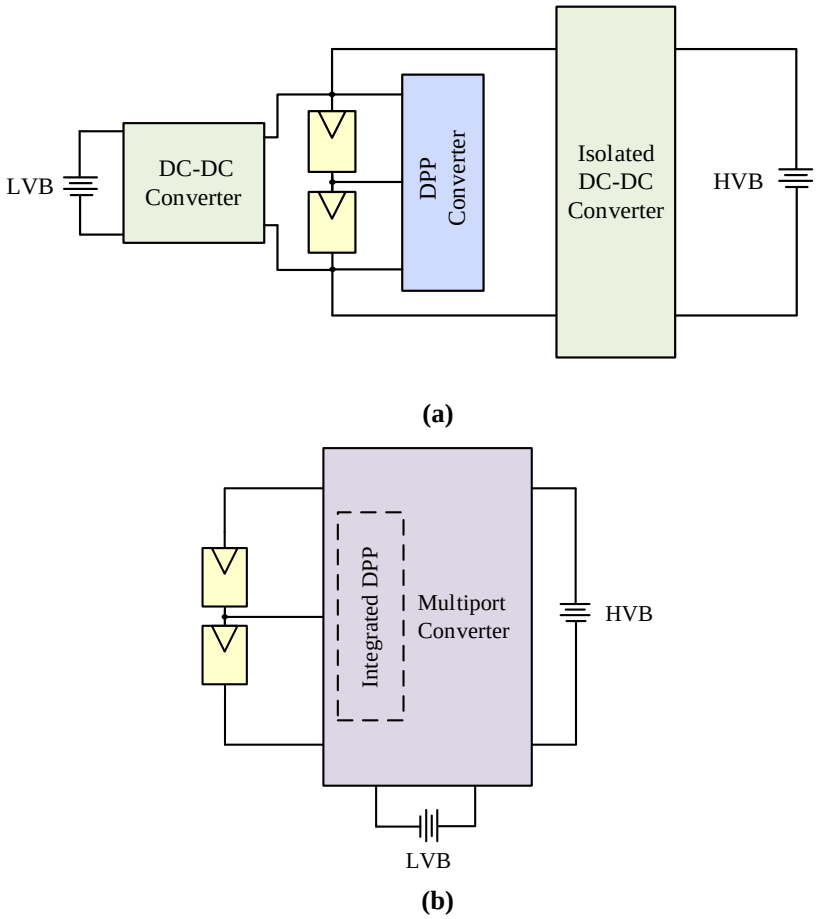


Figure 7-1: SEV architecture conceptual diagrams for a) non-integrated design with DPP, b) integrated multiport converter with DPP.

Integrated topologies including solar DPP, and a DC-DC converter are presented in [6]-[7],[9][12][16]. Since the SEV application has a solar input and two loads (HVB and LVB), integrated topologies with multiple ports [8] are of special interest.

References [9] and [16] propose non-isolated multiport converters integrated with solar DPP. In [16], a non-isolated multiport converter is proposed in which a SC converter, a series resonant converter, and a bidirectional converter are integrated to connect three PV modules, a low voltage battery, and a load. Reference [9] integrates a SC converter with DPP capability, a buck-boost converter, and a phase-shift SC converter. Pulse-width

modulation (PWM) and phase-shift modulation are used to transfer energy to a load and a low voltage battery. However, [9] and [16] are not suitable for the SEV application as they do not provide electrical isolation between the solar module and the HVB.

On the other hand, numerous papers have proposed isolated or partially-isolated multiport converters [17]– [22]. In [17], a bidirectional buck converter and LLC resonant converter are integrated to transfer power to a battery and a 45V load. It uses PWM to charge the low-voltage battery and pulse-frequency modulation (PFM) to regulate the isolated load voltage. Reference [18] integrates a dual-active-bridge converter and an interleaved PWM converter to provide an energy path from PV to low-voltage battery and load. In [19], an interleaved boost converter and an LLC converter are integrated, and the load can be charged with either PV or battery. Reference [20] integrates the phase-shifted full-bridge converter and LLC converter to charge/discharge a battery or charge a load. In [21], the proposed topology consists of two bidirectional ports and an isolated output port. The primary circuit functions as a buck-boost converter and provides a power flow path between the ports on the primary side. Reference [22] proposes four partially isolated three-port converters derived from a two-switch forward converter for renewable energy applications. However, none of these converters use DPP to improve solar energy capture during partial shading of PV modules. Furthermore, no designs or prototypes focus on a high-voltage battery load, such as in a SEV.

This research addresses these gaps by proposing a SC converter-based multiport converter with integrated DPP for solar power processing during partial shading, which also has electrical isolation in the path to a high voltage load, suitable for an EV traction

battery. The third port connects to a nominal 12V load, representing the vehicle's low voltage electrical accessories. An LLC converter is integrated with a bidirectional buck converter to regulate HVB and LVB charging. The transformer plays two roles: providing the required electrical isolation and providing the high voltage step-up gain required from PV to HVB. Thus, the proposed topology is the first to meet all the crucial requirements for an integrated SEV electrical architecture. By integrating the components, conceptually shown in Figure 7-1(b), the component count is minimized, leading to lower cost and smaller size, compared to a more conventional non-integrated topology. Furthermore, the proposed topology achieves zero-voltage switching (ZVS) at the primary side and zero-current switching (ZCS) at the secondary side even at low load, resulting in high efficiency.

The remainder of the chapter is organized as follows: Sections 7.2 to 7.4 describes the proposed integrated converter and its different modes of operation, and Sections 7.5 to 7.8 analyzes the proposed converter. Section 7.9 discusses the experimental prototype and results, and Section 7.10 summarized the chapter.

7.2 Proposed Integrated Converter

7.2.1 Overview

The proposed topology is derived from the integration of a SC-DPP converter, a bidirectional buck converter, and a unidirectional LLC converter. These three separate converters are shown in Figure 7-2(a), (b), and (c), respectively, for two solar modules connected in series. For a non-integrated solution with these converters, 8 switches are required, including the associated gate driver circuitry for each switch. The proposed

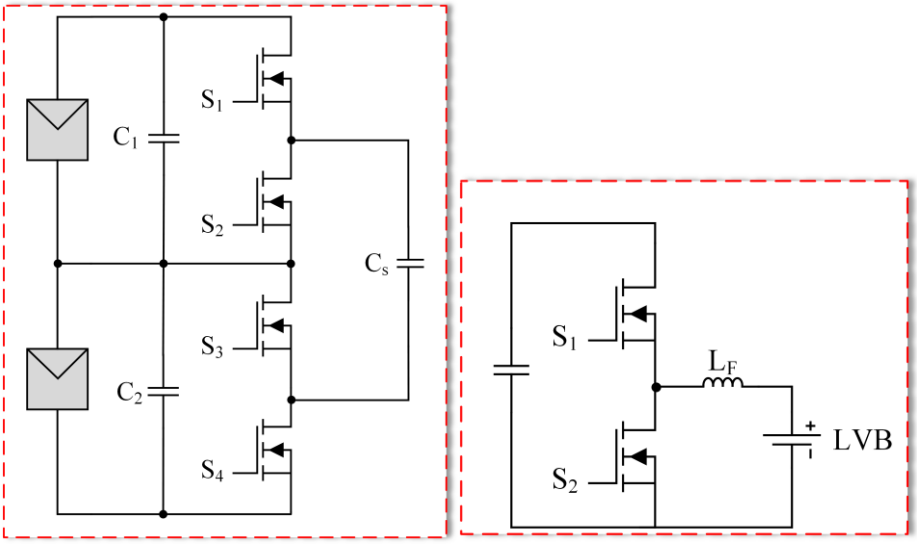
integrated topology is shown in Figure 7-2(d). In the integrated topology, switches are shared between the three converters so that a total of only 4 switches are required, significantly reducing cost and complexity compared to a non-integrated solution. The leakage inductance of the transformer is utilized as the resonance inductance, meaning only one magnetic core is required in the PV-HVB path. If more PV modules are required in series, the topology can grow vertically by adding more SC-DPP structures along with the additional modules. The proposed topology will regulate power to the HVB using PFM and to the LVB using PWM for a given input PV power, meaning the control for each port is decoupled from the other and thus the control scheme is straightforward and simple to implement.

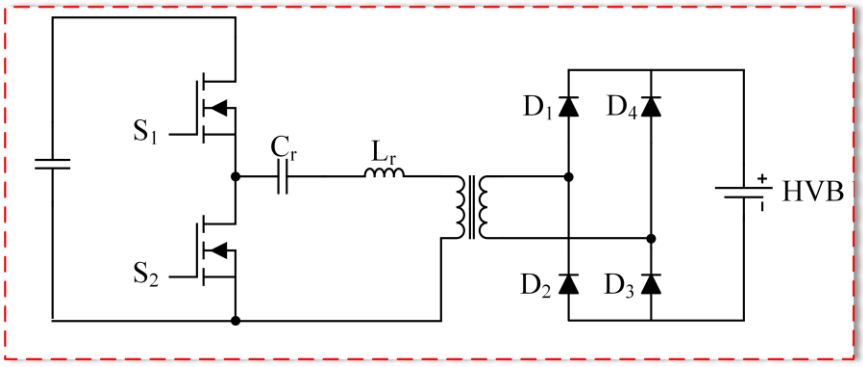
For the target SEV application, it is assumed to have one unidirectional input power source to model the PV modules, one high voltage (~ 400 V) output load to model the HVB, and one low voltage (~ 12 V) output load to model the LVB. Conventional EVs also have an isolated DC-DC converter between the HVB and LVB, often called the auxiliary power module (APM), to allow the HVB to power the low-voltage vehicle accessory loads (controllers, lights, etc.), often with a rated power around 2 – 3 kW. This APM is also required in the SEV, as the proposed topology focuses on controlling solar power flow only. The power balance for the proposed topology can be described as (1),

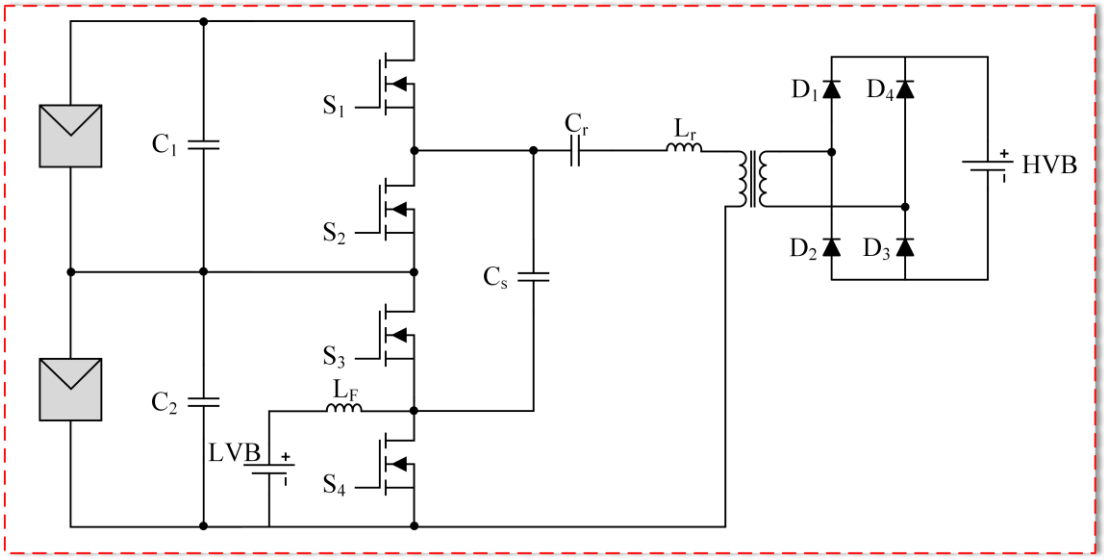
$$P_{PV} = P_{LVB} + P_{HVB} \tag{1}$$

Equation (1) guarantees that if two ports of the converter are being controlled with the two control variables of duty cycle (d) and switching frequency (f_{sw}), the power of the third port will be determined by (1).

P_{LVB} is determined at any instant by the power demand required at the LVB, which is often 400 W or more when the vehicle is on. Since it is more efficient to send low-voltage solar power directly to the LVB (rather than stepping its voltage up to the HVB and then back down through the APM, passing through 2 transformers), the priority is to send solar power directly to the LVB when it is needed for the accessory loads. Four modes of operation are possible:







(d)

Figure 7-2: Integration process of core converters to the proposed integrated topology a) SC-DPP converter b) bidirectional buck converter c) half-bridge LLC converter d) proposed integrated topology.

Dual Charging Mode ($P_{PV} > P_{LVB}$, $P_{LVB} > 0$):

In this mode, both P_{LVB} and P_{HVB} are > 0, and solar power, P_{PV}, flows to both loads because the generated solar power is greater than the requirement of the LVB. This happens when the vehicle is driving with low accessory load and high solar power generation, or when the vehicle is parked and the LVB requires low power. PFM is used to control P_{HVB} and PWM is used to control the current to the LVB. The detailed operation of this mode is described in Section II-B.

LVB Charging Mode ($P_{PV} < P_{LVB}$, $P_{HVB} = 0$)

In this mode, the solar power is less than the required P_{LVB}, so all solar power is sent to the LVB, and no power is left over for the HVB. This happens when either the vehicle is driving in low sun conditions or the vehicle accessory load is high, or both. In this mode, the HVB will be disconnected from the multiport converter and no current will flow

through the resonant network. The odd and even numbered switches in each leg will perform complementarily with PWM to control the current charging the LVB.

HVB Charging Mode ($P_{LVB} = 0$)

In this mode, all solar energy is sent to the HVB for storage. This happens most often when the vehicle is off (parked) but could also happen anytime the state-of-charge of the low voltage battery is very high, such that the LVB does not require further power for a period of time.

MPPT Mode (new partial shading pattern)

In this mode, the operation is similar to Mode 1. However, a new shading pattern is occurring for at least one of the PV modules. To extract the maximum power from the PV modules, a standard MPPT control (such as *Perturb & Observe*) can be applied by adjusting the *d* at the PV input port, and the HVB will be controlled by PFM. Unlike in Mode 1, in this mode when shading is detected, PWM is applied to $S_{1,3}$ and $S_{2,4}$ by bi-polar switching to extract the maximum PV power. In this case, unlike in the microconverter structure, the DPP feature of the topology helps the converter to process only the difference in power between the solar modules, which improves the efficiency of the system. After dealing with the shading, the converter will continue in Mode 1 operation. In this case, the difference between the available solar energy and the adjusted HVB charging power is stored in the low-voltage battery.

Understanding the DPP performance lies in the function of capacitor C_s. In the proposed topology, the C_s capacitor plays an important role in balancing the input capacitors, C_1 and C_2. As the PWM duty cycle changes based on the charging requirements of the LVB, the

voltage across C_1 and C_2 can be unbalanced. However, the proposed circuit has a self-balancing feature: when S_1 and S_3 turn on, the voltage across C_s will be equal to C_1 and when S_2 and S_4 are on, the voltage across C_s will be equal to C_2. Accordingly, any imbalance of electric charge between C_1 and C_2 will be handled by C_s.

7.3 Detailed Operation

This subsection describes the detailed operation of Mode 1 (Dual Charging Mode), which also applies to Mode 4 (MPPT Mode). The only difference between these two modes is that PWM is used in Mode 1 to control the current charging the LVB, while in Mode 4, the PWM is used to perform the MPPT algorithm. The converter is operated in continuous conduction mode for both the paths to the HVB and LVB. With the assumptions that the dead-time is negligible, and all switches are ideal, the topology operation is described and shown in Figure 7-3. Also, the waveforms of switches and magnetizing and resonance inductors are shown in Figure 7-4.

Interval 1(Figure 7-3(a)): In this interval, S_1 and S_3 are turned on when the current is still flowing in their respective anti-parallel diodes (ZVS condition). A quasi-sinusoidal current is flowing within the resonant network with the resonant frequency f_r. The output transformer, diode rectifier, and filter establish a DC output voltage from the sinusoidal tank currents. The power flows into inductance L_F and charges the LVB. C_s is charged by the PV modules. At end of this interval, the magnetizing current and quasi-sinusoidal current meet which results in zero current of the secondary diodes. The sum of the voltage of C_1 and C_2 is clamped to V_{in} as,

$$V_{in} = V_{C_1} + V_{C_2} = 2V_d \tag{2}$$

where V_d is the nominal voltage across each solar module. The total charge of both capacitors is constant. As a result, as much as C_1 charges, C_2 discharges,

$$i_{C_1} = -i_{C_2} \tag{3}$$

Interval 2 (Figure 7-3(b)): At the beginning of the interval, D_1 and D_3 block the current as the increase in magnetizing current leads to negative winding current in the secondary of the transformer. At $f_{sw}<f_r$, the diodes will naturally be turned off and ZCS occurs. In this interval, the solar power does not flow to the HVB and constant current flows to the LVB. At the end of this interval, S_1 and S_3 are turned off.

Interval 3 (Figure 7-3(c)): In this interval, S_2 and S_4 turn on with ZVS. The voltage across the primary and resonant inductance becomes negative, resulting in lowering the magnetizing inductance and resonant tank current. After the resonant tank current becomes negative, C_s and the magnetizing inductance will charge the HVB. The voltage across L_F is also negative and will start to charge the LVB. At t_5, both magnetizing and resonant tank currents become the same and the rectifying diodes will block the current afterwards.

Interval 4 (Figure 7-3(d)): In this mode, the power will not flow to the HVB and current flows to the LVB. At the end of this mode, S_2 and S_4 are turned off. As the current passes through the anti-parallel diode of S_4, the switch will be turned off with ZCS.

7.4 Converter Analysis

The resonant tank consists of a series resonant inductance L_r, a magnetizing inductance L_m, and a resonant capacitor C_r. The upper and lower switching devices are modulated in a complementary fashion, with an appropriate dead-time.

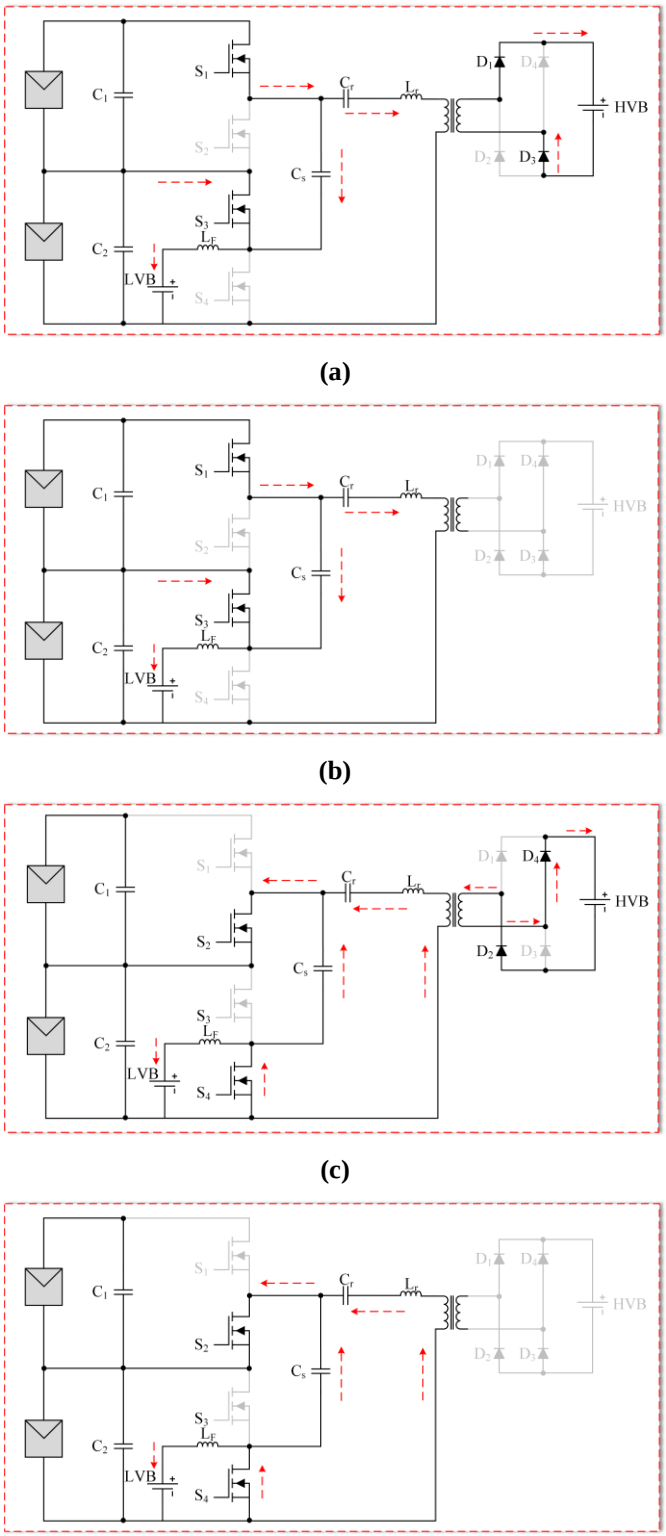


Figure 7-3: Operational intervals for Mode 1, (a) Interval 1 (b) Interval 2 (c) Interval 3 (d) Interval 4

The square-wave voltage input results in a quasi-sinusoidal current flowing within the resonant network. Changing the frequency of the square-wave voltage input from the half-bridge changes the effective impedance of the resonant tank, and therefore the resulting output current. There are two resonant frequencies for the LLC converter.

The series resonant frequency of the LLC converter, f_r, is the point where the L_r and C_r combination have zero impedance and the gain M is unity (in a lossless circuit). The second resonant frequency is caused by the combination of L_m, L_r, and C_r. These two frequencies are shown as (4) and (5),

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{4}$$

$$f_m = \frac{1}{2\pi\sqrt{(L_r + L_m)C_r}} \tag{5}$$

Defining m as (6),

$$m = \frac{L_r + L_m}{L_r} \tag{6}$$

It can be concluded that $f_m = \sqrt{m} f_r$. A reasonable initial value for m is between 6 and 10 which makes fm two to three times fr. Lower values of m can achieve higher boosting gain, in addition to a narrower range of the frequency modulation, meaning more flexible control and regulation, which is valuable in applications with a wide input voltage range. Nevertheless, low values of m for the same quality factor Q and resonant frequency fr means smaller magnetizing inductance Lm, hence, higher magnetizing peak-to-peak current ripple, causing increased circulating energy and conduction losses.

7.5 LLC Voltage Gain Derivation

The proposed topology uses an LLC converter to transfer power from the low voltage PV modules to the HVB. The resonant tank will be excited at a switching frequency close to fundamental frequency, which can vary the voltage gain of resonant tank. However, the gain depends not only on the switching frequency and tank design, but also on the converter load resistance, R_O. The DC output resistance R_O can be approximated by an equivalent AC load resistance R_e. R_e is used to calculate the quality factor, Q, which defines how the resonant gain changes as a function of frequency, in (7) and (8). N_p and N_s are the number of turns at the primary and secondary sides of the transformer, respectively.

$$R_e = \frac{8}{\pi^2}\left(\frac{N_p}{N_s}\right)^2 R_O \tag{7}$$

$$Q = \frac{1}{R_e}\sqrt{\frac{L_r}{C_r}} \tag{8}$$

With the approximation of $L_{lks} = \left(\frac{N_p}{N_s}\right)^2 L_{lkp}$, where L_{lkp} and L_{lks} are the leakage inductances of the primary and secondary sides of the transformer, fundamental harmonic approximation analysis can be applied. The equivalent leakage inductance at the primary side can be modeled as resonant inductance, Lr, or a part of it. The equivalent circuit is shown in Figure 7-5. The square wave applied to the resonant tank has a peak of Vd, and its fundamental component, v_{d_1}, is shown in (9), where $\omega_{sw} = 2\pi f_{sw}$.

$$v_{d_1} = \frac{2V_d}{\pi}\sin(\omega_{sw}t) \tag{9}$$

$$V_{\mathrm{Re}} = \frac{4nV_O}{\pi}\sin(\omega_{sw}t) \tag{10}$$

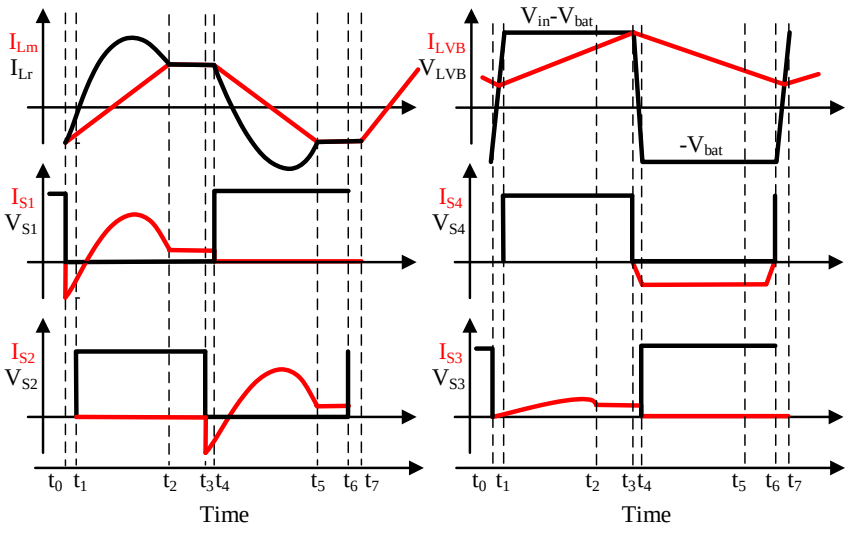


Figure 7-4: Waveforms of the proposed integrated converter in Mode 1

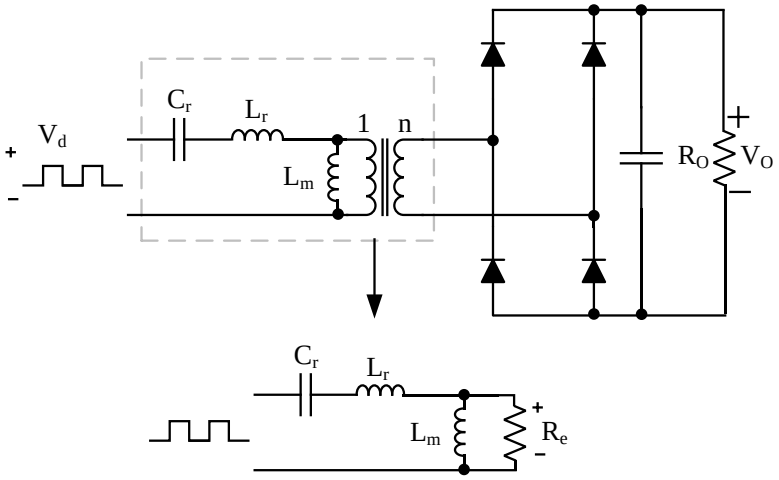


Figure 7-5 :The fundamental harmonic approximation of the LLC converter

The gain of the LLC converter can be written as,

$$M_{LLC} = \frac{1}{2} nM \tag{11}$$

where M is the gain of the resonant tank, given as,

$$M = \frac{F_n^2 (m-1)}{\sqrt{(mF_n^2 - 1)^2 + F_n^2 (F_n^2 - 1)^2 (m-1)^2 Q^2}} \tag{12}$$

The normalized frequency is defined as $F_n = f_{sw}/f_r$. Figure 7-6 shows a series of curves highlighting how the switching frequency and quality factor impact the gain of a lossless converter. The simulation is done for m=6.2. In Figure 7-6, the dashed line shows the point where the phase of the resonant circuit is zero, indicating a transition from a capacitive current in the resonant tank at lower frequencies to an inductive current at higher frequencies. Maintaining an inductive current is essential to achieve ZVS on the primary half-bridge. This also maintains a consistent relationship where increasing the converter switching frequency results in a decreased voltage gain.

7.6 PWM Converter

The PWM converter operates very similarly to a conventional buck converter. S_3 and S_4 act as the main switch and the diode of the buck converter respectively. The only difference between this buck converter and a conventional one is that C_2 and C_s both discharge their current to the LVB. The voltage conversion ratio based on the PWM converter is,

$$V_{LVB} = dV_d \tag{13}$$

where d is the duty cycle of S1 and S3. S2 and S4 will operate in a complementary way. The PWM converter will control the LVB by adjusting the duty cycle. In order to decouple the frequency modulation technique which controls the high voltage battery, intervals 2 and 4 are vital. These intervals allow the switches to be turned on naturally with ZVS and diodes turned off naturally with ZCS. Accordingly, twice the duty cycle must be between the normalized frequency (Fn) and (2-Fn). The formula presented in (14) will satisfy this requirement.

$$F_n < 2d < 2 - F_n \tag{14}$$

Considering that the minimum frequency for the LLC converter to work in the inductive region is around half of the fundamental resonant frequency, the duty cycle will be approximately between 0.25 and 0.75. Assuming the nominal voltage of each solar module (Vd) is 30 V, the LVB ranges from minimum 8 V to maximum 16 V (at duty cycle of 0.53).

7.7 ZVS Condition

In order to achieve the ZVS condition, there should be lag between the resonant current and the input voltage of the LLC resonant tank. The switched capacitor Cs is large, so it will not affect the ZVS condition for switches S1 and S2. According to the investigated operational intervals, the anti-parallel diode of S4 will be on when the switch turns on so the ZVS condition will be satisfied on the condition that an appropriate dead-time is applied to the switches. If the lag between the resonant current and input resonant voltage is θ, the value of the resonant current at half of the resonant period (Tr) must be large enough to discharge the stored charge in the drain-source capacitor of the switches in the dead-time,

$$i_{Lr}(\frac{T_r}{2}) = \sqrt{2} I_r \sin(\theta) \geq \frac{4 C_{ds} V_d}{T_{dead}} \tag{15}$$

where Tdead is the dead-time between S1,2 and S3,4. The input power of the resonant tank can be expressed as,

$$P_{in} = \frac{V_d I_r}{\pi} \cos(\theta) \tag{16}$$

From (15) and (16), the needed lag for the ZVS condition can be written as,

$$\tan(\theta) \geq \frac{2C_{ds}V_d^2}{\pi P_{in} T_{dead}} \tag{17}$$

The input impedance of the resonant tank shown in Figure 7-6 is,

$$Z_{in} = sL_r + \frac{1}{sC_r} + \frac{R_e(sL_m)}{R_e + sL_m} \tag{18}$$

The normalized impedance can be expressed as,

$$Z_{in} = \frac{F_n^2(m-1)Q}{1+F_n^2(m-1)^2Q^2} + j\left(\frac{F_n(m-1)}{1+F_n^2(m-1)^2Q^2} + \frac{F_n^2-1}{F_n}\right) \tag{19}$$

The value of tanθ can be written as the ratio of the imaginary part of the input impedance over the real part of the input impedance.

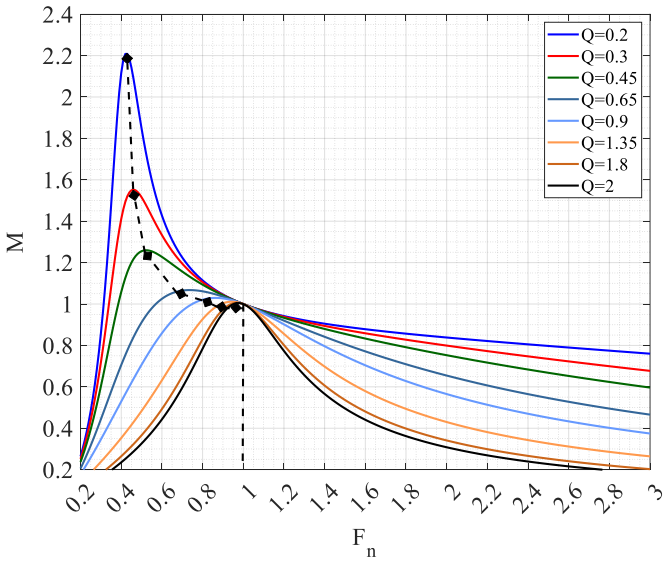


Figure 7-6: Resonant tank gain, M, as a function of normalized frequency for m=6.2

Using (19), the ZVS condition stated in (17) can be rewritten as,

$$Q(F_n - \frac{1}{F_n}) + \frac{mF_n - 1}{(m-1)^2 QF_n^3} \geq \frac{2C_{ds}V_d^2}{\pi P_{in} T_{dead}} \tag{20}$$

7.8 Proposed Control Strategy

According to the operational modes described in Section II, a proposed closed-loop control diagram is shown in Figure 7-7. PWM is used for MPPT control (when new partial shading patterns appear) or charging the LVB (at all other times), and PFM is used to control HVB charging. A control loop is designed so that the voltage of the HVB is sampled and compared to a reference voltage, and a feedback signal (VF) will be generated which is sent to a microcontroller. In the controller, according to different modes, the appropriate pulse with a certain duty cycle and frequency based on (14) will be produced.

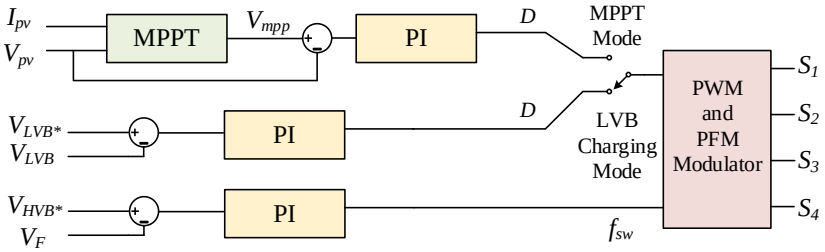


Figure 7-7: Proposed control loop for the proposed topology

7.9 Experimental Prototype and Results

The converter is designed for a solar-charged EV application with two PV modules in series, a HVB port with a voltage range of 250 – 400 V, and a LVB port of 8 – 16 V. Table 7-1 gives the full specifications of the proposed three port converter. The nominal voltage of the HVB is 380 V, and the nominal voltage of the PV modules is 30 V each, for a total around 60V. As the primary side of the LLC is a half-bridge topology, the turns ratio of the transformer can be calculated as,

$$n = \frac{V_{HVB(nom)}}{V_{d(nom)}} = \frac{380}{30} = 12.67 \tag{21}$$

Table 7-1: Specifications of the Proposed Converter

Components	Values
PV Module Voltage Range	25-35 V
HVB Voltage Range	250-400 V
Nominal HVB Voltage	380 V
LVB Voltage Range	8-16 V
Resonant Frequency	110 kHz
Minimum Switching Frequency	50 kHz
Dead time	300 ns
Maximum HVB power level	200 W
Maximum LVB power Level	80 W
Maximum Quality Factor	0.45
m	6.2

The transformer is custom-made using an EPC40 ferrite core with magnetizing inductance of 9.5 μH and leakage inductance of 0.1 μH. Based on (21), the turns ratio is set to 4:51. The maximum power rating of the LLC converter is set to be 200 W and Q_{max} is chosen as 0.45 to ensure the voltage gain requirement is met at maximum load. The value of m is set to be 6.2 to minimize the circulating current losses and also to provide enough voltage gain to charge the HVB battery. According to (4)-(11) the value of C_r, L_r, and L_m are calculated as shown in Table 7-2, along with the other design parameters. The output capacitor is selected for 1% output voltage ripple.

Figure 7-8 shows the experimental prototype of the proposed converter. Two inductors MSD1514-123MEB (24 μH) are used in series to provide enough inductance for continuous input current for the LVB port. According to the power rating, the programmable load is set to a constant resistance mode to provide the power balance expressed in (1). Measurements are obtained using Tektronix current and differential voltage probes.

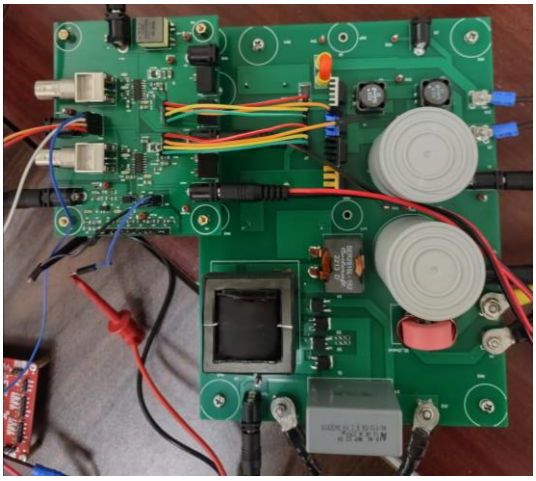


Figure 7-8: The experimental setup of the proposed converter

Figure 7-9 shows experimental results for $2V_d = 60V$, $V_{HVB} = 380V$, $P_{HVB} = 200W$, $V_{LVB} = 13.2V$, and $P_{LVB} = 80W$. The HVB output voltage ripple is 3 V which is less than 1% voltage ripple. Figure 7-10 and Figure 7-11 show the switches' drain-source voltages and currents and verify the ZVS turn-on for all switches. Furthermore, ZCS turn-off is achieved for S_1 and S_4. Figure 7-12 shows the measured experimental efficiency, η, for different power levels of PHVB, which is calculated based on (22).

$$\eta = \frac{P_{LVB} + P_{HVB}}{P_{in}} \tag{22}$$

Table 7-2: Design Parameters of the Proposed Multi-port Converter

Components	Values
Resonant Capacitor (Cr)	Film capacitors 1250 V,1.8 µF
Resonant Inductor (Lr)	Fixed inductors 1.5 µH, 100 A 1.65 mΩ
Magnetizing Inductor (Lm)	9.5 µH
Transformer	Custom made EE40, 1:13
The SC capacitor (Cs)	Film capacitors 350 V, 65 µF
Input Capacitors (C1, C2)	Aluminum electrolytic, 100 V, 220 µF
LVB inductor (Lf)	48 µH,10 A
SC switches	(TK100A08N1), 80 V MOSFETS
Rectifier Diodes	600 V, 5 A, (RFNL5BGE6STL)
Output Capacitor	Film capacitors 50 µF, 500 V
Microcontroller	TI Launchpad, F280049C

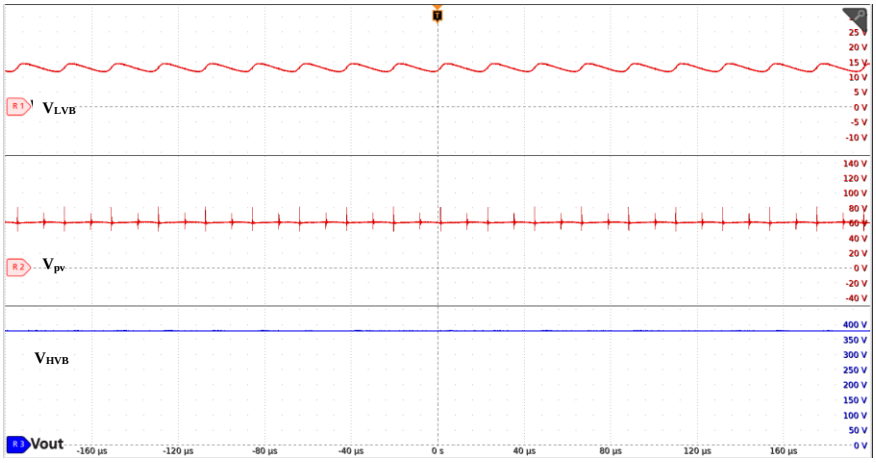


Figure 7-9: Three port electrical waveforms at P_{LVB}=80W, P_{HVB}=200W

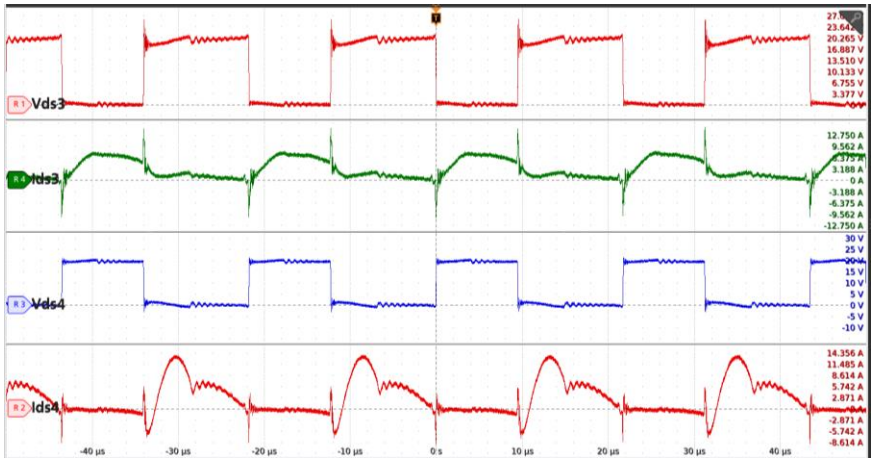


Figure 7-10: The drain-source voltage and switch current of S_3 and S_4

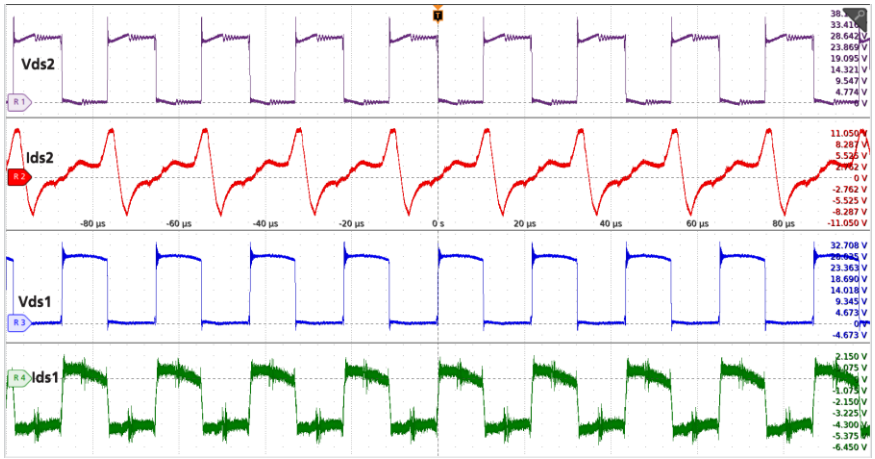


Figure 7-11: The drain-source voltage and switch current of S_1 and S_2

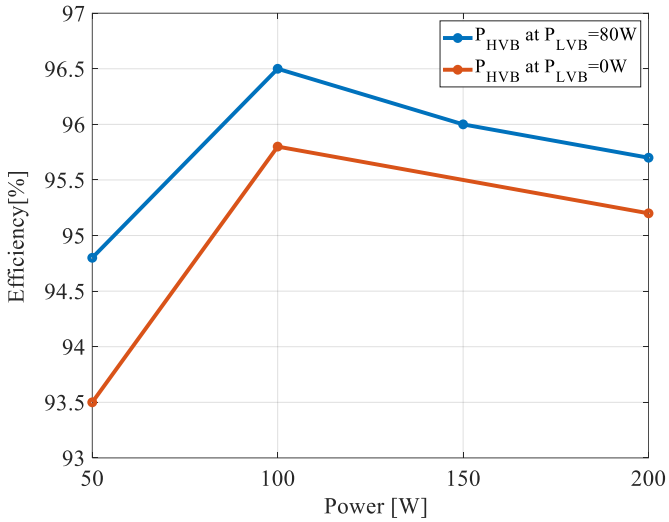


Figure 7-12: Experimental efficiency results for different levels of P_{HVB}, when P_{LVB} is 80 W or 0 W, $2V_d$ = 60V, V_{HVB} = 380 V, V_{LVB} = 13.2 V

Figure 7-13 shows the measured experimental efficiency curves for different charging powers at the LVB port when the HVB port is being charged with 100 W.

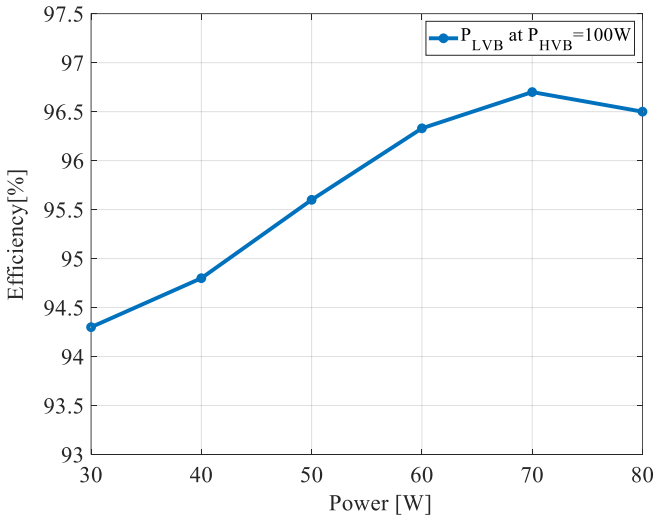


Figure 7-13: Experimental efficiency results for different levels of PLVB when P_{HVB}=100W, $2V_d$ = 60V, V_{HVB} = 380 V, V_{LVB} = 13.2V

In all measurements the voltage across the three ports is respectively, $2V_d$ = 60V, V_{HVB} = 380 V, and V_{LVB} = 13.2 V. The prototype peak efficiency in dual charging mode is 96.7%,

and the peak efficiency in HVB charging mode is 95.8%. Furthermore, additional experiments show that when 80 W of solar power is only sent to the LVB (peak power for the LVB path), the efficiency is 94%.

In order to show the control performance and verify that the two output ports can always be controlled independently, Figure: 7-14 shows that as the HVB charging current reduces, the voltages across the LVB and HVB ports remain almost constant. Furthermore, in Figure: 7-15, the charging current of the LVB reduces, but the control loop keeps the voltages across the LVB and HVB ports almost constant.

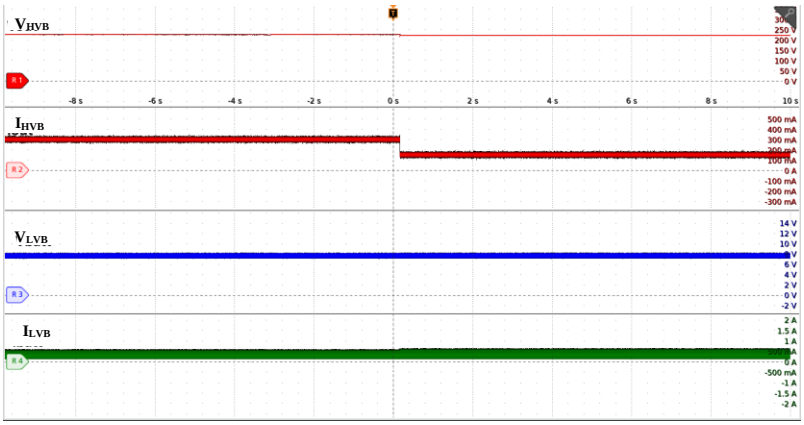


Figure: 7-14 The dynamic characteristics of the converter when IHVB changes from 0.3A to 0.15A

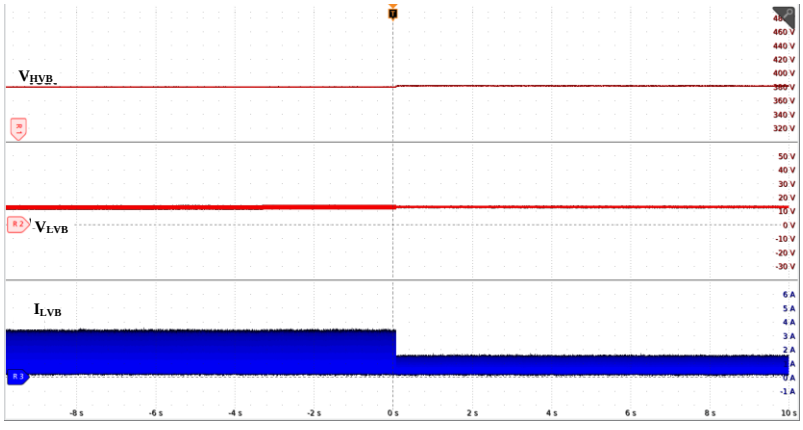


Figure: 7-15: The dynamic characteristics of the converter when ILVB changes from 2A to 1A

7.10 Summary

This chapter presents a novel multiport converter for use in solar-charged EVs, where input solar power can flow to the high-voltage traction battery (with electrical isolation) and/or the low-voltage bus for vehicle electrical accessories. A main novelty is that an integrated SC-based DPP converter is used to maximize solar power generation during partial shading conditions. Furthermore, an integrated LLC converter and buck converter provide the charging paths to the HVB and LVB ports, respectively. Compared to a non-integrated solution, which would require 8 switches, the proposed integrated multiport converter requires only 4 switches, significantly reducing the cost and complexity of the circuit. The proposed control is straightforward, with PFM used to control the HVB port, and PWM used to control the LVB charging and DPP performance. ZVS is achieved for all switches over a wide power range, leading to high efficiency. The 200 W prototype exhibits peak efficiency of 96.7% in dual charging mode (power to both HVB and LVB) and 95.8% in HVB charging mode. Future work will focus on adapting the design for use with EVs employing 800 V batteries.

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Chapter 8

Conclusions and Future Work

8.1 Conclusions

One approach to extend the driving range of EVs or reduce the charging requirement from the grid is to employ solar arrays on the upwards-facing surfaces of EVs. The goal of this thesis is to propose novel power electronic architectures which can transfer solar energy to the vehicle loads (high voltage and low voltage bus) in an efficient way with low component count. This research has first proposed two novel non-isolated high step-up dc-dc converters with high efficiency that can be used in the SEV application, along with a generalized methodology for comprehension of such converters. The main feature of the first converter (Chapter 3) is low input current ripple, which is required for PV cells. The main feature of the second converter (Chapter 4) is high voltage gain with a low number of components, which would be especially useful for a SEV with a very high voltage battery or low voltage PV array.

The generalized method in Chapter 4 was developed because many converters are proposed in the literature which use many techniques to achieve high step-up voltage gain. Many of these converters are a variation of the same converter. For the same voltage gain at the same pulse requirement, many converters with different numbers of active and passive components exist. The question is, how do these techniques affect the voltage gain or voltage stress of the switches, or how one can design a converter for a specific gain requirement with minimum number of components and high efficiency? The novel generalized methodology for designing high step-up converters was proposed to address this question. The research presents a novel generalized method to derive the voltage gain of boost-based converters using switch capacitor (SC), couple inductor (CI), and voltage

multiplier cells (VMC) techniques. The proposed generalized method uniquely reveals the unifying theory underlying boost-based converters with any variation of SC/CI/VMC (with one switch and one CI core) and requires only four equations for gain.

An integrated power electronic approach for SEVs is presented in Chapter 5, which relies on a flying capacitor topology for both battery charging and driving the motor. The solar energy is used to solve the common problem of balancing the flying capacitors, which at the same time helps the solar voltage boost problem since the solar power no longer needs to be boosted to the full battery voltage.

Chapter 6 performs a simulation-based investigation of two SEV architectures. In the first architecture, the solar arrays transfer power to the low voltage battery through a buck converter and to the high voltage battery using a bidirectional auxiliary power module (APM). This system uses few components because the APM already exists on the vehicle is reused for the SEV purposes. However, the efficiency path of the isolated DC-DC converter is not high at low power (~500 W) compared to its nominal design which is (~3 kW). The second approach uses non-isolated DC-DC converters to transfer the power directly to the high voltage battery. Although a separate high step-up converter must be installed on the vehicle, the efficiency is higher than the first approach. Detailed PLECS efficiency results are added to a vehicle model to investigate the efficiency during a real drive cycle with multiple solar radiation profiles. The results show that the best high step-up boost converter yields 9.9% higher efficiency than the best converter in the architecture utilizing the existing APM, but has 2.8 times the cost.

In Chapter 7, a partly-isolated three-port converter is proposed for interfacing the solar arrays, low voltage battery, and high voltage battery. The performance of the converter is improved by employing differential power processing (DPP) converters which will process only the power difference between the solar arrays and improves the power density and efficiency of the system. An integrated DPP with isolated LLC is designed to charge the high voltage battery. Also, a path for charging the low voltage battery is integrated with the topology. The proposed converter uses fewer components than a discrete converter approach, and achieves very high efficiency.

8.2 Future Work

Further investigation of integrated topologies including solar arrays and high voltage and low voltage batteries can be an interesting idea to move forward on this topic. Other topologies and control methods can be explored, to extend the research in Chapter 7. It is suggested this work should include an isolated path from the solar array to high voltage battery, since this is the most challenging type of architecture in terms of efficiency and power density.

Another approach can be to improve the design of the bidirectional APM so that it can offer higher efficiency at the lower solar powers. Interleaving could be used to achieve this, where only some phases operate at a time, depending on the power level. If the APM is used in the solar architecture, system-level simulations studies can be performed to determine the appropriate control strategy (meaning how much solar power is transferred directly to the 12 V bus, and when), and to quantify the net energy use benefit of the vehicle of sending solar power directly to the 12 V bus when the vehicle is on.

Further investigation can be made into MPPT control of the solar arrays, with a focus on fast algorithms for quickly finding the new maximum power point, possibly even when the vehicle is moving, and shading patterns are changing quickly. New MPPT algorithms can be adopted and developed for this purpose to increase the efficiency and reliability of the system throughout the day for many different solar radiation patterns.

Regarding Chapter 5, the 3-phase rectifier/inverter can be investigated for the proposed topology, and the RSS table can be adapted according to the 3-phase system. An exact model of the motor can replace the previous generic motor model of MATLAB, and the THD and PF in inverter mode and rectifier mode can be investigated more in detail.

Another interesting opportunity will be applying the proposed method, circuits, and analysis performed throughout the whole thesis on larger solar-charged vehicles such as transport trucks or busses. The integration of larger solar areas results in much higher power captured by the solar cells, and integration will be different. An analysis can be done on different truck sizes to identify the most optimum topological options for harvesting the solar power.