MULTI-SOURCE DUAL ACTIVE BRIDGE DC/DC CONVERTER FOR MORE ELECTRIC AIRCRAFT: DESIGN, CONTROL, AND PERFORMANCE OPTIMIZATION

MULTI-SOURCE DUAL ACTIVE BRIDGE DC/DC CONVERTER FOR MORE ELECTRIC AIRCRAFT: DESIGN, CONTROL, AND PERFORMANCE OPTIMIZATION

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A THESIS

SUBMITTED TO THE DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

AND THE SCHOOL OF GRADUATE STUDIES

OF MCMASTER UNIVERSITY

IN PARTIAL FULFILMENT OF THE REQUIREMENTS

FOR THE DEGREE OF

DOCTOR OF PHILOSOPHY

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Doctor of Philosophy (2022) McMaster University

(Electrical and Computer Engineering) Hamilton, Ontario, Canada

TITLE:	Multi-Source Dual Active Bridge DC/DC Converter for More Electric Aircraft: Design, Control, and Performance Optimization
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NUMBER OF PAGES:	xxvii, 178

Abstract

System reliability and design optimization are the main concerns in power electronic converters of more-electric aircraft (MEA). The fundamental distribution networks of aircraft are reviewed to establish context. The Isolated DC-DC converters are considered the building blocks of modern aircraft electrical power distribution systems (EPDSs). The DC/DC converters transfer power from the main generation direct current (DC) bus to various loads aboard the aircraft. As a result of the electrical power demand increase in the emerging EPDSs of MEA architectures, more energy storage systems (ESSs) are utilized in the distribution network. A single DC/DC converter unit is conventionally dedicated to each energy source. This thesis focuses on replacing several DC/DC converters used in the existing distribution networks by more optimized multi-source converter units.

Standard industry and literature topologies are reviewed including structures aimed for multi-source system integration. The topology proposed in this thesis aims for a multiple sources/loads integration to improve the power density of the distribution network. The different operating modes of the proposed topology add flexibility to the system enabling power flow between different sources, while controlling the power supplied to the low voltage (LV) network on the aircraft. Better system utilization is achieved as compared to conventional solutions. The system stability

is improved considering that the multi-source dual active bridge (MSDAB) topology can be configured to stabilize the high-voltage DC (HVDC) generation bus in case of voltage sag. A power-flow mechanism between the different sources utilizing the magnetizing inductance of the transformer is proposed and discussed as one of the operating modes of the converter.

A design process using genetic algorithm (GA) optimization is introduced to optimally select the converter parameters to minimize the converter RMS current. The mathematical model of the proposed MSDAB topology is developed based on Fourier transform of key converter waveforms. The optimization is split into two layers; the first is to select the hardware components and the second is to optimize the converter control parameters. Simulation and experiments of the control schemes were performed to validate optimal operation of the proposed converter.

A review of the magnetic components in MEA DC/DC converters is conducted. The high-frequency transformer utilized in such converters is the major contributor to the size and weight besides the thermal management system. An optimization design methodology is introduced to minimize the transformer core size and improve the converter performance through optimized winding configurations. Different magnetic materials, winding configurations, and core paralleling are considered in the optimization process.

The trade-offs between the converter efficiency and transformer power density are discussed. The transformer parasitic elements effect on the converter performance is presented. Multi-layer minimum gradient (MLMG) winding configurations are proposed to eliminate the high-frequency oscillations (HFO) caused by the transformer parasitics. The proposed configurations resulted in better converter performance with

20% improvement in the transformer volume as compared to a similar conventional configurations. Three different transformer configurations are implemented and validating experimentally using an impedance analyzer. The improvements on the converter performance are highlighted through finite element analysis (FEA) simulations and converter experiments.

This work is dedicated to my parents, Mona and Ibrahim, and my sister Heba.

Acknowledgements

I would like to thank my supervisors, Dr. Mehdi Narimani and Dr. Ali Emadi, for the continuous support and encouragement. I am grateful for Dr. Ali Emadi for giving me the opportunity to grow professionally at the McMaster Automotive Resource Center (MARC). Dr. Mehdi Narimani, thank you for your technical feedback and guidance throughout my studies.

I would like to extend my profound appreciation to my committee members; Dr. Berker Bilgin and Dr. Armen Baronian for their insightful feedback during my committee meetings.

This research was undertaken in part, thanks to funding from Mitacs through the Mitacs Accelerate program and EATON Aerospace Group.

I am deeply indeptent to Nilou Keshmiri for the encouragement and support throughout the duration of my PhD studies. To James Emmens, Maryam Alizadeh, Yuhang Yang, Kyle Kozielski, Rachit Pradhan, Peter Azer and all my friends at MARC, thank you for the great time and memories.

I'm extremely grateful to all my friends back home and in Canada. Thank you to Medhat, Rasha, Mai, Essam, Husssien, Ali, Adel, Abubakr, Pola, Ayman, Omar, Tarek, and Eslam for your support and friendship.

Words cannot express my gratitude for the unconditional love from my parents,

Mona and Ibrahim, my sister Heba, and all my cousins. Thank you for your continuous support throughout my studies.

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Abbreviations and Symbols

Abbreviations

MEA	more electric aircraft
EPDSs	electrical power distribution systems
DC	direct current
ESSs	energy storage systems
LV	low voltage
MSDAB	multi-source dual active bridge
GA	genetic algorithm
MLMG	Multi-layer minimum gradient
HFO	high-frequency oscillations
FEA	finite element analysis
HV	high-voltage

DAB	dual-active-bridge
LUT	look-up-table
MPECs	modular power electronic cells
APU	auxiliary power unit
HVDC	high voltage dc
KB-APU	kerosene-based auxiliary power unit
SSPCs	solid state power controllers
CSM	constant speed motor
AEA	all electric aircraft
LVDC	low voltage direct current
ZVS	zero-voltage switching
ZCS	zero-current switching
FBPP	Full-bridge push pull
FB	Full-bridge
MOSFETs	metal?oxide?semiconductor field-effect transistors
SPS	Single phase shift
TPS	Triple phase shift (SPS)
CHB	cascaded H-bridge

FC	flying capacitor
NPC	neutral point clamped
ANPC	active neutral point clamped
IPOP	input-parallel-output-parallel
ISOP	input-series-output-parallel
QAB	quadruple-active bridge
DPS	dual phase shift
RMS	root mean square
CM	common mode
DM	differential mode
AP	area product
MMF	magnetomotive force
SiC	Silicon Carbide
CC-CV	constant-current constant-voltage

Symbols

D	Duty cycle
N	Transformer turns ratio

V_{in}	Input voltage
V_{out}	Output voltage
D_1	Duty cycle of the boost stage
f_n	normalized frequency
f_{sw}	switching frequency
f_o	resonance frequency of the added tank
L_n	inductance ratio
L_m	magnetizing inductance
L_r	external resonant inductor
Q_e	quality factor
R_e	reflected output resistance to the primary side
V_{br1}	primary bridge output
α	multilevel primary inner phase shift 1
β	multilevel primary inner phase shift 2
ϕ	multilevel primary-to-secondary phase shift
L_{lkg}	leakage inductance
ϕ	is the DPS primary to secondary phase shift
ϕ_{in}	DPS inner phase shift

J	winding current density
k_t	topology factor
B_{max}	maximum flux density
F_r	AC/DC losses ratio
δ'	skin depth.
M	number of layers
t	copper thickness
L_{ext}	external inductance
P_{core}	transformer core loss
P_{copper}	transformer copper losses
P_{tot}	total transformer losses
K_u	utilization factor
MLT	mean length per turn
W_A	window area
n	number of turns
ρ	copper resistivity
$R_{winding}$	winding resistance
I_{tot}	total current referred to the primary side

λ	voltseconds
B_{max}	maximum flux density
A_c	core area
V_{core}	core volume
β	Steinmetz exponent
K_{fe}	frequency-dependant constant
K_{gf}	geometrical constant
B_{sat}	saturation flux
V_i	voltage across turn
C_p	individual turn's capacitance
E_i	individual turn's energy
C_{eqv}	equivalent capacitance
E_{tot}	total layers energy
i_L	inductor current
V_{br2}	secondary bridge voltage
Z_L	inductor impedance
I_{rms}	Inductor RMS current
$W_{i,j,k}$	operating point weighting factor

L_{max}	maximum allowed inductance
ϕ_f	fundamental phase shift
P_avg	average power
P_{out}	output power

Chapter 1

Introduction

1.1 Background and Motivation

As a step towards more efficient and sustainable aircraft, electric solutions have started to emerge replacing the traditional pneumatic, hydraulic, and mechanical systems in more electric aircraft [1–4]. The Advisory Council for Aeronautics Research in Europe (ACARE) has specified a long-term roadmap aimed to reduce Co_2 emissions by 75% and NO_x by 90% by 2050 [5]. The electrical loads on a conventional aircraft include avionic systems, entertainment systems, air conditioning and lighting systems [6]. Efforts have being made in the design of compact, lightweight electric power distribution systems while enhancing the efficiency and increasing the power handling capabilities. Several articles have investigated the progression of the system architecture of aircraft [7–9]. The evolution of the system architectures of aircraft is dependant on the increase of the electrical power demand and utilized electrical components [10]. With the increased electrical power demand, new challenges arise regarding the design aspects of the electrical components utilized.

Among the required electrical power units aboard the aircraft, one can cite AC/DC rectifier units, DC/AC inverters and DC/DC converters. For modernized more electric networks, DC/DC converters are considered the building blocks of the aircraft architecture. Previous review articles in literature focuses either on the system level architecture of the modernized electrical network in the aerospace industry [1, 7–9], or the technical theory of the utilized power conversion elements such as the DC/DC converters [11]. There is a trend towards moving to higher-voltage systems to improve the distribution system's efficiency, which impacts the design of the DC/DC converters aboard the aircraft. The DC/DC converters are used to link the main high-voltage (HV) generation bus to the LV link. The DC/DC converters provide isolation

between the LV and HV DC links as well as regulating the LV bus as mandated by industry regulatory standards.

DC/DC converter configuration is an interdisciplinary design problem. Most commercialized MEA DC/DC converters use traditional dual-active-bridge (DAB) based topology as they feature simple control, high efficiency and have a bidirectionality nature.

With the movements towards more electric energy sources aboard the aircraft, several derivatives of the conventional MEA structures has been developed recently to better integrate the different energy sources. Among the emerged topologies are the multi-port and multi-source DC/DC converters which introduce an apparent solution for improved power density and system utilization. The multi-output configurations in literature either depends on paralleling or serializing low-power converter cells. Another approach is magnetically coupling the different sources through having a single multi-output transformer with each connected to an energy source. The main focus in the source-integration process is enhancing the system utilization and hence improve the converter network power density.

Maximizing the power conversion efficiency of the DC/DC network is crucial in the MEA structure. Different control techniques can be applied to such converters for enhanced efficiency across a wide operating range [12, 13]. Multi-objective optimization is required for improved efficiency and dynamic system response [14]. With the aim of enhancing the efficiency and performance, accurate knowledge of the system's stray elements becomes of paramount importance. The high conversion ratio required for such converters introduces new issues regarding the isolating transformer design and circuit parasitic control. The converter operation deviate away from ideal

mathematical models based on the value of the stray elements and hence has to be considered in the optimization design process of the converter.

In this thesis, a novel transformer design methodology is presented to optimize the transformer core size, switching frequency, and converter performance. The stray capacitance of the high-ratio transformers is discussed and modelling techniques are developed for various winding structures. The effect of the different winding configuration on the transformer losses and converter performance is discussed. A new winding configuration is proposed to enhance the converter performance through lowering the stray capacitance of the transformer layers. A 20% improvement in the transformer power density was achieved as compared to conventional configurations in literature aimed to lower the stray capacitance to improve the converter performance.

This rest of the thesis focuses on the development of a multi-source DAB (MS-DAB) DC/DC converter that allows for different energy sources integration while enhancing the overall system efficiency and stability. The converter network utilization is improved considering the different operating modes of the proposed converter topology. The mathematical model of the proposed topology is derived and the different operating modes are discussed. The effects on the system size and power flow control between the different energy sources through the proposed topology are highlighted. A two-layer optimization process is developed for the proposed converter to select converter parameters and generate a look-up-table (LUT) of the optimized control variables. A 4 kW prototype is developed and validated experimentally for the standard operating range set by industry regulatory standards.

1.2 Objectives and Contributions

The thesis objective is to provide design guidelines and optimization algorithms for DC/DC converters utilized in modern MEA architectures through novel technical advances regarding the converter topology and transformer design optimization. The thesis contributions are summarized below.

- A comprehensive review of MEA architectures and their regulatory standards as well as the potential DC/DC converter topologies considered for aircraft distribution networks. Future trends in DC/DC topologies to accommodate the HV distribution network and the increase of electrical energy storage elements in the MEA structures are discussed. Published in [15].

- A review of the basic magnetic elements utilized in DC/DC converters with a focus on the magnetic material and high-frequency transformer configurations. Discussion on the impact of the magnetic parasitic element effect on the converter performance.

- An integrated design algorithm for the MEA transformer to optimize the power density and system performance. A core-selection algorithm considering the converter switch loss analysis is presented. A novel transformer winding configuration is proposed to minimize the winding capacitance and improve the converter performance. Published in [16, 17].

- Development and experimental validation of an integrated multi-source DC/DC topology for energy sources integration. Submitted to IEEE Open Journal of Power Electronics.

- Comprehensive design analysis and converter optimization based on a Fourier transform modeling approach and including the system stray inductances in the process. Accepted in IECON 2022 conference.
- Two-layer GA-based optimization process for the developed multi-source topology.

1.3 Thesis Outline

The thesis is organized into seven chapters.

Chapter 1 discussed the motivation for the development of multi-source DC/DC structures for more electric aircraft. The research objectives and main contributions have been highlighted.

Chapter 2 presents the fundamentals of DC/DC converters utilized in the aerospace industry. The basic distribution network structures for modernized aircraft are reviewed. A review of the basic topologies and their derivatives to meet the MEA requirements is conducted. The need for converters integration into more compact solutions is highlighted considering the distribution network on a system-level.

Chapter 3 reviews the basic magnetic components in DC/DC converters in the MEA architecture. A comprehensive comparison is performed between ferrite and nanocrystalline materials including the potential advantages of nanocrystalline cores and their drawbacks in industry. The basic elements of Electromagnetic interference (EMI) filters and standard test setups for EMI tests are discussed. Several transformer configurations are compared including the trade-offs for each between the losses and parasitic elements. The effect of the transformer parasitic elements on the converter performance is highlighted.

Chapter 4 introduces a design methodology for the isolating transformer utilized in the DC/DC converter unit. The optimization process is split into transformer core optimization and winding configuration optimization. An integrated algorithm is developed to combine the converter loss analysis and the transformer core selection. Two new winding configurations are proposed to minimize the transformer capacitance and improve the converter performance. FEA simulations are performed to compare the proposed configurations against conventional structures. Three different transformer configurations are implemented and experimental results are compared to the analytical analysis.

Chapter 5 presents the proposed multi-source DAB topology. The different modes of operations are discussed. The realization of modular power electronic cells (MPECs) architecture through the proposed multi-source topology is discussed. The effect on the system stability and utilization is highlighted as compared to conventional solutions.

Chapter 6 introduces the developed mathematical model for the proposed MSDAB topology through Fourier transform of converter the key waveforms. The effect of the system parasitics is included in the analysis. A two-layers optimization algorithm based on genetic algorithm is presented to optimally select the converter parameters in different operating modes. The converter range mandated by industry regulatory standards for the MEA DC/DC converter is considered in the optimization process. The optimization process considers triple phase shift control technique for the two main operating modes of the proposed converter. A 4 kW prototype is implemented to validate the MSDAB topology. The different operating modes are tested at rated power and efficiency plots of each mode are presented.

Chapter 7 is dedicated to conclusions and future work.

Chapter 2

Topological Evaluation of Isolated DC/DC Converters in MEA Applications

2.1 Introduction

This chapter focuses on linking the aircraft architecture and its effects on DC/DC converters implementation. Different aircraft architectures are discussed highlighting the trend towards more electric distribution systems. A review of the standards mandating the design of such converters is conducted for MEA DC/DC converters. The basic converter topologies considered for the MEA applications in literature are presented. Derivatives of the basic DC/DC topologies to meet the MEA requirements are discussed. Different control schemes of the DAB configuration are discussed highlighting the effect on the converter efficiency across the full operating range.

2.1.1 Challenges in MEA electrical power distribution systems

Aboard a traditional aircraft, such as the Airbus A320 and the Boeing B767, two main engines and an auxiliary power unit (APU), provide an AC bus voltage 115 VAC. A conversion stage is then required to supply the 28 Vdc power network required for the conventional electrical loads aboard the aircraft. On the other hand, on a more-electric aircraft, the main engines/generators generate either a 115 VAC or a 230 VAC bus voltages. Two DC link voltages of either +/- 135 V or +/- 270 V can be generated from a 115 VAC or the 230 VAC, respectively, through a power conversion unit. A +/- 135 Vdc is utilized aboard the airbus A380 to generate the standard 270 Vdc bus link. A +/- 270 Vdc bus such as that adopted on the Boeing 787 provides the standard 540 V also known as the high voltage dc (HVDC) link of new electric networks in the aircraft. Similar to the conventional aircraft, a conversion stage is required to supply the 28 Vdc bus from the HVDC link [18]. Both the A380 and B787 are examples of a more electric large civil aircraft. Fig. 2.1 shows the trend

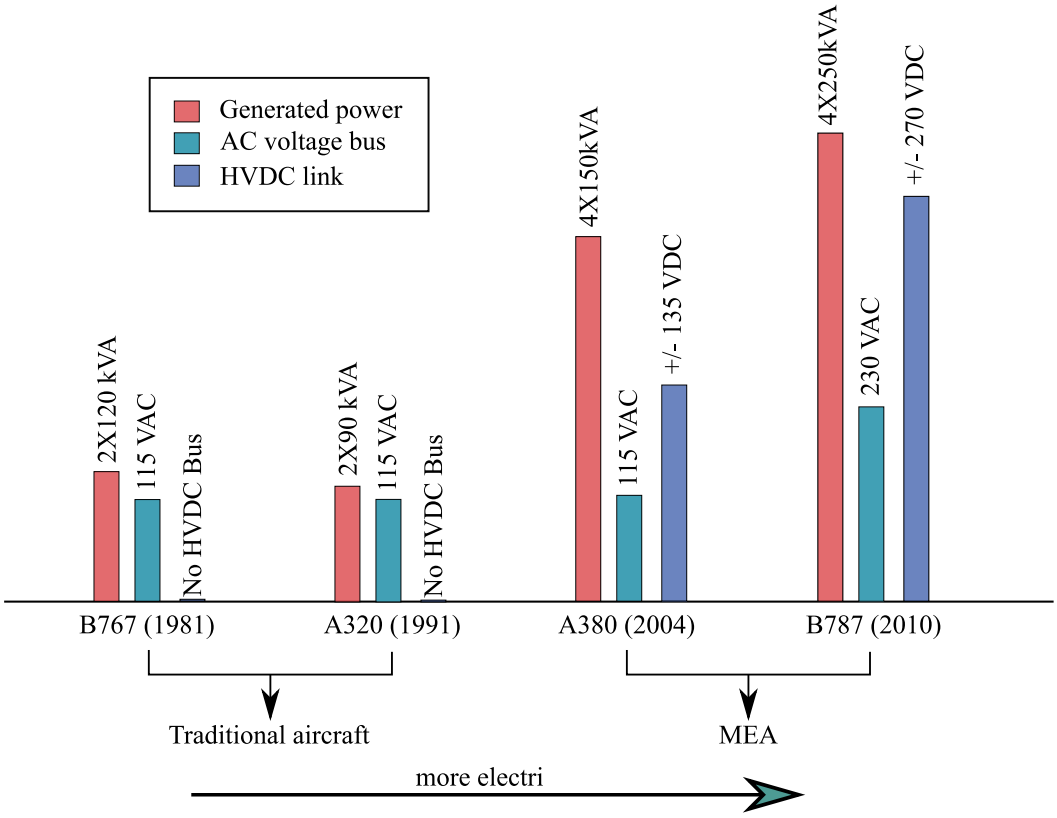

Figure 2.1: Comparison between conventional and MEA distribution system specifications.

of the increase in the generated power towards a more-electric architectures. With the increase of electrical power demand, higher voltage buses are utilized to control the power losses in the distribution systems [19–21]. Power electronic components are considered the main building block of the emerged electrical power distribution systems of MEA [22, 23]. The movement towards a more-electric aircraft is dependant on the technology advancement of electronic systems utilized in the MEA EPDSs [24]. With the increase of the electrical power and the movement towards high voltages, the specifications of the power electronics components utilized in the conversion stages distributed along the electrical network on the aircraft become more challenging. As

can be seen from Fig. 2.1, there is a trend towards pushing for HV system architectures which introduces new challenges to the DC/DC converters utilized to link these HV buses to the LV 28 Vdc network required for the newly utilized electrical loads aboard the aircraft. These challenges include the requirement of a high step down DC/DC converters which increase the design complexity of the isolating transformers usually utilized in these converters. The stray elements effect is also amplified when a high transformer ratio is used. Pushing the DC link voltage also limits the selection of semiconductor devices as well as the converter topology to reduce the voltage stress across the utilized switching devices. The increase in power demand also introduces a challenge regarding the design complexity of high current DC/DC converters. This includes the PCB design, thermal management systems and magnetic elements design. Increasing the electrical power demand is also associated with adding more energy storage systems [25–30]. Moreover, the conventional kerosene-based APU systems are being replaced with ESS such as batteries and fuel cells [31–33]. Converters integration to accommodate the added ESSs becomes of paramount importance to increase the power density and system utilization in the distribution network.

2.1.2 Conventional architectures vs parallel cells architecture

The basic electrical power distribution network aboard a MEA is illustrated in Fig. 2.2. Fig. 2.2 shows the HVDC distribution network for the MEA supplied through two main engines and a kerosene-based auxiliary power unit (KB-APU) and having solid state power controllers (SSPCs) between the different buses for protection. The basic architecture shown considers a symmetrical electrical distribution system for the left and right side of the aircraft. The main propulsion system of the modernized

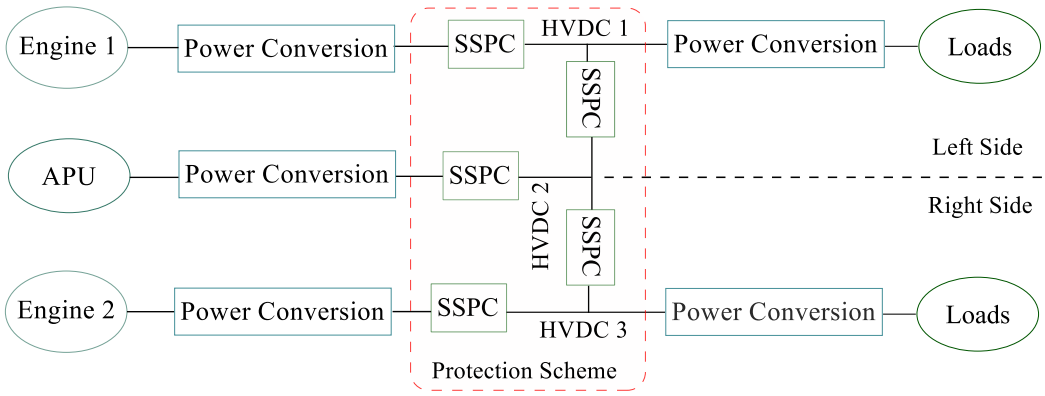

Figure 2.2: MEA electrical distribution system architecture.

MEA such as the A380 and B787 rely entirely on the two main engines. However as a step towards electrifying the traditional architectures, the hydraulic and pneumatic systems in the MEA architecture are swapped with electrical alternatives. Fig. 2.3 shows a detailed example of the MEA architecture. The main engines and the APU unit are connected to a rectifier unit which provides the HVDC bus. The different HVDC links are connected via SSPCs as shown in the basic architecture illustrated in Fig. 2.2. The HVDC loads are directly connected to the main HVDC bus. DC/AC inverters are used to connect the AC loads to the main bus. DC/DC converters are utilized to link the HVDC bus to the LV distribution network used to supply the avionic systems, entertainment systems, and flight control systems. The next step of electrification is moving towards electric propulsion systems. The series hybrid system architecture is shown in Fig. 2.4. The main engine along with the electrical ESS which is either a fuel cell or a battery are connected to the main HVDC bus [34, 35]. DC/AC inverter drives are then used to supply a constant speed motor (CSM) which

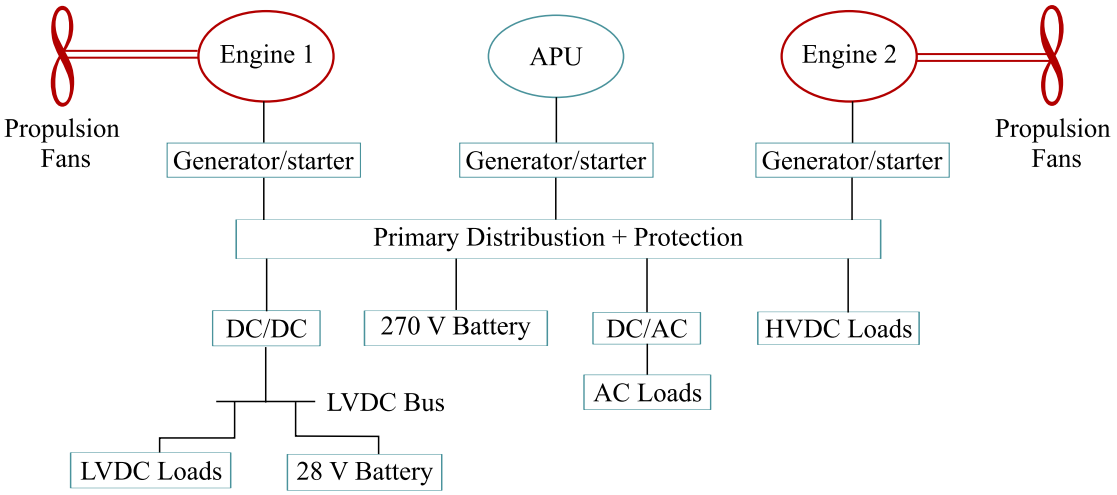

Figure 2.3: MEA electrical power distribution network

is coupled to the propulsion fans as shown in Fig. 2.4. The same requirement of the DC and AC loads as the MEA are present for this architecture and hence power electronics converters are utilized as well. The last step of electrification is the all

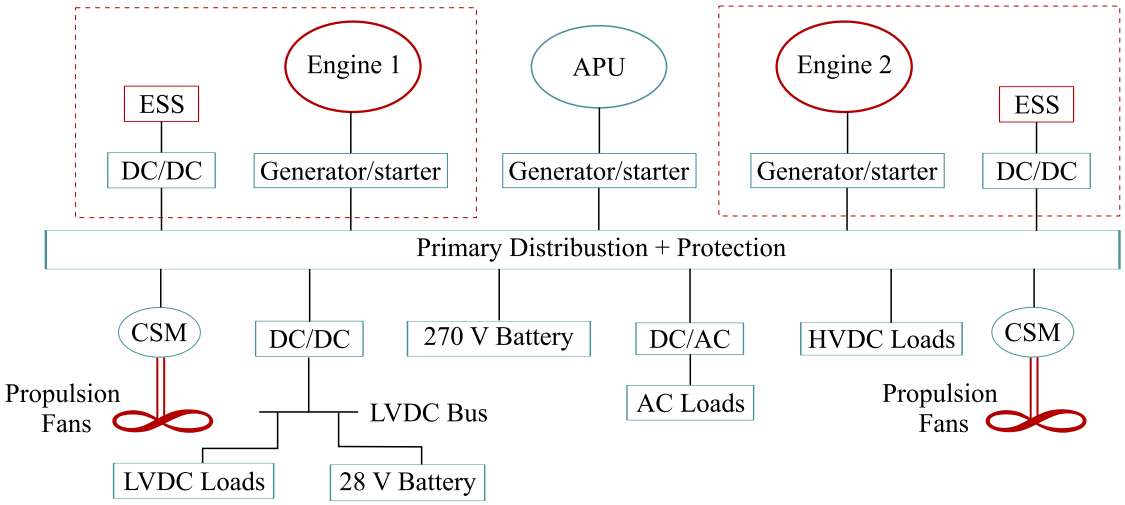

Figure 2.4: Electrical propulsion - hybrid series architecture.

electric aircraft (AEA) propulsion system. In all electric aircraft the main engines are replaced by electrical ESSs [36]. The ESS is either connected directly to the HV

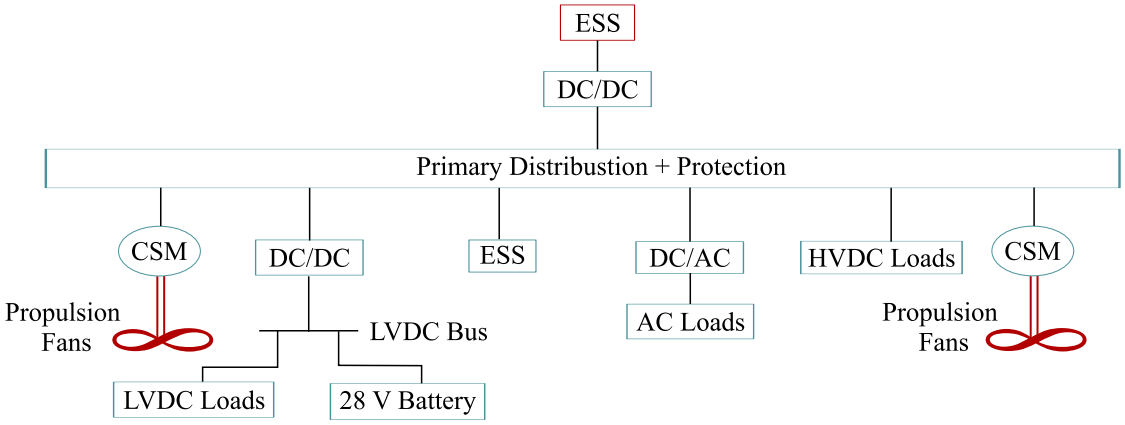

Figure 2.5: Electrical propulsion - all electric architecture.

bus or a DC/DC converter is used to step up the ESS voltage to the required main HVDC link voltage. Similar to the series hybrid architecture, AC/DC inverters are utilized to drive the CSMs connected to the propulsion fans. Similar power electronics network as the MEA and series hybrid architectures is required to supply the AC and DC loads aboard the aircraft.

From the 270 V or the 540 V HVDC bus in all the above architectures, the 28 V DC bus is generated, also known as low voltage direct current (LVDC) bus. The LVDC bus supplies the electric loads in avionic systems. In a MEA or electric propulsion aircraft, these converters are used to step down the dc bus voltage to the voltage required for other LV loads. In most cases, the voltage range requires a high transformer turn-ratio to achieve the required high conversion ratio [37]. Therefore, a high-frequency transformer is often used to provide galvanic isolation between the high and low voltage sides. In recent years, design of highly efficient and power dense isolated DC/DC converters have been gaining a lot of attention in the industry. One of the most important contributing factors to the efficiency and power density is the

transformer design. The transformer must be designed to ensure low weight and volume while optimizing efficiency. A compact and highly efficient transformer is crucial in the design of a power-dense high-performance converter. Other derivative architectures have been derived from the basic MEA and all electric aircraft to improve the system utilization of the power electronic converters used to link the HVDC bus to the LVDC bus. The topology configuration of the DC/DC converter unit is dependant on the system architecture of how the converters are connected on a system level. The configuration is also dictated by the auxiliary ESS in the system and their connection to the main HVDC and LVDC buses. Among the derivatives is the modular power electronic cells architecture which utilizes lower power electronic cells in parallel to meet the power demand by the LV network. The MPECs architecture is shown in Fig. 2.6. Several low-power converter cells are utilized each with access to all three main bus links. The architectre adds flexibility to the distribution network and prevents oversizing the DC/DC converter network [38]. A main supervisor linked to the cells network is utilized to control the power sharing between all DC links. The converter configuration, topology, switching devices, magnetic components are entirely relying on the system architecture. For example, the switching devices technology utilized in such converters in a 270 Vdc bus system could be different than that of a 540 V system. The design challenges of a low-power module are also limited as compared to a single converter system. The integration between the power cells could be carried out through multi-port and multi-source converter topologies. In the following, the standards considered for the DC/DC converters aboard the MEA, which is the latest architecture utilized in modern civil aircraft, are reviewed and design guidelines are provided. The topologies that are often considered for DC/DC

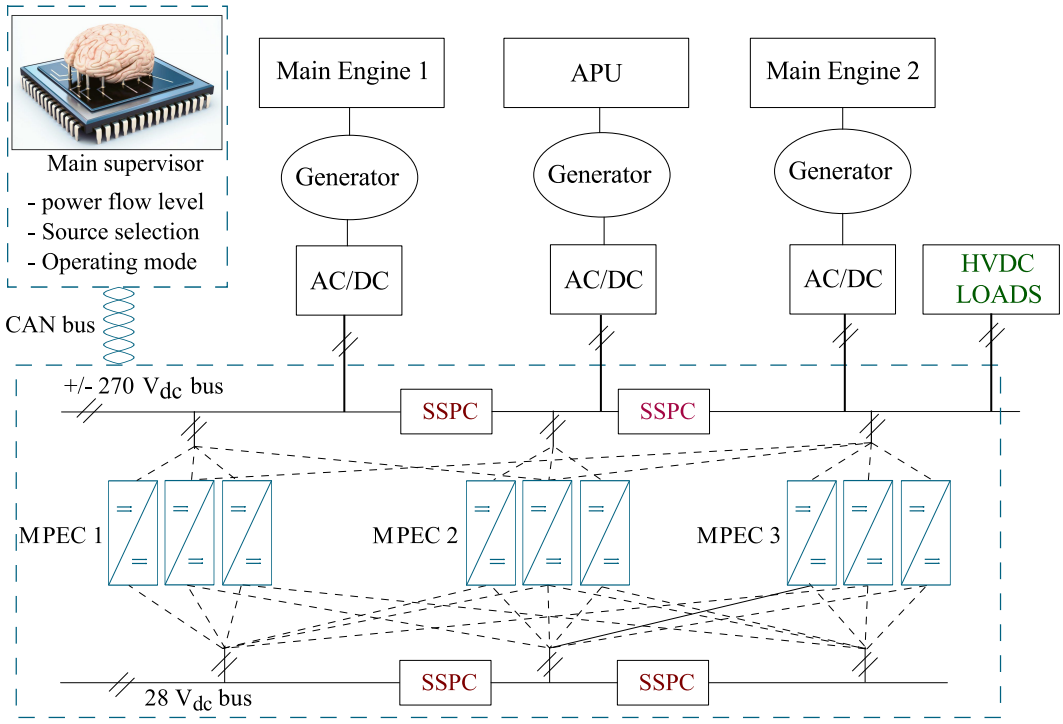

Figure 2.6: Modular power electronic cells architecture.

converters in the MEA architectures are compared and analyzed. Considering that there is a trend towards pushing for higher voltage systems, multilevel derivatives of the basic topologies are reviewed. Series connection and parallel connections of the reviewed topologies to accommodate higher voltage and power levels are discussed. Multi-port configurations in literature considered to realize the MPEC architecture are listed.

2.2 Isolated DC/DC Converters in MEA Applications

2.2.1 Standards and design guidelines

The acceptable regulatory procedure for aircraft power electronic components has been discussed in [22]. Among the set of regulatory standards that govern the hardware testing procedure of the electric power system in the aerospace industry is the DO-160G. The DO-160G governs the environmental conditions for airborne equipment. The DO-160G document lists the set of tests associated with conditions such as temperature effects on the electrical systems as well as humidity tests, vibration scenarios and water proofness tests. Electrical performance tests such as whether the equipment can withstand the effect of voltage spikes as well as emissions and EMI susceptibility tests are listed in the DO-160G. The conducted and radiated emission limits are also illustrated in the DO-160G. Some other electric power requirements and operating limits are listed in the MIL-STD-704F standard. The standards defines the electrical system limits and electrical testing procedure. The MIL-STD-704F standard defines the LVDC network limits between 24 Vdc and 29Vdc with a nominal voltage of 28 Vdc. The HVDC limits are also defined between 260 Vdc to 280 Vdc with a nominal voltage level of 270 Vdc. The DC/DC converter design should ensure operation under these voltage limits. The thermal management system as well as the electrical system ratings shall be based on the worst case operating condition governed by the limits under the MIL-STD-704F standard. The design of the DC/DC converters connected to the APU or auxiliary ESSs utilized during an emergency operation shall be designed in accordance to the emergency operating requirements

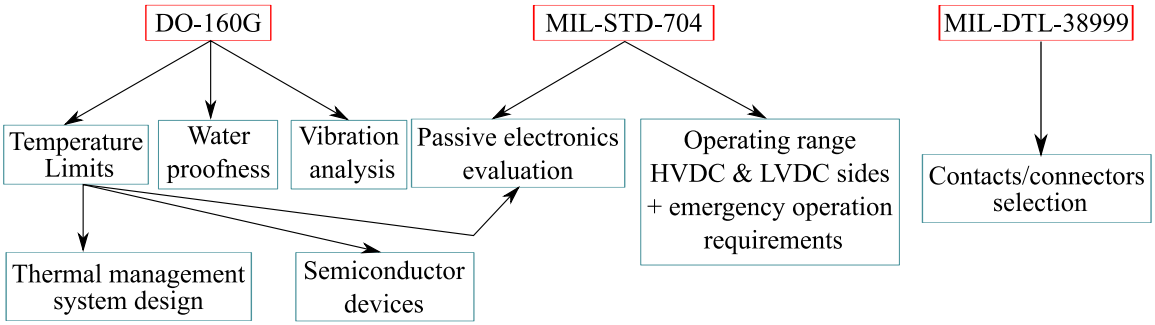

Figure 2.7: MEA standards and design guidelines.

listed in the MIL-STD-704F standard. The contacts/connectors selection based on the stress and sealing requirements is dictated by the MIL-DTL-38999 M. Fig. 2.7 illustrates the linking between the different design aspects of the DC/DC converters to the two regulatory standards.

2.2.2 Converter topology

The isolated converter topology could either provide a unidirectional or bidirectional operation. Since some of the DC/DC converters utilized in the MEA architecture are connected to a 28 Vdc auxiliary battery at the output side and either the HVDC link or a HV battery on the input side, a bidirectional operation is required. The DC/DC converter could be unidirectional if the input side is connected to a fuel cell. The DC/DC converters can further be categorized based on the control technique applied: duty-cycle controlled, phase-shift control or frequency controlled. Some topologies offer lower switching devices losses allowing for pushing the switching frequency and reducing the magnetics size as well as the heatsink size. Hard switching is referred to when there is an overlap between the switch voltage and current waveforms. One solution to reduce the switching device loss is to eliminate the overlap transition period

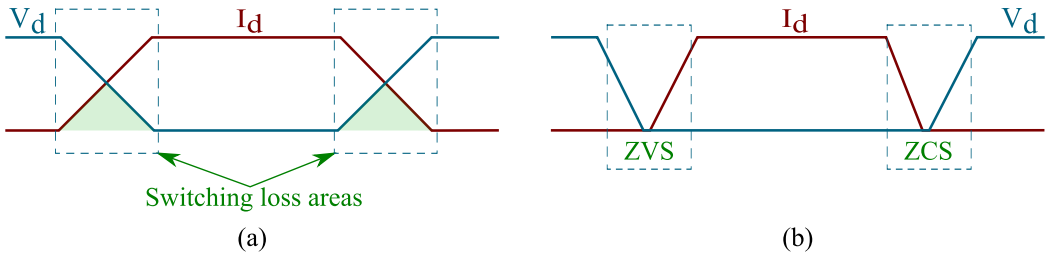

Figure 2.8: Switching losses of power semiconductor devices. (a) hard switching. (b) soft switching

between the switching intervals. The process is known as soft switching where the voltage across the device goes to zero before it being turned on, known as zero-voltage switching (ZVS), or having the current going to zero before turning the device off, known as zero-current switching (ZCS). Fig. 2.8 (a) shows the device waveform when being hard switched while Fig. 2.8 (b) illustrates the soft switching action (ZVS and ZCS). When the device turns on, the voltage goes down while having the current going up creating an overlap area causing the turn-on switching losses and same while the device is being turned off causing the turn-off switching losses. The turn-on switching losses are eliminated in case of ZVS while the turn-off are eliminated for the ZCS case. The ZVS/ZCS action is achievable for phase-shifted topologies such as the full-bridge push pull converter, dual active bridge converter and resonant converter such as LLC and CLLC converters. The full bridge converter is one of the isolated unidirectional duty-cycle controlled topologies suitable for high-gain high-power applications such as the MEA DC/DC converters. Other unidirectional DC/DC converters can be considered as well such as the Full-bridge push pull (FBPP) converter which is modulated using phase shift control and the resonant LLC converter which is a frequency control topology.

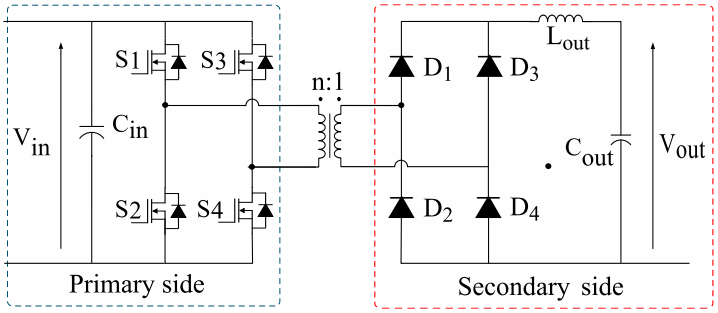

Figure 2.9: Full-bridge converter schematic.

Full-bridge (FB) converter

The FB converter topology is shown in Fig. 2.9. The topology consists of an active bridge on the primary side of an isolating transformer and a secondary passive diode rectifiers. The converter is controlled by modulating the duty cycle of the primary switch. The diagonal switches S_1 and S_4 are modulated with the same gate signal. Similarly, the complementary gate signal is fed to both S_2 and S_3. Volt-seconds balance of the transformer is achieved by limiting the primary bridge duty cycle to 50%. The FB converter operates only in buck mode with the output limited to DNV_{in}. Where D is the primary duty cycle, N is the transformer turns ratio, and V_{in} is the input voltage. An additional boosting stage is required to cover the full input and output voltage range mandated by the MIL-STD-704F [39]. Fig. 2.10 shows the FB converter with an additional boost converter stage added at the input side of the converter. The total boost FB converter gain is shown in Eq. 2.2.1, which allows the converter to operate in boost mode to cover the full input and output range.

$$V_{out} = \frac{DNV_{in}}{1 - D_1}. \tag{2.2.1}$$

Where D_1 is duty cycle of the added boost converter stage.

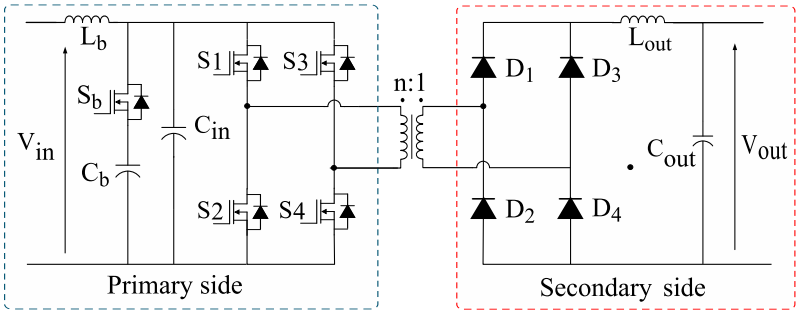

Figure 2.10: Full-bridge converter schematic with an additional boost stage.

One of the main challenges of the DC/DC converters in the MEA architecture is the high current on the secondary side since the power demand is high and the output voltage level is 28 Vdc. The efficiency of the conventional FB converter is low considering using a passive rectifying diodes with high voltage drop on the secondary high current side. Only unidirectional operation is achieved with the passive rectifier configuration. Another variation of the conventional FB converter is achieved by replacing the secondary side diodes with active switches to reduce the conduction losses on the high current side. Bidirectional operation is also possible when a synchronous rectifier utilizing metal-oxide-semiconductor field-effect transistors (MOSFETs) are used on the secondary side instead of the passive diodes.

Full-bridge push pull (FBPP) converter

The FBPP is widely used in applications where a high gain conversion is required. The FBPP converter schematic is shown in Fig. 2.11. Similar to the FB converter, all switching devices on the primary side operates at a fixed 50% duty cycle. However, both primary legs are phase shifted to modulated the duty cycle of the primary voltage waveform. The topology allows for ZVS operation resulting in reduction in the devices

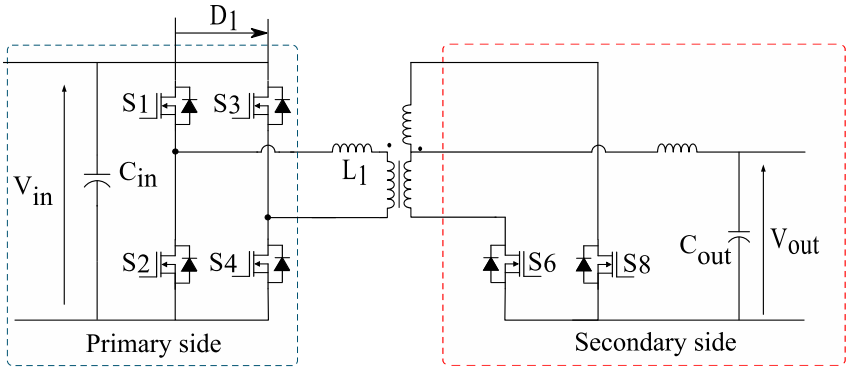

Figure 2.11: full-bridge push pull converter schematic.

switching losses. The FBPP topology could be implemented with a passive rectifier on the secondary side which only allows a unidirectional operation. However, since the current in the MEA application is high on the secondary side, a synchronous rectifier is preferred for high efficiency operation. The voltage transfer ratio of the FBPP converter can be derived as shown in Eq. 2.2.2.

$$V_{out} = 2DNV_{in}. \tag{2.2.2}$$

Where D is transformer primary duty cycle.

Limited research for the bidirectional FBPP topology has been carried out in literature for the MEA application [40–42].

Dual active bridge (DAB) converter

The DAB converter is often the topology considered for DC/DC converters aboard the more electric aircraft due to its control simplicity and high efficiency [43–48]. The schematic of the DAB converter is shown in Fig. 2.12. The topology consists of two full bridges across an isolating transformer and an external inductor inserted

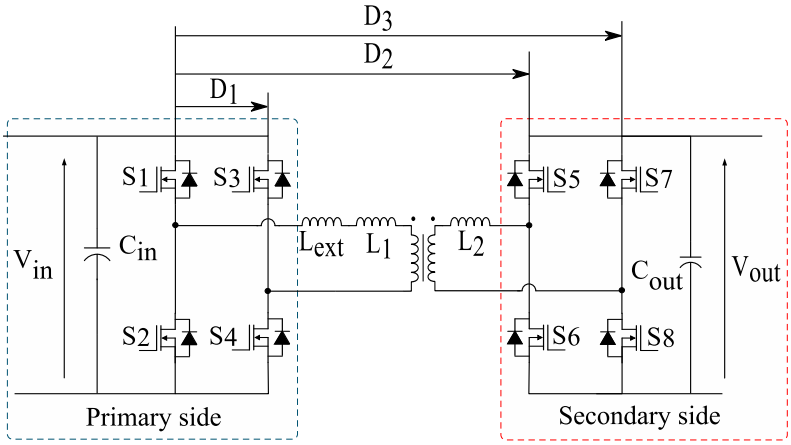

Figure 2.12: Dual active bridge converter schematic.

in-between. The transformer design can be carried out to have a leakage inductance equal to the required external inductor for the converter operation. In such cases, the external inductor is eliminated, and the operation relies on the leakage of the transformer. The added inductor along with phase shifting the two bridges causes current to flow when the devices are turned off. This current flows to discharge the output capacitance of the power devices and forward bias the device body Diode. This process occurs during the deadtime causing the devices to turn on while the diode is conducting allowing for ZVS and eliminating the turn on losses of the device. There are several modulation techniques discussed in the literature for the DAB converter [49–51]. These modulation schemes are based on phase shifting the gating signals between the four full-bridge legs. The simplest technique is the single phase shift (SPS) where the gating signals of the secondary bridge are phase-shifted with respect to the primary side. Triple phase shift (TPS) modulation is a generalized scheme where there are three degrees of freedom. The first primary leg acts as a master as shown in Fig. 2.12 where three phase legs are phase-shifted with respect to the first primary phase leg as D_1, D_2, and D_3. The converter gain is dependant on

the modulated phase shift based on the control technique applied. The high efficiency across a Wide voltage range of operation makes the DAB converter suitable for the MEA DC/DC converter [52].

LLC resonant converter

The LLC converter discussed in [53–55] is considered in wide-range DC/DC converter applications due to its high efficiency at different load conditions. The LLC converter is often considered for a high input voltage where a high conversion ratio is required to get a low output voltage. The LLC-DAB converter, shown in Fig. 2.13, has the same circuit configuration as the DAB converter with an additional resonant capacitor on the primary side of the transformer. The external inductor and capacitor added to the primary side form a resonant tank. The converter gain is controlled by varying the switching frequency and hence controlled the gain of the resonant tank. The LLC-DAB converter is a frequency-modulated converter which adds more design complexity compared to the DAB converter. The LLC converter is designed to operate at, or in the vicinity of the switching frequency to ensure operating in the inductive region, where ZVS is achievable. The resonant components selection is crucial during the design process to determine the operating frequency range to get the required gain and to ensure operation in the inductive region. To simplify the converter analysis, an assumption is made that at or in the vicinity of the resonant frequency, the current flowing through the series resonant tank is sinusoidal. The overall converter gain is the resonant tank gain multiplied by the turns ratio. Some variables are defined in literature and used in the design process of the LLC converter as follows:

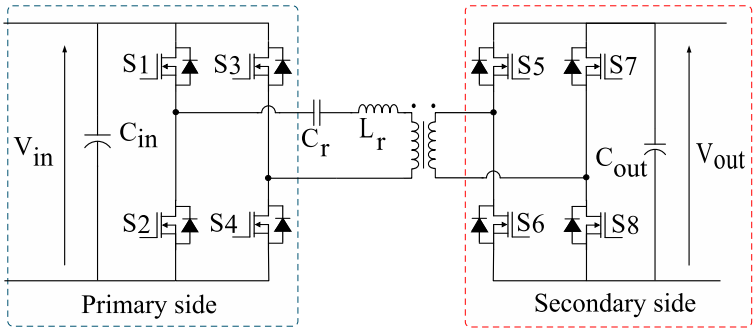

Figure 2.13: LLC series resonant converter schematic.

$$\begin{aligned} f_n &= \frac{f_{sw}}{f_0} \\ L_n &= \frac{L_m}{L_r} \\ Q_e &= \frac{\sqrt{L_r/C_r}}{R_e} \end{aligned} \tag{2.2.3}$$

Where f_n is the normalized frequency, f_{sw}, is the switching frequency, f_o is the resonance frequency of the added tank, L_n is the inductance ratio, L_m is the magnetizing inductance, L_r is the external resonant inductor, Q_e is the quality factor, and R_e is the reflected output resistance to the primary side.

Using the simplified circuit of the LLC topology, the resonant tank gain of the converter can be found as in Eq. 2.2.4 [56].

$$M_g = \frac{v_{primary}}{v_{bridge}} = \text{Mag}\left(\frac{(jX_{Lm} \| R_e)}{(jX_{Lm} \| R_e) + j\left(X_{Lr} - X_{Cr}\right)}\right). \tag{2.2.4}$$

The main goal of the LLC design process is to select the inductance ratio L_n and the quality factor Q_e based on the required converter operating range. The resonant tank components values are then selected based on Eq. 2.2.3.

The LLC converter is considered for the MEA application due to the high efficiency

across a wide range of operation [53, 57–59]. Since high-efficincy operation is required for the MEA converter and considering the high current on the secondary side, synchronous rectification is required for the secondary side. Different synchronization methods between the primary and secondary devices are discussed in [60, 61]. Often in the DC/DC MEA converter, several converter modules are paralleled to achieve the required power level. Modules synchronization and equal current sharing has to be considered for optimal system efficiency. For the LLC converter, the synchronization scheme and converter paralleling is challenging since the topology is frequency modulated, some synchronization mechanisms are discussed in [62, 63] for the LLC topology.

Multilevel converter topologies

Considering the movement towards higher voltages for MEA architectures, multilevel-based DC/DC topologies can potentially be utilized in such HV architectures. Multilevel converters are found in medium voltage applications due to the low-voltage stress for the switching devices utilized in these topologies [64,65]. Multilevel topologies offer better EMI immunity as well as reduced harmonic distortion due to the multi-level nature of the converter waveform. However, this comes at the cost of adding extra switching devices, gate drivers and complex design and control methods. The DC/DC multilevel topologies are based on the basic traditional two-level topologies such as the FB, DAB and LLC converters. The multilevel structure can be used for the HV bridge, the FB structure can still be used for the secondary 28 Vdc side. The most common structures for multilevel bridges are the cascaded H-bridge (CHB) [66], flying capacitor structure (FC) [67,68], neutral point clamped (NPC) and

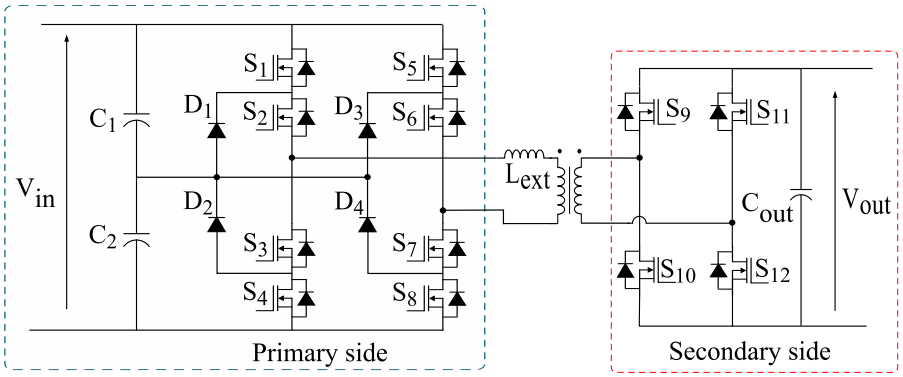

Figure 2.14: Neutral-point-clamped dual active bridge converter schematic.

active neutral point clamped (ANPC) [69, 70]. The FC, NPC and ANPC structures offer lower voltage stress across the switching devices as compared to the CHB [71]. The capacitor size of the FC is higher than the NPC and ANPC which results in lower power density for the FC based topology [15]. The most common multilevel DC/DC converter structures in literature are based on the DAB converter. The NPC-DAB and ANPC-DAB converters have been discussed an analyzed in [15, 72–74] for aerospace and automotive applications. The converter control is based on phase shift control between the primary NPC/ANPC structure and the secondary conventional full bridge synchronous rectifier. The schematic of the multilevel NPC-DAB converter is shown in Fig. 2.15. The ANPC-DAB structure is the same as the ANPC-DAB but with replacing the neutral clamped diodes on the primary side by active switches. The key waveforms of the multilevel NPC/DAB converter are shown in Fig. 2.15 [75]. Five voltage levels are generated on the transformer primary voltage waveform. Each NPC leg on the primary side generates three levels ($V_{in}/2$, 0, and $-V_{in}/2$). There are three control variables for the NPC/DAB topology, α, β, and ϕ. The phase angle between the primary and secondary side (ϕ) is modulated similar to the conventional DAB converter. Moreover, α and β are modulated to control the duty cycle of the

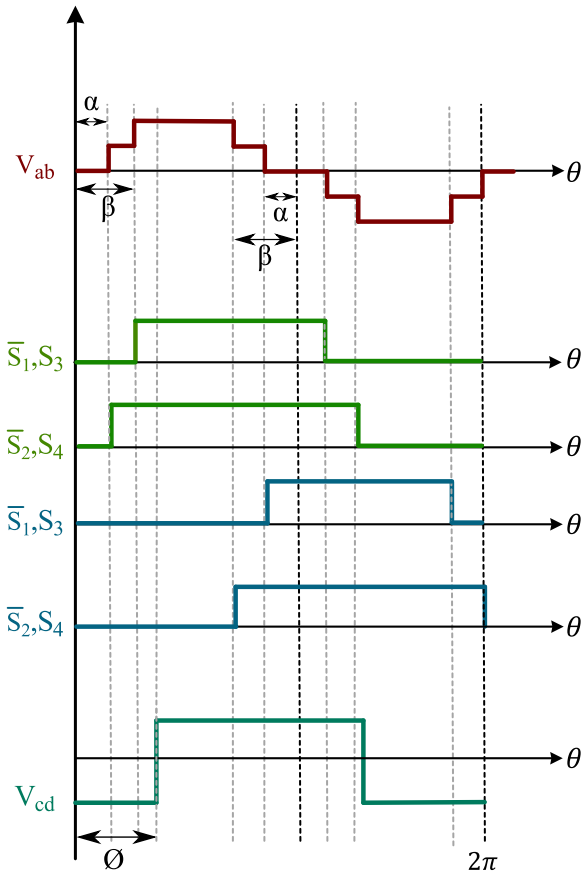

Figure 2.15: Key switching waveforms of the NPC-DAB converter.

multilevel primary bridge output (V_{br1}) as shown in Fig. 2.15.

2.3 Multiple Input/Output Converter Configurations

The MEA architecture relies on the reliability and modularity of the power electronic components utilized in the distribution network. The discussed DC/DC converter topologies can be configured to offer benefits such as higher voltage or current operation. This is achieved by having a modular structure for the DC/DC converter where several identical converter modules can be connected either in series to increase

the voltage handling capability or in parallel to handle higher currents. The main key goals of the modularity approach is to increase the system reliability, integration and efficiency. The modular approach is based on having a lower power unit that can be connected either in series or parallel to improve the converter performance. One example of this is the MPECs MEA architecture, where several low power cells are connected in parallel instead of a single high power unit. The MPECs system provides improved safety and low power capability as compared to a conventional architecture. Weight and volume reduction is also achieved by using low power units in parallel. The converter efficiency is also improved since at each power level a high-level supervisor control how many parallel units should operate for optimized performance. Other configurations can also be implemented by using lower power units in series/parallel.

The main multi-cells configurations are shown in Fig. 2.16. Fig. 2.16 (a) shows the input-parallel-output-parallel (IPOP) structure where several low power cells can be implemented and connected in parallel at the input side as well as the output side [76,77]. This structure is the same as the MPECs paralleled cells. The current at the input side and output side is reduced by the number of modules. Since the voltage at the secondary side is 28 Vdc, the DC/DC converter of MEAs linking the HVDC bus to the LVDC link exhibit high secondary current which becomes a challenge in the PCB design, magnetics and filter design. Another configuration is the input-series-output-parallel (ISOP), shown in Fig. 2.16 (b), where the low-power modules are connected in series at the input side and parallel on the output side [78, 79]. This configuration is beneficial in terms of reducing the voltage stress across the primary devices and the current stress on the secondary. This approach could be

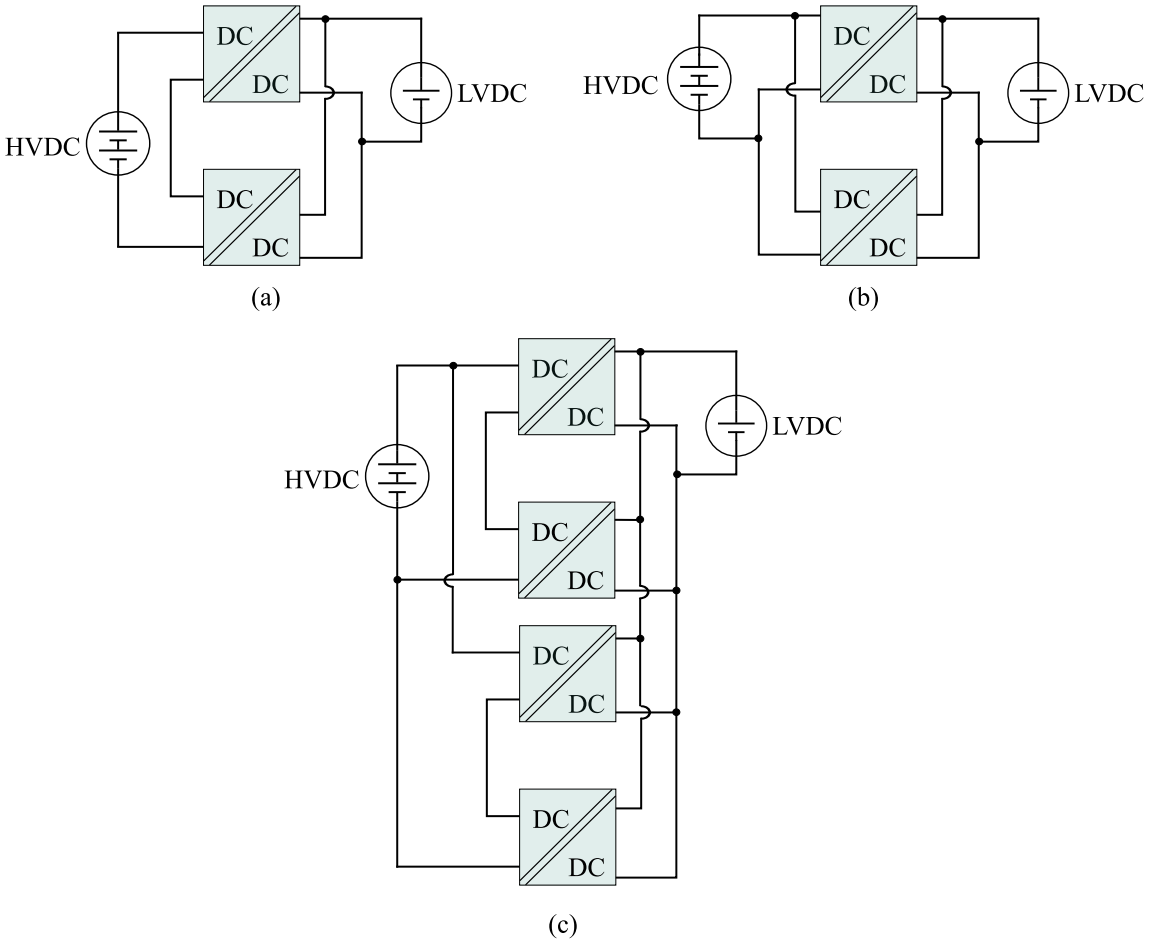

Figure 2.16: Multi-port DC/DC configurations. (a) ISOP (b) IPOP (c) Hybrid ISOP/IPOP

considered for HV input converters instead of multilevel structures. [15] provides a detailed comparison between the ISOP-DAB, NPC-DAB, and ANPC-DAB for a HV MEA application. Fig. 2.16 (c) shows a hybrid combination between the ISOP and IPOP structures where two converters could be connected in an ISOP configuration and combined with an identical combination as an IPOP structure. In conclusion each of the multiple input/output configuration has its advantages and the selection of the converter configuration is dependant on the voltage level, required power and

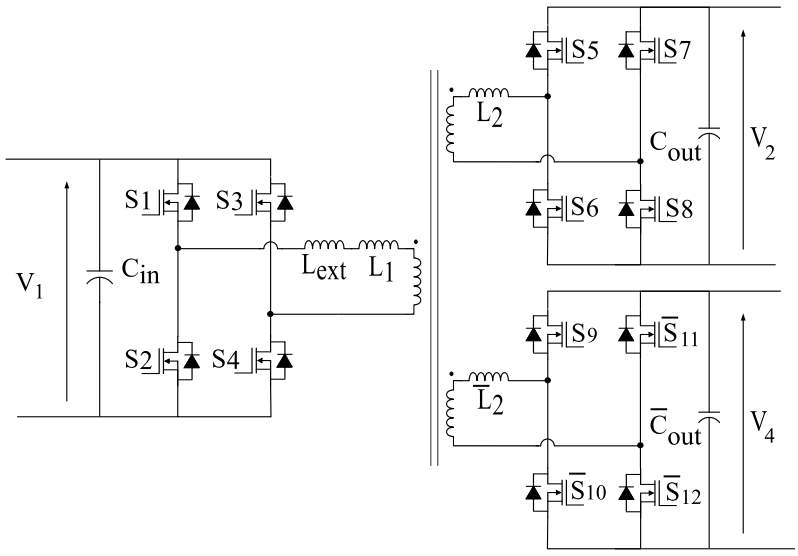

Figure 2.17: Three-ports magnetically coupled DAB converter.

the efficiency analysis of each structure for a specific application.

2.4 Multi-port Converter Configurations

Several multiport and multi-source structures have been derived from the basic topologies for the MEA application [80–82]. With the increase of the electrical voltage buses and ESSs in the MEA architectures, sources integration becomes of a paramount importance. A three-port magnetically coupled bidirectional converter has been proposed in [83]. The three-port converter, shown in Fig. 2.17., controls the power flow between the different HVDC networks in MEAs. A combination of a droop control and phase shift modulation was proposed to control the power transfer between the three sources in [83]. Another three-port converter integrating three energy sources has been proposed and discussed in [11, 84]. The integrated three-port converter schematic is shown in Fig. 2.18. One port is connected to the HVDC bus, two ports

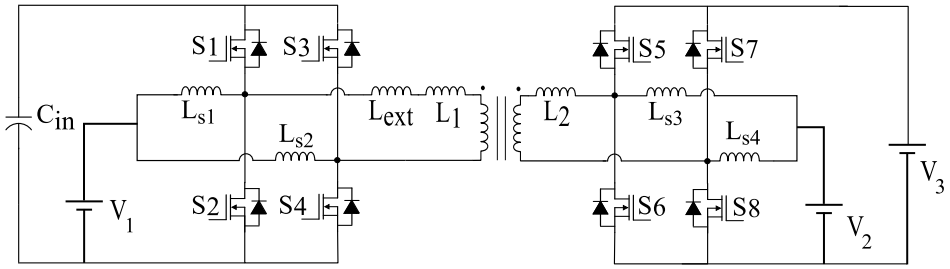

Figure 2.18: Integrated Three-ports DAB converter.

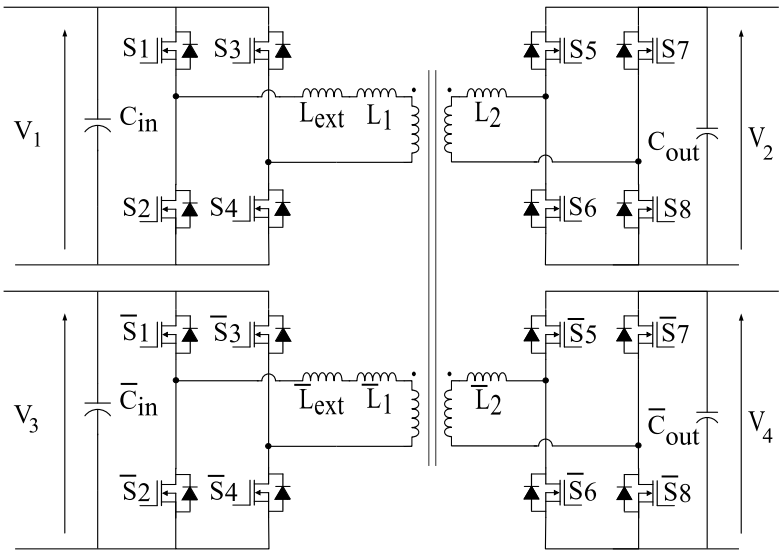

Figure 2.19: Quadruple-active bridge (QAB) converter schematic.

connected to battery and supercapacitor. This configuration require less magnetic elements as compared to the magnetic coupling solution in [83]. The power density is improved by removing the magnetic coupling of this solution. Phase shift control algorithm is developed to control the power transmission between the three sources.

A quadruple-active bridge (QAB) converter has been proposed in [82], which is based on the conventional DAB converter. Different ESSs are often utilized in the MEA architectures due to the different ESSs chemistry characteristics. The QAB, shown in Fig. 2.19, allows for power transfer control between four different voltage sources.

The QAB in [82,85,86] integrates four different energy sources: the HVDC bus, battery, supercapacitor and a fuel cell. The paper discusses the closed loop control of the QAB and the tuning algorithms of the multi-port configuration.

2.5 Dual active bridge (DAB) Converter Modulation Schemes

Since the DAB converter offers simple control, high power density solution, the DAB is widely utilized for the MEA DC/DC converter linking the HVDC bus to the LV network. Most of the multi-source, multi-port and multilevel topologies presented in literature for such application are based on the DAB topology. In this section, the different DAB modulation techniques are reviewed.

2.5.1 Single phase shift (SPS) control technique

The DAB simplified schematic is illustrated in 2.20. The simplified circuit consists of the DAB inductor in-between two square-wave generators representing the output of the primary and secondary switching. The phase shift created between the two square waveforms allows for the power transfer through the DAB inductor. The SPS modulation technique, shown in Fig. 2.20 (b), is the simplest modulation method for the DAB converter. This technique has one control variable, referred to as the phase shift angle between the primary full-bridge and the secondary full-bridge [87–90]. The phase shift angle between the primary and secondary transformer voltages is denoted

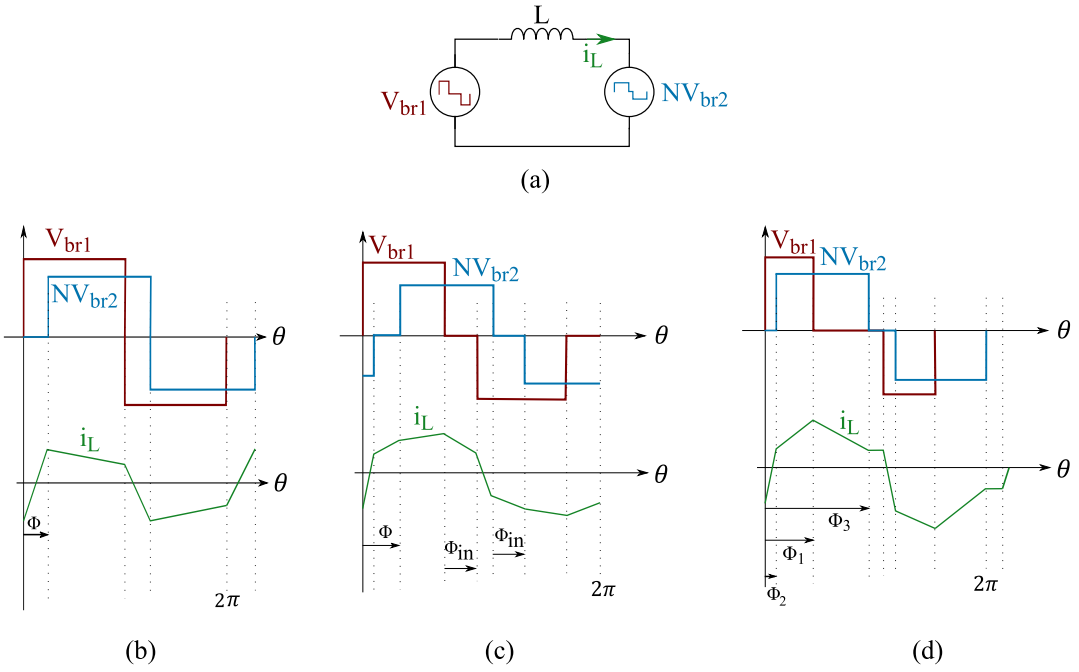

Figure 2.20: Different DAB modulation techniques. (a) Equivalent simplified circuit. (b) SPS. (c) DPS. (d) TPS.

as D_2. The power equation for SPS control is defined as: [91]

$$P_{SPS} = \frac{NV_{in}V_{out}}{2L_{lkg}f_{sw}} D_2(1 - D_2) \tag{2.5.1}$$

Where the input voltage, output voltage, transformer turns ratio, switching frequency and leakage inductance are represented by V_{in}, V_{out}, N, f_{sw} and L_{lkg}, respectively.

One method to ensure the high-efficiency operation of DC/DC converters is through ZVS. With ZVS, the voltage across the switch drops to zero prior to turn-on. The overlapping area between the current and voltage is therefore eliminated, leading to zero turn-on losses. SPS modulation has a limited ZVS range, which requires investigation of other control techniques to ensure high-efficiency operation at all load conditions [91].

2.5.2 Dual phase shift (DPS) control technique

The dual phase shift (DPS) modulation technique, shown in Fig. 2.20 (c), contains two control variables. The phase shift angle between the primary and secondary full-bridge is referred to as the outer phase shift [92–96]. The second control variable is the phase shift angle between the gating signals of the two legs within each full-bridge. The following power equation under DPS control holds: [50, 92, 93]

$$P_{DPS} = \frac{NV_inV_out\left(-\frac{1}{2}\phi_{in}^2 + \phi(1-\phi)\right)}{2L_kf_{sw}}, \phi \geq \phi_{\text{in}}\,. \tag{2.5.2}$$

$$P_{DPS} = \frac{NV_inV_out\phi\left(1-\phi_{in}-\frac{1}{2}\phi\right)}{2L_kf_{sw}}, \phi < \phi_{in}. \tag{2.5.3}$$

$$\phi + \phi_{\text{in}} \ < 1 \tag{2.5.4}$$

Where ϕ is the primary to secondary phase shift, ϕ_{in} is the inner phase shift between both primary legs and both secondary legs.

With DPS control, the number of switches achieving ZVS are higher compared to SPS modulation, especially at low power levels [96].

2.5.3 Triple phase shift (TPS) control technique

The triple phase shift (TPS) modulation technique, shown in Fig. 2.20 (d), contains three degrees of freedom [51, 97–101]. Three phase shifts with respect to one of the primary legs are defined as (ϕ_1, ϕ_2, and ϕ_3). The first is the phase shift angle between the primary and secondary full bridge. The second is the phase shift angle between

the two legs within the primary bridge and the third is the phase angle between the legs of the secondary bridge.

To ensure low conduction loss, switching loss, inductor, and transformer winding loss with minimized electromagnetic interference (EMI) and superior dynamic performance, the TPS strategy used must be suitable for a given voltage and power level [102]. Most literature focuses on TPS schemes aimed at minimizing the peak and root mean square (RMS) currents [103, 104]. The TPS technique can be categorized into six modes of operation based on the phase shift and conduction angle [105]. The TPS modulation can be considered as a generalized modulation technique where more degrees of freedom are available including those available in SPS and DPS. TPS modulation is of great interest in the design of highly efficient converters. This is due to its ability to achieve ZVS across the entire operating range [105].

2.6 Summary

DC/DC converters are crucial building blocks of modern aircraft architectures. The different aircraft architectures are reviewed and the future trends have been identified for more-electric aircraft networks. Standards and design guidelines are presented for the MEA application. The converter operating range and environmental constraints and certification testing procedure have to be considered in the converter design stage in compliance with the discussed standards. Several unidirectional and bidirectional topologies from existing literature were discussed. The primary goal of the MEA DC/DC converter is higher system efficiency and high power density. ZVS-based topologies have been of interest in such application due to the reduction of switching losses and improved converter efficiency across a wide range of operation. The DAB

converter and resonant converters are utilized in applications where high efficiency is required due to their wide-range ZVS operation. The DAB converter is widely adopted for the MEA DC/DC converter based on public academic research and production converters. Since the trend in MEA is towards higher voltage networks, several derivatives of the DAB converter including multilevel and multi-port based topologies are presented in literature. Different variations of the DAB to improve the system integration have been proposed in literature including ISOPs, IPOPs, three-port DAB, QAB. The derivative structures have emerged considering having multiple energy sources in the aircraft distribution network such as fuel cells, batteries and supercapacitors. A high-level comparison of the different control techniques of the DAB converter are presented. Three different control techniques are presented, SPS, DPS, and TPS. TPS is considered a generalized control technique with three degrees of freedom. Since TPS expands the ZVS region across all power levels, it is the most promising control method to ensure the high-efficiency operation of the converter at all operating points.

Chapter 3

Magnetic Design for Power Converters in Aerospace Applications

The major concerns in the design of isolated DC-DC converters for more-electric aircraft are the efficiency and power density. The areas that are mainly investigated to increase the efficiency and power density are the converter topology, switching devices technology, switching frequency optimization, magnetic components design, and converter control optimization. The magnetics design process is crucial to attain high power density and low converter weight. The converter performance is also dependant on the magnetic elements. The added parasitic elements associated with the magnetic components such as the isolating transformer and the filter inductors can alter the converter operation and should be considered in the magnetic design process. The parasitic elements include the transformer leakage inductance, equivalent series resistance of the windings and the capacitance formed between the winding layers either in inductors or transformers. This chapter goes through the different magnetic elements such as transformers, EMI filter chokes and filter inductors. The different magnetic materials and magnetic technologies are discussed. The effect of the magnetic parasitics on the converter performance is highlighted.

3.1 Magnetic Components in MEA DC/DC Converters

The first thing to consider in the magnetic design is the magnetic material of the core. Among the materials used for magnetics for DC/DC converters are silicon steel, ferrite, and noncrystalline materials.

Silicon steel is typically used for low-frequency applications of around 1 kHz for the high maximum flux density of the material [106]. Considering the low resistivity

of silicon steel, the silicon-steel core is built up from laminations to reduce the eddy current losses generated in the core.

Utilizing wide band gap switching devices allows for pushing towards high frequency operation to reduce the magnetics size. However, there are still limitations from the magnetics side relating to the increase of the core losses with frequency and the heat management issues related to the temperature rise. The magnetic material should exhibit low core losses at high frequencies for an improved power density. Nowadays, ferrite material is the most widely adopted magnetic material used in DC/DC converter applications. This is due to the available variety of off-the-shelf cores for different power levels as well as their low-power loss at high frequencies as compared to silicon steel. The low core losses of ferrite materials is due to the high core resistivity which results in lower eddy current losses [107].

Another type of materials that have been used lately in power electronics applications are nanocrystalline materials. The core losses per volume for nanocrystalline materials are lower than their ferrite alternatives at higher flux densities [108, 109]. Nanocrystalline materials also exhibit high relative permeability as compared to ferrite materials leading to higher power density [110]. Other advantages to nanocrystalline cores are the high curie temperature as compared to ferrite cores as well as the high permeability over a low to high frequency range which makes the material suitable for EMC common chokes and EMI filter inductors [111]. However, there are still limited research on nanocrystalline materials in literature.

Table 3.1 lists the properties of a ferrite material 3C93 in comparison to Vitroperm500F and FT-3M nanocrystalline materials.

Table 3.1: Magnetic materials comparison - Ferrite Material vs. Nanocrystalline Materials [109,112]

Material type	Material	B_{sat} (T)	Thermal conductivity (W/mK)	Density (g/cm^3)	Core losses (kW/m^3) @ 0.1T, 20kHz	Permeability @ 20 kHz
Ferrite	3C93	0.52	3.5-5	4.8	5	1800
Nano-crystalline	Vitroperm 500F	1.2	10	7.3	5	13200
Nano-crystalline	FT-3M	1.23	10	7.3	5	15000

Nanocrystalline materials have the potenial for improved power converter densities and weight and better thermal performance. However, given the low cost and availability of ferrite cores and limited research on nanocrystalline materials in comparison, ferrite material is the most utilized material for high frequency DC/DC converters in aircraft.

EMI chokes and filter inductors

Electromagnetic interference is one of the main design problems in DC/DC converters. The filter design involves the usage of magnetics elements such as filter inductors and chokes to satisfy the regulatory standards. Regulating and filtering the devices emissions is very crucial since this could affect critical flight sensors aboard the aircraft. The EMI tests also determine where the equipment can be located in relative to the critical components. The EMI requirements are specified in the DO-160 for commercial aircraft and by the MIL-STD-461E for military aircraft. The frequency response limits and range for the conductive and differential noise are specified in the standard along with the Line Impedance Stabilization Network (LISN) used in the test.

The EMI topology depends on the required attenuation to meet the standard [113]. The EMI filter typical configuration is shown in Fig. 3.1. The LISN is connected to a common mode (CM) and differential mode (DM) discrimination network to separate the total noise. The selection of the filter inductor and choke values is dependant on the required cut-off frequency to attenuate the noise in accordance to the regulatory standard [114]. The inductor core could be designed with either nanocrystalline or ferrite materials. Ferrite materials are usually used in the MEA DC/DC converter

due to the availability of off-the-shelf suitable chokes and filter inductors.

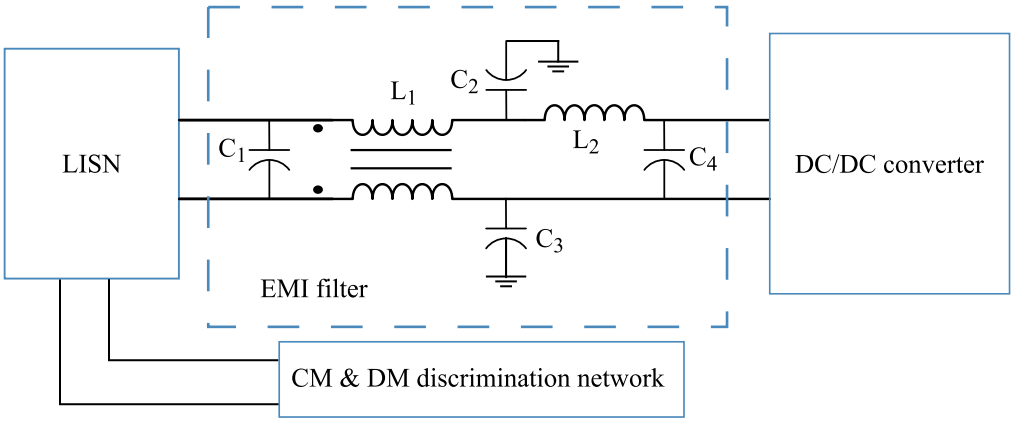

Figure 3.1: Typical EMI test setup for MEA DC/DC converters.

Power transformers

In an MEA, the DC/DC converters required to link the HVDC bus to the LV network require a high step-down ratio. Therefore, a high-frequency transformer is often used to provide galvanic isolation between the high and low voltage sides as well as to provide the high conversion ratio. In recent years, design of highly efficient and power dense isolated DC/DC converters have been gaining a lot of attention in industry. One of the most important contributing factors to the efficiency and power density is the transformer design. A compact and highly efficient transformer is crucial in the design of a power dense high-performance converter.

Planar magnetics are recently considered to increase the power density of DC/DC converters. Planar technology allows for power-dense, compact designs and provides homogeneous temperature distribution due to the large surface area of the planar cores [115, 116]. Selecting an optimum switching frequency is the first basic step to optimize the transformer size. A higher switching frequency is associated with

reduction of the self-inductance and the core size, resulting in more compact designs [117]. On the other hand, a higher switching frequency is associated with an increase in the switching losses for the power semiconductors in the converter. Core losses also increase at higher frequencies and temperature rise along with proximity and skin effects on the windings. Therefore, an optimal switching frequency selection procedure is required for optimum power density and converter efficiency. Based on these factors, an integrated optimization method combining both transformer design and the device switching losses can be beneficial in MEA applications. There have been many attempts in literature for optimizing transformers. One method presented in [118] is based on the integrated leakage inductance of the transformer and its phase shift within a dual active bridge converter. One benefit of this strategy is that the core dimensions are optimized and hence are not a limiting factor as discussed in detail in [118]. Other methods consider the switching frequency in the optimization process. The optimal switching frequency is chosen based on the lowest obtained losses with consideration of the transformer volume [119, 120].

3.2 High-frequency Transformer Configurations for DC/DC Converters

The transformer design process is split into core design and winding design. The current density of the windings has to be considered in the core selection process. The core window area needs to be large enough to fit enough winding copper to limit the current density of the windings. The window area utilization factor is based on the windings and core technology. Most transformer core design techniques presented

in literature use the area product (AP) method. In this method, the core is selected based on a factor related to the core geometry as well as the power handling capability of the core. Using the AP approach, core loss and thermal limitations dictate the selection of the flux density at a specific frequency.

The AP method is the most common approach to select a transformer core. The method is based on a factor which is the product of the window area and core area which is usually provided by most core manufacturers in their datasheets [121–123]. The AP factor can be tied to the converter specifications using the following equation:

$$A_p = \frac{P}{K_t J B_{max} f}. \tag{3.2.1}$$

where f_{sw} is the switching frequency, J is the winding current density, k_t is a factor depending on the converter topology, B_{max} is the maximum flux density and P is the converter power rating.

The maximum flux density in this method is selected, rather than optimized, to limit the core losses for a predetermined switching frequency.

Transformer winding configurations

The transformer winding configuration affect both the converter performance and efficiency. There are trade-offs concerning the winding design in terms of efficiency and transformer parasitic elements. The parasitic elements include the transformer leakage inductance and the capacitance formed between the transformer layers. An accurate prediction of the transformer losses is needed based on the windings configuration. High frequency power transformer windings suffer from AC losses associated with eddy current effects due to the skin effect and proximity effect. The AC losses

are dependant on the number of layers and the current distribution in the winding layers.

The configurations can be split into non-interleaved, semi-interleaved and interleaved configuration. Interleaving refer to alternating the primary and secondary windings of the transformer which in result lowers the magnetomotive force (MMF) amplitude between the layers resulting in lower winding loss. Fig. 3.2 shows three common windings configurations. The AC losses highly depends on the the MMF amplitude across the winding. For the non-interleaved windings shown in Fig. 3.2 (a), the peak MMF amplitude between the layers is high resulting in higher losses as compared to the interleaved and semi-interleaved structures shown in Fig. 3.2 (b) and (c) respectively.

The AC/DC resistance ratio is obtained using Dowell's formula to get the AC losses [124, 125]:

$$\begin{aligned} F_r &= \frac{P_{AC}}{P_{DC}} = \frac{R_{ac}}{R_{dc}} = \Delta[\zeta_1 + \frac{2}{3}(M^2-1)(\zeta_1 - 2\zeta_2)] \\ \zeta_1 &= \frac{sinh(2\Delta) + sin(2\Delta)}{cosh(2\Delta) - cos(2\Delta)} \\ \zeta_2 &= \frac{sinh(\Delta)cos(\Delta) + cosh(\Delta)sin(\Delta)}{cosh(2\Delta) - cos(2\Delta)} \\ \Delta &= \frac{t}{\delta}. \end{aligned} \tag{3.2.2}$$

where F_r, is the AC/DC losses ratio, M is the number of layers, t is the copper thickness, and $\delta^{'}$ is the skin depth.

The value M is defined as follows:

$$\mathrm{M} = \frac{MMF(x)}{MMF(x) - MMF(0)}. \tag{3.2.3}$$

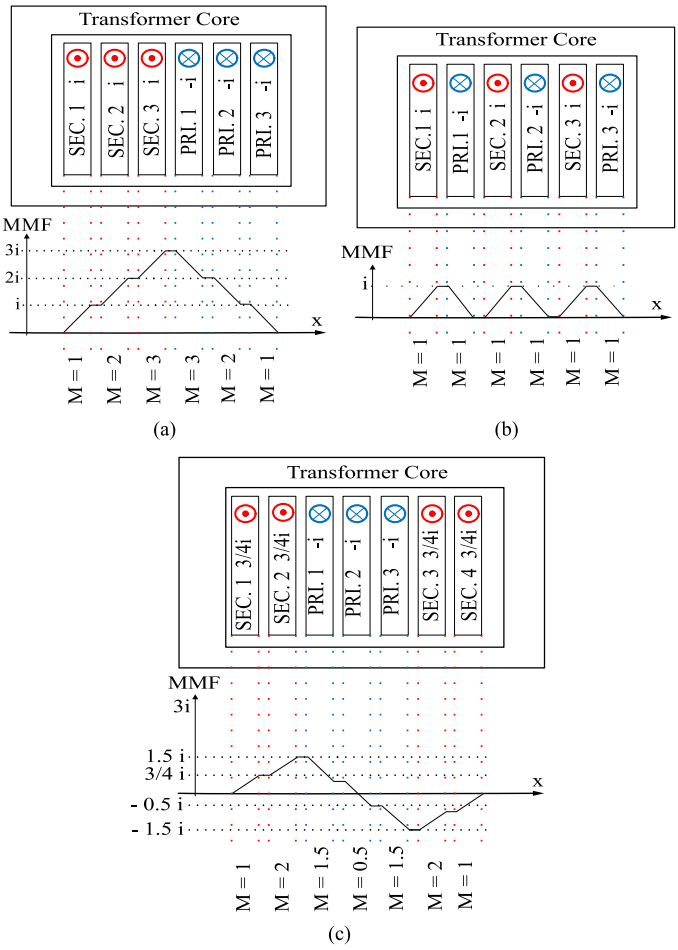

Figure 3.2: MMF diagram of different transformer windings configurations. (a) non-interleaved configuration. (b) interleaved configuration. (c) semi-interleaved configuration.

Where MMF (x) and MMF (0) are the normalized MMF amplitude across the winding.

As can be seen in Fig. 3.2 (a), the interleaved winding has a fixed value of M equals to 1 which lowers the AC loss value of the windings. However, M is higher for the semi-interleaved and fully interleaved configurations. In conclusion, the interleaved structure is often preferred to minimize the eddy effect in high-frequency transformer. This represents one aspect of the transformer winding design based on minimizing

the AC losses. The other aspect is the transformer parasitic capacitance which highly impacts the converter performance. The different winding configurations results in different formed parasitic capacitance between the transformer winding layers.

3.3 Magnetics Parasitic Capacitance and Converter Performance

For planar magnetics, since a larger overlap area between the winding layers is present, a larger capacitance is formed between the windings terminals as compared to the conventional cores. The effect of the stray capacitance is usually not considered for most optimization processes in literature, which is a crucial parameter for the performance of planar transformers. There are two types of parasitic capacitance; self capacitance (intra-winding capacitance) which is formed between the same winding terminals and mutual capacitance (inter-winding capacitance) which appears between different windings.

The effect of the inter-winding and intra-winding capacitances can be modeled using six different capacitors highlighted in Fig. 3.3 (a) [126]. The inherit parasitic capacitances can also be lumped into a single capacitor model as illustrated in Fig. 3.3 (b). High frequency oscillations on the transformer voltages are the result from the formed resonant tank between the stray capacitance, and the leakage inductance as shown in Fig. 3.4. The amplitude and frequency of oscillations depends on the resonant tank components values, the switching frequency, and the converter external inductors in case of DAB and resonant converters. The high oscillations

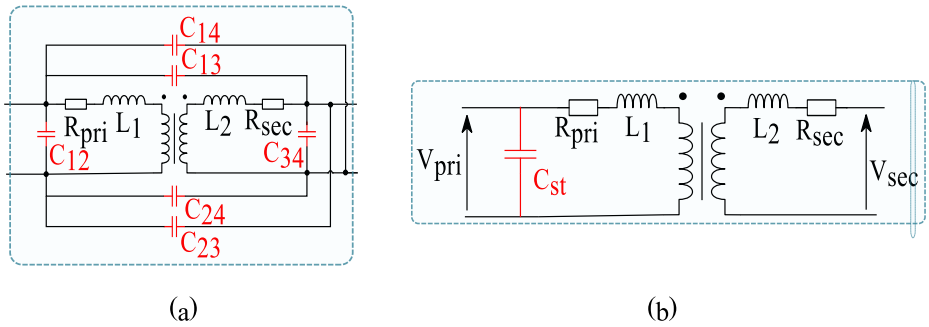

Figure 3.3: Stray Capacitance Effect on the Transformer Waveforms.

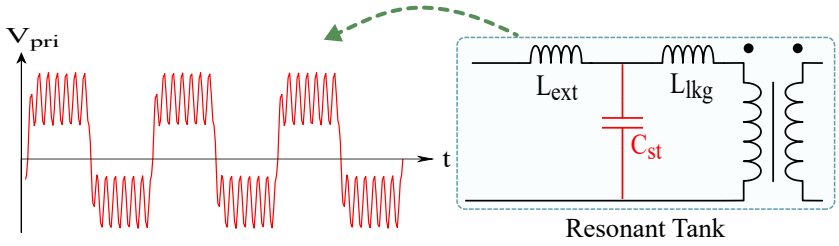

Figure 3.4: Stray Capacitance Effect on the Transformer Waveforms.

highly affects the converter performance, power density and reliability. For the interleaved windings, more interfaces are formed between the primary and secondary sides, resulting in higher inter-winding capacitance, but lower capacitance between the layers of the same windings and hence a lower intra-winding capacitance. One of the main concerns in MEA DC/DC converters is converter performance and reliability [127]. This is particularly important in high switching speed applications, where the high-frequency oscillations problem due to the transformer stray capacitance and high dv/dt transitions are more apparent [128]. The HFO compromises efficiency through increasing AC losses in the transformer at high frequencies. Power density of the converter is impacted as a result of the HFO due to the requirement of a large EMI filter at the input [129]. One method proposed in literature to address the high dv/dt of the DAB is through adding a snubber capacitor in parallel with the power

devices [129]. In [130], a detailed analysis in core loss, winding loss, stray capacitance and leakage inductance of planar transformers is investigated with consideration of the trade-offs. As outlined earlier, the DAB converter performance can be enhanced by minimization of the winding capacitance. Most attempts in literature use conventional double layer designs to reduce the transformer winding capacitance and either investigate changing the stacking configuration or the turns arrangement. The double layer approach can compromise the efficiency as well as the power density through increased width of the planar PCB [131]. Different winding configurations were investigated in [131]. The non-overlapping structure has no overlap between turns on both PCB layers, which results in no overlapping area between the layers and hence a significant reduction in the capacitance. The non-overlapping arrangement has high AC losses due to lower transformer utilization factor. Some configurations found in literature, such as the alternating winding configuration, aims to reduce voltage gradient between the layer [130–132].

3.4 Summary

In this chapter, various magnetic materials has been compared. Ferrite materials are the most widely used in high-frequency converters. Nanocrystalline cores exhibit high potential for their high saturation flux as compared to ferrite materials. The typical test setup for the EMI filters in accordance to the DO-160 standard was discussed. The transformer windings arrangement introduces a trade-off between the transformer AC losses and windings parasitics. The winding structure has to be analyzed considering both the AC losses and capacitance which a crucial design step for planar magnetics utilized for the MEA converters to ensure optimized performance.

Chapter 4

Design Optimization Methodology for Planar Transformers for MEA Applications

In this chapter, an optimization method is developed; this algorithm considers different materials and cores paralleling with a large planar cores database. The design procedure is based on minimizing the overall transformer losses by selecting an optimum maximum flux density. The algorithm performs a frequency sweep to identify the optimal core material and configuration at each switching frequency point based on the optimization variables. The core optimization results are then integrated with the converter switches loss analysis to obtain the global optimum switching frequency. With the magnetic core geometry defined, the winding design takes place. The winding configurations affect the transformer parasitic elements such as leakage inductance and stray capacitance. The transformer parasitic components directly impacts the converter performance. After selecting an optimum core, the rest of the chapter presents a proposed winding configuration to mitigate the issues caused by the transformer parasitic components.

A new multi-layer minimum gradient configuration is proposed to reduce the transformer stray capacitance while improving the transformer efficiency and power density. The MLMG configuration aims to reduce the voltage gradient between the layers in the same winding, through a multi-layer arrangement with blind-hole connection between the layers. The capacitance is therefore reduced. With this multi-layer approach, the power density and AC losses are not compromised to reduce the stray capacitance. Simpler assembly is also obtainable with this configuration. The proposed three-layer winding arrangement provides 20% higher power density than a similar double-layer design. This structure has higher power density than the non-overlapping and alternating winding structures proposed in [131] and does not sacrifice efficiency. Converter performance is improved through eliminating HFO caused by

the stray capacitance, through reduction of the capacitance.

The chapter is presented as follows. Section 4.2 presents the developed optimization methodology and the relation between the different tools used in the process. Section 4.3 looks at the core optimization procedure and covers the different transformer design methods, and a discussion of the algorithm results. Section 4.4 proposes two multi-layer minimum-gradient configurations and compares them to the conventional spiral configuration. Finally, the experimental validation of the proposed winding structures including the effect on the converter performance is presented in Section 4.5.

4.1 Proposed Transformer Design and Optimization Procedure

Isolated DC-DC converters are utilized to supply the low voltage (28Vdc) loads in MEA. The DAB topology is used as a case study to validate the transformer design methodology proposed in this chapter. The DAB converter is the most utilized topology for the MEA converter for the simple control, bidirectional operation and wide ZVS operation [52, 77, 85, 127]. The converter schematic considering the transformer parasitic elements is shown in Fig. 4.1. An external inductance (L_{ext}) is utilized to control the power flow between the two full bridges connected across the transformer. One of the simplest control strategies utilized to control the DAB converter is phase-shift modulation. Where the voltages across the primary and secondary bridges are phase-shifted with respect to each other. Both the external leakage inductor and the phase shift control the power flow in a bidirectional manner. The DAB transformer

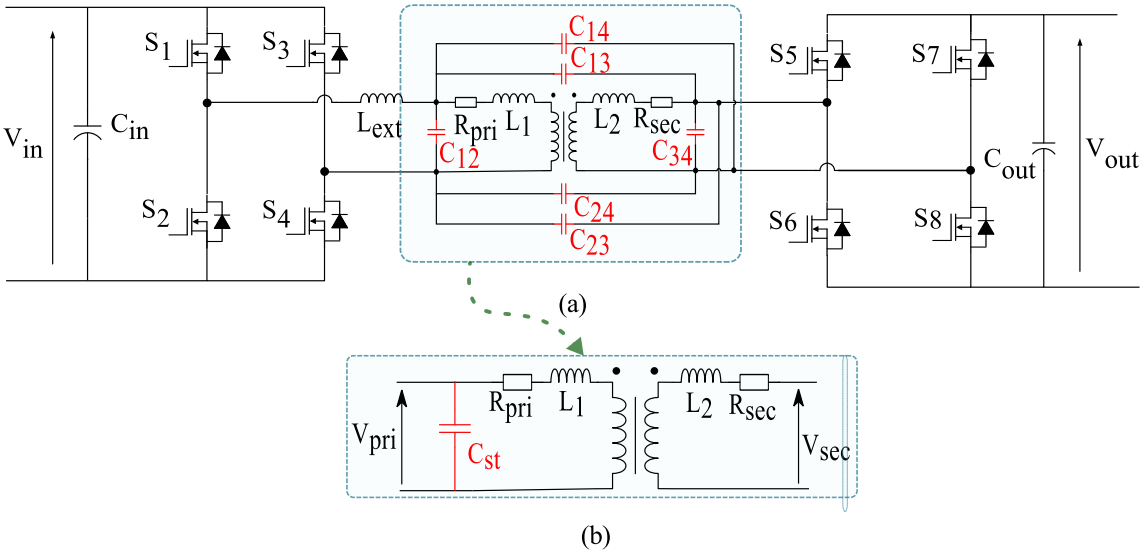

Figure 4.1: DAB Converter Schematic Considering the Transformer Parasitic Elements: (a) DAB schematic - six capacitors model and (b) Transformer lumped capacitor model.

specifications are listed in Table 4.1. In the developed design methodology, both the transformer core and the windings configurations are optimized to minimize the transformer volume and losses and improve the DC-DC converter performance. The procedure is composed of three main tools: an optimization tool to minimize the core weight and volume, a semiconductor loss analysis tool, and an optimization process for the windings configuration.

The Venn diagram, shown in Fig. 4.2, highlights the overlap between the three optimization aspects to reach an optimum transformer design in terms of specific power, volume, efficiency and EMI performance. The switching frequency and core selection is based on an integration process between the semiconductor loss analysis tool and the core optimization tool.

Table 4.1: DAB Converter Specifications

Parameter	Value
Input Voltage	480-650 V (600 V nominal)
Output Voltage	22-28 V
Power	4 kW
Transformer Ratio	22:1
Secondary RMS Current	210 A
Primary RMS Current	10 A

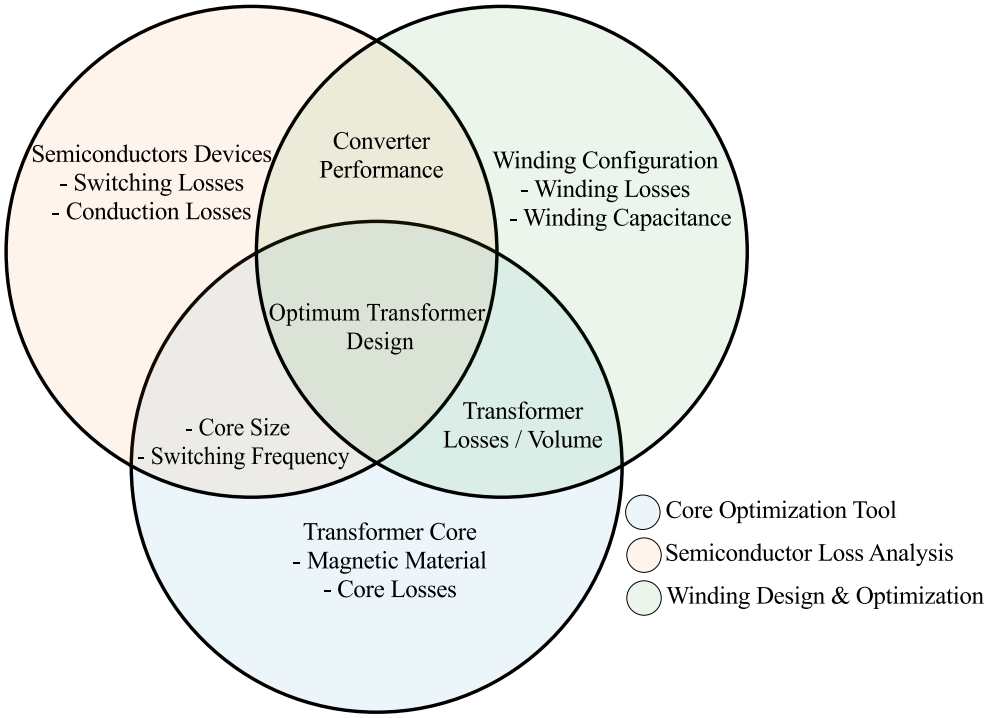

Figure 4.2: Venn Diagram of the Developed Design Tool.

The transformer losses and volume are linked between the optimally selected core and the winding configurations. The converter performance is a function of both the switching frequency and winding configuration.

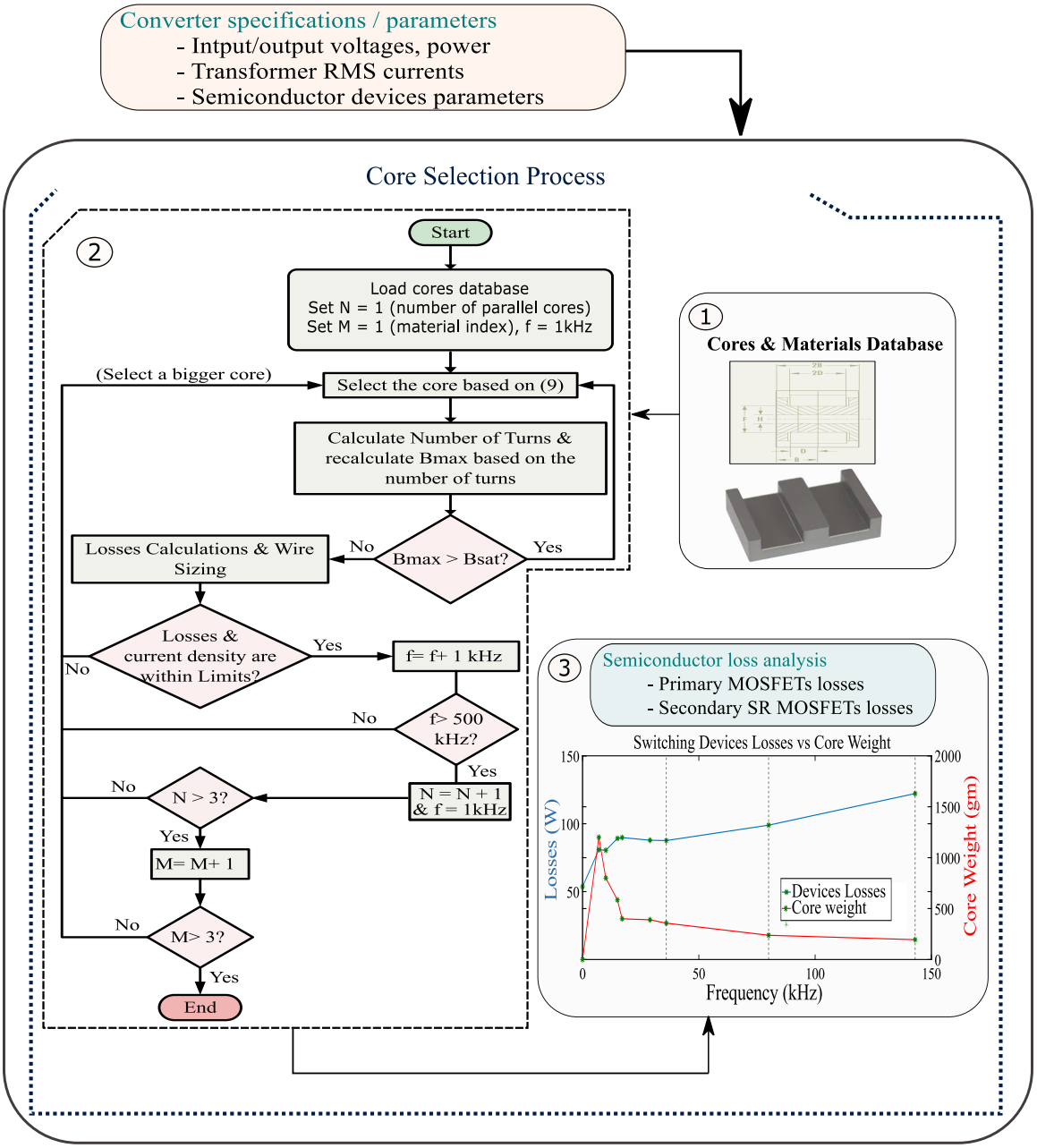

Figure 4.3: Core design methodology block diagram.

Fig. 4.3 illustrates the design flow of the proposed core optimization methodology. Based on the converter specifications and semiconductor parameters, the optimal core

is selected through the integration process between the core optimization algorithm and the loss analysis tool. The core optimization tool includes the effect of the magnetic material and core paralleling on the transformer power density. The materials properties as well as the cores data are obtained from Magnetics Inc. catalogue [112]. Cores paralleling is considered due to large cores avail ability and to add flexibility to the selection process. The design chart shown in Fig. 4.3 outputs the optimal core weight, total losses, and maximum flux density at different frequencies.

The total transformer losses are minimized at each frequency point by selecting an optimum flux density. The relationship between the maximum flux density and both copper and core losses is shown in Fig. 4.4, where the maximum flux density can be selected to minimize the transformer losses [128]. The local optimal frequency points are extracted from the core design tool and passed to the semiconductor loss analysis tool to obtain the overall device losses and plot it against the core weight.

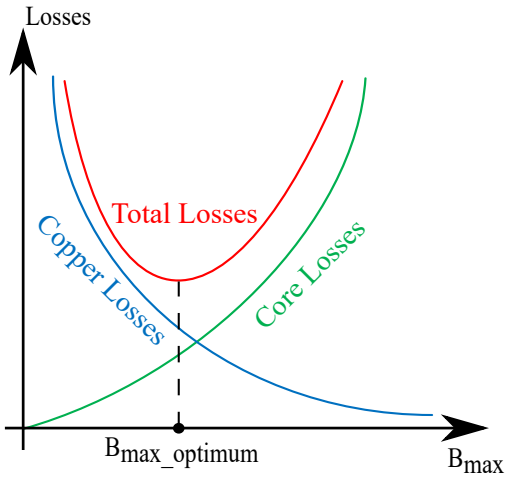

Figure 4.4: Optimum flux density and the total losses relation.

Finally, the global optimum frequency point is obtained with the optimum core material and configuration from the database. The optimal core is then passed to

the winding design and optimization tool. Based on the selected core geometry, the transformer windings are automatically designed for different configurations. Two configurations are proposed and compared with two conventional winding configurations highlighting the effect on the transformer performance. The optimal core is then fed to the winding optimization algorithm as shown in Fig. 4.5. The different winding configurations are generated and the stray capacitance is extracted for each. The noise analysis is carried out in the PLECS simulation environment. FEA simulations are carried out to validate the proposed windings in comparison to the conventional structures.

The proposed designs aim to mitigate the HFO issue without sacrificing the transformer power density and efficiency. The single stray capacitance is obtained analytically through the design tool for four different configurations. The values are automatically passed to PLECS to simulate the converter with the obtained parameters. The amplitude and frequency of oscillation are obtained highlighting the effect of the different configurations on the converter performance. The different configurations are simulated in ANSYS Maxwell to extract the capacitances values and evaluate the losses and compare it to the analytical tool results. The proposed design methodology is suitable for planar transformers in most applications to improve the power density and reduce the stray capacitance. However, the MEA application introduces a challenge in the required high turns ratio as well as the high current on the secondary side which must be considered while proposing a specific structure to reduce the transformer capacitance. Being one of the bulkiest elements in the power converters used onboard the aircraft, improving the power density by investigating

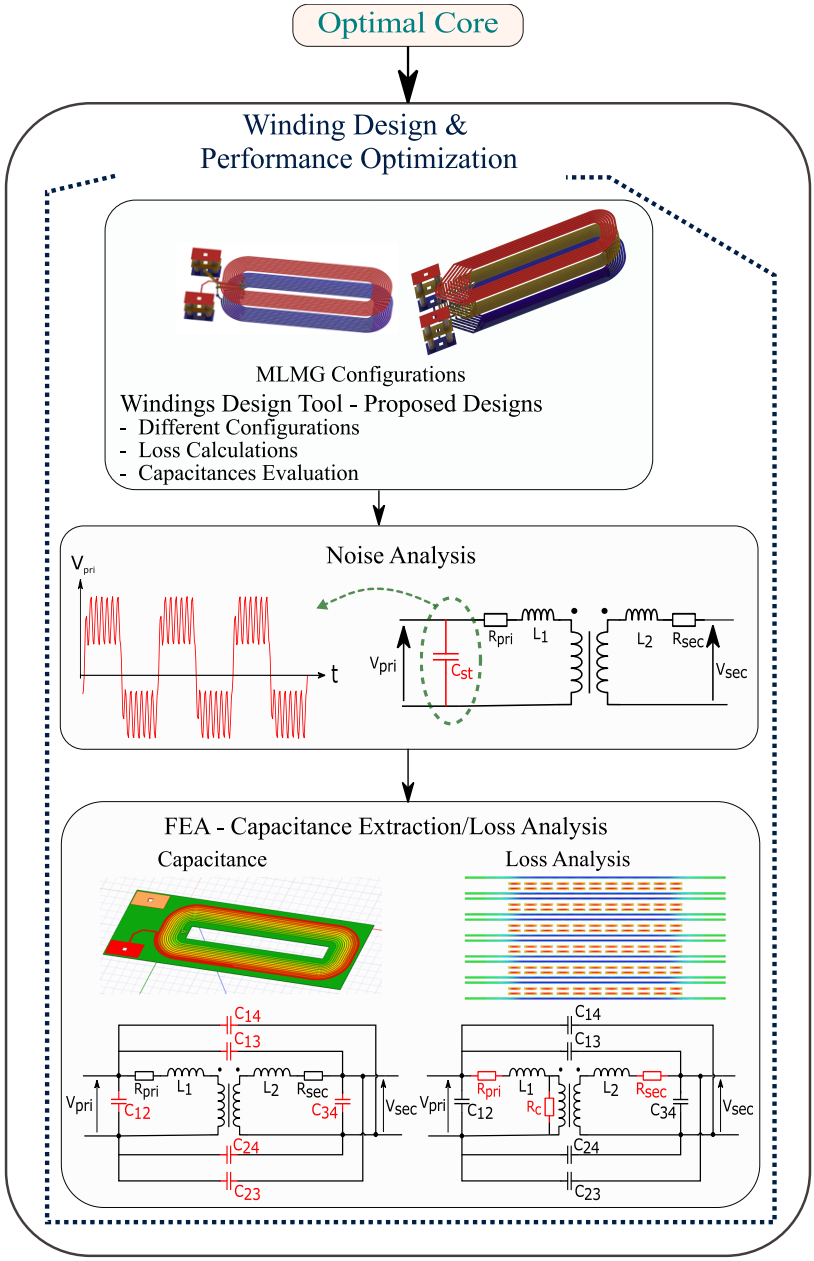

Figure 4.5: Winding design and performance optimization procedure.

different materials, cores in parallel, etc. is crucial in such application. The transformer mechanical assembly process of the proposed structures must be suited to the high-current transformers utilized in MEA converters. All the mentioned concerns have been considered in the proposed design methodology in this chapter.

4.2 Transformer Core and Switching Frequency Selection

4.2.1 Transformer core selection algorithm

The core material selection is the first step in the magnetic design process. The magnetic material highly affect the core losses and hence its temperature rise. Materials that features high permeability and high saturation-density such as nanocrystalline materials have been used lately in high-frequency applications. Such materials allow for size and weight reduction by pushing towards high-frequency operation due to their high saturation flux density and low core losses as compared to ferrite materials [133, 134]. The high cost and core shapes availability are the limiting factors for nanocrystalline materials where custom-made cores are needed for an optimized design. Ferrite materials, on the other hand, are available in many off-the-shelf core shapes and offer low core losses as compared to silicon steel. For these reasons, ferrite materials are still widely utilized in industry for high-frequency magnetics in power electronic converters. Three ferrite materials offered by Magnetics Inc. are considered in the optimization process proposed in this section. The material properties are listed in Table 4.2. A large planar off-the-shelf cores database is used in the design process.

Table 4.2: Material Properties - Magnetics Inc. [112]

Material	Properties	Permeability @20kHz	$B_{sat}(T)$	Core losses (mW/cm^3)	Density (g/cm^3)	Thermal conductivity ($mW.cm^{-1}.\ ^\circ C^{-1}$)
F	High temperature	3000		110		
P	stability, low losses,	2500	0.47	65	4.8	35-43
R	and high saturation flux	2300		58		

The design method utilized in the optimization process is based on selecting an optimum maximum flux density to minimize the total losses. This optimum value can be obtained by finding the derivative of the total losses with respect to the maximum flux density and equating it to zero as follows:

$$\frac{dp_{tot}}{B_{max}} = \frac{dp_{copper}}{B_{max}} + \frac{dp_{core}}{B_{max}} = 0. \tag{4.2.1}$$

where P_{copper}, P_{core}, and P_{tot} are the copper losses, the core loss, and the total losses respectively.

The copper losses can be expressed as follows:

$$P_{Copper} = I_{tot}^2 R_{winding} = \frac{I_{tot}^2 n^2 MLT\rho}{W_A K_u}. \tag{4.2.2}$$

K_u is the utilization factor, MLT is the mean length per turn, W_A is the window area, n is the number of turns, ρ is the copper resistivity, $R_{winding}$ is the winding resistance, and I_{tot} is the total current referred to the primary side.

Applying Faraday's law, the number of turns can be found as:

$$n = \frac{\lambda}{2B_{max}A_c} 10^{-4} A_c^2. \tag{4.2.3}$$

where λ = D * f_{sw} * v_{in} is the voltseconds, D is the duty cycle, f_{sw} the switching frequency, v_{in} is the input voltage, B_{max} is the maximum flux density and A_c is the core area.

The copper losses can then be derived as:

$$P_{Copper} = \frac{I_{tot}^2 \lambda^2 MLT \rho}{4 w_A K_u A_c^2 B_{max}^2}. \tag{4.2.4}$$

Steinmetz equation is used to obtain the core losses:

$$P_{core} = K_{fe} B_{max}^{\beta} V_{core}. \tag{4.2.5}$$

where V_{core} is the core volume, β is the Steinmetz exponent and K_{fe} is a frequency-dependant constant.

An equation relating the core geometry and the converter specifications can the be derived from (4.2.1):

$$\frac{w_A A_c^{(2(\beta-1)/\beta)}}{MLT\ l_m^{(2/\beta)}} \left[\frac{\beta}{2}^{-\left(\frac{\beta}{\beta+2}\right)} + \frac{\beta}{2}^{\left(\frac{\beta}{\beta+2}\right)} \right]^{-\left(\frac{\beta}{\beta+2}\right)} = \frac{I_{tot}^2\ \lambda^2\ \rho K_{fe}^{\frac{2}{\beta}}}{4K_u\ P_{tot}^{\frac{\beta+2}{\beta}}}. \tag{4.2.6}$$

Equation (4.2.6) can be used to select the transformer core. The left-hand side of (4.2.6) is related to the core geometry and can be calculated for a specific core, similar to the AP factor, using the dimensions given in the datasheet. The transformer core can then be selected based on K_{gf} in (4.2.7):

$$K_{gf} \geq \frac{I_{tot}^2\ \lambda^2 \rho K_{fe}^{\frac{2}{\beta}}}{4K_u\ P_{tot}^{\frac{\beta+2}{\beta}}}. \tag{4.2.7}$$

The core loss plots provided in the materials datasheet are used to obtain the Steinmetz coefficients at different frequencies. This is carried out by fitting the data given to the Steinmetz equation as in Fig. 4.6. The parameters are extracted for all the materials used in the optimization process and are listed in Table 4.3.

Following the design chart shown in 4.3, at first, the geometrical constant K_{gf},

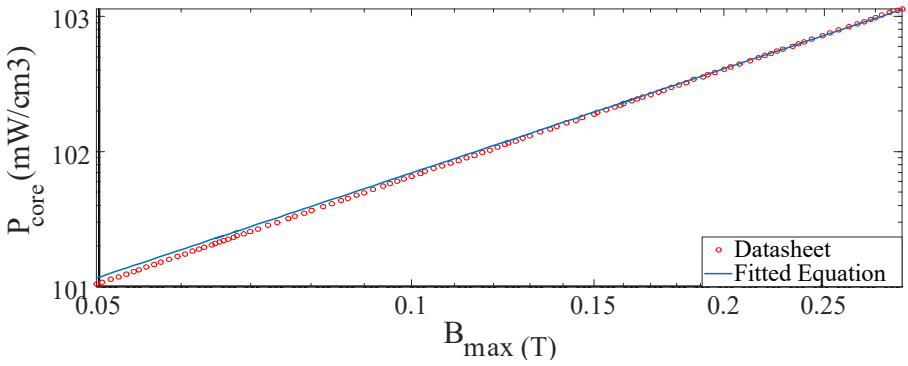

Figure 4.6: Datapoints fitting to Steinmetz equation.

Table 4.3: Extracted Steinmetz Coefficients.

Frequency range	Coefficients	F-material	P-material	R-material
100kHz <f < 500kHz	K	27.42	18.092	17.23
	α	1.66	1.63	1.64
	β	2.68	2.62	2.68
f <100kHz	K	32.77	114.461	52.388
	α	1.72	1.36	1.43
	β	2.66	2.86	2.85

that is the left-hand side of (4.2.6), is obtained for all the cores listed in the database. The frequency is initialized as 1 kHz and the number of cores in parallel (N) is set to 1 and the first material is selected. Based on the converter specification, the core is selected based on (4.2.7). Using Faraday's law, the number of turns is then calculated. The flux density is reevaluated using (4.2.3) based on the number of turns and ensured to be below the core saturation flux (B_{sat}). The transformer losses are then obtained using (4.2.4) and (4.2.5) and verified not to exceed a predetermined limit set by the designer, based on the required efficincy and the cooling method used. The process selects a larger core in case of flux saturation, or if the losses or the current density are above the limits. The frequency is then incremented by a 1 kHz step and the

optimum selection process is repeated up to 500 kHz. The number of parallel cores is then incremented and the process is repeated. The number of cores in parallel is limited to three cores due to mechanical stacking limitations and the average MLT to limit the conduction losses. When a maximum of three paralleled cores is reached, the design process is carried out for the next available material. The results of this design process yields some potential optimum frequency points as will be discussed in the results section. Those frequency points are then passed to the semiconductor loss analysis tool, where the switches losses are calculated for the different frequency point. The optimum switching frequency is then selected based on the integration process and hence the optimum transformer core.

4.2.2 Switching frequency and core selection results

A single-core design is considered first to compare between the three materials. Figures 4.7 and 4.8 show the total transformer loss and the core weight for different materials respectively. The power loss changes with frequeny since different optimum flux density is selected at each frequency point and hence different number of

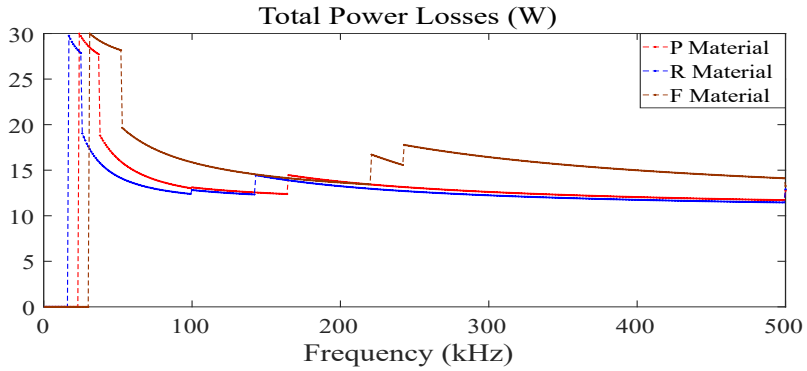

Figure 4.7: Total Transformer Losses against Frequency for Different Materials.

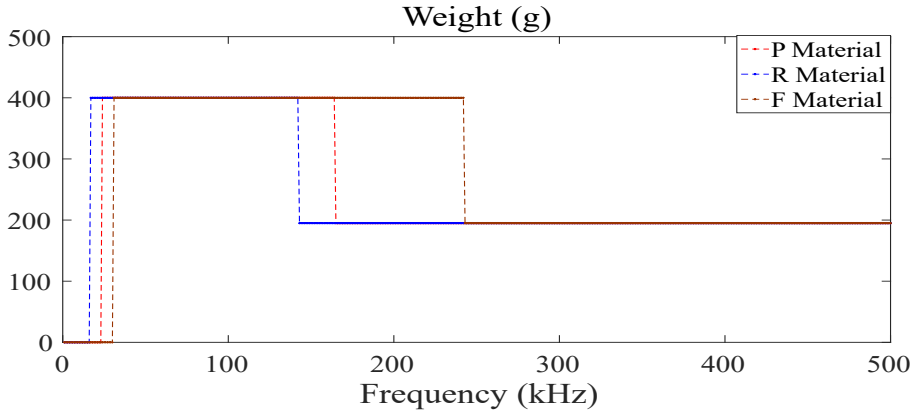

Figure 4.8: Weight against Frequency for Different Materials.

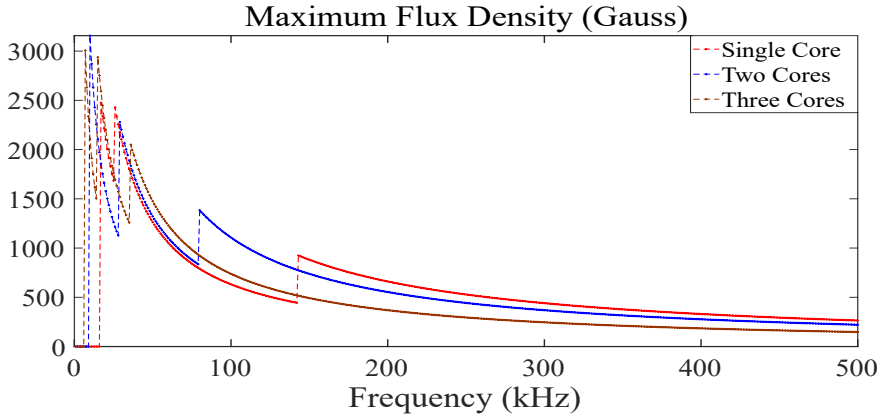

Figure 4.9: Maximum flux density against frequency.

turns. As illustrated in Fig. 4.8, there are limited single cores available to meet the power requirements and hence a multiple parallel core design is required to optimize the core weight. R material shows the best characteristics in terms of losses and transformer weight vs frequency as shown in Figs. 4.7 and 4.8. The analysis is then carried out for R material considering cores paralleling. Fig. 4.9 illustrates the maximum flux density as a function of the frequency for different number of parallel cores for R material. The maximum flux density decreases as the frequency increase to limit the core losses. The core size cannot be lowered after a specific frequency

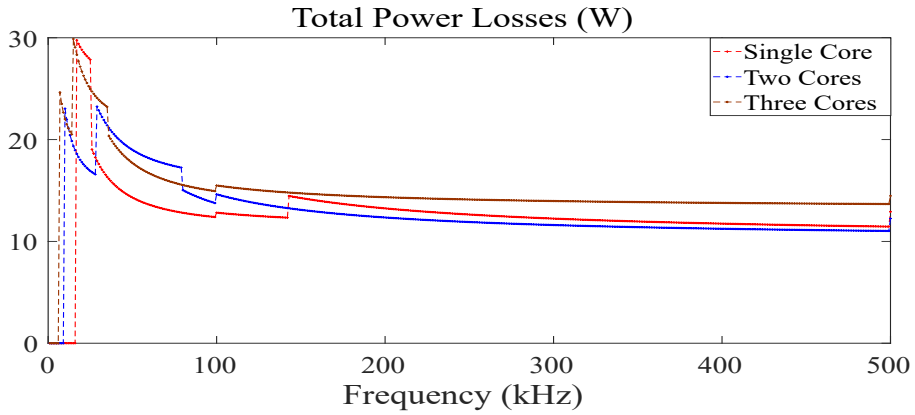

Figure 4.10: Total transformer losses against frequency for parallel cores.

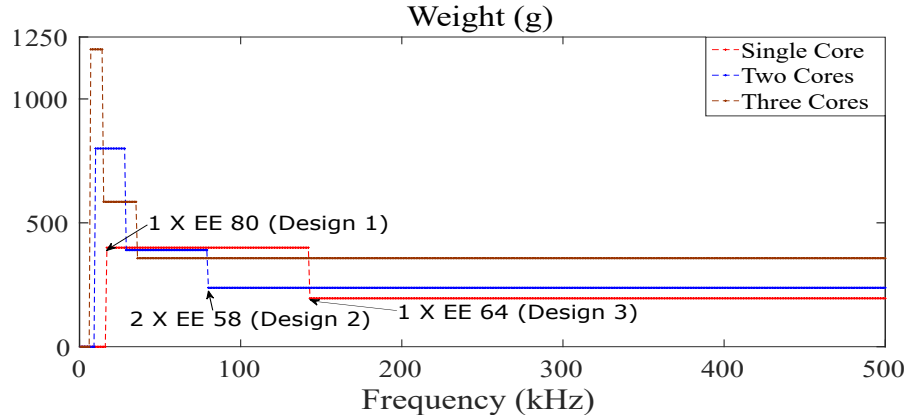

Figure 4.11: Core weight against frequency for parallel cores.

point because of the current density limitation. A minimum copper area for the windings and hence a minimum window area is required based on the current density constraint. The losses and weight considering paralleled cores configuration are shown in Figs. 4.10 and 4.11 respectively. As a result, Two EE 58 cores, labeled as Design 2 in Fig. 4.11., were obtained with a total weight of 238 g, featuring a volume of 49200 mm^3 and 15 W of losses. Design 3, on the other hand, is a single EE 64 core weighting 200 g, featuring a volume of 41400 mm^3 and 14 W of losses. Design 3 seems to be the optimum design from the transformer's perspective since

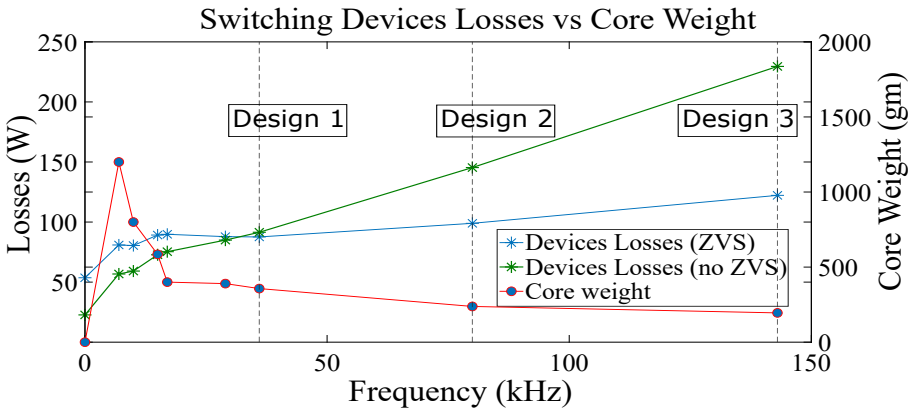

Figure 4.12: Semiconductor losses integration results.

it is 16% lighter and less voluminous and it has 7% lower losses. However, Designs 1 & 2 features lower switchng frequency as compared to Design 3 and hence lower switching losses and better efficiency on the converter level. This calls for an integration between the core selection and the switches loss analysis to ensure an overall optimized design on the converter level. There are local optimum frequency points from the transformer perspective such as the three designs highlighted in Fig. 4.11. Those points are passed to the switches loss tool and results of the loss analysis are used to get a global optimum switching frequency. The losses of the MOSFETs of the DAB converter are then obtained at the different local frequency points extracted from the transformer tool. The design has been developed with Silicon Carbide (SiC) FETs for the HV bridge (SCT3160KLHRC11) and Silicon (Si) devices for the LV side (IPP023N10N5AKSA1). Two SiC devices are connected in parallel for each primary switch and six Si devices are paralleled for the secondary-side switches. Results of the loss analysis are illustrated in Fig. 4.12 considering having ZVS and also in case of no ZVS. This is to discuss the importance of integrating the loss analysis with the transformer tool results in selecting the optimum switching frequency and hence the

optimum transformer core. Fig. 4.12 shows three design lines, at 35 kHz, 85 kHz and 150 kHz. Considering having a ZVS condition, Design 2 at 85 kHz seems to be better than Design 1 at 35 kHz since the losses have not increased significatly and the weight of the core is reduced by 33%, also the EMI filter size will reduce for Design 2 due to the higher switching frequency. However, if the topology does not have ZVS, it can be seen from Fig. 4.12 that the losses increase by a large value from Design 1 line to Design 2 and in this case, Design 1 seems to be the optimum design. This indicates that the global optimal switching frequency point depends on the topology as well. As for Design 3, the losses increase compared to Design 2, which results in an increase in the thermal management requirements, and only a reduction in the core weight by 35 g. Weighting factors can be assigned to both the total losses and core weight to select the switching frequency. In this MEA application, the weight assigned to the losses is 40% and 60% to the core weight. Based on the converter design requirements, different weights can be assigned. Design 2 was selected as the optimum frequency point. The developed tool provides guideliness to optimize the core weight considering the overall converter efficiency by optimizing the flux density and selecting and optimum switching frequency.

4.3 Transformer Winding Design and Optimization

4.3.1 Transformer stray capacitance

Large overlapping area in the conventional winding configurations in planar transformers results in high frequency oscillations limiting their applications in MEA. The

Table 4.4: Windings Description.

Parameter	Value
Number of secondary turns	1
Number of primary turns	22
Copper thickness	175 μm
Number of secondary layers	12
Number of primary layers	6

HFO resulted from the transformer parasitic capacitances highly impacts the converter reliability. This section proposes a multilayer winding design to mittigate the HFO issue. The optimum core geometry and required number of turns resulted from the transformer core optimization process are used to design the winding stack. Based on the optimal core height, the number of layers are specified and kept the same for all configurations. The copper thickness is selected based on the optimum switching frequency to limit the winding AC losses. The windings information are listed in Table 4.4. The proposed designs are compared to two conventional configurations highlighting the impact on the converter performance. Fig. 4.13 shows the parasitic capacitances for the conventional interlaved configuration. There are trade-offs between reducing the eddy current effect by interleaving the layers and increasing the mutual stray capacitance. The stray capacitance forms a resonant tank with the leakage inductance and the auxilary inductance added in the DAB converter as well as in resonant converters. For the same winding, the same capacitance is formed between the turns on different layers as shown in Fig. 4.14. However, the voltage across each capacitance is different due to the voltage drop between the turns. This results in an unequal voltage distribution across the capacitors as illustrated in Fig. 4.14. The energy stored in each capacitor can be obtained and summed up to represent a single intra-winding capacitor. Since the energy of each capacitor is proportional

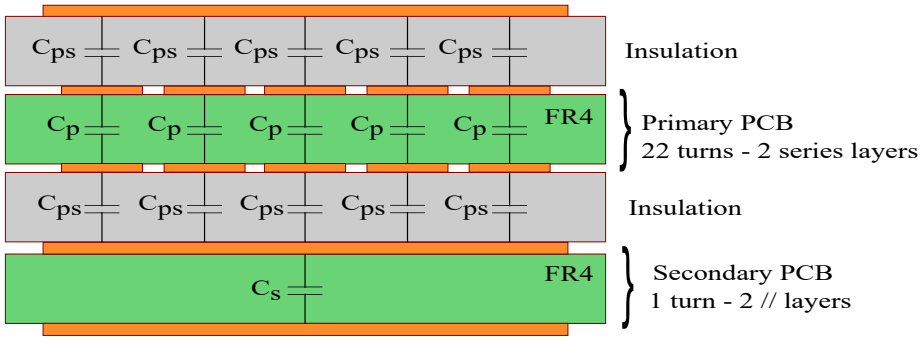

Figure 4.13: Layers capacitances in planar transformers.

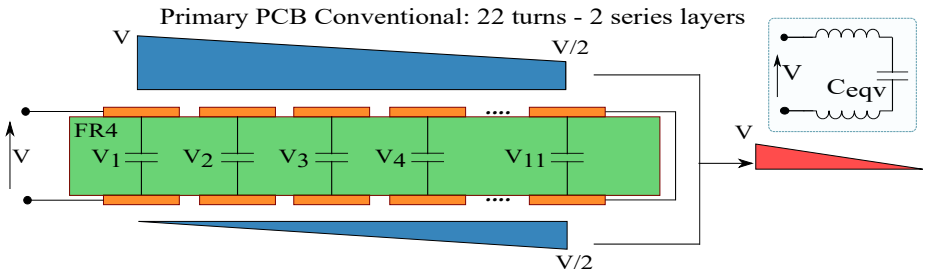

Figure 4.14: Primary winding capacitance for conventional configuration.

with the voltage squared across it, the equivalent capacitor of such configuration is large and causes HFO on the transformer voltage waveforms. The winding equivalent capacitance and stored energy can be expressed as follows [130]:

$$V_i = \frac{(n+1)-i}{n} V, (i = 1, 2, 3, ..., n). \tag{4.3.1}$$

$$\begin{aligned} E_{tot} = \sum_{i=1}^{n} E_i &= \frac{1}{2} C_p V^2 \sum_{i=1}^{n} \left(\frac{(n+1)-i}{n} \right)^2 \\ &= \left(\frac{(n+1)(2n+1)}{12n} \right) C_p V^2. \end{aligned} \tag{4.3.2}$$

$$C_{eqv} = \left(\frac{(n+1)(2n+1)}{6}\right) nC_p. \tag{4.3.3}$$

V_i is the voltage across the individual turns between the PCB layers, V is the overall voltage across the winding, C_p and E_i are the individual capacitance and energy respectively, C_{eqv} and E_{tot} are the equivalent capacitance and energy stored respectively.

Changing the way the turns are routed on the planar PCBs can result in an equal low voltage distribution across the turns capacitance and hence a lower equivalent intra-winding capacitance as illustrated in Fig. 4.15. The MLMG aims to have an equal voltage distribution across all turns capacitances by utilizing blind crossed vias connections between the layers. Fig. 4.16 illustrates the conventional and proposed configurations highlighting the winding connections of the proposed design with the equivalent electrical schematic of the turns. The overall transformer power density is kept the same as the conventional configuration. The board thickness, if required, can be kept the same as the double layers design by reducing the copper thickness of the turns on each layer. The current density is maintained low by increasing the width of turns since lower number of turns are routed on each layer. However, the intra-capacitance is lowered by having equal lower voltage distribution across the turns capacitance of $\frac{V_{winding}}{N}$. Based on the same approach of getting the total energy stored between the layers, the equivalent energy stored and winding capacitance of the MLMG configuration can be expressed as follows:

$$E_{tot} = \sum_{n=1}^{N} E_i = \frac{2}{N^2} C_p V^2. \tag{4.3.4}$$

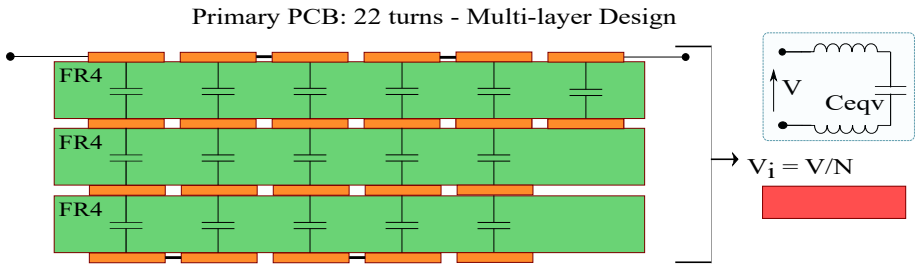

Figure 4.15: Primary winding capacitance for MLMG configuration.

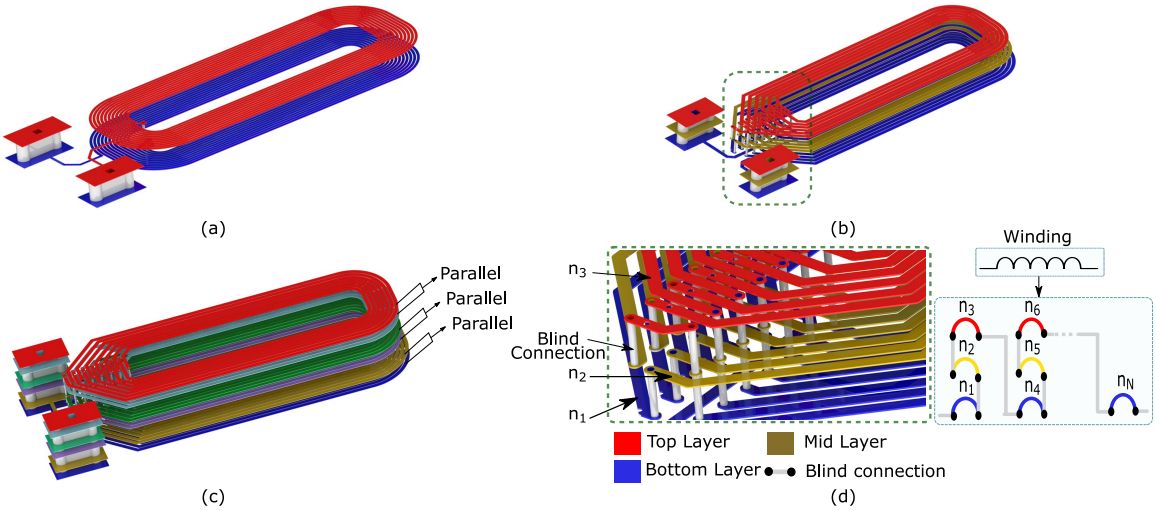

Figure 4.16: Different winding turns configurations: (a) Conventional 2 layers configuration, (b) Proposed MLMG configuration 1 - 3 layers, (c) Proposed MLMG configuration 2 - 6 layers, and (d) Zoomed-in view of the MLMG configuration.

$$C_{eqv} = \frac{2}{N^2} C_p. \tag{4.3.5}$$

Compared to a similar low-voltage distribution conventional two-layers design, the transformer power density is improved by 20%. As illustrated in Fig. 4.13, inter-winding capacitances are also formed between the primary and secondary layers. Reducing the interfaces between the different winding turns results in a lower

lumped stray capacitance. The second proposed configuration, aims to utilize multi-layer configuration to reduce the interfaces between the primary and secondary layers reducing the inter-winding capacitance. Each layer of the 3-layers board is duplicated and connected in parallel to the original layer so that zero voltage is across them. However, the leakage flux between the layers is increased resulting in higher AC losses. This is the trade-off between the transformer losses and lower stray capacitance previously mentioned. Both proposed configurations are compared to the conventional interleaved and non-interleaved configurations in terms of AC losses and stray capacitance.

Even though the non-interleaved configuration has only one interface between the primary and secondary windings and hence lower inter-winding capacitance, it is usually not considered for its high losses. As highlighted, a loss analysis for the different configuration is crucial in the design process while comparing the stray capacitance of each configuration. The inter-winding capacitance between the primary and secondary boards can be reduced as well by increasing the insulation thickness between them; however, this will result in a lower core window utilization and hence higher copper losses.

The insulation between the primary and secondary layers for MEA applications is limited by the Information Technology Equipment Safety standard IEC 60950-1 for voltages below 600 V. The insulation needs to be at least 0.4 mm, when a single-layer insulation is used. While for reinforced insulation (double layers), no specific minimum thickness is required. The used insulation thickness and material affects the inter-winding capacitance. For instance, air has lower permittivity than other insulation materials such as FR4 or Kapton and hence lower capacitance between the

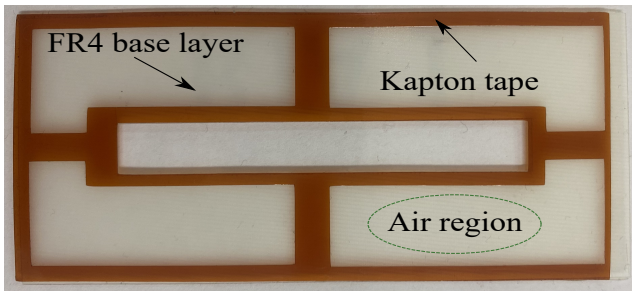

Figure 4.17: Double insulation layers between the primary and secondary windings.

layers; however, the insulation must withstand the breakdown voltage between the layers. A double insulation layers with either FR4 or Kapton as the first layer and air as the second layer will ensure meeting the breakdown voltage requirements as well as MEA standards of using double insulation. This will result in lower capacitance since one of the layers is air instead of FR4 or Kapton. Fig. 4.17 shows the insulation layer; where FR4 material is utilized as the first insulation layer and hollow Kapton tape is used on top to create an air seperation between the windings acting as a second layer. Each of the two layers is of 0.1 mm thickness which ensures meeting the voltage breakdown requirement. This configurations allows for reducing the inter-winding capacitance without increasing the AC losses.

Fig. 4.18 compares between the conventional high-capacitance design, the MLMG design and low-capacitance two-layers configuration. The volume is kept the same with the multilayer design. However, for the conventional two-layers design, in order to reduce the transformer capacitance, the volume of the transformer is increased by 20%.

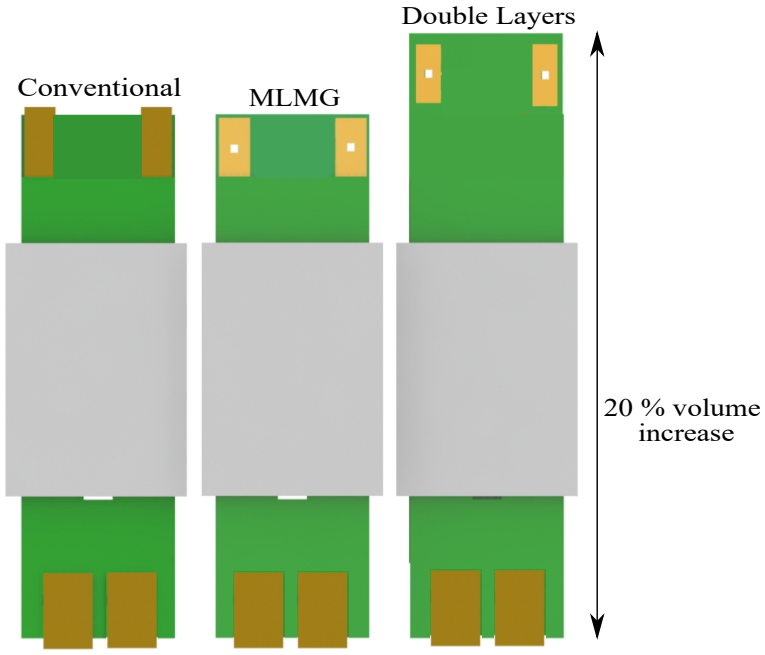

Figure 4.18: Power density comparison - conventional design vs. MLMG configuration.

4.3.2 Transformer loss analysis

The windings configuration and operating frequency highly impact the transformer losses due to the eddy losses which calls for an accurate prediction of the transformer losses to optimize its performance. The non-interleaved windings is often omitted due to the high copper losses caused by the proximity effect. On the other hand, the interleaved configuration exhibit lower copper losses. The MMF distribution of the interleaved layout, illustrated in Fig. 4.19, indicates a low MMF generated in between and inside the layers. This results in a uniform current distribution inside the layers and hence a reduction of the losses caused by the proximity effect [135].

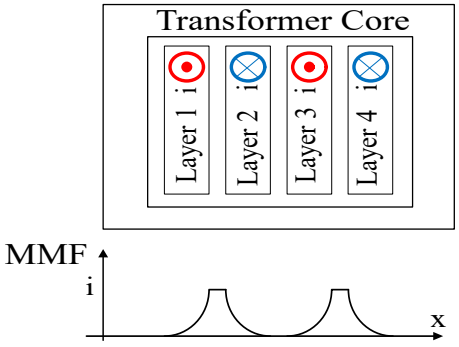

Figure 4.19: MMF diagram of fully interleaved windings.

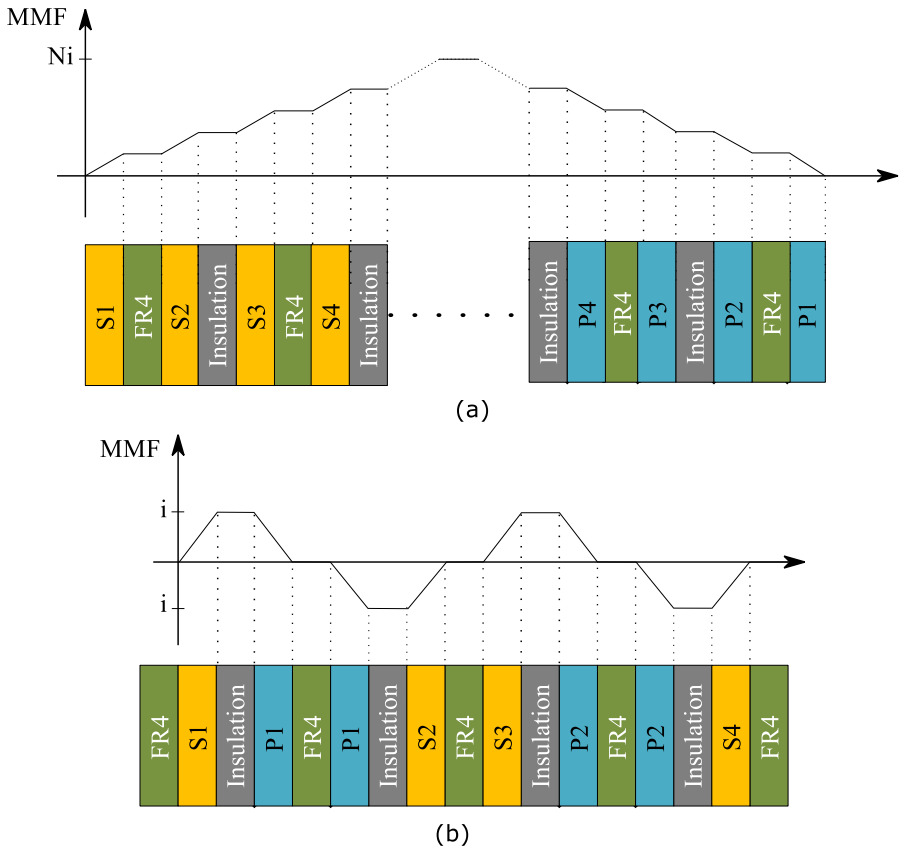

Figure 4.20: MMF diagram for conventional stacking structures. (a) non-interleaved configuration SSSS—PPPP, and (b) conventional fully interleaved configuration SPPSSPPS.

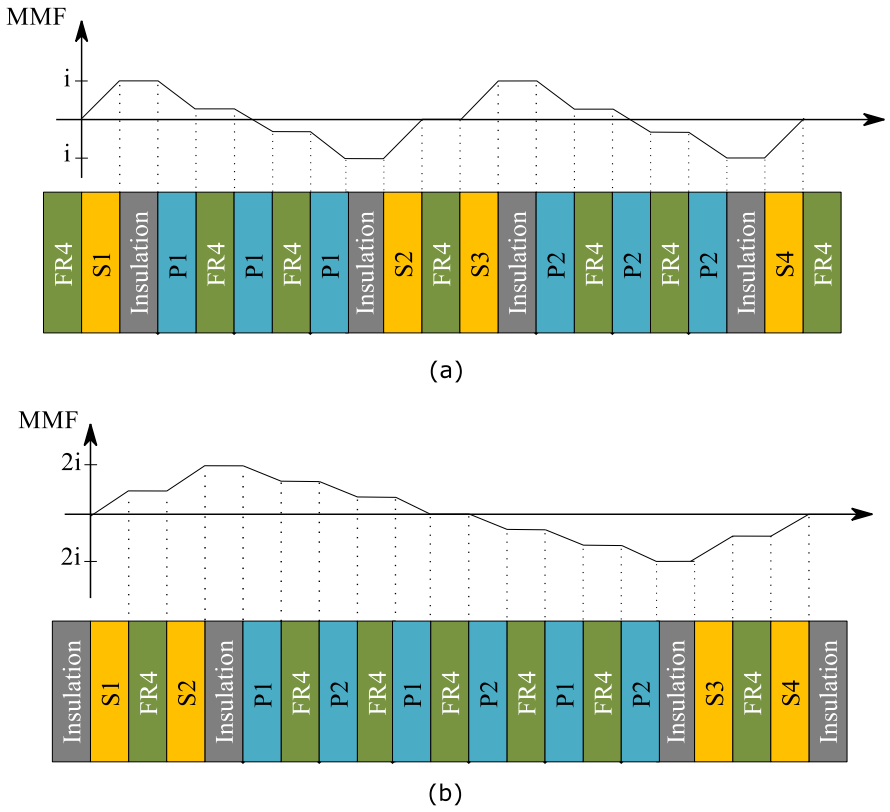

Figure 4.21: MMF diagram for Proposed stacking structures. (a) MLMG 3-layers fully interleaved - SPPPSSPPPS, and (b) MLMG 6-layers semi-interleaved SSPPPPPPSS

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To minimize the winding losses, a copper thickness of equal or less than the skin depth is required [136]. Hence, PCBs are considered for both the primary and secondary windings with 5 oz (175 μm) copper thickness. Different stacking structures are investigated considering both the proposed and conventional configurations. Fig. 4.20 and Fig. 4.21 show the MMF diagram of the conventional configurations and the proposed structures respectively. The proposed 3 layers configuration, shown in Fig. 4.21 (a), has the same MMF amplitude as the conventional fully interleaved winding, illustrated in Fig. 4.20 (a), and hence the same AC/DC resistance ratio. However, the

6 layers configuration, illustrated in Fig. 4.21 (b), is similar to the semi-interleaved configuration with less interfaces between the primary and secondary windings and higher MMF amplitude. The non-interleaved structure, shown in Fig. 4.20, has the highest MMF amplitude and therfore higher leakage flux between the layers resulting in higher AC losses. The analytical calculations based on the analysis presented are compared with FEA results.

4.3.3 FEA validation and noise analysis

Three different winding layouts are simulated in ANSYS Maxwell to validate the low capacitance and minimum voltage gradient between layers for the proposed designs for the primary winding. Since the secondary winding has only one turn, the equivalent intra-capacitance formed between the parallel layers is zero since the voltage across the parallel laters is zero and hence no electric field stored in-between the layers. Fig. 4.22 shows the voltage distribution for a conventional double layer design for the primary side. Half of the turns are implemented on the top layer and the other half on the bottom layer. Unequal voltage distribution across the turns capacitances results in a non-uniform electric field with high strength towards the outer turns. The electric field magnitude reduces to become minimal at the most inner turns. This results in a high total stored energy between the two layers and therefore a higher intra-capacitance.

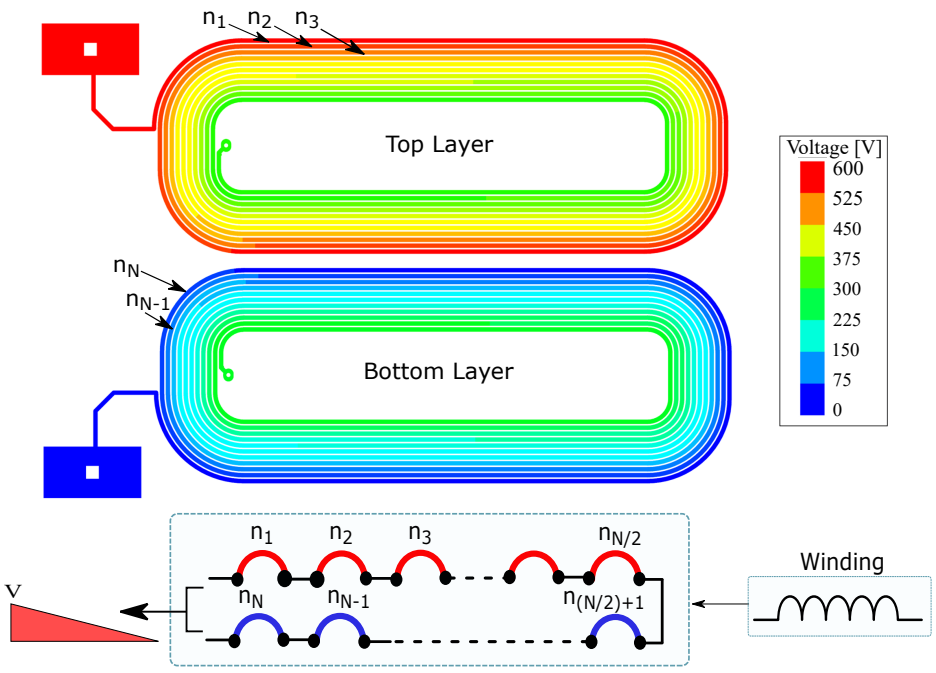


Figure 4.22: Voltage distribution across the turns - conventional configuration.

The voltage distribution of the proposed MLMG design is shown in Fig. 4.23. The voltage gradient between the overlapping turns across all layers is minimized by alternating the turns between all layers. Since three layers are utilized to route the turns, more space is available to increase the turn width and reduce the DC resistance as compared to the double-layers design. The transformer power density is not compromised either by maintaining the width of the PCB as the conventional double-layers layout. A similar double-layers design would require an increase in the boards width and result in a 20% increase in the transformer volume. The voltage distribution of the MLMG 6-layers layout is the same as that shown in Fig. 4.23, since its the same layout but with each layer duplicated and connected in parallel to the original three layers. However with a main aim to reduce the intersections between the primary and secondary windings. Table 4.5 lists the capacitances extracted from

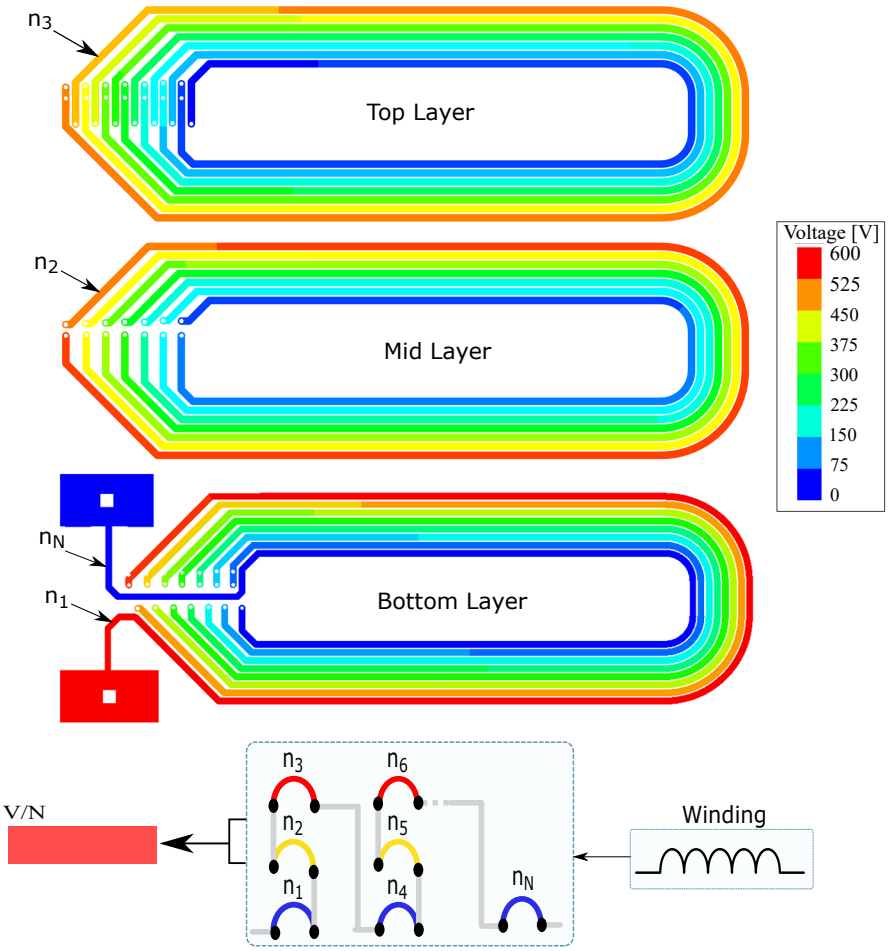


Figure 4.23: Voltage distribution across the turns - MLMG configuration.

the three FEA models and compares the values to the analytical approach.

Two conventional interleaved and non-interleaved configurations are compared to one fully-interleaved MLMG 3 layers design and a semi-interleaved MLMG 6-layers stacking layout. The current density plots of the conventional configurations are shown in Fig. 4.24 and the current density plots of the proposed structures are shown in 4.25. Since the MMF magnitude is highest for the non-interleaved configuration, the layers current density is very high which results in high AC losses. Both the

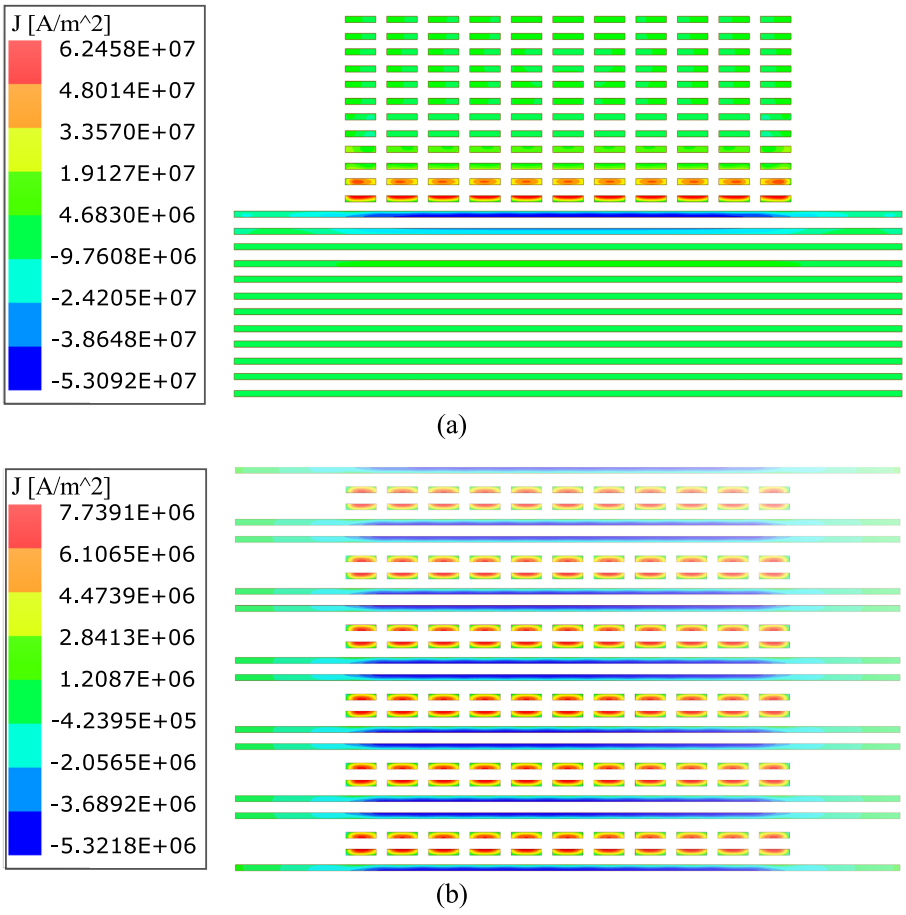


Figure 4.24: Current density plot of conventional configurations. (a) non-interleaved configuration SSSS—PPPP, (b) conventional fully interleaved configuration SPPSSPPS.

conventional and MLMG interleaved configuration exhibit the lowest current density and ac losses. The MLMG stack has better current distribution compared to the conventional stack since the width of the turns is increase to utilize the board space which results in higher efficiency. For the MLMG 6-layers stack, the current density is higher than the 3-layers layout due to the high AC losses caused by the higher MMF magnitude.

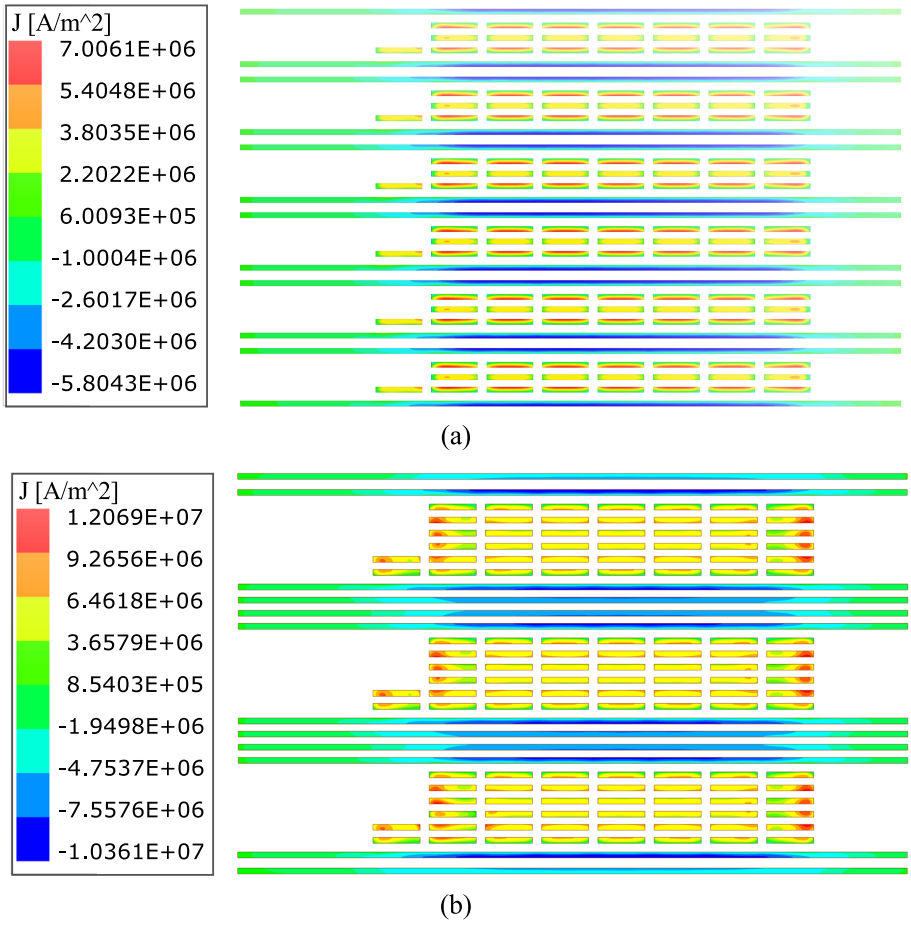


Figure 4.25: Current density plot of proposed configurations: (a) MLMG 3-layers fully interleaved - SPPPSSPPPS, and (b) MLMG 6-layers semi-interleaved SSPPPPPPSS.

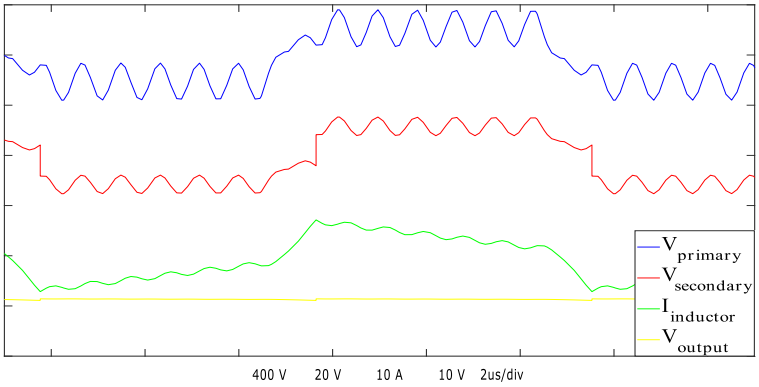
Table 4.5 lists the total copper losses resulted from the FEA as compared to the analytical approach. Since the MLMG 3-layers layout exibits the highest efficiency and low intra-winding capacitance, its transformer performance is analyzed in PLECS and compared to the conventional configuration highlighting the effect on reducing the HFO.

The extracted capacitances and winding AC resistances are imported in PLECS for both configuration. Two series 20 µH inductors, with an 8 mΩ series resistance

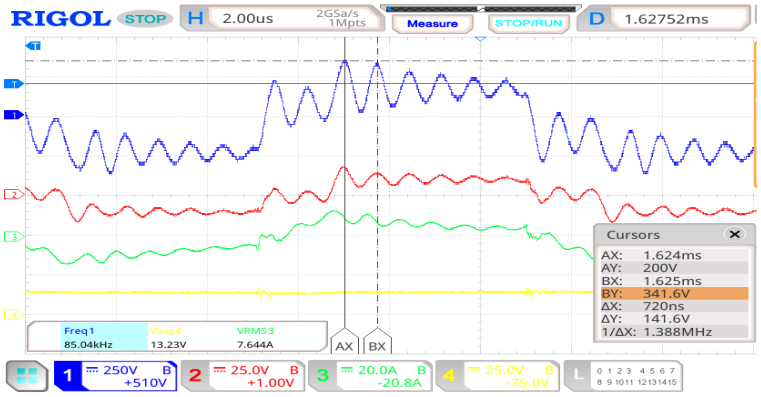
Table 4.5: Simulation vs. Analytical Results.

Configuration	Intra-winding capacitance (pF)		Copper Losses (W)	
	Analytical	FEA	Analytical	FEA
Conventional Non-interleaved	125.4	120	152.57	140.3
Conventional Interleaved	125.4	120	19.93	16.66
MLMG 3-layers	8.29	7.97	15.2	14
MLMG 6-layers	7	6.6	26.26	28.3

each, were used in the converter testing. Two SiC FETs are used in parallel for the HV bridge switches (SCT3160KLHRC11) and six Si devices in parallel for the LV side switches (IPP023N10N5AKSA1). The output capacitance of the MOSFETs, on both the primary and secondary sides, were modeled along with the parasitic series resistance of the added external inductor. The transformer stray capacitance, leakage inductance and windings resistances were added in the PLECS model as well. Fig. 4.26 shows the transformer waveforms for the interleaved configuration both in PLECS and experimentally. The analysis shows a close match in terms of the amplitude and frequency of the oscillations. Fig. 4.27 shows the waveforms in PLECS for proposed configuration. The oscillations are substantially reduced for the proposed design due to the reduction of the parasitic capacitance.



$V_{overshoot} = 140\,V, f_{osc} = 1.388\,MHz]$
(a)



$V_{overshoot} = 160\,V, f_{osc} = 1.35\,MHz]$
(b)

Figure 4.26: Parasitic capacitances effect - interleaved configuration((a) PLECS simulation) and (b) Experimental waveforms.

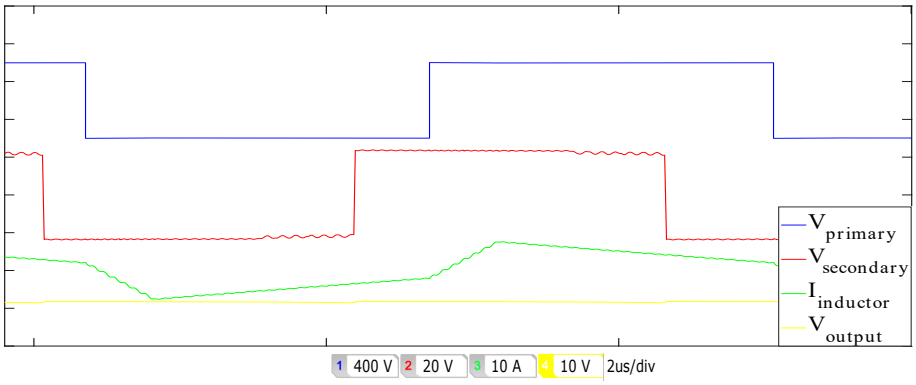


Figure 4.27: Parasitic capacitances effect - MLMG configuration (PLECS simulation).

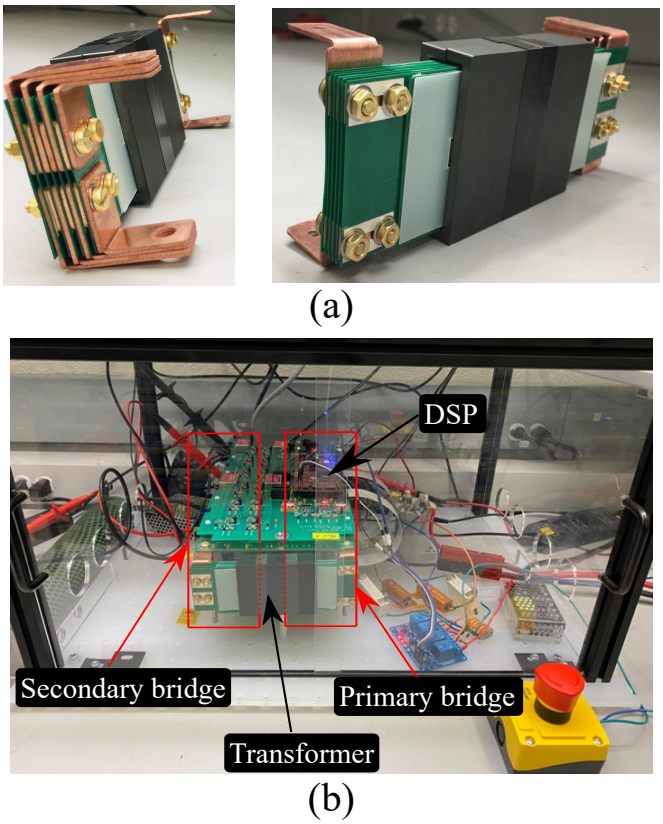


Figure 4.28: Experimental prototype: (a) Transformer prototype and (b) DAB converter platform.

4.4 Experimental Validation

Three transformers were built to verify the design approach. The transformer parts were designed, manufactured and assembled as illustrated in Fig. 4.28 (a). The transformers were assembled with a DAB platform as illustrated in Fig. 4.28 (b). One of the transformers utilizes the MLMG configuration along with double insulation layers; one of which is an air layer. The two other transformers includes double FR4 insulation stack. The manufacturing cost is almost the same for the three prototypes since the same number of PCB layers are used in each. Despite having higher number

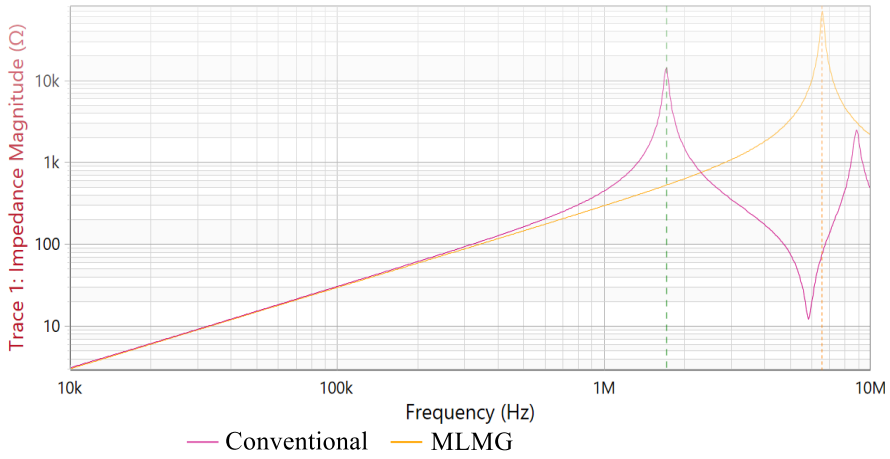


Figure 4.29: Single PCB frequency response - conventional vs. MLMG.

of PCB layers, the MLMG board cost is still the same as the conventional configuration since more space (layers) are available to route the turns which allows for lowering the copper thickness as compared to the conventional configuration. The frequency response of a single layer for both the conventional and MLMG designs is shown in Fig. 4.29. The resonance frequency of the MLMG configuration is higher than the conventional design due to the lower capacitance. This is the case since both designs have the same number of turns, therefore the same inductance and, for fixed inductance, the capacitance ratio of an LC circuit is the square of the resonance frequency ratio. The experimental results shows 15 times $(6.56/1.713)^2$ less capacitance for the MLMG with a close match to the FEA simulations previously listed in Table 4.5.

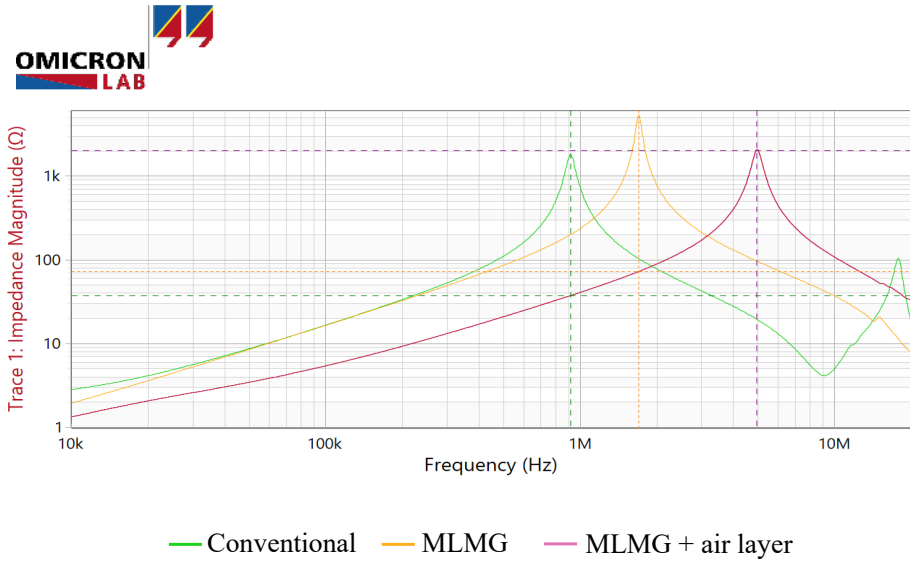


Figure 4.30: Frequency response of transformer stack with shorted secondary.

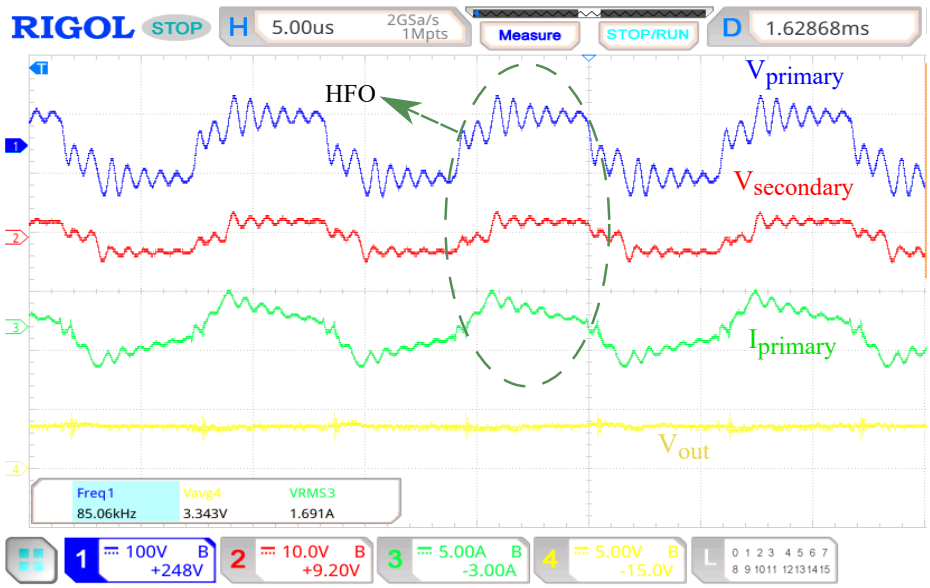


Figure 4.31: Converter performance - conventional structure waveforms.

Fig. 4.30 shows the frequency response for the three assembled transformer for a shorted secondary side emulating a rated-load operation. Both MLMG transformers

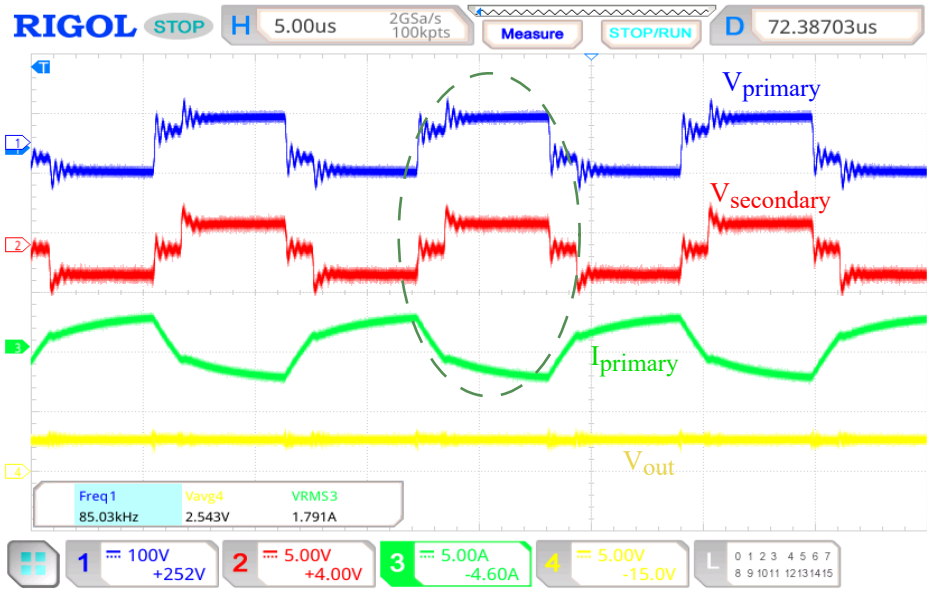


Figure 4.32: Converter performance - conventional structure waveforms.

surpassed the conventional design in-terms of the higher resonance frequency and hence the lower lumped capacitance. The MLMG transformer utilizing an air layer has the highest resonance frequency due to the low inter-winding capacitance. Fig. 4.31 and Fig. 4.32 show the transformer waveforms at light load. By comparing both figures, the HFO are significantly reduced for the proposed design.

The power density is the same for both prototypes since no PCB area is added for the MLMG configuration to achieve low-voltage gradient between the layers which is the main advantage of this multi-layer configuration. The converter is tested at full load with the optimized transformer. The resonant tank behaviour is related to the phase shift of the DAB converter. A higher phase shift will cause a high voltage drop across the external and leakage inductances and therefore alter the oscillations magnitude.

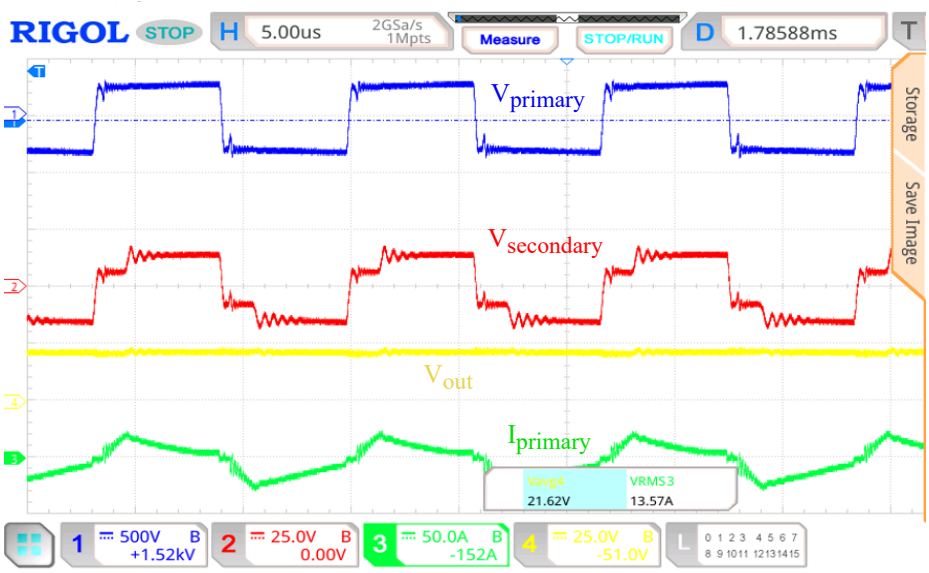


Figure 4.33: Experimental waveforms (4 kW , 300V input, 22V output).

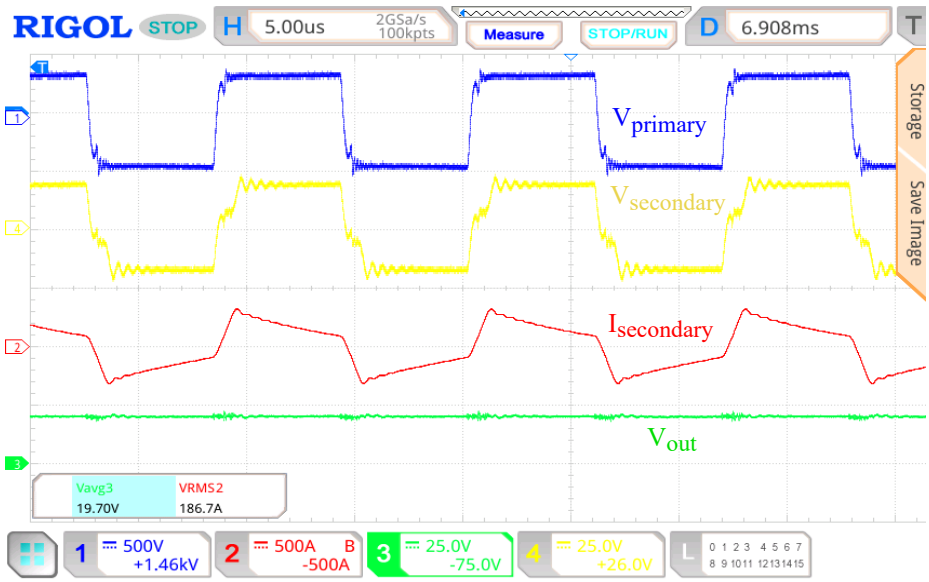


Figure 4.34: Experimental waveforms (3.8 kW , 400V input, 20V output).

The converter is tested at full load and different operating points. This is done to ensure high converter performance at different phase shifts across the operating

range. Fig. 4.33 shows the experimental waveforms of transformer primary and secondary voltages as well as the leakage inductance current at 4kW with 300V and 22V as input and output voltages respectively. The transformer was then tested at the second opeating point at 3.8kW, 400V at the input, 190A at the output side, and 20V. The waveforms of the primary, secondary and output voltages as well as the high secondary current waveforms are shown in Fig. 4.34.

4.5 Summary

In this chapter, a transformer design mehodology was proposed. The optimization algorithm is divided into two main layers: transformer core selection layer and winding optimization layer. The core selection process is based on optimizing the maximum flux density to minimize the overall transformer losses. Different ferrite materials and core paralleling were considered in the process. The algorithm results are combined with the converter loss analysis to select an optimal switching frequency. The optimal switching frequency and selected core are fed to the winding optimzation layer. The effect of the transformer stray capacitance on the converter perfoemance was discussed. The trade-offs linking the winding capacitance to the transformer losses were highlighted. Various winding structure were considered in the design process. The MLMG configurations were proposed as a solution to minimize the transformer layers capacitance. FEA simulations were performed to extract the transformer losses and winding layers capacitance. The FEA results were compared to the analytical analysis. Three winding structures were implemented and tested to validae the optimization concept. The proposed winding structure showed significant reduction in

the winding capacitance as compared to the conventional configuration. The transformers parameters were extracted through an impedance analyzer (Bode 100). The conventional transformer and the proposed transformer were tested with a 4 kW DAB prototype. The MLMG structure showed a significant impact on the transformer waveforms by eliminating the HFO.

Chapter 5

Multi-Source Dual Active Bridge (MSDAB) DC/DC Converter for MEA Applications

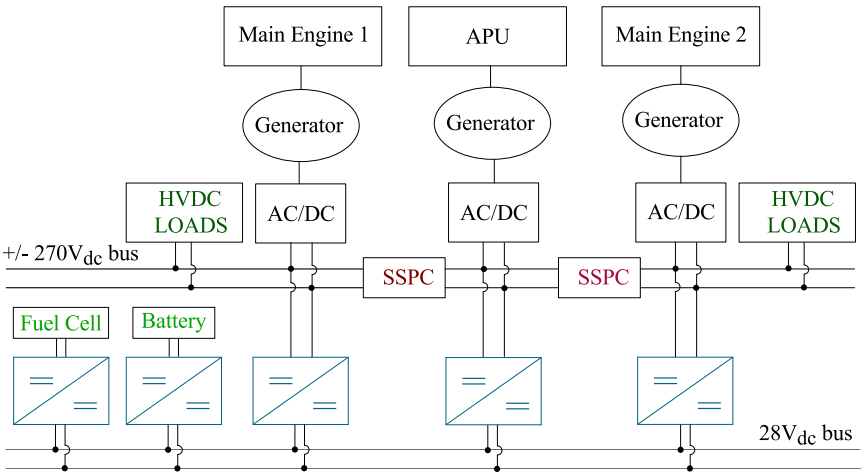


Figure 5.1: Generalized MEA electrical distribution system.

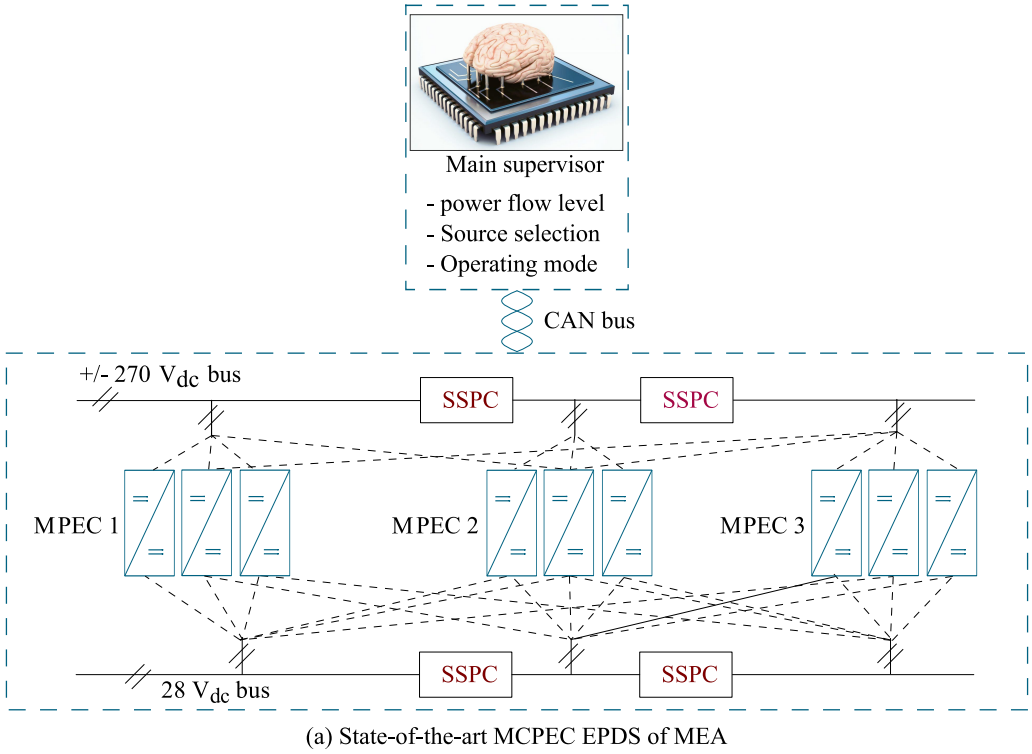
Several derivatives of the basic EPDS have been developed over the years with a dependency on the available power electronics and control technologies [137]. Efforts have been made in the design of compact, lightweight distribution systems while enhancing efficiency and increasing power handling capabilities. Electric power utilization has increased in the modern MEA architectures to replace the traditional mechanical systems. The basic EPDS aboard the aircraft is illustrated in Fig. 5.1 [138]. Two main engines and an auxiliary power unit are connected to generators with AC/DC rectifiers connected at the output of the generators to supply the HVDC bus where solid-state power controllers are used for protection. The HVDC link utilized in modern aircraft architectures provides an internal HVDC link that can be used for equipment such as radars and actuator controllers without the need for a conversion stage. The HVDC bus is then connected to a low voltage bus through multiple step-down isolated DC-DC converters. Other high voltage DC loads are connected directly to the main HVDC bus.

The HVDC EPDS has been of interest among several research groups such as Airbus HVDC project [139], and CleanSky project [140]. The MEA EPDSs are the latest electrification level for commercial aircraft. Conventionally, a single-source DC/DC converter is used to link a power source such as the HVDC bus, batteries, and fuel cells to the low-voltage (28 V) DC network. The distribution system has to include auxiliary sources other than the main engines for emergency and ground operations. Multiple energy storage systems chemistries are utilized such as supercapacitors, batteries, and fuel cells. Each ESS chemistry provides benefits such as lower cost, faster response time, and higher performance. Some of the energy storage systems are connected to the low voltage network through isolated power converters as shown in Fig. 5.1. Conventionally, a kerosene-based APU is utilized to provide emergency power. ESSs are used to provide power from the time the main engines fail till the activation of the KB-APU system. In case of failure of all systems including the KB-APU, ESSs have to supply the rated power for a short period of time. In compliance with the MIL-STD-704 standard, all power characteristics in emergency operation shall be the same as normal operation. Batteries and other independent ESSs should also be able to supply power for 30 minutes in an emergency state. Before the aircraft takes off, ground operation relies entirely on the KB-APU and ESSs when the main engines are shut off. The efficiency of a conventional KB-APU on the ground is very low which contributes the most to the emissions of airports. For the conventional systems, the ESSs are sized to supply power before the KB-APU takes over. This results in a very bulky system which forms 40% of the overall distribution system weight [141].

More electric technology can be achieved by replacing the traditional kerosene-operated turbine APU with a fuel cell system-based APU. This technology has been

adopted recently due to strict emission regulations in airports while also promoting higher overall distribution system efficiency. Using fuel cells and batteries instead of or along with the KB-APU system reduces the system size required for ground and emergency operation. A more-electric configuration includes multiple energy sources/loads which calls for integration of the isolated DC-DC converters to improve the power density of the EPDS of the aircraft. Each section of the distribution system needs to be able to supply the peak power. The KB-APU along with the ESSs are sized to supply the rated power required in normal operation. This results in over-sizing the system since not all sources supply the peak power at the same time. Considering the conventional configuration of the EPDS, the isolated DC-DC converters are oversized.

Other architectures have been developed for improved integration of the different energy sources aboard the aircraft and the low-voltage network [142, 143]. A derivative of the architecture shown in Fig. 5.1 is the flexible modular power electronic converters architecture, shown in Fig. 5.2, where several isolated bidirectional DC/DC converters are connected in parallel [38]. Each low-power converter is considered a bidirectional cell and can be connected to any of the main primary HVDC buses. The MPECs architecture provides flexibility and fault tolerance since all cells can operate in a modular parallel approach. The EPDS of the MPECs architecture can be considered as a micro-grid where an online supervisor controls the power flow of the modular converters. Control optimization of the modular converter can lead to a significant reduction in the system volume and weight. The MPEC approach allows for a reduction in the size of the isolated DC-DC converters supplying the LV network, since lower-power paralleled DC-DC converters are utilized with access



(a) State-of-the-art MCPEC EPDS of MEA

Figure 5.2: Modular power electronic converters architecture.

to all HVDC links and battery/fuel cell terminals. A main supervisor is responsible for controlling the power flow between the paralleled converters. A multi-source isolated DC/DC converter is proposed in this chapter following the MPECs approach of paralleling multiple low-power modules. The multi-source topology allows for power flow between the different energy sources/DC links. This can be realized through a similar approach as the MPECs, by having multiple parallel multi-source isolated DC-DC converters where power flow between the input terminals can be controlled. The power can be supplied to the LV network through either of the connected sources or through splitting the power between the different sources.

The proposed MSDAB topology is introduced in Section 5.2 based on the conventional DAB converter. The importance of multi-source integration is highlighted

in this section. A design comparison to the conventional approach, considering the different modes of the MSDAB topology, is carried out. The switching schemes for the different operating modes are presented in Section 5.3.

5.1 MPECs Approach and Proposed Multi-source DC-DC Converter

This section presents the realization of MPECs architecture through the proposed MSDAB topology. The different modes of operation are discussed and compared to the conventional architecture. Galvanic isolation has to be maintained between the HVDC buses and the LVDC (28 V) network following the MIL-STD-704 standard. However, the output of the main generators and APU are directly connected to either separate HVDC links or a single HVDC bus. SSPCs are used as electrical non-isolated power interrupters in case of faults. As stated in the MIL-STD-704, AC inputs cannot be paralleled; however, DC sources can be paralleled with blocking diodes added for protection. The developed architecture has to comply with the isolation and protection requirements stated in the MIL-STD-704 standard. Better converters utilization can be achieved through several multi-source DC-DC converters connected in parallel. This allows for power flow between the different energy sources/DC links whilst supplying power to the LV bus, which increases the stability of the system in case of voltage sag in one of the energy sources. The power can be supplied to the LV network through either of the connected sources or through splitting the power between the different sources. Fig. 5.3 (b) shows the realization of the MPECs architecture with two input sources connected through the proposed MSDAB topology

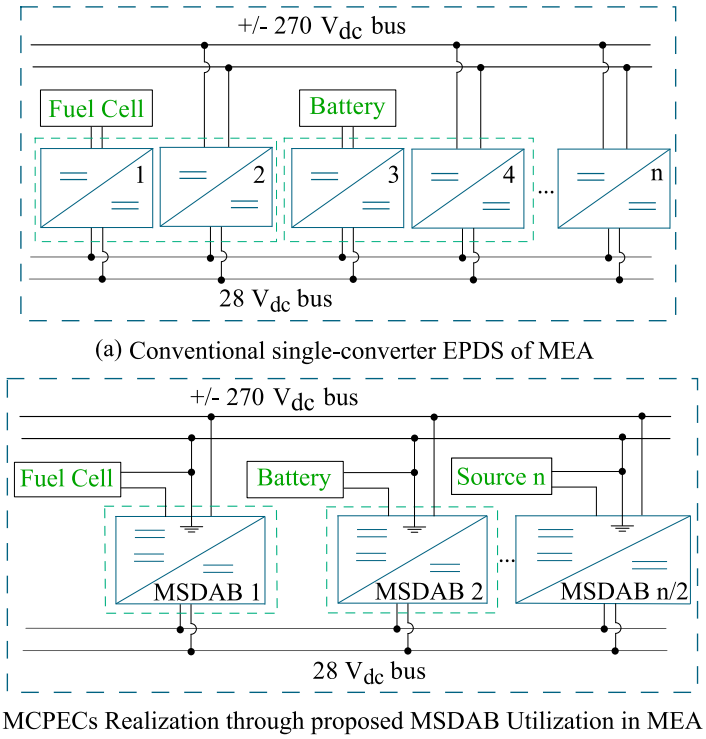


Figure 5.3: Architecture comparison: (a) Conventional single-converter EPDS. (b) MPECs realization through proposed MSDAB utilization in MEA EPDS.

as compared to the conventional approach illustrated in 5.3 (a). The power can be shared between the different sources while maintaining galvanic isolation between the HV sources and the LV network. Compared to the conventional structure, the number of converters is halved in the case of utilizing MSDABs. The MSDAB topology allows for power flow between the different energy sources/DC links, which can help to increase the stability of the system. This can be realized through a similar approach as the MPECs, by having multiple parallel multi-source isolated DC-DC converters where power flow between the input terminals can be controlled. The power can be supplied to the LV network through either of the connected sources or through splitting the power between the different sources.

In the conventional EPDS, the isolated DC/DC converters connected to each of the HVDC buses are sized at the full rated power. The multi-source topology allows for a system size reduction as compared to the conventional configuration since power is split between all the sources and not all sources are required to supply the full power at the same time. For instance, the auxiliary batteries mainly supply power in ground operation or during an emergency, but conventionally a full-power converter is connected to each of the sources even though at some point some of these converters are not operating. This results in poor system utilization, which can be improved if those different sources had access to the same converters forming a multi-source architecture.

The different paralleled multi-source converters can be controlled by the main supervisor in a similar manner to the MPECs approach. Additionally, the power flow between the different sources can be controlled as well through the multi-source topology. Constant power needs to be supplied to the LV network and hence in case of voltage sag of any of the connected sources, a higher current is drawn to fix the delivered power which affects the system stability. In case of a voltage sag of the HVDC link, the power delivered from the HVDC link can be reduced and batteries, fuel cells as well as the APU can provide more power through the multi-source converter. The batteries can be used as well to regulate the HVDC voltage by controlling the multi-source converter as a boost converter. The distribution system can be further optimized by determining the number of multi-source converter cells to be paralleled and investigating how the sources will be distributed among the cell terminals while considering the power supplied by each source.

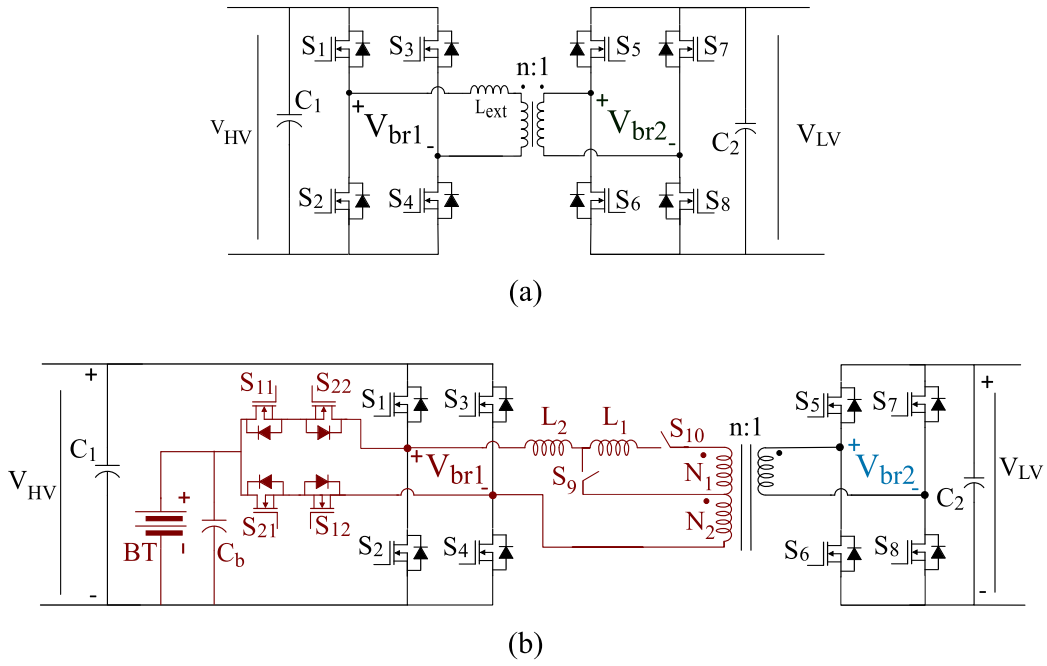


Figure 5.4: Topological schematic comparison. (a) Conventional DAB schematic. (b) Proposed MSDAB topology schematic.

5.1.1 Multi-source dual active bridge (MSDAB) converter structure vs. conventional DAB configuration

The DAB converter is the most commonly used converter topology in MEA application. This is due to the features offered by the DAB converter, such as high efficiency, zero voltage switching capability, and controllability. The topology is shown in Fig. 5.4 (a), where an inductor (L_{ext}) is added between the HV bridge and the isolating transformer known as the external leakage inductor. The operating principle of the converter is discussed in detail in [144, 145]. A multi-source derivative of the DAB converter is proposed in this chapter and is shown in Fig. 5.4 (b).

The advantage of the MSDAB in terms of improving the system power density lies

in the reduction of the number of transformers required as well as the secondary high-current switches and thermal management system. Even though the number of the primary switches is increased, 75% of the converter volume can be attributed to the transformer and the secondary side thermal management, high-current output filter and busbars assembly. In case of the MSDAB, a single converter is required instead of two in the conventional case, which results in lower number of required magnetic elements and secondary sides. However, to achieve a split power mode between the two sources, an additional MSDAB is required, but in this case the converters are rated at half the power so that each contributes half of the required power by the LV network. This results in two MSDAB converters with half the power each as the conventional approach, but with added switches on the primary side which do not propose a design challenge due to the low current on this side. However, halving the required power by the transformer and secondary side and hence reducing the transformer and secondary side current levels lead to a substantial improvement in the system power density.

The same transformer as the conventional structure can be used in the MSDAB topology with an added termination to the turns to form a centre-taped configuration. The same design concept to lower the capacitance is applicable in the MSDAB case. The primary turns needs to be sized to handle the worst case current in both main operating modes. However, since the current is low on the primary side as compared to the secondary, increasing the winding trace width or thickness do not introduce a challenge on this side. Since the same power is considered for both operating modes, the same core can be used in both cases. Even though the current is increased in the battery mode due to the reduction in the input voltage, the number of turns is also

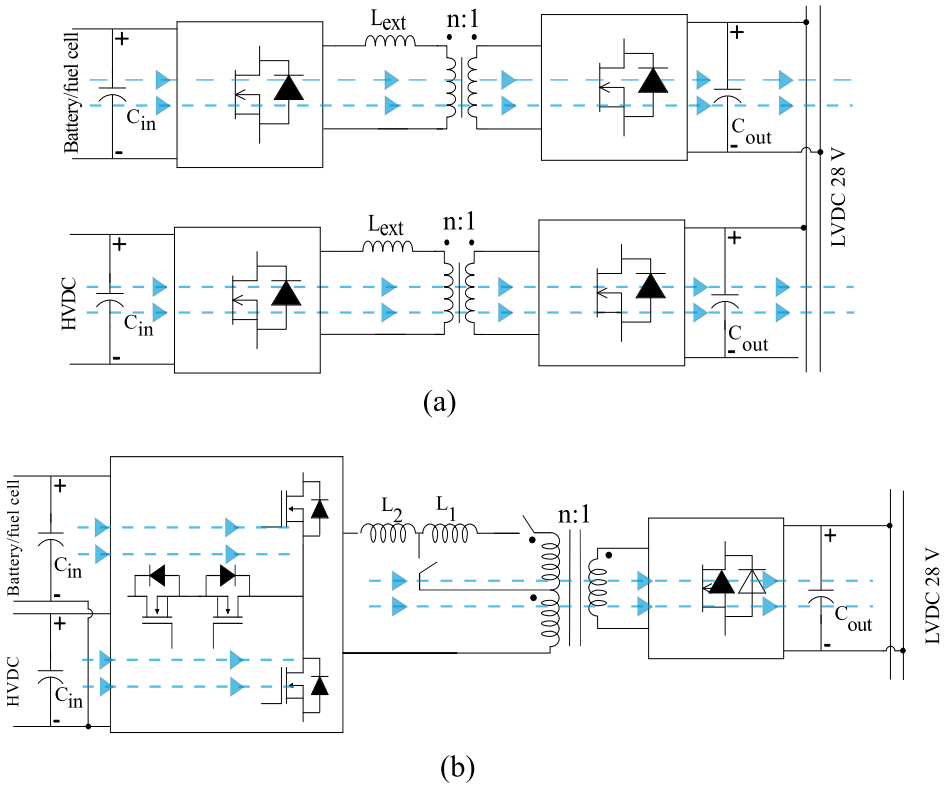


Figure 5.5: DC/DC converters configuration. (a) Conventional dual converters configuration. (b) Single multi-source configuration

lowered in this mode, which results in almost the same maximum flux density which is selected to avoid core saturation.

Conventionally, each DC-DC converter is connected to the two HVDC links generated from the two main engines, or the APU HVDC link have to be sized at the rated power which results in an oversized system. Fig. 5.5 shows the conventional configuration of the DC-DC converters in the MEA architecture vs. the proposed multi-source structure. Fig. 5.5 (a) shows two converters which are supplied by a separate source and rated at full power. Alternatively, as shown in Fig. 5.5 (b), a single MSDAB can be used with two sources connected at the input side. Two lower power input-parallel-output-parallel converter units of the MSDAB can be considered

to realize the MPECs structure allowing power split between the two sources. The modular parallel approach provides control flexibility and increased system reliability. The MSDAB delivers the same power as the two paralleled conventional converters preventing over-sizing of the distribution network. Two energy sources, the HVDC link, and the auxiliary 300 V battery/fuel cell are considered in this paper to illustrate the operating principle of the multi-source topology. Considering different voltage levels for the connected sources, the transformer turns ratio can be actively changed based on the operating mode. This is achieved by adding a tap changer to the transformer where some of the transformer turns can be bypassed in case of a lower input voltage. As shown in Fig. 5.4 (b), there is an additional switch added to the conventional topology, labelled S_9, which bypasses some of the transformer turns as well as part of the added external inductance. S_{10} is also added to avoid shorting the transformer during the battery mode. Both S_9 and S_{10} can be realized using a double pole double throw relay (DPDT) relay. Since the two switches are either on or off, no modulation is required for them and relays can be used to lower the number of required gate drivers, avoid a thermal management system and reduce the control complexity. This is added to have different optimized turns ratios and external inductance for each of the input sources. Power split between the two sources is achieved as well with the proposed structure. Two bidirectional switches are added to connect the second source to the primary side winding terminals. A switch (S_9) is placed across a portion of the primary transformer winding (N_1) to actively control the turns ratio. The placed switch (S_9) also bypasses a portion of the external inductance (L_1) for optimized ZVS operation in different operating modes. The transformer is configured as having a center-tapped winding on the primary side.

The reason for the center-tapped configuration is that the HVDC bus voltage (540 V_{dc}) is almost twice the battery voltage (300 V), so that the converter would not be optimal if the same turns ratio and external inductance are used for both sources.

Table 5.1: Topology comparison - proposed MSDAB vs conventional DAB

Topology comparison		Devices		Magnetics	
		# Switches	Switch rating	# External inductors	# Transformers
Proposed MSDAB	Primary	10	$V_{HV} * I_{HV}$	2	1 (tap changer)
	Secondary	4	$V_{LV} * I_{LV}$		
Conventional	Primary	8	$V_{HV} * I_{HV}$	2	2
	Secondary	8	$V_{LV} * I_{LV}$		

5.2 Multi-source Dual Active Bridge (MSDAB) Modes of Operation

There are four main operating modes for the proposed converter; mode 1: supplying power to the LV network through the HVDC link, mode 2: supplying power from the battery/fuel cell (source 2) to the LV network, mode 3: regulating the HVDC bus voltage in case of voltage sag by controlling the power flow from the battery to the HVDC bus, and mode 4: charging the battery from the HVDC bus. In each mode, the converter switches are modulating to control the power flow in the required direction. The control flexibility of such a system is improved as compared to the conventional structure since the power can be controlled between the sources as well as the power supplied to the LV network. For the proposed structure, only one mode can be achieved at a time; for this reason, a lower-power paralleled converter is beneficial since each converter can be controlled by the main supervisor to provide power in the required direction.

The LV network can be supplied from the HVDC bus by turning off the additional bidirectional switches (S_{11}, S_{22}, S_{21}, and S_{12}), added for the second source. All transformer turns ($N_1 + N_2$) are utilized in that case to step down the HV to the lower voltage side. The generalized diagram of the HVDC mode is illustrated in Fig. 5.6 (a). The switching scheme of this mode is shown in Fig. 5.6 (b). The second mode of operation, shown in Fig. 5.7 (a), is when the converter is supplied from the battery. This is achieved by activating the two added bidirectional switches as well as the switch across a portion of the transformer's primary windings (N_1) as illustrated in Fig. 5.7 (b). This configuration is similar to the conventional DAB topology,

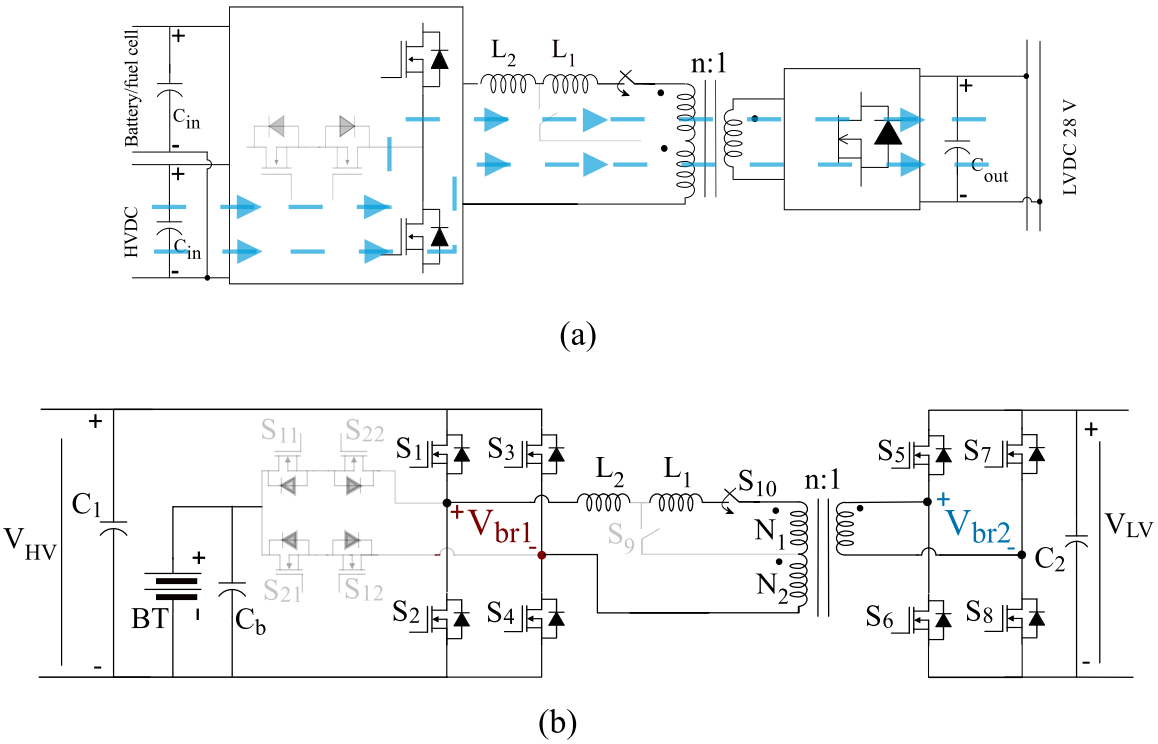


Figure 5.6: HVDC mode of operation. (a) Converter block diagram in the HVDC mode. (b) HVDC mode switching scheme.

and the same control principles of the DAB converter can be applied to control the power flow to the LV side. The bidirectional switches (S_{11}, S_{22} and S_{21}, S_{12}) are added to prevent the power flow from the HVDC link to the second source. Since the voltage is higher for the HVDC link than that of the battery, if a single switch is added, power will flow between the two sources through the body diode of the FETs. MIL-STD-704 mandates that blocking diodes must be added in case of using different DC power sources in parallel, which is the case in the proposed structure. For these reasons, an additional power switch is added in a bidirectional manner for protection. As illustrated, both the transformer turns ratio and added external inductance in the HVDC mode are higher than the battery mode, since the bypassing switch (S_9) is off. This comes from the requirement for a higher stepping down ratio in the case of the

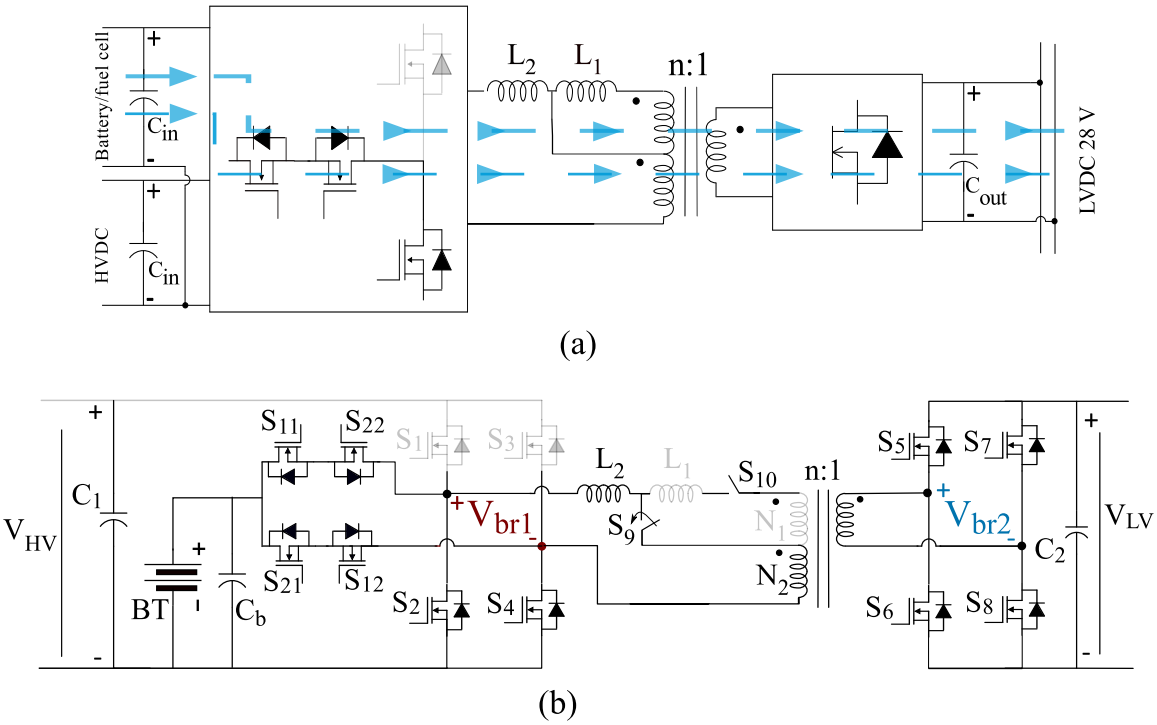


Figure 5.7: Battery mode of operation. (a) Converter block diagram in the battery mode. (b) Battery mode switching scheme.

HVDC operation. Furthermore, a split-power mode can be achieved by having two low-power converters in parallel where each is connected to an MSDAB converter.

Either both converters are supplied from the HVDC/battery, or power is split between the two sources through both converters. The MSDAB converter has two additional modes that are not possible with the conventional approach: bus regulation mode and battery charging mode. The battery charging mode is when power is supplied from the HVDC link to the battery. A conventional CC-CV charging algorithm can be implemented as shown in Fig. 5.8 (a), where the magnetizing inductance along with the added external inductance is utilized as a filter. The switching scheme of the battery charging mode is illustrated in Fig. 5.8 (b), where the converter is modulated as a buck converter. Similarly, in the case of voltage sag in the HVDC

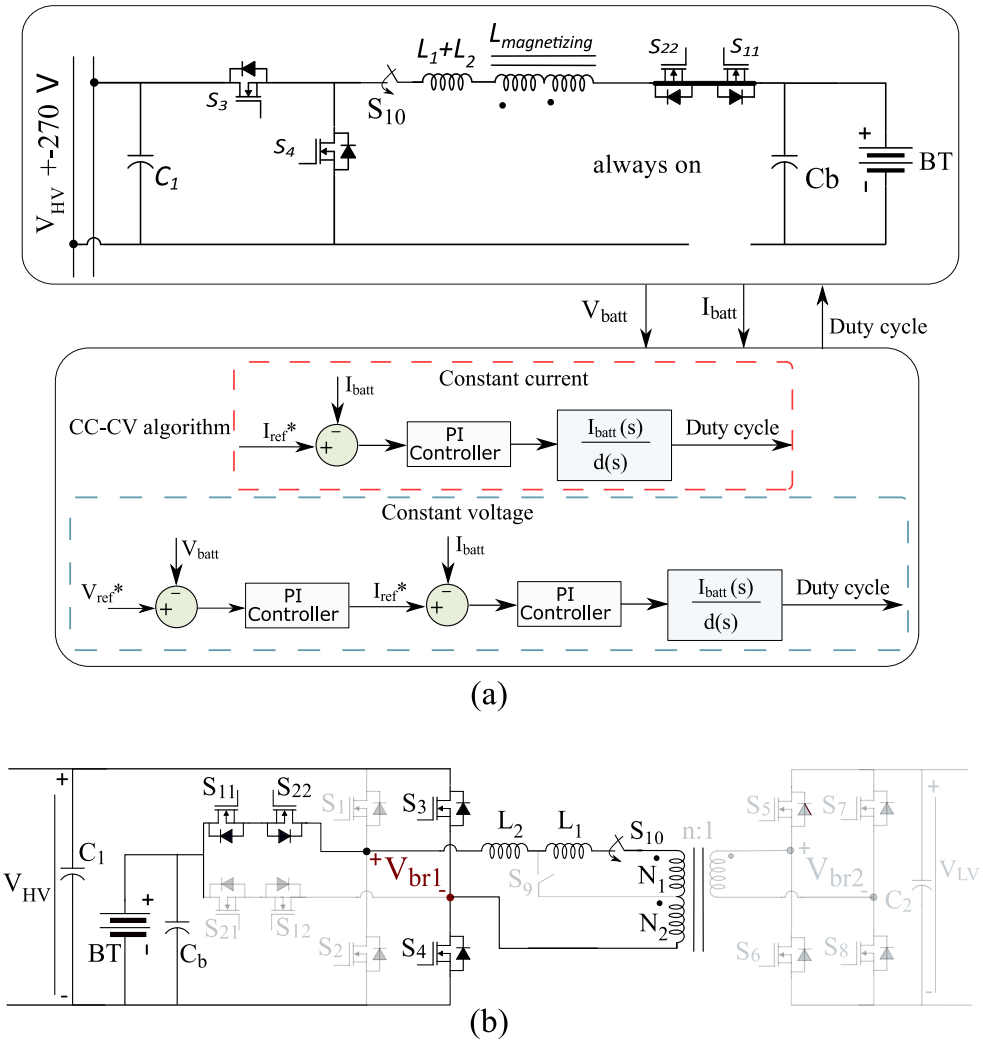


Figure 5.8: Battery charging operating mode: CC-CV charging algorithm

bus, the battery can be used to stabilize the bus voltage, by using the same switches as in the battery charging mode as shown in Fig. 5.9. In this case, the converter is configured as a boost converter and the magnetizing inductance along with the external inductor are used as a filter. The battery charging and the bus regulation modes eliminate the need for external circuitry to perform bus stabilization or battery charging. Having multiple parallel low-power MSDAB converters allows for more flexibility for the controller to select different modes for each converter. Where some

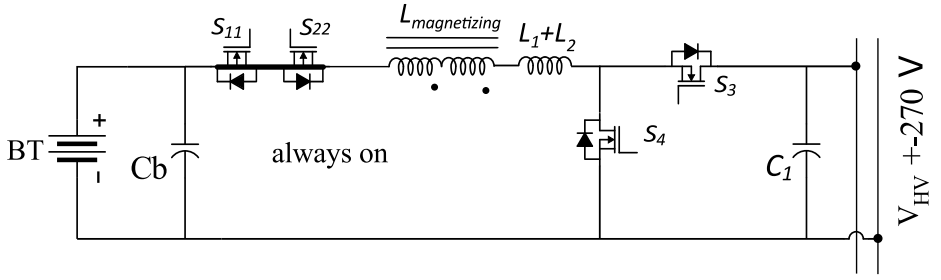


Figure 5.9: Simplified schematic of the HVDC Bus regulation operating mode.

converters will permit power split between the two sources and other converters can be used for bus stabilization in case of voltage sag.

5.3 Summary

In this chapter, the trend towards adding more energy sources aboard the aircraft has been highlighted. The mandatory standards for emergency operation results in an oversized distribution system. Multi-port and multi-source configurations have the potential to decrease the number of required DC/DC converters in the distribution network. A multi-source topology based on the conventional DAB converter has been proposed. The MPECs architecture can be built utilizing the proposed MSDAB configuration. The different modes of operations of the topology increase the reliability and system utilization of the converters network. The topology allows for power transfer between the input energy sources which is not achievable by the conventional structures. Battery charging and bus regulation modes are achievable with the proposed topology without added converters to the network.

Chapter 6

Design, Control, and Performance Optimization of MSDAB DC/DC Converter

This chapter goes through the modelling, design guidelines and control optimization process of the proposed MSDAB converter. The process is split into two optimization layers; the first is to determine the values of N_1, N_2, L_1, and L_2. The second optimization layer is to determine the values of the optimized phase angles at several operating points for both the HVDC and battery operating modes. The angles optimization is carried out based on the triple-phase-shift control technique.

The high turn ratio amplifies the effect of the system's stray inductance and alters the converter operation. The stray inductance elements include the switching devices' lead inductances, PCB tracing, connectors, and busbars. To provide high efficiency, multiple switching devices in parallel are often required on the LV side of the converter since the current on this side is high. A stray inductance network of the parallel devices is required to complete the optimization analysis. In the DAB converter, an external inductor is added to control the power transfer between the two HV and LV sides. The reflected stray inductance value along with the transformer leakage inductance is considered the minimum inductance that can be utilized, and any additional required inductance needs to be added externally. The first design step for the DAB converter is to specify the required transformer turns ratio (N) and external inductor (L_{ext}). In this section, the converter PCBs and connectors are modeled in Ansys Q3D and the resultant inductance network of the paralleled MOSFETs structure is extracted and fed to a genetic-algorithm based optimization technique to determine the required turns ratio and inductor value. The algorithm is based on mathematically modeling the DAB converter through Fourier expansion of the leakage current and bridge voltages. The selection of N and L_{ext} of each operating mode (HVDC mode and battery mode) is based on having different operating points and

assigning a weighting factor for each. The attained N and L_{ext} are then fed to another optimization layer to determine the phase angle based on a TPS control technique to minimize the RMS transformer current. The process for both optimization layers is carried out at various power and voltage levels.

6.1 MSDAB Converter Modelling

The optimization process is based on a developed generalized model for the DAB converter based on the Fourier transform. There are several control techniques presented in the literature for the DAB converter. The simplest control technique for the DAB converter is phase-shift control where signals for both primary and secondary switches are phase shifted, with a fixed 50% duty cycle, controlling the power flow in either direction [49]. Several DAB control techniques have been introduced in literature based on phase shifting the signals fed to the primary and secondary bridges legs [50, 98, 99]. The proposed modelling and optimization algorithm is based on the triple phase shift technique, which can be considered as a generalized modulation technique for the DAB converter.

The MSDAB converter configuration in the two main modes, where power is supplied to the LV network from either the HVDC bus (HVDC mode) or from the battery (battery mode), can be simplified as shown in Fig. 6.1. The MSDAB converter in these two modes acts as the conventional DAB converter; however, with different switching devices being modulated in each mode. The main differences between the two modes are: having a different input source connected at the input side, different external inductance, and transformer turns ratio for each mode. The DAB converter operation relies on the DAB inductor to transfer power in a bidirectional manner.

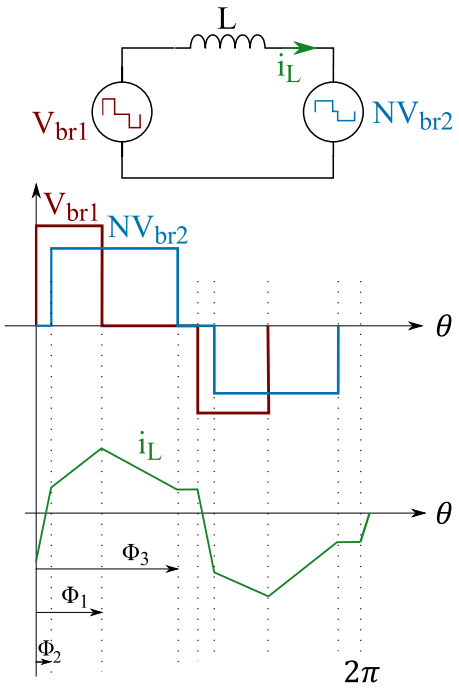


Figure 6.1: Simplified dual-active bridge model.

The primary and secondary bridges can be modelled as two square-waveform generators on both sides of the inductor. The basic converter waveforms are shown in Fig. 6.1 for the TPS control algorithm. The inductor current can be formulated through the simplified MSDAB model as follows:

$$i_L = \frac{(V_{br1} - NV_{br2})}{Z_L}, \tag{6.1.1}$$

where V_{br1} is the primary bridge voltage, N is the primary to secondary transformer turns ratio, V_{br2} is the secondary bridge voltage, and Z_L is the inductor impedance. The Switching waveforms of V_{br1} and V_{br2} can be expressed as follows,

$$V_{br1}(\theta) = \begin{cases} V_{\text{in}}\,, & 0 < \theta < \phi_1 \\ 0, & \phi_1 < \theta < \pi \\ -V_{\text{in}}\,, & \pi < \theta < (\pi + \phi_1) \end{cases}$$
$$V_{br2}(\theta) = \begin{cases} V_{\text{out}}\,, & \phi_2 < \theta < \phi_3 \\ 0, & \phi_3 < \theta < (\phi_2 + \phi_3) \\ -V_{\text{out}}\,, & (\phi_2 + \phi_3) < \theta < (\pi + \phi_3) \end{cases} \tag{6.1.2}$$

Where V_{in} is the converter input voltage, V_{out} is the output voltage on the LV side, and ϕ_1, ϕ_2 , and ϕ_3 are the phase angle as illustrated in Fig. 6.1.

Both V_{br1} and V_{br2} can be expressed in the form of a Fourier expansion as in (6.1.3):

$$\mathrm{V}(\theta) = v_0 + \sum_{K=1}^{\infty} \left[v_{an} \cos(K\theta) + v_{bn} \sin(K\theta) \right], \tag{6.1.3}$$

where K is the harmonic order.

The bridge voltages, V_{br1} and V_{br2}, can be expressed in the expanded Fourier form as in (6.1.4):

$$\begin{aligned} V_{br1}(\theta) &= \sum_{K=1,3,5,....}^{\infty} \frac{4V_{in}}{K\pi} \sin(\alpha) \cos(K\theta - \alpha) \\ V_{br2}(\theta) &= \sum_{K=1,3,5,...,}^{\infty} \frac{4V_{out}}{K\pi} \sin(\beta) \cos(K\theta - \alpha - \epsilon), \end{aligned} \tag{6.1.4}$$

where $\alpha = \dfrac{K\phi_1}{2}, \beta = \dfrac{K\left(\phi_3 - \phi_2\right)}{2}$, $\epsilon = K\phi_f$, and ϕ_f is the phase shift between the fundamental components of V_{br1} and V_{br2}.

By plugging (6.1.4) into (6.1.1), the inductor current can then be expressed as in

(5):

$$i_L(\theta) = \sum_{K=1,3,5,\dots}^{\infty} \frac{2V_{in}}{K^2\pi^2 L f_{sw}} [\sin(\alpha)\sin(K\theta - \alpha - \pi/2) - d\sin(\beta)\sin(K\theta - \alpha - \epsilon - \pi/2)], \tag{6.1.5}$$

where d is the converter gain and equals to $\frac{NV_{out}}{V_{in}}$, and f_{sw} is the switching frequency.

The generalized inductor formula is used in the two-layer optimization algorithm. The algorithm objective is to minimize the RMS inductor current. Since the current on the LV network side is high, minimizing the RMS current is considered as the algorithm objective to optimize the efficiency. The RMS value of the inductor current is obtained numerically using MATLAB by implementing Eq. 6.1.5. The inductor current is a function of N, L_{ext}, and the three phase shift angles. SPS is considered in the first layer of the optimization to select the optimal turns ratio and external inductor value for each operating mode separately.

6.2 MSDAB Converter Design and Control Optimization

The MSDAB converter specifications are listed in Table 6.1. Since the transition ratio between the HVDC bus to the LV bus is high, a transformer with a high turns ratio is required. The high turns ratio increases the effect of the stray inductance on the secondary side, altering converter operation. This is particularly important in high current converters, where multiple switches are connected in parallel, impacting current sharing. To ensure equal inductance and current sharing between paralleled

Table 6.1: CONVERTER SPECIFICATIONS

Parameter	Value
HVDC voltage [V]	480 - 650
Battery voltage [V]	270 - 350
Output voltage [V]	22 - 29
Output power [kW]	4
Primary RMS current - HVDC mode [A]	10
Primary RMS current - battery mode [A]	20
Secondary RMS current [A]	220

branches, careful design of the connectors, layout, and PCB must be considered. The secondary inductance reflected on the primary side is proportional to the turns ratio squared. This reflected inductance varies for each mode of operation, due to differing turns ratio. Thus, obtainment of the external leakage inductance from an optimization algorithm is dependent on the reflected stray inductance. The stray inductance network can be represented as a single equivalent inductance shown in Fig. 6.2, connected in series with the connector inductance. Both inductances can then be reflected to the primary side. The total reflected inductance, which is a function of the turns ratio, is fed to the optimization algorithm.

6.2.1 Stray inductance model in Ansys Q3D

The algorithm is performed initially to obtain the initial values of N and L, but re-evaluated after the converter hardware design. The current values and transformer ratio, listed in Table 6.1, are extracted from the design tool considering SPS modulation and without considering the converter stray inductances. Considering the

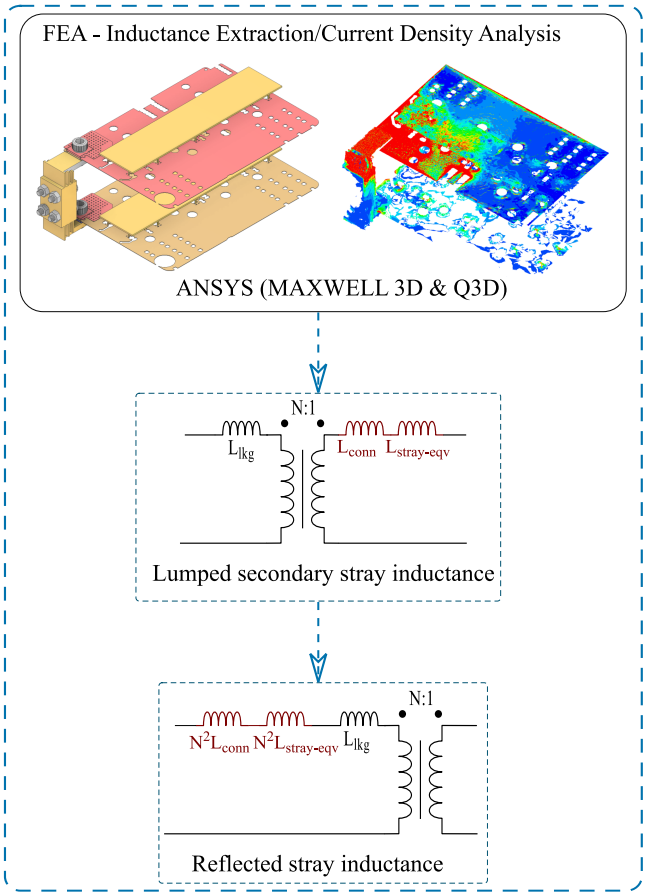


Figure 6.2: Design methodology - inductance extraction in Ansys Maxwell 3D and ANSYS Q3D.

high current on the secondary side and the required high efficiency of such converters, multiple discrete switching devices are used in parallel. Silicon Carbide MOSFETs (C3M0021120D) are selected for the primary side switches for both modes and Si MOSFETs (IPP023N10N5AKSA1) are selected for the secondary side. A single SiC device is used for the primary switches and six Si devices are paralleled for the secondary-side switches. The stray inductance network on the secondary side is extracted for the developed hardware from ANSYS Q3D. The stray inductance of the

secondary side has a negative impact on the current sharing between the paralleled devices. The PCB design, connectors design and layout need to be examined carefully to ensure equal inductances between the paralleled branches which results in a better current distribution. However, the focus of the analysis carried out in this paper is to highlight the effect of such inductances on the converter performance. The inductance is reflected on the primary side with a transfer ratio equal to the turns ratio squared. The large transfer ratio amplifies the effect of the inductance network. The parasitics model of the secondary side for one of the H-bridge legs is illustrated in Fig. 6.3. Both H-bridge legs are symmetrical and hence have the same stray inductance model. The lead inductances of the devices are denoted as L_{ld}; which represents the inductance of the drain and source leads. The stray inductance network depicted in Fig. 6.3 can be represented as a single equivalent inductance shown in Fig. 6.4 (a) in series with the connector inductance. Both inductances can then be reflected to the primary side as in Fig. 6.4 (b). The reflected inductance of the secondary terminal connector and the reflected stray inductance along with the leakage inductance of the transformer are then fed to the optimization algorithm. As discussed, the inductance value changes with the selected turns ratio and hence should be included in the converter analysis.

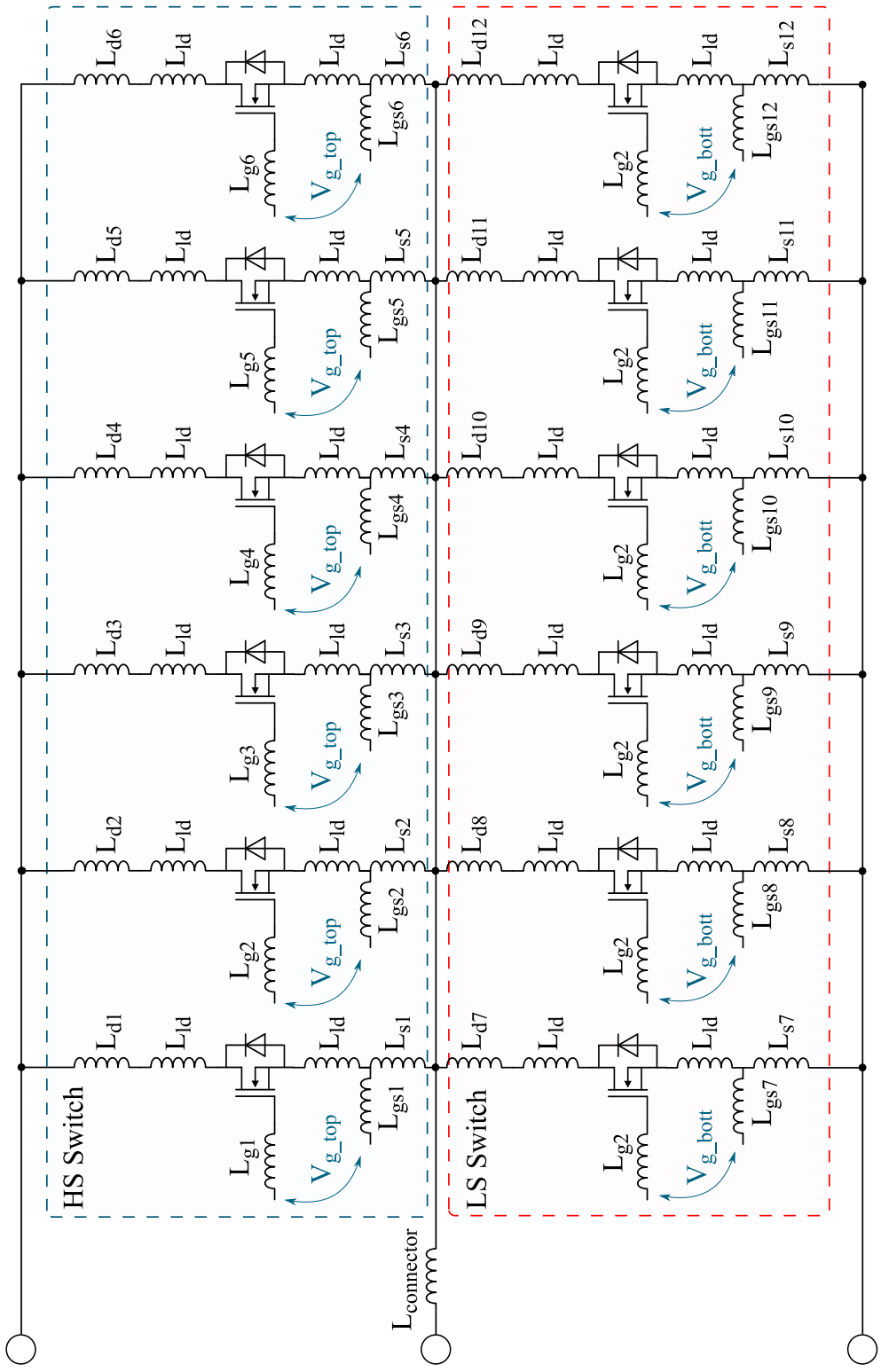


Figure 6.3: Stray inductance modeling - Inductance network - ANSYS Q3D.

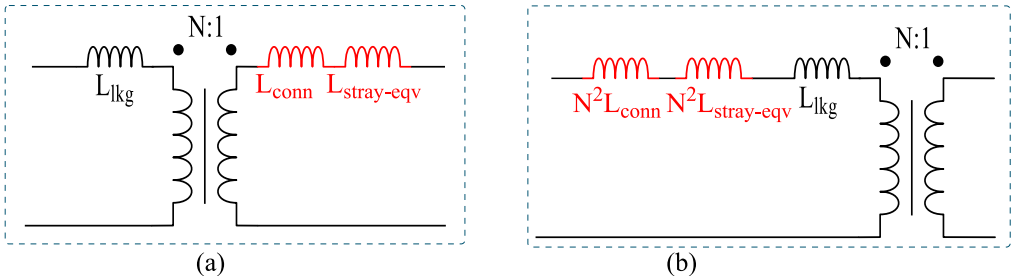


Figure 6.4: Stray inductance modeling. (a) Simplified inductance model. (b) Reflected inductance model.

The optimization process is outlined in Fig 6.5. The optimization process is split into two main layers. The first part includes optimization of the transformer turns ratio and external inductance, for the two main operating modes of the MSDAB. The second part optimizes the phase shift angle generating a look-up table (LUT) for different operating points under each mode. It is worth mentioning that the value of the reflected inductance is dependent on the transformer turns ratio which is an optimization variable in the algorithm. As shown in Fig. 6.2, the stray inductance of the secondary side is extracted using ANSYS Q3D. A lumped total inductance is obtained to represent the total secondary side inductance. The lumped inductance is then reflected on the primary side. In each of the operating modes, this reflected inductance value is different due to the different turns ratio used in each mode. The N_1, N_2, L_1 and L_2 selection is performed to minimize inductor RMS current across different operating points. The optimization is performed for both the HVDC and battery modes separately at various operating points. Different weighting factors are used for each point. Based on converter specifications, the weight of each operating point is determined. A representative RMS current for all operating points is analyzed. The operating range of the input and output voltages and the converter output power range are shown for the HVDC mode and battery modes.

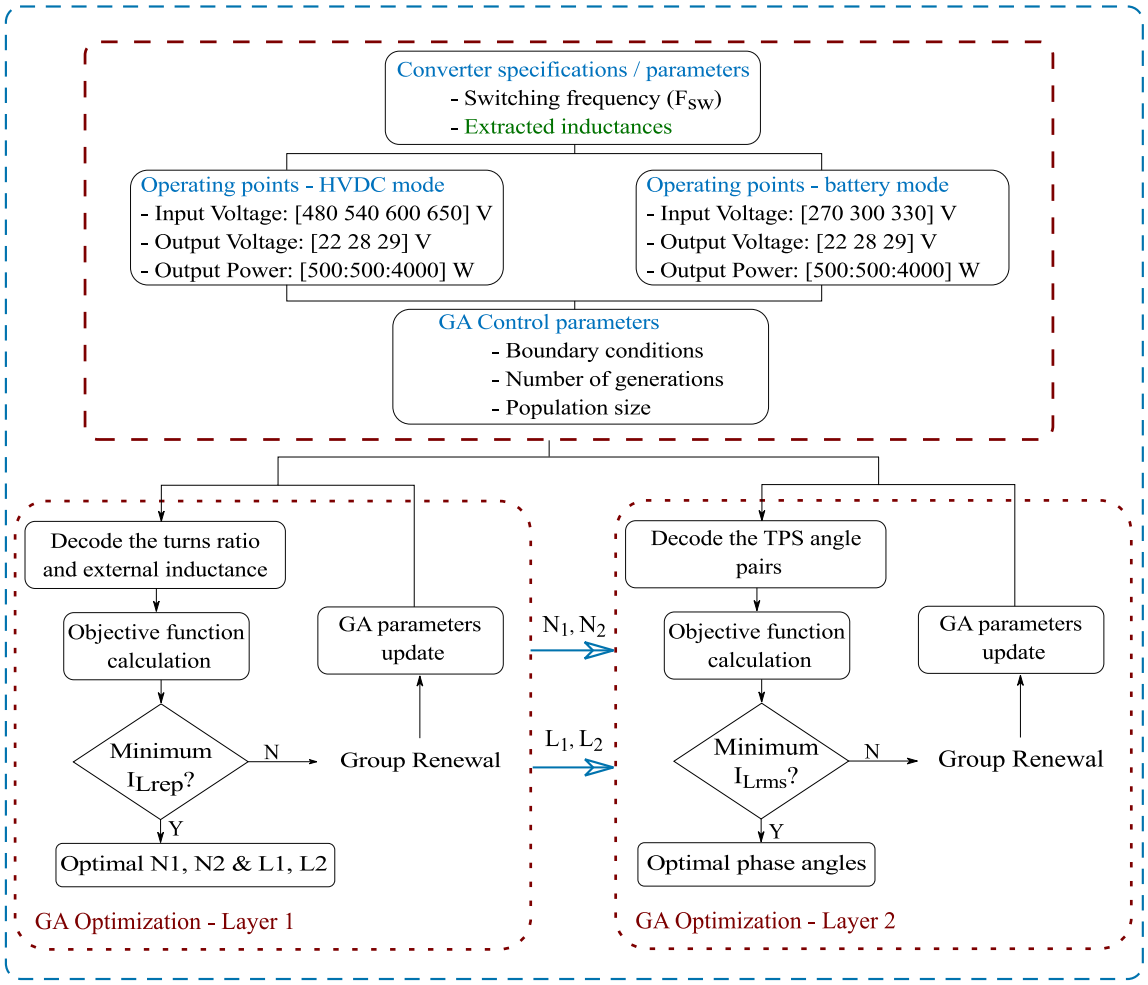


Figure 6.5: Design methodology flow chart - GA optimization layers.

$$V_{\text{in -HVDC}}(\text{i}) = \begin{pmatrix} 480\ \text{V} & 540\ \text{V} & 600\ \text{V} & 650\ \text{V} \end{pmatrix}$$

$$V_{\text{in - Battery}}\ (\text{i}) = \begin{pmatrix} 270\ \text{V} & 300\ \text{V} & 330\ \text{V} \end{pmatrix}$$

$$V_{\text{out}}\ (\text{j}) = \begin{pmatrix} 24\ \text{V} & 26\ \text{V} & 28\ \text{V} & 29\ \text{V} \end{pmatrix}$$

$$P_{\text{out}}\ (\text{k}) = \begin{pmatrix} 500\ \text{W} & 1\ \text{kW} & 2\ \text{kW} & 3\ \text{kW} & 4\ \text{kW} \end{pmatrix}$$

The representative RMS current, expressed in (6), is formed by summing out the

RMS current of all points multiplied by the weighting factor set by the designer. This representative current is obtained separately for the HVDC and battery operations.

$$\bar{I}_{Lrms} = \sum_{i=1}^{4}\sum_{j=1}^{4}\sum_{k=1}^{5} W_{i,j,k} I_{rms}(i,j,k), \tag{6.2.1}$$

where $W_{i,j,k}$ is the weighting factor of the corresponding operating point.

The RMS current for each mode is evaluated based on the generalized formula derived in the previous section under SPS control, with the phase angle calculated according to (7) for all operating conditions.

$$P_{SPS} = \frac{NV_{in}V_{out}}{2Lf_{sw}}\phi_2(1-\phi_2), \tag{6.2.2}$$

where f_{sw} is the switching frequency.

The lead inductances of all MOSFETs are the same for the parallel devices. The series PCB stray inductance of the drain and source, which is reflected on the primary side, along with the lead inductances are added to the connector inductance. The extracted secondary side inductance is denoted as the equivalent inductance shown in Fig. 6.2. The inductance values are extracted from ANSYS Q3D and fed to the GA optimization layers. The equivalent series inductance is fed to the optimization algorithm. A GA based optimization is adopted to select the external inductor value and turns ratio. The GA process outputs an optimal solution by going through multiple generations and variable mutations. This optimization algorithm is simple and efficient and is therefore utilized in this chapter. The following formulas linking

the stray inductances to the turns ratio are used:

$$\begin{aligned} L_{\text{reflected}} &= N^2 L_{\text{stray-equivalent}} \\ L_{\text{total}} &= L_{\text{reflected}} + L_{\text{ lkg}} + L_{ext}. \end{aligned} \tag{6.2.3}$$

The optimization problem of selecting N and L is defined as below:

Min : $I_{rms} = \sum_{i=1}^{4} \sum_{j=1}^{4} \sum_{k=1}^{5} W_{i,j,k} I_{rms}(i,j,k)$

Constraints:

$$L \leq L_{\max},$$

where L_{max} is the maximum allowed inductance realizing all operating points. The maximum inductance is obtained at maximum input voltage and minimum power. The maximum allowable phase shift ($\phi_{\max}$) is $\pi/2$ to achieve maximum power for a given turns ratio and input voltage. The maximum inductance allowed is different in each operating mode and can be calculated as follows:

$$L_{max} = \frac{\phi_{\max}\left(\pi - \phi_{\max}\right) N V_{in-\max}}{2\pi F P_{\text{out-min}}}. \tag{6.2.4}$$

This condition ensures all operating points function under a maximum phase shift of $\pi/2$. After the selection of N and L_{ext}, the converter parasitics are considered. In this case study, the total stray inductance on the secondary side is obtained as 70 nH for the secondary side PCB and connectors. This value is fed to the N-L optimization layer of each operating mode referred to as "GA Optimization - Layer 1" in Fig. 6.5. The weighting factor ($W_{i,j,k}$) for the nominal point, mid-power level, and remaining power levels are 50%, 25%, and 25%, respectively. The weighting factor selection is based on the design requirements and the importance of each operating

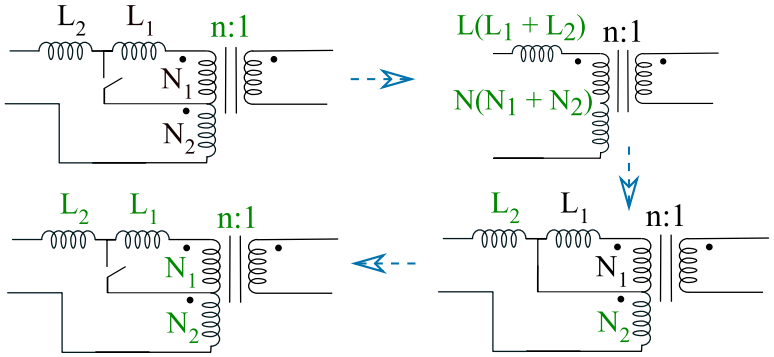


Figure 6.6: Optimization steps to attain the turn ratios and external inductances

point. First, as shown in Fig. 6.6, the values of N ($N_1 + N_2$) and L ($L_1 + L_2$) are obtained, which are the turns ratio and inductance values utilized in the HVDC mode. After which, the values of N_2 and L_2 are obtained, which are the turns ratio and inductance values of the battery mode. Finally, the values of N_1 and L_1 can be attained. This corresponds to running the optimization algorithm twice to obtain the optimal turns ratio and inductance value of both main modes while having the same secondary inductance fed to the algorithm for both modes. The different turns ratio and inductance values utilized in each mode ensure optimal operation and a wider ZVS range of the MSDAB in the main two operating modes. The optimized values for the turns ratio and total inductance are 20:1 and 45 µH, 10:1 and 11 µH for the HVDC and battery mode respectively. Part of the resulting optimized inductance is the secondary reflected inductance. In this scenario, only 11 µH external inductance is needed in the HVDC mode and the remaining inductance is provided by the inherit secondary stray and connectors design and no external inductance is required for the battery mode. For this design case, $L_2 = 0$, $L_1 = 11$ µH. Both $L_1 + N_1$ are bypassed in the battery mode by turning on switch S_9 The N-L_{ext} selection is dependent on the hardware design and must be included in the optimization process.

The optimal values are inputted to the second GA optimization layer as demonstrated in Fig. 6.5. The objective of the second part of the optimization process is to find the optimal phase shift values, under TPS control.

The optimization process is repeated for all operating points. Unlike the first optimization layer where a single representative current is optimized, the individual operating points' current is optimized in the second part, with phase shift selection based on each operating point. The optimization process for the selection of the phase angles is defined as below: Min: $I_{\text{rms}}\left[\text{V}_{\text{in}}(i)\,\text{V}_{\text{out}}(j)\,\text{P}_{\text{out}}(k)\right]$

Constraints:

$$\phi_3 - \phi_2 \leq \pi$$

$$\phi_f < \frac{\pi}{2}$$

$$P = P_{avg},$$

where ϕ_f represents the phase shift between the fundamental components of the bridge voltages V_{br1} and V_{br2}. The first constraint is to ensure the maximum phase shift between the secondary legs is π which is the case for SPS modulation. The upper limit for ϕ_1 is set to π which restricts the phase shift between the primary legs to π. Similar to SPS, maximum power transfer occurs at $\phi_f = \pi/2$. This condition is a constraint, which is included in the optimization process. The final constraint ensures that the target power is obtained at the optimal phase angle.

6.3 Converter Performance Analysis and Simulations

The different modes of operation of the MSDAB are investigated using the developed analytical model for the main modes and using PLECS for the battery charging and

bus regulation modes. The simulation and analytical parameters are set based on the converter specifications and the attained optimal converter turns ratio and external inductance for the different operating modes. To verify the developed analytical Fourier-based model, the tool is used to plot the converter waveforms in different bucking and boosting conditions. The developed analytical model exhibited a match to the ideal DAB simulation in PLECS.

6.3.1 HVDC supplies power to the LV network - HVDC mode

The converter has to be designed while considering the full operating range of the input voltage, output voltage and power. At some operating points, the converter currents may be higher than the nominal point. The devices ratings and transformer windings, external inductors need to be selected based on the worst operating point. The DAB converter operating and ZVS action also depends on the operating point. The developed Fourier model is used to display variables such as the RMS, peak currents and phase shift range across the full operating range. Fig. 6.7 shows the converter secondary RMS current, peak secondary current, and the phase shift across different output voltage and power levels. Fig. 6.7 (a) is obtained at the minimum input voltage 480 V. The plot highlights the transition between the buck and boost modes which occurs at unity converter gain ($\frac{NV_{out}}{V_{in}} = 1$). The maximum secondary peak current at this input voltage level is around 300 A. The converter output current is limited to the output current at the nominal operating point (V_{in}) = 600 V, V_{out} = 28 V, and P_{out} = 4 kW. This results in a power limit line as shown in Fig. 6.7 (a), (b), and (c). The power is limited for output voltages lower than the nominal point (V_{out} = 28 V), since more current is required to achieve the rated power level. On

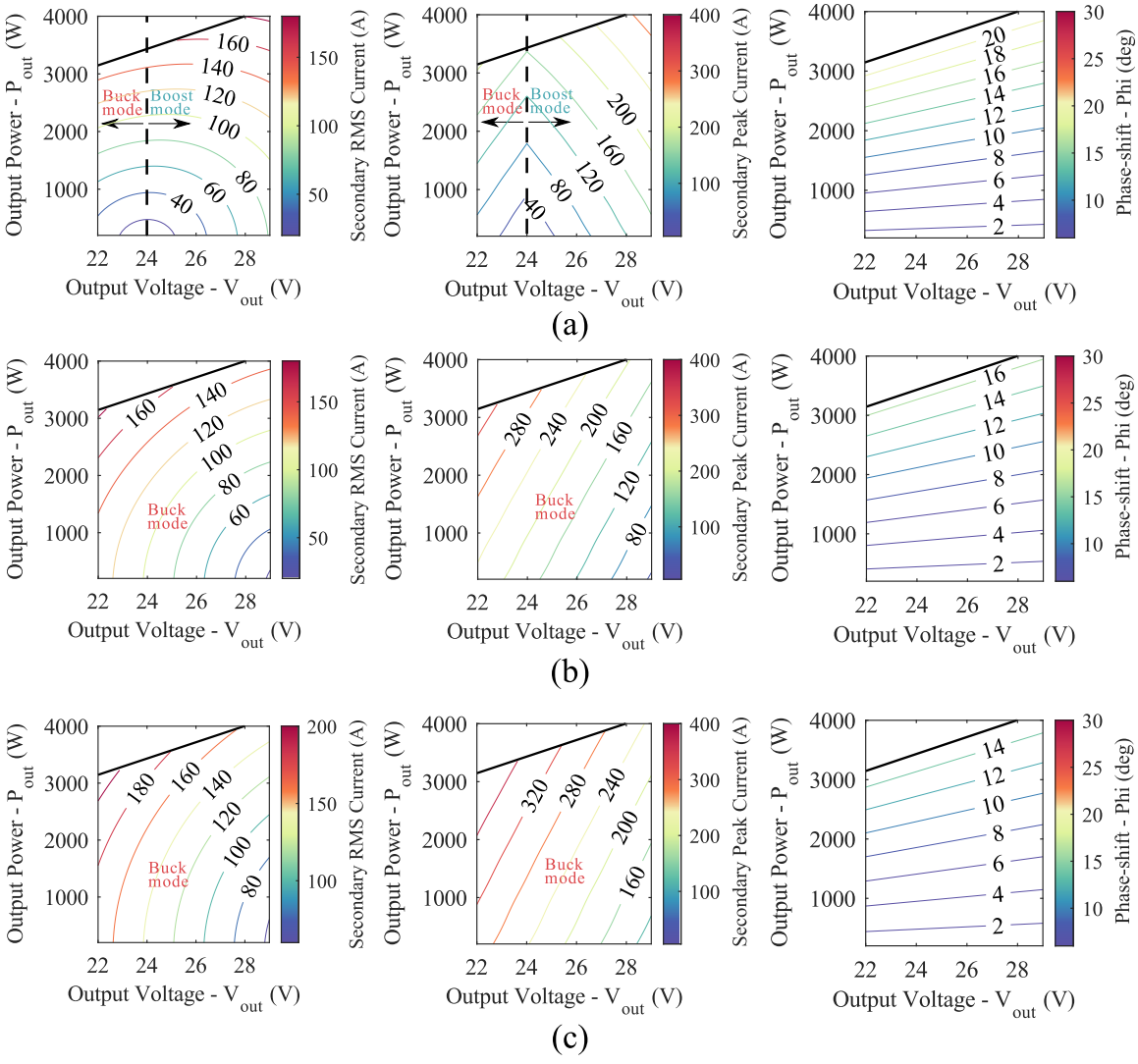


Figure 6.7: Converter operating-range map - HVDC mode. (a) $V_{in} = 480V$. (b) $V_{in} = 600V$. (c) $V_{in} = 650V$

the other hand, 6.7 (b), and (c) show that the converter only operate in buck mode for V_{in}) = 600 V and V_{in}) = 650 V. The required converter gain at these two input voltage levels is less than unity gain to realize the full output operating range. The primary and secondary devices ratings are sized based on the peak currents shown in 6.7. The analysis is carried out considering SPS modulation to select the devices ratings. The secondary maximum RMS current is 210 A and the peak current is around 330 A as shown in Fig. 6.7 (c).

Fig. 6.8 shows the converter waveform resulted from the Fourier expansion tool for the HVDC mode at the nominal operating point, 600 V / 28 V, and 4 kW. Since the converter gain the converter ($\frac{NV_{out}}{V_{in}}$) at this operating point is less than 1, the converter operates in buck mode. As, shown in 6.8 (a), the reflected secondary voltage (NV_{Br2}) amplitude is less than the primary bridge voltage (V_{Br1}), which results in the converter operating in buck mode. The voltage drop across the inductor placed between the primary bridge and the transformer is shown in 6.8 (b) where the voltage developed is during the phase shift period. As can be seen in 6.8 (c), the primary peak current (I_1) is less than the reflected secondary peak current I_2, which is expected in the buck mode operation. Both I_1 and I_2 are larger than zero, indicating that ZVS is achievable at this operating point for both the primary and secondary switches. Finally, the primary MOSFET current is shown in 6.8 (d) which can directly be used to extract the MOSFET RMS and switching current to obtain the switch losses.

The boost mode of operation of the DAB in the main HVDC mode is also examined for the operating point 480 V / 25.2 V, and 4 kW. The converter gain ($\frac{NV_{out}}{V_{in}}$) at this operating point is larger than 1, indicating that the converter operates at boost mode for this operating condition. The converter waveforms for this operating condition is

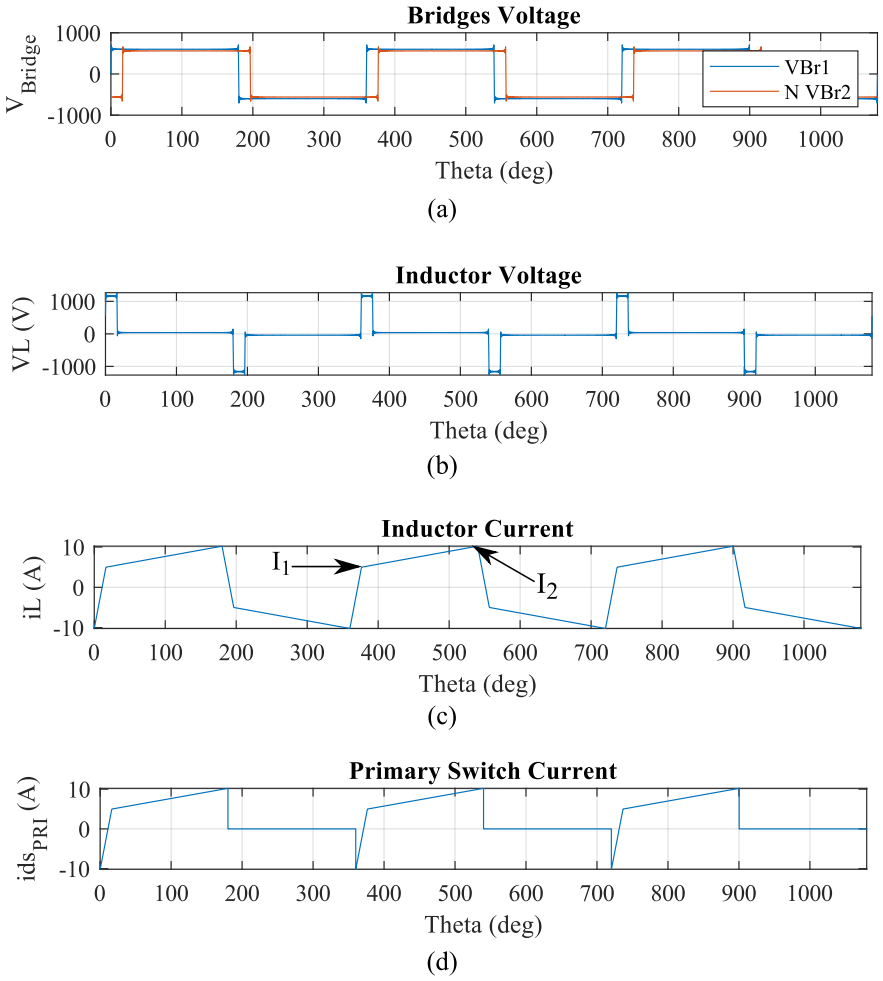


Figure 6.8: Fourier tool converter waveforms - HVDC mode: SPS $V_{in}/V_{out} = 600/28$, DAB bucking mode.

shown in Fig. Fig. 6.9. Unlike the buck mode of operation, the reflected secondary bridge NV_{Br2} in boost mode is higher than the primary bridge voltage (V_{Br1}) as shown in Fig. 6.9 (a). Similarly to buck mode, a voltage drop is developed across the inductor during the phase shift period as shown in Fig. 6.8 (b), which allows power to transfer between the indput and output sides. In the boosting mode of the DAB, I_1 is higher than I_2, as shown in Fig. 6.9 (c), which is resulted from opposite polarity of the voltage developed across the inductor as compared to the

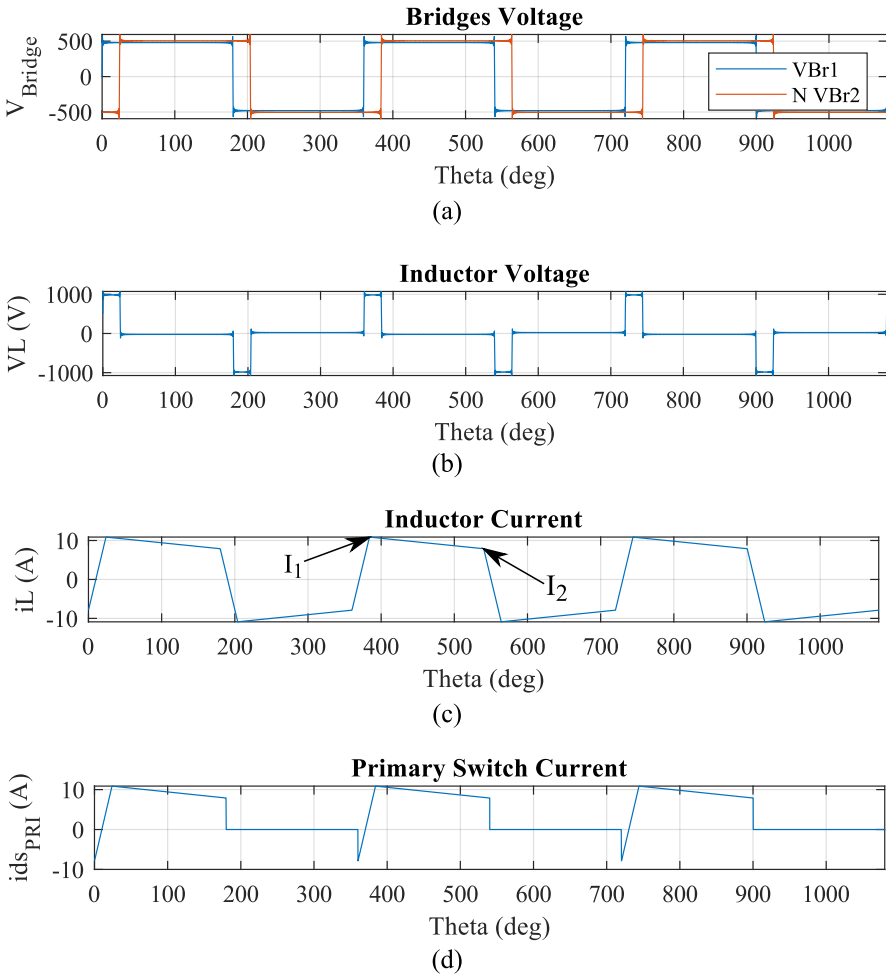


Figure 6.9: Fourier tool converter waveforms - HVDC mode: SPS $V_{in}/V_{out} = 480/25.2$, DAB boosting mode.

buck mode. The primary MOSFET current is extracted from the inductor waveform and is illustrated in Fig. 6.9 (d).

6.3.2 The battery supplies power to the LV network - battery mode

In this mode, the transformer ratio is adjusted using the tap changer to reduce the number of turns on the primary side since the input voltage is half that in the HVDC mode. Similarly, both buck and boost modes of operation are examined for the battery mode. The full operating range is also considered in this operating mode similar to the HVDC mode. Since the input voltage is lower than that of the HVDC mode, the required current to achieve the same rated power level is higher. However, since the turns ratio is half that utilized in the HVDC mode, the secondary current is close to that of the secondary current in the HVDC operating mode. The same analysis process is carried out for this mode of operation to display the key parameters of the converter, such as the phase shift range, maximum transformer RMS and peak currents across the full operating range. Fig. 6.10 shows the converter secondary RMS current, peak secondary current, and the phase shift across different output voltage and power levels. Fig. 6.10 (a) is obtained at the minimum input voltage 270 V. Fig. 6.10 (a) displays the transition between the buck and boost modes which occurs at unity converter gain ($\frac{NV_{out}}{V_{in}} = 1$). It can be seen in Fig. 6.10 (a), and Fig. 6.10 (b) that the converter operates in both buck and boost modes based on the required output voltage level. However, when the input voltage is increased to V_{in} = 330 V, the converter only operates in buck mode as shown in Fig. 6.10 (c). Similar to the HVDC mode, the output current is limited to the nominal point current (V_{in}) = 300 V, V_{out} = 28 V, and P_{out} = 4 kW). The secondary peak current can be extracted from Fig. 6.10 (c) as 370 A which is higher than the HVDC mode (330 A). Since both sources, the HVDC link and the battery, share the same secondary side, the

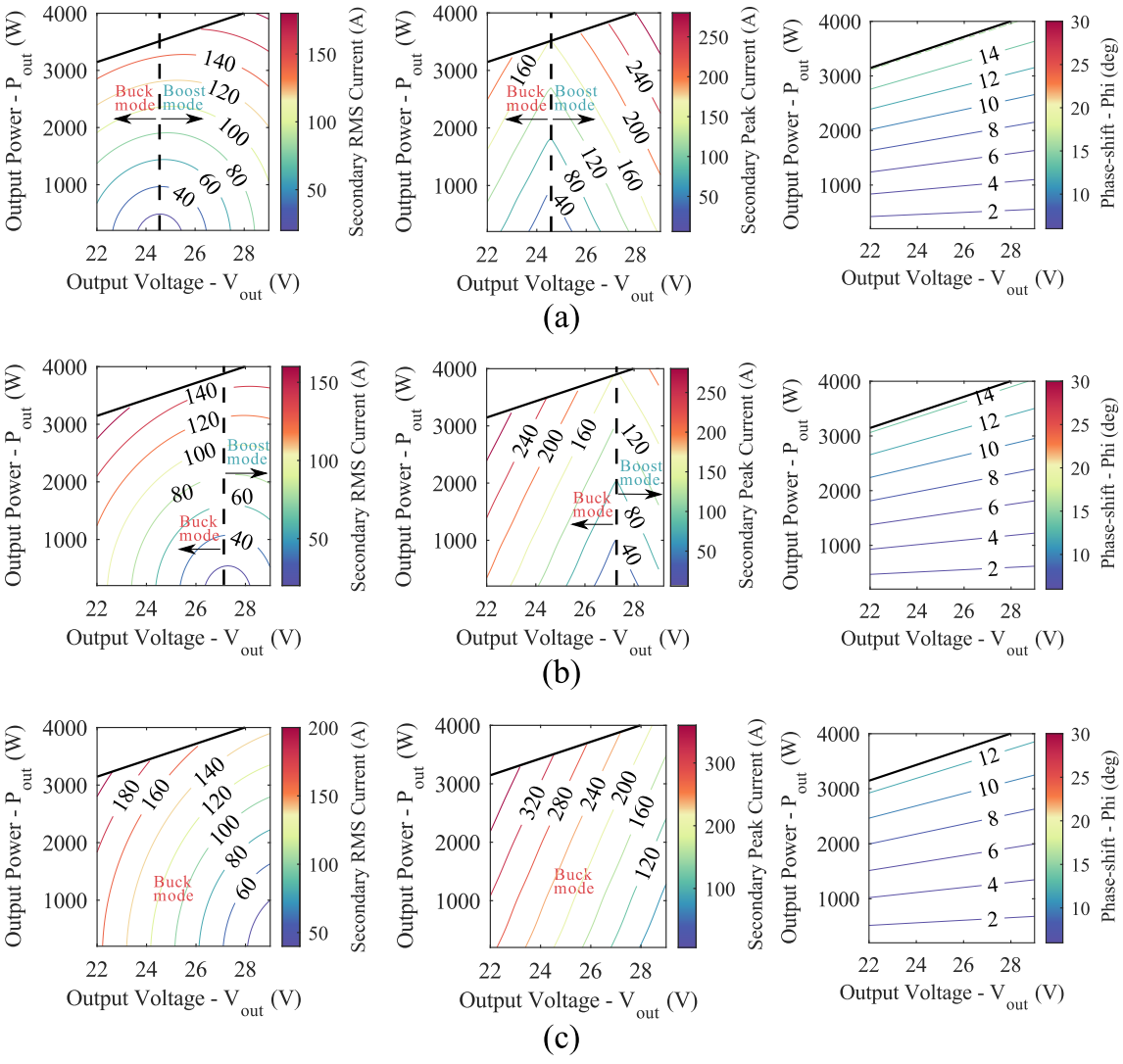


Figure 6.10: Converter operating-range map - battery mode. (a) $V_{in} = 270V$. (b) $V_{in} = 300V$. (c) $V_{in} = 330V$

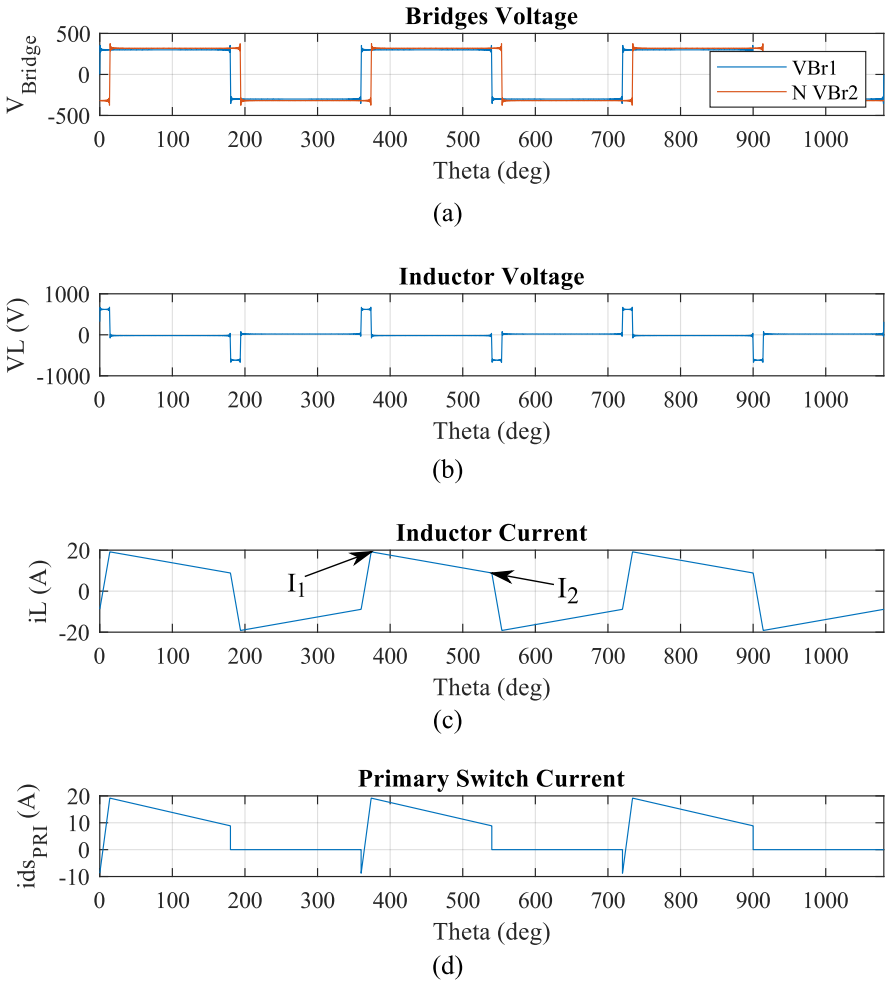


Figure 6.11: Fourier tool converter waveforms - battery mode: SPS $V_{in}/V_{out} = 300/28$, DAB boost mode.

secondary devices have to be selected based on the worst operating condition in both modes.

The nominal operating point of this mode, 300 V / 28 V, and 4 kW operates in boost mode, since the converter gain the converter ($\frac{NV_{out}}{V_{in}}$) at this operating point is larger than 1. The converter waveforms are shown in Fig. Fig. 6.11. The buck mode of operating is then simulated at the operating point, 330 V / 29 V, and 4 kW. The converter gain for this operating point is less than 1. The converter waveforms of this

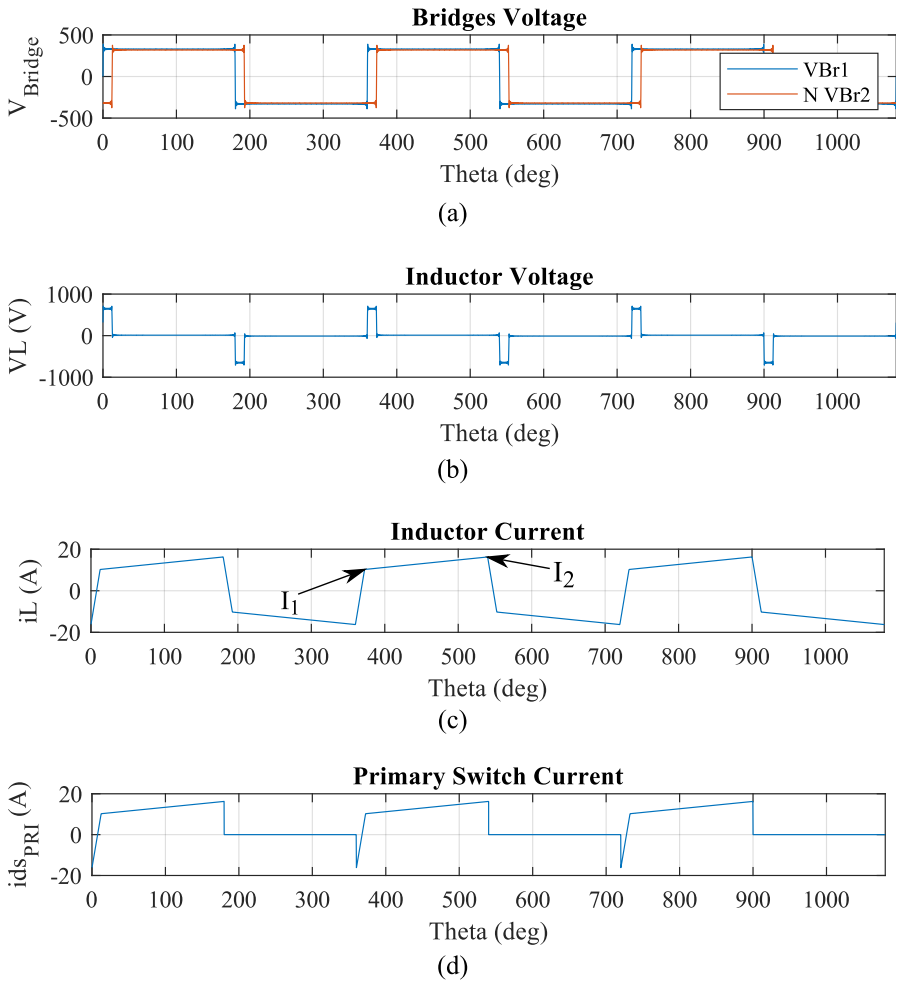


Figure 6.12: Fourier tool converter waveforms - battery mode: SPS $V_{in}/V_{out} = 330/29$, DAB buck mode.

operating point are shown in Fig. Fig. 6.12. As noticed at the rated power, both I_1 and I_2 are higher than zero, which results in having ZVS for both the primary and secondary sides. The loss of ZVS is also examined at low power level. Two cases are examined where the ZVS action is lost either on the primary side or the secondary side. Fig. 6.13 (a) shows that the primary switches exhibits hard switching at $V_{in}/V_{out} = 330/29$, 800 W (one fifth the rated power). The loss of ZVS action on the primary is resulted from the negative peak current I_1, which results in not having

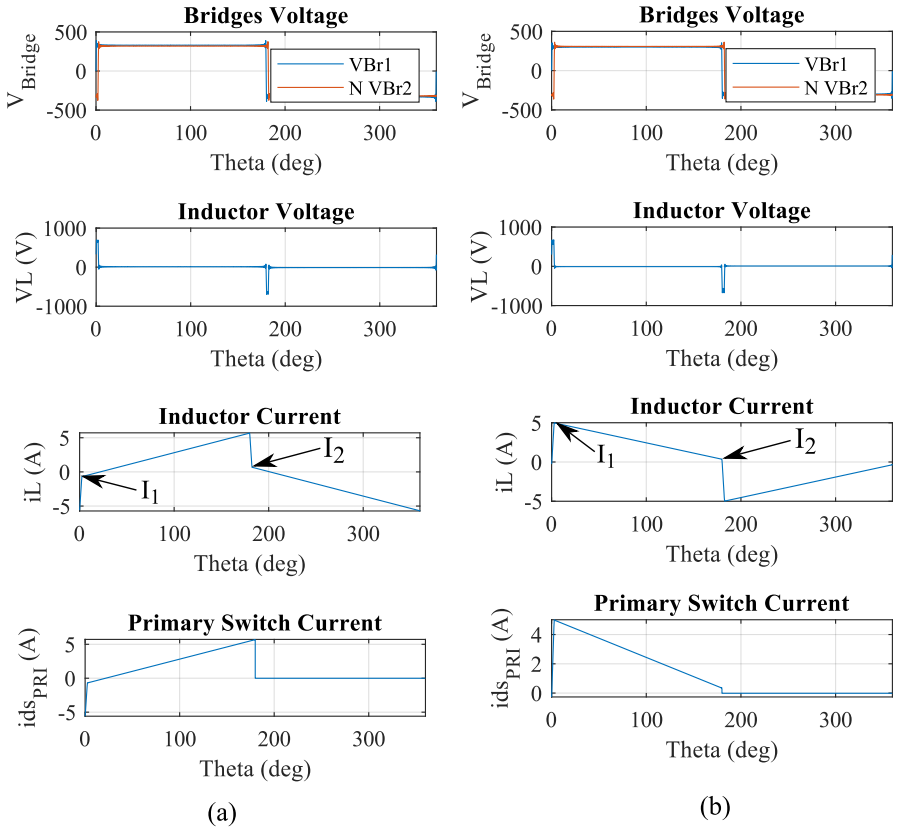


Figure 6.13: Loss of ZVS - battery mode. (a) primary ZVS loss, $V_{in}/V_{out} = 330/29$, 800 W. (b) secondary ZVS loss, $V_{in}/V_{out} = 300/28$, 800 W

enough energy in the inductor to cause ZVS during the deadtime. On the other hand, for the operating point $V_{in}/V_{out} = 300/28$, 800 W, the secondary devices exhibits hard switching since the peak current (I_2) is close to zero. The developed Fourier tool can be utilized as a comprehensive simulation tool that outputs the converter waveform without the need for a simulation tool or a developed state-space model for the converter. Several parameter like the inductor RMS current, peak currents of the switching devices on both the primary and secondary sides as well as the transformer currents can be extracted numerically from the waveform. Other control techniques can be also examined using the Fourier tool to extract the converter parameters such

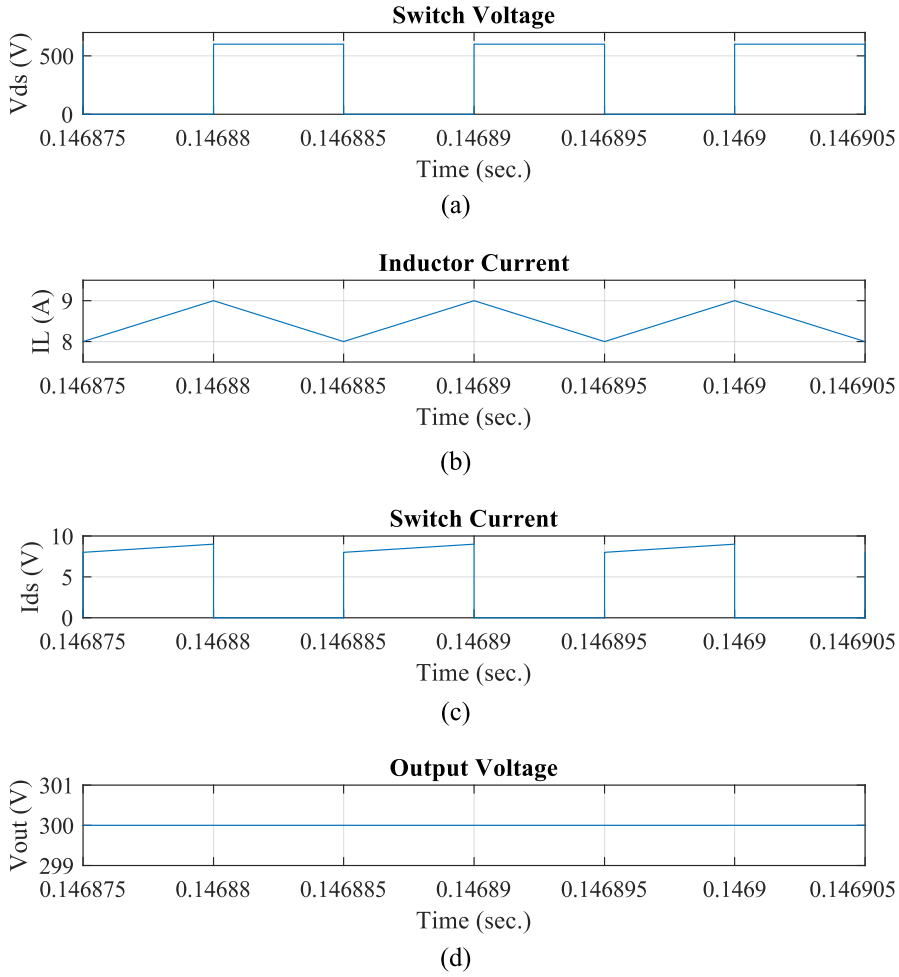


Figure 6.14: PLECS simulation - battery charging mode, 600 V to 300V, 2.5 kW

as the devices RMS and switching currents. The ZVS action as well as the converter loss analysis can be integrated with the Fourier modeling tool without the need for a converter simulation tool such as Simulink or PLECS.

6.3.3 Battery charging mode of operation

The converter waveforms for the battery charging mode are shown in Fig. 6.14. During this mode, the HVDC bus charges the battery and the magnetizing inductance

is utilized as part of a low pass filter. The converter configuration in this mode is the same as the buck converter. An output capacitor is selected to be 150 µF to limit the voltage ripples to 0.5%. Two PI controllers are designed for the CC-CV charging technique and simulated in PLECS; the battery is modeled as resistor in each mode considering that the charger power is 2.5 kW in this mode. (50% of the original converter power) The current reference is 8.3 A, and the constant voltage value is 300 V. The charging current is limited to prevent lithium plating and to extend the lifetime of the battery. The converter in this mode behaves as a conventional buck converter. The closed loop system design of the CC-CV mode is designed using the PLECS small signal analysis tool.

6.3.4 HVDC bus regulation mode of operation

In the bus regulation mode, similar to the battery charging mode, the magnetizing inductance is also utilized as part of a low pass filter. The converter in this mode behaves as a conventional boost converter. The same switches as the battery charging mode are utilized as explained in the converter modes of operation section. The maximum regulation power is the same as the converter rated power (4 kW). PLECS small signal analysis tool is used to design the PI controller utilized in this mode. The converter waveforms for the bus regulation mode are shown in Fig. 6.15

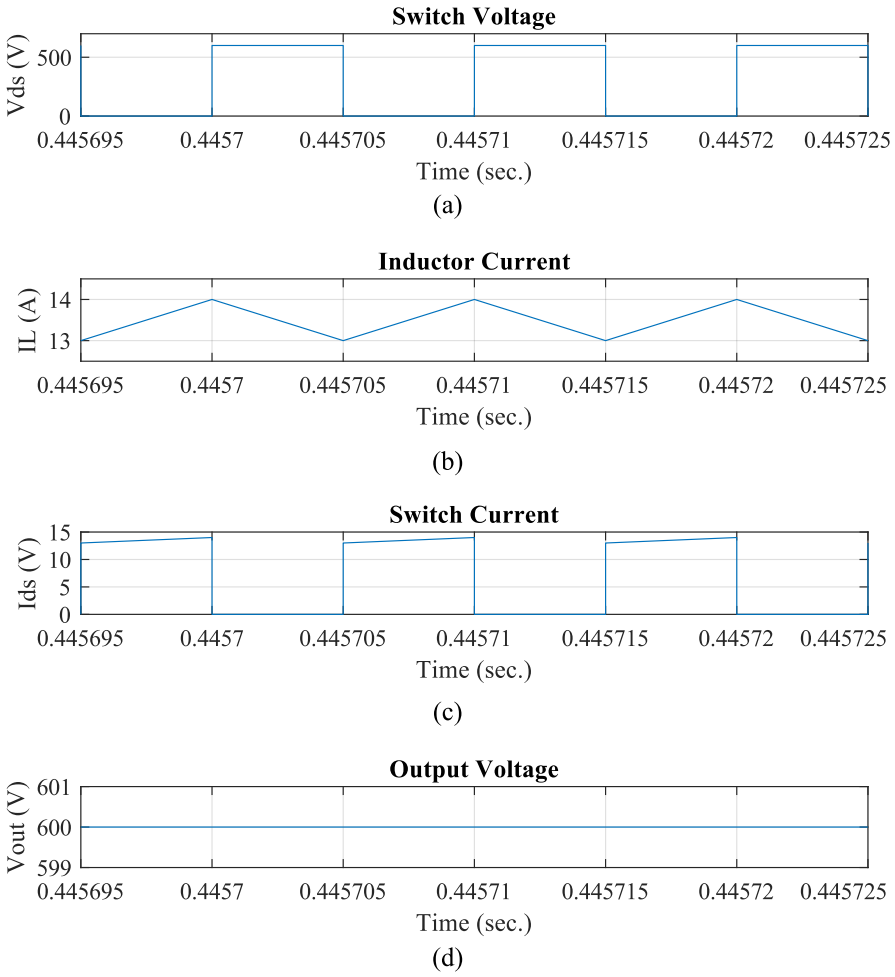


Figure 6.15: PLECS simulation - bus regulation mode, 300 V to 600V, 4 kW

6.4 Experimental Validation

A 4-kW prototype, shown in Fig. 6.16, was built to validate the proposed MSDAB topology. The specifications for the implemented converter prototype is listed in Table 6.1. To highlight the effectiveness of the proposed stray inductance modeling method and FEA analysis, the converter phase shift is tested with different added external inductances (L_{ext}) and transformer turns ratios (N). The phase shift analysis was carried out at the nominal operating voltage point (600 V/28 V) and different power

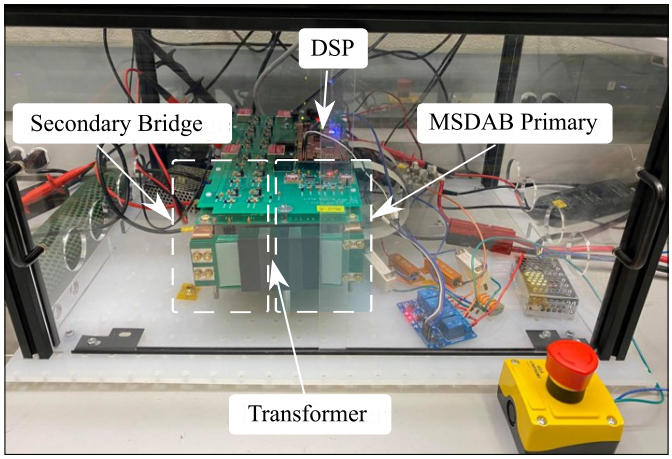


Figure 6.16: Multisource dual-active bridge experimental setup

levels from 1.5 kW to 5 kW. After which, the deviation between the expected phase shift from the conventional DAB model and the proposed DAB stray inductance model is plotted against the actual experimental phase shift in Fig. 6.17. It can be noticed in Fig. 6.17 (a) that the phase shift deviation between the proposed method and the actual one is considerably lower by several orders of magnitude compared to the conventional method. To further validate the robustness of the proposed method, different converter parameters were tested and the results were plotted in Fig. 6.17 (b), (c), and (d). All tests showed remarkably lower phase shift deviation between the actual and proposed method compared to the conventional one. As such, this method can lead to a more optimized design with better performance insight.

The effectiveness of the proposed optimization methodology has been tested across different voltage and power levels in the main two operating modes. In the HVDC mode (HVDC link supplies power to the LV network), the transformer tap changer is deactivated and the full turns of the transformer are utilized to provide a high step-down ratio resulting from the optimization algorithm. In the battery mode (battery

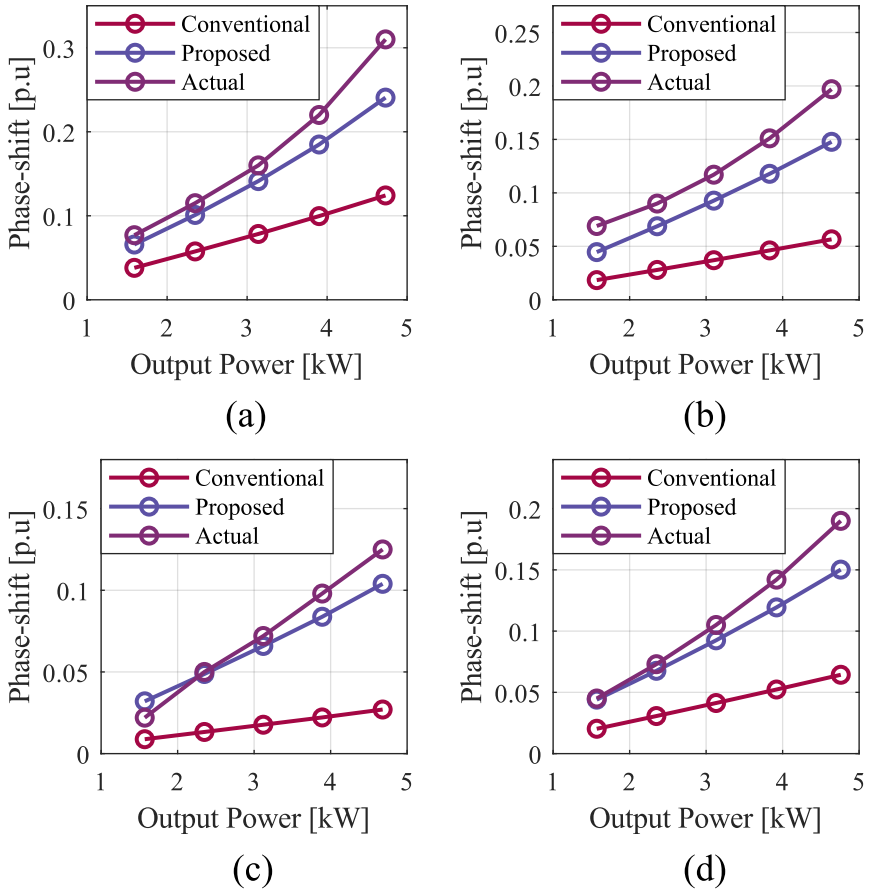


Figure 6.17: The proposed DAB stray model phase shift analysis. (a) $N = 22, L_{ext} = 50\,\mu H$. (b) $N = 22, L_{ext} = 25\,\mu H$. (c) $N = 20, L_{ext} = 11\,\mu H$. (d) $N = 20, L_{ext} = 25\,\mu H$.

supplies power to the LV network), the transformer ratio is adjusted using the tap changer to reduce the number of turns on the primary side since the input voltage is half that in the HVDC mode. ZVS is achieved through the added external inductor and the reflected stray inductance which is dependent on the turns ratio utilized in this mode.

To validate the phase shift angles optimization, the converter is tested at multiple voltages and power operating points. The converter's power efficiency is measured for both operating modes under both SPS modulation and the optimized TPS angles.

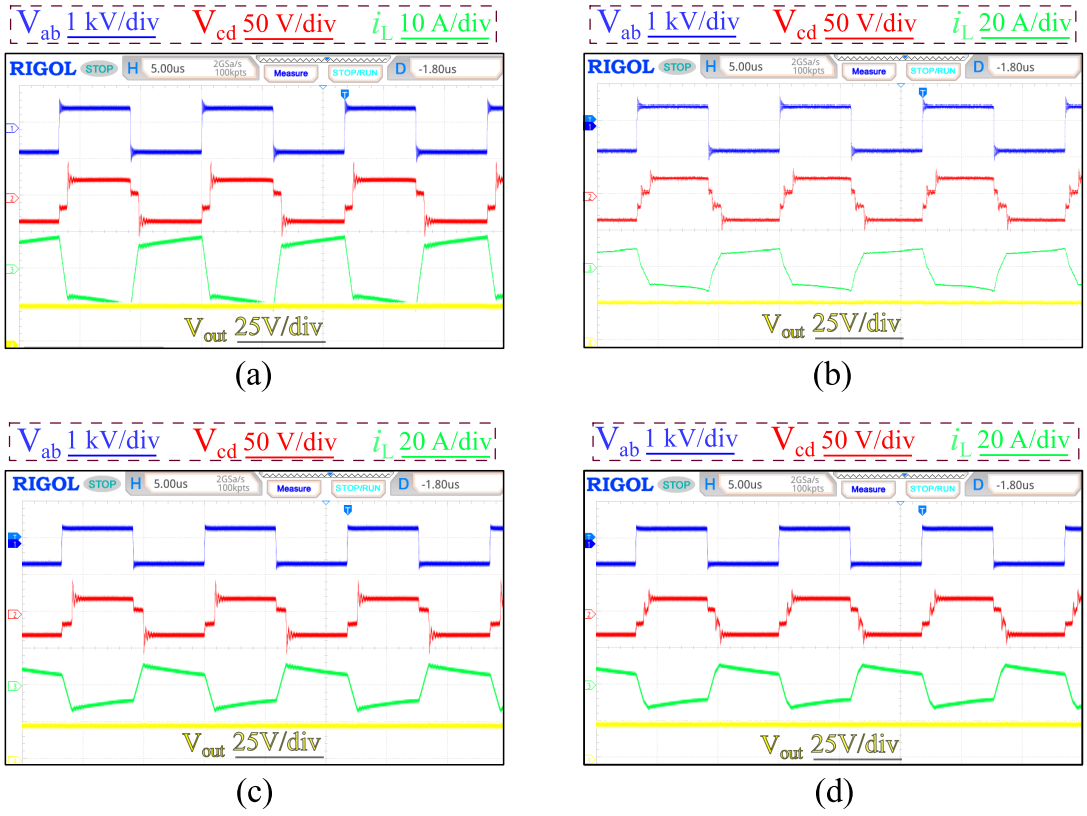


Figure 6.18: Experimental waveforms for SPS, TPS ($N_1 = 9$, $N_2 = 11$, $L_1 = 30\,\mu H$, $L_2 = 11\,\mu H$): (a) HVDC mode: SPS $V_{in}/V_{out} = 600/28$, (b) HVDC mode: TPS $V_{in}/V_{out} = 600/28$, (c) HVDC mode: SPS $V_{in}/V_{out} = 480/25.2$, and (d) HVDC mode: TPS $V_{in}/V_{out} = 480/25.2$

Fig. 6.18 illustrates the converter waveforms at the rated power when the LVDC network is supplied through the HVDC bus. Both SPS and TPS optimized algorithm are tested.

Similarly the converter is tested at the rated power in the battery mode. The converter waveforms considering both SPS and TPS modulation are shown in 6.19 for the battery mode.

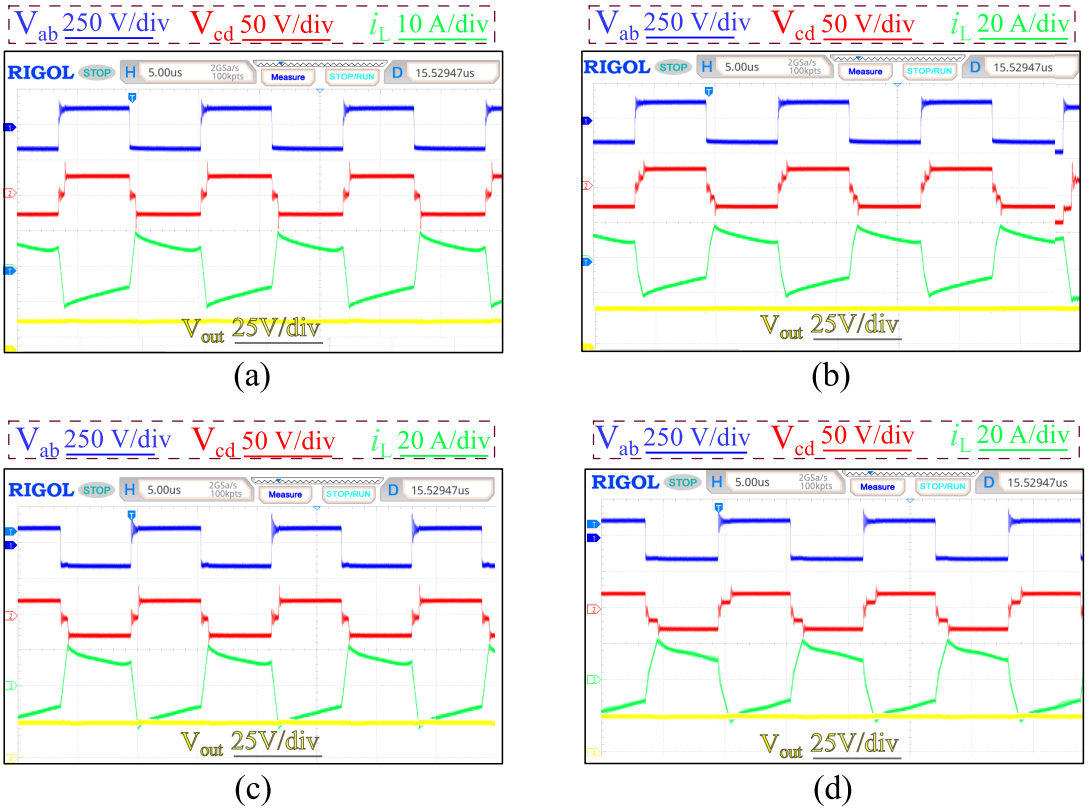


Figure 6.19: Experimental waveforms for SPS, TPS ($N_1 = 9$, $N_2 = 11$, $L_1 = 30\,\mu H$, $L_2 = 11\,\mu H$). (a) battery mode: SPS $V_{in}/V_{out} = 300/28$, (b) battery mode: TPS $V_{in}/V_{out} = 300/28$, (c) battery mode: SPS $V_{in}/V_{out} = 270/25.2$, and (d) battery mode: TPS $V_{in}/V_{out} = 270/25.2$

The extent of TPS optimization on the converter efficiency was tested at different power and voltage levels to highlight the effectiveness of the proposed optimization algorithm. The experimental efficiency plots for the two main modes are shown in Fig. 6.20. Different input and output voltage levels are considered, as shown in Fig. 6.20, to validate the developed algorithm across the whole converter operating range. For all the considered operating points in both operating modes, TPS modulation consistently outperformed the SPS modulation in efficiency.

The third operating mode is when the converter operates so that the HVDC bus

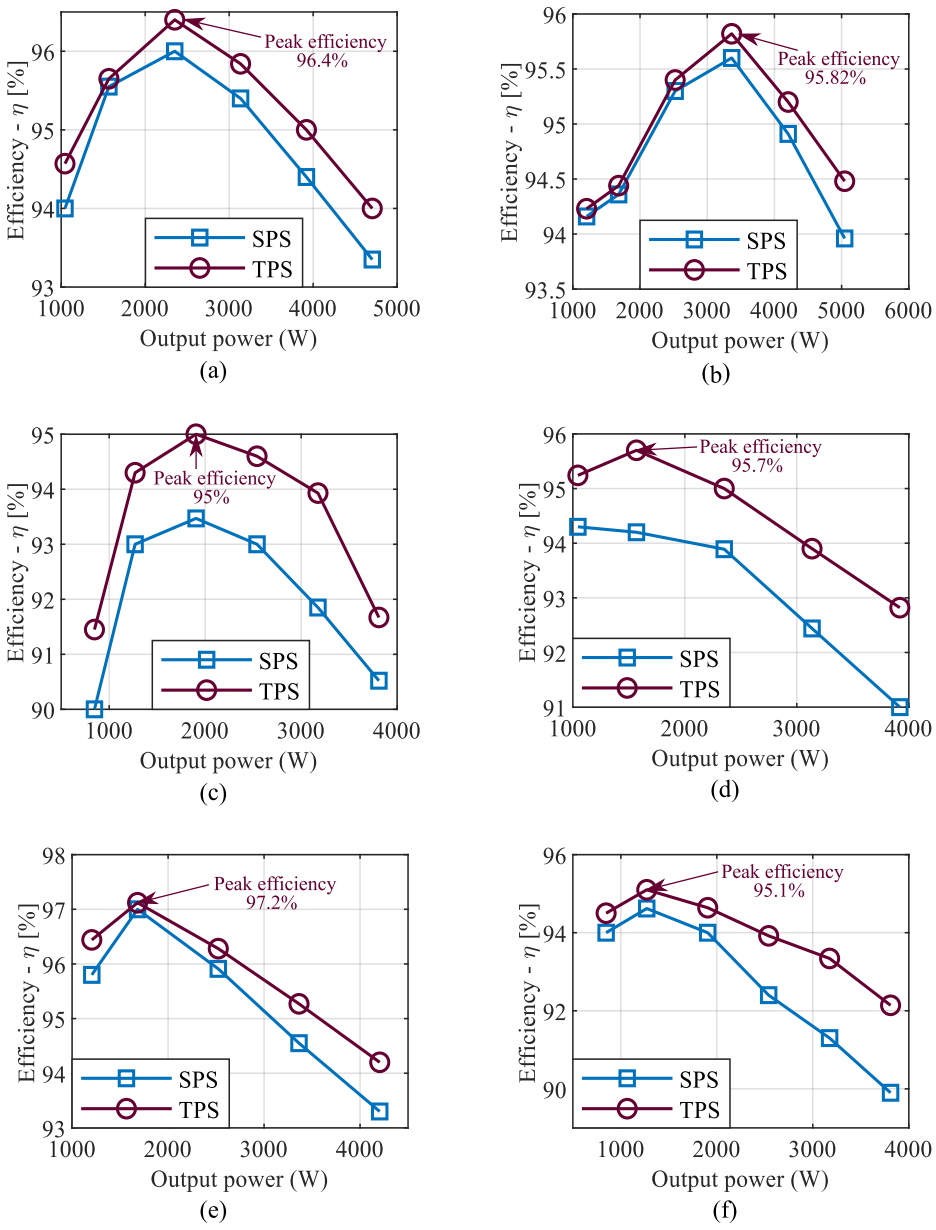


Figure 6.20: Experimental efficiency for SPS, TPS ($N_1 = 9$, $N_2 = 11$, $L_1 = 30\,\mu H$, $L_2 = 11\,\mu H$). (a) HVDC mode: $V_{in}/V_{out} = 600/28$. (b) HVDC mode: $V_{in}/V_{out} = 650/29$. (c) HVDC mode: $V_{in}/V_{out} = 480/25.2$, (d) battery mode: $V_{in}/V_{out} = 300/28$, (e) battery mode: $V_{in}/V_{out} = 330/29$, and (f) battery mode: $V_{in}/V_{out} = 270/25.2$.

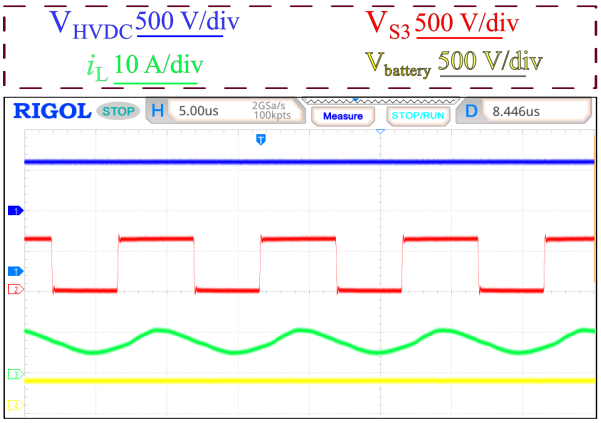


Figure 6.21: Experimental waveforms for the battery charging mode at 2.5 kW.

charges the battery. The battery charging mode is then tested by modulating S_3 and S_4 as was shown in the switching scheme for this mode. During this mode, the HVDC bus charges the battery, and the magnetizing inductance is utilized as a part of the output low pass filter. The converter configuration in this mode is the same as the buck converter. An output capacitor is selected to be 150 µF to limit the voltage ripples to 0.5%. Two PI controllers are designed and implemented on the DSP C2000 Launchpad F28379D for the conventional CC-CV charging technique. The transfer functions of both the inner current loop and outer voltage loops are extracted using the small signal analysis toolbox in the PLECS environment. The charging power is limited to 2.5 kW in this mode, to extend the battery lifetime and prevent lithium plating due to high charging currents. The experimental waveforms of this mode are shown in Fig. 6.21. The implemented charging profile is shown in Fig. 6.22 (a) and the experimental efficiency is plotted in Fig. 6.22 (b) at different HVDC bus voltages. The efficiency of this operating mode is high across all operating points since only the HV side bridge is utilized.

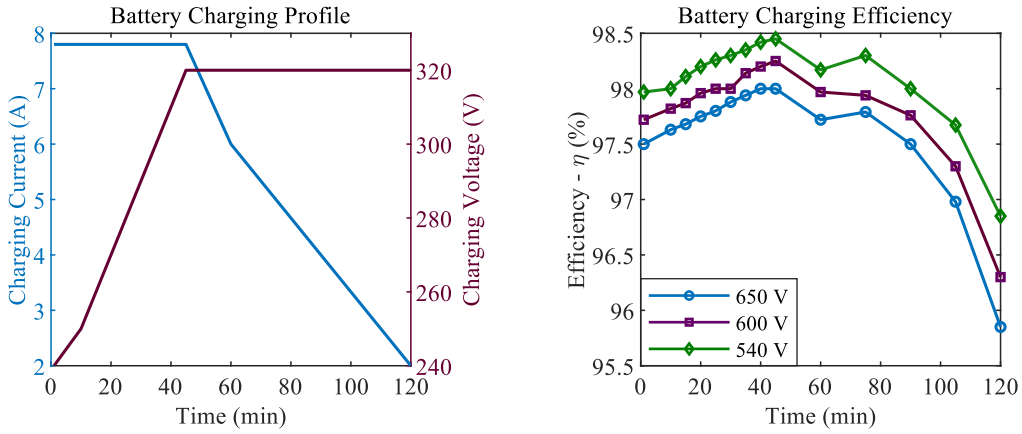


Figure 6.22: Experimental efficiency for the battery charging mode. (a) battery CC-CV charging profile, and (b) Implemented charging profile using CC-CV technique at different input bus voltage

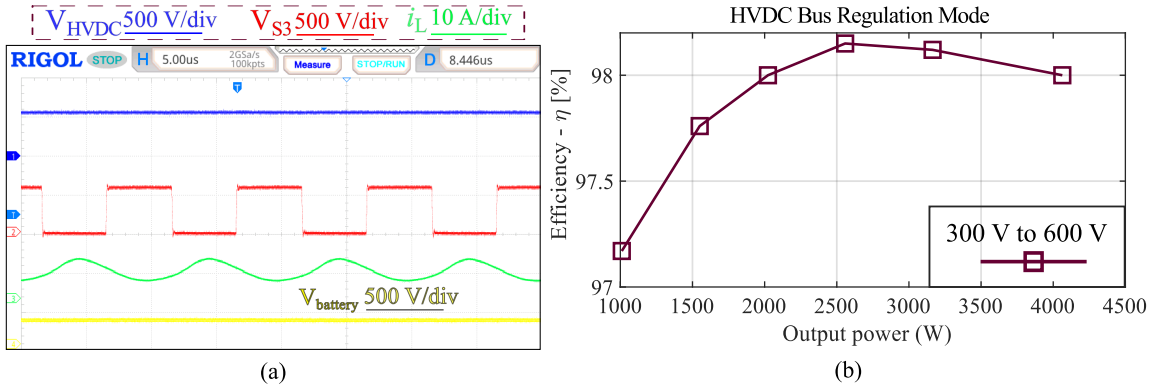


Figure 6.23: Experimental efficiency for the bus regulation mode: (a) Converter waveforms at rated 4 kW and (b) Converter efficiency at different power levels.

Finally, the HVDC bus regulation mode is tested, where the battery (second source) supplies power to stabilize the HVDC link in case of voltage sag. Unlike the battery charging mode where the current is limited, the regulation current of the HVDC regulation mode can be set to the rated converter current. The experimental key waveforms of this mode are illustrated in Fig. 6.23 (a). The main system-level

supervisor sets the required current and power to stabilize the HVDC bus voltage. The converter is tested in this mode under different power demand conditions and the efficiency plot is shown in Fig. 6.23 (b).

6.5 Summary

In this chapter the MSDAB modelling and control has been presented. The mathematical model of the MSDAB topology is developed based on the Fourier-transform approach. Furthermore, an optimization methodology was proposed to optimize the two main modes of operation which includes two layers of optimization through a genetic algorithm. Layer 1: optimization of transformer turns ratio and DAB inductor, and layer 2: phase angle optimization by using triple phase shift (TPS) control for the DAB converter [51,97,98]. The experimental setup is shown, and key waveforms and efficiency plots are presented. The effect of considering the converter stray elements in the optimization process was highlighted experimentally. The developed GA algorithms are tested for the two main converter modes at different power and voltage operating points. The results showed 1-2% improvement in the converter efficiency at different operating conditions. The different modes of operations are tested highlighting the effect on the control flexibility and system stability.

Chapter 7

Conclusions and Future Work

7.1 Conclusions

This thesis introduces the conceptual development and optimization of multi-source DC/DC converters for more-electric aircraft.

The development of system requirements based on the existing aircraft electrical distribution architectures is established. Design guidelines considering the industry regulatory standards are presented. It has been established that there is an electrical power demand increase of modern aircraft architectures. More ESSs are utilized in the MEA distribution networks. As highlighted, a system-level integration of the DC/DC converter unit is required for better system utilization. Existing literature techniques for converters integration including multi-port topologies has been reviewed. A topological evaluation of the basic DC/DC converter topologies considered for the MEA application was carried out. The challenges associated with the HV distribution network of MEA structures were presented. The DAB converter topology is the most widely adopted converter configuration considered in MEA DC/DC converters. Other variations of the basic DAB topologies has been introduced in literature to accomodate the arising challenges with the HV distribution system such as the multi-level NPC-DAB and ANPC-DAB. Other configurations based on the DAB as well including ISOPs, IPOPs and magnetically coupled multi-ports DC/DC converters have emerged as well to increase the system stability and enhance the converter efficiency. The basic modulation techniques of the conventional DAB topology were reviewed. TPS modulation is the most general technique considered for the DAB topology with potential wide ZVS range as compared to SPS and DPS control schemes.

A review of the magnetic components with a focus on the isolating transformer and its winding configurations has been conducted. The trade-offs between minimizing the

transformer parasitic to enhance the converter performance and the transformer power density were presented. The relation between the transformer winding structures, transformer parasitics and converter performance were established.

A design methodology for planar transformers for MEA was presented with the main focus on the transformer power density and converter performance. The selection of the optimal switching frequency and the transformer core were discussed. The importance of the optimization tool was highlighted considering paralleling of cores and different magnetic materials. The core selection guidelines are combined with the results from the device switching loss analysis. Having such an integrated solution between the transformer and the switching devices ensures an optimum selection of the switching frequency to optimize the size and weight of the transformer core considering the overall converter efficiency. The process of extracting the transformer parasitic components has been discussed highlighting the importance of considering the effect of such parasitics and how the transformer performance can be affected. Two winding structures were proposed and compared to the conventional spiral double-layer configurations. The proposed structures showed a significant reduction in the transformer capacitance and improvement of the converter performance. By utilizing multi-layers, the transformer power density and efficiency are not compromised. The proposed structures were validated in ANSYS Maxwell 3D and the converter performance was investigated in PLECS. The developed methodology is able to provide reliable results that were experimentally validated with a DAB converter prototype.

A MSDAB topology was proposed and different modes of operations for the converter were discussed showing the switching scheme for each mode. The topology allows for integration between two different sources to supply the LV network aboard

the aircraft. The different modes add flexibility to the system, enabling power flow control between different sources in the EDPS of the aircraft. Better system utilization as compared to conventional solutions is achieved. The power density of the proposed MSDAB configuration is increased by the reduction in the number of switching devices as well as magnetic components. The MSDAB has been modeled based on the Fourier transform technique. A two-layer GA-based optimization process has been developed for the two main modes of the MSDAB topology. The algorithm was validated experimentally across different operating points and at various operating voltages. The efficiency considering the developed GA algorithm is improved by 1-2 % compared to the conventional SPS modulation technique. Furthermore, the power flow control between the two sources has been validated at different power levels. The proposed topology showed promise in terms of sources integration and system stability as compared to the conventional DAB converters often utilized in such applications.

7.2 Future Work

The following future work can be considered to improve the proposed integrated MSDAB converter:

1. System-level converter optimization can be carried out to improve the system utilization. It has been highlighted throughout the thesis that paralleling low-power converter units is beneficial in-terms of converter performance and system utilization The supervisor development and system-level optimization can be carried out to control the power flow between the different energy sources through the multi-source topology.

2. System stability analysis can be carried out highlighting the system dynamics when switching between the different MSDAB converter modes. The impact of the bus regulation during voltage sag in the HVDC bus and fault conditions can be discussed.

3. Interleaving between the paralleled low-power cells will result in reduction in the output filter size. Control schemes strategies between the paralleled modules can be developed to reduce the input and output filter size.

4. Including the leakage inductance in the transformer analysis for the different winding configurations. Tight control over the transformer leakage inductance is advantageous to omit using and external inductance for the MSDAB topology to further enhance the converter power density. The trade-offs between the transformer losses, winding capacitance and controlled leakage inductance can be introduced.

5. Implementation of the EMI filter to meet the regulatory DO-160 standard. The effect of the transformer capacitance on the HFO and hence the EMI filter size can be included.

6. The converter loss model can further be improved by including the system parasitics in the analysis. The converter parasitics affect the HFO and the voltage spikes amplitude as well as current sharing between the parallel switching devices. Accurate loss prediction can be achieved by including the parasitics in the loss analysis.

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