A Systematic Approach to Critical Electrical Fault Mitigation Strategies in an Electric Vertical Take-Off and Landing (EVTOL) Electrical Propulsion Unit

A SYSTEMATIC APPROACH TO CRITICAL ELECTRICAL FAULT MITIGATION STRATEGIES IN AN ELECTRIC VERTICAL TAKE-OFF AND LANDING (EVTOL) ELECTRICAL PROPULSION UNIT

BY

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A THESIS

SUBMITTED TO THE DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING

AND THE SCHOOL OF GRADUATE STUDIES

OF MCMASTER UNIVERSITY

IN PARTIAL FULFILMENT OF THE REQUIREMENTS

FOR THE DEGREE OF

DOCTOR OF PHILOSOPHY

Doctor of Philosophy (2022) McMaster University

(Electrical & Computer Engineering) Hamilton, Ontario, Canada

TITLE:	A Systematic Approach to Critical Electrical Fault Mitigation Strategies in an Electric Vertical Take-Off and Landing (EVTOL) Electrical Propulsion Unit
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NUMBER OF PAGES:	xxi, 176

To my parents France Pageot and Djaafar Ramoul along with my brother Bryan Ramoul. Thank you for always being there and to never have given up on me. We all had our own battles and I am glad we have come out of them!

Abstract

The electric vertical take-off and landing (EVTOL) platform is opening a new market segment that is disrupting the commercial and military aircraft industry. This particular vehicle platform is filling the gap between road vehicles and aircrafts. The main idea is to avoid the gridlock in major metropolitan cities where a journey that should take 30 minutes now takes more than one hour. Key enablers such as the newly developed infrastructures known as Vertiports and the move of electrification of aircrafts have driven this new market segment with fast time to market. To enable the deployment of these EVTOLs in the commercial world, their fault behavior needs to be known as faults will happen, a fault mitigation strategy must be developed to ensure that when the fault happens, the EVTOL and its passengers along with its surrounding are protected from catastrophic failures.

To give a brief context on what these EVTOL platforms are, potential and developed EVTOLs in the market currently are introduced. The categorization of these platforms is done within four types of categories being Helicopters, Multi-Rotor, Lift & Thrust and Tilt-X. Their general advantages and disadvantages are discussed and the categories are rated in terms of which platform could be the most viable option to be in service by 2024. Their main electrical distribution system is introduced with their critical components and how they can fail. Each critical component such as the

battery, electrical propulsion unit (EPU), protection devices, power distribution units and auxiliary electrical loads are discussed in details.

The thesis discusses one of the main safety aspects of an EVTOL, which is protection of a propulsion unit. The critical electrical faults in the EPU are introduced along with their behavior on the EVTOL electrical distribution system (EDS). Open circuit faults and short circuit faults from the inverter and its power devices to the electric motor are analyzed. Furthermore, the sensor failures such as the rotor position sensor and the current and voltage sensors are discussed. The controller stage failures are discussed as well as it becomes a critical component that can fail in many ways.

Once the electrical faults are discussed, a fault mitigation strategy (FMS) is introduced for each fault ranging from a simple inverter disabling strategy, to a sensorless control law for the loss of position sensor. A protection device known as the solid state power controller (SSPC) is inserted at the input of the EPU and its design is discussed for a 270VDC/180A modular architecture. This SSPC becomes the redundant and final protection stage of the EPU to ensure if the developed FMS fail to protect the EPU, the SSPC can isolate the EPU from the rest of the EVTOL EDS. The main contribution of the thesis is the systematic approach to fault analysis and mitigation/protection strategies that were not addressed in literature so far for this type of platform. The use of a single FMS for multiple faults is introduced where the aim is to reduce the efforts for verification and validation (V&V) of the corresponding software and firmware. Finally, the practical implementation challenges of the SSPC are discussed and shown in experimental lab setups.

Acknowledgements

I would like to express my deep gratitude and appreciation to my supervisor Dr. Ali Emadi. I have learned a great deal on not only technical aspects of engineering but how to live and survive as an engineer and managing a team in this fast paced world. The knowledge I have acquired throughout my journey of a masters and Ph.D student has been quite fulfilling and priceless. I would also like to thank Dr. Babak Nahid-Mobarakeh for the endless discussions on technical help in the aerospace industry as well as helping me keep my french during the course of my studies at McMaster Automotive Resource Center (MARC).

I would like to thank the team at MARC for providing support and technical advise whenever needed. I would like to extend a special thank you to Alan Dorneles Callegaro, Silvio Rotilli Filho, Sumedh Dhale, Peter Azer, Mohamed Ibrahim, Nilou Kashmiri and many others for the laughs, tough moments we have gone through and technical help you have provided during my time at MARC. I would also like to thank Armen Baronian and Piranavan Suntharalingam for the endless support you have given me even though you did not have too! Also to Kyle Kozielski, Mohamed Omar and Haomin Li for providing support in the RTA5 team and to Gayan Amaradasa in RTA4 whenever I could not support at the end of my studies.

Finally, I would like to thank my family and for the endless support during my

professional and personal life. I could not have done it without your support and without the "take your kids to work" at L3 Communications where the spark for aerospace research started. I also would like to thank Julia Corcoran and her cat Jax for the countless hours of being there for me when I needed to unwind from the research.

This research was undertaken, in part, thanks to funding from Eaton Aerospace and MITACS.

Notation and Abbreviations

AEA	All Electric Aircraft
ARINC	Aeronautical Radio, Incorporated
BEMF	Back Electromotive Force
CM	Configuration Memory
DAL	Design Assurance Level
DC	Direct Current
DCCB	Direct Current Circuit Breaker
EASA	European Union Aviation Safety Agency
ECS	Environmental Control System
EDS	Electrical Distribution System
EMI	Electromagnetic Interference
EPU	Electrical Propulsion System
EVTOL	Electric Vertical Takeoff and Landing
FAA	Federal Aviation Administration
FCC	Flight Control Computer
FFT	Fast Fourier Transform
FMS	Fault Mitigation Strategy

FOC	Field Oriented Control
FPGA	Field Programmable Gate Array
FSA	Flight Surface Actuator
FSO	Fail Safe Operation
FTC	Fault Tolerant Control
FW	Firmware
HVDC	High Voltage Direct Current
HW	Hardware
IC	Integrated Circuit
ICE	Inernal Combustion Engine
IGBT	Insulated Gate Bipolar Transistor
IMC	Integrated MagnetoConcentrator
IPISL	Improved Proportional-Integral Sensorless Law
IT	Instantaneous Trip
ITSCF	Inter-Turn Short Cicuit Fault
KVL	Kirchoffs Voltage Law
LD	Long Delay
LPF	Low Pass Filter
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
MCAS	Maneuvering Characteristics Augmentation System
MEA	More Electric Aircraft
MOV	Metal Oxide Varistor
NCAA	National Civil Aviation Agency of Brazil
NASA	National Aeronautics and Space Administration

OCF	Open Circuit Fault
OPF	Open Phase Fault
PCB	Printed Circuit Board
PDU	Power Distribution Unit
PPDU	Primary Power Distribution Unit
PI	Proportional Integral
PLL	Phase-locked-loop
PM	Permanent Magnet
PMSM	Permanent Magnet Synchronous Motor
P2PSCF	Phase-to-Phase Short Circuit Fault
PWM	Pulse Width Modulation
RAM	Random Access Memory
RMS	Root-Mean Squared
RPS	Rotor Position Sensor
SEU	Single Event Upset
Si	Silicon
SiC	Silicon Carbide
SOC	State of Charge
SPDU	Secondary Power Distribution Unit
SW	Software
SRAM	Static Random-Access Memory
SSCB	Solid State Circuit Breaker
SSPC	Solid State Power Controller
TRL	Technology Readiness Level

TVS Transient Voltage Suppressor

UK United Kingdom

V&V Verification and Validation

VTOL Vertical Takeoff and Landing

WIPS Wing-Ice Protection System

Contents

List of Figures

List of Tables

List of Algorithms

Chapter 1

Introduction

1.1 Background and Motivation

With the advancements of technology in the field of automobiles, reduction of ownership costs and the convenience of having a personal automobile has become an integral part of the human life. Based on data acquired by Hedges & Company, there were 284.5 million registered road vehicles in the United States in 2019 with expectations that this number will increase in the years to come [9]. With high volume of cars, the traffic is bound to increase if the infrastructure is not changed. This results in someone's drive to work from San Francisco's Marina to downtown San Jose, now taking over two hours [10]. Similarly, a drive from Hamilton to Toronto in Canada has become more than two hours during rush hour due to the increased traffic even though the main highways are over six lanes each. Now, imagine if one could decrease this commuting time to say ten minutes instead of two hours by flying in a Vertical Take-Off and Landing (VTOL) aircraft.

VTOL aircrafts have been widely known in the aerospace industry where the

first manned VTOL flying machine was developed in 1907 by Paul Cornu [11, 12]. Although the flight was successful, the reliability and safety of the aircraft was inadequate. Fast-forward to the 21rst century, society has become more aware of its environmental footprint and impact due to fossil fuels to power cities and transportation. Electrification of land, sea and air transportation is an inevitable trend and has been widely accepted by the public worldwide [13–15]. The transition from conventional aircrafts to more electric aircraft (MEA) and all electric aircraft (AEA) requires electrical energy to do the job that pneumatic, hydraulic and mechanical energy used to do in the past [16, 17]. These jobs include (but are not limited to) the wing ice protection system (WIPS), flight surface actuators (FSA), environmental control systems (ECS) and the removal of the use of bleed-air to start the main propulsion system [13, 18, 19]. The most recent trend within electrification is electrifying the drive system of an aircraft. The first vehicle that is getting electrified is the so called VTOL. By electrifying the VTOL, an electric vertical take-off and landing (EVTOL) aircraft is born!

EVTOL is opening a new market segment in air transportation that is filling the gap between passenger vehicles and aircrafts. The advantages that EVTOL offers are significant but due to its low technology readiness level (TRL), more technology development in multiple areas of electrification is needed. With the advancements in residential and industrial electrical distribution systems (EDS), the same technology can be leveraged for EVTOL applications. Many startup companies such as Lilium [20], Joby [21], Volocopter [22], KittyHawk [23] and others have started designing their own EVTOL aircrafts with different architecture and topologies. As well, big players in the aerospace industry such as Airbus and Embraer have started to develop their

own EVTOL platform respectively as the CityAirbus NextGen [24] and the EmbraerX EVTOL [25].

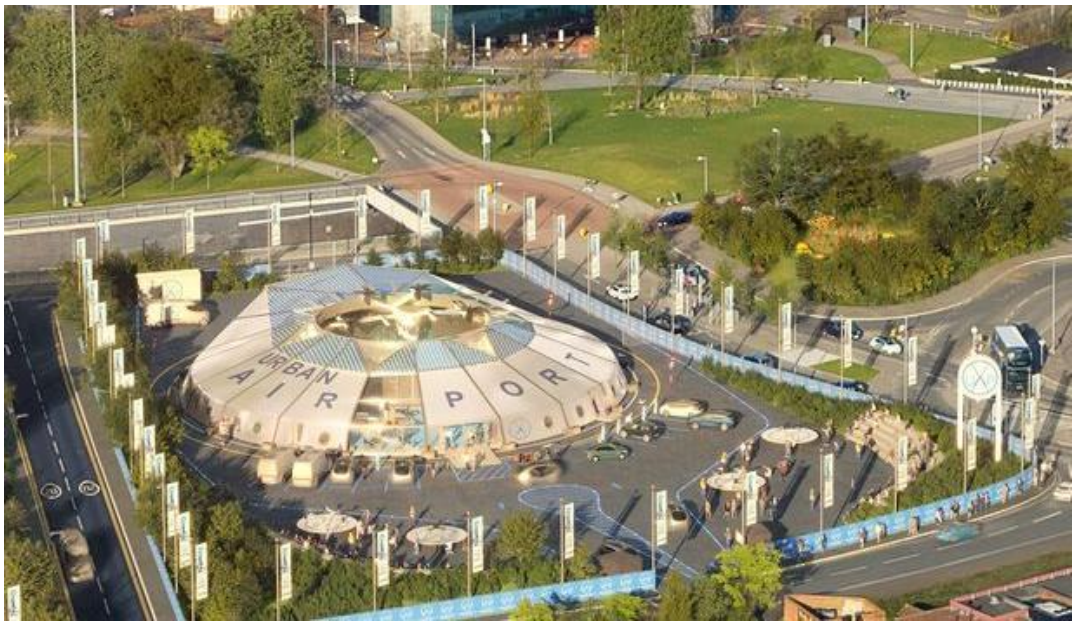


Figure 1.1: Existing vertiport in Coventry city centre in the UK [1].

One of the important enablers for the EVTOL is the infrastructure to support this new market segment. Existing helipads and airports are natural choices to support initial air taxi routes, as they are already equipped with adequate physical space, air traffic control processes, and supporting personnel. In the early years of EVTOL, new vertiports will likely be built on city outskirts, thus allowing city-to-city hops while minimizing the need to fly over other infrastructure. Finally, the vertiports built on the rooftops will enable flights from building to building within a city. An example of a vertiport that has already been built exists in Coventry city center in the UK shown in Fig.1.1 [1]. A completely new air traffic management and autonomous flight

operation that needs to be developed may enable mass-scale adoption of the new means of transport within the next 10 to 20 years. Once the EVTOL technology is proven on existing and adapted infrastructure the next step will be to enable access to charging, air clearances, and proximity to ground transportation.

The next enabler for the EVTOL is related to the work performed in the electrification of aircrafts which is very similar to the one exhibited in the automotive industry where mechanical components are being replaced with electrical components [26]. A major challenge that exists in the electrification of aircrafts is the safety level requirement with these new electrical components and systems. In the paper [13], the authors provide a flowchart for the accepted means of compliance for functional safety of avionics hardware and software on conventional aircrafts. Unlike a road vehicle, an aircraft cannot simply "pull-over to the side of the road" if there is a failure. The aircraft must fail safely in the air and still have the ability to land. Although the distributed EDS and propulsion, which are usually present in these newly developed EVTOL applications [7], present many advantages such as increased efficiency, they also present challenges for component integration as the vehicle becomes more complex [27, 28]. Therefore, components and solutions used in electrical aircraft may pose challenges to the airworthiness certification standards which may be different from the ones used for conventional aircrafts [13]. Thus, the adaptation and creation of new standards and guidelines by authorities such as European Union Aviation Safety Agency (EASA), National Civil Aviation Agency of Brazil (NCAA) and the Federal Aviation Administration (FAA) may be necessary to enable this new class of vehicle. To demonstrate the importance of safety, a recent example occurred to the

aircraft manufacturer Boeing on its 737-MAX aircraft. What was presented as a simple software change known as the Maneuvering Characteristics Augmentation System (MCAS), led to the grounding of the aircraft for one year due to two catastrophic events that lost the lives of 346 people [29].

Currently, the state of the art of protection and mitigation strategies for faults within the electrical propulsion unit (EPU) of an EVTOL are not well understood. This thesis provides a systematic approach for analysis and a methodology for mitigating the problems related to a typical EVTOL EPU failures. The main focus of this thesis are the analysis and fault protection of an EPU in an EVTOL. This thesis also addresses the mitigation and protection strategies for the most critical electrical faults that can happen within an EVTOL EPU. Furthermore, the methods developed are taking into account an additional constraint such that if a fault occurs, the EVTOL aircraft must land safely. The simulation and experimental results support the theoretical developments.

1.2 Thesis Contributions

This thesis provides four main contributions to the development of fault mitigation strategies for an EPU in an EVTOL. First, a state of the art review of the current aerodynamic EVTOL concepts and their typical EDS is provided. Existing EVTOL concepts that are currently applying for type certification in the near future are presented along with a summary table of pros and cons for the concepts discussed. The review presents a typical electrical architecture of an EVTOL with the emphasis on a minimum required components in the architecture considering a power source, electrical loads, power distribution unit and protection devices.

A detailed analysis of the most critical electrical failure modes in EVTOL EPUs is presented. The effects of these electrical failure modes on the possible flight behavior of the EVTOL are analyzed to understand the faults criticality. To meet a safe landing requirement during failure modes, the design of appropriate fault detection and protection strategies is addressed. The main goal behind this study is to safely land the aircraft if a critical electrical failure occurs during cruising phase of the EVTOL flight profile. Some of the studies have been published in [30].

Furthermore, the thesis contributes to the detailed development of a solid state power controller (SSPC) for providing critical protection functionality to EVTOL EPUs and its crucial role that it is playing in protection of future EVTOL platforms. The SSPC is proposed as the input of the EPU such that when the EPU's inverter controller fails to detect a critical short circuit or overvoltage (OV), the SSPC would be the redundant protection device to protect the rest of the EVTOL EDS regardless of the EVTOL concept.

At last, a thorough development and introduction of fault mitigation strategies (FMS) are applied to the critical electrical faults that can occur in the EVTOL EPU. These FMS range from firmware implementation to directly using the SSPC as the final stage of protection against these failure modes. Also, to make the development of firmware (FW) and software (SW) easier which would ideally decrease certification efforts, single FMS methods are applied to more than just a single failure mode.

1.3 Thesis Outline

The thesis is organized into six chapters. In Chapter 1, the concept of EVTOL is introduced and benefits of this new technology are outlined. The challenges related

to protection of EDS on such vehicles are introduced and motivation for this these has been presented. Furthermore, the problem of designing a fail safe EPU for an EVTOL utilizing new technology is addressed. Certification challenges and technology readiness level (TRL) are outlined in Section 1.1. The list of main contributions of this thesis are stated in Section 1.2.

In Chapter 2, a typical aerodynamic and electrical architecture of an EVTOL is introduced. A state of the art review is presented based on the existing EVTOL concepts that are seen on the market and are in process of applying for type certification in the near future. Furthermore, in Section 2.2, the minimum number of components required in a typical electrical architecture of an EVTOL is described along with their function on the aircraft. The power source, power loads, power distribution unit (PDU) and protection devices are introduced at the system level.

In Chapter 3, the normal operation and critical electrical failure modes are identified for a typical EVTOL EPU. The electrical faults of interest in this thesis include open circuit in Section 3.2, short circuit faults in Section 3.3, communication loss in Section 3.4.4 and of control stage failure in Section 3.4. The fault effects at the system level of the EPU are addressed.

In Chapter 4, the design of mitigation strategies and protection methods for the faults introduced in Chapter 3 are elaborated. To ensure that the EVTOL can land safely under any of the fault conditions, an appropriate design and protection strategy needs to be employed. The additional contribution of this thesis is that for each electrical failure mode that can happen, an analysis is performed to understand the severity of the fault reflected on the safety of flight. If a fault is critical, lives on the EVTOL may be lost and adequate design is mandatory to ensure protection or

mitigation strategies for such scenarios are in place.

In Chapter 5, simulation and experimental results are presented. To validate the theoretical methods developed and outlined in Chapter 4 of this thesis, the simulation results are presented in Chapter 5. A full agreement between theoretical analysis and simulation results has been demonstrated and documented. Some of the simulation results have been validated through experiments. Finally in Chapter 6, conclusions are drawn and future topics of interest to advance the research in this area are outlined.

Chapter 2

State of the Art Architecture of an EVTOL

This chapter introduces the state-of-the-art EVTOL model architectures with existing prototypes and concepts. The typical EDS architecture for an EVTOL is introduced along with the necessary critical components such as the battery, electric motor, inverter and protection devices. Furthermore, the EPU is introduced in details outlining the electrical and mechanical components.

2.1 State-of-the-Art EVTOL Concepts

In 2018, the National Aeronautical Space Association (NASA) presented three key vehicle designs for air taxi operations ranging from a 250lb to 3000lb payloads and having a range of 100km to close to 1000km [31]. The first concept consists of the electric quadrotor concept with up to one passengers, a payload of 300lb, and a range of up to 100km. The second concept consists of having up to six passengers, a payload

of 1200lb, and a range of 2200km but has a hybrid propulsion. With the advancements of technology, this concept has been adapted to fully electric, in some cases, and is currently being used by many companies trying to develop EVTOL concepts and will be the focus of this thesis.

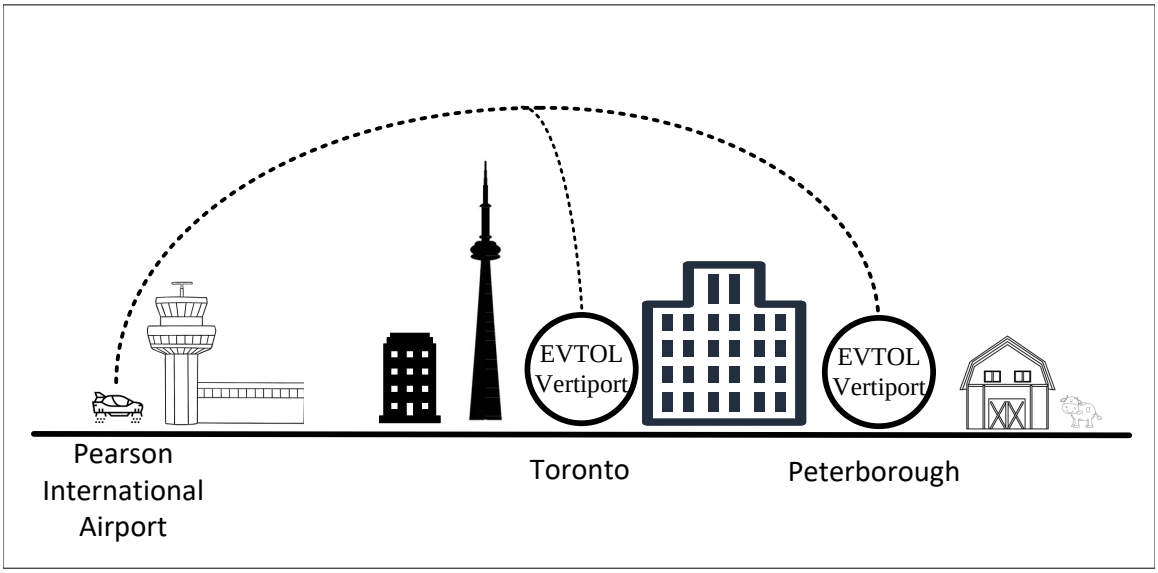


Figure 2.1: Typical flight profile envisioned for inter and outer city EVTOL based on [2].

Due to the many EVTOL concepts, a categorization of its basic models is needed. Many different companies have developed different types of EVTOL models as mentioned in Chapter 1 which meet the requirements outlined by NASA in [31], but each one of these developed models have their own advantages and drawbacks based on the time to market, maximum travel speed, fail safe mechanisms, weight, maximum flight time and many more aspects. The concept of having EVTOLs for air taxi purposes within the next five years is pictured in Fig.2.1. The EVTOL would follow a specific flight profile with a known start, like an airport, and end points being vertiports or

helipads, just like commercial aircrafts with airports as being their destinations. The EVTOL would have a flight altitude between 2000 to 3000 meters, a flight range of 200 to 300 km and a cruise speed of 200 to 300km/hr. For example, currently a commute in car from the Pearson international airport to downtown Toronto can take upwards to one hour due to the congested roadways. A flight with the EVTOL would take roughly ten minutes and could take you anywhere in the city without waiting for the train or subway or having to wait in congested roads.

2.1.1 Helicopter

The helicopter EVTOL model consist of retrofitting existing internal combustion engine (ICE) into purely electric motor drives. This process ensures a low risk of failures as the aircraft aerodynamic and construction is well known. Helicopters have been used in search and rescue, firefighting, police services and for ambulance purposes [32]. The typical helicopter has one main propeller providing the lift and thrust while it has second propeller, known as the horizontal stabilizer, which directs the aircraft in a certain direction [33]. One of the most known architecture of a helicopter is shown in Fig.2.2. Standards and guidelines exists for this type of model which makes certification efforts easier [33]. The main disadvantages consist of having a low flight duration with a low air speed of the vehicle. Also, helicopters are known to generated high amounts of noise due to its single propeller design. In failure conditions such as a motor driver failure, the helicopter can land with auto gyro of main propeller albeit with a harsh but safe landing [33].

Figure 2.2: Example of helicopter aerodynamic structure from the Robinson 44 [3].

2.1.2 MultiRotor

The Multirotor concept is a well known technology used in both military and commercial zones [34]. Multirotors have been used in manned and unmanned applications from a simple burrito delivery system in [35] to complex military procedures [36]. Delivery services also use these types of aircraft to facilitate their delivery protocols [37]. Multirotor aircrafts tend to have from four to having possibly eight propellers providing lift and thrust to the aircraft. By changing the speed of each propeller, the MultiRotor EVTOL can change its position. Their fail safe mechanism is having a parachute in case propulsion of aircraft is no longer available [24]. The MultiRotor has the advantage to have a robust control in unpredictable weather, lower noise than helicopters, and have no movement of propeller arms. Their main drawbacks include

a short flight duration, low speed and low lift to drag ratio. There are no current standards to certify this type of aircraft which would make increase certification efforts. A typical multi-rotor is shown in Fig.2.3.

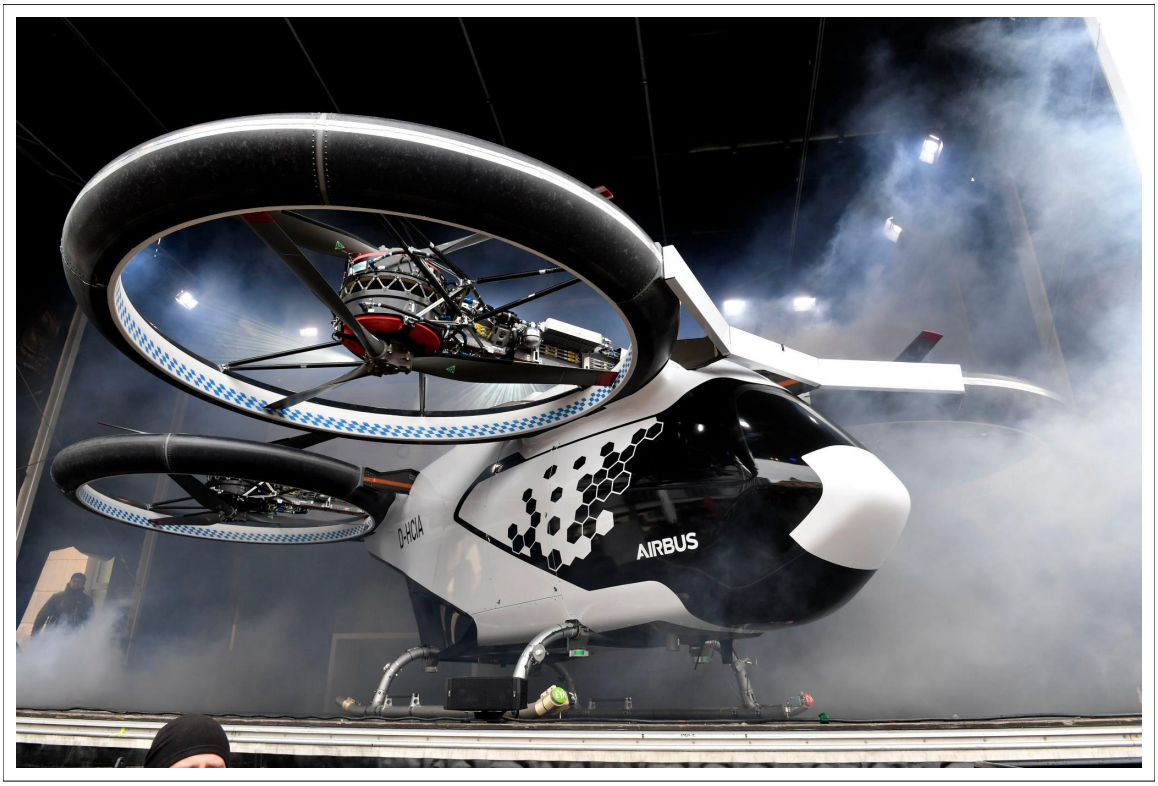


Figure 2.3: Example of Multirotor aerodynamic structure from CityAirbus NextGen [4].

2.1.3 Lift and Thrust

The Lift and Thrust concept starts the flight like a helicopter by using two main lift propellers. The EVTOL then goes into horizontal flight with the help of its thrust propellers as depicted in Table 2.1. For a single lift propeller, once the aircraft is moving horizontally, the lift propellers are then in autogyro function [38, 39] which

could be used as generators if needed. When multiple lift propellers are used, the propellers are tucked away to avoid all possible drag during horizontal flight but could be used to recuperate any energy as well [40]. In both cases, the fixed wings are used to provide the lift of the aircraft [40]. The lift and cruise models usually have ducted propellers for better power/thrust ratio and noise reduction [41]. Although propeller in duct usually improves noise and power/thrust ratio, it also brings bigger weight and manufacture cost [41]. The main advantages of Lift and Cruise EVTOL includes simple control, potential high speed, no movement of propeller arm, lower noise than helicopters, and long flight distance. Their main drawback include its weight due to the fact that both lift and thrust propellers have different functions and are not used simultaneously. Further more, the single push propeller does not allow the aircraft to fly over inhabited area in case of emergency landing.

Figure 2.4: Example of Lift and Thrust aerodynamic structure from Eve Air mobility, formerly known as the EmbraerX [5].

2.1.4 Tilt-X

The Tilt-X concept can have a tilted wing and motor or just tilted motor system [42]. There are more variants like this concept, that do not differ in power management system. Some of them have tilted propeller and some of them have ducted propellers. This concept is aiming all the benefits from force distribution along the whole airplane. These airplanes have low power/thrust ratio of single motors, but there are advantages of distributed motors which improve the total aerodynamics of the plane. These concepts have a modular EPU design to enable easy maintenance. Moreover, these

concepts are resilient to power or motor loss failures. When a single motor fails, the plane can still fly. This architecture seems to be one of the most advantageous but having a complex EVTOL platform. They have the advantage of having propellers that provide both lift and thrust simultaneously only by rotating the propeller arms. Furthermore, their operation is quite simple and have low noise capabilities. Some of their disadvantage include the complexity of that rotating propeller arm, low power to thrust ratio and current no standards exist for this type of aircraft.

Figure 2.5: Example of Tilt-X aerodynamic structure from the Lillium Jet [6].

2.1.5 Summary of EVTOL Concepts

By combining all main EVTOL models into the four mentioned aerodynamic structures, a summary rating of their time to market, fail safe landing, noise emissions, flight time and speed, development price and complexity is presented in Table 2.1. Important factors to be analyzed is that many manufacturers want their EVTOL to be in operation by 2024 at latest but also have the ability to adapt to the ever changing world of technology and transportation. Furthermore, the EVTOL must have minimal noise emissions due to their proximity to cities and wildlife. The EVTOL also would need to have a long flight time and speed in case of emergency vehicles.

Table 2.1: Summary of advantages and drawbacks for each category of EVTOL models.

	Helicopter	Multi-Rotor	Tilt-X	Lift & Thrust
Time to Market	++	+	- -	-
Fail Safe Landing	++	- -	+	+
Noise emissions	- -	++	++	+
Flight Time	-	-	+	++
Flight Speed	-	-	++	++
Complexity	++	+	- -	-

As can be seen, to provide adequate and quick feedback for the development and certification efforts of EVTOLs for commercial air taxis or emergency vehicles, the electric helicopter has the best time to market although it does not provide good noise emissions, flight time or speed. In terms of noise emissions, flight time and speed, it seems that the other three platforms would win the case. The main merit to see

would be the time to market where the Lift & Thrust EVTOL models seem to be the most viable option for an EVTOL model to be in service by 2024 for both emergency and commercial operations. The thesis will focus solely on these types of EVTOL models hereon.

2.2 Typical EDS Architecture of an EVTOL

A typical EVTOL EDS is shown in Fig.2.6. The EVTOL EDS can be considered as a DC microgrid. Although different EVTOL models have very different flight control, their EDS are relatively similar consisting of an energy storage, auxiliary electrical loads, primary power distribution unit (PPDU), secondary power distribution unit (SPDU), electrical propulsion unit (EPU) and protection devices. The main power source of the EDS in an EVTOL is comprised of a Li-ion battery providing a high voltage direct current (HVDC) which provides electrical power to the EPU through a PDU comprised of protection devices and wiring. Having the HVDC at the battery side helps to minimize the weight of the copper in the cables as was demonstrated with the HVDC of +/-135V and +/-270VDC on the F-22 and F-35 military aircrafts [43]. The HVDC in the EVTOL EDS is 800VDC. Furthermore, power is distributed to the low voltage electronics loads by the means of a DC/DC converter which steps down the 800VDC to a nominal 28VDC. This is because in an aircraft, maximizing power density is of high importance. The other important factor is to ensure a specific safety level is achieved which would require the EDS to have fail safe operation (FSO) during failure modes. This can be done with redundancy or designing for peak power, but both of those solutions reduce power density. The optimal solution is found by minimizing the difference between peak power and average power [44]. Many faults

can occur in a HVDC microgrid such as short circuit faults, open circuit faults, control failure, component degradation or malfunction, and other mechanical and electrical faults [45–47]. The components in the EDS must be properly designed and coordinated between each other to ensure a state of FSO is achieved for the EVTOL.

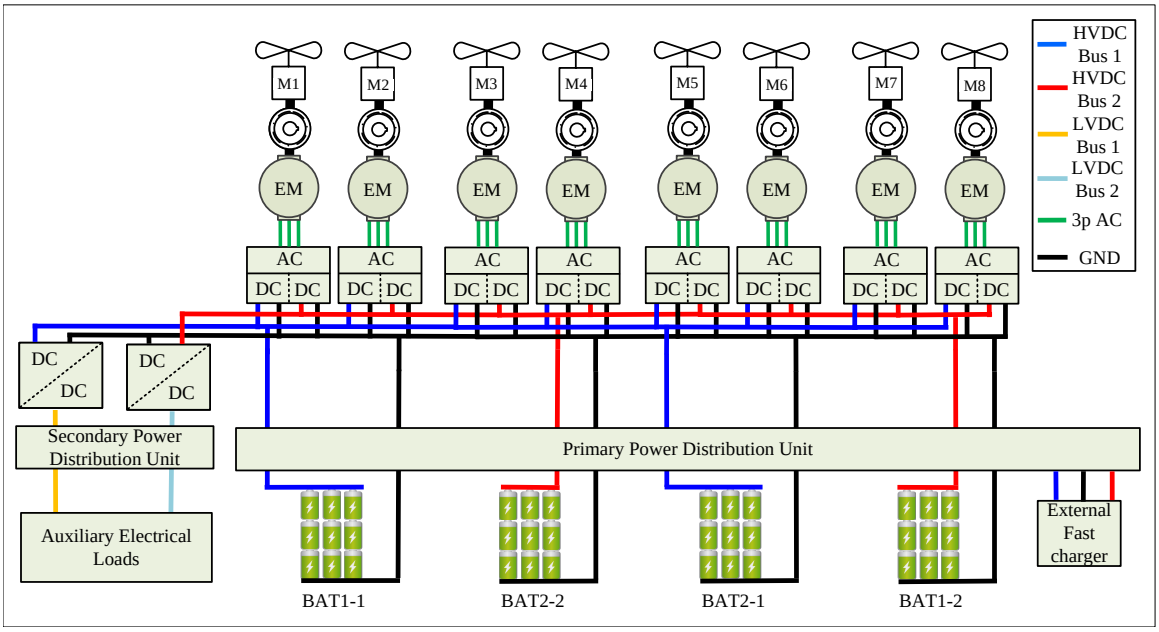


Figure 2.6: Typical EDS for an EVTOL based in [7].

2.2.1 Energy Storage

EVTOL EDS mainly use Li-ion batteries as the main energy storage [13]. They are well known and used in many applications such as automotive, microgrids, personal devices and many more applications [48, 49]. Batteries are rated with kWh and for EVTOL applications, the energy rating are from 100kWh to 200kWh depending on the EVTOL [31]. Just like any other components, the battery has complex fault scenarios such as overcharging and discharging, overheating, internal and external

short circuits, chemical leakage, swelling, degradation and thermal runaway [50]. Due to them being the sole energy storage on the EVTOL, their safety is very important [50]. Li-ion batteries have been known to catch fire under certain fault conditions like that in Boeing's 787 Dreamliner [51] and also in personal devices [52]. One of the main theory behind the fires attributed to Li-ion batteries is linked to their thermal runaway properties [53, 54]. Fig.2.7 depicts the components inside a typical battery pack system since EVTOL manufacturers will be integrating Li-ion battery packs already assembled into the EVTOL. It consists of the battery module consisting of many singular battery cells. Each cell (or branches of cells) is monitored through its temperature, current and voltage to ensure that they are balanced which will limit the aging of the battery cells and this is done through the battery management system (BMS). The BMS can fail in ways where power supply is no longer valid, or erroneous control is present.

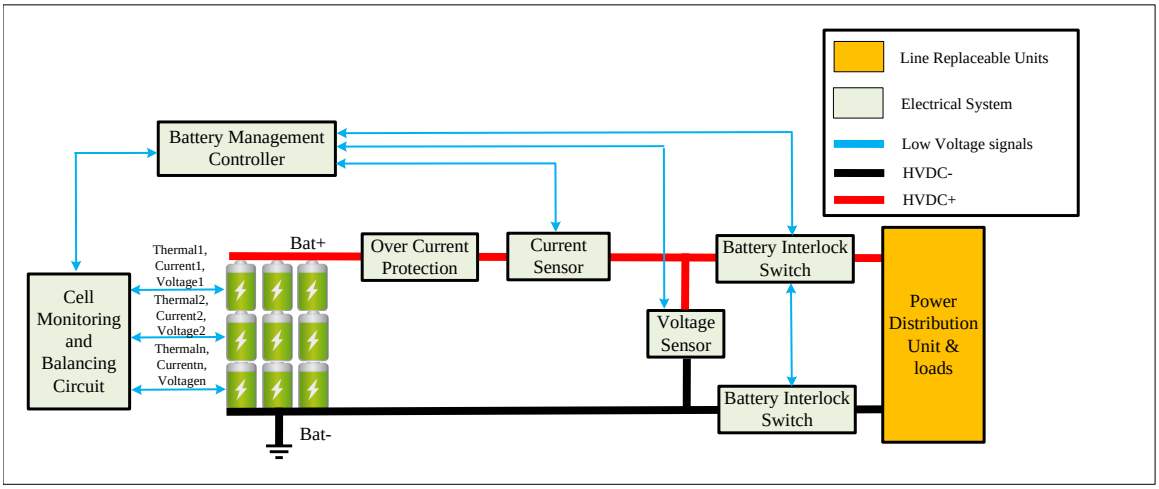


Figure 2.7: Block diagram of a typical battery pack system with protection and BMS.

If the BMS fails or any other components in the battery system it is necessary to

ensure that the EVTOL is protected if a short circuit occurs internally or externally of the battery. The main parameter of the battery that is of interest for its short circuit capabilities include the internal impedance and external cable impedance [55–57]. Typically, a li-ion battery is modeled by its first-order equivalent circuit model (OCV-R-RC) with the help of open circuit voltage (OCV) experimental data of a single cell [58]. Internally to the battery, its own impedance would contribute to the short circuit capabilities. Furthermore, once this battery is connected to a load, that load's impedance will also affect the short circuit capabilities of the battery along with the impedance of the cable that is used to connect the battery to the component [57]. With a known energy rating of the battery and the impedance of the EDS, the short circuit capabilities of the battery can be known and the EDS components can be protected through design. To ensure external short circuits of the battery are dealt with, there is over-current protection with interlock safety switches to ensure the battery is disconnected from the rest of the aircraft.

Another parameter of the battery that is very important for safe landing is the state-of-charge (SOC) of the battery. When a short circuit current is seen by the battery, the SOC would dramatically reduce and may reduce to a point where landing is no longer achievable since it is directly proportional to the current of the battery [58]. Fast detection of the short circuit current is critical for the EVTOL flight and energy storage [59].

2.2.2 Electrical Propulsion Unit

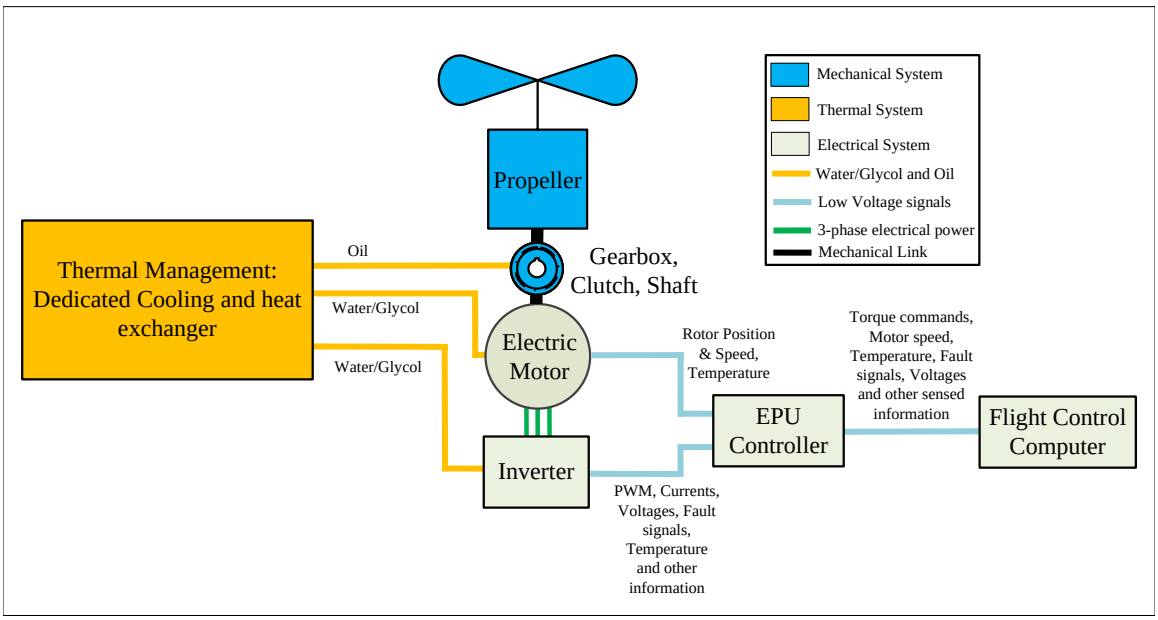


Figure 2.8: EVTOL EPU airchitecture.

The EPU is a critical component of the EVTOL EDS as it provides movement for the EVTOL. The typical EPU in an EVTOL is shown in Fig.2.8. It includes an inverter, a permanent magnet synchronous machine (PMSM), a mechanical link, and a control board. When designing an EPU for an EVTOL, the performance objectives and power requirements are defined based on several factors, such as the size of the EVTOL, the number of passengers, and the expected flight time and distance [60]. Another key aspect of EPU design is the fact that the EPU must be able to handle its failure modes. Each component in the EPU has its own failure modes and different methods are used to protect the EVTOL from them.

One of the main component in the EPU is the inverter. It is a three phase, two level inverter with six MOSFETs. The inverter has a DC link capacitor which provides

large current demands and includes three current sensors and a voltage sensor. By controlling the MOSFETs appropriately, an AC current waveform is supplied to the PMSM from the DC link capacitor. To ensure this is done properly, the inverter needs to function normally. Many faults can occur in the inverter which would cause it not to function properly. The MOSFETs may be faulty where an open failure or short failure could occur [61,62]. The DC link capacitor may also have been damaged and thus its capacitance is not the same anymore [63, 64]. Furthermore, the sensors themselves may be damaged and thus not provide a proper reading for controlling the inverter current [62].

The PMSM provides the means to transfer the electrical energy to mechanical energy. Due to the high safety level of the PMSM component, appropriate control and monitoring functions are needed to ensure its safe and reliable functionality just like that with ICE or turbo engines in a conventional aircraft [19]. The PMSM can fail in many ways such as having a phase to phase short circuit or open phase [30], inter-turn short circuit [65, 66], and demagnetization of the magnets [65, 67]. Other possible faults that could occur on the inverter or PMSM components is a phase to neutral and phase to ground fault [65].

The control board is the heart of the EPU as it manages the control of the speed, torque and state of the EPU. The control board not only provides control but also monitors the EPU to ensure it is within the specified requirements of the design [68]. If an abnormal condition is detected, a flag is asserted to make sure that other components in the EVTOL know that a failure has occurred. Many failures can also occur at the controller level such as error in control, controller failure [69] and also single event upsets (SEU) where a logical cell in the controller chip is altered due to

external radiation [70].

The mechanical link is the final stage which provides the movement of the aircraft. The mechanical link consists of a gearbox to increase the torque output of the PMSM and a propeller or a fan which provides lift and thrust for the EVTOL [7]. Since the mechanical link provides the movement, it is a crucial component and its reliability and safe behavior are needed to appropriately move the EVTOL. Some ways that the mechanical link may fail could be due to gearbox jam [71, 72], bearing failure [73], loss of lubrication and possible contact of the shaft with another component [74, 75].

Other possible failures that may arise in the EPU consist of communication loss from avionics [76], loss of cooling for the EPU and improper manufacturing of components [77].

2.2.3 Protection Devices

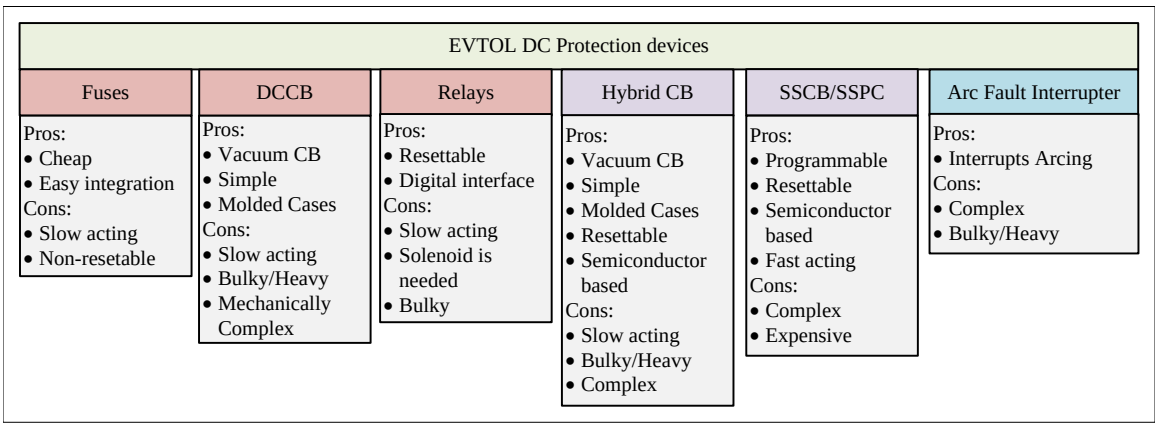


Figure 2.9: Summary of DC protection devices in EVTOL based on [8].

The EVTOL EDS can be considered as a DC microgrid. The typical DC microgrid protection devices used are shown in Fig. 2.9. Protection devices play an important

role in the EVTOL EDS by detecting and then protecting the EDS against critical electrical faults such as short circuit currents, over voltages and faulty operations [78, 79]. Different types of protection devices have been developed depending on the electrical configuration and requirements.

Fuses have been conventionally used due to their simple and cheap design. The challenge with fuses is that they are a single use device and cannot be reset [80, 81]. Furthermore, DC circuit breakers (DCCB) have also been used extensively in conventional aircraft but they tend to be bulky, heavy and slow [45, 81].

Solid state power controllers (SSPC), also known as solid state circuit breakers (SSCB), are semiconductor based devices and provide fast response to electrical faults whenever they are tripped [82, 83]. SSPCs also provide the benefit of having programmable logic embedded in them to make them configurable for the appropriate application. The semiconductor technology used in SSPCs provide high voltage and current capabilities, low conduction losses and no internal arcing [84].

Even though the protection devices offer protection to the EVTOL EDS, they also can fail in their own ways due to their internal components [85]. If an SSPC is used in an EDS to distribute power from the battery to the EPU, then it must operate safely in all modes. If for some reason it fails, a mitigation strategy must be designed. Redundancy is a good way to include this safety [86]. If one SSPC fails, the other SSPC would be turned on and provide the power until a safe landing is achieved. Furthermore, the SSPC may monitor its own parameters such as current, voltage temperature and other aspects to ensure that safe functionality is obtained.

2.2.4 Primary Power Distribution Unit

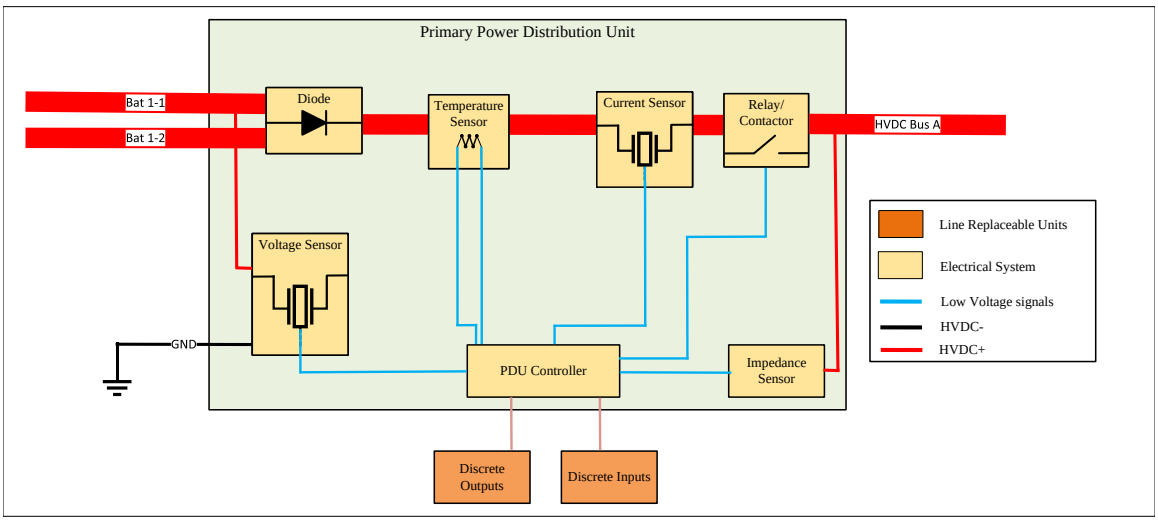


Figure 2.10: Typical architecture of an electric aircrafts PDU.

To ensure power is delivered safely and efficiently from the battery to the EPU, a PPDU is used [87]. Depending on the EVTOL range, the PPDU is appropriately sized to meet the power load demands [88–90]. Ideally, the PPDU includes the protection devices mentioned in section 2.2.3. The PPDU's reliability and safety if of utmost importance in EVTOL EDS since if the PDU fails, the EVTOL will no longer have the ability to safely distribute power to the EVTOL [91]. Redundancy has been one method to overcome the reliability issues of the PDU but also presents challenges as it increases weight [89]. Typically, there are two main PPDUs on the EVTOL, a right PPDU and a left PPDU [90]. This ensures that different power distribution methods are present on the EVTOL which makes the probability of failure lower than if only one PPDU were to supply the complete EVTOL.

The PPDU comprises of high power diodes, protection devices and relays, voltage

sensors, current sensors, temperature sensors, insulation/impedance measurement devices, discrete inputs and outputs and a main controller which provides the necessary firmware (FW) to control and monitor the distribution of power throughout the EVTOL. The PPDU has at the least an design assurance level DAL-B (if not DAL-A) which means that it could result in catastrophic failures if something would behave in the wrong method [92, 93]. Electrical power is distributed through either large gauge cables or large bus bars which can handle a high current of sometimes more than 2000A [13]. Furthermore, with recent MEA, AEA and EVTOLs, the PPDU must handle not only large currents but also high voltages of 800VDC to 1.2kVDC [60, 94].

2.2.5 Auxiliary electrical loads

The others loads included in the EVTOL that require attention consist of cabin and exterior lighting, wing-ice-protection system (WIPS), environment control system (ECS), flight surface actuators (FSA) and entertainment systems. Depending on the safety level of the component, these systems can fail and just be turned off or disconnected from the main bus through the SPDU to ensure they do not interfere with flight or mission critical components such as the EPU or battery [13]. The SPDU ensures that appropriate power quality is supplied to these auxiliary loads.

Chapter 3

Critical Electrical Failure Modes of an EPU in an EVTOL

In this chapter, critical electrical failure modes in an EVTOL EPU are introduced. In the fast paced environment of EVTOL development, understanding the critical electrical failure modes that is applicable to EVTOL would help to reduce the development time and increase the platforms functional safety assurance. Furthermore, to enable protection of these failure modes, a thorough investigation into the cause of these failure modes is needed along with their behavior at the system level. Mathematical modeling of these failure modes is demonstrated in this chapter. Healthy operation of the EPU is demonstrated first as a baseline of the intended EVTOL EPU behavior before understanding the failure modes of the EPU.

3.1 Healthy Operation of a Typical EVTOL EPU

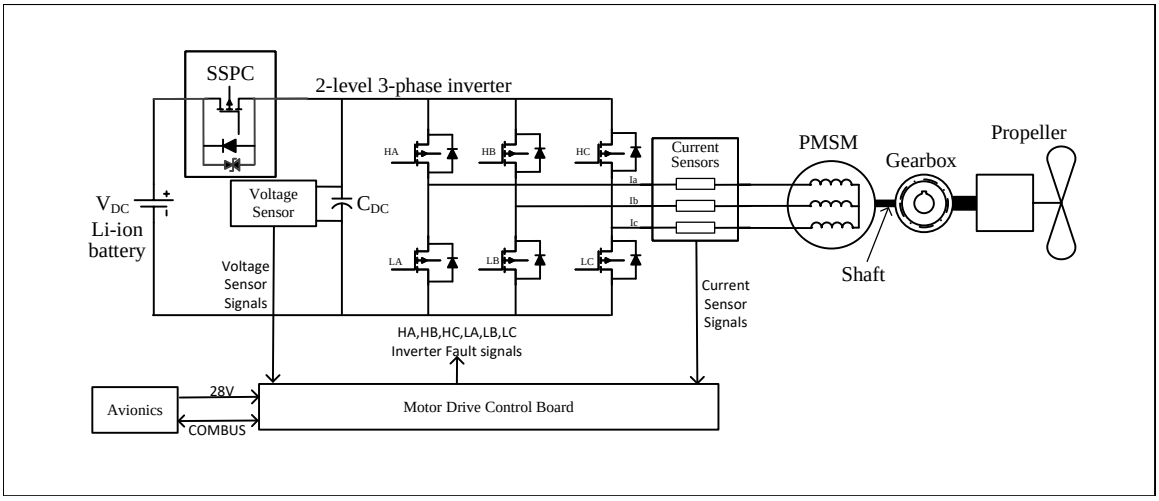


Figure 3.1: Typical healthy EPU for EVTOL.

To understand the behavior of an electrical fault occurring in the EPU, the healthy operation of the EPU needs to be well understood. A typical EVTOL EPU is shown in Fig.3.1. The EPU can be divided into three main categories being electrical, mechanical and thermal. The electrical behavior directly influences the mechanical behavior and thermal behavior. The healthy operation of an EPU consists of having proper input DC voltage supplying the DC link capacitor, then controlling the three phase currents for the PMSM to provide the necessary speed and torque to make sure the aircraft flies safely.

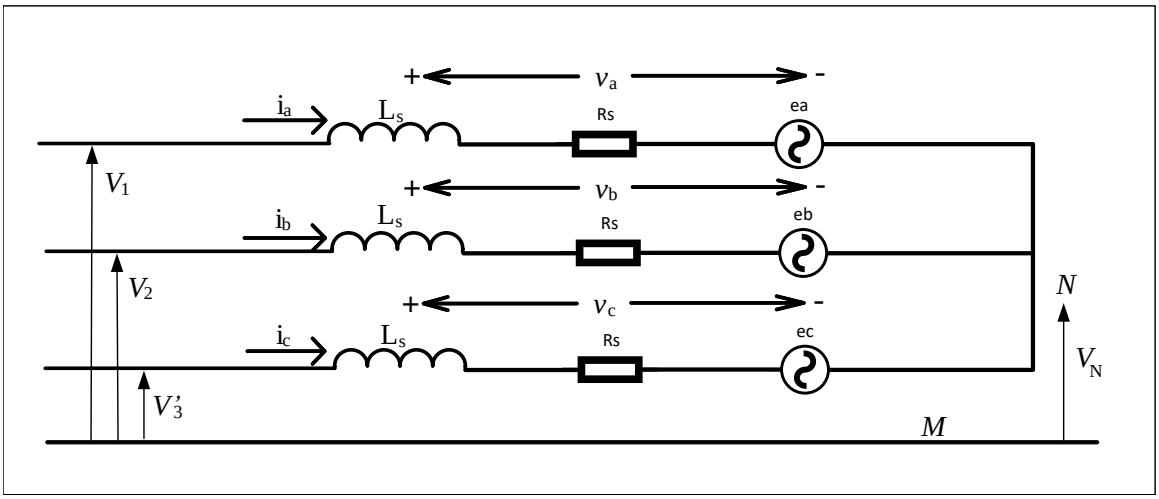


Figure 3.2: Healthy PMSM equivalent electrical circuit.

To start, a healthy PMSM electrical equivalent circuit is needed. The equivalent electrical circuit of a PMSM comprises of three identical phases consisting of an inductor, resistor and a back electromotive force (BEMF) voltage source which is proportional to the speed of the rotor as shown in Fig.3.2. In a healthy, balanced PMSM with an isolated neutral point, the relationship between all three phase currents is demonstrated in (3.1) and the phase voltages provided by the inverter are described in (3.2). The PMSM is configured as a fractional-slot concentrated winding machine which introduces physical space to reduce the probability of creating ITSCF, which is itself a mitigation technique [95]. Knowing the inverter healthy output voltages V_1, V_2, V_3, PMSM pre-fault phase voltages v_a, v_b, v_c, and neutral point voltage V_N in (3.2), the electrical fault conditions can be understood.

$$i_a + i_b + i_c = 0 \tag{3.1}$$

$$V_1 = v_a + V_N, V_2 = v_b + V_N, V_3 = v_c + V_N \tag{3.2}$$

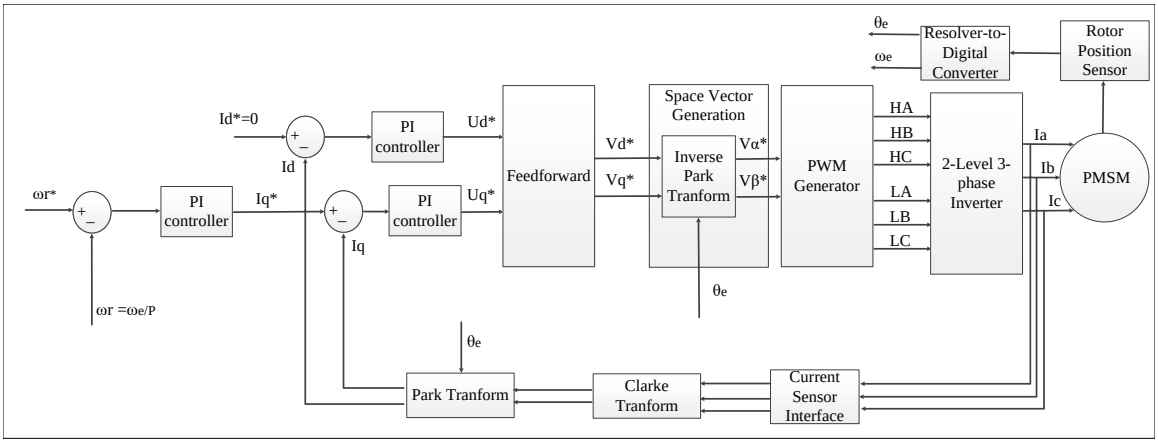


Figure 3.3: Field Oriented Control algorithm for PMSM drive.

Furthermore, to appropriately control the torque and speed of a PMSM, field oriented control (FOC) is the widely used control method in industry and academia [96]. A block diagram of the FOC is shown in Fig.3.3. As can be seen, measurement of the three phase currents i_a, i_b, i_c and the rotor position θ_e is necessary to be able to transform to its equivalent dq voltages, v_d and v_q, and currents, i_q and i_d. FOC algorithm is used to provide the command voltages v_d and v_q to generate the necessary stator currents i_q and i_d of the PMSM as shown in (3.3) where R_s is the stator winding resistance of the PMSM, L_s is the stator winding inductance of the PMSM, ψ_{pm} is the permanent rotor flux of the PMSM and ω_e is the rotor electrical speed. By measuring the three phase currents and controlling i_q and i_d, the speed and the torque of the motor can be controlled. The torque and the speed of the PMSM as a function of its dq currents and voltages is shown in (3.4) where P is the number of pole pairs of the PMSM, L_d and L_q are the PMSM equivalent dq inductances,

and τ_e is the electromagnetic torque produced by the PMSM. The controller used in the FOC algorithm consists of a cascaded proportional-integral (PI) controller with anti-windup architecture with an outer speed loop and an inner speed loop. To ensure stability, the inner current loop of the cascaded PI architecture is set to ten times the bandwidth of the outer speed loop.

$$\begin{aligned} v_d &= R_s i_d + L_s \frac{di_d}{dt} - \omega_e L_s i_q \\ v_q &= R_s i_q + L_s \frac{di_q}{dt} + \omega_e L_s i_d + \psi_{pm} \omega_e \\ \omega_e &= \frac{d\theta_e}{dt} \end{aligned} \tag{3.3}$$

$$\tau_e = \frac{3}{2} P(\psi_{pm} i_q + (L_d - L_q) i_d i_q) \tag{3.4}$$

To ensure that the demanded torque and speed of the PMSM can be attained, a specific DC link voltage and current is necessary. The minimum battery voltage for a commanded v_d and v_q is shown in V_{bat}. As a rule of thumb, it is necessary to saturate the voltages v_d and v_q in the FOC algorithm to ensure there is sufficient DC link voltage for control. Furthermore, the demanded current from the DC link capacitor is shown as I_{inv}. As long as the DC link voltage and current demands are in normal operating range and saturated with (3.5), the torque and speed of the PMSM can be controlled.

$$\begin{aligned} I_{inv} &= i_s = \sqrt{i_d^2 + i_q^2} \\ \frac{V_{bat}}{\sqrt{3}} &> v_s = \sqrt{v_{dsat}^2 + v_{qsat}^2} \\ v_d &<= v_{dsat} \\ v_q &<= v_{qsat} \end{aligned} \tag{3.5}$$

Table 3.1: Simulation environment for the EPU fault analysis.

Parameter	Value	Unit
DC Link Capacitor (C_{DC})	450	μF
DC Link voltage (V_{DC})	800	V
Nominal current (I_s)	166.5	Arms
Nominal torque (T_e)	166.3	Nm
Rated speed (ω_r)	5000	RPM
PM flux linkage (ψ_m)	0.0582	Wb
Inductance (L_d, L_q)	150	μH
Stator resistance (R_s)	0.0154	Ω
Number of pole pairs (P)	8	-
Inverter switching frequency (f_s)	10	kHz
Number of turns per coil	11	-
Number of coils per phase	6	-
Saturation current (I_d, I_q)	400	A
Saturation voltage (U_d*, U_q*)	461	V
Motor Inertia (J_m)	1.41	kgm^2

Simulation results are demonstrated through a MATLAB/Simulink model. The simulation starts in steady state with the parameters mentioned in Table 3.1. At the first second, the fault (other than the healthy operation) is asserted in the model to see its affect. Then, at two seconds, a step load of 20Nm is applied to emulate some sort of turbulence due to the wind to see how a load disturbance would affect the behavior of the EPU under faulty conditions. The results for healthy operation of

the EPU is shown in Fig.3.4. The PI controllers were tuned such that when a step load occurs, there is a change of 1.5RPM on the electrical speed of the motor with minimal current overshoot and undershoot. Furthermore, a torque ripple of 14.84% is found on the torque produced by the motor. The simulation simulates the EPU working in cruise mode with a constant speed and torque while at two seconds, a type of turbulence cause a load disturbance while cruising. To make each simulation fault scenario stable, it is assumed that the source battery has enough SOC and can provide enough current to supply the DC link.

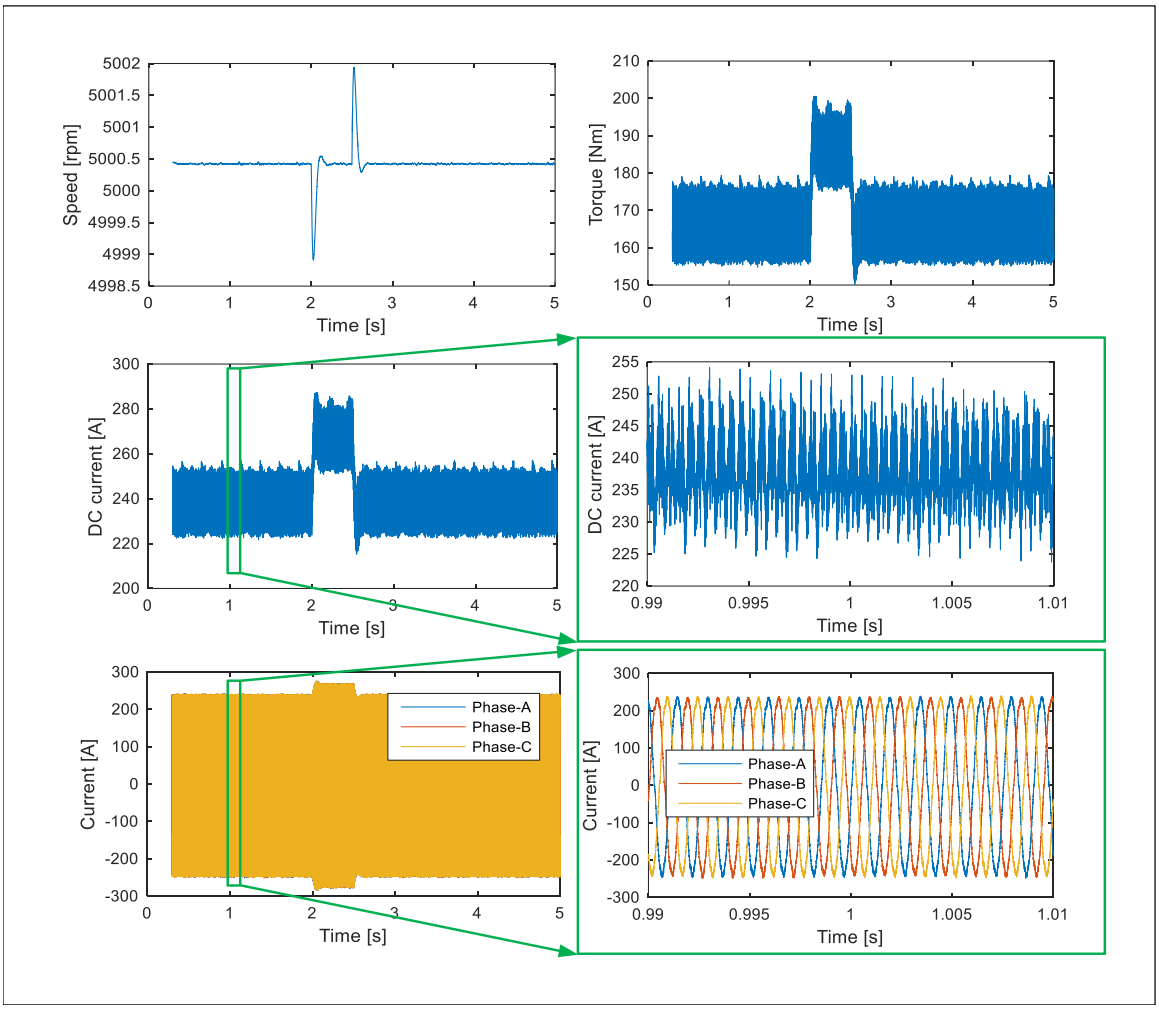


Figure 3.4: Healthy operation of PMSM with FOC control.

Now that the healthy operation is understood for the EVTOL EPU, a common modeling method is used for understanding the critical electrical faults. By knowing the inverter pre-fault output voltages V_1, V_2, V_3, PMSM pre-fault phase voltages v_a, v_b, v_c, and neutral point voltage V_N in (3.2), the faulty EPU models (where applicable) are derived in this from (3.6) where v'_a, v'_b, v'_c and V'_N are the post-fault phase voltages, and post-fault neutral point voltage respectively. V'_1, V'_2 and V'_3 are the post-fault

inverter voltages. The derivation of a mathematical model for a post-fault PMSM is the core to understanding its behavior.

$$V_1' = v_a' + V_N', V_2' = v_b' + V_N', V_3' = v_c' + V_N' \tag{3.6}$$

3.2 Open Circuit Faults

Open circuit faults are an important fault to consider. They can be caused due to disconnection of a component or break in the harness due to pinching of wire. Mechanical vibrations could cause a connector to disconnect from a component thus creating an open circuit fault. Without appropriate detection strategies, the open circuit faults will cause instability in the control of the speed and torque of the EPU. Furthermore, they will cause unwanted oscillations in the EPU currents and voltages [97]. They tend to have fault tolerant control algorithms that enable enough time for the EVTOL to land [30]. Although they may be controllable, their post-fault behavior is necessary such that an appropriate fault mitigation strategy can be implemented. In this section, the open circuit faults that can occur in the EPU are discussed.

3.2.1 Motor Open Phase Fault

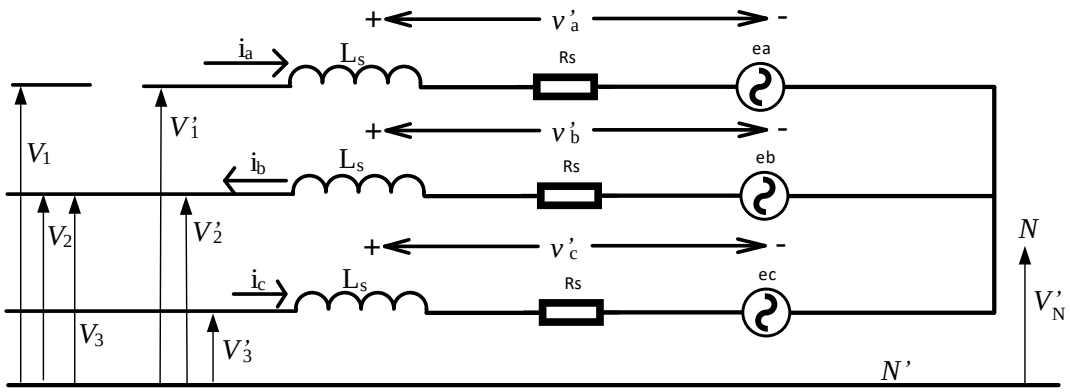


Figure 3.5: PMSM equivalent electrical circuit under OPF.

$$\begin{aligned} V_1' &= e_a + V_N' \\ V_2' &= V_2 = V_b' + V_N' \\ V_3' &= V_3 = V_c' + V_N' \end{aligned} \tag{3.7}$$

The first type of open circuit fault that can occur in the inverter consists of the PMSM open phase fault (OPF). The PMSM OPF is mathematically derived in this section and its equivalent electrical circuit is shown in Fig.3.5. Under OPF, the PMSM has the same current relationships shown in (3.1) due to its isolated neutral point. From Fig.3.5 and (3.7), it can be seen that the only voltage which is different from its healthy counterpart is V_1. The one term that is not known in the faulty behavior in (3.7) is V_N'. By adding all three voltages in (3.7) and knowing that the windings are balanced, the value of V_N' is obtained as shown in (3.8).

$$V_N' = \frac{1}{2}(V_2 + V_3 + e_a) \tag{3.8}$$

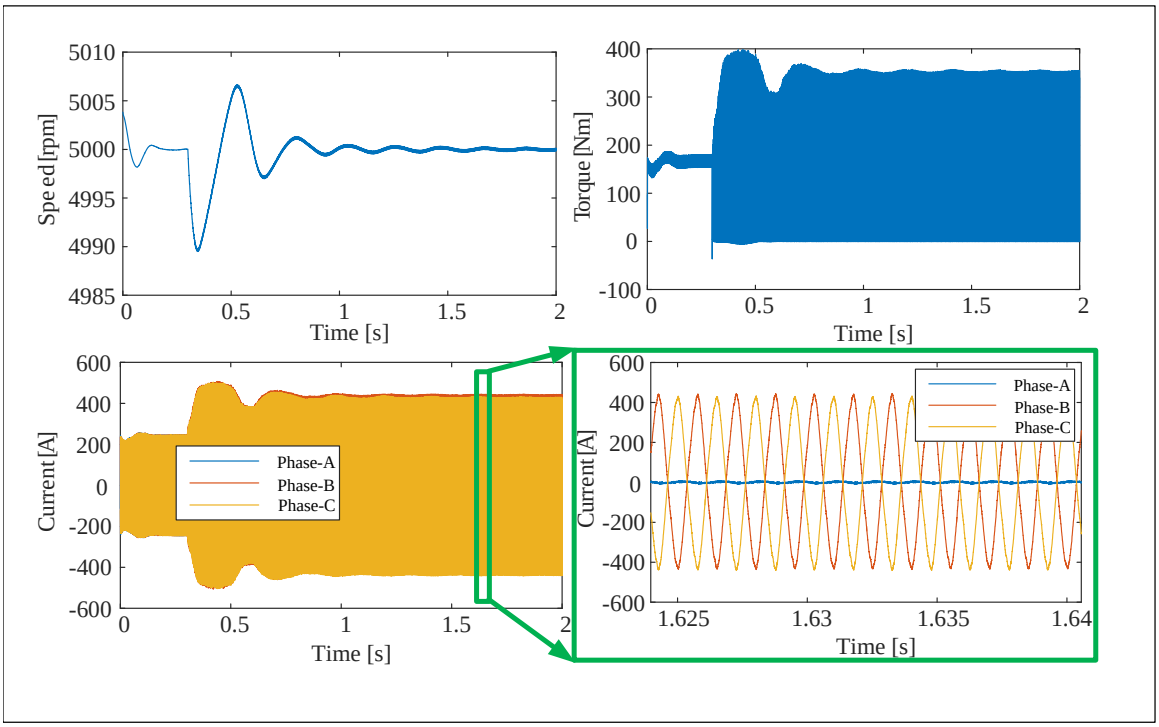


Figure 3.6: Open Phase fault simulation results.

Once the fault occurs, the behavior of the controlled torque and speed of the PMSM becomes quite different. Fig.3.6 shows the effects of the fault on the three phase currents, torque and speed of the PMSM. The simulation starts in steady state at a speed of 5000RPM and at time 0.3s, the fault is triggered by opening phase A in the Simulink model. As can be seen in the simulation results, the PI controller can recuperate the desired speed of the propeller but the torque ripple is much larger then in the healthy case. Furthermore, $i_a = 0$ which means that the rest of the energy must be distributed between phase B and C which is seen in the increase in current amplitude of 400A peak. Both phase B and C are 180 degrees out of phase from each other due to the isolated neutral point. The torque ripple will cause vibrations on the aircraft chassis which would not be ideal for passengers if the flight is continued.

3.2.2 Power Device Fail Open

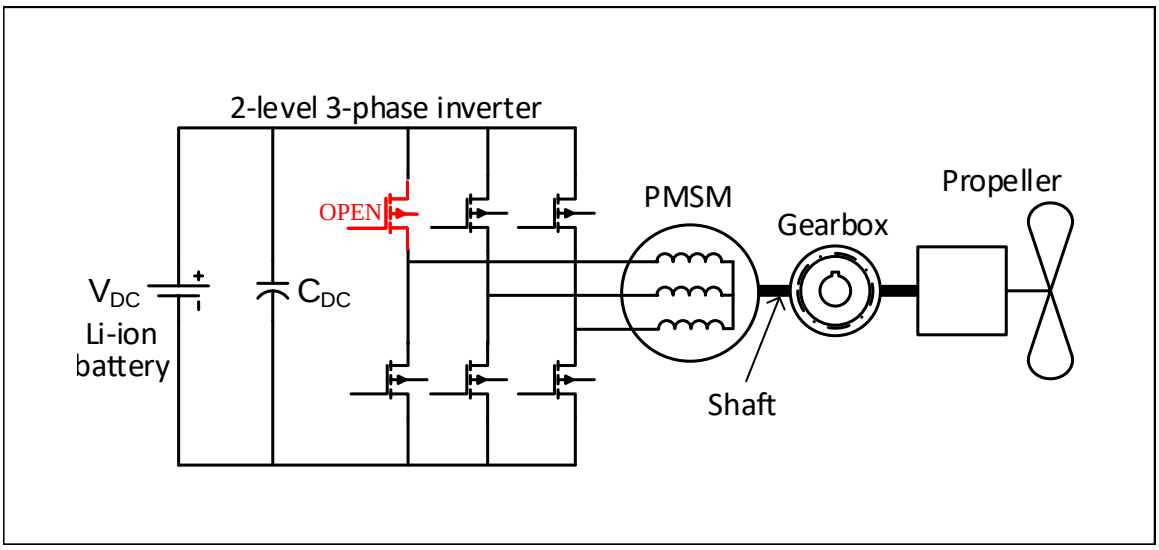


Figure 3.7: EPU under power device fail open.

The second type of open circuit fault that can occur in the inverter consists of having a malfunctioning power device that is left in the open state. This would cause half of one of the inverter leg to become permanently open thus creating an open circuit to the PMSM as shown in Fig.3.7. As will be shown, only half of the waveform for the faulty leg will be driven (positive current only if bottom is faulty and only negative current if top is faulty) which would cause a reduce in average torque production.

The behavior of the failed open power device on the motor control is a bit different to that of the OPF mentioned previously. The motor drive controller would try to maintain the appropriate speed by controlling the currents but with only five power devices instead of six. The simulation results of such a behavior are shown in Fig.3.8.

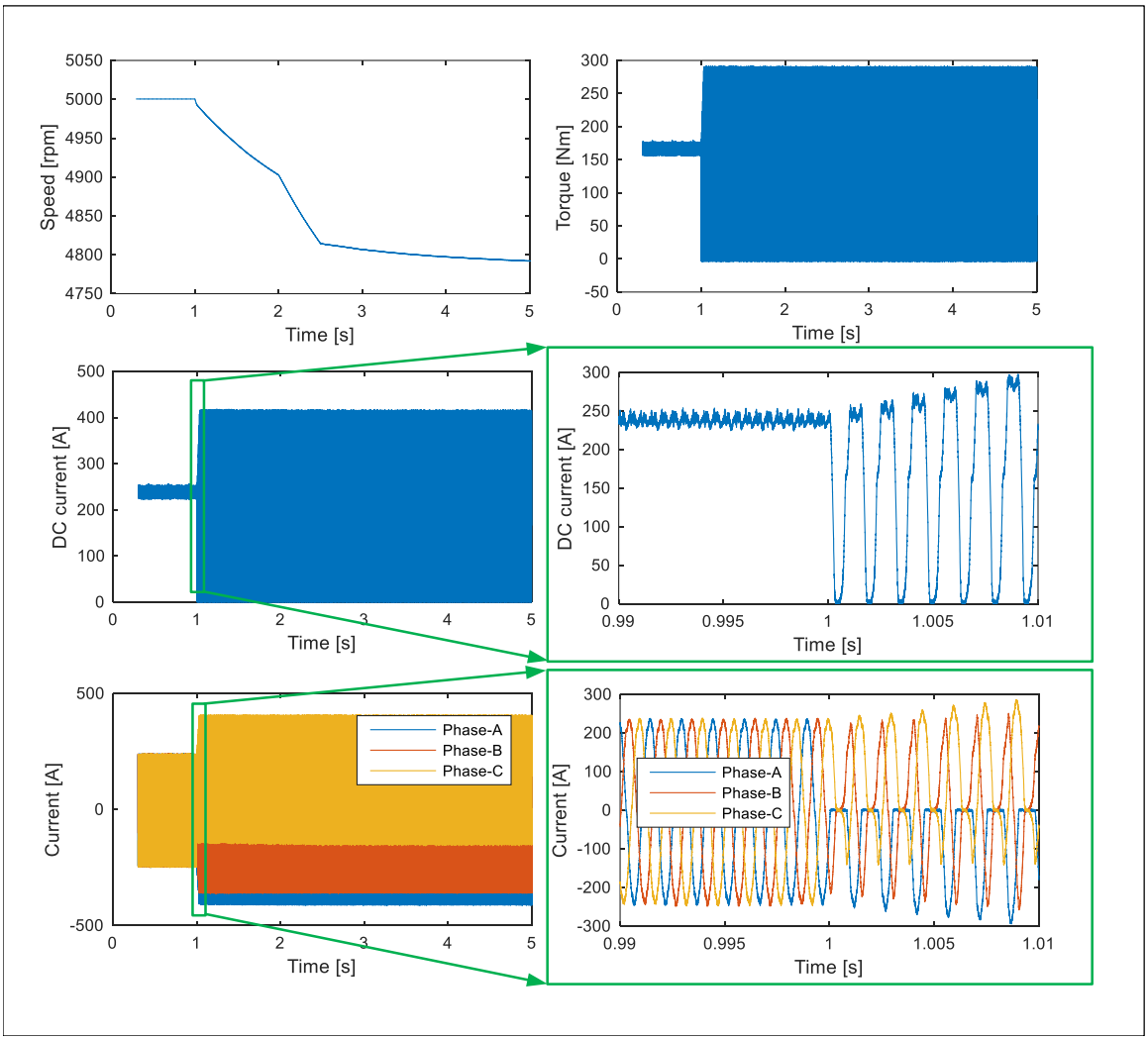


Figure 3.8: EPU under power device fail open simulation results.

As can be seen, the speed controller tries to keep the speed of the motor at the set speed but due to the loss of the top phase a switch, only negative current flows through that open switch through the body diode and thus, the produced torque now has large oscillations and the average torque of 151.8Nm instead of 166.1Nm. Furthermore, the DC link current now produces large $\frac{di}{dt}$ of close to 400A which is the saturation current of the current PI controller. Also during the load disturbance,

it can be seen that the speed drops even more which could be detrimental if many events of disturbance occurs. A safe landing would be extremely tough to do in such scenario.

3.3 Short Circuit Faults

The short circuit fault is typically a destructive fault as it can cause fires due to the over current over heating harnesses and circuit board traces. The short circuit current can also cause an overheating of the battery which could lead to a catastrophic failure of the main power source. Thus, it is crucial to understand how a short circuit fault can occur and protection against this type of fault is crucial to the safe operation of the EVTOL EPU. Some short circuit faults are caused by degradation of component parameters and some can occur due to mechanical stresses. Furthermore, like open circuit faults, a wire could be pinched by something and thus causing two wires shorting together or to cause the wire to touch a metallic surface like the chassis of the EVTOL. In this section, short circuit faults on the EVTOL EPU are discussed.

3.3.1 Phase-to-Phase Fault

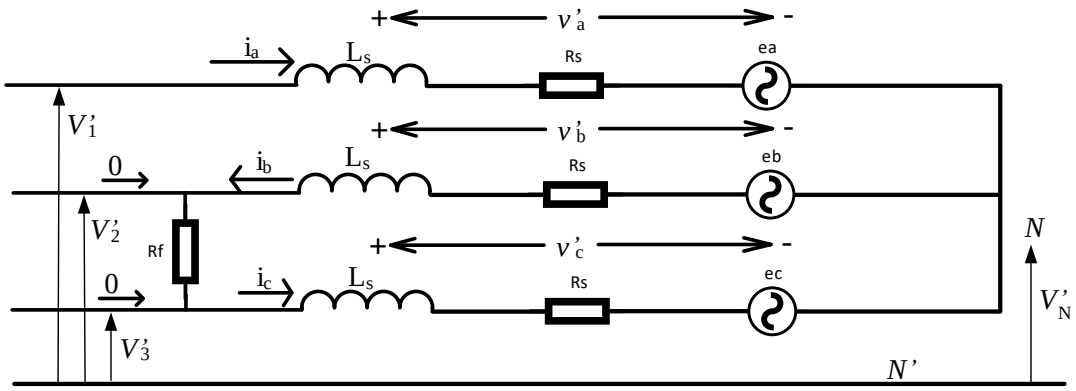


Figure 3.9: PMSM equivalent electrical circuit under P2PSCF.

The start of the derivation of the phase to phase short circuit fault (P2PSCF) assumes the following two cases:

- Case 1: The inverter is disconnected once the fault is detected leaving all switches open in the inverter.
- Case 2: The inverter bottom switches are turned on while the top switches of the inverter remain open.

The model assumes a short circuit resistance, depicted by R_f, between phases b and c as shown in the equivalent circuit of the P2PSCF in Fig.3.9 for both of the above cases. Knowing that the PMSM's neutral point is isolated, relations in (3.1) can be used where i_a, i_b, and i_c are phase currents of the PMSM. The condition of $i_a = 0$ occurs as the inverter is disconnected. Thus, phases b and c have the same current magnitude but in opposite directions.

Hence for the first case, the v'_a can be expressed as in (3.9) where e_a is the electromotive force of the phase a winding. The resistance R_f is chosen to make i_a zero within a reasonable time. In other words, R_f controls the time constant of the phase a winding to accurately model the transients behavior of the i_a due to the fault. By using (3.6), (3.1), and the expression for v'_a in (3.9), the v'_b and v'_c can be obtained as in (3.9).

$$\begin{aligned} v'_a &= e_a \\ v'_b &= \frac{1}{2}[-R_f i_b - e_a] \\ v'_c &= \frac{1}{2}[R_f i_b - e_a] \end{aligned} \tag{3.9}$$

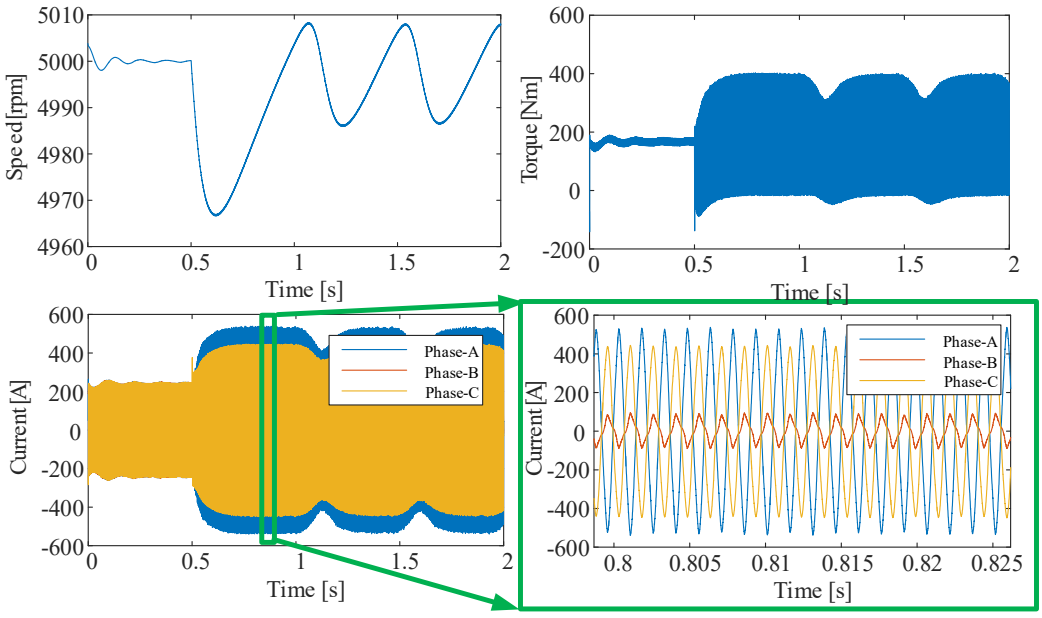


Figure 3.10: Phase to Phase short circuit fault simulation results.

For the second case, since a neutral point is created using the inverter bottom switches, this makes the following true $v'_a = v'_b = v'_c$. Since there is an isolated neutral point, the only solution left is (3.10). Thus, the phase voltages of the PMSM are known with (3.6) and (3.10).

$$v'_a = v'_b = v'_c = 0 \tag{3.10}$$

Fig.3.10 shows the results of having a P2PSCF on phase A of the EPU. As can be seen, the speed can be controlled about an operating point with large oscillations which can cause instability on the flight controls. The torque supplied by the rotor also oscillates and could cause further damage to the aircraft in the case of mechanical vibrations. The P2PSCF generates large currents in the motor windings. These large currents are shown in Fig.3.10 along with the rotor speed and torque. It can be seen that once the P2PSCF occurs at 0.5 seconds between phase b and c, a large torque ripple occurs on the rotor along with an increase on all phase currents. The copper losses have increased with P2PSCF up 161.72% while the torque ripples have also increased to 232.13% compared to pre-fault operation.

Furthermore, due to the P2PSCF, the phase currents are no longer the same so the power devices do not see the same currents anymore and age differently which could result in one power device failing earlier than the others.

3.3.2 PMSM Inter-turn Short Circuit Fault

One of the most common ways a PMSM could fail is the inter-turn short circuit fault (ITSCF) [75,98]. An ITSCF occurs when the insulation between turns in a stator coil fails and thus two or more turns in a stator coil create a short circuit together [98].

ITSCF could be detrimental to the PMSM and the EVTOL EPU. There is a large increase in the power loss and torque ripple of the PMSM whenever an ITSCF is present in the machine, which could further damage the machine and cause the entire EPU to be in a catastrophic state. Thus a thorough understanding of the fault both quantitatively and qualitatively is needed to ensure safety on the EVTOL EPU. In this section, a mathematical model of PMSM during ITSCF is presented, and the model is implemented in MATLAB/Simulink environment.

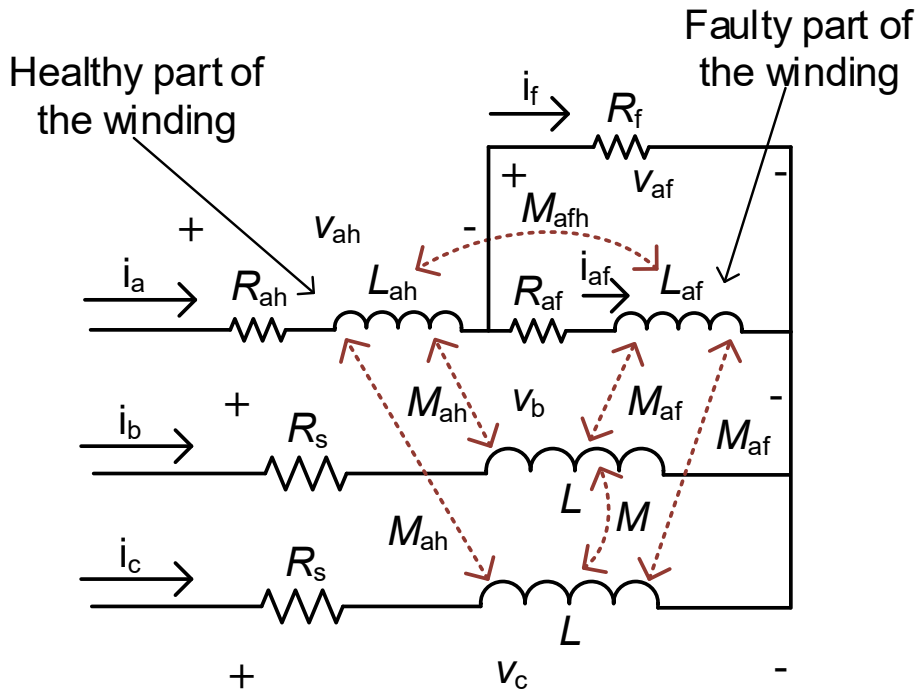


Figure 3.11: Equivalent electrical circuit of PMSM phase A under inter turn short fault.

The ITSCF occurs in the same phase within a stator tooth between coils due to stator winding insulation failure [75, 98]. The insulation can fail due to high overvoltage transients, high temperature and harsh environments [13]. Once the insulation fails, the adjacent turns in a coil are no longer isolated from each other and thus create an extra electrical branch which is parallel to the faulty turns in the coil. The ITSCF can occur between just two turns or as many turns as the coil has. An equivalent circuit of a PMSM under ITSCF on Phase A is shown in Fig.3.11. The ITSCF equivalent electrical circuit model consists of an extra electrical branch in the faulty phase coil, with very low resistance, R_f, where current can circulate with a very high amplitude.

The faulty winding can be divided into two sections, a healthy part, and a faulty part. The R_{ah}, L_{ah}, R_{af}, and L_{af} in Fig.3.11 are phase resistance and self-inductance of the healthy part and the faulty part of the winding, respectively. The M_{afh} is the mutual inductance between the healthy part and the faulty part of the phase-A winding. The M_{ah} and M_{af} are the mutual inductances between the healthy part and other phases and the faulty part and other phases, respectively. The L and M in Fig.3.11 are the self and mutual inductances of the remaining healthy phases, respectively. Equations (3.11-3.19) have been derived from Fig.3.11 depicting the equivalent electrical circuit of the PMSM under ITSCF for phase A. The dq axis flux linkage vector, λ_{dqf}, is defined as (3.11)

$$\lambda_{dqf} = L_{dqf} I_{dqf} + \lambda_{mf} \tag{3.11}$$

where I_{dqf} and L_{dqf} are d- and q-axis current vector, and inductance matrix, respectively. The vector, λ_{mf}, is defined as in (3.12)

$$\lambda_{mf} = \begin{bmatrix} \lambda_{pm} \\ 0 \\ \mu\lambda_{pm} \end{bmatrix} \tag{3.12}$$

where λ_{pm}, μ are permanent magnet flux linkage and the percentage of the faulty winding, respectively. The dq axis voltages can be written as in (3.12)

$$V_{dqf} = R_{dqf}I_{dqf} + X_{dqf}I_{dqf} + L_{dqf}I^{|}_{dqf} + E_{dqf} \tag{3.13}$$

where V_{dqf} and E_{dqf} are d- and q-axis voltage and induced voltage vectors, respectively. The R_{dqf} and in (3.13) are resistance and reactance matrices, respectively. For completeness, the equations depicting the matrices of L_{dqf}, R_{dqf}, X_{dqf} and E_{dqf} are shown in equations (3.14-3.17).

$$L_{dqf} = \begin{bmatrix} L_m & 0 & \frac{-2}{3}L_{mf}sin(\theta_e) \\ 0 & L_m & \frac{-2}{3}L_{mf}cos(\theta_e) \\ L_{mf}sin(\theta_e) & L_{mf}cos(\theta_e) & -L_{af} \end{bmatrix} \tag{3.14}$$

$$R_{dqf} = \begin{bmatrix} R_s & 0 & \frac{-2}{3}R_{af}sin(\theta_e) \\ 0 & R_s & \frac{-2}{3}R_{af}cos(\theta_e) \\ R_{af}sin(\theta_e) & R_{af}cos(\theta_e) & -(R_{af}+R_f) \end{bmatrix} \tag{3.15}$$

$$X_{dqf} = \begin{bmatrix} 0 & -\omega_e L_m & 0 \\ \omega_e L_m & 0 & 0 \\ \omega_e L_{mf}cos(\theta_e) & -\omega_e L_{mf}cos(\theta_e) & 0 \end{bmatrix} \tag{3.16}$$

$$E_{dqf} = \begin{bmatrix} 0 \\ \omega_e \lambda_{pm} \\ \mu \omega_e \lambda_{pm} cos(\theta_e) \end{bmatrix} \tag{3.17}$$

Where:

$$L_m = L - M \tag{3.18}$$

$$L_{mf} = L_{af} + M_{afh} - Maf \tag{3.19}$$

Table 3.2: Simulation results for the ITSCF MATLAB/Simulink model for pre-fault and post-fault of 5 and 11 faulty turns in a single coil.

Number of faulty turns in winding	5	11
Fault-Current (ARMS)	4590	2464
Pre-fault copper loss (kW)	1.28	1.28
Post-fault copper loss (kW)	25.64	14.6
Copper loss increase (%)	2003.1	1140.6
Pre-fault torque ripple (%)	19.3	19.3
Post-fault torque ripple (%)	184.22	187.89

Using the specifications mentioned in Table 3.1, the PMSM under ITSCF was analysed for pre-fault and post-fault behavior for 5 and 11 turns. As can be seen in Table 3.2, as the faulty turns are increased, the current amplitude in the faulty winding is reduced while the torque ripple is over 100% in all cases due to the imbalance

among the 3-phases. This is due to the fact that the reactance of the faulty part of the winding increases with the number of faulty turns in a winding. The transient results for the 5 and 11 faulty winding of a PMSM under ITSCF is shown in Fig.3.12 and Fig.3.13 respectively. Simulating with just having two faulty adjacent turns is difficult due to the inductance of the faulty part becomes very small. A very small inductance causes very small $\frac{L}{R}$ time constant in the model. So a time step around 0.1ns is needed due to this very small time constant. As shown in the simulation results, the severity of the ITSCF is dependent on the number of windings that are shorted together.

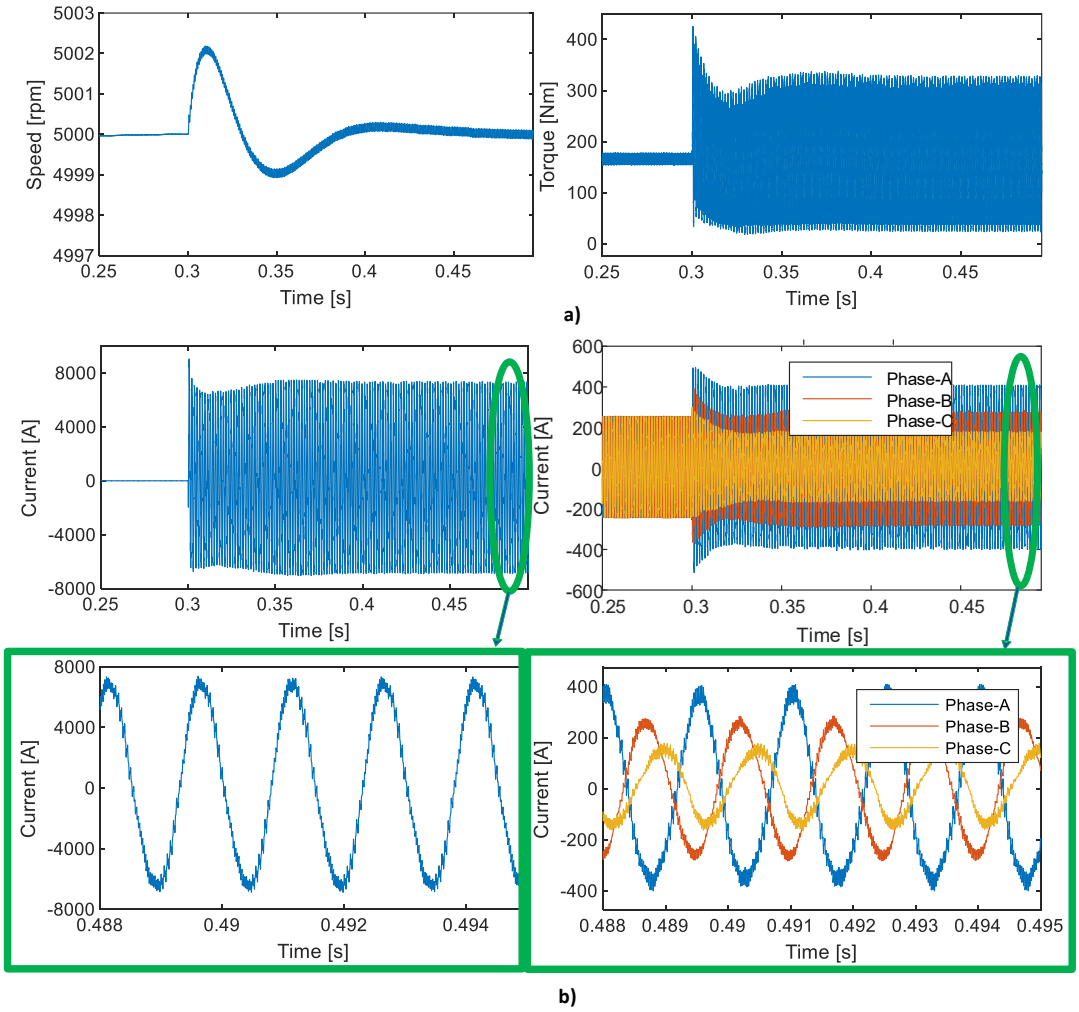


Figure 3.12: Simulation results for the PMSM under ITSCF with 5 faulty turns in a winding: a) Mechanical behavior of the PMSM under ITSCF b) Electrical behaviour of the PMSM under ITSCF.

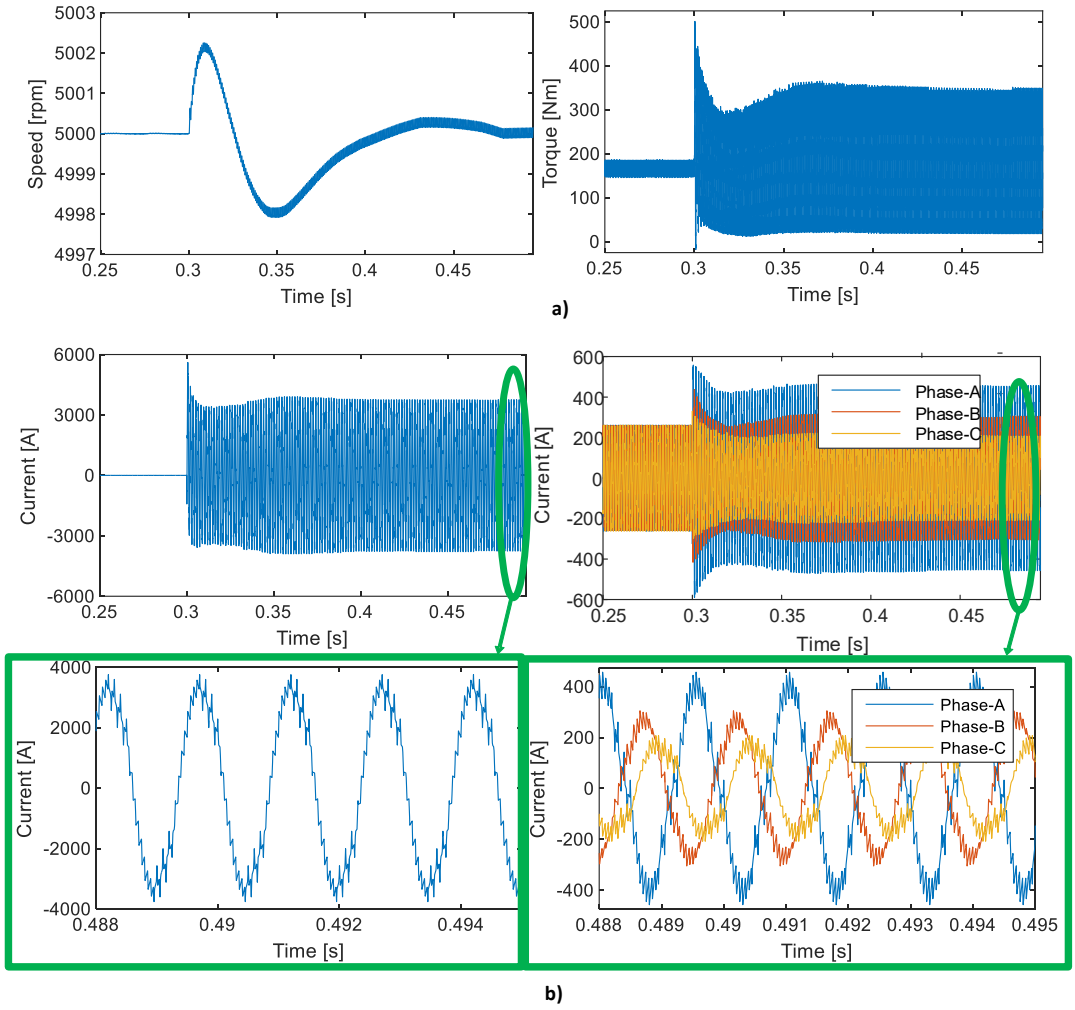


Figure 3.13: Simulation results for the PMSM under ITSCF with 11 faulty turns in a winding: a) Mechanical behavior of the PMSM under ITSCF b) Electrical behaviour of the PMSM under ITSCF.

3.3.3 Power Device Fail Short

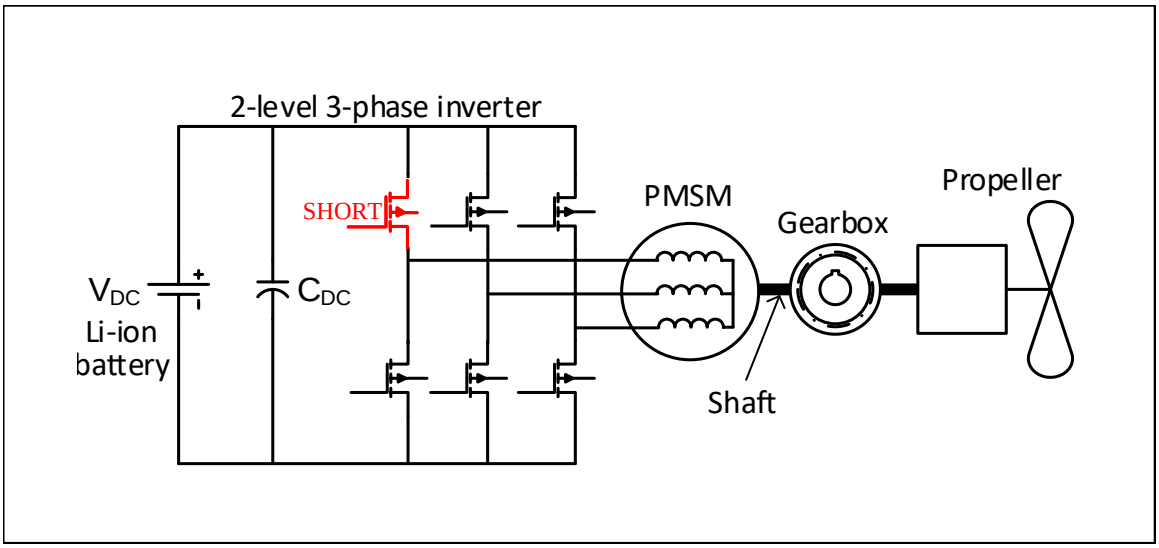


Figure 3.14: EPU under power device fail short.

This case occurs if the power device itself fails shorted or its antibody diode is failed short as shown in Fig.3.14. In both cases, a short circuit occurs on one switch and thus the controller cannot control appropriately the current due to having shoot through short circuits every time its respective counter part switch is turned on.

The effects of a shorted MOSFET can be seen in Fig.3.15 where the top switch of phase A is shorted and thus always on. The current does not travel into the three phases as they should and thus causes large oscillations on the output torque of the motor as well as the motor speed slowly decreasing. This could be detrimental to the flight of the EVTOL due to the mechanical vibrations that would persist from the fault. The effects of this fault on the phase A current seems to be opposite to the open phase since mainly positive current flows through the switch due to the shorted condition. Something that is not shown in the figure is that whenever a shoot through

occurs, the DC link voltage of the inverter would drastically drop and thus a large shoot through current occurs in the leg of the inverter. This could be detrimental to the battery as it would cause large $\frac{di}{dt}$ values that can wear the battery life or even worse cause a thermal runaway of the battery.

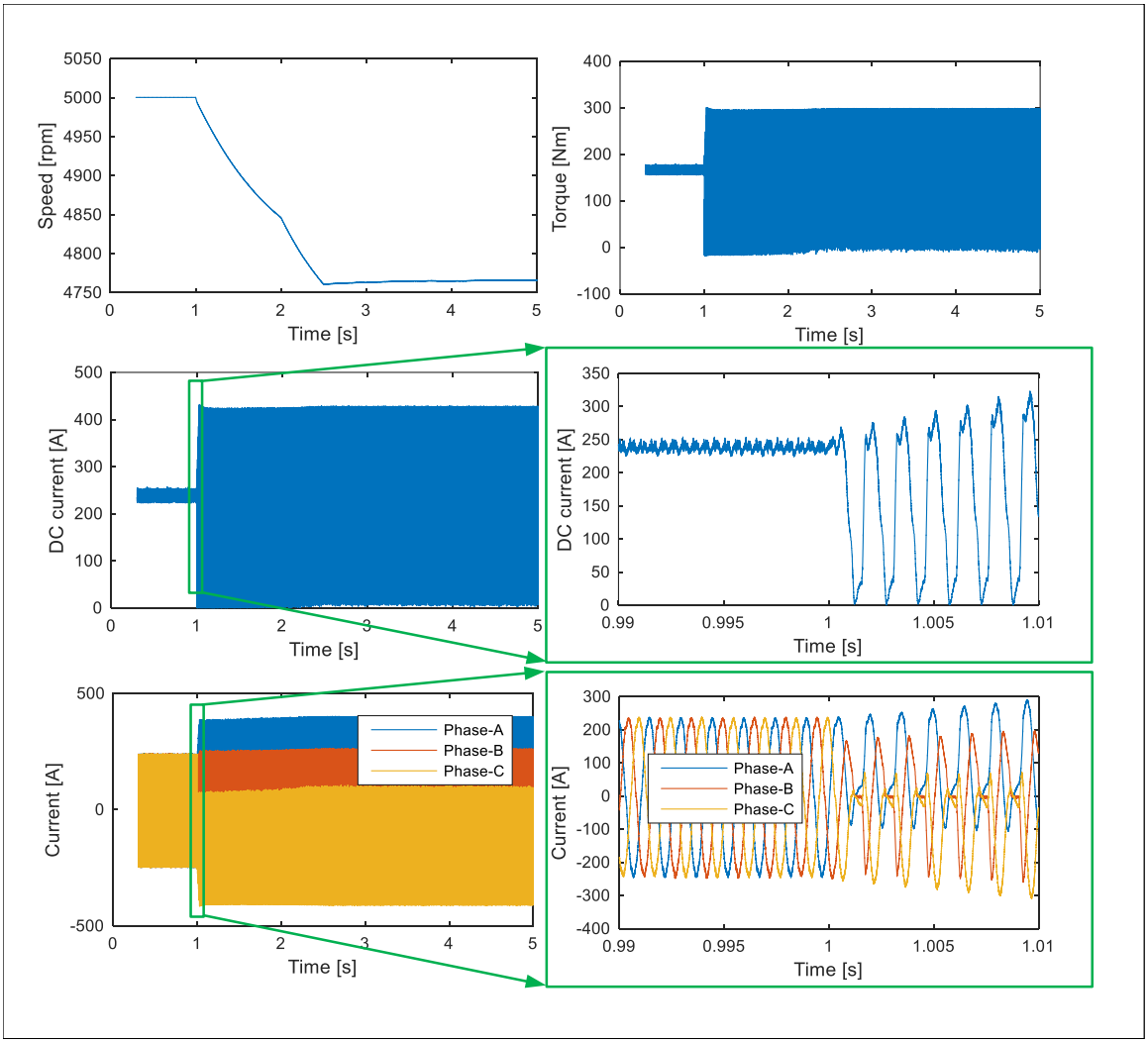


Figure 3.15: EPU under power device fail short simulation results.

3.3.4 Inverter power stage short circuit

This failure could be due to having two power devices shorted or turned on at the same time in one leg of the inverter thus causing a shoot through current and depleting the capacitor voltage. This fault would be destructive in the control of the EPU as it would cause a large voltage drop at the DC link due to the large current demand. The short circuit current would depend on the short capacity of the battery and the $\frac{L}{R}$ time constant of the cable, SSPC and inverter system.

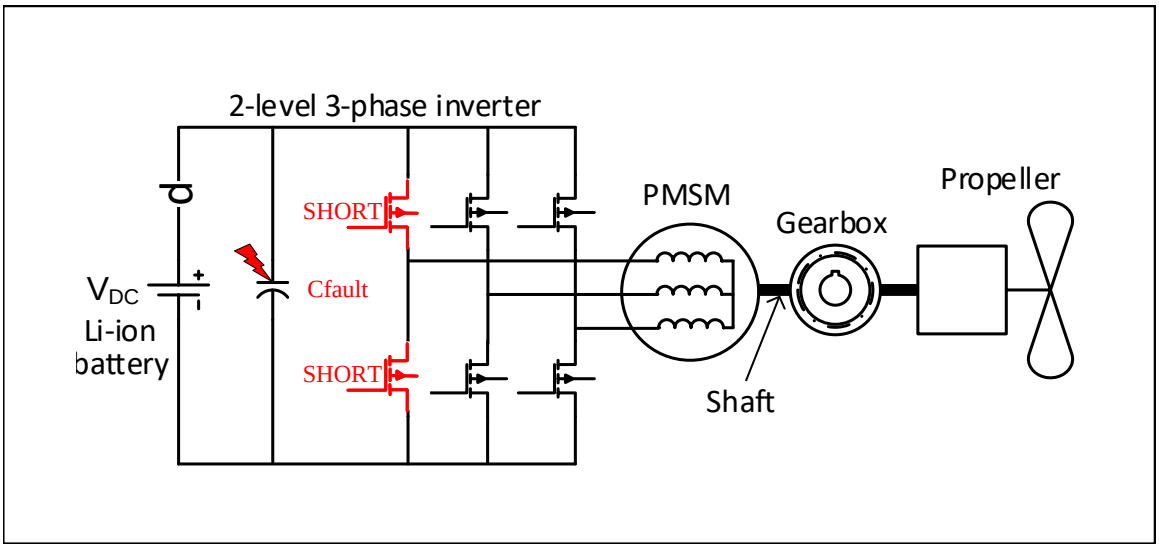


Figure 3.16: EPU under inverter short circuit failure caused by capacitor degradation or shorted leg.

This failure could also occur if the DC link capacitor degrades or for some reason the two legs of the inverter is damaged, thus driving of the motor is not possible [99]. Since the impedance of the capacitor is directly related to its capacitance, C, frequency, ω and its equivalent series resistance, R_{ESR}, as shown in (3.20) that the short circuit current through the capacitor would be dictated by its R_{ESR} [100].

$$Z_C = \frac{1}{j\omega C} + R_{ESR} \tag{3.20}$$

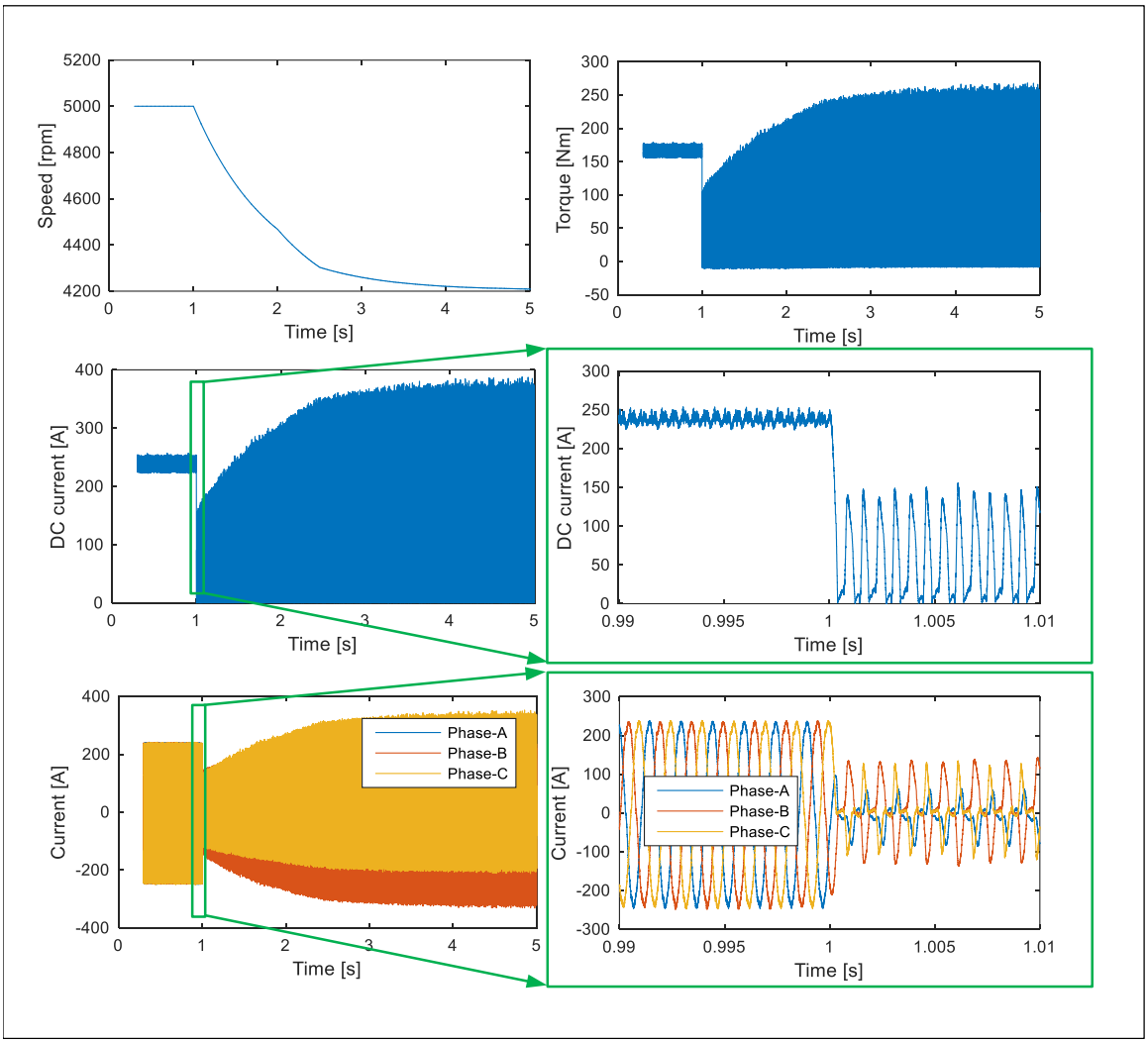


Figure 3.17: EPU under power device fail short simulation results.

The resultant post-fault behavior is shown in Fig.3.17 assuming that the source can supply the necessary energy. As can be seen, the PI controller tries to maintain the average demanded torque but is limited by the amount of voltage and energy that

the DC link capacitor can supply. If the energy can be supplied, the battery would have to provide its short circuit current which would deplete the battery very fast and a thermal runaway could occur on the battery if the short circuit is not detected in time.

Furthermore, the large oscillations on the DC link current could be seen by the battery and thus cause further damage to the battery. The speed controller saturates to the maximum current of 400A after a certain while and thus cannot provide more energy to the motor such that the speed of 5000RPM can be attained. This could be detrimental as a safe landing could not be performed.

3.4 Control Stage Faults

Other than the power stage and the PMSM failing, other faults can occur such as a control board failure. In a case of control board failure, the sensors could fail which would result in a wrong sensing signal for the control board. Furthermore, the power supply for the control board may suddenly be interrupted or auxiliary power supplies on the control board may stop functioning for some reason. In this section, failures consisting of the control board for the motor drive are discussed.

3.4.1 Sensor Failure

One of the most important part of the control board and the motor drive algorithm is to sense the necessary signals and then feed them back into the control board to ensure proper control of the EPU. The EPU has four types of main sensors which aid in the safe control of the EPU being:

- Motor rotor position sensor
- Three phase current sensors
- DC link voltage sensor
- Temperature sensors for power devices and PMSM

Typically, a resolver is used as a rotor position sensor (RPS). For aerospace application, high robustness is needed for all feedback sensors especially if only one sensor is available. The feedback of the resolver consists of having a sinusoidal and cosine signal which are then processed to obtain the absolute position of the PMSM [101]. The signals are then fed into a demodulation algorithm to obtain the position from the cosine and sine signals. The resolver can fail in many ways but the main two types of failures that can occur is in the feedback signals being distorted or the feedback signals having an offset thus causing the measured position to be wrong [102]. This can cause instability in the control and cause disturbances on the speed and torque of the motor. Furthermore, extra harmonics could occur on the DC bus which would effect other components on that DC bus.

A typical RPS consists of two coils separated by 90 degree mechanical angle which is then excited by either an external excitation sinusoidal signal or by eddy currents as in the Sumida RPS [103]. The feedback signals consist of having a cosine and sine waveform that is periodic to the rotor position and has a frequency equal to the electrical speed of the rotor of the PMSM as shown in Fig.3.18. By demodulating both signals, the position feedback of the PMSM can be acquired.

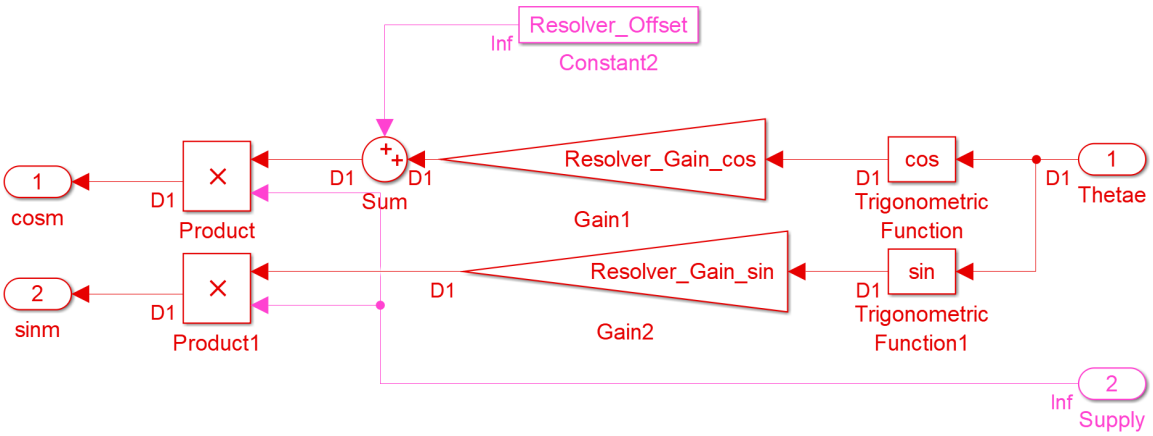


Figure 3.18: MATLAB/Simulink electrical model of resolver.

There are mainly two ways of demodulating the signal either by using dividing both sine and cosine signals and then using the four quadrant arctangent to obtain the position as shown in (3.21). This method needs the amplitude, A and B, of both the sine and cosine signals to be the same. Furthermore, the DC offset of both signals must be removed to ensure the right angle is calculated, or else it could result in a wrong angle. The phases, ϕ_{sin} and ϕ_{cos} between both signals must remain the same or else an error for the angle used for the FOC could arise which would increase losses in the PMSM and could result in uncontrollability of the EPU. This method is easy to use as long as the signal acquisition chain and the sensor itself provides a reliable signal, but that is not always the case.

$$\theta_e = arctan(\frac{A * sin(\theta_e + \phi_{sin}) + DC_{Offset(sin)}}{B * cos(\theta_e + \phi_{cos}) + DC_{Offset(cos)}}) \tag{3.21}$$

Another method of obtaining the rotor position feedback consist of using a Phase-Locked Loop (PLL) as shown in Fig.3.19. The PLL can be tuned such that it can

respond to some input error with a known bandwidth, phase margin and gain margin [104]. Ideally, the bandwidth of the PLL should include the operating rotor speeds of the EPU. Furthermore, a gain margin of above 10 and phase margin above 45°is needed to get a stable response for the chosen bandwidth.

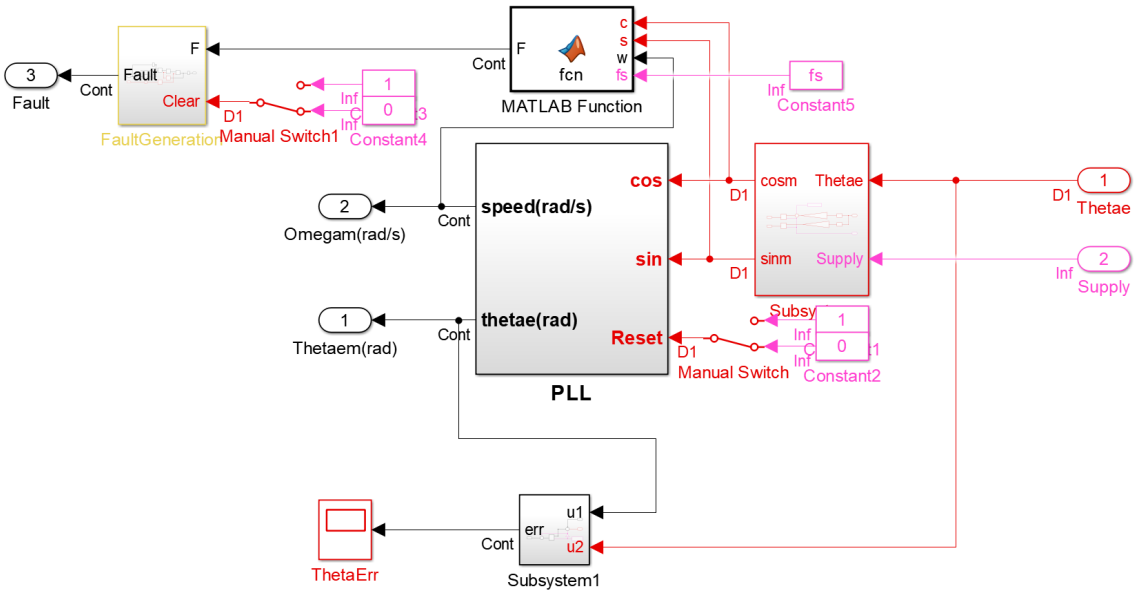


Figure 3.19: MATLAB/Simulink model of PLL used to decode the resolver signals.

By using a PLL, the faults that could occur in the RPS feedback system are analyzed. Mainly, the power following RPS faults are analyzed:

- Power supply fault: Voltage supplying the RPS or any other components used in the signal feedback other than the main controller is not existent.
- RPS offset fault: An offset is seen at $DC_{Offset(cos)}$ or $DC_{Offset(sin)}$ which skews the results.
- RPS cosine and sine imbalance: Imbalance in the sine and cosine signal amplitudes, A and B, resulting in skewed results.

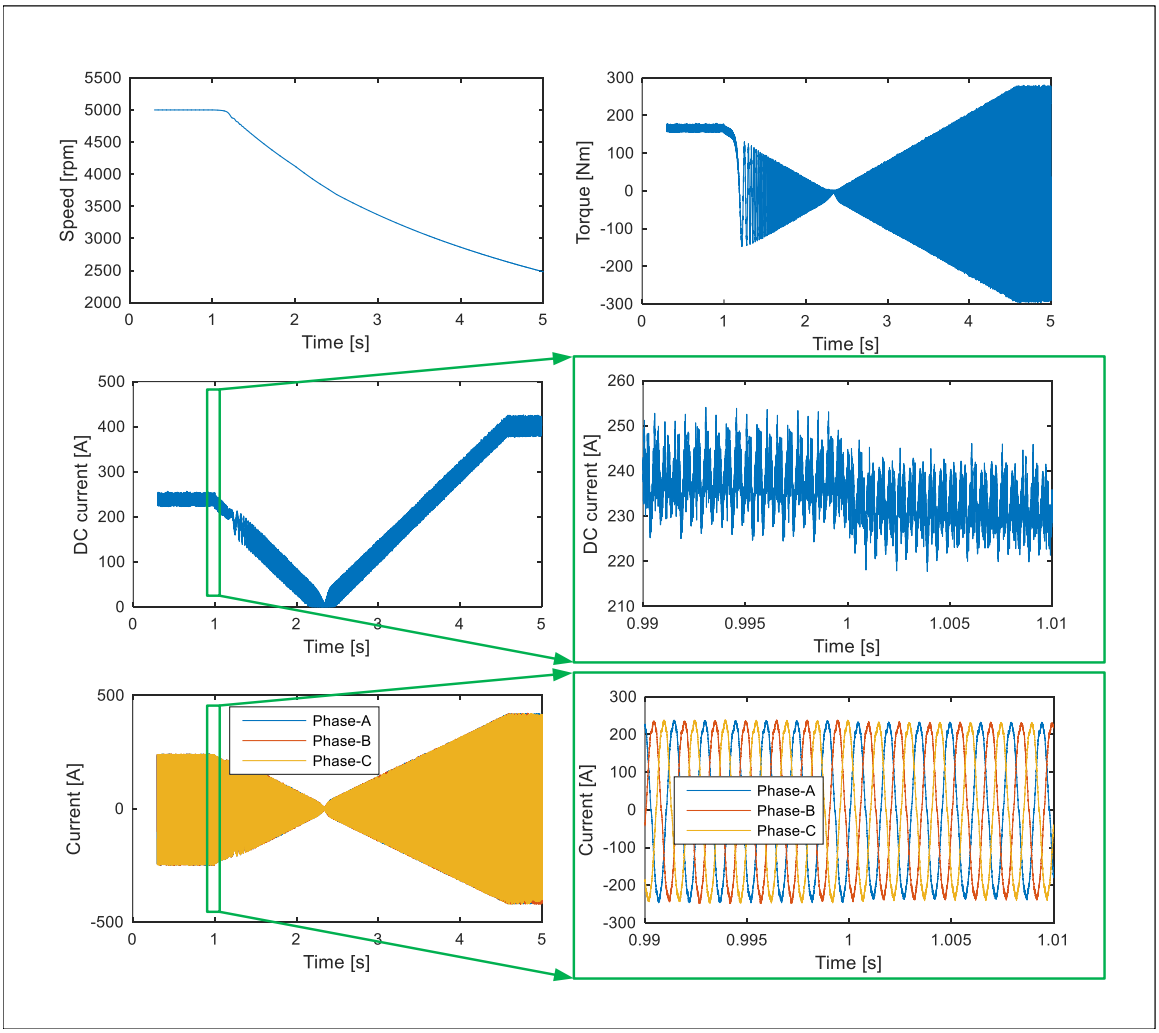


Figure 3.20: Simulation results for resolver supply failure.

Fig.3.20 shows the results of having a resolver supply failure. It can be seen that due to having no more position or speed feedback, the control algorithm becomes unstable and causing large torque oscillations and higher phase currents which makes the speed uncontrollable. As soon as the fault occurs at one second, the speed starts to drop. This is because the power supply which enables the voltages for the sine and cosine feedback signals cause these signals to be constant zero voltages. So the speed

provided by the PLL starts to drop and the position provided by the PLL starts to be out of phase and not true. As the speed drops, the speed controller tries to maintain the 5000RPM speed by increasing the current command but since the position is not correct, the current controller cannot provide the right current values which makes the needed torque oscillate and provide an average of -9.82Nm. This makes the EPU become a generator which could be detrimental as voltage from the BEMF of the motor increases and could cause overvoltage on the EVTOL EDS.

Fig.3.21 shows the results of having an offset of 50% on the cosine signal from the RPS feedback. The speed cannot be maintained but settles down to close to 4200RPM due to the wrong estimated speed and position. The controller can maintain an average torque of 105.09Nm which explains the steady state speed of 4200RPM. This could be enough for a harsh landing but other factors could be detrimental to the safe landing. It can be seen that the phase currents are skewed and do not resemble sinusoidal currents anymore. Depending on the offset level, the phase currents could be more skewed or less skewed. The DC current varies from the maximum allowable current to zero which could cause problems just like previous faults on the EVTOL EDS and battery. If the inverter is not properly thermally protected, it will overheat due to this prolonged over current conditions which would cause fire on the harnesses or the power device themselves. The torque oscillations could cause instability in the EVTOL flight which again, could inhibit a safe landing.

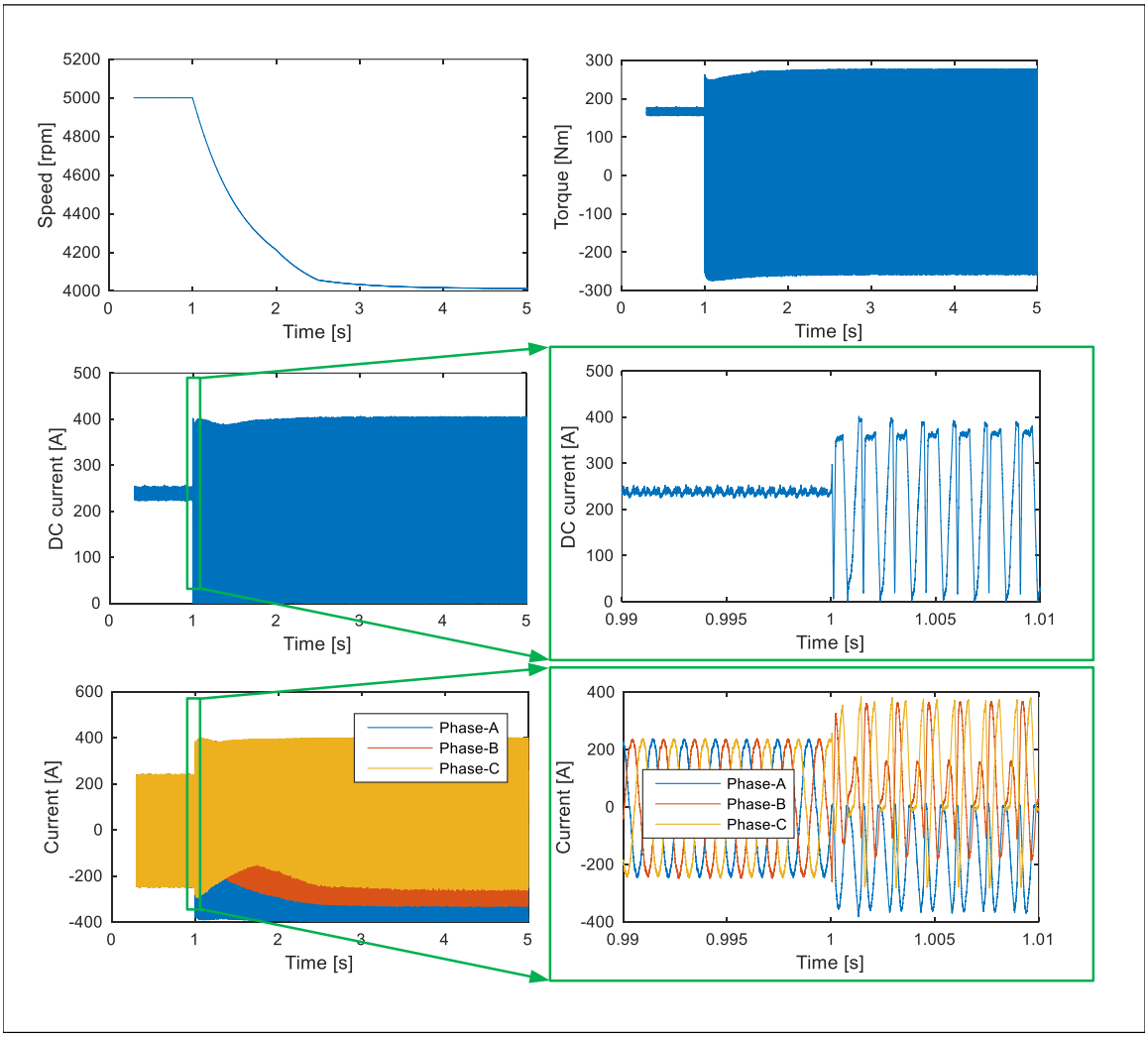


Figure 3.21: Simulation results for resolver signal offset failure. The cosine signal has 50% of the amplitude as an offset compared to the sine signal.

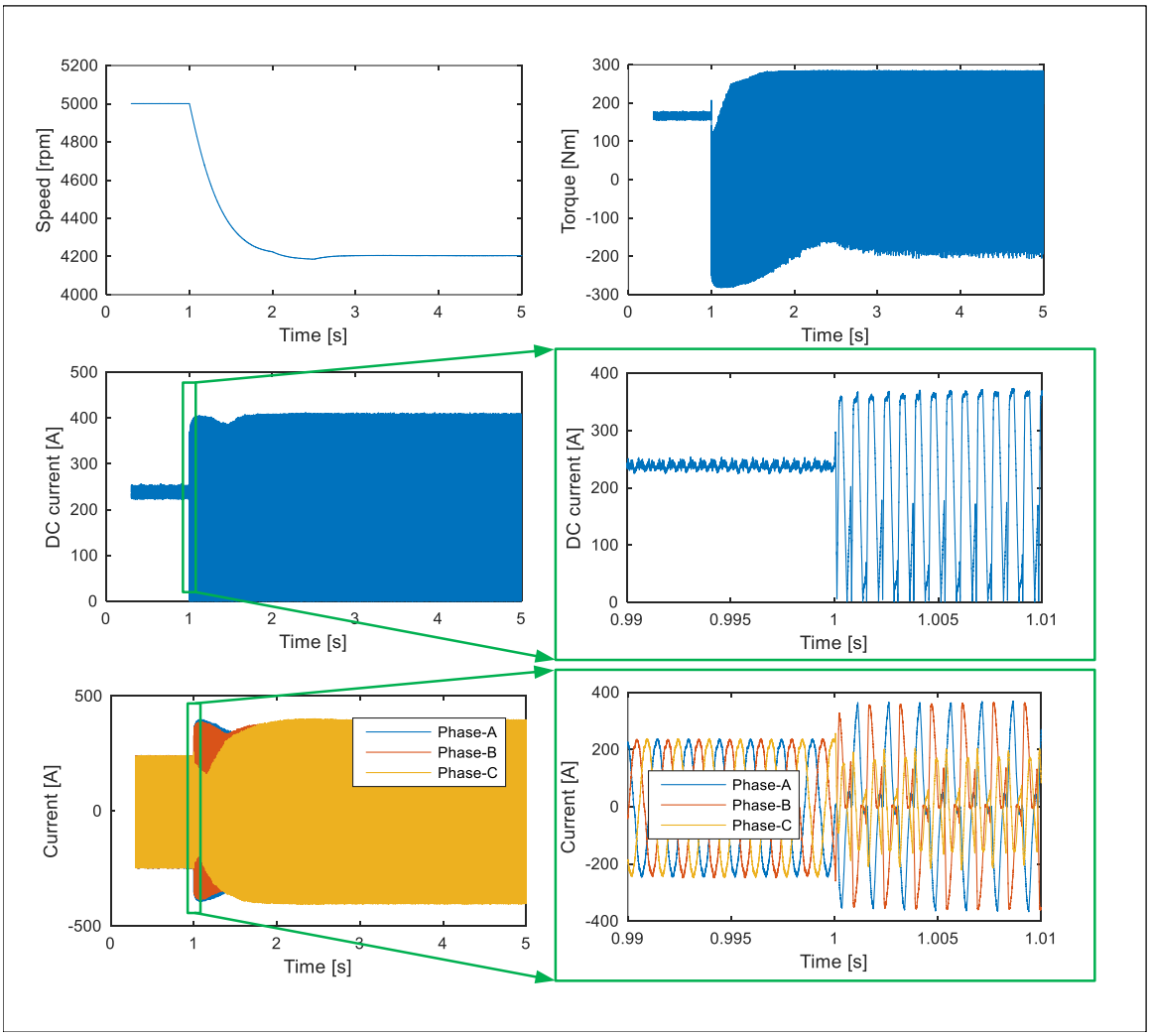


Figure 3.22: Simulation results for resolver imbalance circuit failure. The sine signal is 50% less in amplitude than the cosine feedback signal.

Finally, in Fig,3.22, the imbalance in amplitudes is shown with very similar effects as the offset fault. In this simulation, the sinusoidal signal is imbalanced by 50% compared to the cosine signal. The speed drops to a steady value of 4200RPM but the same effects of large $\frac{di}{dt}$ are found on the torque and the DC link current. The current controller can still maintain 118.6Nm which could be enough to handle a

safe landing albeit the large torque oscillations making the EVTOL flight unstable. Although a large average torque is obtained, large current amplitudes are found in the phase currents and DC link current. Again, this could cause the battery to wear out and as well cause thermal runaways due to the large current amplitude. Furthermore, the phase currents are no longer sinusoidal which would be detrimental to the motor and diminish its lifetime.

The current sensors used could be based on hall effect or a shunt resistor. In this thesis, shunt resistors are chosen as the technology to sense current and they use Ohm's law to obtain a voltage measurement. The current sensors may fail by over heating that can affect the gain of the voltage signal in the controller. The power supply used to power the current sensors can also fail which would cause the sensors to output a voltage that does not represent the real current.

In the simulation scenario, the power supply of the current sensor is put into failure mode and the current sensor does not output a voltage signal anymore. The simulation results for this behavior on phase A current sensor is shown in Fig.3.23. As the fault occurs at one second, the speed controller senses a disturbance and tries to counteract this disturbance by adding a larger I_q reference current close to its saturation current of 400A. The speed controller achieves to get 166.1Nm average torque which is necessary to keep the speed at 5000RPM during the load disturbance and normal conditions. Although the speed is maintained, the large oscillations caused by the missing current sensor signal causes the phase A current amplitude to increase. The RMS current of the phase A current becomes 242A while phase currents B and C become much less. Due to this imbalance in amplitudes, the DC link current starts to exhibit large oscillations close to 300A. This translates to large torque oscillations on

the EVTOL. The larger amplitudes will cause the power devices to be used unevenly which will age one leg of the inverter more than the others which can then lead to a power device failure to that one leg.

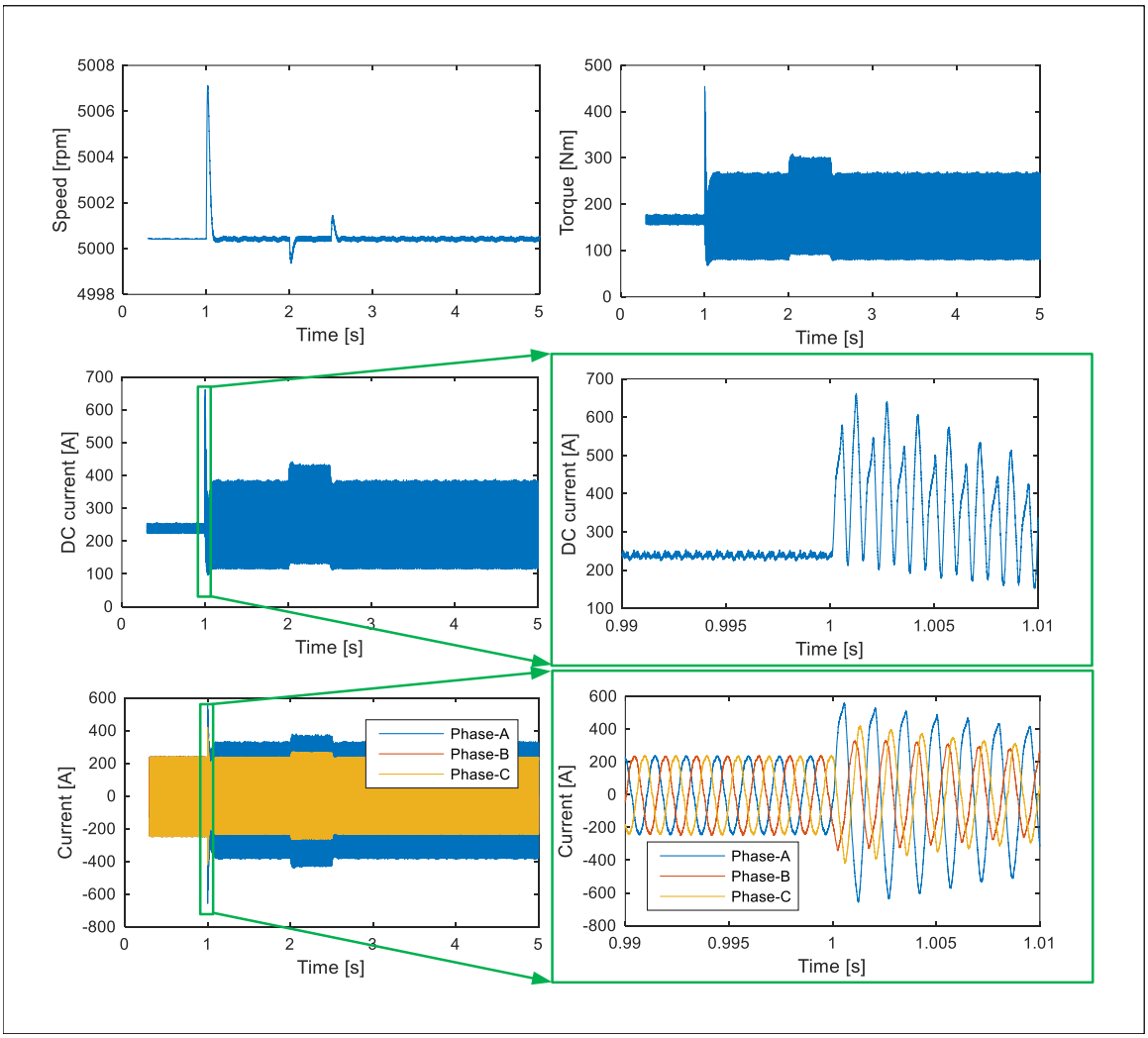


Figure 3.23: Simulation results for phase A current sensor failure.

The voltage sensors used in this application consist of a hall effect sensor [105]. The voltage sensors could fail such that the signal is buried in electrical noise or such that the power supply to the voltage sensor fails. If the voltage sensor signal is fed

back into the control algorithm, this could cause another type of instability where there is a demand of energy and not enough DC link voltage is available or maybe too much voltage which would cause some problems in the PWM driver having small duty cycle values. In this thesis, a constant voltage value is used for the control and the feedback voltage sensor signal is only used in monitoring to ensure the appropriate state of the EPU is achieved.

Temperature sensors could also be a source of failure in the same way position, current and voltage sensors can fail. The temperature signal can be buried in the noise floor of the PCB, it can also have in inherent voltage offset that causes the wrong temperature to be read. In this thesis, it is assumed that this sensor is functional at all times and provides the correct temperature to the control system.

3.4.2 Controller Failure

The control board itself could fail such that either it loses its main power of 28V or the auxiliary supplies could fail which would result in the loss of power for the control chip used for motor drive. This type of fault is catastrophic as this would result in failure of the motor drive controller. Typically for an application with high design assurance level (DAL) such as an EPU, the controller integrated chip (IC) needs to be robust and a field programmable gate array (FPGA) is used.

In general, a single event upset (SEU) can cause a state change within a given controller IC such as an FPGA. It can affect the configuration memory (CM), the random access memory (RAM) and the operating logic of an FPGA . Furthermore, aircrafts flying at higher altitudes are more susceptible to this failure and could create a catastrophic failure by altering the state of bits which are used to control and

monitor the EPU [106].

3.4.3 Gate Driver Failure

The gate driver of the inverter power devices can also fail which would cause the power devices to not function properly [107]. The resultant failure could be a shorted or open power device as mentioned in previous section or there could be a nuisance noise such as conducted or radiated EMI which would cause the gate driver to turn on mistakenly. The resultant behavior would be that of section 3.2.2 if the gate driver makes the switch fail open or that of section 3.3.3 if the gate driver makes the switch fail short.

3.4.4 Communication Loss

One of the last critical electrical fault that could occur is the communication loss on the avionics bus. In the case of communication loss, if the design of the control board FW is such that it relies on this communication bus only, the real-time command would not be read by the controller and thus the appropriate control commands would not be met. This could result in a catastrophic scenario where the aircraft cannot control its flight behavior in case of landing or turbulence during cruise.

Chapter 4

Design of Fail Safe Operation of EVTOL EPU

Based on the analysis in chapter 3, the current state of the art protection methods are not up to par for this new application. Minimal research has been done to understand the behavior of these faults in an EVTOL. The fault mitigation process is shown in Fig.4.1. The process to design the fail safe operation of the EVTOL EPU starts by identifying the faults that can occur in the EPU. Then, the measurement signals that are available in the EPU are analyzed to see which one can provide the best response in detection of the fault. Pre-processing of the data is then performed through various algorithms to enable the detection of the fault. Detection of the fault needs to be simple in terms that it is a threshold based system such that certification of the FW and SW can meet the fast paced development schedules but be robust enough to land safely. Once the fault is detected, the protection and coordination of components from the fault can be performed.

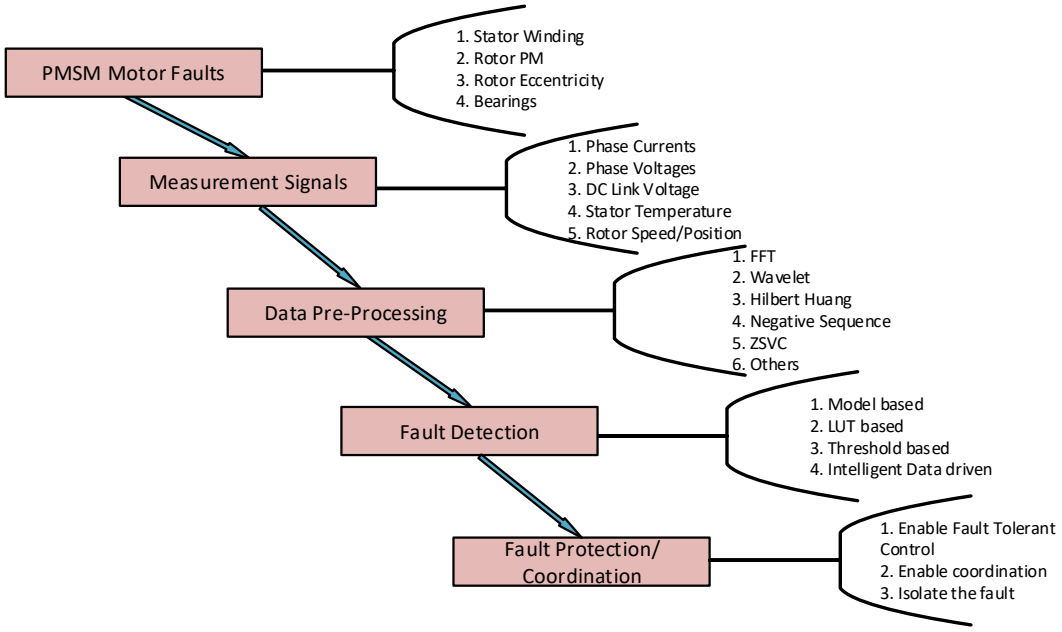


Figure 4.1: Fault process diagram tree.

4.1 Open Circuit Fail Safe Operation Strategies

The open electrical faults tend to not be a destructive fault and a fail safe control can usually be applied as seen in chapter 3. Whenever an open circuit occurs on the phases of the EPU, a fault tolerant control (FTC) can be applied such that mechanical vibrations and oscillations are reduced. In this section, a method to obtain the same average torque for the EPU is analyzed and applied to the OPF. It must be noted that a simple fail safe strategy must be chosen to ensure complexity is minimized.

4.1.1 Fault Tolerant Strategy for OPF in EPU

A very simple method to detect the fault for an OPF in an EPU consists of monitoring the current sensors as well as the balanced three phase currents as shown in (3.1). If

The goal of the OPF FTC is to minimize the torque ripple on the PMSMs rotor shaft and obtain the same pre-fault average torque. This minimizes the vibrations on the entire aircraft during the OPF. Nevertheless, this raises the copper loss of the PMSM. The OPF FTC aims to keep the same PI architecture to ensure low complexity. The OPF FTC consists of just changing the reference currents I_d and I_q while having an open phase a.

$$i_b = I_m sin(\theta - \beta), i_c = -I_m sin(\theta - \beta) \tag{4.1}$$

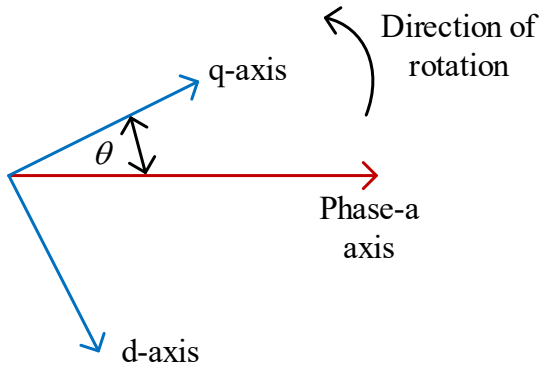


Figure 4.2: PMSM position reference of θ.

The derivation of the OPF FTC method starts by knowing (3.1) and then assuming a specific phase shift, β, to the reference currents i_b and i_c as shown in (4.1) which is relative to the angle θ as shown in Fig.4.2. Thus, two unknowns I_m and β need to be determined. According to the reference current in (4.1), the resultant average torque can be written as (4.2).

$$< T'_{em} >= \sqrt{3}\psi_{pm} I_m cos(\beta)\frac{P}{4} \tag{4.2}$$

By applying the Clarke and Park transformations to (4.1), the equivalent DC currents can be calculated in the dq reference frame. By choosing I_m to be at the desired operating point, the correct torque can be applied. The value of I_m can be calculated such that the same pre-fault average torque is provided by the PMSM faulty drive using $< T'_{em} >$, in (4.2). As shown in (4.2), the maximum average torque is whenever $\beta = 0$. This gives an expression for I_m in relation to the pre-fault I_q reference current as shown in (4.3).

$$I_m = \sqrt{3} I_{q,ref} \tag{4.3}$$

Using equations from (4.3), the post-fault current references $I'_{d,ref}$ and $I'_{q,ref}$ can be written as (4.4). These new current references enable the use of the same PI controller architecture as during healthy operation, minimizing the complexity of the overall EPU SW.

$$\begin{aligned} I'_{d,ref} &= -I_{q,ref} sin(2\theta) \\ I'_{q,ref} &= I_{q,ref}(1 - cos(2\theta)) \end{aligned} \tag{4.4}$$

4.2 EPU Short Circuit Fail Safe Operation Strategies

Due to the harsh nature of a possible short circuit between the motor phases, the inverter itself could result in damages if not properly protected. Thus it is necessary to ensure that the PMSM would fail-safe once a P2PSCF occurs. Both mitigation techniques use the inverter switches to mitigate the fault by either turning off all switches or turning on the bottom switches and turning off the top switches. One of the main requirements during a P2PSCF is to stop the rotor as fast as possible. Other methods are presented for the ITSCF depending on its severity.

4.2.1 Turning off the Inverter (FTC1)

To ensure the PMSM under P2PSCF is isolated from the rest of the eVTOL components, the inverter can be disabled by turning off all of its switches. This will prevent over-current conditions in the inverter switches and avoid penetrating the fault to the R-EDS. This technique is shown in Fig.4.3. To ensure that symmetry is kept within the EVTOL flight, if a fault occurs on the PMSM drive unit F_1 in Fig.2.6, then its counter part B_1 would be turned off [7].

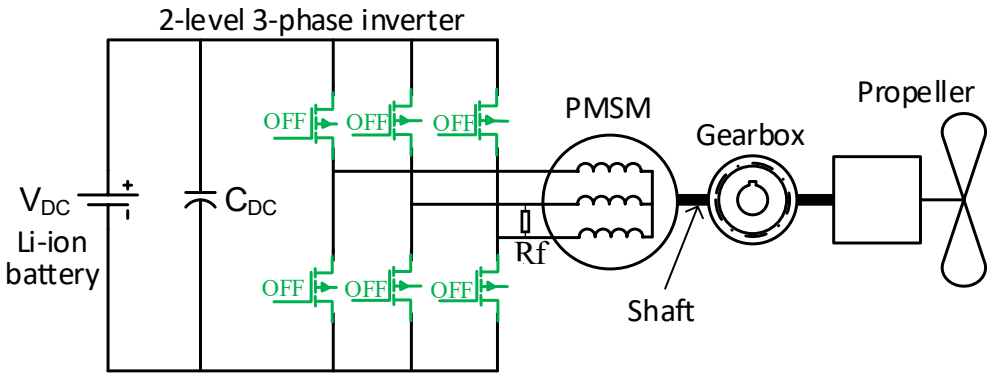


Figure 4.3: PMSM P2PSCF first mitigation technique (FTC1): Disable inverter by opening all switches.

4.2.2 Creating a Virtual Neutral Point (FTC2)

Creating a neutral point at the inverter side includes using the bottom switches of the inverter that connects all three phases to the negative terminal of the battery. In addition to that, creating a neutral point is arranged to short-circuit the zero sequence component of the phase voltages without affecting the positive and negative sequence components. This method is shown in Fig.4.4.

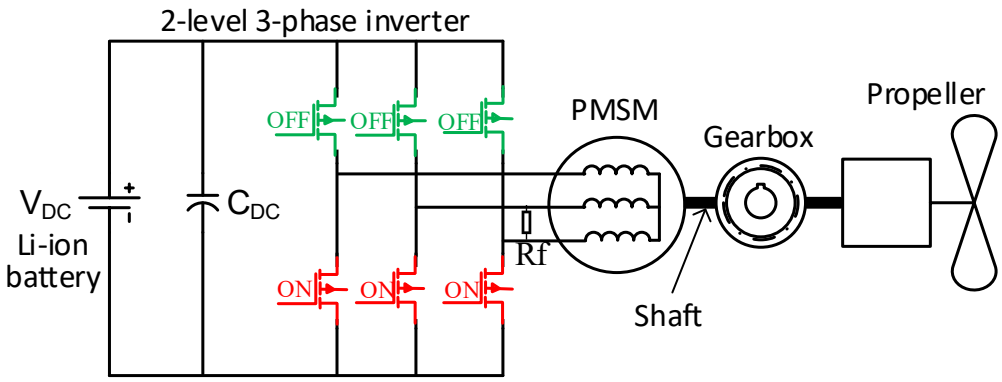


Figure 4.4: PMSM P2PSCF second mitigation technique (FTC2): Creating a virtual neutral point.

For the second case, the inverter bottom switches are turned on while the top switches of the inverter remain open. Since a neutral point is created using the inverter bottom switches, this makes the condition $v'_a = v'_b = v'_c$ during steady state. With the isolated neutral point, the only solution left is (4.5).

$$v'_a = v'_b = v'_c = 0 \tag{4.5}$$

4.2.3 EPU Inter-turn Short Circuit Fault Mitigation Strategies

There are many methods of detecting an ITSCF based on building a model such as state or parameter estimation [108–111], or a data based methods [112–114]. For this thesis, an analysis of the symmetrical components (zero sequence, positive sequence

and negative sequence components) of phase currents which could be used as a potential metric to detect the fault is presented as in [115]. The potential to use the symmetrical components of the phase currents consist of performing a fast fourier transform (FFT) to develop a simple threshold based algorithm to detect the fault.

To understand the negative and positive sequences of phase currents, the derivation for both of its parts is shown below. For a balanced 3-phase system, theoretically only positive sequence components exist. Once ITSCF occurs, the phase currents are no longer balanced and negative sequence components start to appear in the currents.

$$\begin{bmatrix} I_0 \\ I_{pos} \\ I_{neg} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & e^{j\frac{2\pi}{3}} & -e^{j\frac{2\pi}{3}} \\ 1 & -e^{j\frac{2\pi}{3}} & e^{j\frac{2\pi}{3}} \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \tag{4.6}$$

We can use (4.6) to calculate the symmetrical components. In (4.7), the three phase currents are expressed with phase shift and with an amplitude of I_{mx} where x denotes the phases a,b and c.

$$\begin{aligned} I_a &= I_{ma}cos(\omega t + \phi_1) \\ I_b &= I_{mb}cos(\omega t + \phi_2 - 2\pi/3) \\ I_c &= I_{mc}cos(\omega t + \phi_3 + 2\pi/3) \end{aligned} \tag{4.7}$$

We can write the 3 phase currents in complex domain and apply the (4.6) to obtain the positive and negative sequence components as shown in (4.8).

$$\begin{aligned} I_{pos} &= \frac{1}{3}(I_{ma}e^{j\phi_1} + I_{mb}e^{j(\phi_2 - 2\pi/3)} + I_{mc}e^{j(\phi_3 + 2\pi/3)}) \\ I_{neg} &= \frac{1}{3}(I_{ma}e^{j\phi_1} + I_{mb}e^{j(\phi_2 - 4\pi/3)} + I_{mc}e^{j(\phi_3 + 4\pi/3)}) \end{aligned} \tag{4.8}$$

We can define current space vector, $\boldsymbol{I}_s$, in complex domain as (4.9) which represents the demanded current of the PMSM which is supplied by the inverter.

$$\boldsymbol{I}_s = \frac{2}{3}(i_a - 0.5(i_b + i_c)) + j\frac{\sqrt{3}}{3}(i_b - i_c) \tag{4.9}$$

We can substitute complex representation of Ia, Ib and Ic in (4.9) and we can obtain an expression of the inverter current as a function of the positive and negative sequence components.

$$\boldsymbol{I}_s = \boldsymbol{I}_{pos}e^{j\omega t} + \boldsymbol{I}^*_{neg}e^{-j\omega t} \tag{4.10}$$

(4.10) confirms magnitudes of positive frequency terms gives the positive sequence components and magnitudes of the negative frequency terms are corresponding to the negative sequence components. We can use (4.9) to calculate the complex space vector in simulations and we can apply FFT to get the frequency spectrum of the Is. In that frequency spectrum positive frequencies are corresponding to the positive sequence components and negative frequencies are negative sequence components according to the (4.10).

Simulation results for both signal metrics are shown as well. It must be noted that the main goal of this section is to use the three phase current sensors and a position sensor for the EPU as the main sensor signals to detect the fault just as shown in Fig.3.1.

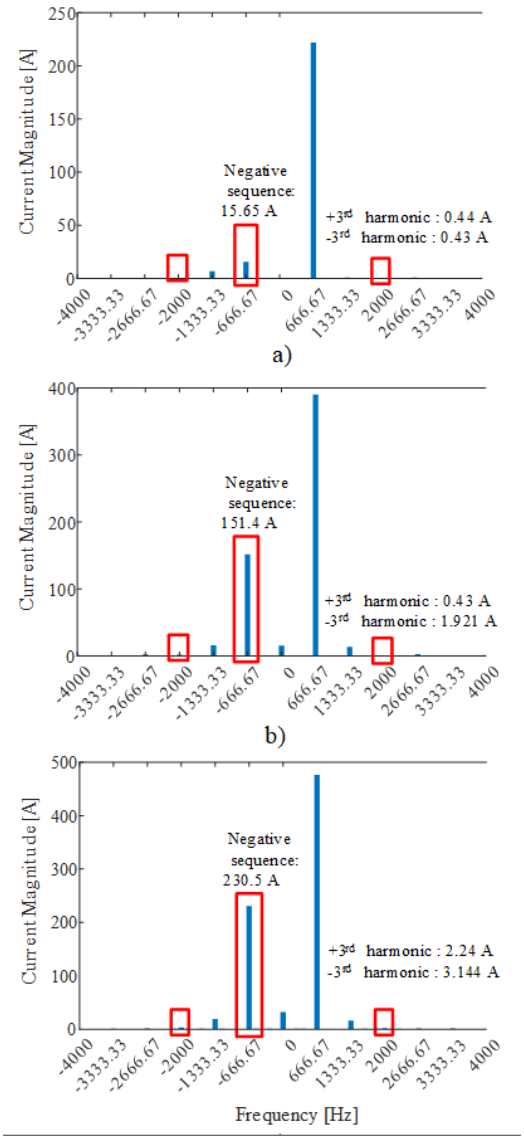


Figure 4.5: Simulation results for the FFT of Is in the PMSM: a) Healthy machine b) ITSCF with 5 faulty turns c) ITSCF with 11 faulty turns

The frequency spectrum for the signal, $\boldsymbol{I}_s$, is shown for healthy and faulty operations in Fig.4.5. The samples are for the FFT are sampled at 10kHz with a fundamental frequency of 666.67Hz. Five cycles are taken for the FFT with an FFT

sampling frequency of 1MHz.

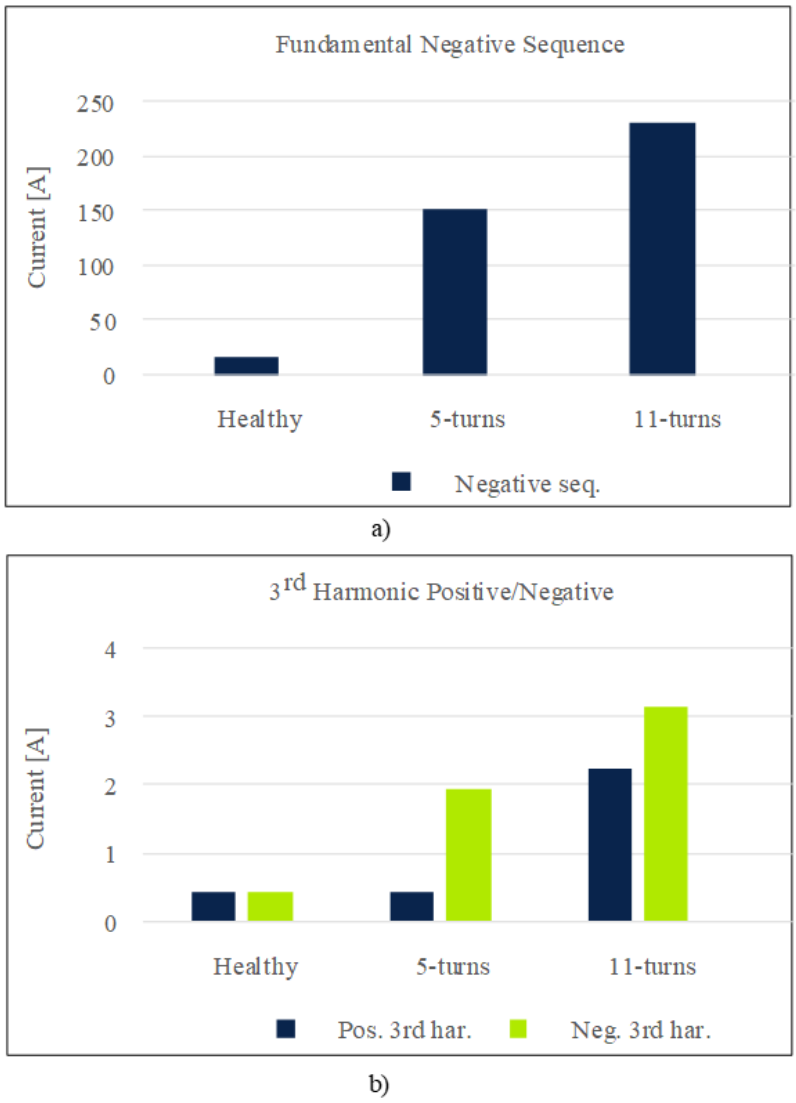


Figure 4.6: Simulation results for the FFT of the phase A current: a) Fundamental negative sequence amplitudes b) Third harmonic amplitudes.

The FFT in Fig.4.6 shows that even with a healthy machine, some negative sequence components are present. By increasing the number of faulty turns, the negative sequence component increases in amplitude. This may not identify the fault itself but at least gives a good analysis on what happens to the negative sequence components during this fault. With this information, a threshold based detection can be implemented by performing some analysis on the PMSM in the EVTOL EPU.

Furthermore, the fundamental and third harmonic signal of the phase currents, would exhibit an increase with the presence of the ITSCF due to the unbalanced 3-phase system. From running the fault for 5 and 11 faulty turns, the results obtained are shown in Fig.4.6 as a summarized bar chart. It can be seen that a combination of signals could be the proper metric to use for this type of fault to be able to localize and identify what type of fault.

In the event that the fault occurs and is detected, there are three main fault tolerant control methods that are considered in this analysis. The three types of fault tolerant control that is applied is:

1. Adapted current PI controller bandwidth to counter act the second order harmonics due to ITSCF. The response time of the PI controller is doubled to make sure the second order harmonics can be handled by the controller.

2. Opening all switches in the inverter. This is the same as in Fig.4.3.

3. Creating virtual neutral point with inverter by closing the bottom switches and opening the top switches. This is the same as in Fig.4.4.

The main purpose of these FTC methods is that the aircraft needs to be able to land safely without causing casualties. Since the EVTOL flight time is around

10 minutes to one hour, the methods above are satisfactory. Further development is needed to develop a detection method that is properly suitable for the ITSCF such that predictive maintenance can be enabled [66, 98].

4.2.4 Design of SSPC

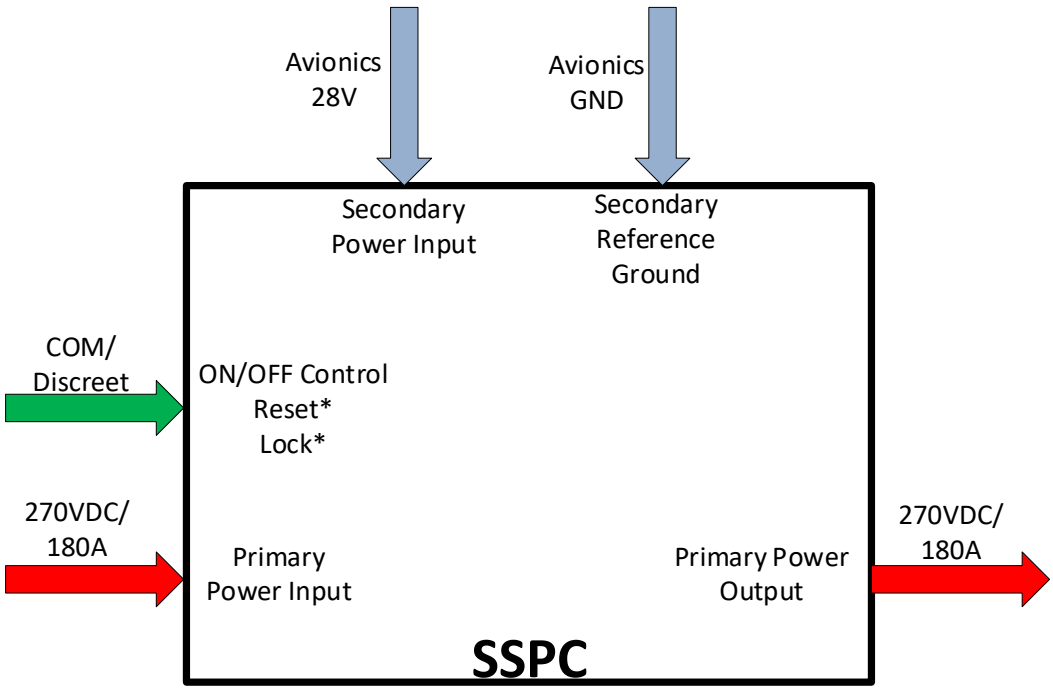


Figure 4.7: SSPC block diagram with I/O for HV and LV power.

In the case of having a short circuit failure on one of the MOSFETs or having a short circuit failure on a full leg of the inverter, FTC1 and FTC2 are no longer acceptable means of protecting the EVTOL EDS from the failure. As well, if the above FTC1 and FTC2 fail to protect the EVTOL EDS in certain conditions, like having an EPU

become a generator due to the EVTOL falling or the inverter controller fails for some reason, the SSPC is the backup protection device to ensure the fault is segregated from the rest of the EVTOL. In the case of having the inverter with a failed power device or having a complete shorted leg, the SSPC would act as the protection device from the rest of the EVTOL EDS. The SSPC can also be used during FTC1 and FTC2 to ensure that the EPU is segregated from the EVTOL EDS. Therefore, by using the SSPC at the input of the inverter to disconnect the inverter from the EDS, the EDS can be protected from further damage.

The SSPC is gaining popularity in the world of circuit breakers as they can be re programmable, can be reset, they have low power losses and they can react very quickly within the microseconds [84, 116]. They supervise and perform diagnostic algorithms to identify overload conditions and to protect components from short circuits [80, 83]. A simple block diagram of an SSPC module is shown in Fig.4.7.

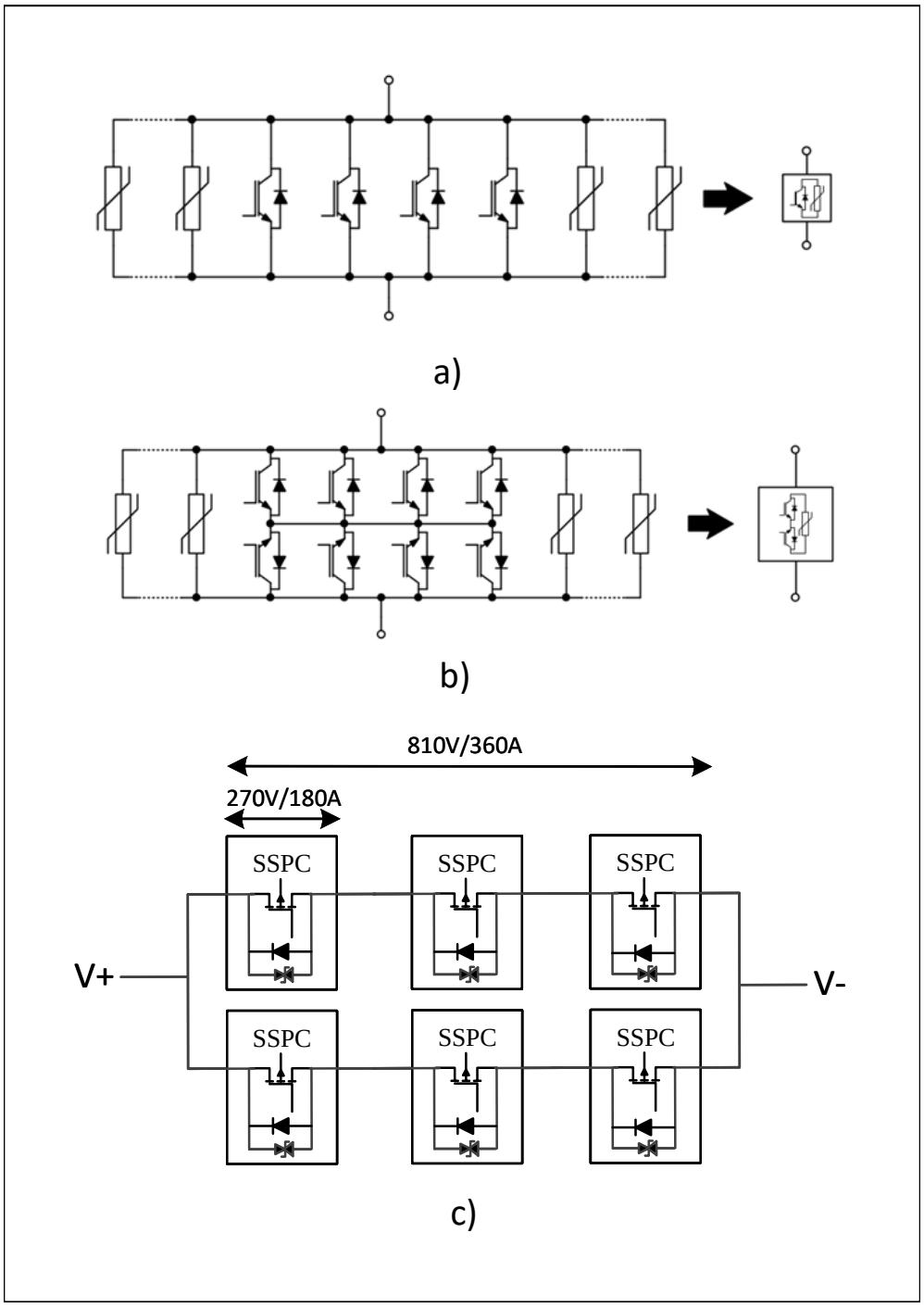


Figure 4.8: SSPC modular concept design. a) Unidirectional module b) Bidirectional module c) Combination string of SSPC modules.

The design of the SSPC consists of having a modular approach where each SSPC can be serialized and parallelized to achieve the necessary power of the application. Each common SSPC is sized with 270VDC/180A voltage and current ratings as shown in Fig.4.8-a for a unidirectional module or Fig.4.8-b for a bidirectional module. To obtain the necessary power of the inverter, three SSPCs are put in serial configuration and two parallel branches are achieved to ensure a safe and reliable power delivery as shown in Fig.4.8-c for the configuration needed with unidirectional 270VDC/180A SSPC modules for the EVTOL EPU. Due to time constraints, a unidirectional module was manufactured for feasibility studies. To achieve the bidirectional module, two unidirectional modules are put anti-parallel to each other to achieve the bidirectional blocking capabilities.

There are four main electrical components in the SSPC to take into critical consideration being the semiconductor device, the energy absorption or protection device, the current sensing device and the control board. The main specs of the SSPC designed is from the SAE standard AS4805A.

The component that performs the job to deliver the power from the source to the load consists of the switching device. This switching device is chosen to be a SiC MOSFET. These types of MOSFETs tend to have low on-state resistance which helps to minimize copper losses. Due to the nature of SiC, the turn on and turn off of the MOSFET can be done much faster than just an IGBT or a regular Si MOSFET. Furthermore, the device itself needs to be able to withstand the large transient power of the SSPC during turn on and turn off.

There are many MOSFET ICs available on the market with different packages as well with different die technology. The SiC MOSFET is chosen in this application due

to its high technology readiness level (TRL), ability to withstand high temperatures and its ability to turn on and off relatively faster than its counter part silicon. GaN technology is not considered in this application due to the low voltage characteristics of available ICs on the market. Although GaN devices have low voltage right now, they would be an interesting candidate for future applications. In this work, the TO-247-4L package is chosen due to its ability of segregating the source pin and the kelvin source pin [117]. This ensures that the parasitic inductance of the gate driving circuit is minimized in the gate driving circuit which is very crucial if we want to ensure fast slew rate for the turn on and off of the SSPC [118]. The chosen MOSFET consist of the UF3SC065007K4S from UnitedSiC [119]. The reason to choose this MOSFET is due to its low on-resistance ($R_{DS(on),typ}$) of $6.7m\Omega$. To meet the power loss requirement of less than 100W, six MOSFETs are put in parallel to ensure that a $1.1m\Omega$. With a nominal current of 180A, this would give the SSPC a theoretical power loss of 35.64W which is just a bit above the 60W power loss requirement.

There are many ways of driving multiple MOSFETs for SSPC applications [120, 121]. To ensure that the size and volume of the prototype SSPC is minimized, a single gate driver module is used to drive all six MOSFETs. The gate driver used consists of Infineon's 1ED020I12 [122]. To ensure that all six MOSFETs are driven properly with the appropriate instantaneous drive current, the IXD630 current amplifier is used which can deliver 30A in total. This will make it sufficient to drive all six MOSFETs at once [123]. Furthermore, this extra current amplifier ensures that current is always available to turn on and off the MOSFETs even though extra power is needed to drive the current amplifier.

When current is flowing in an electric circuit, it is always flowing through some

amount of inductance, L_{series}. This inductance acts to resist the change in the current. One might think of this affect as sort of an electrical inertia, it takes work to change the flow of current. To increase the current, the energy is stored in the inductance. To decrease the current, this energy must be transferred out from the inductance. When the semiconductor switching device is turned off, the current that was flowing through the switching device is transferred from the switch to the energy absorption device. In this part of the circuit, the energy absorption device is comprised of a Metal-Oxide Varistor (MOV) or transient-voltage-suppressor (TVS) [124, 125]. In this thesis, a TVS is chosen to protect the MOSFETs as well as the load from any overvoltage (OV) that can occur while connecting or disconnecting the load with an equivalent series inductance, L_{series}. This is because TVS diodes tend to have a higher reliability than MOV under continuous transient events and provide a faster response [125–127].

The blocking voltage of the TVS must be less than the maximum voltage of the MOSFETs as well as the maximum bus voltage allowed on the EVTOL. Due to kirchoffs voltage law (KVL), the higher the clamping voltage of the TVS, the faster the current would reach the zero mark as stated by (4.11) [125].

$$\begin{aligned} V_{clamp} - V_{Bus} &= L_{series}(\frac{\delta I_{SSPC}}{\triangle t}) \\ \therefore \triangle t = t_{faultcurrent} - t_{zerocurrent} &= \frac{L_{series}(I_{SSPC})}{V_{clamp} - V_{bus}} \end{aligned} \tag{4.11}$$

Where V_{clamp} is the clamping voltage, V_{Bus} is the bus voltage, I_{SSPC} is the current through the SSPC, $t_{faultcurrent}$ is the time when the fault current occurs and $t_{zerocurrent}$ is the time when there is no longer any current through the SSPC. Although it would be advantageous, a higher clamping voltage would mean a larger peak power, P_{TVS}, that the TVS would need to dissipate as depicted in (4.12). Furthermore, the energy

absorbed, E_{TVS}, by the TVS, shown in (4.13), is the integral of the peak power dissipated by the TVS which means that if a larger voltage is used, a larger TVS must be used.

$$P_{TVS} = I_{faultcurrent} V_{Clamp} \tag{4.12}$$

$$E_{TVS} = \int_{t_{faultcurrent}}^{t_{zerocurrent}} P_{SSPC}(t)dt \quad = \frac{1}{2} I_{faultcurrent} V_{clamp} * \triangle t \tag{4.13}$$

Where $I_{faultcurrent}$ is the fault current. To ensure that the power is safely dissipated in the TVS, the $10/1000\mu s$ double exponential current waveform is used but with a factor of roughly 1.32 less power due to the fact that the current waveform is triangular and not exponential [125–127]. The $10/1000\mu s$ double exponential waveform lets the designer know how much power can be dissipated by the TVS before failing. Since the first prototype SSPC needs to withstand currents of up to 540A and the chosen MOSFETs have a maximum voltage of 650V, it is necessary to choose a TVS diode that have a clamping voltage which is 50% of that value. Therefore, due to the nominal bus voltage of 270VDC and the requirement such that 540A for the peak fault current, the chosen TVS consists of the 30KPA270CA from Littelfuse [128]. Its clamping voltage is of 331.76V and its maximum current is 69.5A and the TVS can dissipate 30kW of power. By putting 3 in parallel to one MOSFET in the SSPC, this would give enough margin for the TVS to be able to handle fault currents of 540A total for the SSPC while not worrying that the TVS would fail. Its operating temperature ranges from -55°C to 175°C which is acceptable for the case of the SSPC.

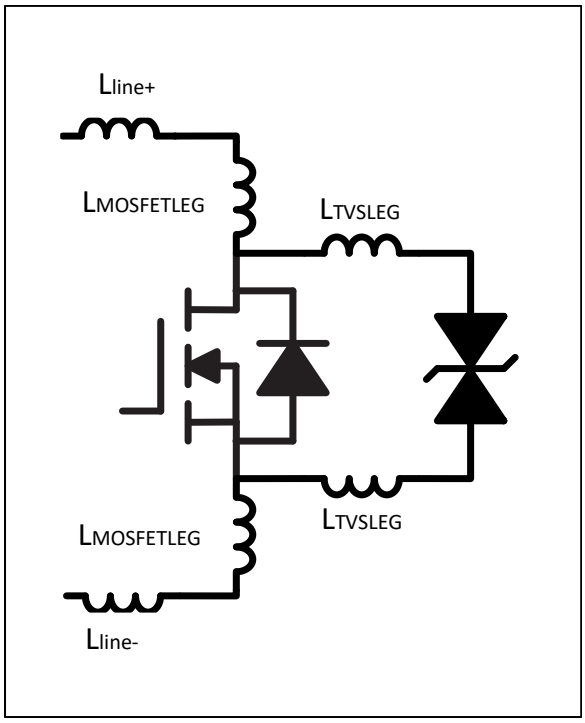


Figure 4.9: Building block of the SSPC consisting of the switching and protection devices with stray inductance.

To ensure that the SSPC can switch off high currents very fast, the power board must be designed with the goal of minimizing stray inductance in the components and in the board itself. Since the components chosen have large leads, the trace inductance must be minimized. A simple building block of the SSPC MOSFET and protection device with their stray inductance is shown in Fig.4.9. As can be seen, minimization of L_{line+} and $Line_{line-}$ must be performed to minimize the total stray inductance of the building block as they are the only degree of freedom in the chosen design.

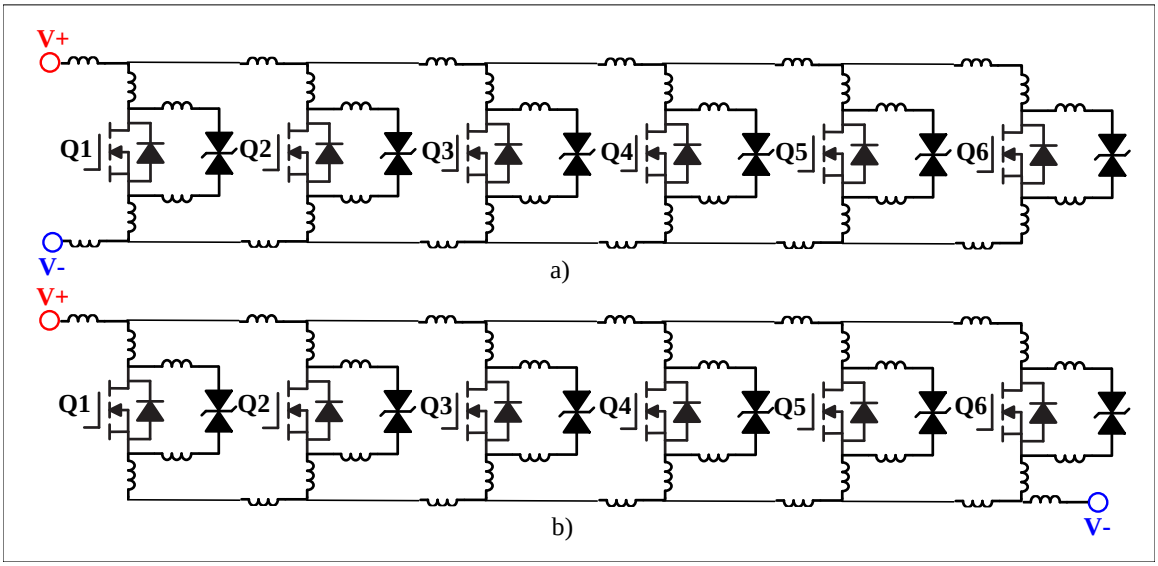


Figure 4.10: Design concepts for the SSPC power board main power traces: a) Connections of both the positive and negative are made on the first MOSFET b) The positive connection is on the first MOSFET and the negative connection is on the last MOSFET

The SSPC power board geometry consists of a card which can be rack mounted.This makes the maintenance of the EDS much easier and similar to internet cards in data servers. Since the main power connections have to be made on the same side of the SSPC, there are two methods that the SSPC power board traces can be designed to achieve such a system design which as shown in Fig.4.10. Fig.4.10-a shows a design where both connections are done on the first MOSFET, Q1, while Fig.4.10-b shows the positive connection on the first MOSFET, Q1, while the negative connection is on the last MOSFET, Q6. As will be shown later, the second configuration will have an added power trace with no components on top, which could be considered as a waste of space for the power density.

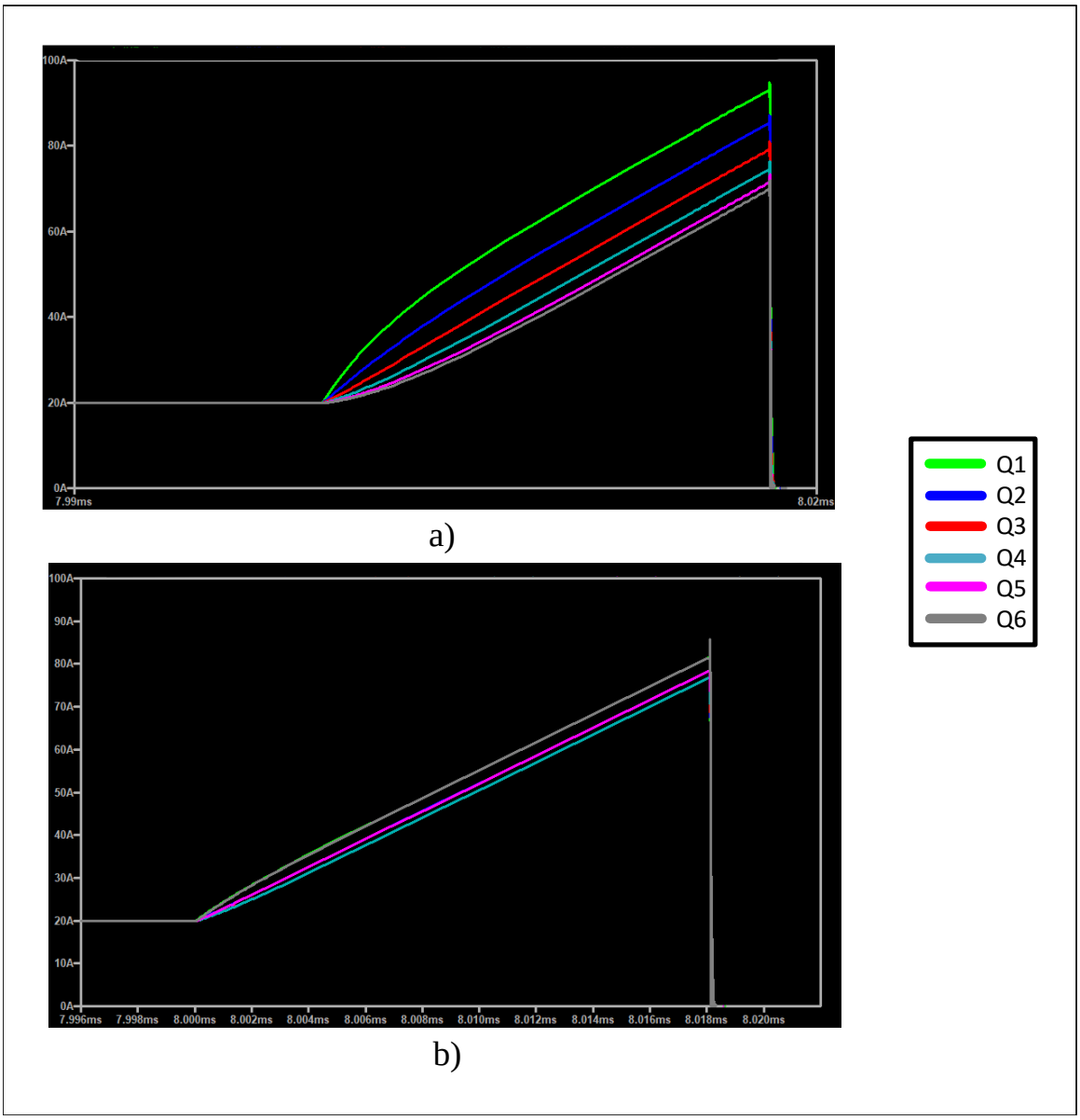


Figure 4.11: Current distribution of SSPC MOSFETs during fault conditions: a) First configuration b) Second Configuration

To illustrate the current distribution for both configurations, an LTspice simulation was performed with the stray inductance of both configurations modeled. The

simulation was performed with inductance $L_{MOSFET} = 4nH$, $L_{TVS} = 4.3nH$ and $L_{line+} = L_{line-} = 3nH$. The current in each MOSFET is analyzed during fault conditions where the MOSFET carries 20A of current and then is increased to 80A. The first configuration shows a minimized stray inductance of only L_{line+} for the first MOSFET Q1, but a stray inductance of $6 * L_{line+}$ at the input of MOSFET, Q6, due to the five extra SSPC building blocks in front of it. This may be advantageous but as will be shown, the current distribution during transient conditions are not ideal for this configuration. The extra impedance of the sixth MOSFET makes it that it receives less current than Q1 during fault conditions as shown in Fig.4.11-a. The total difference in current distribution was as high as 35A in simulation. This inconsistent current distribution may lead to Q1 failing much faster than Q6 and thus cause the SSPC to fail at a more rapid rate.

Compared to the second configuration, an added output inductance is added to make sure that the negative connection is on the same side as the positive connection, but all MOSFETs see the same inductance. This added inductance was simulated to be 6nH. Thus, all MOSFETs have very similar impedance which makes the current distribution during transient conditions much more favorable as shown in Fig.4.11-b. The largest difference seen in simulation was 10A between the maximum current and minimum current through a MOSFET. The outside MOSFETS (Q1 and Q6) had the least amount of impedance while the middle MOSFETs (Q3 and Q4) had the largest impedance. This will make the failure rate of each MOSFET more close to each other and thus increase the lifetime of the SSPC compared to the first configuration where each MOSFET had different impedance where Q1 has the lowest impedance and Q6 has the highest impedance.

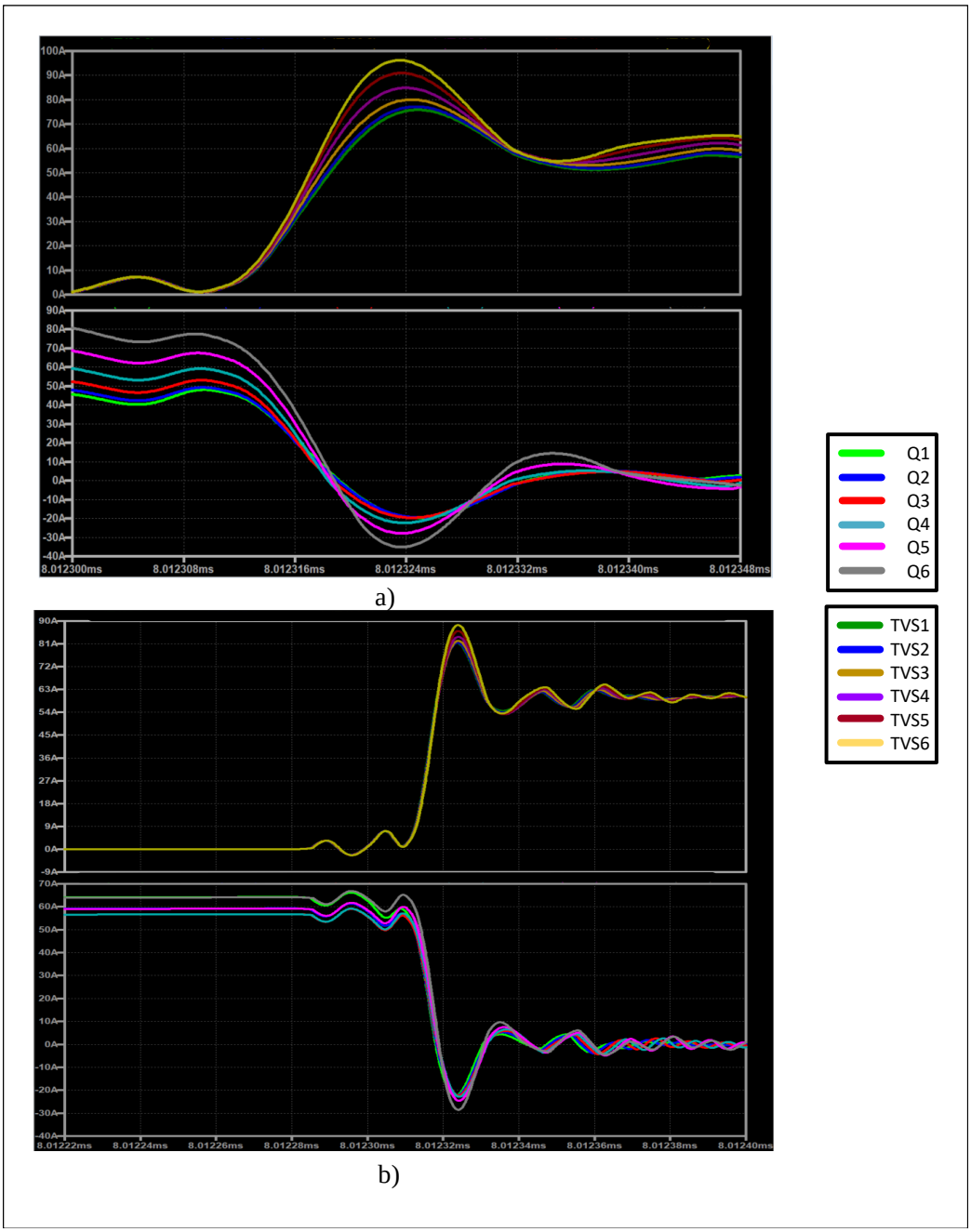


Figure 4.12: Current distribution of SSPC MOSFETs during turn off with TVS current on the top waveforms and MOSFET current on the bottom waveforms: a) First configuration b) Second Configuration

To evaluate the turn off conditions for both the TVS and MOSFETs, the same simulation is carried out. The TVS and MOSFET current distributions are compared for both configurations. Fig.4.12 demonstrates the current distribution results in simulation during turn off conditions. The same simulation profile is used as in Fig.4.11 simulation results. As can be seen in Fig.4.12-a for the first configuration, the maximum difference in current amplitude of the TVS diodes between TVS1 and TVS6 is of 25A while the maximum difference in MOSFET current from Q1 and Q6 is 35A. This again, can create large complications in the lifetime of the SSPC as devices may fail quicker than anticipated. In the second configuration shown in Fig.4.12-b, it can be seen that the maximum difference between TVS1 and TVS3 is about 11A while the maximum different between MOSFET current Q1 and Q3 is 10A which is much lower than the 35A from the second configuration. So, with these simulation results, the second configuration is chosen for final design of SSPC.

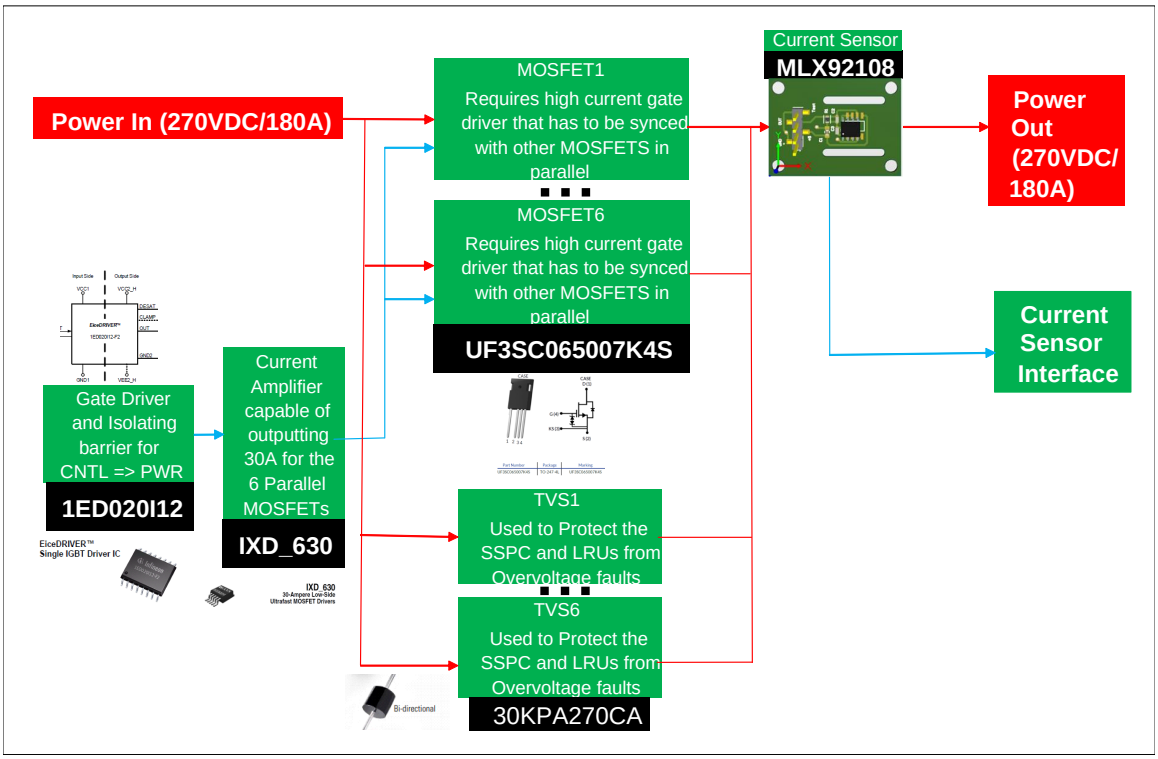


Figure 4.13: Design of the power board circuit for the SSPC.

By choosing the second configuration with added trace inductance but better current distribution The final power board design can be done. The final power board design of one SSPC module consists of having 18 30KPA270CA TVS in parallel along with six UF3SC065007K4S in parallel and is shown in Fig.4.13. The design of one module may be a bit overkill but ensures that the SSPC will not fail in the worst case scenario.

The current measurement method is very important in the SSPC since it protects the bus from any over current conditions from the load. Their are many methods of measuring current but the main three options are shunt resistor and hall effect based current sensors. For the current range of the SSPC, a shunt resistor will have to be

a large such that its resistance and power losses are low. Furthermore, due to the large nature of this shunt resistor, this shunt resistor would have a large parasitic inductance compared to a purely capacitive or resistive load.

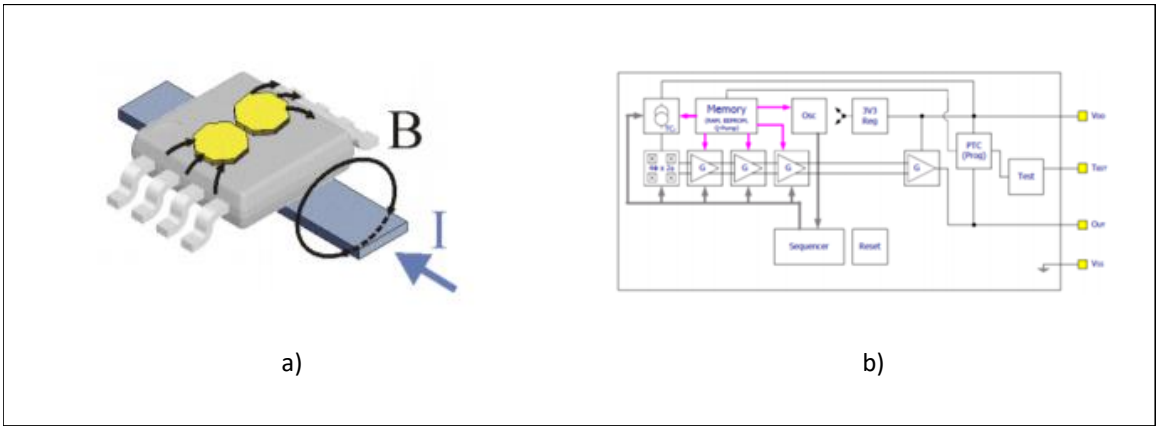


Figure 4.14: SSPC current sensor MLX91208 block diagram and functionality overview [129]. a) Current measurement method b) overall block diagram of the MLX91208

The technology used to sense current is the hall effect IC from Melexis called the MLX91208 [129]. The MLX91208 is a fully customer-programmable monolithic sensor IC packaged in standard SO-8 package. The product is a single chip Hall sensor which provides an output signal proportional to the flux density applied horizontally and is therefore suitable for current measurement. It is ideally suited as an open loop hall effect current sensor for printed circuit board (PCB) or bus bar mounting. It features small size application design and a simple construction for various current ranges from few Amperes up to 1000 Amperes. The transfer characteristic of the MLX91208 is programmable in terms of offset, gain or temperature compensation. The linear analog output is designed for applications where a very fast response is

required, as in SSPCs. The sensor features the IMC-Hall® technology, which leads to very high sensitivity thanks to integrated magnetic concentrators (IMC) deposited on the die. The Hall Sensor provides a high speed analog output signal proportional to the external applied flux density. The MLX91208 current sensors enables the user to construct a precise current sensor solution with fast response time of $3\mu s$. The conventional planar Hall technology is only sensitive to the flux density applied orthogonal to the IC surface. The IMC-Hall current sensor is sensitive to the flux density applied parallel to the IC surface. This is obtained through the IMC-Hall technology which is deposited on the CMOS die (as an additional back-end step). The MLX92108 used has a gain of 10mV/A.

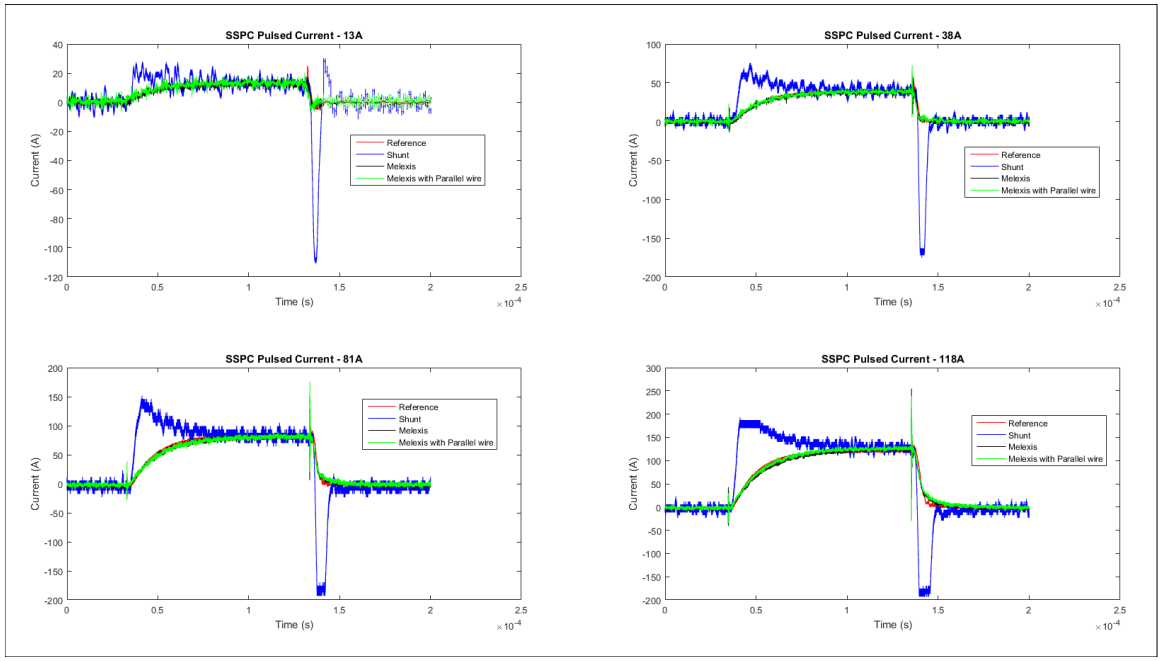


Figure 4.15: SSPC Current measurement method with 270VDC.

As can be seen in Fig.4.15, the melexis current sensor gives very good response with very low error during transients and steady state conditions. The shunt resistor

can be seen to have a large over shoot during turn on and a large under shoot during turn off which could false trip the SSPC SW. A filter could be used but this would reduce the bandwidth of the SSPC response. The melexis has the appropriate time response and does not provide large over shoots during turn on. Some noise during turn off is found but this is due to the measurement method with a passive probe through an oscilloscope.

To ensure that the SSPC can respond within the required timing of less than $10\mu s$ in case of a short circuit current, a hardware (HW)based logical latching is needed as shown in Fig.4.16. The logical latching itself consists of a voltage reference to set the tripping equivalent voltage, a low pass filter (LPF) to ensure that any false tripping is avoided, a comparator, a latch to ensure the system is always off, and logical AND gates to ensure the system does not turn on unless external signals are asserted from avionics. In the case of failure of the SW or high short circuit currents, this circuit will react within the specified required time to ensure protection of the load and source.

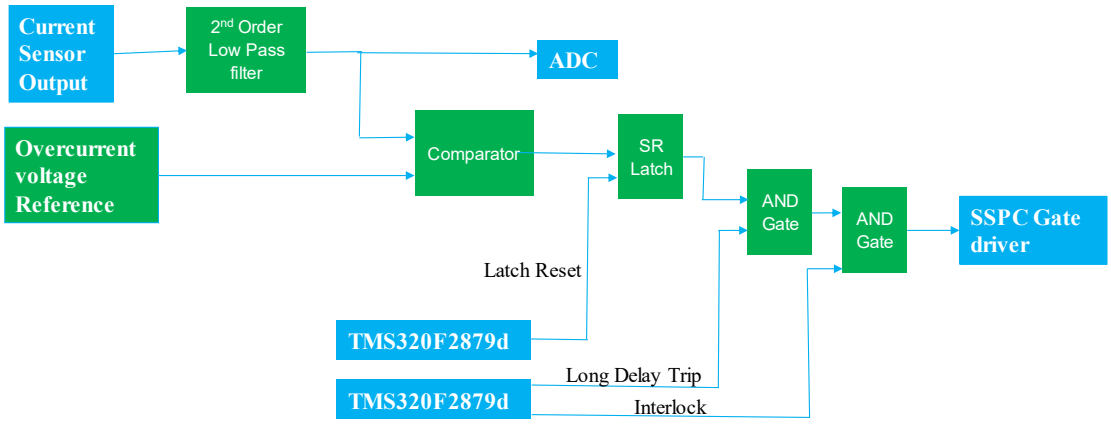


Figure 4.16: Designed instantaneous logical latching for HW interrupt.

To ensure that the logical latching would react within the specified time and not

produce any false tripping due to noise, the ICs for the architecture of the logical latching must be chosen carefully. The low pass filter (LPF) cut-off frequency is set to 200kHz to ensure a response of $5\mu s$ is achieved by using a second-order Butterworth filter with the TLV341IDBVR operational amplifier (Op-Amp) from TI [130]. The Op-Amp has an internal bandwidth of 2.3MHz which makes it ideal to meet the necessary timing requirement. The comparator IC consists of a LMV331M5 from TI as well which has a 200ns propagation delay [131]. The SR Latch consists of the SN74LVC02ADR IC from TI which has a maximum of 4.4ns propagation delay [132]. The AND gates are SN74LVC2G08DCTR from TI with a maximum 4.7ns propagation delay [133]. The final propagation delay value considered is the gate driver itself which consists of Infineon's 1ED020I12 with a propagation delay of 170ns [122]. According to (4.14), which calculates the total propagation delay from current sensor to the gate driver, the total delay is $8.3\mu s$ which meets the $10\mu s$ delay requirement for large short circuit values.

$$\begin{aligned} Delay_{Propagation} =& Delay_{MLX92108} + Delay_{LPF} + Delay_{Comparator} + Delay_{Latch} + \\ & 2 * Delay_{ANDGate} + Delay_{GateDriver} + TurnOffTime_{MOSFET} \end{aligned} \tag{4.14}$$

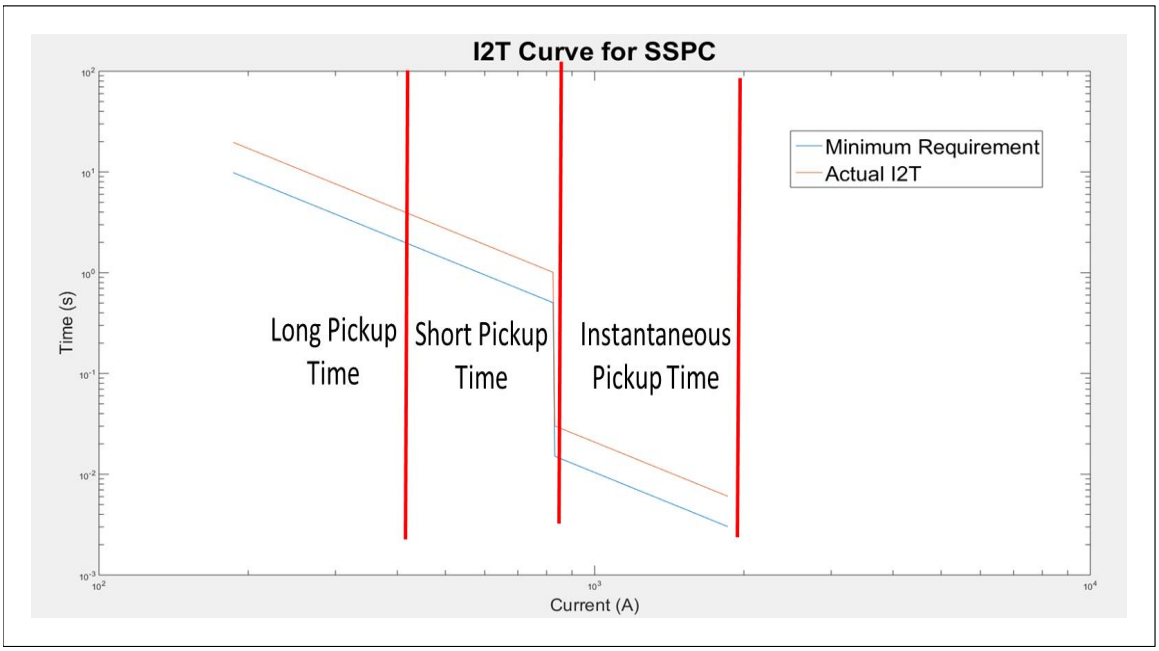


Figure 4.17: SSPC design of I2T curve tripping.

Unlike circuit breakers, SSPCs provide true I^2T protection. An SSPC cuts power when there is too much energy transfer where a circuit breaker will trip only when the current gets to its trip point. If a short circuit is about to happen in a system and the current slowly gets higher instead of instantly reaching the trip point, the I^2T protection of an SSPC will turn the output off. This functionality is demonstrated in (4.15). The corresponding I^2T curve is shown in Fig.4.17.

$$I^2 = \int_{t_1}^{t_2} (i(t) - I_{rated})^2 dt \geq (I^2T)_{max} \tag{4.15}$$

The I^2T curve has three main points where we need to distinguish between the long pickup time, short pickup time, being long delay (LD) trips and instantaneous pick up time being instantaneous trips (IT). Each one of these parts of the I^2T curve

consist of a different maximum time and current and then applying (4.15) with these appropriate values. The values designed for this application are shown in Table 4.1.

Table 4.1: Pick up times and currents for I2T curve of the SSPC.

	Minimum Time (s)	Desired Time(s)	Current (A)
Long Pick up	2	4	414
Short Pick up	0.5	1	828
Instantaneous Pick up	0.003	0.006	1863

The SW process state machine to be implemented is shown in Fig.4.19. The SSPC SW consists of five states:

- **Blocked**: The SSPC is initialized in this state where only external avionics can make it switch states. This state is also used when the SSPC senses that a fault has persisted for the number of Reset_Count on the load.
- **Off**: The SSPC senses voltage and current but block voltage and current to the load.
- **On**: The SSPC is delivering power to the load while monitoring current with the I^2T curve SW.
- **Tripped**: The SSPC is turned off until current goes down to zero due to an overcurrent fault in I^2T or instantaneous latch trip. Once current reaches zero, the SSPC is turned on again.
- **Locked**: A configuration of the SSPC that prevents it from going to the On state.

With these five states, the SSPC also consists of having 6 digital signals which are listed below:

- **Off/On** : Commands the SSPC SW monitoring.
- **g** : Gate signal to let power through the SSPC.
- **LD** : Long delay tripping based on I^2T curve.
- **IT** : Instantaneous tripping signal based on the HW latching circuit.
- **Reset_count** : Persistence count in the presence of a LD or IT fault.
- **Lock** : External signal which locks the SSPC in the off state.

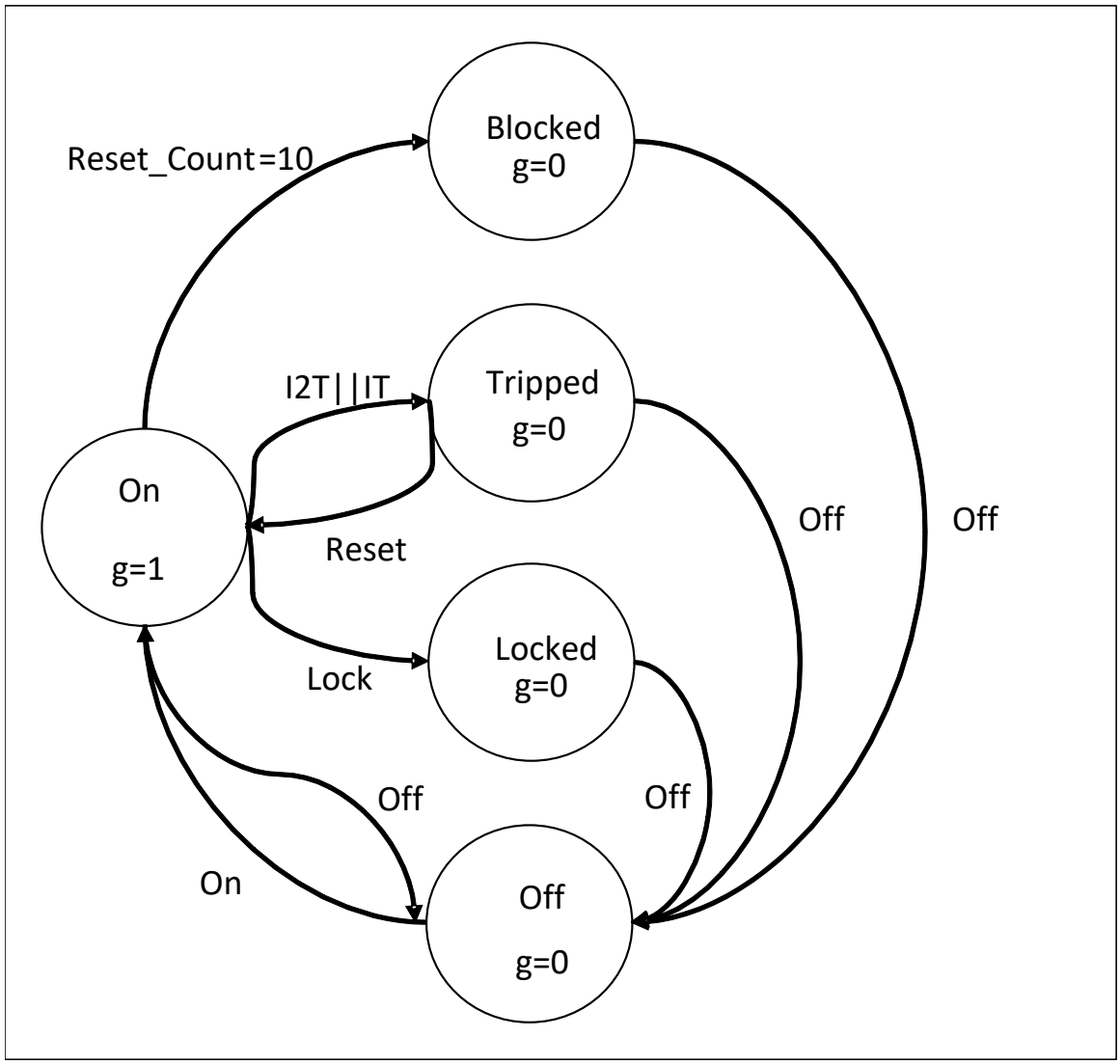


Figure 4.18: SSPC design process for SW/FW development.

With the above known IOs and state machine, the development of the FW can be performed through a process demonstrated in Fig.4.19 to minimize verification efforts when integrating the power and control boards together. By ensuring the concept is properly implemented, a MATLAB/Simulink model is developed by using the Stateflow toolbox to interface with a Simulink model of the physical SSPC. The

stateflow model exactly implements the state machine in Fig.4.18 along with the I^2T algorithm with the values in Table 4.1. Once the stateflow model and Simulink model have the appropriate results, code is generated from the stateflow model and then implemented on a TMS320F28379D launchpad which is then tested with an emulated voltage sensor. This is to avoid to interface the SW with high power currents to ensure its functionality is as intended. Once the functionality of the SW is validated, the SW can then be verified through experimentation on the physical SSPC. This development allows parallel designs of the power board, control board and SW design to ensure a fast time to market.

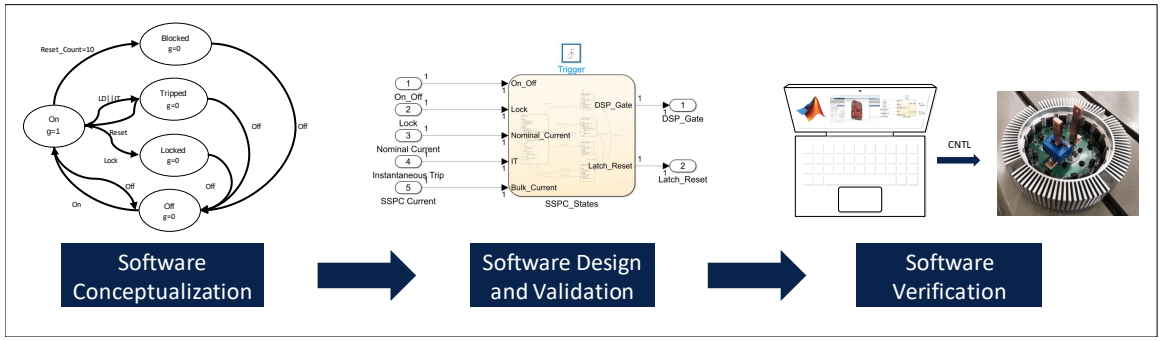


Figure 4.19: SSPC design process for SW/FW development.

With the power board, current sensor board, control boards and SW concept designed, the final PCB stack can be assembled and manufactured. All three boards are shown in Fig.4.20.

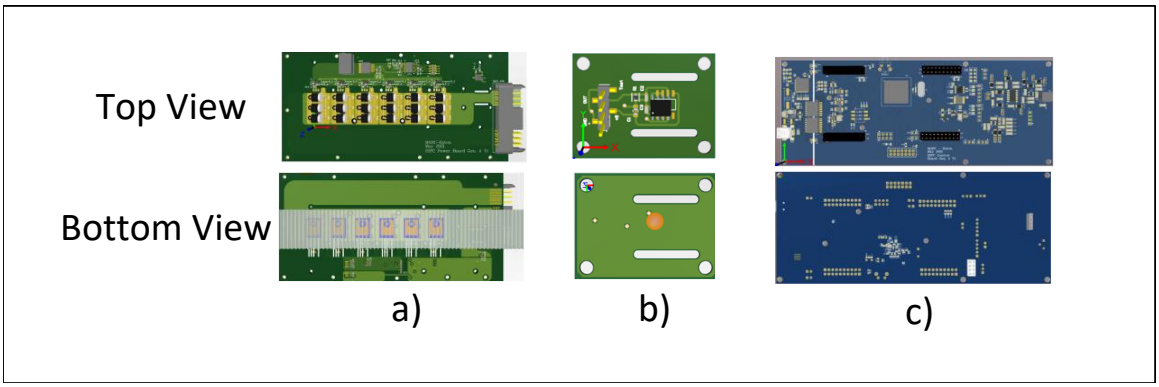


Figure 4.20: Designed SSPC PCB Assembly. a) Board stack assembly b) SSPC in 3D printed enclosure

The full stack assembly with a 3D printed enclosure in shown in Fig.4.21. The final step to testing the SSPC consists of its ability to dissipate heat. The SSPC must be able to handle to dissipate close to 60W of heat to ensure the MOSFETs do not overheat and thus increase in resistance which would increase power losses. This is done by dissipating the heat of the MOSFETs while they conduct through a heat sink the size of the PCB. The thermal design details of the SSPC can be found in the following research [134].

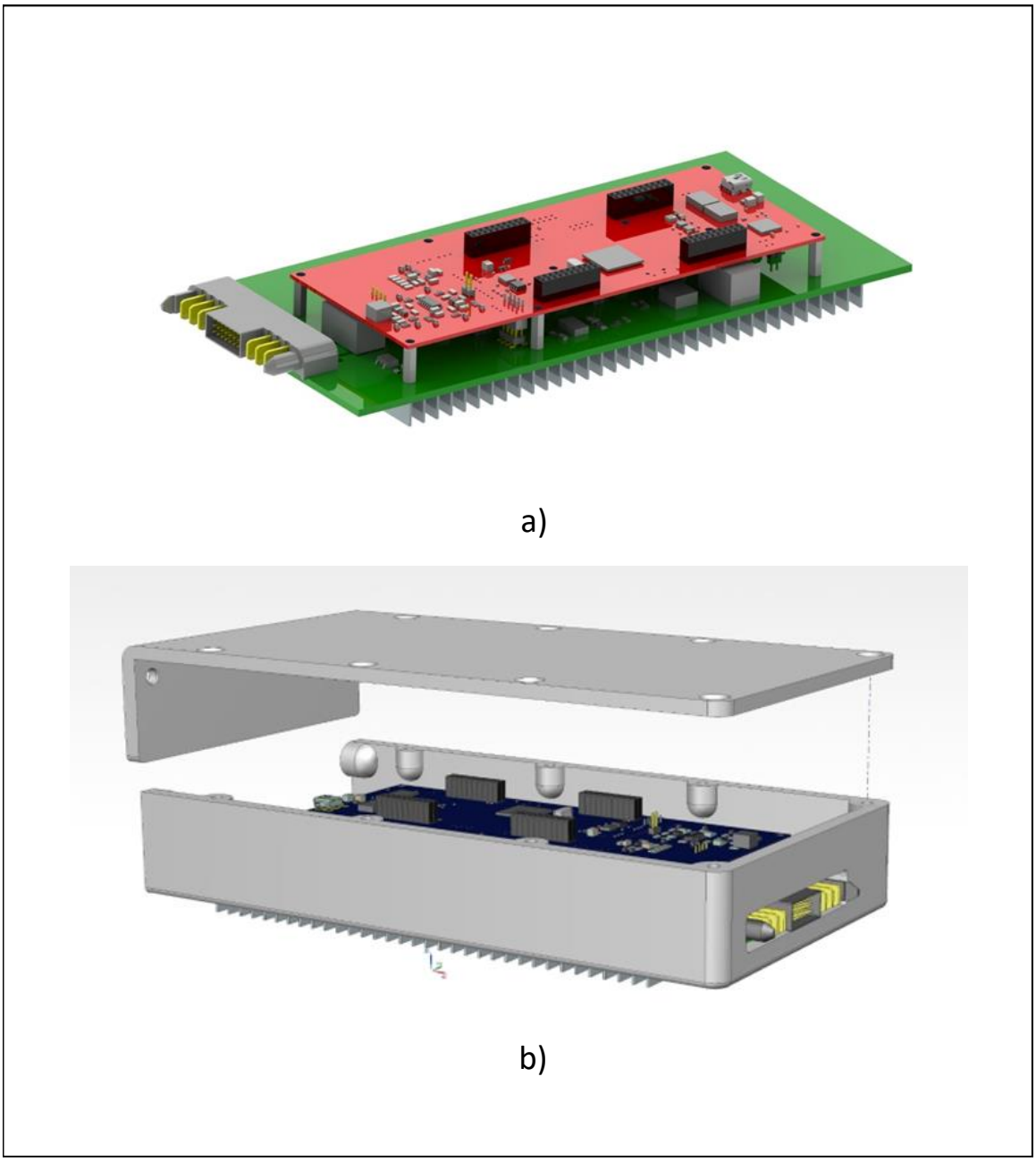


Figure 4.21: Designed SSPC PCB Assembly. a) Board stack assembly b) SSPC in 3D printed enclosure

4.3 Control Stage Fail Safe Operation Strategy

In terms of the control stage failure mitigation strategy, a simple control is needed such that complexity is minimized. Sensorless laws are well known but tend to be complicated and become a cumbersome activity for verification. To minimize the efforts in verification, sensorless laws can be used in certain known conditions and minimize the feedback loops such that stability analysis activities are minimized. In this section, assumptions on the EVTOL failure modes are made to ensure the techniques proposed are valid during the failure mode. Monitoring techniques are mentioned such that a safe landing can occur.

4.3.1 Sensor failure mitigation strategies

To detect an RPS faulty supply, imbalance fault or offset fault, the detection of the fault can be performed by using a simple trigonometric relation shown in (4.16), where $Threshold = 0.05$ as this would give a 5% error from either sine or cosine signal amplitudes. Of course, the assumptions take into account that only the RPS is in failure and that the PMSM is still running in the healthy condition with the appropriate parameters.

$$abs(sine^2 + cosine^2 - 1) > Threshold \tag{4.16}$$

Once the fault is detected, the fault mitigation strategy can be used. In the case that the RPS fault is detected, a sensorless control scheme could be used for a short time to ensure that the aircraft lands safely [135]. The type of sensorless law to be used consists of the improved proportional-integral sensorless law (IPISL) which is

depicted in (4.17). The block diagram of this method is shown in Fig.4.22.

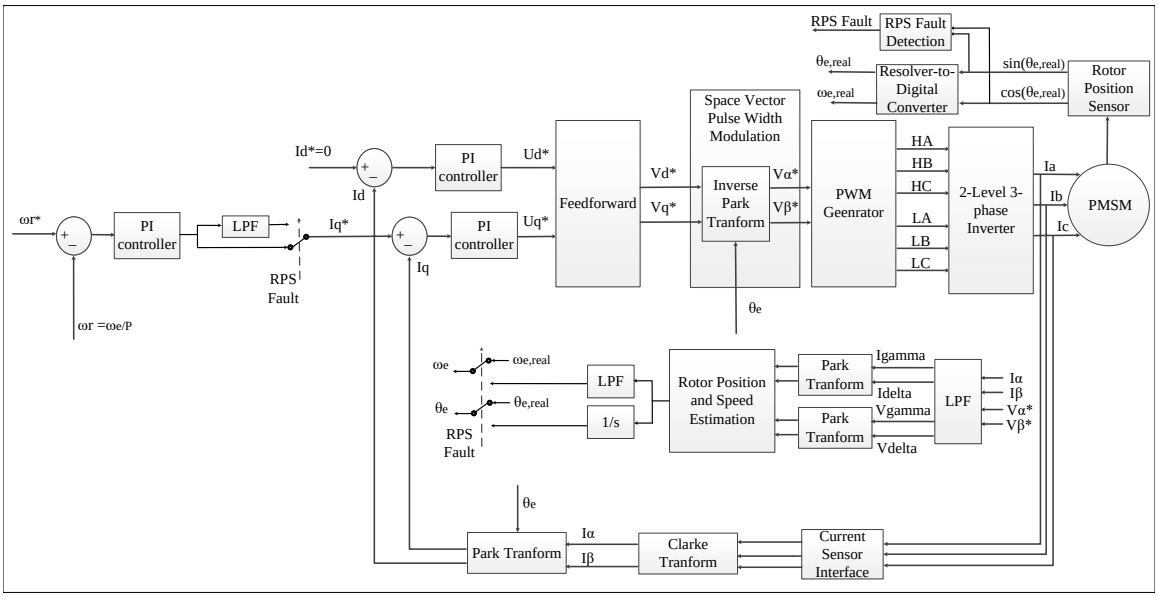


Figure 4.22: Block diagram of FOC with IPISL during RPS fault.

$$\omega_{e,estimated} = \frac{1}{\lambda_{pm}}(e_{gamma} - (1 - K_{si}sign(e_{delta}))bsign(e_{gamma})e_{delta}) \tag{4.17}$$

Where e_{gamma} and e_{delta} are the errors on the back EMF of the PMSM due to the mechanical sensor failure. The factor b consists of a tuned parameter which greatly influences the response of the IPISL. K_{si} is another tunable parameter which helps with the convergence of the equation along with the new $sign(e_{delta})$.

The scenario in which the IPISL algorithm is implemented assumes that the PMSM is healthy, and that if a RPS fault is detected with (4.16), then a reduced bandwidth of the control speed is used as shown in Fig.4.22 by using a simple first order LPF. This is to remove any noise which could come from the IPISL algorithm

that could come from the sensors themselves and give a slower response for the current controllers. This would not affect too much the landing of the EVTOL since the rotor is still spinning at an appropriate speed and a large acceleration is not needed in this case. The conditions during the fault consist of the rotor spinning at 5000RPM while having a torque set to 166.1Nm. The algorithm 1 describes the FSO while an RPS fault occurs.

Algorithm 1 FMS for the FSO of an EVTOL while an RPS fault occurs.

1: **if** $abs(sine^2 + cosine^2 - 1) > Threshold$ **then**
2: "RPS Fault warning"
3: "Run the IPISL algorithm to feed $\theta_{e,est}$ and $\omega_{e,est}$ to FOC"
4: "Use filtered I_{qRef} to the inputs of the current controller"
5: "Keep running until safe landing"
6: **else**
7: "continue running normally"
8: **end if**

In the case of a current sensor failure on phase A, knowing that the PMSM has an isolated neutral point and is in healthy operation, (3.1) can be used such that (4.18) is used whenever the fault is detected. A threshold based method can be performed just like that for the RPS to detect the fault. The threshold based is shown in algorithm 2. Once the threshold is detected, the root-mean-squared (RMS) of the current value will decrease to zero if the sensor is faulty and thus another threshold based method is used to identify the faulty current sensor. The fault is reported to the avionics to let the flight computer know there is a problem.

Algorithm 2 FMS for the FSO of an EVTOL while a single current sensor failure occurs.

if $mean(abs(i_a + i_b + i_c)) > threshold$ **then**
  "Current sensor fault warning"
  if $RMS(i_a) < PreviousRMS(i_a)$ **then**
    "Current sensor fault on phase A"
  else if $RMS(i_b) < PreviousRMS(i_b)$ **then**
    "Current sensor fault on phase B"
  else if $RMS(i_c) < PreviousRMS(i_c)$ **then**
    "Current sensor fault on phase C"
  end if
else
  "continue running"
end if

Where the $PreviousRMS(i_x)$ is the previous RMS value of the phase currents once the sum of the currents have exceeded the threshold value. Once the faulty sensor is known, (4.18) is used to provide a signal to the faulty phase current to keep running effectively. If there are multiple faulty phase current sensors, then the EPU would need to shut down. In this FMS design, if the rotor is at a low speed, it would take longer to identify the faulty phase current sensor due to the fact that a reliable RMS calculation needs one complete cycle to compute the true RMS value. Due to this fact, this method is only used if the EPU is already operational at a known speed. In this case, since the rotor is at a constant speed during the cruising phase, this algorithm is suitable for this application.

$$i_a = -i_b - i_c \tag{4.18}$$

In the case of a voltage sensor failure, the algorithm 3 can be used to determine if a sensor is known to be faulty. The main idea behind this statement is that it is simple to implement as well as it assumes that if a proper control current I_q is measured, but the voltage is way under the specified limit, a sensor fault is detected. Thus the fault is reported to avionics.

Algorithm 3 FMS for FSO of an EVTOL while a loss of the VDC sensor.

1: **if** $((0.9 * i_{qref} < i_q < 1.1 * i_{qref})$ AND $VDC << 550VDC)$ **then**
2: "VDC sensor fault warning"
3: "continue running until safe landing"
4: **else**
5: continue running
6: **end if**

Furthermore, instead of using the feedback signal measured by the voltage sensor in the FOC algorithm, the PI controller is tuned around a DC voltage value from a maximum and minimum DC link voltage. This enables a known bandwidth and stability of the PI controller no matter if the voltage sensor is faulty or not. This in-turn reduces efforts for the V&V activities for certification [136].

4.3.2 Controller stage failure mitigation strategies

In terms of having a main power supply failure, where the 28V of the control board is lost, a very well known technique used is by having a hold-up capacitor bank. This

is mentioned in the environmental guidelines document DO-160 [137]. By being able to hold the 28V for a minimum period of time, the controller itself can finish the task at hand while landing the aircraft safely or continuing the flight while reporting the fault to avionics such that an appropriate action can be performed by the flight control computer (FCC).

For any SEU, many well known techniques to avoid this failure mode consists of having radiation hardened controller chips such as a Anti-fuse or Flash based technology in terms of controller chips [138]. For example, an FPGA such as the A3P1000 from Microchip [138], has dedicated static random-access memory (SRAM) as part of the FPGA architecture and its use can be confined to buffering the input data to minimize the probability of SEUs occurring. The FPGA compensates for SEUs occurring within SRAM by updating the input data regularly for each operation before using the sampled data.

4.3.3 Gate Driver failure mitigation strategies

The FMS used if a gate driver failure occurs are comprised in the MOSFET fail short or Open sections. If the power supply to the gate driver does not operate properly, an under voltage lockout (UVLO) would occur and thus safely turn off the gate driver and set the switch to remain open at all times. A fault for the gate driver would then be relayed back to the avionics to ensure that an appropriate action can be done.

4.3.4 Communication Loss Fail Safe Operation Strategy

If a communication loss failure occurs on the controller side, a feedback loop is used to mitigate improper data transfer to the FCC where the controller itself would shut

down the EPU. Since there is a link of communication from the SSPC to the EPU, if the EPU is shutdown, communication would be relayed back from the SSPC to the FCC to ensure that the FCC would be able to do its own FMS.

Chapter 5

Verification of FMS for Critical Electrical Faults in EVTOL EPU

The FTC and FMS for the critical failure modes of the EVTOL EPU must be verified. The behavior of the EPU consisting of current, torque, and speed variables of the EPU is analyzed between the pre-fault, post-fault and having the FTC or FMS applied. In this section, the methods developed in section 4 to protect the EVTOL's EPU from the faults described in section 3 are tested in both simulation and experimental results. Results are then discussed and analyzed.

5.1 Verification of FMS for Open Circuit Faults in EVTOL EPU

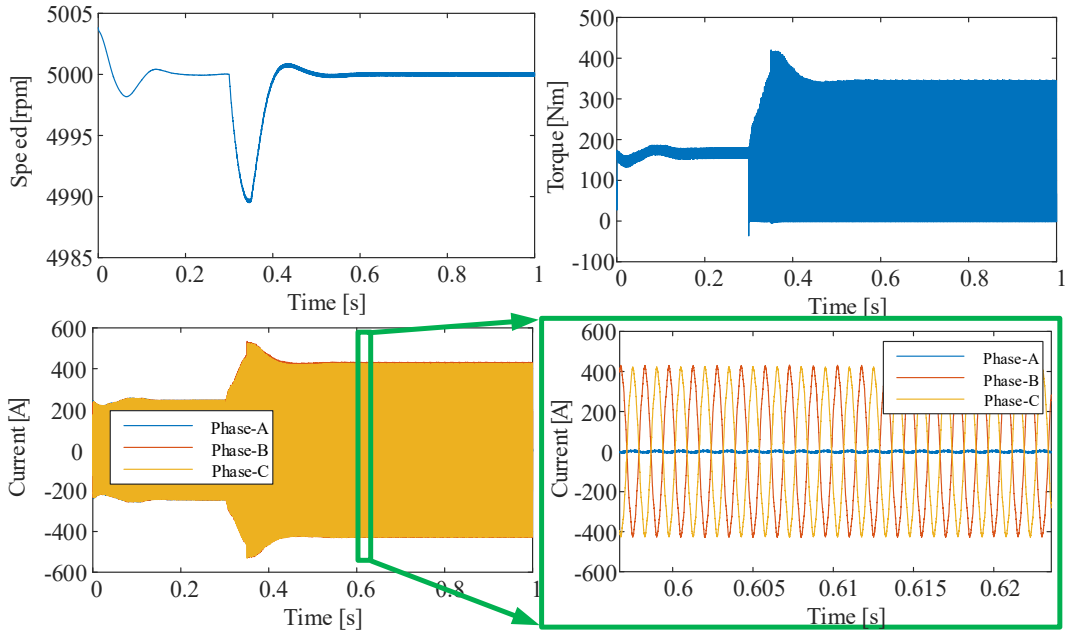


Figure 5.1: Open Phase fault simulation results.

The OPF FTC is analyzed and shown in Fig.5.1. Compared to pre-fault conditions, by applying the OPF FTC when the fault is detected, the torque ripple increases to 210.13% compared to 244.07% once the OPF occurs. This would ideally reduce the mechanical vibrations on the EVTOL which may let the EVTOL land safely during certain conditions. The resultant copper losses are very close, and as well the appropriate average torque is produced. This type of FTC for an OPF may be helpful if the final PMSM drive would fail, and thus a quick landing can be achieved. Furthermore, the SW or FW used for implementing this FMS uses the same feedback signals and

architecture just with a different reference current. This reduces verification efforts in terms of having different and adaptive SW or FW [136]. The major drawback would be to ensure that the EPU itself can withstand the thermal dissipation of the extra copper losses which could increase the weight of the EPU in total.

Table 5.1: Simulation results comparing healthy PMSM to post-OPF PMSM and enabling FTC to a post-OPF PMSM.

	Healthy	OPF	OPF with FTC
Post Fault Current (ARMS)	Ia = 168.5 Ib = 168.5 Ic = 168.5	Ia = 3.97 Ib = 290.68 Ic = 288.31	Ia = 3.87 Ib = 292.6 Ic = 289.8
Copper Losses (kW)	1.28	2.58	2.61
Copper Loss Increase (%)	0	101.56	104.1
Average Torque (Nm)	166.3	165.57	165.98
Torque Ripple (%)	14.53	244.07	210.13

5.2 Verification of FMS for Short Circuit Faults in EVTOL EPU

5.2.1 FTC1 for P2PSCF

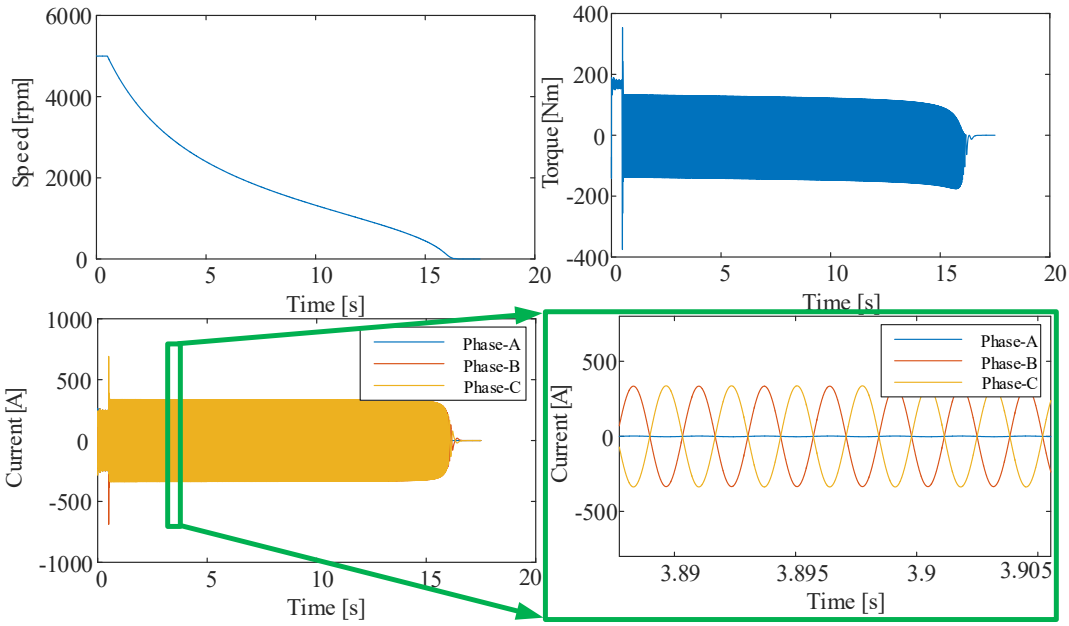


Figure 5.2: PMSM P2PSCF first mitigation technique (FTC1) simulation results.

FTC1 disables the inverter and thus removes the short circuit from the EPU power source and bus. Once the short circuit is detected, a large torque ripple is seen at the rotor of 2280.3%, while a 21.23% copper loss increase is seen. If the eVTOL can sustain high vibrations from the torque ripple, this FTC1 would be acceptable since the copper losses are minimized. As can be seen, the speed reaches zero within 15 seconds. To ensure this method is properly implemented, the oppsite EPU on the EVTOL would need to be turned off to ensure that the EVTOL does not start to

turn on its own axis. Another method would be to have a redundant EPU with lower performance such that the second EPU would be turned on to ensure the landing can be done safely.

Table 5.2: Simulation results comparing healthy PMSM to post-P2PSCF PMSM and enabling FTC1 to a post-P2PSCF PMSM.

	Healthy	P2PSCF	P2PSCF with FTC1
Post Fault Current (ARMS)	Ia = 168.5 Ib = 168.5 Ic = 168.5	Ia = 350.60 Ib = 49.98 Ic = 303.50	Ia = 1.2 Ib = 223.9 Ic = 224.9
Copper Losses (kW)	1.28	3.35	1.55
Copper Loss Increase (%)	0	161.72	21.23
Average Torque (Nm)	166.3	181.25	-13.5
Torque Ripple (%)	14.53	232.13	2280.3

5.2.2 FTC2 for P2PSCF

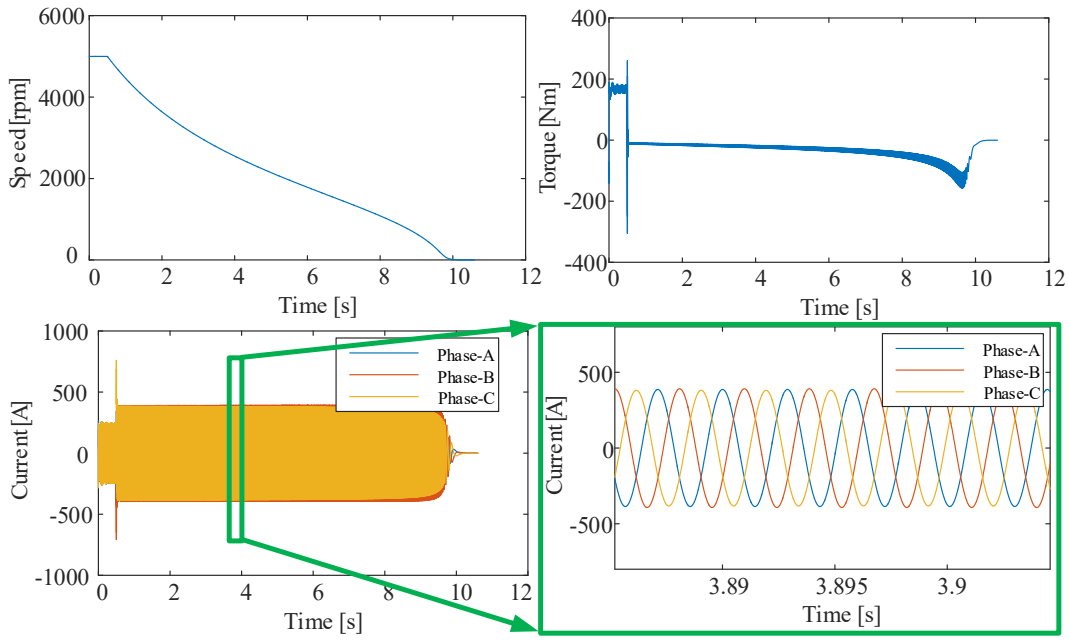


Figure 5.3: PMSM P2PSCF second mitigation technique (FTC2) simulation results.

For FTC2, a much greater copper increase of 140.3% was seen but had a much lower torque ripple of 40.23%. This method would be beneficial if lower vibration levels are needed during fail-operational applications. These results are very much similar to the FTC1 results but as can be seen, the speed reaches the zero speed within 10 seconds compared to 15 seconds.

Table 5.3: Simulation results comparing healthy PMSM to post-P2PSCF PMSM and enabling FTC2 to a post-P2PSCF PMSM.

	Healthy	P2PSCF	P2PSCF with FTC2
Post Fault Current (ARMS)	Ia = 168.5 Ib = 168.5 Ic = 168.5	Ia = 350.60 Ib = 49.98 Ic = 303.50	Ia = 256.5 Ib = 263.9 Ic = 253.3
Copper Losses (kW)	1.28	3.35	3.07
Copper Loss Increase (%)	0	161.72	140.2
Average Torque (Nm)	166.3	181.25	-32.98
Torque Ripple (%)	14.53	232.13	40.23

Between both FTC1 and FTC2, different conditions are to be considered. For FTC1, higher torque ripple are present on the rotor shaft which could make landing tough for a pilot as the EVTOL would vibrate much more. Although this torque increase may not be beneficial, the copper losses are half of what FTC2 provides which makes the inverter thermal dissipation design much easier. FTC2 could make the speed reach zero much quicker and reduce the torque ripple which could make the landing much easier for the pilot, but copper losses are doubled due to this fact. Thus a trade-off between torque ripple and copper losses are needed to be chosen between these two applications.

5.2.3 FMS for ITSCF

The main goal of the fault tolerant control is to minimize power losses and to avoid catastrophic failure of the EPU PMSM. The results shown in Fig.5.4 show the RMS value of the fault currents. By creating a virtual point using the inverter bottom switches has shown to be the most promising method as it isolates the fault and reduces power losses rather than not acting on the fault.

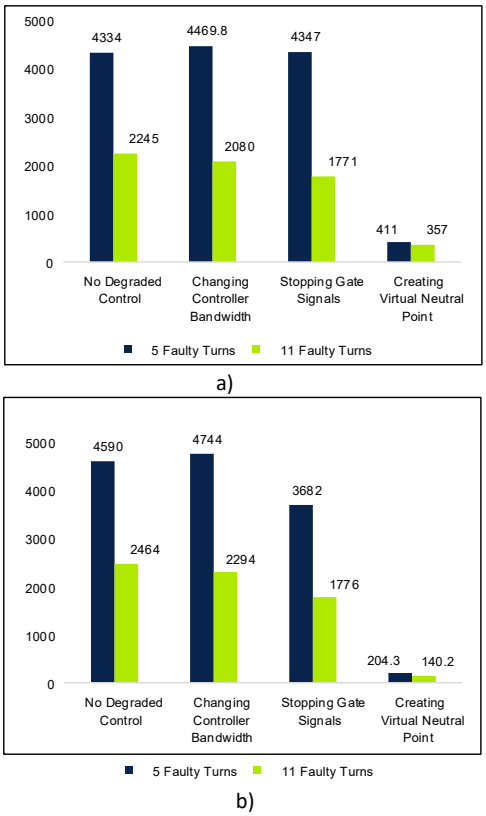


Figure 5.4: Simulation results for FMS of ITSCF: a) RMS current of I_f in phase A b) RMS current of I_af in phase A.

Although creating a virtual neutral point does produce minimized copper losses

and torque ripple, it may inhibit the ability to land safely in certain cases. Just like the FTC1 and FTC2 problem, choosing the different types of FTCs for the ITSCF based on the situation could be beneficial. By incorporating the PI controller with double the bandwidth, this would require larger V&V efforts but could save lives in certain conditions where the aircraft must land smoothly. If the number of faulty turns is higher, than the changing of controller bandwidth could be a viable solution to ensure the speed is maintained ot land safely. If the number of turns in smaller, then if it can be detected, the EVTOL could then use FTC2 to then ensure the fault does not degrade more. Once the ITSCf becomes at 100% than a P2PSCF occurs and thus FTC1 or FTC2 must be used to reduce further damage of the EVTOL EDS.

5.2.4 FMS using the SSPC

As mentioned in section 4.2.4, the SSPC is used as the main protection device in any case of the EPU failing. The SSPC can see the current and voltage footprints of the EPU attached to the EDS of the EVTOL. The final designed and manufactured SSPC with a 3D enclosure is shown in 5.5. The final configuration of the SSPC would consist of having 3 series strings of SSPCs and having two strings in parallel to each other to achieve a 800V/360A protections. To obtain a greater current or voltage for any other EVTOL platforms, this configuration can be changed. 360A for one EPU in the EVTOL should be enough to handle large current demands while remaining in a safe operating condition.

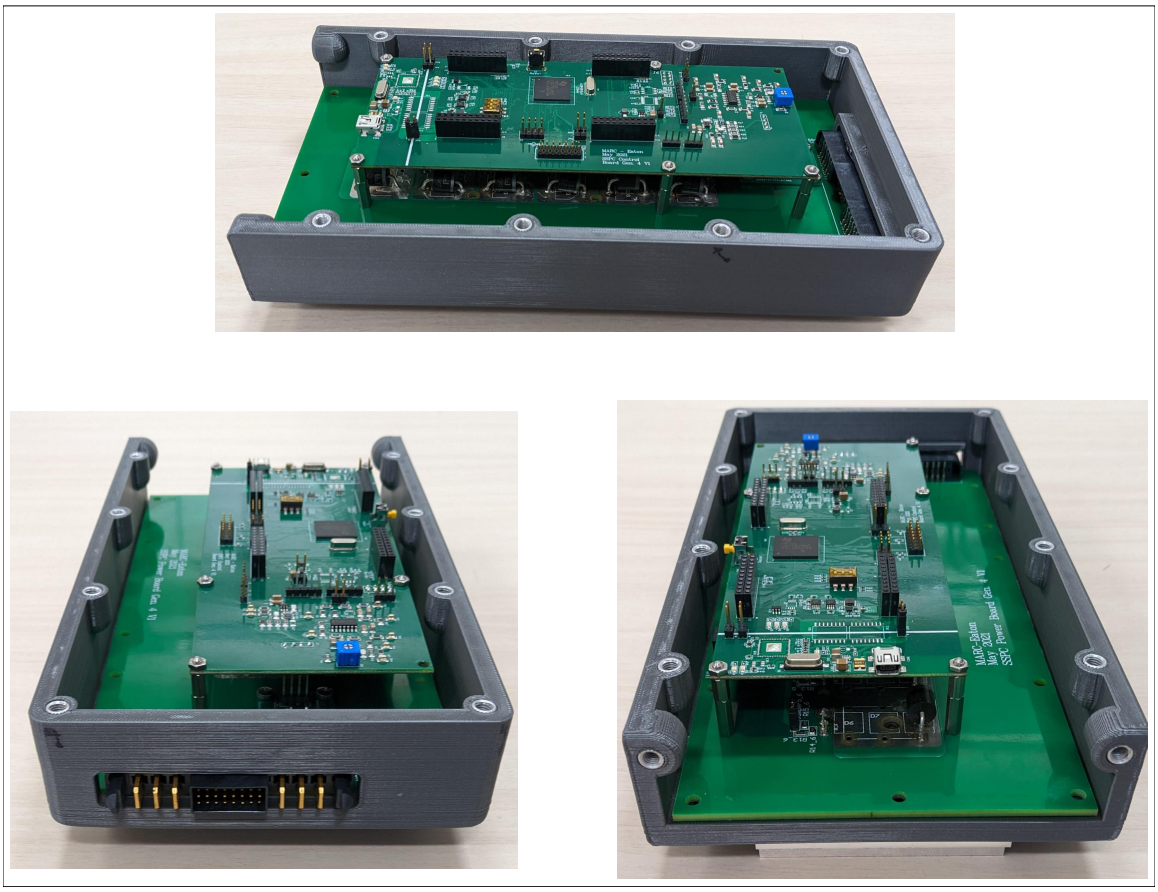


Figure 5.5: Assembled SSPC Board stack with 3D printed enclosure.

The SSPC is used as the main protection circuit for the rest of the EVTOL EDS from an EPU short circuit or over-voltage. To ensure that the SSPC handle the short circuit currents of greater than 180A (per SSPC strings), a testbench must be used that can generate such pulses of high current. The testbench used to test the SSPC platform is shown in Fig.5.6. The testbench consists of a high voltage power supply capable of delivering 20kW. Furthermore, this high voltage power supply is connected to a capacitor bank which is charged at the necessary voltage of 270VDC. A second power supply is used to provide the necessary continuous current of 180A

to the SSPC. This second supply would be helpful to test I^2T algorithms. The load consists of mainly a load inductor and a resistor to ensure the short circuit current is controlled.

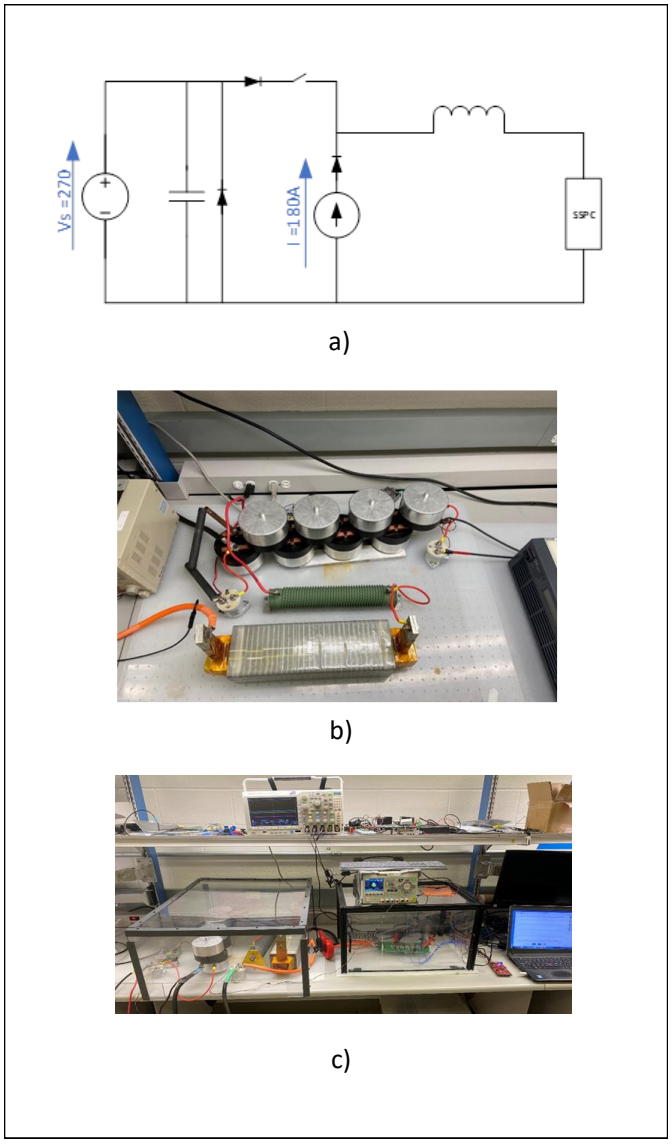


Figure 5.6: Experimental testbench for SSPC Pulse testing. a) Block diagram for pulse Generator and continuous testing setup b) Components used for pulse generator and RL load. c) SSPC connected to pulse generator

There are mainly two types of testing for the SSPC, one consisting of the pulse test, and the other consists of a continuous current test. The pulse test helps to test the SSPC under large current and high voltage for short duration while the continuous test helps to determine the steady state temperature of the SSPC. The voltage measurements are done with a high voltage differential probe while the current is measured with a rogowski coil.

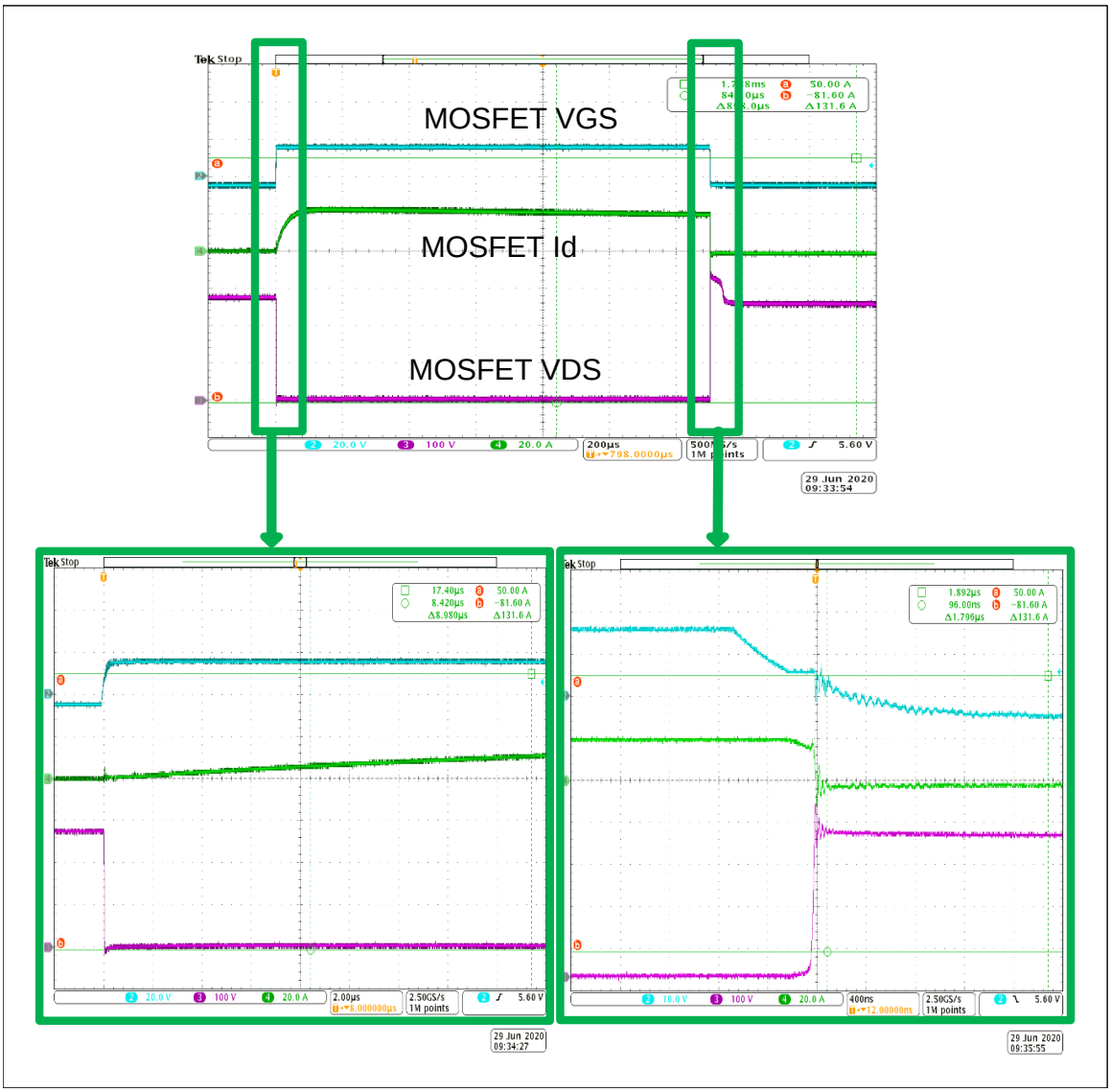


Figure 5.7: Experimental result of SSPC turn on and turn off characteristics at 270VDC and 27A.

At first, low power is applied to the SSPC to ensure it is functional and this is shown in Fig.5.7. The load resistance is set to 10Ω to ensure a current of 27A is achieved. The SSPC turns on properly with appropriate VGS voltage of 15V, the

SSPC current is remained at 23A and the voltage is set to 270VDC. The reason of the lower current is due to the added resistance of the cables used to connect the load components as well as the internal resistance of the inductive load which was calculated to be a total of 0.8Ω. There is also an internal error of 2A on the Rogowski coil which explains the difference in current measured. Once the SSPC turns off, the TVS starts to conduct to provide a path for the inductor to discharge and the TVS ensures that the voltage stay within its clamping voltage of 344V.

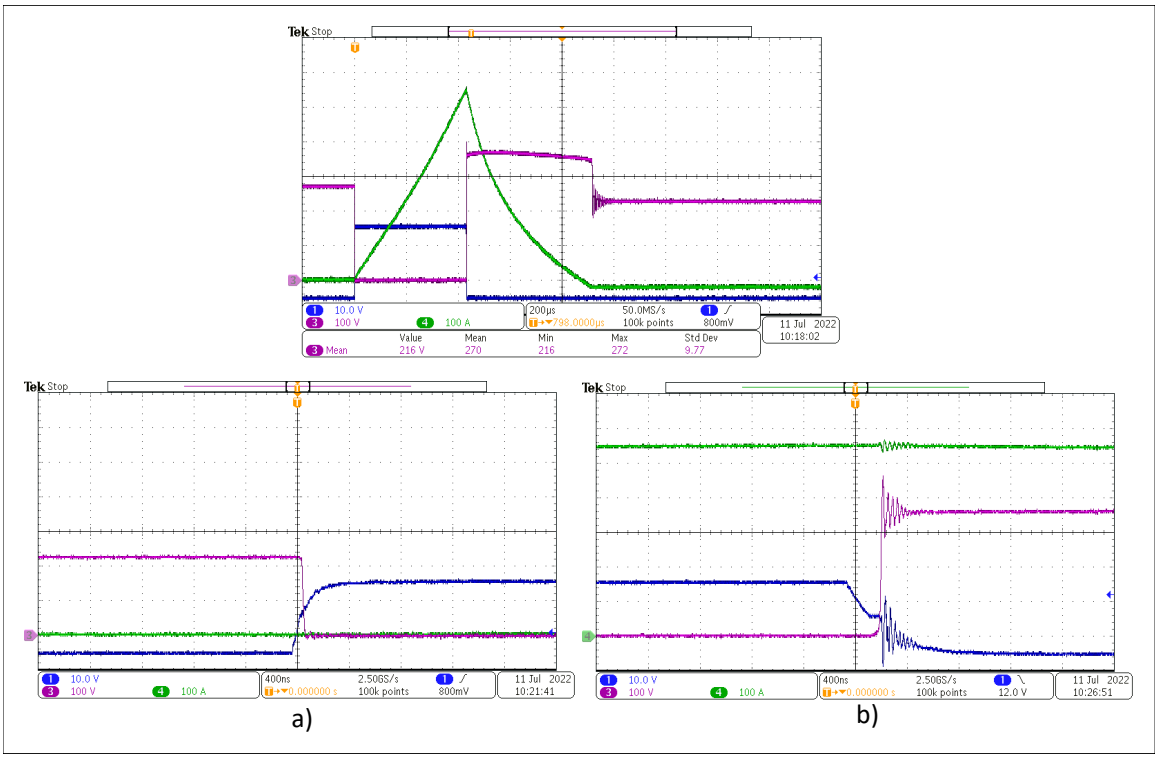


Figure 5.8: Experimental result of SSPC turn on and turn off characteristics at fault current of 540A and 270VDC bus. a) turn on b) turn off

Now that the SSPc is tested with a low power, a higher fault current is provided by setting a total circuit resistance of 0.5Ω. Cable lengths were reduced to achieve

this low resistance. The results are shown in Fig.5.8. A pulse of $213\mu s$ was used to ensure the SSPC turns off at 540A to see if the TVS can withstand the turn off of a $156\mu s$ inductive load which is close to the value of the motor phase. 540A is a larger current than the 400A maximum seen in section 3 which means that if the SSPc can protect against that fault current, it can protect against the 400A current. As can be seen, when the SSPC turns off at 540A, the TVS conducts the current and clamps the voltage at 344V until the current reaches zero after $300\mu s$. The current waveform is not triangular due to the fact that a rogowski coil is used. During turn off, it can be seen that the VGS oscillates a bit but it is only measurement noise and not part of the actual circuit. This type of turn off was performed more than 400 times for over 2 years and the SSPC has still survived after these number of tests.

In terms of propagation delay, the measurements are shown in Fig.5.9. Fig.5.9-a shows the results of the instantaneous tripping capability of the SSPC with a set tripping point of 400A. As can be seen, the delay from the measurement of the current to the latching signal turning on is $8.76\mu s$. The noise seen in the zoomed version of the waveform consist of measurement noise and is not actually present in the circuit. This is due to the fact that a passive probe is used to measured the lower voltage signals instead of a differential probe. This signal is isolated from the high power sources so it is fine using that type of probe. Ideally, a low voltage differential probe should be used to measure these types of signals in such noisy environments where large $\frac{di}{dt}$ and $\frac{dv}{dt}$ are present.

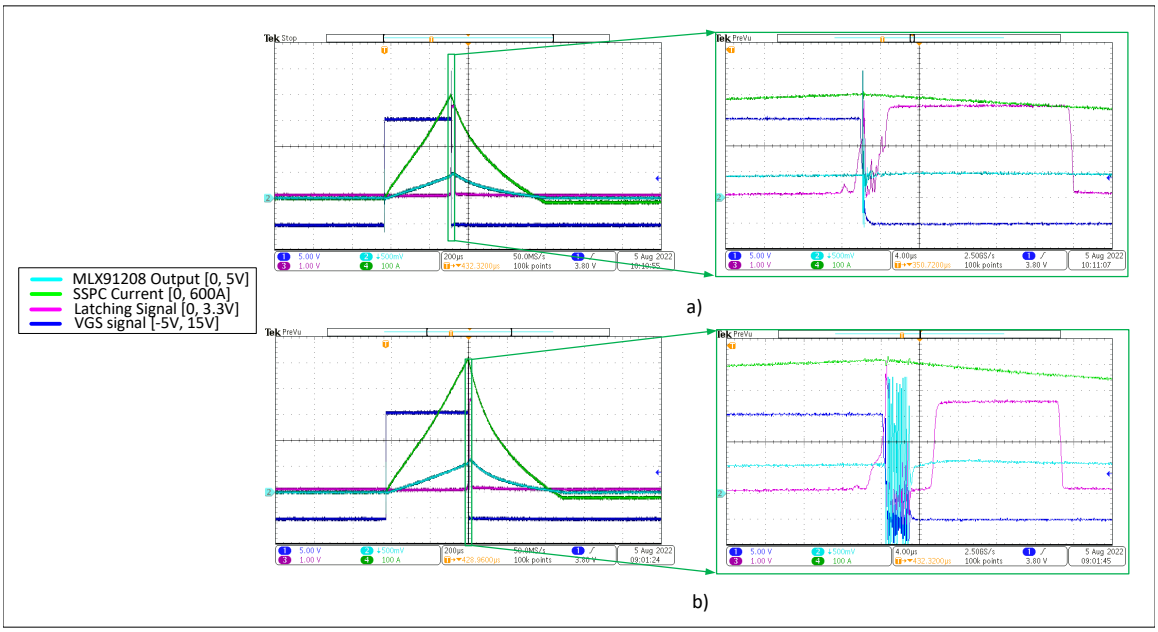
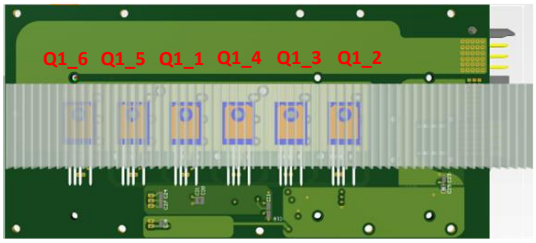


Figure 5.9: Experimental result for the propagation delay of the SSPC during different fault condition. a) with threshold equivalent to 400A b) with threshold equivalent to 540A.

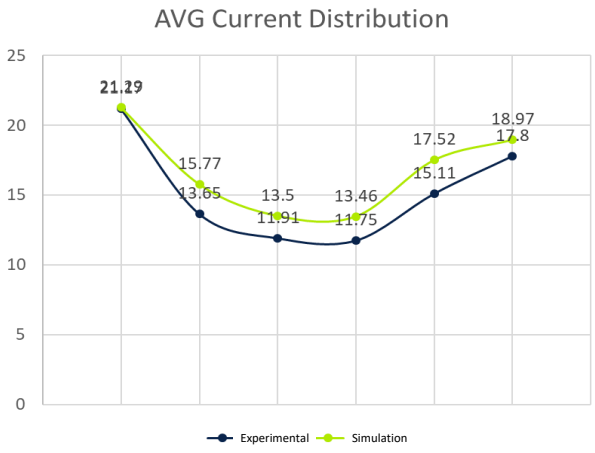
With the threshold set to 540A, the propagation delay seemed to be a bit higher being a value of $9.56\mu s$ from Fig.5.9-b. This is a bit more than the anticipated propagation delay and the errors may be due to the measurement noise due to the large $\frac{dv}{dt}$ and $\frac{di}{dt}$ that are caused by the SSPC turning off such a high current at 270VDC. Furthermore, delay could be reduced as well by improving the circuit with faster ICs. In both cases, the requirement for the propagation delay are met but this was performed in lab. Further analysis needs to be performed to ensure this SSPC works as intended in different atmospheric and temperature settings. Furthermore, a better design in shielding the CNTL board from the power board can be done to ensure a smooth turn on.



a)

MOSFET	AVG Id (A)	
	Experimental	Simulation
Q1_2	21.17	21.29
Q1_3	13.65	15.77
Q1_4	11.91	13.50
Q1_1	11.75	13.46
Q1_5	15.11	17.52
Q1_6	17.80	18.97
Total Current (A)	91.39	100.51

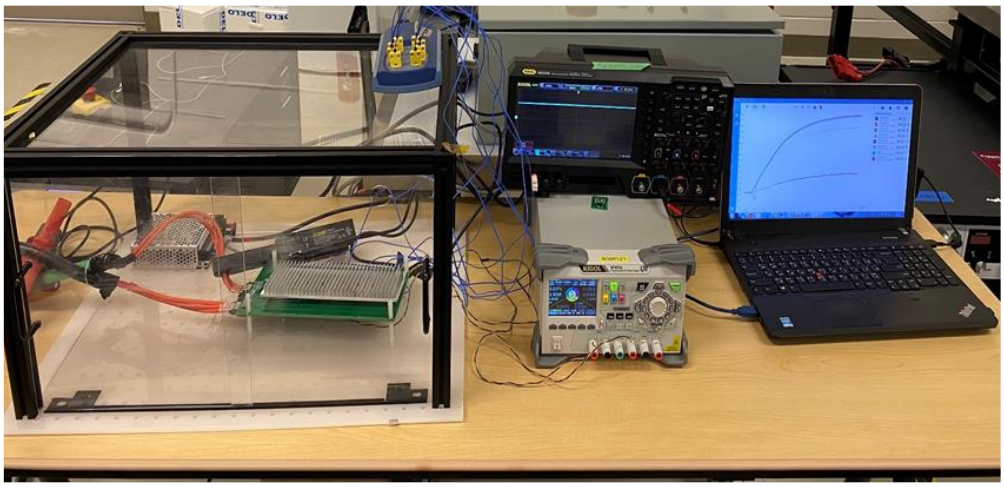
b)



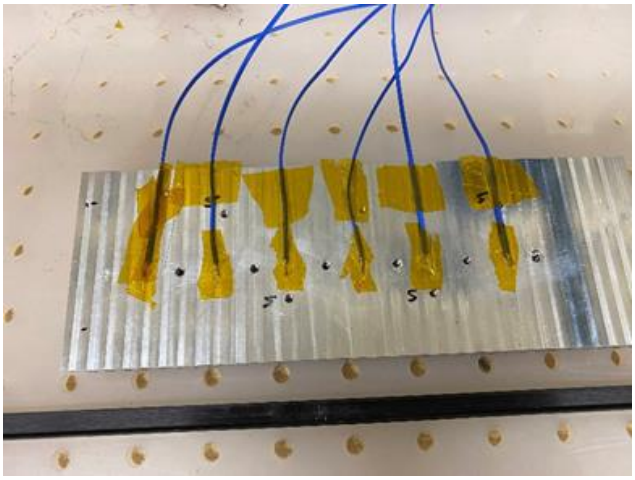
c)

Figure 5.10: Experimental result for the current distribution of the 6 parallel MOSFETs.

The next step is to see the current distribution between all six MOSFETs. Simulation results are compared with experimental results and are shown in Fig.5.10. The first and last SSPC have the larger currents due to the fact that they have less resistance between the bus compared to the middle MOSFETs which see the first and last MOSFETs resistance. This test was performed in transient tests. For steady state, the current distribution are within 10% of each other.



a)



b)

Figure 5.11: Experimental testbench for SSPC steady state temperature test. a) SSPC connected to current source and data acquisition b) Location of thermocouples for temperature data.

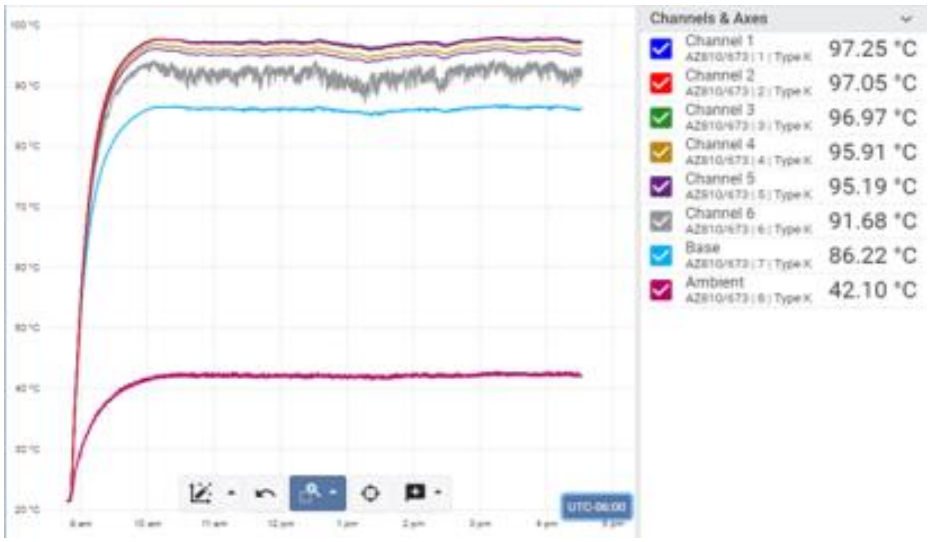


Figure 5.12: Experimental results of steady state temperature of SSPC at 120A.

To ensure the resistance of each MOSFETs are relatively close to each other, the temperature testing is the next step. The steady state temperature testbench is shown in Fig.5.12.In this test, a current source power supply is used to provide 120A to the SSPC to see its steady state temperature. The reason why 120A is used instead of 180A is due to a manufacturing error on the heat sink. K-type thermocouples are used to measure the temperature between the MOSFET and heat sink to see what steady stat temperature is reached. Thermocouples were also put to measure the ambient temperature of the box as well as the PCB temperature to see if the FR4 material of the PCB could handle the current. the results are shown in Fig.5.12.

Table 5.4: Pickup current and time values for I2T low power tests at 5A rated current.

	Desired Time(s)	Current (A)
Long Pick up	0.3	11.5
Short Pick up	0.02	23
Instantaneous Pick up	0.002	51.75

As the final test to verify the SSPC, the state machine of the SSPC needs to be experimentally verified. The same testbench as the pulse testing is used for this verification minus the inductor load, making the load completely resistive. To make sure the tests are safe in the lab and that the state machine works with appropriate SW and PCB stack assembly, the I^2T curve is altered with the parameters mentioned in Table 5.4.

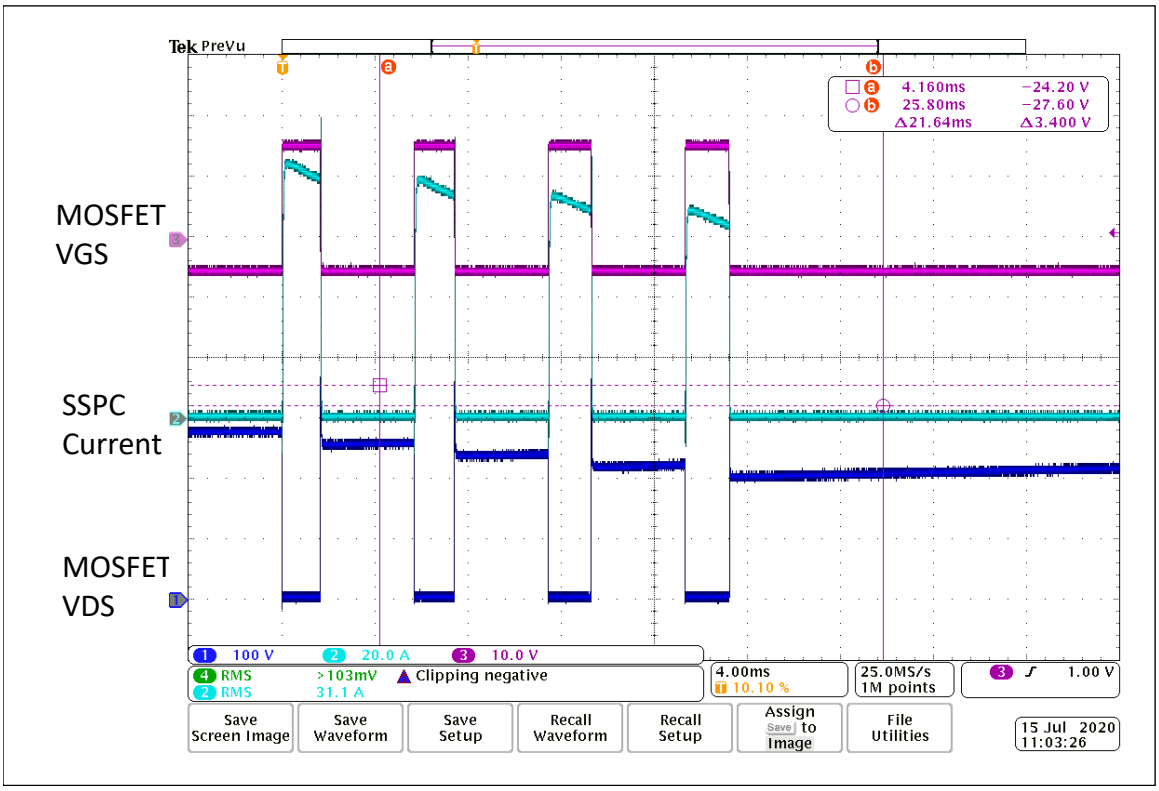


Figure 5.13: Experimental result of SSPC I2T SW. Lower current I2T curve is used to test I2T curve. Reset_Count = 4.

The voltage is set to 270VDC and the resistance is set to 2Ω such that 80A is the maximum short circuit current. The results are shown in Fig.5.13. The parameter of Reset_count is set to 4 just to make sure as well that the SSPC can withstand the state machine. As can be seen, since the current is higher than 51A, the SW turns off the SSPC after 1.8ms and waits until the current reaches zero with a delay of 6ms, turns the SSPC back on, and since the current is higher than 51A, the SW detects it, waits for 2ms and then turns the SSPC off again. This is repeated 2 more times until the SSPC latched in the off position until an external signal is seen by the SSPC from the FCC. The reason the value is 1.8ms and not 2ms is due to the fact that

the current kept increasing above 51.75A and so the SSPC needed to turn off quicker than the 2ms.

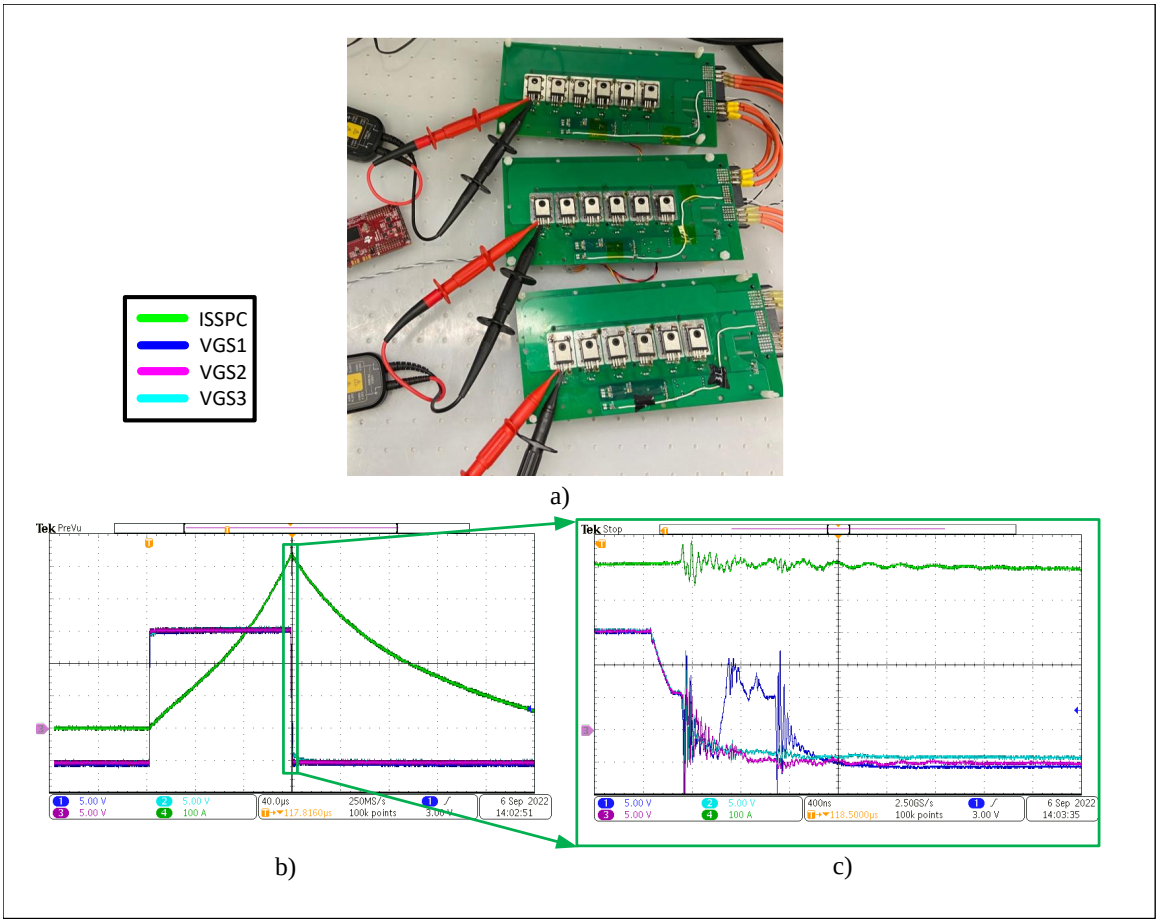
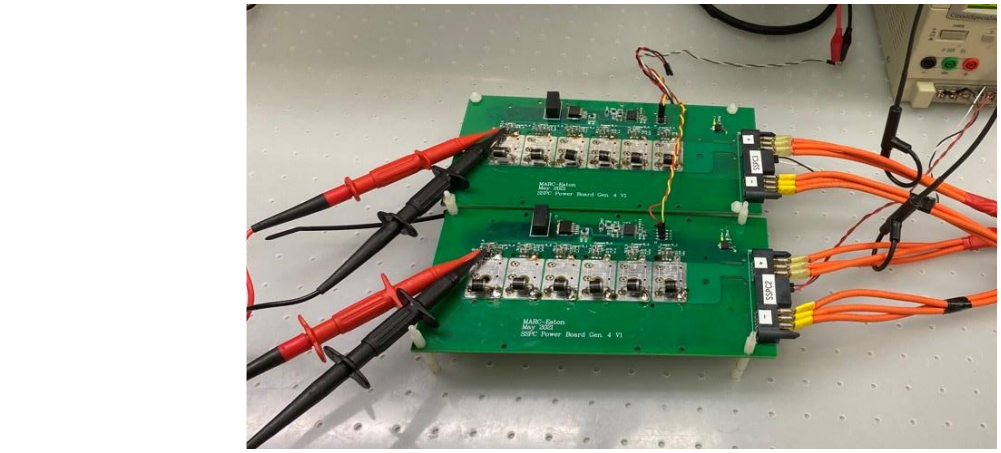


Figure 5.14: Experimental result of three SSPCs in series. a) experimental setup b) pulse testing at 810V and 540A fault current c) zoom of turn off of SSPC modules.

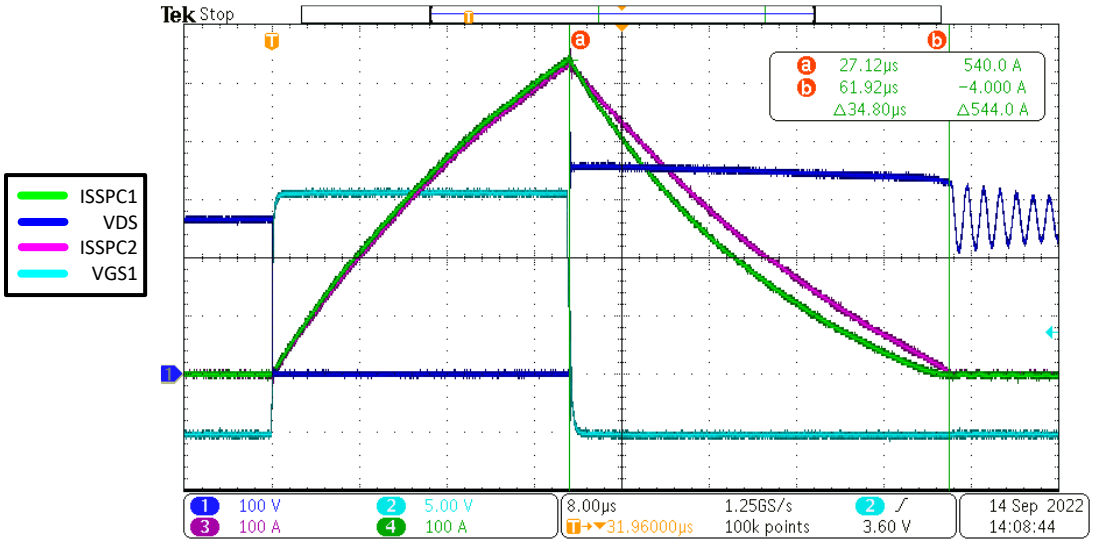
Now that the individual testing and characterization of the SSPC has been performed, three SSPCs were setup in series to achieve a nominal voltage of 810V/180A which would match that of the EPU of the EVTOL. A simple pulse testing at 810V and 540A fault current was performed. The experimental setup is shown in Fig.5.14-a and results are shown in Fig.5.14-b and Fig.5.14-c which has the same RL load as

the single SSPC. The SSPCs are controlled with just a single controller to ensure that all three SSPCs receive the same signal with minimal delay. As can be seen, only a single VGS signal (which is the SSPC connected to the positive HVDC bus) has a false tripping it seems from the measurement. This is believed to be due to a measurement noise which does not cause a problem since it can clearly be seen that the current of the SSPC modules turns off properly. Care must be taken to properly choose the SSPC components (MOSFETs and TVS diodes) to ensure proper current voltage sharing between each SSPCs connected in series which could be a daunting task.

Preliminary testing for the parallel configuration of the SSPC was also performed. This time, only a resistive load was used due to the current rating of the inductive load could only handle 600A and saturation of the inductive load was not wanted in this test. The experimental setup is shown in Fig.5.15-a and the resultant 270V with 1080A pulse current results are shown in Fig.5.15-b. Extra care was taken to make sure that the input cables were of equal lengths such that the turn on current were as close as possible. As can be seen, as the fault current is detected and the TVS diodes start to conduct, the TVS diodes properly clamp the voltage to close to 340V making sure all other components down the line to not suffer a larger voltage. Furthermore, it can be seen that the turn off currents are not equal and that is due to the fact that the TVS diodes and MOSFETs on the SSPCs were not bought at the same time and not from the same batch. As in the parallel case, extra care is needed to ensure an impedance match when serializing and parallelizing the SSPCs.



a)



b)

Figure 5.15: Experimental result of two SSPCs in parallel. a) experimental setup b) pulse testing at 270V and 1080A fault current

5.3 Verification of FMS for Controller Stage Faults in EVTOL EPU

5.3.1 FMS for Resolver failure

The goal of the FMS is to be stable for enough time such that the EVTOL can land safely. In these analysis, the RMS values, copper losses and torque ripple are calculated from after the load disturbance which is at 2.5 seconds until the end time of the simulation. This is to see that when a disturbance occurs, how well can the EPU come back to its original state or how badly does the system behaves.

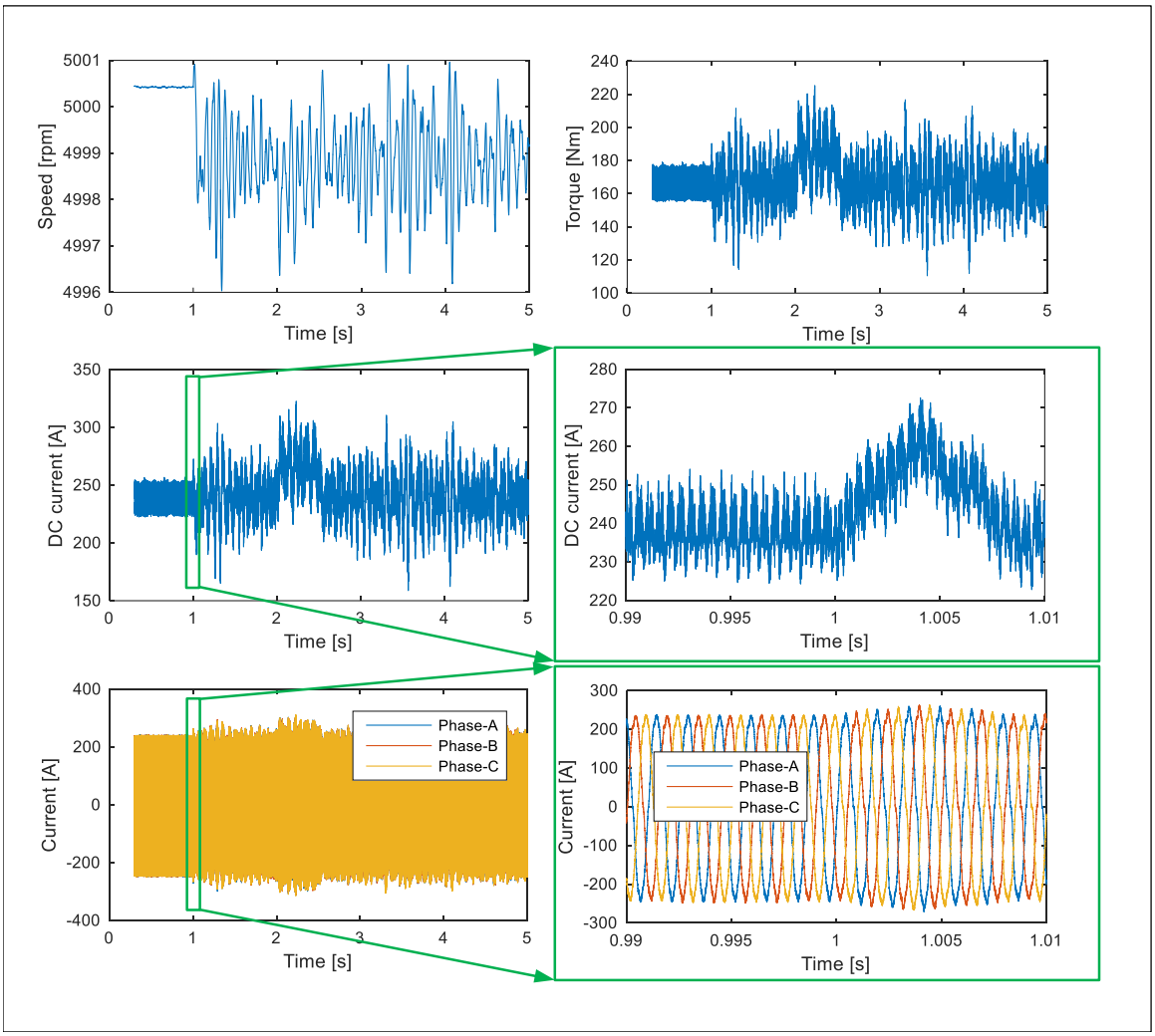


Figure 5.16: Simulation results of resolver supply fault occurring at 1s with Ksi = 0.01 and b = 1.01.

As shown previously in section 3, the RPS supply fault could be detrimental to the overall EVTOL if not detected and protected. By using the IPISL mentioned in section 4, the results are shown in Fig.5.16. By using he values of $b = 1.01$ and $Ksi = 0.01$, the estimation algorithm results seem promising. As shown in Table 5.5, the resultant RMS current values are just 1A more than the healthy case while

the copper losses have increased by about 1%. The torque ripple has increased to 64.03% but the average torque remains as in the healthy case of 166Nm. This will give enough time for the pilot to land the EVTOL safely with the appropriate speed albeit the extra mechanical vibrations caused by the fault.

Table 5.5: Simulation results comparing healthy PMSM to post-RPS Supply fault and enabling FSM.

	Healthy	Supply fault	With IPISL
Post Fault Current (ARMS)	Ia = 168.3 Ib = 168.3 Ic = 168.3	Ia = 195.2 Ib = 195.2 Ic = 195.2	Ia = 169.1 Ib = 169.1 Ic = 169.1
Copper Losses (kW)	1.31	1.76	1.32
Copper Loss Increase (%)	0	34.47	0.956
Average Torque (Nm)	166.3	-9.824	166.0
Torque Ripple (%)	14.84	5875	64.03

It can also be seen that if a turbulence wind would cause a load disturbance, the IPISL would still be stable and provide the necessary average torque and speed despite the load disturbance. This is exceptionally useful as this will help the pilot land the EVTOL safely with and without the load disturbance. Further tunning of the IPISL or controllers can be done when the EVTOL would be in different conditions.

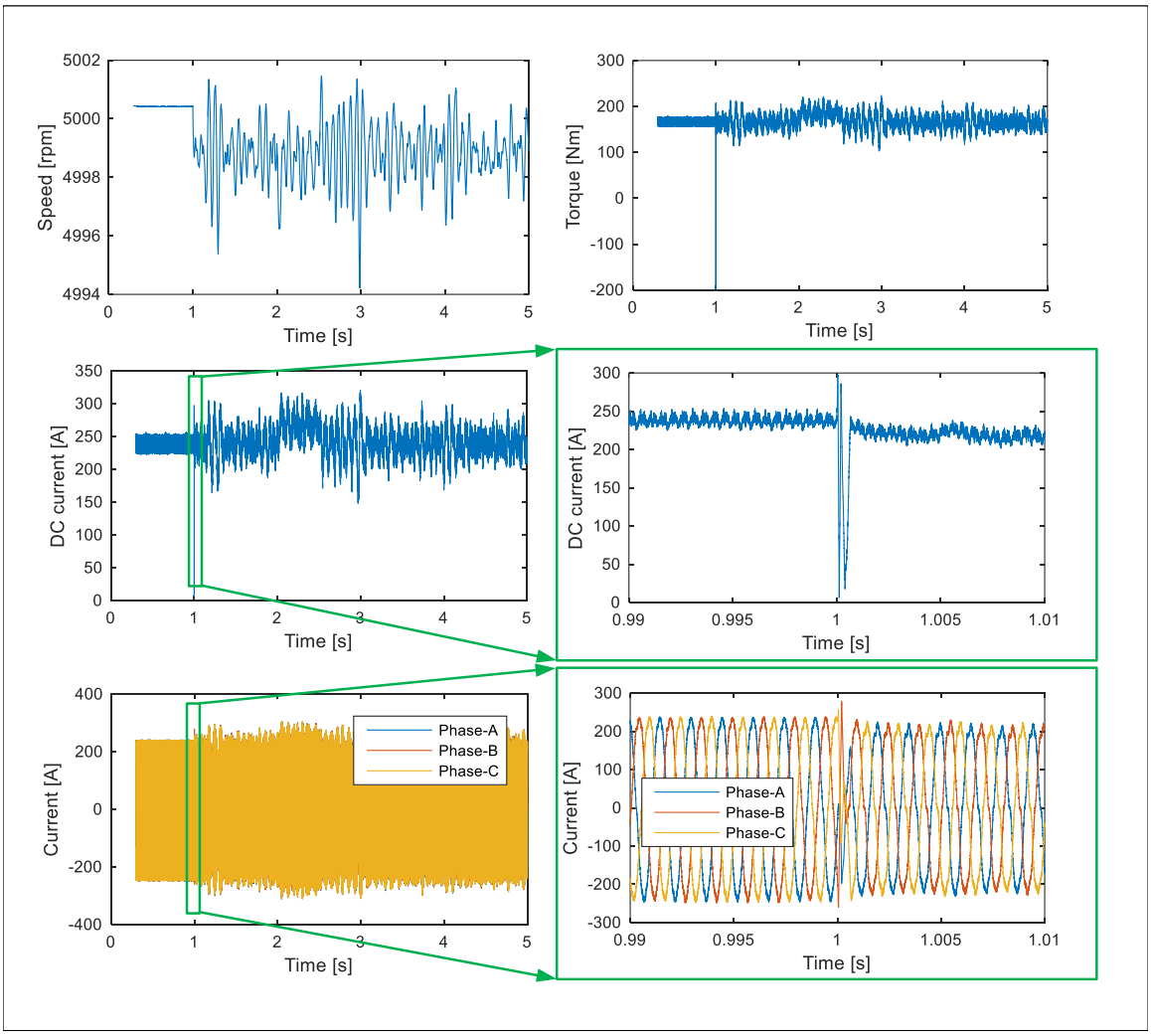


Figure 5.17: Simulation results of resolver Offset fault occurring at 1s with Ksi = 0.01 and b = 1.01.

In the case of the RPS offset fault, the results are shown in Fig.5.17. As can be seen, it has a very similar behavior as the power supply fault but with a small dip in torque whenever the fault occurs. This was present when the IPISL was not implemented. To be able to remove this behavior, a faster detection time would be needed which would be a daunting task. Nonetheless, this small dip in current occurs

only on the inverter side, so it will be filtered by the DC link capacitors assuming they are still healthy. Furthermore, in the same case as the power supply failure, the speed and load torque are kept within the reference values and thus a safe landing can be achieved.

Table 5.6: Simulation results comparing healthy PMSM to post-RPS offset fault and enabling FSM.

	Healthy	Offset fault	With IPISL
Post Fault Current (ARMS)	Ia = 168.5 Ib = 168.5 Ic = 168.5	Ia = 254.7 Ib = 231.1 Ic = 212.4	Ia = 169.2 Ib = 169.3 Ic = 169.2
Copper Losses (kW)	1.31	2.52	1.32
Copper Loss Increase (%)	0	92.31	1.09
Average Torque (Nm)	166.3	105.09	165.9
Torque Ripple (%)	14.53	512.3	73.12

In this method and shown in Table 5.6, the RMS value of the phase currents are very similar then the healthy operation just with 1.1A increase which would increase the copper losses by 1% which is not a problem. The torque ripple has increased to 73.12% of its average value of 165.9 which is just below the necessary 166.3 but is not detrimental to the speed as the steady state speed seems to oscillate around 4999RPM. The IPISL under the RPS offset fault is stable under different load conditions in case of aload disturbance caused by wind or difference in pressure in the air.

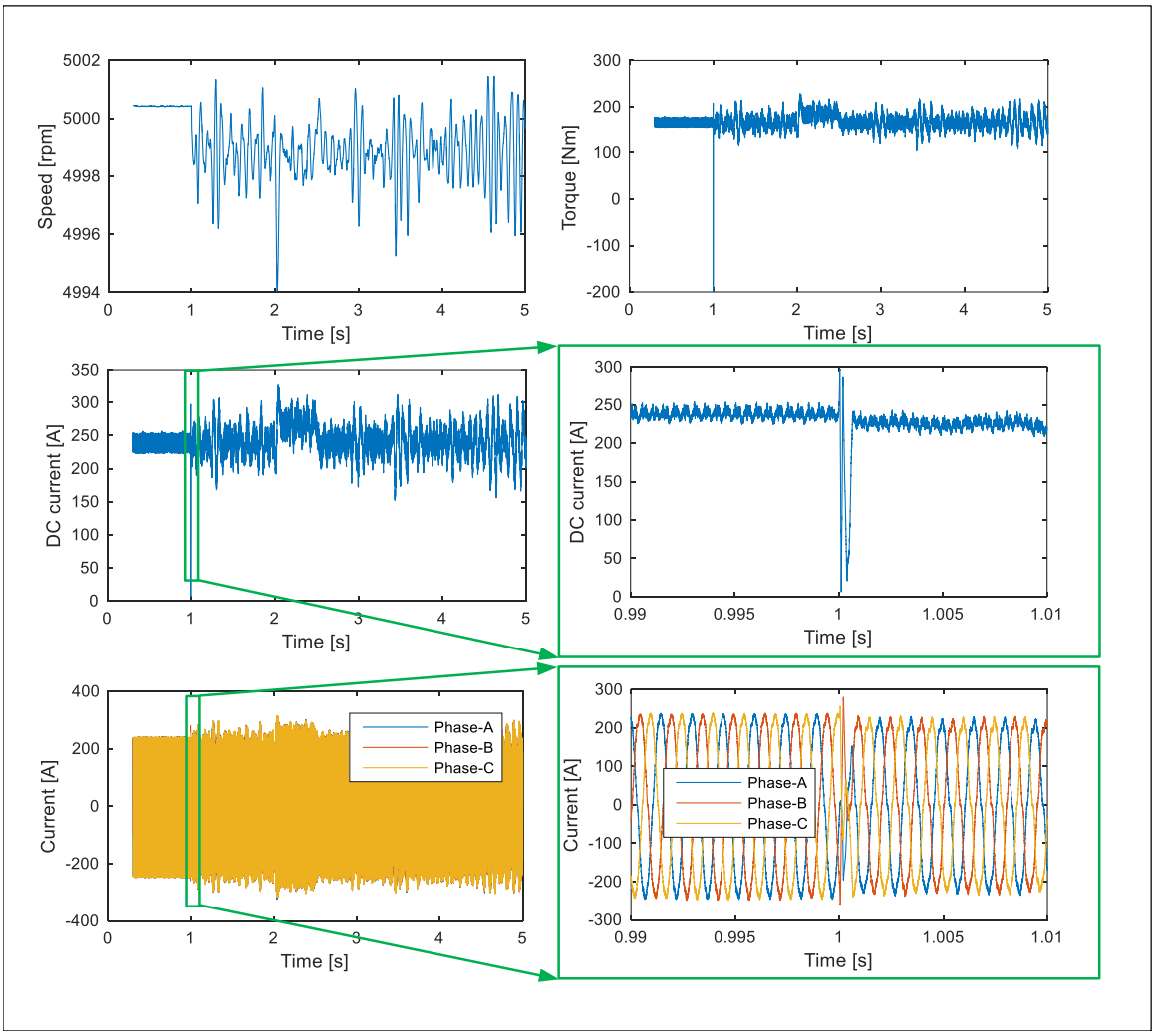


Figure 5.18: Simulation results of resolver Imbalance fault occurring at 1s with Ksi = 0.01 and b = 1.01.

Finally, the RPS imbalance fault with the IPISL applied to protect the EVTOL from the fault behaves very similar to the RPS offset fault FMS as shown in Fig.5.18. A very similar dip in torque and Dc current is seen when the fault occurs. This again may cause a hiccup in the flight of the EVTOL but the time frame is so small that the it would not cause instability in the flight of the EVTOL. As shown in Table

5.7. it can be seen that the same RMS phase currents are attained along with a very similar average torque which would enable safe landing due to the constant speed. The copper losses are as well increased by roughly 1% and that torque ripple is 68% of the average torque. This is a promising solution if the EPU is on its last leg and the EVTOL needs to be landed safely. The load disturbance is also properly controlled with the IPISL under the RPS imbalance fault.

Table 5.7: Simulation results comparing healthy PMSM to post-RPS imbalance fault and enabling FSM.

	Healthy	Imbalance fault	With IPISL
Post Fault Current (ARMS)	Ia = 168.5 Ib = 168.5 Ic = 168.5	Ia = 133.6 Ib = 185.7 Ic = 230.8	Ia = 169.3 Ib = 169.3 Ic = 169.3
Copper Losses (kW)	1.31	1.63	1.32
Copper Loss Increase (%)	0	24.26	1.19
Average Torque (Nm)	166.3	118.6	165.9
Torque Ripple (%)	14.53	415.2	68.02

The IPISL has demonstrated its effectiveness for all RPS faults. By using the same method of FMS for all RPS faults, the SW/FW would make it less efforts to perform V&V activities. Therefore, by knowing in which condition each EPU is in as well as the complete EVTOL aircraft, this method can be properly deployed and easily verified due to the use of one FMS for three different faults.

5.3.2 FMS for current sensor failure

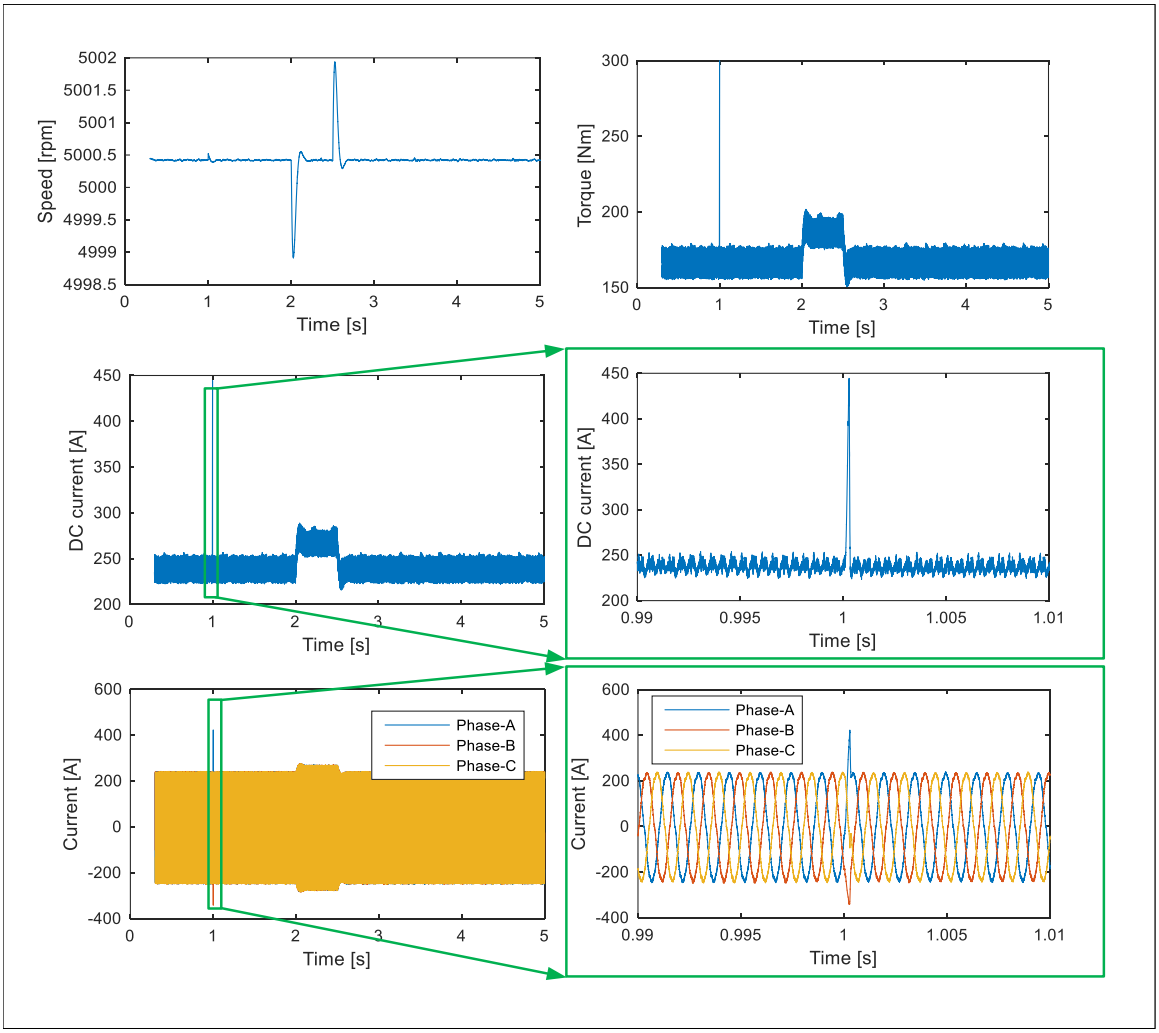


Figure 5.19: Simulation results for FTC of one single current sensor fault.

As shown in section 3, the loss of one current sensor failure can be properly managed by just the speed controller but with an increased copper loss of 20% and with an increased torque ripple of 115%. The one detrimental factor would be the increased DC current and its increased $\frac{di}{dt}$ which can cause further damage down stream on the EVTOL EDS. To ensure that this type of fault is segregated from the rest of the EDS,

the FMS developed in section 4 is implemented and simulation results are shown in Fig.5.19.

From Table 5.8, it can be seen that once the fault occurs and the FMS is used, the RMs phase currents drop back to 168.2A and the average torque produced is now 166Nm which is very close to the healthy operation. The copper losses are returned to their healthy case. The only different is that an increased torque ripple is found at 20% instead of 14%. This increase in torque ripple would not cause a big problem to enable continued cruising or to enable safe landing.

Table 5.8: Simulation results comparing healthy PMSM to post-current sensor fault and enabling FMS.

	Healthy	Current sensor fault	With FMS
Post Fault Current (ARMS)	Ia = 168.5 Ib = 168.5 Ic = 168.5	Ia = 242.8 Ib = 139.4 Ic = 153.8	Ia = 168.2 Ib = 168.2 Ic = 168.2
Copper Losses (kW)	1.31	1.57	1.31
Copper Loss Increase (%)	0	20.10	0
Average Torque (Nm)	166.3	166.0	166.0
Torque Ripple (%)	14.53	115.7	20.95

5.3.3 FMS for other control stage failures

The voltage sensor fault FMS is used in the control stage FOC of this thesis. A constant VDC is used to ensure minimal feedback signals are used to cause instability,

but the VDC is always monitored to ensure it is within reasonable bounds. If that is not the case, then the FMS provided in the previous section is triggered.

The FMS for the controller stage and communication loss are not tested in this thesis as they are just system level suggestions and need further experiments especially for SEU.

Chapter 6

Conclusions and Future Work

6.1 Conclusion

This thesis presents the main electrical challenges in designing an EPU in the new market segment of EVTOLs. Although electrical faults occurring in the industrial sector are well known, no well defined studies have presented such faults on an EVTOL platform. Within the new market segment of EVTOL, four categories of EVTOL were introduce such as the Helicopter, Multi-rotor, Lift & Thrust and the Tilt-X architectures. Due to the fast time to market of these EVTOLs that their manufacturers need, it was found that the Lift &Thrust seems to be the most viable option for main aircraft manufacturers to reach type certification by 2024.

The critical electrical faults that can occur for a typical EPU in an EVTOL are analyzed and presented both at their component level as well as the system level. The presented electrical faults include the category of open circuit faults, short circuit faults and controller stage faults. Focus of the effect of the fault is limited to the EPU as well as the main HVDC bus of 800VDC which supplies the main power for the

EPU. Some of these faults are destructive and can cause catastrophic behaviors as soon as they happen such as the short circuit current faults that can occur between motor phases or on the input of the inverter or HVDC bus. Open phase faults were found to be detrimental to the system due to the increased mechanical vibrations that could occur on the EVTOL. Controller stage faults were found to be detrimental after a certain time after the fault occurs. The behavior of these faults are compared to the baseline of a healthy EPU during cruise and during a load disturbance which emulates the turbulence effects of an EVTOL in flight.

Once the faults occur, a FMS is developed such that the EVTOL can land safely causing no harm to cities below the EVTOL flying or anyone in the EVTOL. Detection methods for open circuit, short circuit and control stage faults based on RPS, current sensor and voltage sensor signals for a typical EPU are presented. Once the faults are detected within a reasonable time, the protection methods are introduced. The protection methods for open circuit faults include a simple FTC which enable the EPU to function for a short time such that the EVTOL can safely land. The fault tolerant control simply alters the reference currents of I_d and I_q for the PMSM such that the same control algorithm is used which reduces control complexity and V&V efforts. In terms of short circuit faults in the EPU, mainly two types of FTC were introduced being disabling the inverter by opening all switches, or by creating a virtual neutral point with the bottom switches all turned on. It was found that a trade-off between torque ripple and copper losses had to be chosen. Extra copper losses would mean that the EPU thermal dissipation system would need to be designed to withstand it, while the extra torque ripple would need to be handled by the EPU as well.

For the RPS faults, a sensor-less control known as the IPISL is used. The IPISL

was used in three different types of RPS faults being the power supply fault, offset fault, and an imbalance fault in the feedback signals. It was shown that by detecting the fault by using a simple trigonometric relation of the feedback signals, that the IPISL could within a short time be used as the FMS to enable the EPU to function for a safe landing. The IPISL offers controlability for safe landing of the EVTOL for all RPS faults with similar results. In regards to the voltage sensor fault, a constant VDC value is used in the control stage but monitoring functions are added to ensure the control stage is aware a fault occurred. In regards to the current sensor faults, if only one current sensor is faulty, the algorithm uses the aspect that the EPU is balanced by knowing at least two healthy current sensor signals.

If the above FMS methods fail to protect the EPU during fault scenarios, the SSPC would be used as the redundant protection device. Especially for destructive faults such as the short circuit faults, power device or for more than one current sensor fault, an SSPC is added to the input of the EPU to protect the rest of the EVTOL components from being affected. The design of the SSPC including its power stage, control stage and sensing stage are discussed. A MOSFET is used to perform the switching action, a TVS is used for energy absorption, the MLX92108 is used for current sensing and a control algorithm comprising of an instantaneous analog logical latching to protect against high short circuits and an I^2T curve to protect on over current conditions. Simulation results and experimental results are shown for the FMS of the aforementioned electrical faults. Results showed that the SSPC is able to protect other EVTOL components within $9.56\mu s$ at a current of 540A. The SSPC was found to be a useful redundant protection device in the case the EPU cannot protect itself or if the EPU is in a fault condition that needs to be isolated from the rest of

the EVTOL EDS. Furthermore, the design of the SSPC was modular to ensure that different voltage and current ratings can be achieved in different EVTOL platforms.

6.2 Future Work

Although this thesis presents many test cases on critical electrical faults that can occur on the EPU of an EVTOL, it is not an exhaustive list of all possible failure modes that could occur in an EPU for an EVTOL, let alone an EVTOL as a whole. The ideas in this thesis could be expanded to include mechanical faults such as locked rotor, demagnetization of PMSM magnets due to over temperature as well as any type of communication error or avionic errors where low voltage electronics is no longer working. Furthermore, the main battery or power source may fail in some instances and this will cause different failure modes such that the EVTOL must land safely. For example, if for some reason all the battery packs fail, the batteries could be disconnected from the EDS of the EVTOL by using an SSPC and each EPU could somehow have a local source of power which would enable a harsh but safe landing.

More analysis needs to be performed for the serialization and parallelization of the SSPCs to increase the voltage and current level to make the SSPC compatible to protect different types of loads and sources. The voltage balancing and current balancing of the SSPCs can be further improved by choosing appropriate components with similar impedance. The development of the SSPC can be further improved by adding it in the EVTOL PDU and performing lab tests with different types of resistive, inductive, capacitive and more complex loads like a real EPU. The EPU can also be further tested by testing different electrical machines such as induction machines or switched reluctance machines (SRM) since SRM tend to be much more fault tolerant

than PMSM. Furthermore, arc fault detection and protection using SSPCs can be further investigated since that is a very likely fault to occur if a wire harness gets pinched due to the increasing voltage levels in EVTOL EDS.

Also, the SSPC's power density can be improved by creating an array of surface mounted TVS diodes instead of using the large TVS diodes in the current SSPC prototype. A bidirectional SSPC can also be created and analyzed with the same tests performed on the unidirectional SSPC but with additional tests concerning the bidirectional capabilities. The SSPC design can be further improved by investigating GaN devices, such as the vertical GaN technology for higher voltages. The GaN devices may help to reduce the propagation delay for higher power applications where $10\mu s$ is too long of a time. So further investigation can be done such that the propagation delay can be further reduced for high power applications.

In terms of the current sensor used in this application for the SSPC, the MLX91208, its behaviour can be investigated for different temperatures and not only in the lab environment since it is an open loop architecture. Furthermore, the aging of the SSPC SiC MOSFETs along with the TVS used can be studied further by testing the SSPC in a temperature room with appropriate high voltage and high current loads. This will ultimately show if the SSPC design is a true candidate for the aviation application as it must stand working for more than 20 years.

Another type of project which can be performed is the placement and coordination of SSPCs in an EVTOL EDS. This work would entail the placement of SSPCs in critical areas in the EVTOL EDS, such as the input of the EPU, output of battery packs (low and high voltages), and other loads where if a fault occurs on any components, the SSPC would be the redundant protection device such that the failure

is isolated as proposed in this thesis for the EPU. The coordination of each SSPC would then need to be handled with care where SSPCs need to be turned off and on based on the fault location and criticality.

The control methods could also be tuned such that if a fault occurs during take-off or landing, the effects can be mitigated. The real behavior of the FMS could also be studied by implementing it on a miniature EVTOL such as a drone or other platform to make sure the FMS works in all flight scenarios. This would help to understand the FMS behavior under a small scale EVTOL that could enable cheap V&V efforts and reduce risks when implementing these methods in a large EVTOL prototype. The detection methods for the ITSCF can also be improved and implemented onto a real controller that would be used in an EVTOL to see its feasibility and response time to such a fault. Predictive maintenance can be implemented to detect a start in ITSCF such that when the EVTOL lands next time through prognostic algorithms, the motor can be analyzed and possibly repaired if a fault is slowly being detected. This would help EVTOL maintenance to be less expensive and with minimal work.

Further analysis with a real EPU in lab could demonstrate and further prove the results of this thesis at an appropriate Dyno facility once the small scale drone experiments are validated. The dyno could be programmed with a specific flight profile (torque profile) that the EVTOL would exhibit and the methods described in this thesis could be tested on this dyno, HV setup. Data collection could be done directly on the dyno setup and then analyzed offline to verify if all requirements are met. This work could be expanded to not only meet the EVTOL industry but other larger aircrafts such as single-aisle aircrafts and large cargo aircrafts for future AEA.

To help type certification for equipment manufacturers and EVTOL air-framers,

an appropriate system level analysis using previously known standard ARP4754 [92] for airborne electronics or its EVTOL equivalent, to conduct a Failure Mode, Effects and Criticality Analysis (FMECA) to further document the ideas in this thesis and to enable an actual quantitative number to the reliability and probability of a fault occurring with a set architecture. This would also include the well-known environmental guidelines and standards DO-160, [137], which is needed to understand the environmental impacts on the EVTOL along with a specific flight profile in cities for commuting or rural areas for emergency purposes. This type of research could help develop the much needed standards and guidelines for EVTOL concepts discussed in this thesis.

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