MODELING AND SIMULATION OF GATE

LEAKAGE IN pGAN HEMTS

MODELING AND SIMULATION OF GATE LEAKAGE IN pGAN HEMTS

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A Thesis Submitted to the School of Graduate Studies in Partial Fulfillment of the Requirements

for the Degree Doctor of Philosophy

TITLE**:** Modeling and simulation of gate leakage in pGaN HEMTs

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NUMBER OF PAGES: 133

Abstract

Recently, gallium nitride high electron mobility transistor [GaN HEMT] has evolved as a promising device in the field of power electronics. It has excellent material qualities such as high bandgap, high saturation velocity, and good thermal stability which is expected to give superior device performances compared to its Si counterparts. One of the major challenges in GaN technology is to achieve enhancement operation (or normally off mode) due to the presence of its inherent two-dimensional electron gas[2DEG]. Among many methods developed to realize this, pGaN HEMT has emerged as the most encouraging technique for power GaN technology due to its high threshold voltage and good reliability. However, one of the major issues in pGaN HEMTs is that it suffers from high gate leakage current which limits their device performance. In this thesis, we have made a detailed study of the gate leakage process in pGaN HEMTs in terms of modeling, TCAD simulations, and alternative methods being used to reduce gate leakage in pGaN devices.

A numerical model has been developed to model the gate leakage in pGaN HEMTs as a function of gate bias and temperature. This model is validated against 5 devices with different contact metals, geometries, and process conditions. A single model with a consistent set of parameters can fit the experimental data for all these 5 devices without the need to invoke multiple mechanisms to explain the gate leakage process.

The numerical model relied on some simplifications, such as ignoring series resistance, using the compact diode model, and using a simplified expression to describe trap-assisted

tunneling. Using commercial TCAD simulations, can address these limitations since the simulator computes the electric field distribution throughout the structure. Furthermore, using TCAD some of the trap levels have been identified which accounts for leakage at low bias. We were able to calibrate our TCAD simulations against published data for the drain current and then used the calibrated simulation environment to accurately simulate gate leakage using parameters that closely correspond to the physical phenomena described, including interface trap parameters, which we identify with known trap levels in GaN.

Finally, we have examined different strategies that have been implemented so far to reduce leakage current. The pGaN layer is important in the whole device operation. Its doping concentration and thickness affect the leakage characteristics. Three modified structures have been studied through TCAD simulations which decrease gate leakage current. In each case, we used our calibrated TCAD model to study the impact on the drain current as well as the leakage current. Our results closely fit published experimental results and therefore provide confidence on the simulated dependence of leakage and drive current behavior on process modifications. The specific results, and our model overall, are expected to be of benefit to device designers in optimizing device structures for leakage while maintaining the required drive current.

Keywords: Gate Leakage, pGaN, HEMT, TCAD simulation, Tunneling

Acknowledgements

Firstly, I want to thank my doctoral advisor, Dr. Yaser M. Haddara for accepting me as his PhD student. His vision and depth of knowledge in academic as well as non-academic matters is paramount and unparallel to anyone I have met in my life. I had the immense pleasure of learning so much from him, especially in semiconductor device modeling. I hope the knowledge I gained from working under his supervision, I can carry forward in my career.

I would like to thank my supervisory committee members- Dr. James Chen and Dr. Jennifer Bauman for their valuable feedback and for providing me with lots of encouragement during the committee meetings. Their support and feedback have helped me a lot in improving my research skills.

I would like to thank our past and current ECE departmental chairs- Dr. Tim Davidson and Dr. Mohamed Bakr for the financial support from ECE department during my PhD study.

I am grateful to all the staff of the ECE department for creating a friendly working environment for all the graduate students. I would especially like to thank Mrs., Cheryl Gies who is like a motherly figure to me. Whenever I have encountered any problem during my time at McMaster University, she has been a constant support and has helped me in the best way she can.

I would also like to acknowledge all my friends, here in Canada who have stood beside me in my difficult moments. Finally, I would like to thank my parents for their unwavering

support and encouragement during my study. Without them, none of this would have been possible. I hope I can make them proud someday with my accomplishments.

<div align="right">

Arghyadeep Sarkar

Hamilton. ON

November 2022

</div>

To my beloved parents,

Prof Chandan Kumar Sarkar

and

Mrs. Mala Sarkar

Declaration of Academic Achievements

This dissertation was used to fulfill the requirement of a Ph.D. degree. All the research was conducted between the duration of September 2018 to November 2022. During this study, gate leakage process in pGaN HEMTs was examined. A numerical model was built to characterize the gate current in pGaN/AlGaN/GaN HEMTs. This model was developed as a function of gate bias and temperature with a consistent set of parameters. The numerical model had some limitations as it is based on simple approximations such as using the compact diode equation and ignoring the series resistance. This problem was remedied using TCAD simulations which compute the leakage current from electric field distribution throughout the device. Finally, three modified structures were studied to reduce gate leakage in pGaN HEMTs without significantly reducing the drive current. This should help device designers to optimize their device structure for future applications. The author of the thesis is the major contributor to all the associated works presented herein.

The manuscript associated with this work are listed below:

1. Arghyadeep Sarkar, and Yaser M. Haddara. "Modeling of forward gate leakage current for normally off pGaN/AlGaN/GaN HEMTs." *Solid-State Electronics* 196 (2022): 108420.

2. Arghyadeep Sarkar, and Yaser M. Haddara. "Analysis of the forward gate leakage current in pGaN/AlGaN/GaN HEMTs through TCAD simulations" (To be submitted).

3. Arghyadeep Sarkar, and Yaser M. Haddara. " Impact of the device structure in the gate leakage simulations for pGaN/AlGaN/GaN HEMTs " (Manuscript in preparation).

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List of Abbreviations

HEMT	High electron mobility transistor
ZB	Zinc-blende
WZ	Wurtzite
2DEG	Two-dimensional electron gas
TCAD	Technology computer aided design
CC	Current collapse
EL	Electroluminescence
TTF	Time to failure
TE	Thermionic emission
TFE	Thermionic field emission
PFE	Poole Frenkel emission
FNT	Fowler-Nordheim tunneling
TAT	Trap assisted tunneling
DT	Direct tunneling
SBH	Schottky barrier height
UID	Unintentionally doped
LDP	Lightly doped p-type
SRL	Surface reinforcement layer

Chapter 1: Introduction

1.1 Introduction on GaN HEMT technologies

This thesis is about gate leakage modeling in GaN devices. Gallium nitride has excellent material properties which makes it suitable for microwave and power electronics applications [1][2][3].Table 1-1 shows the important properties of GaN in comparison to other materials.

Table 1-1: Properties of today' widely used semiconductors[4][5][6].

	Silicon (Si)	Diamond	Gallium Nitride (GaN)	Silicon Carbide (SiC)
Bandgap(eV)	1.12	5.45	3.4	3.2
Electron Mobility (cm2/V. s)	1350	1000	2000	650
Critical Electrical field (MV/cm)	0.25	5.6	3	4
Thermal Conductivity (W/cm K)	1.5	20	1.3	4.9
Relative dielectric constant (ε_r)	11.8	5.5	9.5	9.7

In power electronics, the use of GaN device as a power switch is a big boost for making highly efficient power converters. GaN power switches are high electron mobility transistors (HEMTs). GaN HEMT device can produce a very high drive current due to its inherent two-dimensional electron gas(2DEG) properties which will be discussed in more detail later (see Section 3).

1.2 Crystal Structure of GaN

Like other III-nitride groups, GaN has two common crystal structures- zinc-blende (ZB) and wurtzite (WZ) which is shown in Figure 1-1. The W structure has a hexagonal shape and is considered more thermodynamically stable, whereas ZB is more susceptible to doping[7]. The density of states around the fermi-level for W is much lower than ZB, hence the W structure has a higher bandgap[8].

Ga

N
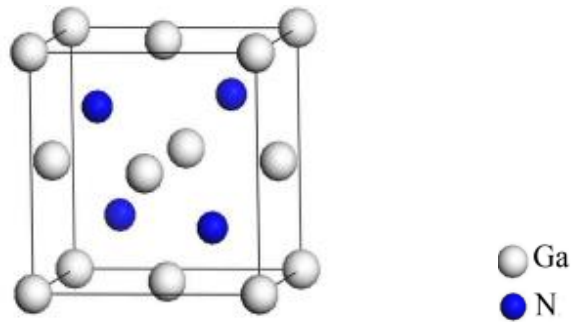
(a)
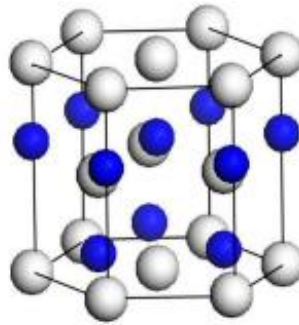
(b)

Figure 1-1:Crystal Structure of GaN (a)Zinc-blende(b)Wurtzite[7].

1.3 Polarization Effects in GaN

Polarization effects are observed in AlGaN/GaN heterostructures as shown in Figure 1-2. There are two types of polarization found in GaN- spontaneous polarization and piezoelectric polarization. There is a strong electrostatic attraction between the gallium and nitrogen atoms due to their strong ionicity which results in atomic displacement. This creates a large spontaneous polarization field within the crystal [9]. In GaN devices, a thin AlGaN layer is grown on top of the GaN layer which is called the barrier layer. As a result of lattice mismatch between the AlGaN and GaN materials, a strain is developed on the barrier layer. Strain creates structural deformation which in turn creates an additional component of polarization known as piezoelectric polarization.
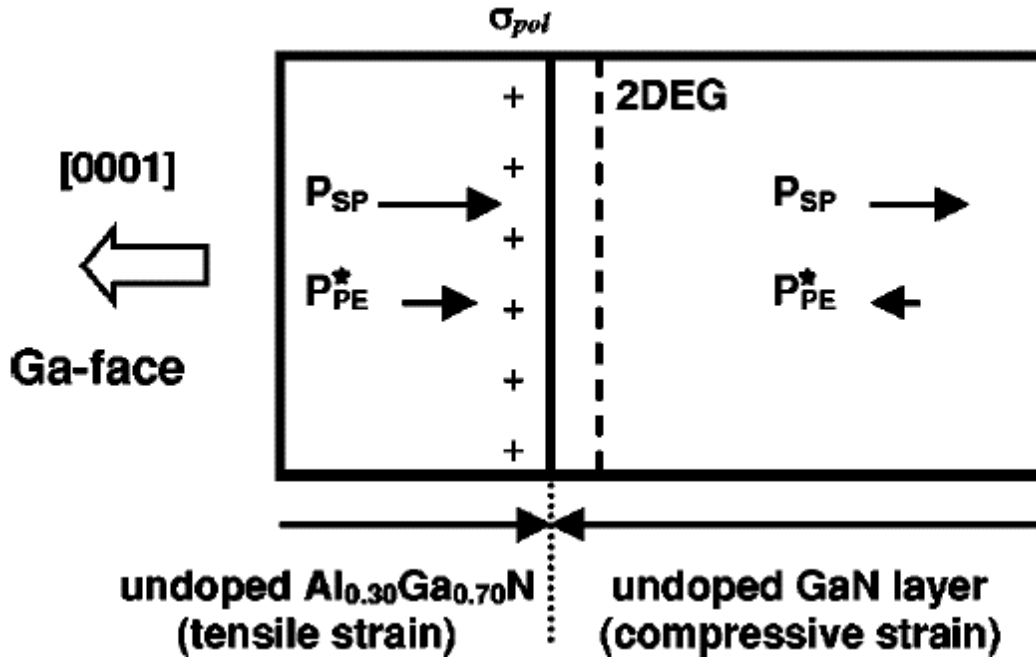
Figure 1- 2 :Polarization effect in AlGaN/GaN heterostructure[10].

These two components of the polarization field induce a strong electron cloud at the interface between the AlGaN and GaN layers. This electron cloud can be represented as a sheet of electron

charge; hence is the term two-dimensional electron gas(2DEG). This 2DEG acts a conducting channel of high mobility electrons for the HEMT devices. One of the biggest advantages of GaN HEMT devices compared to other compound semiconductors such as GaAs is that there is no need for additional doping. Thus, the scattering is significantly less, so the mobility degradation is also less. The band structure of a typical AlGaN/GaN HEMT is shown in the figure below. In Figure 1-3, ϕ_b represents the Schottky barrier height, while E_C, E_V and E_F represent the conduction band edge of GaN, valence band edge of GaN and position of fermi-level at equilibrium, respectively.
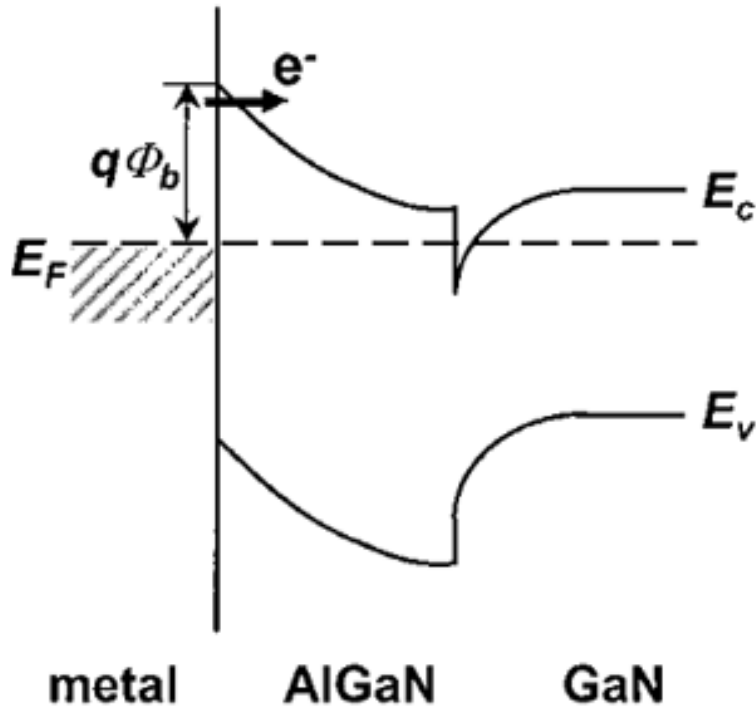
Figure 1-3: Energy band structure of a typical AlGaN/GaN structure.

As stated earlier, in absence of an external electric field, the total polarization is the sum of the spontaneous polarization (P_{SP}) and piezoelectric polarization (P_{PZ}) [11][12]. The spontaneous polarization is given by

$$P_{sp}(x) = (-0.052x - 0.029). \tag{1.1}$$

Here, x is mole fraction of AlGaN layer. So, at x=1, it is AlN and x=0, it is GaN. Similarly piezoelectric polarization can be modeled by[12]

$$P_{PE}(x) = 2\frac{a(x) - a(0)}{a(0)}\left[e_{31}(x) - e_{33}(x)\frac{C_{13}(x)}{C_{33}(x)}\right]. \tag{1.2}$$

Here, a(x) and a (0) represent the lattice constants of AlGaN and GaN respectively, C_{13} and C_{33} are elastic constants and e_{31} and e_{33} are piezoelectric constants. From this polarization charge density at the hetero interface can be calculated as

$$\sigma = P_{SP}(AlGaN) + P_{PZ}(AlGaN) - P_{PZ}(GaN). \tag{1.3}$$

From this, 2DEG carrier concentration can be calculated which is given by [12][13]

$$n_s(x) = \frac{\sigma(x)}{e} - \frac{\varepsilon_0\varepsilon(x)}{de^2}[e\phi_B(x) + E_F(x) - \Delta E_c(x)] \tag{1.4}$$

where $\varepsilon(x)$ is the dielectric constant, d is the AlGaN layer thickness, $e\phi_B$ is the barrier height, E_F is the Fermi-level position, and ΔE_C is the conduction-band discontinuity between the two materials.

1.4 Structure of AlGaN/GaN HEMT

In a conventional HEMT device, a very thin AlGaN barrier layer is deposited over the GaN layer leading to the formation of 2DEG shown in Figure 1-4. As a result of this heterostructure, a triangular quantum well is formed. The electrons are confined to fixed energy levels within this quantum well, hence their mobility is not reduced by scattering effects leading to high electron velocities. This feature makes AlGaN/GaN HEMTs an ideal choice for transistors used in high frequency operations. The basic structure of a normal AlGaN/GaN device is shown below.
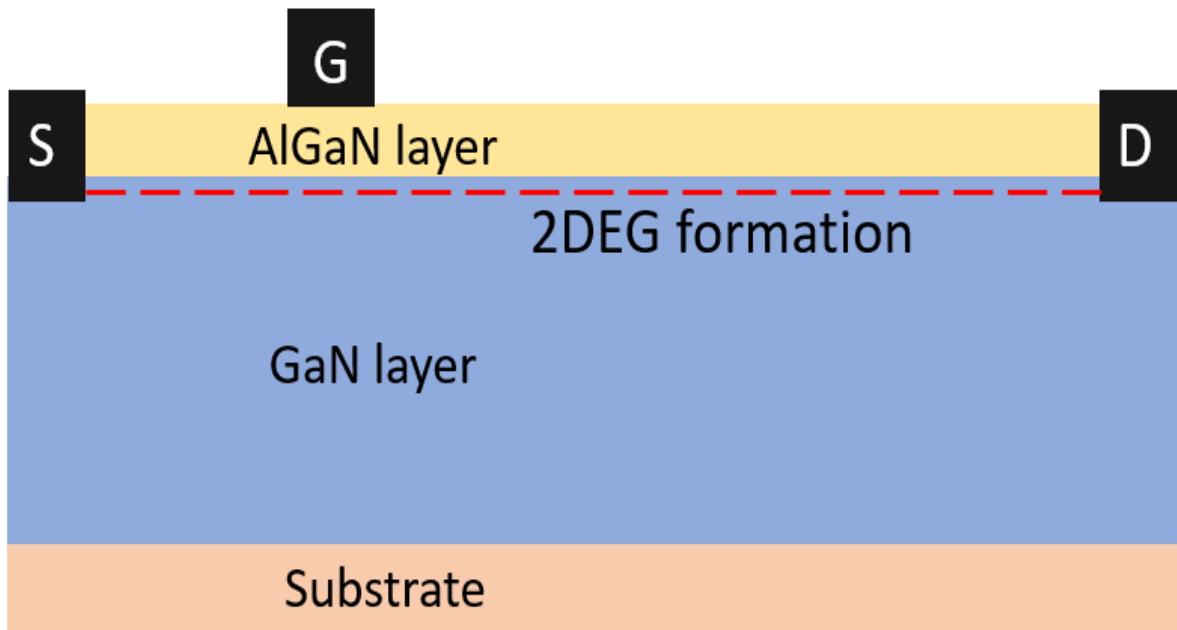
Figure 1-4:Structure of a standard AlGaN/GaN HEMT structure.

The source and drain are generally made to be ohmic contacts while the gate is made to Schottky contact so that the gate current is ideally zero, similar to a conventional MOSFET. As a result of the barrier at the heterointerface between AlGaN and GaN, electrons in the 2DEG should be blocked from spilling over from the channel into the gate. Even though the formation of the 2DEG

is an inherent phenomenon, the gate bias controls the amount of 2DEG present in the channel resulting in a very high current density. This is shown in Figure 1-5. Assuming that the AlGaN layer is completely ionized [14], we can express the 2DEG (n_s) as a function of gate voltage (V_{GS}) by:

$$n_s = \frac{\varepsilon}{qd}\left(V_{GS} - V_{th} - E_f\right) \tag{1.5}$$

where, V_{th} is the threshold voltage and E_f is the position of the fermi-level.
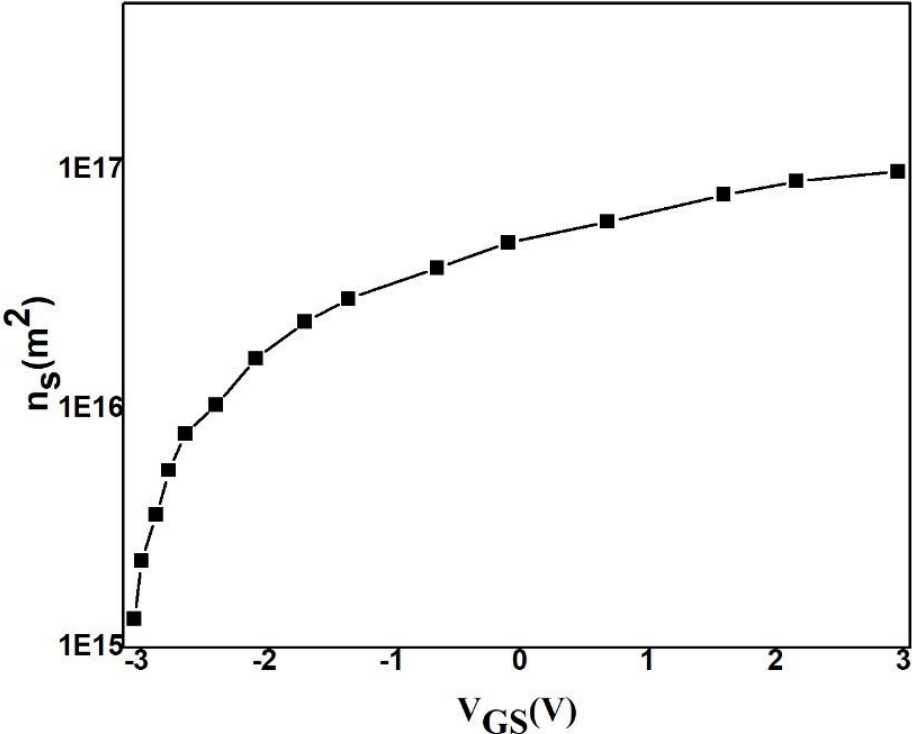
Figure 1-5: Variation of n_s with V_{GS} (adapted from [14]).

One of the major drawbacks in the initial development of GaN devices was that they can only be used in depletion mode operation because of strong 2DEG formation. This means the device is normally on without the application of a gate bias, hence there is always current flowing between the source and drain. Thus, it would require a negative bias to turn the device off.

1.5 Enhancement based GaN devices

Enhancement mode devices are needed for switching-based electronics circuits. Thus, in the last decade, there has been considerable research to develop enhancement mode GaN HEMT devices. One of the most promising avenues for enhancement mode operation is the introduction of a p-doped GaN layer above the AlGaN layer to raise the conduction band edge above the fermi level at zero gate bias.

1.5.1 pGaN HEMT operation

The most attractive option among the enhancement mode techniques developed is to use a p-type doped GaN cap layer under the gate[15]. In this case, the pGaN cap layer lifts the conduction band edge above the fermi-level in the absence of an external bias. To maximize 2DEG depletion, the barrier layer thickness and mole fraction need to be optimized. The typical structure of pGaN gate HEMT is shown below in Figure 1-6.
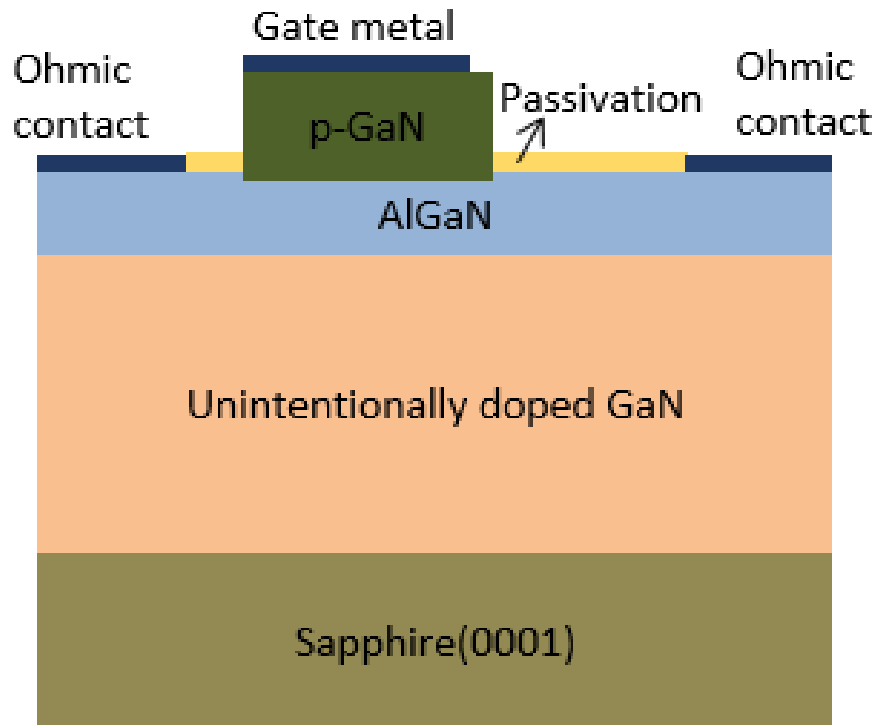
Figure 1-6: Structure of pGaN gate structure.

The cap layer of this structure is generally doped with high concentration magnesium (Mg) ions typically in the range of 10^{19} cm^{-3}. One of the key technological challenges is selective etching [either through inductively coupled plasma (ICP) or reactive ion etching (RIE)] of the cap layer from the access regions. This is due to the fact if pGaN layer is not removed from the source/drain regions, the on-resistance in the channel will increase which will degrade the transfer characteristics of the device.

The pGaN layer and n-doped GaN channel present above and below the AlGaN layer respectively, create a pin diode in the vertical gate structure. Initially, this pin diode is off but once more positive bias is applied to the gate, this diode becomes forward biased. Once pin diode is on, holes from the pGaN cap layer tunnel into the channel. These injected holes can accumulate extra electrons

from source to maintain charge neutrality. Additional electrons are swept away towards the drain under the influence of bias while holes having lower mobility accumulate near the gate. This process helps in significantly raise drain current density. Since channel conductivity is modulated under the gate by this hole tunneling process, this kind of device is called gate injection transistor (GIT).

However, one of the technological challenges in the fabrication of pGaN gate is the doping concentration. Firstly, it is important to implant dopants into the cap layer without destroying its crystallinity and secondly, ions implanted in the cap layer is not completely ionized because of the hole compensation mechanism. Mg ions are compensated by the presence of hydrogen arising from growth process conditions[16]. This needs to be addressed for two reasons-conduction band edge will not go above the fermi-level if the doping is low and the number of holes tunneling into the channel will be lower resulting in a lower drive current for the device. Thermal annealing can activate holes in the pGaN layer by removing all hydrogen complexes [17]. Still some work needs to be done in terms of optimization of process conditions to improve upon hole concentration. Despite all of this, pGaN gate HEMT is the most promising candidate currently among lateral GaN HEMT structures which is getting commercialized for future applications.

1.6 Thesis Overview

This thesis primarily focuses on the gate leakage study in pGaN HEMTs. We have presented a simple numerical model and used TCAD simulations to characterize and analyze the gate leakage current in pGaN HEMTs. The dissertation is divided into five chapters whose brief summary are outlined as below.

The main focus of this thesis is gate leakage. However, before discussing gate leakage, we give a more general introduction to reliability in GaN HEMTs. This is not intended to be a comprehensive review but a brief introduction to some of the main issues in reliability since gate leakage is both a reliability concern and a predictor of device lifetime.

Chapter 2 reviews the 2 important reliability concerns in GaN HEMT devices. This chapter focuses on breakdown voltage and hot electron degradation. Device breakdown occurs when the off-state leakage rises sharply beyond the tolerance limit at a certain bias voltage. This is caused by the leakage path at different regions in the device. The role of hot electrons responsible for the degradation of many device parameters is also discussed. Hot electrons interact with device defects and charge transfer takes place which alters parameters such as V_{th} and g_m. Degradation of these parameters can be used to estimate device lifetime.

Chapter 3 focuses on the gate leakage process in GaN HEMTs. We have looked at different mechanisms through which gate current conduction takes place in GaN HEMT. We have summarized the previous study on gate leakage modeling in pGaN HEMTs and pointed out some of the impending issues that need to be addressed in the model that can give a physical insight into the gate leakage process. Finally, we describe in detail the experimental characteristics of the five devices derived from previously published studies, that will be used for subsequent modeling and TCAD simulation studies for the next two chapters.

Chapter 4 focuses on modeling the forward leakage current in pGaN/AlGaN/GaN HEMTs. The proposed work is a simple numerical model which can explain gate leakage current as a function of gate bias and temperature for different pGaN devices fabricated by different research groups with different gate metal contacts, device dimensions, and process conditions. Gate leakage can be explained primarily by Fowler Nordheim Tunneling mechanism (FNT) without the need to

invoke multiple mechanisms or to hypothesize different leakage mechanisms for different devices. However, at a low bias gate current (I_G) flattens out and FNT undercalculates the current in some devices. It can be assumed that another mechanism is occurring in tandem with the FNT which can describe the behavior at low bias. This mechanism happens via surface traps and is called Trap Assisted Tunneling (TAT).

Chapter 5 focuses on the TCAD simulation study of forward gate leakage current in pGaN/AlGaN/GaN HEMT. One of the limitations of the numerical model developed in the previous chapter is that it is based on simpler approximations such as using the compact diode equation and ignoring series resistance. Using TCAD simulations, the above problems can be resolved since leakage current is computed from electric field distribution in the whole structure. From the simulations, some of trap levels are identified that cause leakage at low bias. These trap levels are compared to the known trap levels in GaN.

Chapter 6 focuses on the device structure of the pGaN/AlGaN/GaN HEMTs and its impact on the gate leakage current. The pGaN doping and its thickness have an impact on the leakage current. We have also examined three modified structures of pGaN HEMTs which can reduce the gate leakage current. We have studied these structures through TCAD simulation and calibrated the leakage current as well as the drain current. Our simulation closely matches the experimental results for these structures. This can help future designers in optimizing their pGaN HEMT devices for better performance.

1.7 Thesis Contributions

There have been quite a few experimental studies in pGaN/AlGaN/GaN HEMTs focusing on the gate leakage process. The authors have used several different mechanisms to explain the gate

leakage process, with some of them being empirical fits. Our objective in this thesis is to simplify the complexities of gate leakage modeling and present a physical insight into the underlying mechanism that can explain the gate leakage process. We hope through this work, we can contribute to the GaN HEMT modeling community. The following contributions have been made.

I.   A simple model with a consistent set of parameters has been developed to model gate leakage current in pGaN HEMT.

II.   This model is validated against five devices from four different research groups with different contact metals, geometries, and process conditions.

III. According to our developed model, Fowler-Nordhiem Tunneling (FNT) mechanism can explain the gate leakage current in all five devices without hypothesizing different leakage mechanisms for different devices. FNT underestimates the leakage current at low bias, where the leakage current is governed by surface traps. Hence, trap assisted tunneling (TAT) has been used for low bias regions.

IV.   This model considers the split in voltage between the two diodes in the gate stack which previously published models have ignored in their analysis.

V.   The numerical model is further supported by TCAD simulations which use the same physical mechanism to characterize the gate leakage. Some important trap levels have been identified from the TCAD simulations and compared with known trap levels in GaN.

VI.   Three potential structures have been explored which can reduce leakage current in pGaN HEMTs. These structure looks promising since they reduce gate leakage current while maintaining the necessary drive current. The published experimental studies for these devices closely match our TCAD simulations for the gate and drain currents. This should encourage device engineers to pursue these modified structures to improve their device design.

This research has generated the following article:

1. Arghyadeep Sarkar, and Yaser M. Haddara. "Modeling of forward gate leakage current for normally off pGaN/AlGaN/GaN HEMTs." *Solid-State Electronics* 196 (2022): 108420.

2. Arghyadeep Sarkar, and Yaser M. Haddara. "Analysis of the forward gate leakage current in pGaN/AlGaN/GaN HEMTs through TCAD simulations" (To be submitted).

3. Arghyadeep Sarkar, and Yaser M. Haddara. " Impact of the device structure in the gate leakage simulations for pGaN/AlGaN/GaN HEMTs " (Manuscript in preparation).

Chapter 2: Reliability issues in GaN HEMTs: Device Breakdown and Hot Electron Degradation

2.1 Introduction

Even though GaN HEMTs have shown impressive performance over the last few years in power applications, it does have certain reliability concerns that need to be addressed. Among them, threshold voltage(V_{th}) shift[18], current collapse[19] and device breakdown[20] are some of the major issues that are being sorted after. For example, current collapse in GaN occurs due to the trapping of channel electrons and device breakdown happens when a leakage path is created in the device structure at the application of high drain voltage. Reliability analysis in GaN HEMT involves three bias states: off state, semi-on state, and on state[21]. In the off state, the device is switched off. At this state, device breakdown is calibrated based on the maximum voltage the device can sustain without leaking any significant amount of current. In the on state, the device is switched on and issues such as V_{th} shift, positive bias temperature instability (PBTI), and time-dependent gate breakdown are examined[21]. In the semi-on state or switching state, the device is not turned on or off. Both the voltage and current across the device are high simultaneously. In this condition, the high electric field in the GaN channel accelerates the electrons, leading them to become "hot".[22]. These hot electrons have sufficient energy to overcome the potential barrier and get injected into the different regions of the device such as the barrier layer, passivation layer, or buffer layer. The traps present in the GaN structure interact with these hot electrons leading to degradations in several device parameters[23]. In this chapter, we are going to discuss very briefly device breakdown mechanisms (off-state) and review primarily the effect of hot electrons in GaN HEMTs.

2.2 Breakdown Mechanism

Generally, semiconductor devices including GaN HEMTs are rated by the maximum voltage they can withstand. It is particularly important for power devices since a high drain voltage is applied across the device during the power converter operations. Device breakdown measurements are performed under off-state conditions which are marked by a sharp rise in drain current at a critical drain voltage. For example, it can be calibrated by measuring the drain voltage at which off state drain leakage is 1 mA/mm or above[24]. Figure 2-1 shows the device breakdown characteristics in GaN HEMT devices.
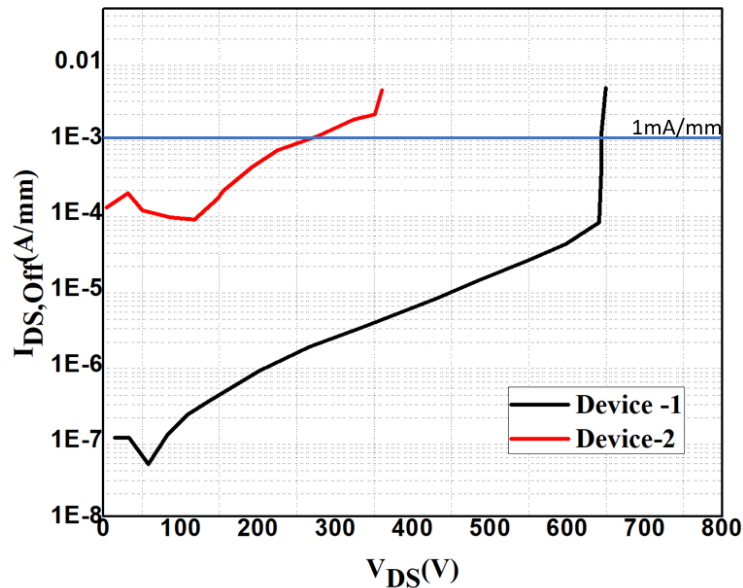
Figure 2-1:Variation of off state leakage current with drain bias for 2 devices[24]. Breakdown voltage is marked at drain leakage of 1mA/mm.

A breakdown can be catastrophic and controlled depending on operating experimental measurement criteria[25]. If set up is performed in a voltage-controlled mode allowing for an

unmanageable rise in drain current, it will lead to permanent damage to the device. However, if the measurements are done in current-controlled mode, a sustainable breakdown can be achieved where different leakage current paths can be identified. Hence, understanding the breakdown process is crucial in optimizing the fabrication process for future applications.

At the application of a high bias, leakage paths are created within the device. The device breakdown along these leakage paths. Now, we look at the breakdown mechanisms originating from different leakage paths[25]. The drain leakage current is governed by reverse gate leakage during the off-state conditions. In this case, gate bias is quite low. So, the leakage is primarily dependent on the reverse gate Schottky junction. The role of surface states becomes very important in this regard. Carrier conduction within the surface states happens via hopping. When the device is being operated very close to the threshold voltage, the drain-source sub-threshold leakage current contributes to the device breakdown[25]. It has been reported that when the gate bias is near-threshold voltage, device breakdown occurs at a much earlier drain voltage, so it can be assumed that sub-threshold current dominates breakdown in these conditions. This effect becomes more prominent for shorter gate-length devices.

Device breakdown directly depends on the gate-to-drain spacing. The device with a longer gate-drain length (L_{GD}) will have a larger breakdown voltage (V_B) shown in Figure 2-2(a). Increasing L_{GD} will improve V_B, but it will increase the on-resistance (R_{ON}), so there is a trade-off between these 2 factors shown in Figure 2-2(b). GaN devices, today are optimized to reach high breakdown capacity in the range of 500~1000 V, and the probability of leakage having a lateral path reduces. In this case, the leakage is determined by the vertical drain to substrate leakage current. This is further illustrated by the sharp rise of substrate current compared to other terminal leakage currents. This usually happens due to poor insulation of the buffer layer.
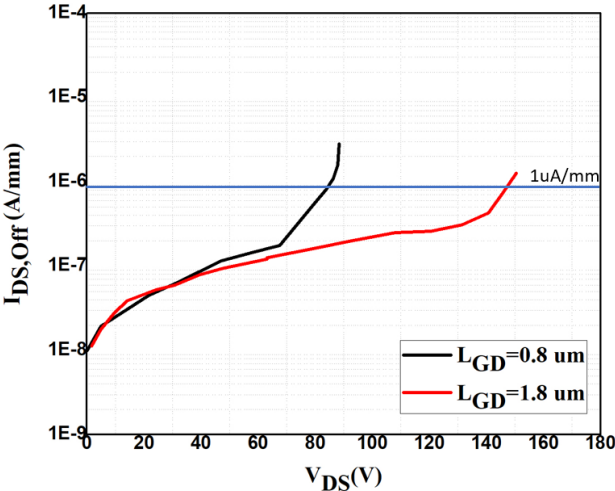
(a)
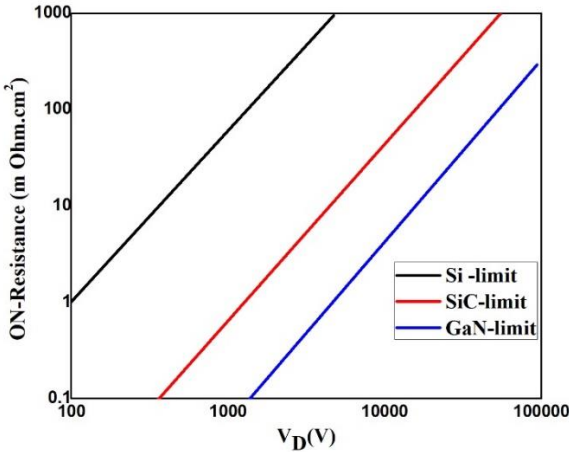
(b)

Figure 2-2 (a): Variation of drain leakage with drain voltage for two with different gate to drain distance. Breakdown is calibrated at 1 uA/mm or above [26]. (b)Trade-off between on-resistance and breakdown voltage for different materials[27].

2.3 Hot electrons in GaN

As previously stated, hot electrons are generated in the presence of a high electric field. Now, we are going to address some of the key reliability issues concerning hot electrons from a GaN device point of view.

2.3.1 Interaction of defects with hot electrons: threshold voltage shift and transconductance degradation

The performance of any semiconductor device depends on material processing. In GaN technology, it becomes more crucial since GaN is grown on foreign materials such as silicon, sapphire, SiC, etc. An important parameter to characterize the quality of the grown material is defect density. Several kinds of defects are formed depending on the various growth conditions [28][29]. GaN HEMT is mainly grown from two process technologies. The first one is molecular beam epitaxy (MBE) [30] and the other one is metal-organic chemical vapor deposition (MOCVD)[31]. One defect common to both processes is point defect. Some of the common point defects in GaN are gallium and nitrogen vacancies, antisites, oxygen impurities, and Fe-based complexes[32]. These defects exist in their hydrogenated form (electrically inactive). So, when hot electrons interact with these hydrogenated defects, it removes from them hydrogen and turns them into electrically active defects[33]. These charged defects act as a trap center for electrons and holes in the GaN device. One of the ways to understand the interaction of defects with hot electrons is to analyze device characteristics such as threshold voltage shift and transconductance.

The threshold voltage (V_{th}) is an important parameter in any FET device as it is the bias point at which the device turns off and on. V_{th} shift happens due to a change of defect state arising from hot electron injection[33]. The hot electrons are most prominent when the device is stressed in a

semi-on state. To modify a defect electrically, hot electrons must have energy higher than the activation energy of that defect. Defect modification can alter the channel potential, hence there is a V_{th} shift. The nature of the V_{th} shift depends on the net shift of charge transfer. V_{th} shift can be modeled based on the change of defect charge density under the gate with stress time[35] using the equation:

$$\Delta V_{th}(t) = \frac{\Delta Q_d(t)\, d_{AlGaN}}{\varepsilon} \tag{2.1}$$

where ΔQ_d, and d_{AlGaN} represent the variation of change of charge density with stress time, and the thickness of the AlGaN layer respectively. V_{th} shift can be positive or negative (Figure 2-3).
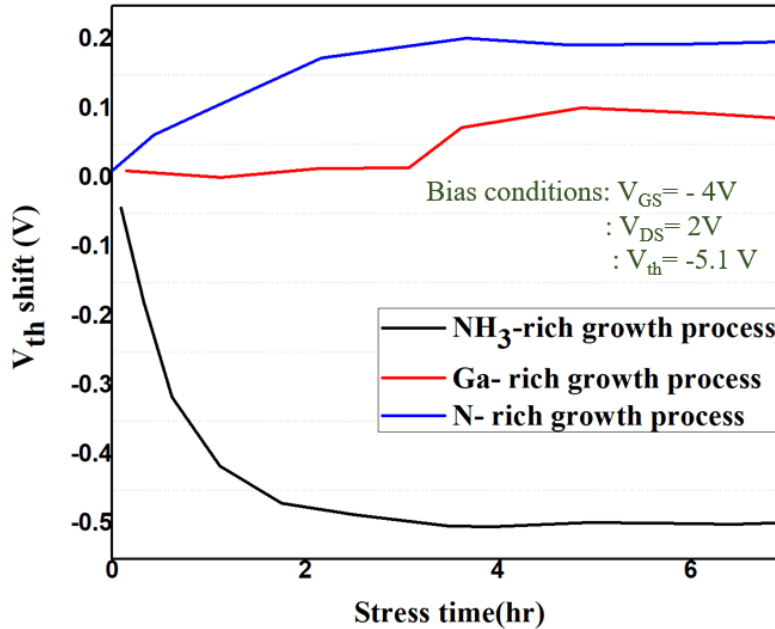
Figure 2-3: Positive shift and negative V_{th} with stress time for the different growth conditions[34].

20

For example, if the V_{th} shift is negative, there is an increase in net negative charge. Similarly, for a positive V_{th} shift, there must be a decrease in net negative charge. Roy *et al.* proposed that the growth of GaN HEMT in Ga-rich or N-rich conditions has a positive V_{th} shift while NH_3-rich conditions would trigger a negative V_{th} shift for stressing the device above threshold voltage[33][34][36][37]. The reason for the positive shift is attributed to the dehydrogenation of Ga vacancies while the negative shift is from N-antisites. However, in a recent publication, the presence of other defects has been reported. For example, a positive V_{th} can be credited to the divacancy complexes whereas a negative V_{th} shift occurs due to the Fe- impurity complexes [38].

With hot carriers reconfiguring defects, variation in transconductance characteristics has been reported[35]. Jiang *et al.* stated that transconductance degradation occurs during the ON state stressing[32]. Not only the nature of the defect is important in GaN HEMTs, but its location in the device structure is also critical. For example, acceptor-like defects are presumed to be located somewhere around the gate edge near the drain side, where the electric field is expected to be the highest. Similarly, donor-like defects are present mostly in the GaN buffer closer to the drain, or in the AlGaN layer. Therefore, when hot electrons are injected into different parts of the device, it encounters these defects based upon which g_m degradation takes place. Both g_m degradation and Vth shift occur due to changes in the charge density. Figure 2-4 shows the g_m degradation across various stress times.
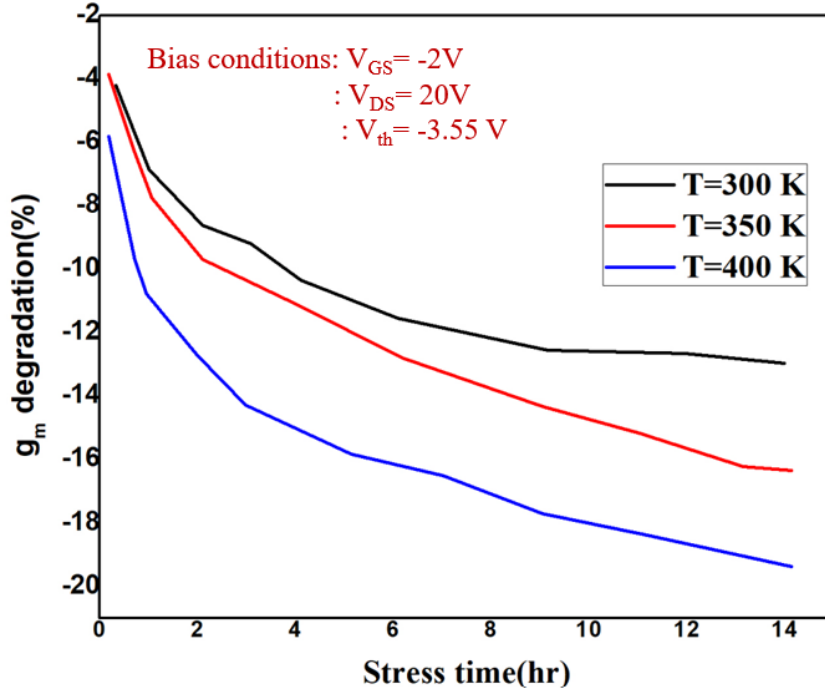
Figure 2-4: Variation of g_m with stress time at different temperatures[35].

2.3.2 Effect of Radiation

GaN HEMT devices are used in space and nuclear applications [40][41].In those cases, these devices will be exposed to highly energetic protons as well as other kinds of radiation. Radiation can be used in form of stressing to generate hot electrons. For example, Martínez *et al.* demonstrated the effect of gamma radiation during the semi-on state from the point of view of hot electrons[42]. It was observed that the dynamic on resistance has increased due to the loss of channel electrons as a result of the hot electron injection process. The double effect of radiation along with semi-on bias stress provides enough energy to the electrons to escape from the channel either into the buffer or barrier layer. This radiation stress was conducted on GaN MISHEMT and p-GaN HEMT to understand how device behavior changes for a different structure. The p-GaN

HEMT showed no effect on dynamic on resistance due to the presence of the p-type GaN layer that initiates the hole injection process which releases back the trapped electrons into the channel. However, in MISHEMT, this radiation along with the semi-on state provides enough energy for the electron to get trapped. The presence of the insulator in MISHEMT makes the trapping behavior more severe which reflects in the increase of dynamic on resistance.

2.3.3 Current collapse

Current collapse (CC) can be defined as a decrease in dc drain current when a high drain bias voltage is applied [43][44]. It has been observed that CC can occur in GaN HEMT devices that previously show no collapse by exposing the device to a high voltage over a long stress time. This CC phenomena typically reduce the maximum drain current and simultaneously increases the knee voltage [45] which in turn reduces the output power of the transistor. Henceforth, it is a significant factor that limits the device's performance. Hot electron plays a part in the CC process[46][47][48]. The electric field has a strong influence on the amount of CC[49]. The peak electric field especially at the gate edge of the drain is critical in this regard. The gate edge area assumes a dominant role in the electron trapping mechanism since it exhibits the highest electric field, thus it is regarded as a localized trap center. However, it has been found that due to surface leakages and hot electrons, the whole gate drain access region could also contribute to carrier trapping and it is called a non-localized trap center[46]. In one report, Meneghini *et al.* verified the above claim of non-localized trapping in the entire gate drain access region by showing an increase in dynamic on resistance for devices with longer gate drain lengths[47].

Now, let us try to understand the physics of hot electrons responsible for CC in GaN HEMT. As stated earlier, during the high power (HP) state channel electrons become hot by gaining enough kinetic energy. These hot electrons can cross the potential barrier of the AlGaN layer and are

injected into it where they become trapped. There is another possibility that hot electrons can generate deep levels in the GaN layer which could become a potential trap site. Both surface and the buffer layer contribute to electron trapping phenomena[48][49][51]. Surface-induced CC is related to surface states and can be explained by the widely accepted virtual gate model by Ventury [50]. Similarly, buffer-induced CC is mainly due to the injection of hot electrons into the buffer traps. The buffer induced CC has been illustrated in Figure 2-5. More details can be found in [51]. Initially, the trap associated with the buffer layer responsible for CC is not occupied at the off state. During the HP state, high energetic electrons are injected into these empty traps and are trapped. The 2-DEG electron density would get reduced and the on-resistance increases. At elevated temperatures, the trapped electrons are released by thermal emission and optical phonon scattering that reduces the buffer-based CC effect. Meneghini et al. studied the role of bias voltage leading to current collapse shown in Figure 2-6[52]. It was reported that increasing the gate bias above the threshold voltage has a pronounced effect on the dynamic R_{ON} degradation due to hot electron generation. Increasing the drain bias also increases the R_{ON} value till it saturates potentially due to the filling up of traps in the device. Two pronounced trap levels labeled as E_1 and E_2 respectively have been identified from isothermal measurements. The effect of the E_1 trap is generally seen during on-state conditions while the E_2 trap is active for both off and on-state conditions. The E_1 trap has an activation energy of 0.60 eV, while E_2 has an activation energy of 0.96 eV.
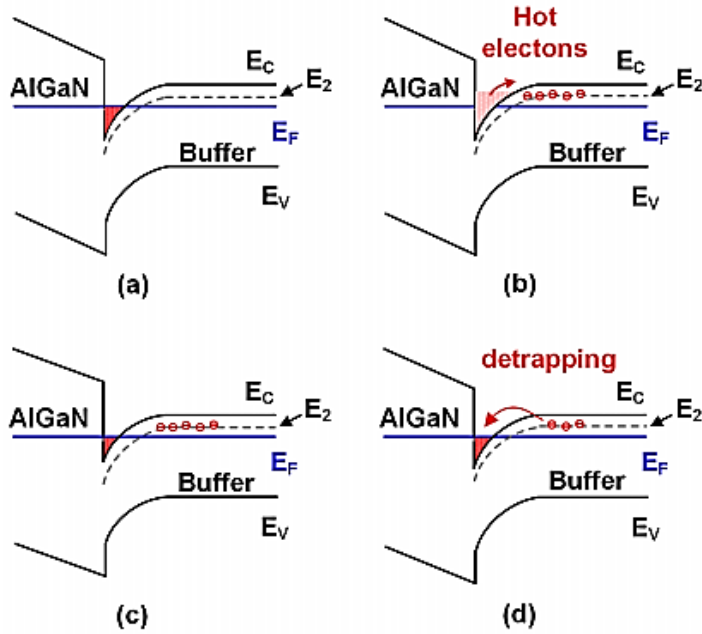
Figure 2-5: Schematic band diagram of the AlGaN/GaN HEMT illustrating buffer-related CC from hot electrons[51].
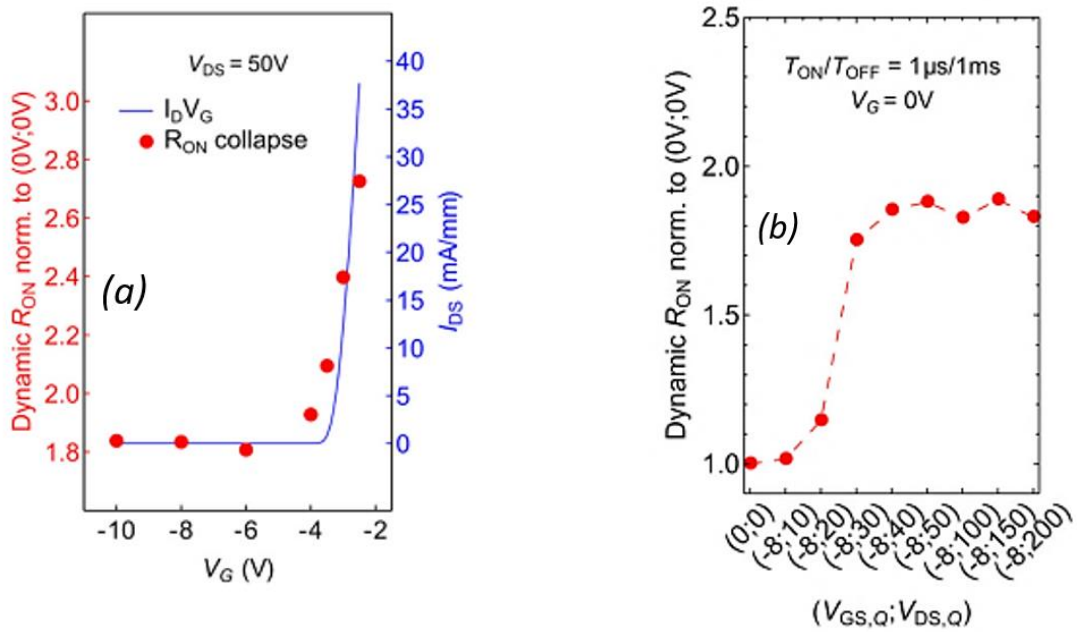
Figure 2-6:Dependence of Ron collapse on :(a) gate bias at semi-on/on state b) drain bias at off state[52].

As CC is a major roadblock for GaN HEMT devices, there has been an extensive study to mitigate this phenomenon [53][54][55][56]. The passivation layer has been used extensively in the literature [57][58] primarily to reduce CC from surface states. The purpose of passivation is to reduce defect densities on the surface. Among them, SiN passivation is quite popular. LPCVD SiN along with a self-aligned slanted gate structure can reduce the electric field at the gate edge, henceforth reducing the effect of hot electrons[59]. Various surface treatment has also been used to suppress the effect of CC[55]. It has been reported that SF_6 plasma treatment has been the most effective when compared to other gas plasma such as O_2, N_2O, or CF_4.SF_6 did not suffer from any cross contamination such as oxygen or nitrogen impurity and also reduced the density of deep levels in GaN. Recently, Tanaka *et al.* developed a hybrid drain embedded gate injection transistor (HD-GIT) which has a p-GaN layer near its drain side which can reduce CC through hole injection[60].

2.3.4 Device Lifetime Analysis

As the GaN HEMT device is used over time and again, its longevity becomes a critical issue for its optimal operation. Eventually, the device fails as one or many critical parameters such as g_m degradation, gate leakage current, and R_{on} degradation, exceed the tolerance limit. In silicon-based FET, it is easier to standardize reliability testing due to vast experience in Si reliability, whereas in GaN-based devices, it is still difficult to come up with established acceleration factor-based models since many failure modes are still unknown to us.

Now, we take a look at some of the previous studies done in GaN HEMT where device failure analysis were conducted .For example, TTF can be defined as the amount of stress time required for a 10% increase in R_{ON}[61][62][63].Likewise in another study, Rossetto *et al.* defined gate leakage current as the signature parameter to define device failure for p-GaN HEMT[64] .In this

case, TTF was defined as the time taken to reach 40 mA/mm gate leakage current with an increasing gate stress time at a particular gate bias. Wang *et al.* defined the time failure criterion on the reduction of drain saturation current by 20% for InAlN/GaN HFETs[65]. Paine *et al.* proposed a reduction of 27% in transconductance(g_m) as a signature parameter for the time to failure criterion[66]. Table 2-1 summarizes the different types of TTF test performed in GaN HEMT based on different fail criteria.

TTF follows a Weibull distribution given by $F(t) = 1-\exp(-t/\eta)^\beta$, where $F(t), \beta$ and η are the Weibull cumulative distribution function, shape, and the scale factor, respectively.. Acceleration factor (AF) which is defined as the ratio of time to failure at normal condition to the time of failure at accelerated stress condition. As per study done in [64],AF is around 10^8[normal stress=5 V and accelerated stress=8V].

Table 2-1: MTTF calculation from different stress conditions.

MTTF	Stress Conditions	Failure criterion	References
30 hrs	V_{GS}= -3V and V_{DS}=30V	10% increase in R_{on}	[61]
> 20 years	V_G=5V	Increase of I_G to 40 mA/mm	[64]
24700 hrs	T_{ch}=203 ° C, V_{ds}=12	27% reduction in g_m	[66]

2.4 Characterization of hot electrons: Electroluminescence

So far, we were looking at hot electrons with respect to various device parameters. Now, we will take a look at the evidence that hot electrons are generated in the GaN device using electroluminescence (EL) spectroscopy. Using EL, changes in electric field distribution during stressing can be observed, hence this can be used to identify the generation of hot electrons in AlGaN/GaN HEMTs [67][68][69][70][71]. The generated number of hot electrons is directly proportional to the EL intensity. The intervalley or intravalley transition of hot electrons within the conduction band is responsible for EL spectra as shown in Figure 2-7.
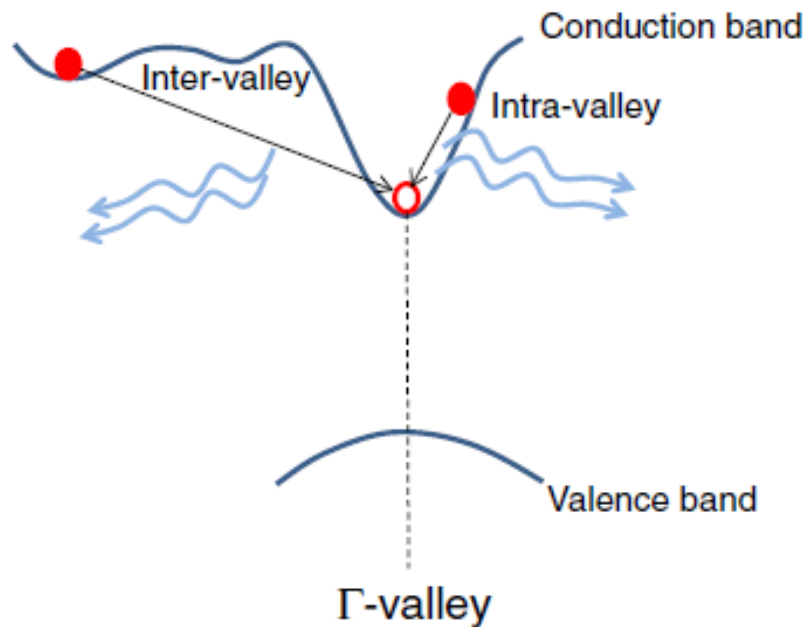
Figure 2-7:Mechanisms responsible for hot-electron electroluminescence in AlGaN/GaN HEMTs[25].

Meneghini *et al.* verified the hot electron degradation from on stress based on EL investigation[73]. When gate bias is increased beyond the pinch-off condition, EL intensity started increasing implying the hot carrier's generation from a high energy level due to a high electric field. It reaches a peak intensity value with a bias increase, then it is observed that intensity starts to decrease due to the reduction of channel electrons shown in Figure 2-8. At higher bias, self-heating dominates. Self-heating effects bring about strong electron scattering, reduction in the mean free path, etc. leading to weaker hot electron degradation.

In one study, EL was correlated to TTF[74].Based on TTF being defined as the stress time for 10% increase in R_{ON} and it is reported that TTF has a power law dependence on electroluminescence (EL) signal (TTF$\approx \alpha.EL^{-\beta}$). The values of α and β are 1.6×10^{-3} and 1.43 respectively. Since EL intensity dependence on applied gate bias has a bell-shaped curve as shown in Figure 2-8, TTF has a similar dependence on gate voltage level.
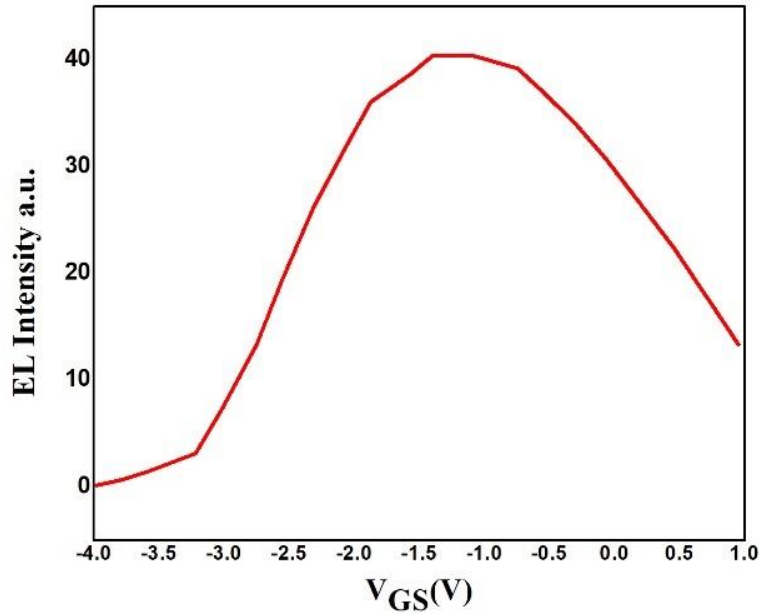
Figure 2-8: EL versus V_{GS} curves measured (at $V_D = 30$ V) before stress. (Redrawn from[73]).

2.5 Hot electrons affect circuit performance

In this section, hot electron degradation will be discussed in terms of GaN-based power converter switching performance[75][76][77][78]. As previously stated, an increase in dynamic on-resistance is a persistent problem in GaN HEMT limiting its commercial growth, its effect becomes more pronounced when during the switching state of the GaN devices[79]. Two kinds of switching occur for GaN-based power converters which can be categorized as hard switching and soft switching.

2.5.1 Hard Switching

When the transistor is turned on or off, the transition time required to reach one stage to another is very short, but it does not happen instantaneously. This transition stage is called switching. The

most common form of switching is hard switching. To elaborate on this, let's take an example of a GaN-based boost converter (Figure 2-9 (a)). As you can see from Figure 2-9(b), during off-state input voltage (V_{in}) which will be equal to the voltage between the drain and source across the GaN switch, and since the gate voltage (V_{GS}) is below the threshold, no current (I_{DS}) will flow. During the switching phase as previously mentioned which is not instantaneous, there is a phase when V_{DS} starts to fall with $V_{GS}>V_{th}$, and the drain current (I_{DS}) starts to rise till it becomes equal to the inductor current. During this short interval of time, there comes a stage when current and voltage are high simultaneously (Figure 2-9(b)). Thus, the electric field in this instant is quite high and it generates a large number of hot carriers responsible for electron trapping effects. This results in an increase in dynamic on resistance. Rossetto et al. demonstrated the presence of hot electrons during hard switching by employing EL spectroscopy [80].
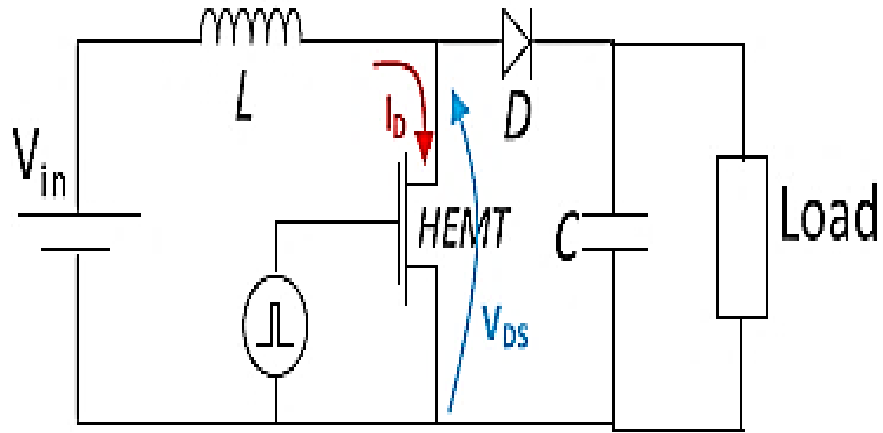
(a)
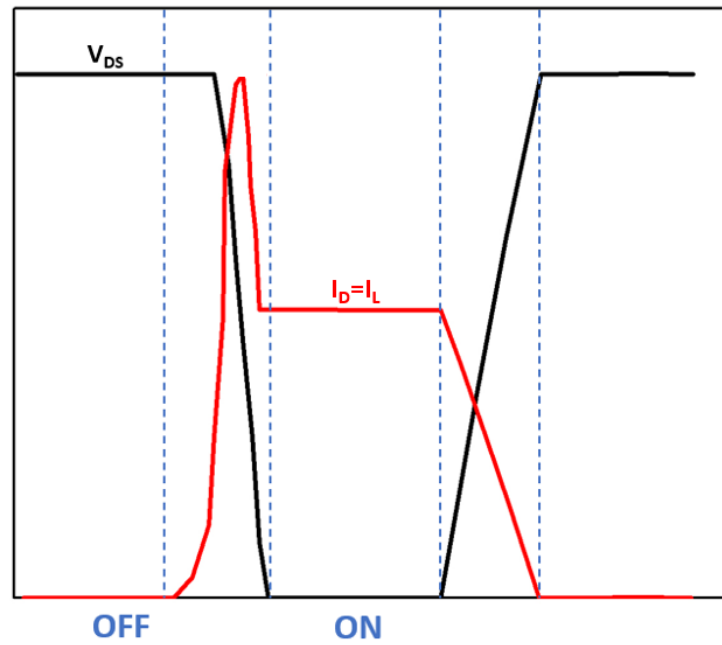
(b)

Figure 2-9: (a)Schematic of the boost converter. (b) V_{DS} and I_D variation during a switching event[80].

When measuring R_{ON} during hard switching, various factors such as time interval, drain current, and switching frequency becomes important to understand the variation of Ron which in turn depends on the number of injected carriers. When the bias voltage is raised, more active trap sites are created which facilitates the electron capture process raising the on resistance. Increasing temperature does increase the on resistance but this effect is more related to self-heating rather than hot electrons.

2.5.2 Soft Switching

In soft switching, switching control is done in such a way that the voltage and current are not high at the same time. The soft switching techniques are of two types: zero voltage switching (ZVS) and zero current switching (ZCS). To create such switching conditions, an initial delay between the drain and gate pulse is created which is called drain to gate delay (DGD). If DGD is negative, it means there is an overlap between the gate and drain pulse therefore it is hard switching. The more the negative value of DGD, the stronger the degree of hard switching. Similarly, if DGD is positive, then it is called soft switching. In soft switching, the switching losses are expected to be less compared to hard switching. Also, if the EL signal is compared for positive and negative DGD, it is evident that for negative DGD values, the EL pattern becomes stronger signifying the generation of hot carriers in the channel, whereas for positive DGD values EL signal is hardly noticeable (Figure 2-10)[80].
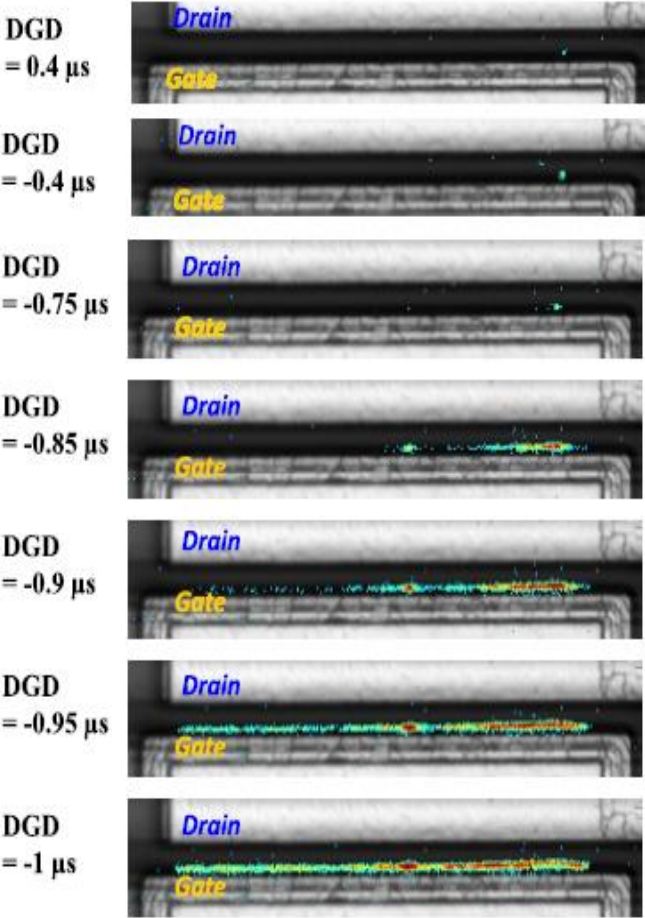
Figure 2- 10 : EL pattern with different DGD for hard and soft switching[80].

2.6 Conclusion

Two important reliability issues: device breakdown and hot electrons, in GaN HEMT transistors, have been explored in this chapter. Device breakdown occurs when the off-state leakage current crosses a particular value at which the breakdown voltage is calculated. Breakdown voltage can be improved by increasing gate-drain distance at the cost of increasing the on resistance. Hot electrons are generated in the semi-on state or the switching stage when the electric field is high. Hot electrons interact with pre-existing defects in GaN and change their charge state which degrade

device parameters such as V_{th} and g_m. Hot electrons also impact current collapse which is a persistent problem in GaN HEMT. Device lifetimes are calculated based on the failure of a particular device parameter, following Weibull distribution. Electroluminescence peak is an important technique used to identify the presence of hot electrons. Finally, two switching modes in GaN converters are discussed and compared in terms of hot electron degradation.

Chapter 3: Gate Leakage in GaN HEMTs

3.1 Introduction

Gate leakage current is an important parameter for GaN HEMTs since it limits the device performance. This leakage current is determined by the quality of gate contact formed between the metal and GaN. A Schottky contact is expected to be formed when a metal is deposited on top of the GaN layer. Despite this Schottky gate formation, a high amount of leakage current is reported at positive gate bias voltages [81][82][83][84]. Comparing to Silicon MOSFETs, the leakage current GaN HEMTs are significantly higher (by approximately four orders of magnitude) [85]. One major disadvantage of this high leakage current is that it can reduce the allowed gate voltage swing to avoid false turn-on problems in power converters having 2 GaN switching devices[86].In terms of device reliability as previously highlighted in the previous chapter, gate current has been used as a degradation parameter to develop lifetime acceleration models[64]. Additionally, gate current can be used to study forward gate breakdown which is then subsequently used to analyse time dependent gate breakdown mechanisms[21]. Therefore, understanding and modeling the leakage mechanism is important to the design and optimization of GaN HEMTs and there has been much work to characterize and model gate leakage current[82][84][87][88]. Various models have been used to interpret the data including Thermionic Emission (TE), Thermionic Field Emission (TFE), Poole Frenkel Emission (PFE), and Fowler-Nordheim Tunneling (FNT). When leakage is sufficiently small, models such as Trap Assisted Tunneling (TAT), Generation-Recombination(G-R), and two-dimensional variable range hopping (2D-VRH) have been invoked. In most cases, different mechanisms are proposed to model the behavior of different devices, including devices

fabricated by the same research group. In some cases, leakage at different gate bias voltages is modeled with different mechanisms, even at high bias[84][87][88].

3.2 Current through the Schottky contact

There are 3 main ways of carrier transport through the Schottky contact between the metal and semiconductor. For example, in the case of metal contact with pGaN, this process is depicted in Figure 3-1.
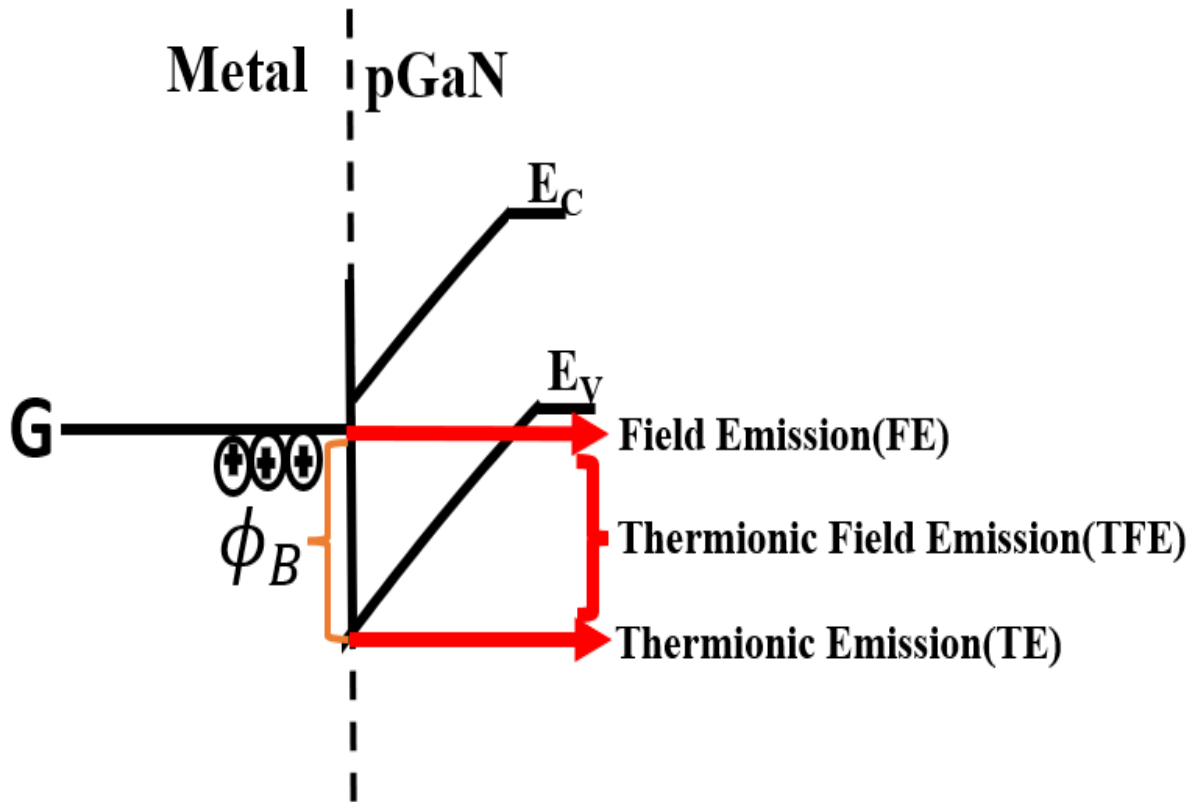
Figure 3-1: Carrier transport process in Schottky diode between metal and pGaN.

Thermionic emission implies that carriers gain sufficient energy to overcome the effective energy barrier to moving over to the other side of the junction. This energy barrier is known as the Schottky barrier height. Field emission refers to the tunneling of carriers through the forbidden gap of GaN. Thermionic Field Emission is the combination between the above two processes. Here, the holes in the case of metal/pGaN can tunnel above the valence band edge but do not have enough energy to overcome the Schottky barrier height. Each process is described below.

3.2.1 Thermionic Emission (TE)

As stated, earlier TE process requires carriers to have enough energy to overcome the energy barrier. This process is highly temperature dependent. The current density derived from the TE process is given by[89]

$$J_{TE} = J_S \left(\frac{eV_A}{nKT} - 1 \right) \tag{3.1}$$

where V_A is the applied voltage, K is the Boltzmann constant, n is the ideality factor and T is the absolute temperature. J_S is the reverse saturation current density given by

$$J_S = A^* T^2 e^{-q\phi_B/KT} . \tag{3.2}$$

Here, A^* represent Richardson's constant and ϕ_B is the Schottky barrier height.

3.2.2 Thermionic Field Emission (TFE)

In the TFE process, the tunneling occurs at an energy above the fermi-level (E_F). This process has a strong dependence both on temperature as well as the electric field. Since the Schottky diode is reverse biased during forward operation, only reverse TFE current density is being considered here, which is given by [89]

$$J_{TFE,r} = J_{s,TFE,r} e^{\frac{V}{\varepsilon'}}. \tag{3.3}$$

Here, V is applied forward bias voltage.

The reverse TFE saturation current is given by

$$J_{s,\text{TFE, r}} = \frac{A^* \cdot T^2 \cdot \sqrt{\pi E_{00}}}{V_t \cdot \cosh\left(E_{00}/V_t\right)} \cdot e^{-\frac{\phi_B}{E_0}} \cdot \sqrt{\phi_{Bn} - V \cdot \cosh^2\left(E_{00}/V_t\right)} \tag{3.4}$$

where,

$$E_0 = \frac{E_{00}}{\tanh\left(\frac{E_{00}}{V_t}\right)}, \tag{3.5}$$

$$E_{00} = \frac{h}{2}\sqrt{\frac{N_A}{m\varepsilon_s}}, \tag{3.6}$$

and

$$\varepsilon' = \frac{E_{00}}{E_{00}/V_t - \tanh\left(E_{00}/V_t\right)}. \tag{3.7}$$

Here, E_0, ε', and E_{00} are energy parameters associated with TFE model, A^* represent Richardson's constant, T is the absolute temperature, V_t is the thermal voltage, ε_s is dielectric constant of GaN, ϕ_B is Schottky barrier height, m is effective mass of holes, h is the Planck's constant, N_V is density of state in the valence band and N_A is the acceptor doping.

3.2.3 Field Emission (FE)

FE process has a very strong dependence on the electric field and weak temperature dependence. At high electric field, the potential barrier becomes narrower. This allows tunneling of carriers through the barrier by quantum mechanical tunneling. The shape of the barrier is important in

determining the amount of tunneling taking place. There are several categories of tunneling which are shown in Figure 3-2.
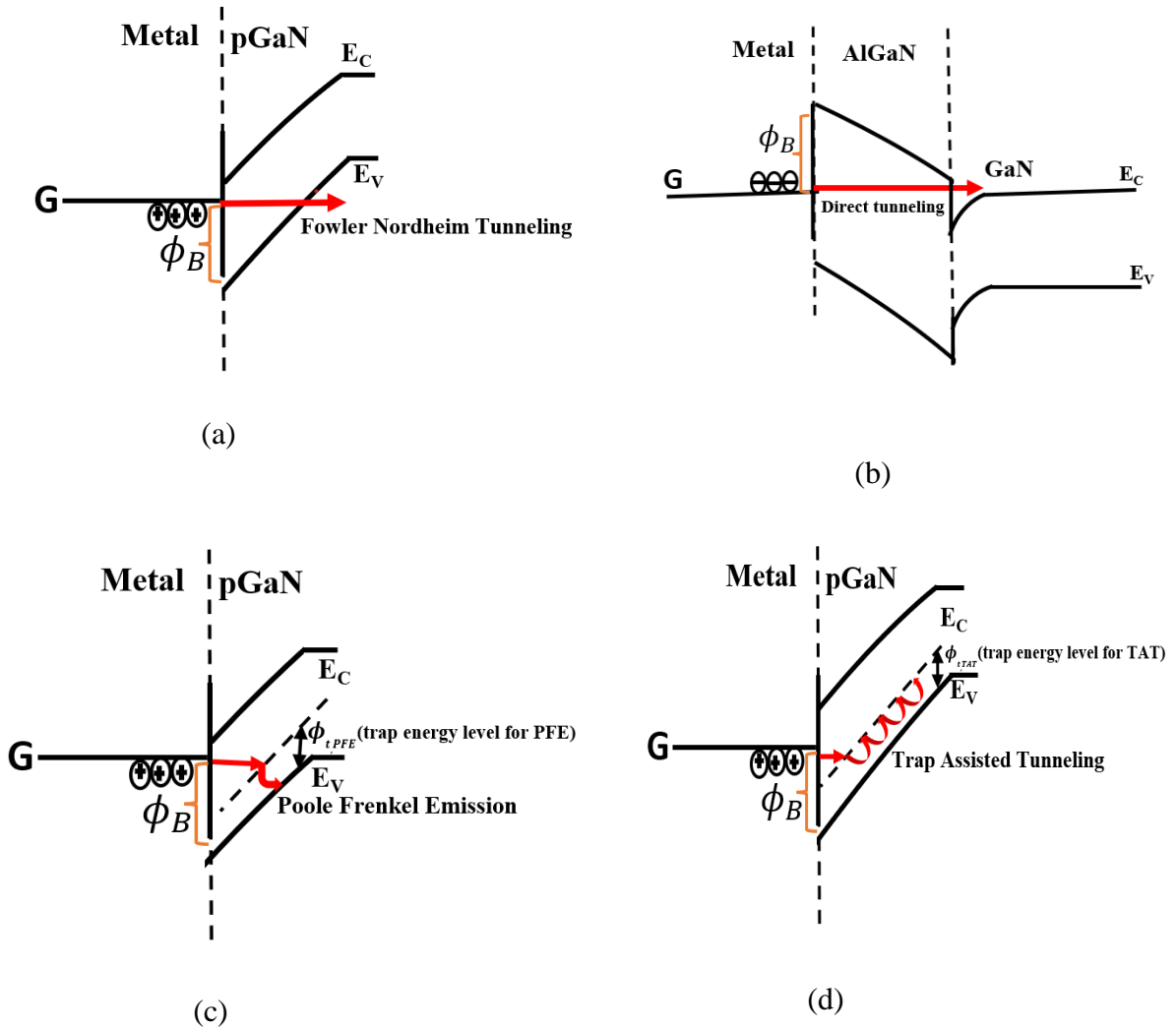
Figure 3-2: Schematic of different tunneling process:(a) Fowler Nordhiem Tunneling (b) Direct tunneling (c) Poole Frenkel Emission (d) Trap assisted tunneling.

3.2.3.1 Fowler-Nordhiem Tunneling

When potential is very narrow and has triangular shape at the presence of very high electric field, tunneling of carriers occurs via Fowler-Nordheim Tunneling (FNT) shown in figure 3.2(a). The current density from FNT is given by[90][91]

$$J_{FNT} = \frac{A}{\phi_B} E_{j,Sch}^2 exp\left(-\frac{B}{E_{j,Sch}} \phi_B^{3/2}\right)$$
(3.8)

where, A and B are FNT constants given below:

$$A = \frac{q^3}{8\pi h}$$
(3.9)

and

$$B = \frac{8\pi(2m^*)^{1/2}}{3qh}.$$
(3.10)

Here, $E_{j,Sch}$ is the electric field at the Schottky junction, ϕ_B is Schottky barrier height, m^* is effective mass of holes, h is the Planck's constant.

3.2.3.2 Direct Tunneling

As already state, the shape of the barrier is important in determining the choice of tunneling mechanism. So, if the depletion region is extended, barrier becomes wider. FNT is no longer valid in this case as the barrier shape is not triangular anymore. The carriers need to travel the entire width of the potential barrier which has a trapezoidal shape, hence direct tunneling takes place (Figure 3-2(b)). The direct tunneling current density is given by[91]:

$$J_{\text{DT}} = \frac{q^3}{16\pi^2\hbar\phi_b} \frac{1}{\left[1 - \sqrt{1 - \frac{qV_{j,Sch}}{\phi_b}}\right]^2} E_{j,Sch}^2 \tag{3.11}$$

$$\times \exp\left\{-\frac{4}{3}\frac{\sqrt{2m^*}\phi_b^{3/2}}{\hbar q E_{j,Sch}}\left[1 - \left(1 - \frac{qV_{j,Sch}}{\phi_b}\right)^{3/2}\right]\right\}$$

where $E_{j,Sch}$ is the electric field at the Schottky junction, is voltage drop across the Schottky junction, ϕ_B is Schottky barrier height, m^* is effective mass of holes and $\hbar$ is the reduced Planck's constant.

3.2.3.3 Poole Frenkel Emission

In Poole Frenkel Emission (PFE), the tunneling process occurs via trap at the presence of a large electric field. The tunneled carriers are initially trapped in localised trapped state characterised by a particular trap level ($\phi_{t,PFE}$). At high electric field, they have energy to break free from its localised state and move into valence band, for example if it is a hole trap. The PFE current density is given by [87]

$$J_{PFE} = CE_{j,Sch}\exp\left(-\frac{q\left(\phi_{t,PFE} - \beta\sqrt{E_{j,Sch}}\right)}{kT}\right) \tag{3.12}$$

where, C is constant associated with PFE and $\beta = \sqrt{q\pi/\varepsilon}$ is the Schottky factor.

3.2.3.4 Trap Assisted Tunneling

Traps aid carrier conduction through hopping mechanism and random fluctuation within an atom. It primarily occurs at low electric field. The TAT current density is given by [92]

$$J_{TAT} = C_1 exp\left(-\frac{C_2}{E_{j,Sch}} \varphi_{t,TAT}^{3/2}\right) \quad (3.13)$$

where, C_1 is a temperature dependent parameter, $E_{j,Sch}$ is the electric field at the Schottky junction,

$\varphi_{t,TAT}$ is the trap depth level measured from the top of valence band and C_2 is given by

$$C_2 = \frac{8\pi\sqrt{2qm^*}}{3h}. \quad (3.14)$$

3.3 Summary of previous gate leakage study

Since this thesis focuses mainly on pGaN-based HEMTs, the study of gate leakage in pGaN/AlGaN/GaN HEMTs from previous literature has been summarized. Table 3-1 looks at the modeling approach of some previous studies. All the previous models focus on a particular gate bias region and their assumptions for a particular mechanism are based on fitting experimental leakage characteristics for that particular gate bias region. So, we see authors propose a number of different modeling approaches to fit different region of gate bias.

Table 3-1:Summary of some of the previous gate leakage modeling work.

Author	Device Structure	Modelling approach
1. Xu (APL 113, 152104 (2018))	pGaN HEMT ($2x10^{19}$ cm^{-3} Mg doping),70 nm pGaN region, Palladium metal contact	2DVH (low FB), TFE (high FB)
	pGaN HEMT ($2x10^{19}$ cm^{-3} Mg doping),70 nm pGaN region, Titanium metal contact	2DVH (low FB), PFE (high FB)
2. Stockman (IEEE TED, 65.12 (2018): 5365-5372.)	pGaN HEMT ($1x10^{19}$ cm^{-3} Mg doping), gate metal not self aligned.	TE (up to 4V), TAT (more than 4 V)
	pGaN HEMT ($1x10^{19}$ cm^{-3} Mg doping), gate metal self aligned with an extra metal layer.	TE (up to 7V), PFE (more than 7 V)
3. Tapajna (APL 107, 193506 (2015))	pGaN HEMT ($2x10^{19}$ cm^{-3} Mg doping),95 nm pGaN region, Nickel contact	Field enhanced carrier generation-recombination process (low FB), PFE (high FB)
4. Wang (IEEE TED, VOL. 67, NO. 9, SEPTEMBER 2020)	pGaN HEMT ($1x10^{20}$ cm^{-3} Mg doping),60 nm pGaN region	TE model for all FB case.
5. Shi (IEEE ISPSD, 2018)	a commercial 650 V rated pGaN device	Ohmic (up to 1.4V), SCLC (from 1.4V to 5.5V), hole injection (more than 5.5 V).
6. Meneghesso (Bodo´s Power Systems, Aug 2018)	a commercial pGaN HEMT	TE (up to 4 V), TAT (more than 4 V)

There are a number of issues with previous efforts for modeling the gate leakage current. For example, each of the authors cited focuses on modeling 1-2 devices fabricated by them and makes no attempt at comparing with published data by other groups[82][84]. Even in cases where one research group fabricated two different devices, different mechanisms are invoked to explain the leakage behavior for the two different devices. This indicates that each "model" is a curve-fitting to the data of one specific device rather than a physically-based interpretation of the data.

Several models do not consider the split in voltage between the Schottky diode and the pin diode[81][82]. This means that the field dependence for the mechanism invoked is incorrect since the voltage used in the equations is not the actual voltage drop across the Schottky junction.

Several model selections are based on empirical fits i.e mostly no physical justification is given for the selection of a particular mechanism[82][84][87]. In particular[87], some of the models invoke mechanisms that do not correspond to the physical situation being studied. For example, invoking TAT for the high bias regime is in direct contradiction to the physical picture of the TAT conduction mechanism whereby surface traps are responsible for tunneling at low fields and the current has a weak dependence on the field.

Some studies do not model the full range of experimental measurements. For example,[84] provided experimental data up to a gate bias of 6V but only fit the "high bias" regime up to 1.1 V. Using the equations in the paper for higher bias would predict a sharp rise in the leakage current, not consistent with the device physics or the experimental data reported.

Several authors[81][87][88], while stating the physical mechanism used to model their data, do not provide sufficient detail to reproduce their work. Our best attempts to fit the data using the physical mechanisms invoked necessitated the use of different parameter values (e.g., different

barrier heights) at different bias voltages or temperatures. In such cases, the variation with temperature did not follow the expected physical dependence on temperature. In other cases, a consistent set of parameters could be used but the values of the parameters were far from what would be predicted by the device physics (e.g., predicting a very low Schottky barrier height whereas most metals on pGaN will have a Schottky barrier height greater than 1eV).

All these trends indicate that most of the modeling work in the literature appears to be empirical curve fitting rather than physically-based modeling. In the modeling work given in this thesis we have (a) invoked physical mechanisms that are consistent with the device physics; (b) used a consistent set of parameters (e.g. the Schottky barrier height for a given metal on GaN was kept constant across all devices using this metal, was bias independent, and depended on temperature only through the bandgap dependence on temperature); and (c) where possible, we made sure that the model parameters were consistent with known experimental values. The last point was difficult for the TAT model because we had no way of characterizing the interfaces for the different devices we modeled. However, our TAT parameters are consistent with published data for some defect levels in GaN. Similarly, there is a very wide spread of reported values for the Schottky barrier heights, and it is known that some barrier pinning occurs at the interface. However, the values we used were reasonably consistent with published experimental values. Because of its importance, this latter point is discussed in further detail towards the end of this chapter.

3.4 Experimental Characteristics of the modeled devices

We have studied 5 devices for which detailed data have been published [81]-[84].These 5 devices will be used for modeling and simulations in the subsequent chapters that follows. All five devices are based on GaN on Si epitaxy substrates grown via metal organic chemical vapor deposition (MOCVD). The basic structure common to these devices is schematically illustrated in figure 3-3.
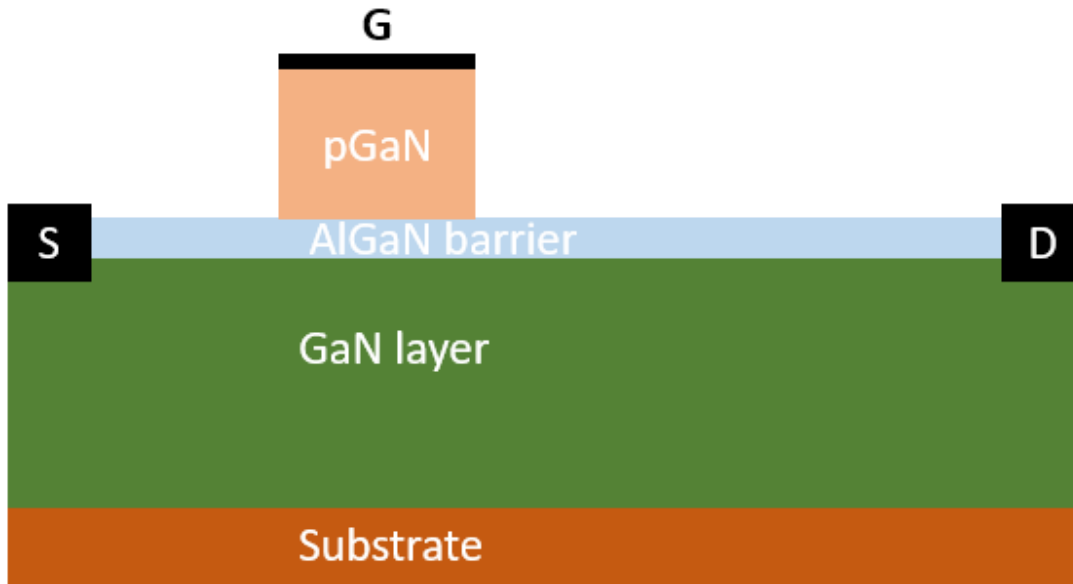
Figure 3-3: Schematic of a conventional pGaN HEMT.

Device 1 has a superlattice buffer structure with 1 μm C-doped back barrier [81] while device 2[82] has a 4.5 μm Fe-dopped GaN buffer layer and the buffer layer in Device 3[83] is 4.7 μm. Devices 4 and 5 [84] have a C-doped buffer layer of 4.35 μm. On top of this buffer layer, there is a very thin $Al_xGa_{1-x}N$ barrier layer responsible for 2DEG formation. Here, x is the mole fraction which varies from 15% to 25% among the 5 devices. The thickness of the AlGaN layer is 12.5 nm for device 1, 15 nm for device 2, 25 nm for device 3, and 18 nm for devices 4 and 5. A GaN cap layer grown epitaxially on top of the barrier layer is p-type doped with Magnesium (Mg) ions. The

doping concentration (N_A) is 2.7×10^{19} cm^{-3} for device 1 while devices 2,3,4 and 5 have a doping

of 2×10^{19} cm^{-3}. The p-type cap layer is responsible for the normally OFF operation of the device.

The reported gate lengths (L_g) are 1.5 μm for device 1, 1.3 μm for device 2, 0.8 μm for device 3

and 2 μm for devices 4 and 5. Device 5 has a silicon nitride passivation ring around the gate region.

In device 3, there is an additional p type GaN layer present near the drain electrode to improve

upon the current collapse effect. The contact metals are Titanium Nitride (TiN) for device 1, Nickel

(Ni) for device 2, Palladium (Pd) for devices 3 and 4, and Titanium (Ti) for device 5. Table 3-2

summarizes the device structures.

Table 3-2:Summary of the device specifications used for gate leakage modeling.

Dev No.	Gate Length (μm)	Gate Width (μm)	AlGaN thickness (nm)	pGaN thickness (nm)	pGaN Doping (cm^{-3})	Gate Metal Contact	Reference
1	1.5	100	12.5	80	2.7×10^{19}	TiN	[81]
2	1.3	250	15	95	2×10^{19}	Ni	[82]
3	0.8	200	25	100	2×10^{19}	Pd	[83]
4	2	100	18	70	2×10^{19}	Pd	[84]
5	2	100	18	70	2×10^{19}	Ti	[84]

The reported gate leakage data for the 5 devices at room temperature are shown in Figure 3-4(a).

It is clear that the Schottky barrier height (ϕ_B) is the most significant factor in determining the

gate leakage current (I_G). The data show that the dependence on other factors is considerably less significant. For example, Devices 3 and 4 were fabricated by two different groups and have different dimensions as well as different thicknesses for both the AlGaN and GaN layers but have the same contact metal (Pd) and display leakage behaviors that are very similar, whereas device 5, fabricated by the same group as device 4 and reported in the same study, only differs in the contact metal used (Ti) and consequently has a markedly different behavior. Similarly, devices 1 and 5 have contact metals with similar work functions, and consequently similar leakage behavior despite other differences in doping and device structure. The second trend observed from the experimental data is that for some devices, as the gate bias decreases, the leakage current appears to flatten out. This is consistent with the expected physical picture of a different leakage mechanism making a contribution at low bias, as we discuss in the modeling section. Finally, Figure 3-4(b) shows the temperature dependence of I_G for devices 2,4 and 5. We note that I_G is less sensitive to temperature at high bias, indicating that the dominant leakage mechanism at high bias is not primarily a thermally activated process such as thermionic emission.
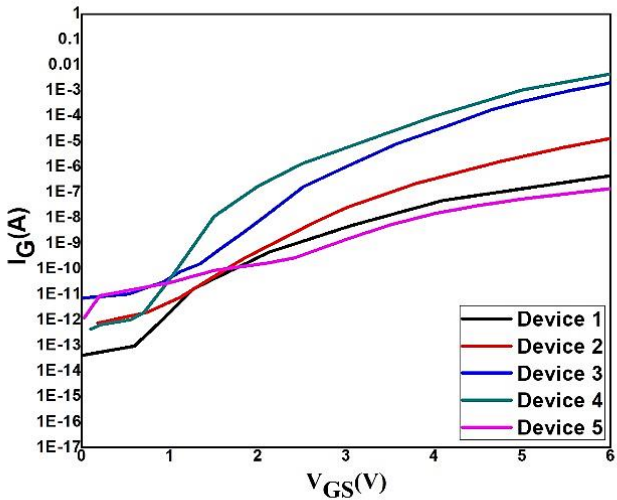
(a)
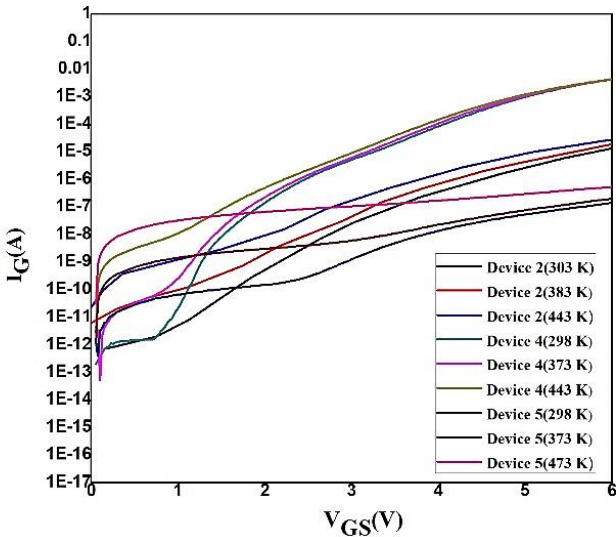
(b)

Figure 3-4: (a) Experimental gate leakage plot of the devices (1~5) at room temperature (b) Gate leakage plot of devices 2,4 and 5 at various temperatures. The plots were extracted from reference[81][82][83][84].

3.5 Importance of Schottky barrier height on gate leakage modeling in pGaN/AlGaN/GaN HEMTs

The most important of the fitting parameters in modeling gate leakage is the Schottky barrier height (SBH). We examined the literature for data on SBH for metals on pGaN. SBH can be studied using spectroscopy[96] but in most of the published work, SBH is usually extracted from IV or CV measurements. In those studies, the assignment of a value to the SBH depends entirely on the assumed conduction mechanism. Thermionic and field emission mechanisms (TE, FE, TFE) as well as several tunneling mechanisms (direct band-to-band, Poole-Frenkel, and Fowler-Nordheim) all depend on SBH. For a given structure, one of these mechanisms is likely to be dominant and the dependence of the leakage current on the SBH will have a given form. For example, Reference [88] extracts two very different values (0.8 eV and 1.9 eV) for TiN on pGaN assuming two different mechanisms. Similarly, for Ni/pGaN contact, one group reported ϕ_B to be 0.57 eV assuming conduction via Thermionic Emission (TE) [97] while in another study another group reported ϕ_B to be 1.07 eV extracted from Thermionic Field Emission (TFE) [100]. Table 3-3 summarizes some of the reported values of ϕ_B from previous experimental studies available in the literature ([88][96]-[104]) and the corresponding assumptions used for ϕ_B calculation. This makes the extraction of a specific value for SBH highly dependent on the assumptions about leakage mechanism.

Table 3-3: Report values of ϕ_B for pGaN/metal contacts

Metal on pGaN contact	Reported Φ_B (eV)	Methods used in ΦB extraction
TiN	0.8	TE
	1.9	FNT
Ni	0.57	TE
	1.07	TFE
Pd	0.51	TE
	1.82	FNT
Ti	0.65	TE
	2.08	TFE

The Figure 3-5 below demonstrates the wide range of published values for ϕ_B. We have strong reservations about the low end of these measurements and believe most of them to be incorrect due to wrong assumptions about conduction mechanism. We restricted ourselves to keep the values of ϕ_B used in our work to have a linear dependence on work function [Schottky-Mott relation] and to be closer to the higher values in the range and excluded the lowest values.
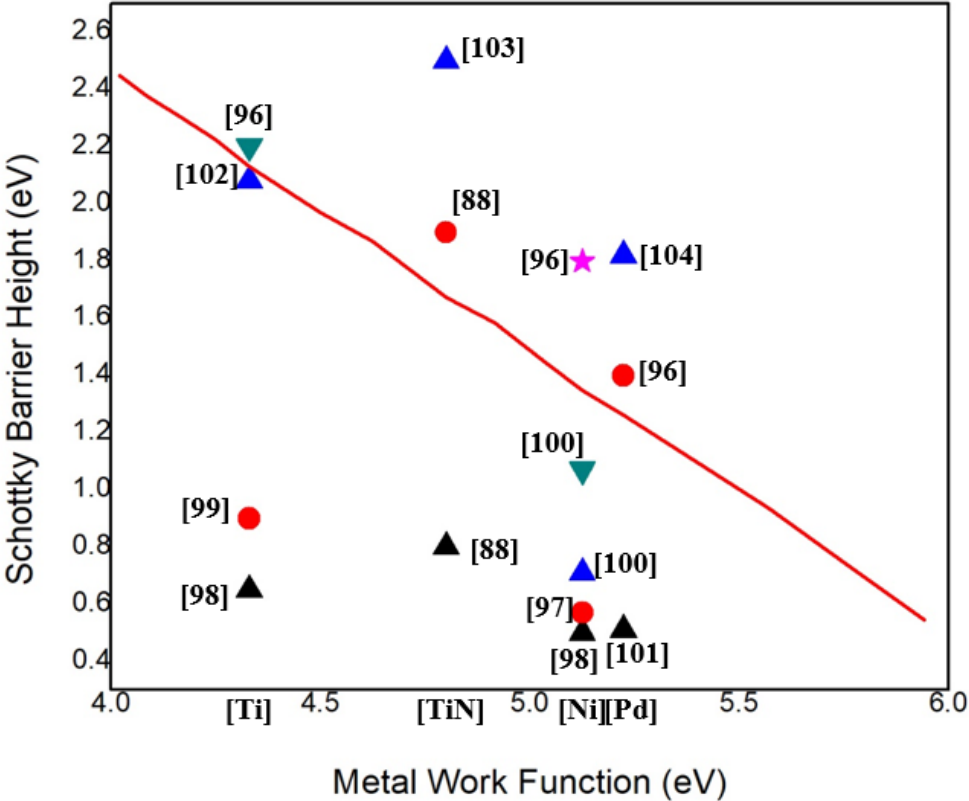
Figure 3-5: Experimental Schottky barrier height (ϕ_B) of different metals on pGaN from literature ([88][96]-[104]).The symbol represent the experiment values.The red line indicate theoretical value of ϕ_B with different metal work-function obtained from Schottky-Mott relation. The metals are enlisted on x-axis of the above curve according to their work function.

3.6 Conclusion

In this chapter, we have surveyed the gate leakage process in GaN HEMTs. The leakage process can be broadly categorized into three physical mechanisms: Thermionic emission (TE), Thermionic Field Emission (TFE), and Field Emission (FE). FE can be further categorized into

Fowler-Nordhiem tunneling (FNT), Direct tunneling (DT), Poole Frenkel (PFE), and Trap assisted tunneling (TAT). We have summarized some of the previous models that have been implemented to model leakage in pGaN HEMTs and enlisted some of the pending issues associated with the model proposed. Finally, we have explained in detail the experimental gate leakage characteristics of the 5 devices that will be modeled and simulated in the subsequent chapters. From the experimental observations, it was found that the Schottky barrier is very important in the gate leakage process since it controls the magnitude of leakage current.

Chapter 4: Modeling of forward gate leakage current for normally off pGaN/AlGaN/GaN HEMTs

4.1 Introduction

In this chapter, we provide a model for gate leakage in pGaN HEMTs that fits published data for multiple devices fabricated by multiple research groups. The published data for all the devices may be explained assuming that leakage occurs primarily via Fowler-Nordheim tunneling (FNT), which is consistent with the expected triangular barrier between the metals used and pGaN. We are able to fit the published data assuming Schottky barrier heights (SBH) consistent with published experimental values. In fitting the leakage data to the expected FNT current, we must take into account the split in applied voltage between the reverse-biased Schottky contact and the forward-biased pin diode in the pGaN HEMT gate stack. Previously published studies that ignore the voltage drop across the pin diode consistently over-estimate the leakage current (or use values for SBH that are much lower than expected from either theory or experiment).

At moderate and high bias, FNT completely accounts for the leakage current. However, for most of the devices, FNT underestimates the leakage at low gate bias. This indicates that some additional mechanism must be in operation. We do not have sufficient experimental data to fully determine this mechanism, but we find that trap assisted tunneling (TAT) may be used to adequately fit the given data. One key limitation of our model is that we have ignored the effect of series resistance. This results in poor fits for two of the devices at room temperature. In those cases, FNT alone overestimates the leakage at low gate bias because the assumed value of voltage drop across the Schottky junction is too large.

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The chapter is organized as follows. In Section 2, we present the numerical model. In Section 3, we report and discuss our results, including the parameters used. Section 4 is the conclusion.

4.2 Modeling the Gate Leakage

The vertical structure of the pGaN HEMT may be modeled as a Schottky diode in series with a p-i-n diode, as shown in Figure 4-1.
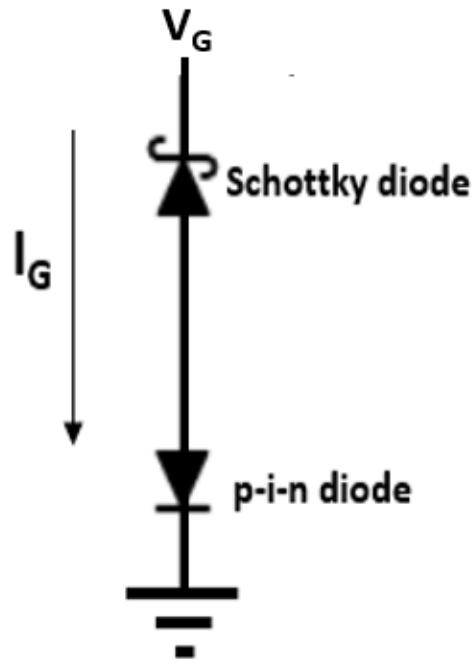
Figure 4-1 : Schematic of the vertical pGaN/AlGaN/GaN structure.

Under positive gate bias, the Schottky diode is reverse-biased whereas the p-i-n diode is forward biased. The band diagram of the pGaN/AlGaN/GaN is shown below in Figure 4-2. At zero bias, the conduction band edge is far away from fermi level, hence no 2DEG is present causing normally off operation. It is observed that when a positive gate voltage is applied, the conduction band edge moves closer to fermi-level and 2DEG is formed at the AlGaN/GaN interface
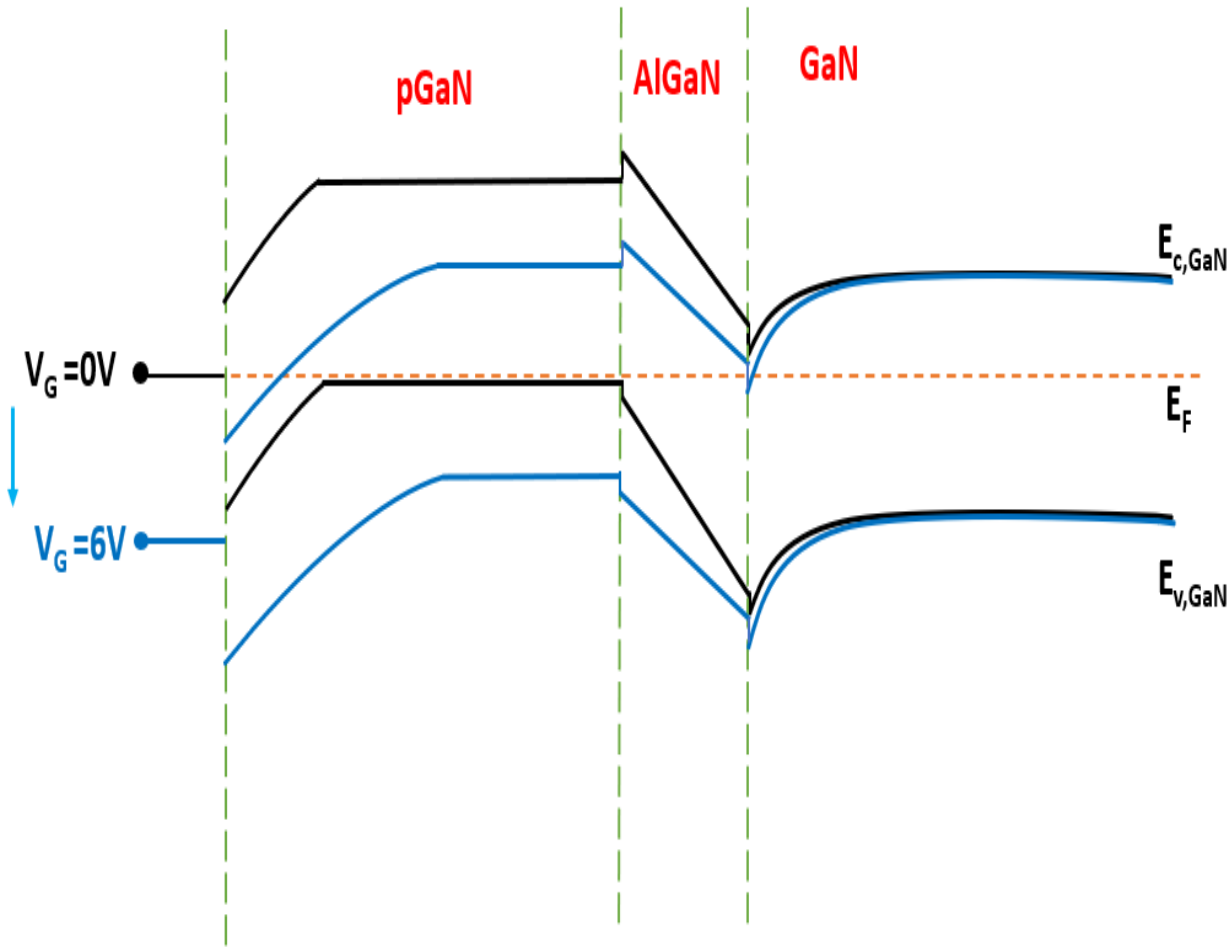
Figure 4-2 :Band diagram at V$_G$=0 V and V$_G$=6 V.

We may write:

$$V_{GS} = V_{pGaN} + V_{pin} \tag{4.1}$$

where V_{GS} is the applied gate bias voltage, V_{pGaN} is the reverse bias across the Schottky junction, and V_{pin} is the total forward drop across the p-i-n structure. Ignoring series resistance,

$$V_{pin} = nV_T ln\left\{\frac{I_G}{I_S} + 1\right\} \quad\quad (4.2)$$

where n is the ideality factor, V_T is the thermal voltage, I_G is the gate leakage current, and I_S is the saturation current of the p-i-n diode.

We suggest that the leakage is dominated by Fowler-Nordheim tunneling (FNT) since, for the metal/pGaN structure with typical parameters (barrier height and semiconductor doping), a thin triangular barrier would be expected consistent with the assumptions of the FNT mechanism as shown in Figure 4-3[91][105]. However, at low bias, the FNT contribution would decrease very rapidly, and the role of surface traps becomes important. Therefore, for some devices we expect trap assisted tunneling (TAT) to become important as shown in Figure 4-4 and cause the leakage current to flatten at low gate voltages. This picture of the tunneling current is consistent with the data at room temperature as well as the different dependence on temperature at low and high bias: TAT would be more sensitive to temperature than FNT. Given this, we write,

$$I_G = I_{TAT} + I_{FNT.} \quad\quad (4.3)$$

The two current components are given by [91][92],

$$I_{TAT} = A_c C_1 exp\left(-\frac{C_2}{E_{j,Sch}}\, \varphi_t^{3/2}\right) \quad\quad (4.4)$$

and

$$I_{FNT} = \frac{A_c A}{\phi_B} E_{j,Sch}^{\,2} exp\left(-\frac{B}{E_{j,Sch}}\, \phi_B^{3/2}\right) \quad\quad (4.5)$$

where A_C is the contact area, C_1 is a parameter dependent on temperature, C_2 is given by [92],

$$C_2 = \frac{8\pi\sqrt{2qm^*}}{3h} \tag{4.6}$$

m^* is the effective mass for holes in the pGaN, h is Planck's constant, q is the electronic charge, ϕ_t is the trap depth level measured from the top of valence band. The value of ϕ_t is used as a fitting parameter in this modeling study and is kept constant at 0.1 eV. ϕ_B is the hole barrier height. A and B are the FNT constants given by[92],

$$A = \frac{q^3}{8\pi h} \tag{4.7}$$

and

$$B = \frac{8\pi(2m^*)^{1/2}}{3qh} \tag{4.8}$$

and $E_{j,Sch}$ is the electric field across the Schottky junction is given by,

$$E_{j,Sch} = \sqrt{\frac{2qN_A}{\varepsilon_{GaN}}(V_{pGaN} + V_{bi})} \tag{4.9}$$

where V_{bi} is the built-in voltage of the Schottky junction, N_A is doping in the pGaN layer and ε_{GaN} is the GaN dielectric constant. The built-in voltage (V_{bi}) is given by

$$qV_{bi} = \phi_B - kT\ln\left(\frac{N_v}{N_A}\right) \cong \phi_B. \tag{4.10}$$

This value will be approximately equal to the Schottky barrier height since the fermi level in the pGaN layer is very close to the valence band edge.

Finally, substituting (4.2) into (4.1) gives an expression for V_{pGaN} in terms of I_G. Substituting that

expression, together with (4.4) and (4.5) into (4.3) yields an equation that may be solved iteratively

to yield I_G for a given value of V_{GS}. This simulation is performed in MATLAB (code is given in

Appendix A).
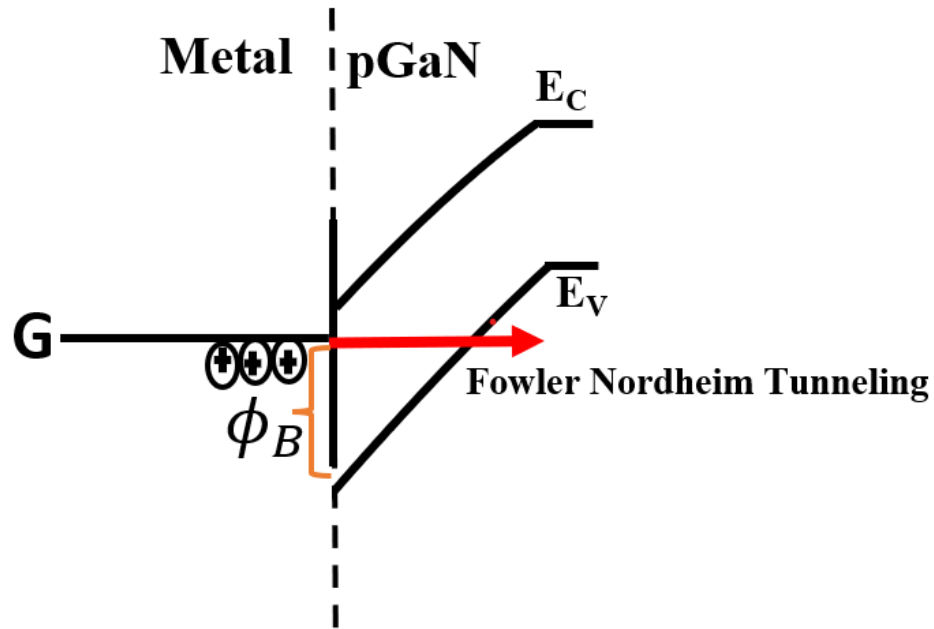
Figure 4-3: Schematic diagram of FNT process.
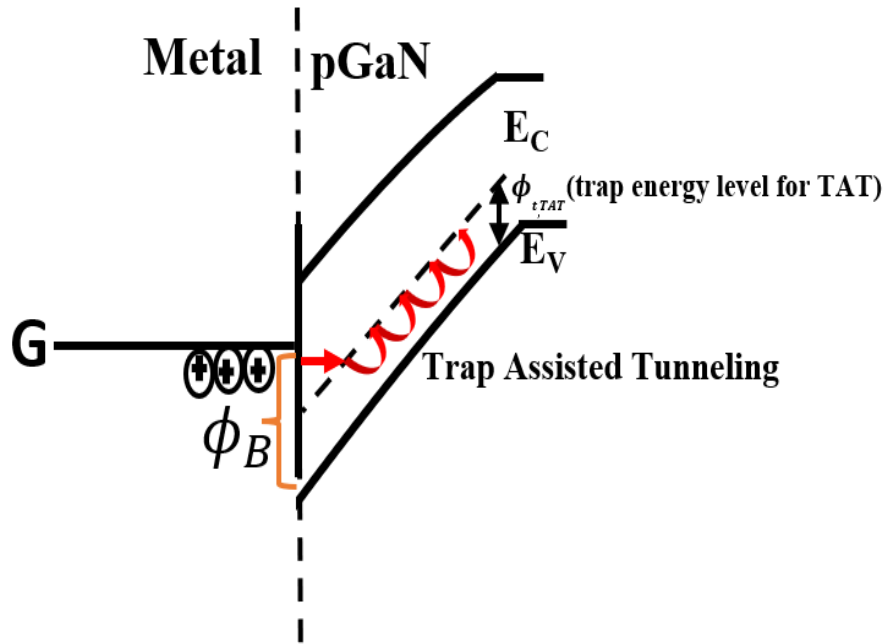
Figure 4-4: Schematic diagram of TAT process.

4.3 Results and Discussion

The model results for all 5 devices are shown in Figure 4-5 for room temperature. Figure 4-6 demonstrates the calculated contribution of each of the two mechanisms (TAT and FNT). Table 4-1 shows the constant parameters applicable to all devices at room temperature. The temperature dependence is shown in Figure 4-7 for devices 2, 4 and 5 (the only ones for which data is available). The calculated contributions of the two current components as a function of temperature are shown in Figure 4-8.

Table 4-1:List of constant model parameters at room temperature.

Parameter	Description	Values	Units
n	Ideality factor of the forward pin diode	1	--
k	Boltzmann constant	1.38×10^{-23}	J/K
ε_{GaN}	Relative dielectric constant of GaN	9.5	--
m^*	Effective mass of holes	$0.8 \times 9.11 \times 10^{-31}$	kg
I_s	Diode saturation current	1×10^{-13}	A
ϕ_t	Trap Energy	0.1	eV
V_{bi}	The built-in voltage at the metal/pGaN junction	1.2-1.75	V
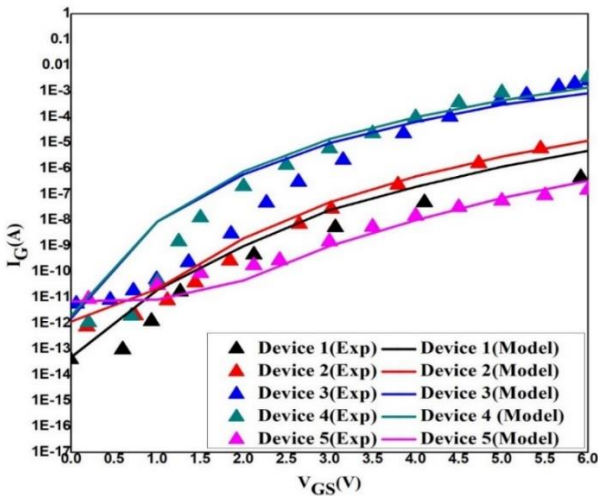
Figure 4-5: Comparison of the model to the experimental data for the gate leakage current at room temperature of all 5 devices. The experimental data for the above plot has been extracted from references[81][82][83][84].
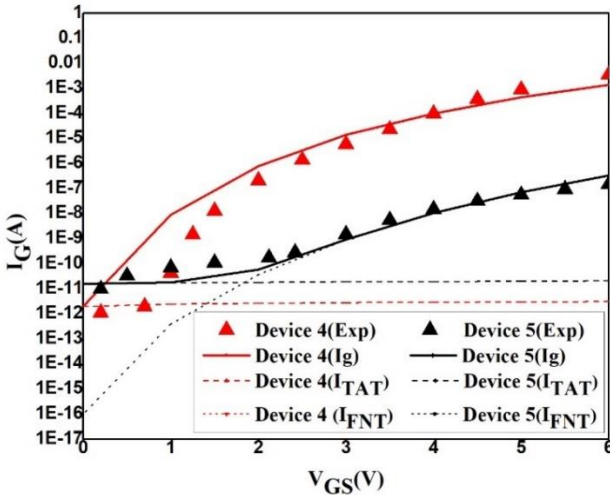
Figure 4-6:Gate current model with TAT and FNT components for devices 4 and 5. The experimental data for the above plot has been extracted from reference[84].
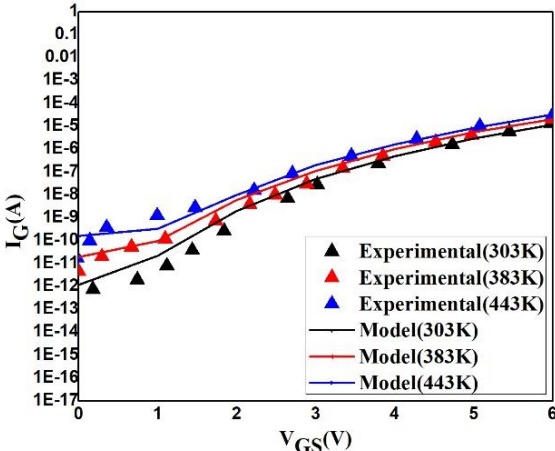
(a)
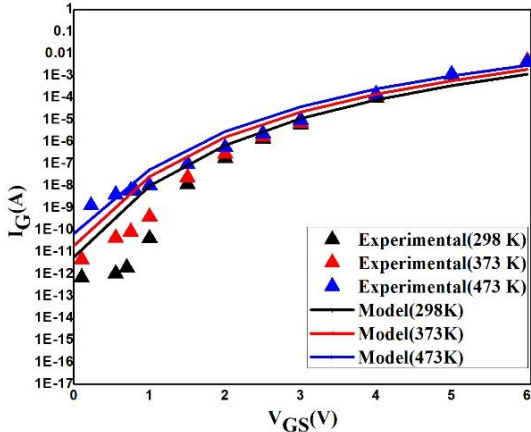
(b)
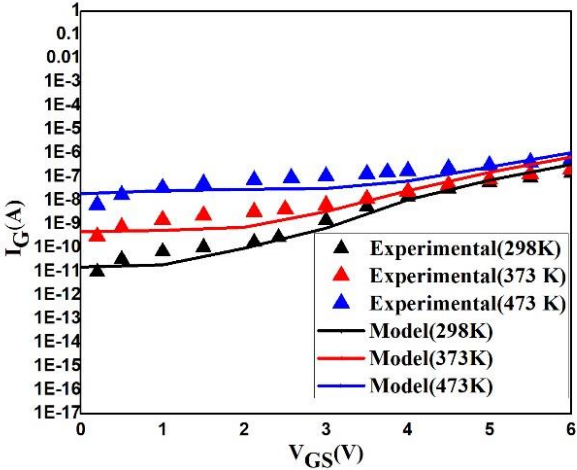
(c)

Figure 4-7: Comparison of the developed model to the experimental data for the gate leakage characteristics at different temperatures for 3 devices (2,4 and 5) listed from (a)-(c). The experimental data for the above plot has been extracted from reference[82][84].
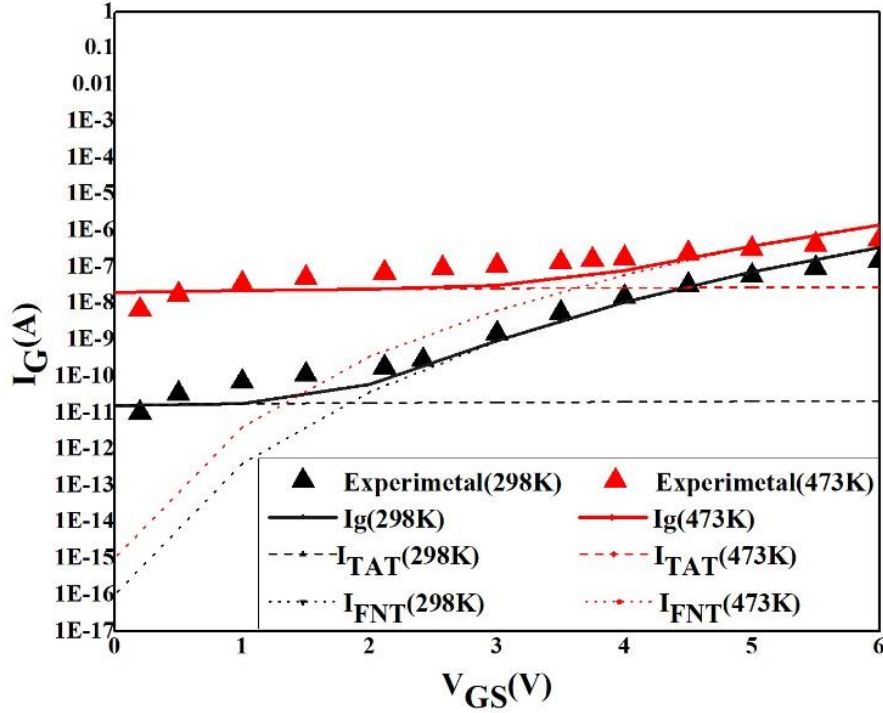
Figure 4-8: Gate current model with TAT and FNT components for device 5 at two different temperatures. The experimental data for the above plot has been extracted from reference[84].

As shown in equation (4.1), an important aspect of modeling the relationship between the leakage current and gate bias is the voltage division between the Schottky diode and the pin diode. The important parameters to calculate V_{pin} are I_S and n. These values depend on a number of factors including the device area, doping concentration, intrinsic layer thickness, etc. In this study, we found that a value of $I_S = 1 \times 10^{-13}$ A may be used for all five devices at room temperature. This is consistent with other studies (see, e.g., [106], taking into account the different device areas). At room temperature, the fit is not very sensitive to the value of I_S as long as it is on this order of magnitude. A lower value leads to unphysical results where the pin diode drop is higher than the applied gate bias. A value that is 1-2 orders of magnitude higher would predict a pin voltage drop

that is too low, leading to an over estimation of the leakage current. I_S is thermally activated, with the activation energy determined by the dominant carrier generation processes in the device. An activation energy of about 0.1eV was found in [106]. The values that gave us the best fit are shown in Table 4-2 and they show an activation energy of $\approx$0.3eV. The ideality factor (n) is taken to be 1 for both room temperature as well for high temperature calculations.

Table 4-2: List of values of I_S varied for different temperature for devices 2,4 and 5.

Device number	Temperature(K)	Values (A)
Device 2	303	1×10^{-13}
	383	1×10^{-12}
	443	8×10^{-12}
Device 4	298	1×10^{-13}
	373	1×10^{-12}
	473	2×10^{-11}
Device 5	298	1×10^{-13}
	373	4×10^{-12}
	473	5×10^{-11}

As we have already noted, the Schottky barrier height (ϕ_B) is very important for analyzing gate leakage current based on the experimental trends for these devices. The Schottky barrier height is dependent on the metal work function. The Schottky-Mott relation gives [$\phi_B(T) = E_g(T) + \chi - \phi_M$], where $E_g(T)$ is the bandgap at a particular temperature(T), χ is the electron affinity of the semiconductor and ϕ_M is the work function of the metal [107]. Schottky barrier height is generally extracted from experimental results. The extracted experimental values of ϕ_B tend to be smaller than the theoretical values. This reduction in ϕ_B is due to the fermi level pinning arising from surface states. In this study, we have used ϕ_B as a fitting parameter but the values we obtained are close to the experimental values of from previous studies[88][96][102][103]. Also, we used the same value of ϕ_B for multiple devices using the same metal contact. The values of ϕ_B used in this work are reported in Table 4-3. The temperature dependence of ϕ_B is solely due to bandgap narrowing in accordance with the Schottky-Mott relation. The bandgap of GaN at a particular temperature(T) can be calculated from Varshni empirical equation [$E_g(T) = E_g(0) - \alpha T^2/(\beta + T)$], where α and β are Varshni coefficients[108][109]. The value of α and β were 0.89 meV/K and 819 K respectively. We used our extracted values at room temperature together with these two equations to determine ϕ_B at higher temperatures.

Table 4-3: The value of Schottky barrier height (ϕ_B) for different gate metals used for this work.

Metals	ϕ_B (eV)	Experimental ϕ_B (eV) from literature	Reference
TiN	1.74	1.9 – 2.5	[88][103]
Ni	1.54	1.8	[96]
Pd	1.2	1.4	[96]
Ti	1.75	2.08 – 2.2	[96][102]

From Figure 4-5, it is clear that ϕ_B is the main determinant of leakage current (I_G) at high bias. Lower ϕ_B gives higher I_G. The gate currents from all these 5 devices are strongly dependent on the gate bias, so a field dependent mechanism like FNT is consistent with the experimental trend. The FNT current is very much dependent on ϕ_B as seen from equation (4.5). Devices 3 & 4 have Pd contact where we observe I_G to be quite high and the FNT current dominates almost the whole bias range. Conversely for devices 1 and 5 with high ϕ_B, the FNT current is expected to be low at high bias. From Figure 4-7, we see that I_G at high bias has a weak temperature dependence, another trend consistent with the FNT mechanism.
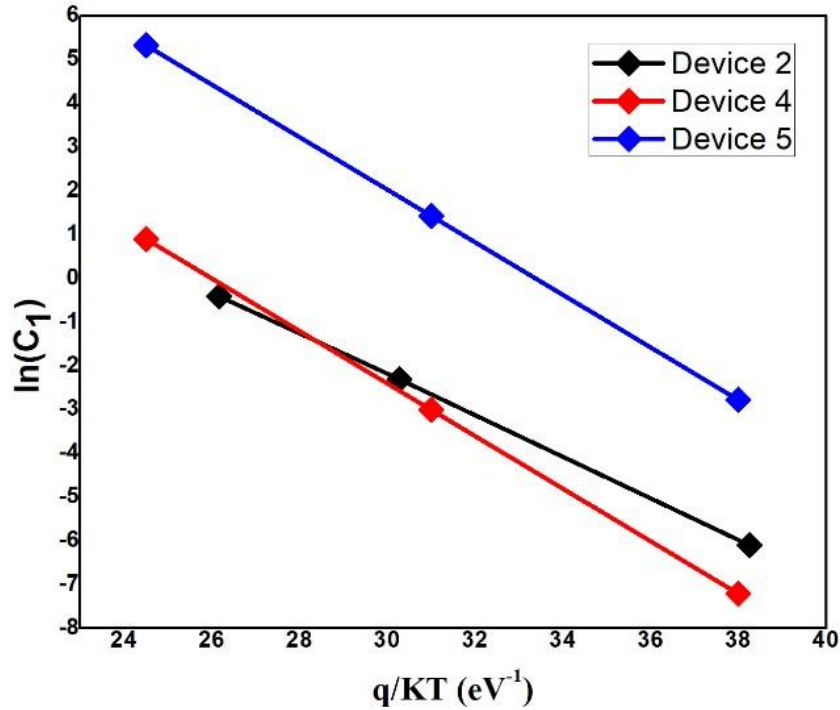
Figure 4-9: Variation of the C_1(log scale) with temperature for device 2,4 and 5.

For some devices such as device 2 at low bias, FNT mechanism underestimates I_G. This implies that some other process must also be present, but it only significantly contributes at low bias where the FNT component is negligible. The TAT component becomes dominant in this region. The TAT current which has a strong temperature dependence, fits the experimental data at low bias. In the TAT current equation, the parameter C_1 is a temperature dependent fitting parameter. This parameter is related to trap density and capture rate and, therefore, the quality of the interface. In our model, we have expressed C_1 as a thermally activated parameter, $[C_1 = C_{1\_0} exp(-V_0/V_T)]$. The values of C_1 at room temperature are $3.3x10^{-4}$(device 1), $3x10^{-3}$((device 2), $6.7x10^{-4}$ (devices 3 and 4) and 0.06 (device 5). The trap energy (ϕ_t) is kept constant at 0.1 eV for all the devices at

all temperatures. Since TAT is sensitive to temperature variation, C_1 increases with temperature which is shown in Figure 4-9. The activation energy, V_0, is 0.47 V for device 2 and 0.6 V for devices 4 and 5. Particularly, in the case of device 5 we observe that at moderate and high bias the leakage is much smaller than the other devices, which is due to the larger barrier height, but at low bias it has higher leakage which must be due to surface states.

Finally, a note on the limitations and the significance of this work. There are three significant limitations in this work: ignoring series resistance, the modeling of the p-i-n diode and using C1 in the TAT model as a fitting parameter. These are necessary in the absence of experimental data to calibrate the individual devices, determine diode parameters, and determine the concentration and energy level of surface traps. These limitations are most significant in the low bias regime. While the quality of fit is excellent for most of the devices, there is a clear discrepancy for device 4 in the low bias region.

Despite these limitations, this work demonstrates that a single, simple model, with a consistent set of parameters is sufficient to model a wide range of published data. This is remarkable given previous work in modeling gate leakage in pGaN HEMTs. Previous studies invoked thermionic emission (TE), thermionic field emission (TFE), and Poole Frenkel emission (PF), in addition to the FNT and TAT contributions that we have invoked in this study to explain very limited data. In some cases, some of these mechanisms were invoked in bias regimes where they are unlikely to dominate (e.g., invoking the TAT for high gate bias). In almost all cases, a different combination of models is invoked for each device, even when the devices are fabricated by the same research group and there is no physical justification for the model combination beyond the empirical fit to the data. We do not claim in this work to have proven that all gate leakage in pGaN HEMTs occurs by FNT or to have disproven other competing models. But we have demonstrated that the data do

not justify the existing modeling complexity. The gate leakage behavior that has been consistently observed and reported for pGaN HEMTs fabricated by many different groups with different geometries, doping, contact metal, and some variation in process steps (e.g. passivation) is all consistent with conduction primarily by FNT, controlled almost entirely by the Schottky barrier height, with some contributions at low bias (below the threshold voltage of the device) from some mechanism controlled by surface traps.

4.4 Conclusion

In this work, we have developed a numerical model to study the gate leakage behavior of pGaN HEMTs. We have studied the gate leakage characteristics of five different devices from four different groups. Leakage appears to be dominated in all cases by Fowler-Nordheim tunneling (FNT) and controlled almost entirely by the Schottky barrier height. In some cases, an additional leakage component is present at low bias, below the threshold voltage of the HEMT. This component is more sensitive to temperature. We have modeled it by trap assisted tunneling (TAT) with the trap level and density used as fitting parameters.

Chapter 5: Analysis of the forward gate leakage current in pGaN/AlGaN/GaN HEMTs through TCAD simulations

5.1 Introduction

Technology Computer-Aided Design (TCAD) simulation is a valuable tool to examine numerous reliability issues in semiconductor devices. In standard AlGaN/GaN HEMT devices, it has been extensively used to understand different reliability issues such as current collapse [110], gate lag [111], and drain lag [112]. One of the phenomena that have been studied through TCAD simulations is the gate leakage current [113]. While this has been extensively studied in conventional MOS devices[114][115][116][117], there are only a few studies for pGaN HEMTs[118][119]. TCAD simulations help in a better understanding of the device structure which can be optimized for the development of future GaN HEMT technologies.

In this chapter, TCAD simulations are used to model the published experimental data of I_G for the same published data from the previous chapter. These data were for 5 devices from 4 different research groups (the same devices studied in the previous chapter) and showed the gate leakage current as a function of gate bias and temperature. Similar to our numerical modeling study from the previous chapter, TCAD simulations show that gate leakage can be explained by Fowler-Nordheim Tunneling (FNT) and Trap Assisted Tunneling (TAT) mechanisms.

TCAD simulation is performed by solving Poisson's equation in conjunction with continuity equations for holes and electrons. In discretizing the device structure and numerically solving the equations in discrete time steps, we are able to take into account the properties of the materials throughout the device structure and solve the full equations describing the device without having

to make approximations (such as using the diode equation) required to simplify the equations. This will, for example, take into account the effect of series resistance automatically. The end result is to compute the electric field distribution throughout the device structure with greater accuracy than would be obtained from a compact model, and thus the simulated leakage current is expected to be more precise than the numerical model [120].

This chapter is summarised as follows: In section 2, we set up the TCAD environment by simulating typical I_D-Vg characteristics of the pGaN/AlGaN/GaN HEMT and defining the model parameters used in this study. In Section 3, we explain the gate leakage mechanism. Section 4 contains the results and discussion of gate leakage TCAD simulations. Section 5 is the conclusion.

5.2 TCAD Simulation setup and calibration

All the simulations performed in this work were done in Sentaurus TCAD[121], which is a suite of tools allowing process and device simulation based on physical models. While the models are physically-based and have been calibrated against extensive data in the literature, it remains a challenge in simulating a particular device structure to select the physical models appropriate to the particular device and to calibrate the model parameters. With the wide range of models and the number of model parameters available in Sentaurus, it is entirely possible to obtain "good" fits to experimental data that make no sense physically. In order to obtain simulations that lead to accurate physical insight and are useful for technology development, one must understand the underlying physics and adopt a calibration strategy that captures all the essential physics of the device. In the case of the pGaN HEMT, before one can use the simulation environment to simulate a second order phenomenon such as gate leakage, we must first ensure that we can adequately simulate the

primary operation of the HEMT, which is best measured in the dependence of drain current on gate voltage. We calibrated the output characteristics (I_D-V_G) of a pGaN HEMT structure (the standard structure that was used in all the experimental data that we studied for gate leakage) against experimental measurements from previously published work as shown in Figure 5-1[122]. Note that we do not have leakage data for the device shown in Figure 5-1, and that authors reporting on gate leakage do not usually report the I_D-V_D characteristics. However, the structure we simulated is a very standard pGaN HEMT device structure, the overall expected behavior of any pGaN HEMT should look similar to this case, and we calibrated the model parameters by specifying the specific attributes of the structure for which data is given in Figure 5-1 (i.e., layer thicknesses, doping levels, and contact metal). For our subsequent gate leakage simulations, we then retained the models and model parameters obtained through this calibration only changed parameters that were specific to each device being simulated (e.g., contact metal).
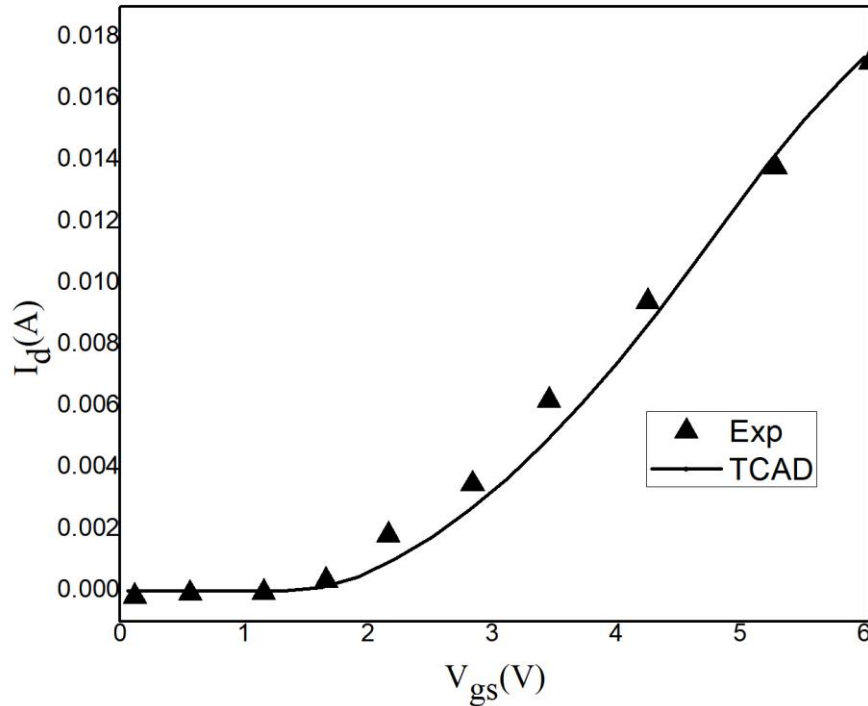
Figure 5-1: Simulation of I_D-V_G for the standard pGaN/AlGaN/GaN HEMT compared with experimental data ([122]).

To obtain the fit shown in Figure 5-1, we used the Hydrodynamic model as the carrier transport model[123]. This model explains carrier transport in terms of energy balance equations considering the non-equilibrium conditions; the energy of each type of carrier is estimated from its own temperature conditions. In addition, we used the Masetti doping-dependent mobility model [127] to account for mobility degradation due to impurity scattering and the Canali model [128] to incorporate high field mobility saturation. Carrier mobilities are calculated from these models using default parameters for GaN provided in Sentaurus. We took into account the bandgap dependence on temperature but assumed no bandgap narrowing due to doping because

of the wide bandgap of GaN[124]. For these models, we used the default parameters in Sentaurus.

Mg ions inside of the GaN crystal have high ionization energy, leading to incomplete ionization of dopants. This is modeled by Fermi-Dirac distribution using the equation [125],

$$N_A = \frac{N_{A,0}}{1+g_A exp\left(\frac{E_A-E_F}{kT}\right)} \tag{5.1}$$

where $N_{A,0}$ is the acceptor concentration, N_A is the ionised acceptor concentration, and g_A is the degeneracy factor for the impurity levels. Equation (5.1) only applies for $N_{A,0} < 10^{22}$ cm^{-3}, which is the case in all the devices we modeled. E_A-E_F is the activation energy for acceptor ionization (E_A is the acceptor level in the bandgap and E_F is the fermi level). Figure 5-2 shows the percentage of acceptors that are ionized as a function of activation energy at room temperature. In our simulations, we set $N_{A,0}$ in each device to the nominal dopant concentration in that device and set $E_A = 0.16$ eV above the valence band edge [125][126]. For Mg in GaN, $g_A = 4$[129].
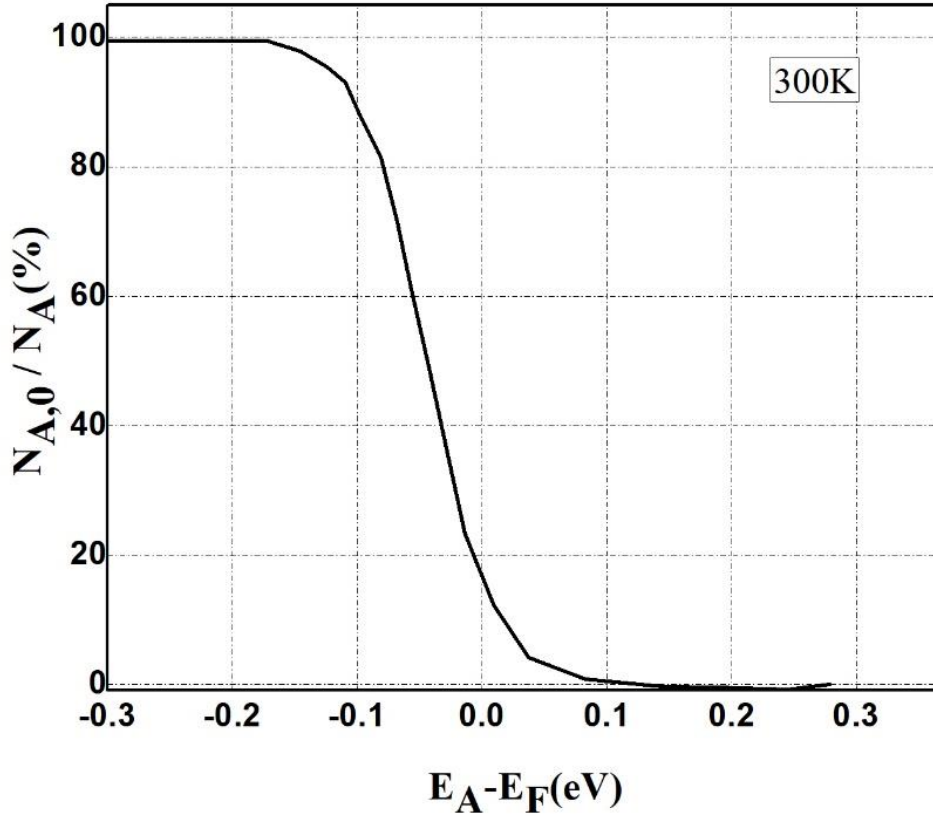
Figure 5-2: Ionised acceptor concentration as a function of activation energy (E_A)

[125][126].

In GaN HEMTs, the two-dimensional electron gas (2DEG) is dependent on the polarization at the AlGaN/GaN interface. The spontaneous polarization parameter is dependent on the mole fraction (m) of $Al_mGa_{1-m}N$ layer [P_{sp} (m)= (-0.052m -0.029) C/m^2][130]. This value is calculated to be -0.039 C.m^{-2} for a mole fraction of 0.2. The other polarisation effect originates from piezoelectric behavior as a result of the strain induced by lattice mismatch between GaN and AlGaN. In our simulation, we used Sentaurus' default model[121][124]. The total polarization vector(P) is given by P=P_{sp}+P_{Strain}. Here, Psp is the spontaneous polarization

mentioned earlier and P_{strain} is computed from piezoelectric strain coefficients which are generated depending on the Al mole fraction. GaN simulations are sensitive to the level of interface charge assumed. This fixed charge (σ) is typically in range of (0.5-1.3) $\times 10^{13}$ cm^{-2} from previous TCAD studies[124][132][133][134].For the I_D-V_G characteristics shown in Figure 5-1, we used a fixed trap charge, $\sigma = 8 \times 10^{12}$ cm^{-2} at AlGaN/GaN interface. There is also a piezoelectric activation factor(F) associated with the strain model available in TCAD whose default value is 1. In our simulations, we have chosen it to be 0.8[135]. This value remains constant for subsequent gate leakage simulations which will be discussed in the following section. The buffer layer is carbon doped with a concentration of 1×10^{16} cm^{-3}[118]. Table 5-1 gives a summary of the TCAD parameters used to obtain Figure 5-1.

Table 5-1:List of TCAD parameters.

Parameter	Description	Values	Units	Ref
m	Mole fraction of barrier layer	0.2	--	-
E_g	Bandgap of GaN	3.4	eV	-
ε_{pGaN}	Relative dielectric constant of GaN	9.5	--	-
E_A	Mg acceptor level	0.16	eV	[125][129]
N_A	Buffer doping concentration	10^{16}	cm^{-3}	[118]
σ	Fixed trap charge at AlGaN/GaN interface	0.8 $\times 10^{13}$	cm^{-2}	[124][125]
F	Piezoelectric activation factor	0.8	--	[135]
g_A	Degeneracy factor for the impurity levels	4	--	[129]
m_h	Effective mass of holes	$0.8 \times 9.11 \times 10^{-31}$	kg	[131]

5.3 Gate Leakage in TCAD

The vertical gate stack of the pGaN/AlGaN/GaN HEMT structure consists of a Schottky diode(D_1) and a pin diode(D_2) in series. We know that for positive gate bias, D_1 is reverse biased while D_2 is forward biased. The current from D_2 is dominated by the spillover of electrons and holes across the intrinsic AlGaN barrier layer of the pin diode. Since the diffusion length of the pGaN cap layer is small (50~100 nm), some electrons may drift under the electric field into gate contact[88]. The current from D_1 is dominated by the tunneling of holes from the gate metal over a thin triangular barrier formed between metal and pGaN. Therefore, we use the Fowler Nordhiem Tunneling (FNT) mechanism in the TCAD simulation, just as we did in our numerical model [120]. However, FNT current at low gate bias is too low to account for the observed leakage. Therefore, it is necessary to consider the additional current originating from surface traps, i.e., Trap Assisted Tunneling (TAT) current.

5.4 Results

Now, we will discuss the results of the gate leakage simulation from TCAD. The value of σ used in the simulations for 5 devices are 0.75×10^{13} cm^{-2}(device 1),1×10^{13} cm^{-2}(device 2), 0.92×10^{13} cm^{-2} (device 3) and 1.1×10^{13} cm^{-2}(devices 4 and 5). From Figure 5-3, we see that gate leakage from TCAD simulations are in good agreement with experimental characteristics of the 5 devices at room temperature. Figure 5-4 shows the comparison of I_G from the TCAD simulations at different temperatures for devices 2,4 and 5.
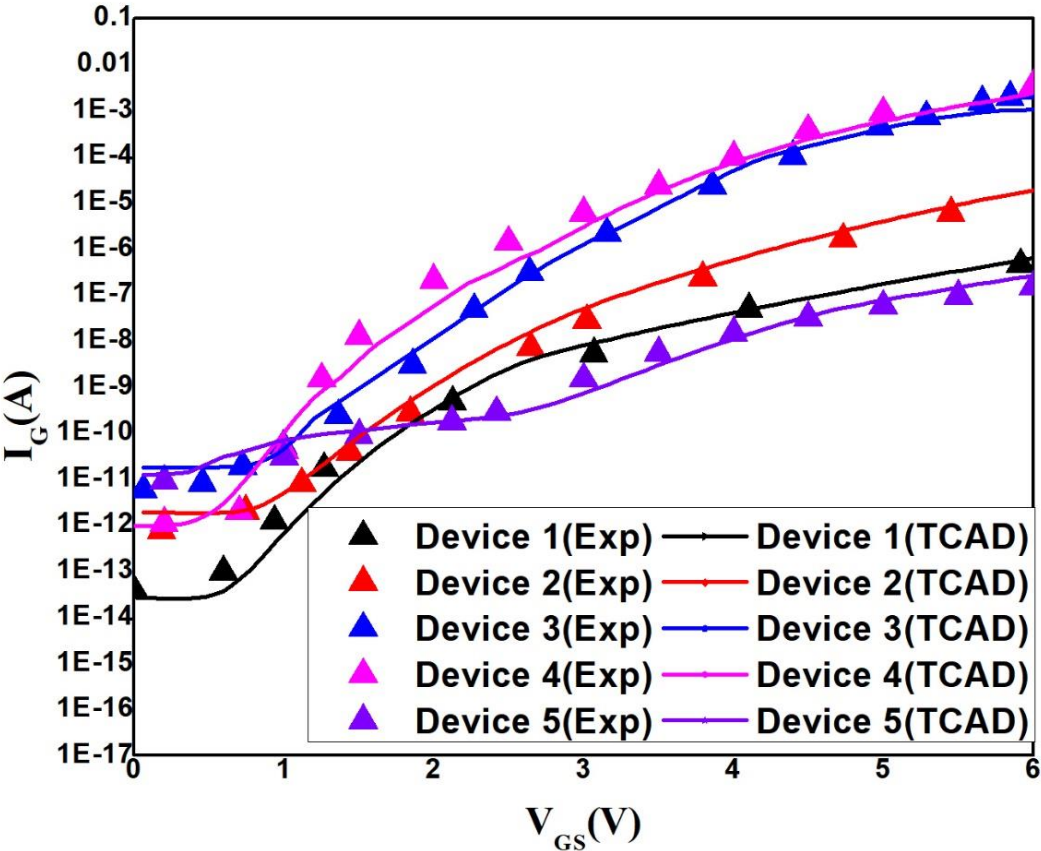
Figure 5-3: Comparison of gate current (I_G) from TCAD simulations with experimental characteristics at room temperature. The experimental data for the above plot has been extracted from references[81][82][83][84]

(a)

(b)

(c)
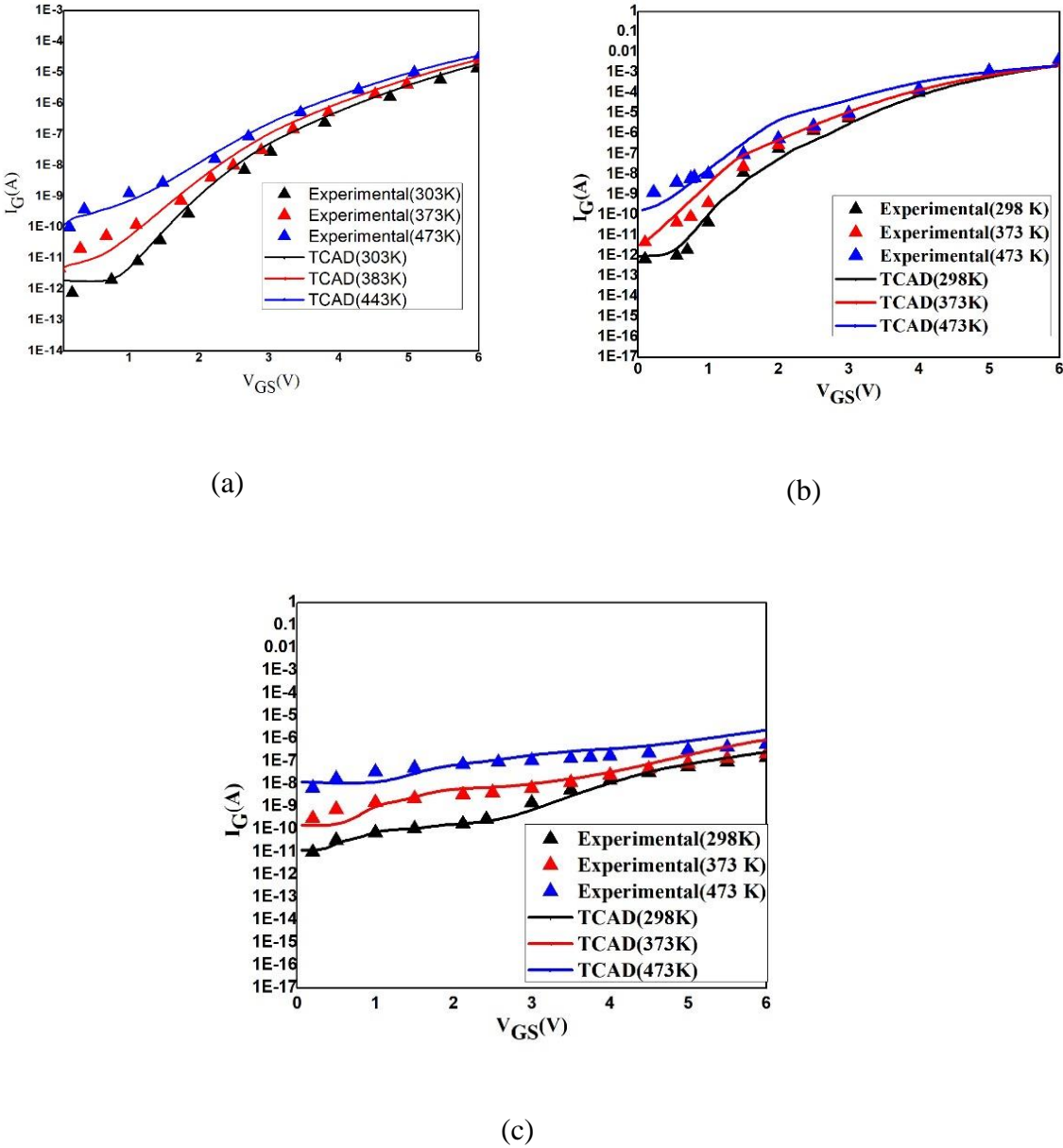
Figure 5-4: Comparison of the model to the leakage current at different temperatures for

devices 2,4 and 5.The experimental data for the above plot has been extracted from

references[82][84].

As stated earlier, ϕ_B is important in gate leakage modeling. In our TCAD simulations using the FNT mechanism, the magnitude of the I_g is controlled by ϕ_B. The list of ϕ_B values used for different metal contacts in our TCAD simulations is shown in Table 5-2.

Table 5-2: The value of Schottky barrier height (ϕ_B) for different gate metals used for this work.

Metals	ϕ_B (eV)	Experimental ϕ_B (eV) from literature	Reference
TiN	1.69	$1.9 - 2.5$	[88][103]
Ni	1.49	1.8	[96]
Pd	1.12	1.4	[96]
Ti	1.74	$2.08 - 2.2$	[96][102]

I_G from FNT is very small at low bias regions. I_G in this region is governed by surface traps. The trap assisted carrier transport is given by[136]:

$$R_{\text{net}} = \frac{N_{\text{TRAP}}\, c_{\text{n}} c_{\text{P}}(np - n_{\text{i}}^2)}{c_{\text{n}}\left(n + \frac{n_{\text{i}}}{g_{\text{n}}}\exp\left(\frac{E_{\text{TRAP}}}{k_{\text{B}}T}\right)\right) + c_{\text{p}}\left(p + \frac{n_{\text{i}}}{g_{\text{p}}}\exp\left(\frac{-E_{\text{TRAP}}}{k_{\text{B}}T}\right)\right)} \tag{5.2}$$

where, n_{i} is the intrinsic carrier concentration, n and p are the electron and hole densities, N_{TRAP} is the trap concentration, E_{TRAP} is the energy of the trap, c_{n} and c_{p} are the electron and hole capture rates, and g_{n} and g_{p} are the electron and hole degeneracy factors, K_{B} is the Boltzmann' constant and T is the operating temperature. The key parameters that were used as fitting parameters in our simulations are the trap concentration (N_{Trap}), the trap level in the bandgap

(E_{Trap}), and the carrier capture rate (c_n, c_p) which are dependent on carrier cross section (σ_n, σ_p), with the most important of these being the trap energy level (E_{Trap}). The trap parameters are summarized in Table 5-3.

Table 5-3:List of Trap parameters.

Device No	Temp (K)	Trap conc (cm^{-3})	Energy level(eV)	Carrier capture cross section(cm^{-2})
1	298	2.7e17	1.3 eV from VB	1e-14
2	303	2e17	0.88 eV from VB	1.5e-14
3	298	2.2e17	0.52 eV from VB	2e-14
4	298	2.1e17	1.1 eV from VB	1.2e-14
5	298	2.25e17	0.5 eV from VB	2e-14

VB-Valence band

The energy levels for the traps in the bandgap are used to identify the dominant defects at the interface for each sample (as detailed in, for example,[137][138][139]). For example, the trap level at E_V+0.88 eV that we used to simulate the behavior of device 2 corresponds closely to the defect labeled as H_d with an energy level at E_V+0.9 eV. This defect is mainly associated with gallium vacancy complexes or carbon states. Similarly, the trap level at E_V+0.5 eV is close to defect (H_c) with an energy level at E_V+0.46 eV. This value is cited for traps related to the nitrogen vacancy [138].

One of the benefits of TCAD simulation is that we are able to gain insight into the device behavior by examining behavior that is difficult to ascertain through measurement. For example, in pGaN devices, 2DEG is realized only when conduction band edge is lowered into fermi-level

with an application of a positive bias. This 2DEG density (n_s) as function of gate bias can be computed from TCAD simulations which is shown in Figure 5-5 for device 2.
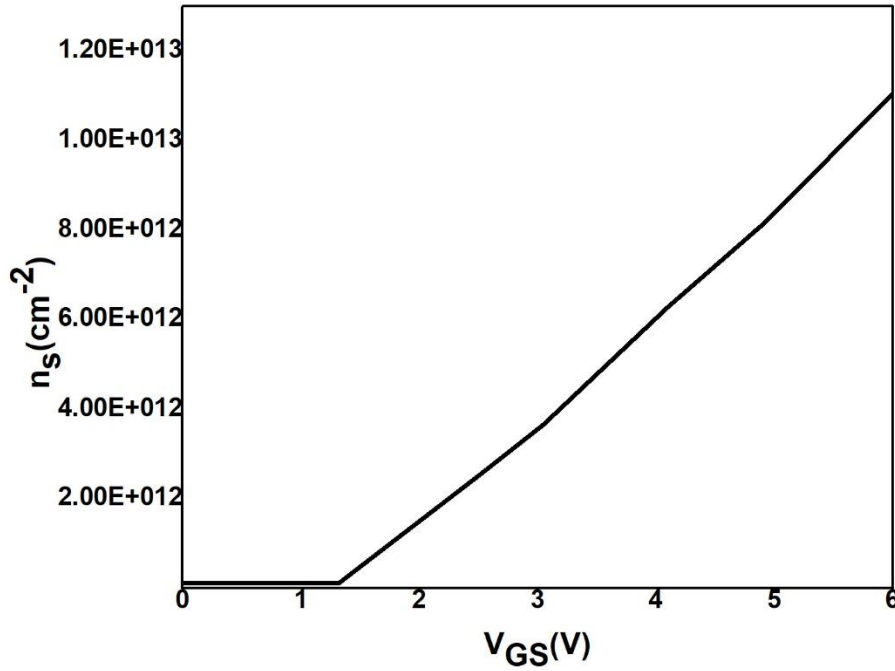
Figure 5-5: Variation of 2DEG (n_s) with gate bias (V_{GS}) for device 2.

Since TCAD simulations calculate the electric field distribution in each layer, we can estimate potential drops at each layer. This can help us compute the voltage division between two diodes in the gate stack. The potential drop in the pGaN/AlGaN/GaN HEMT structure for device 2 is shown in Figure 5-6 for V_{GS}=0V and V_{GS}=6V respectively. The Schottky voltage (V_{sch}) and pin voltage (V_{pin}) are calculated as

$$V_{sch} = V_A - V_{bi,MS} \tag{5.3}$$

$$V_{pin} = V_{bi,AlGaN} - V_B \tag{5.4}$$

where, $V_{bi,MS}$ is the built-in voltage at the metal/pGaN junction, $V_{bi,AlGaN}$ is the built-in voltage of the pin diode, V_A and V_B are the potential at the metal/pGaN junction and the potential inside the pin diode at a particular gate bias, respectively. The built-in voltages $V_{bi,MS}$ and $V_{bi,AlGaN}$ estimated at zero bias are 1.43 V and 2.38V respectively. The variation of V_{sch} and V_{pin} as a function of gate bias (V_{GS}) is shown in Figure 5-7. The V_{ser} voltage drop obtained by the subtraction of V_{sch} and V_{pin} from V_{GS}.
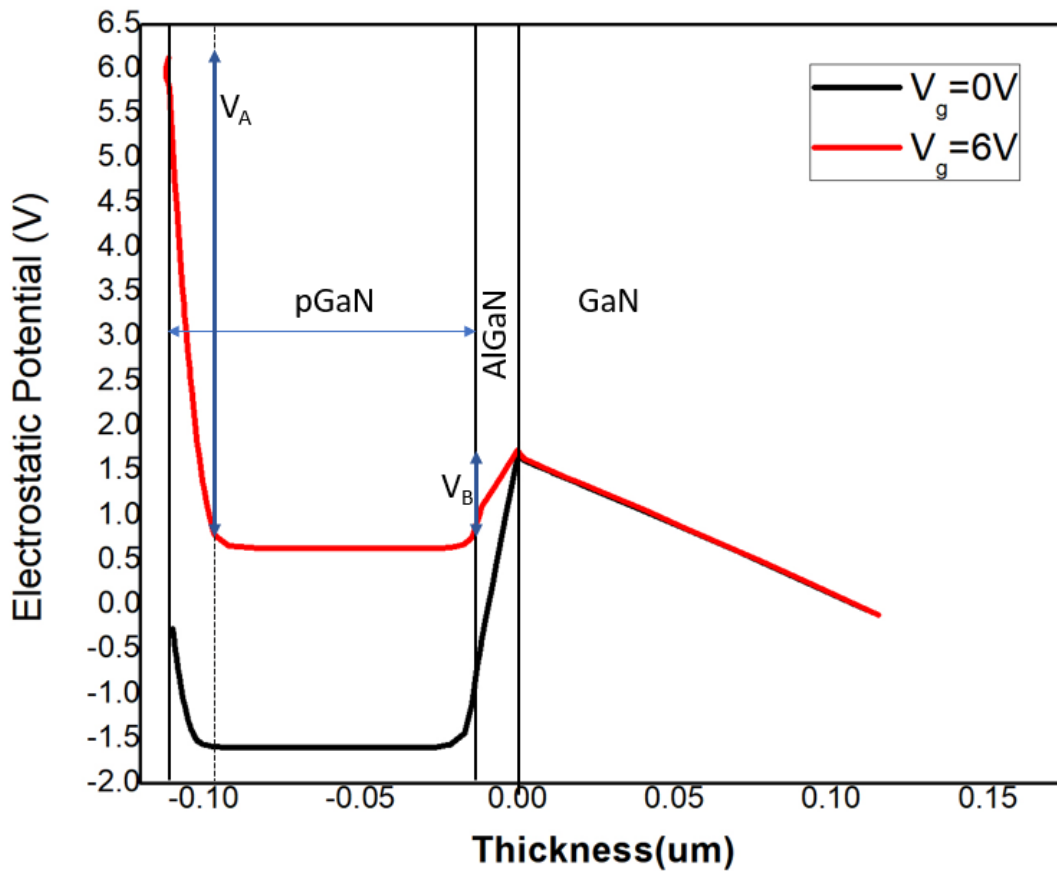
Figure 5-6: Variation of electrostatic potential as function of thickness in the pGaN/AlGaN/GaN gate stack for device 2.
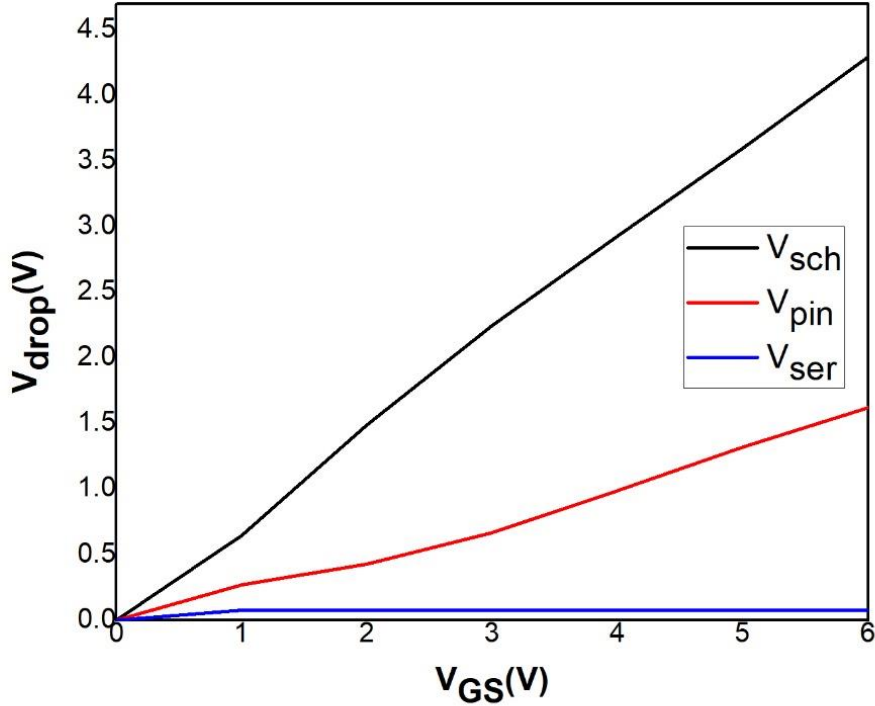
Figure 5-7: Voltage drop across the pGaN/AlGaN/GaN gate stack structure for device 2.

Through TCAD simulations, we have demonstrated that Fowler Nordheim Tunneling (FNT) is sufficient to explain the gate leakage behavior of pGaN HEMTs over a wide range of conditions. However, FNT underestimates the leakage at low gate bias. Leakage under low gate bias appears to be dominated by surface traps. While we have been able to fit the available data by assuming particular trap levels and densities for each device, this part of the work is effectively an empirical fit. Without more data on the specific fabrication processes and/or characterization of the interface, this is the best that can be accomplished. While it falls short of being predictive, it does provide guidance to the device and process engineer on the importance of specific defects

and the trap levels with which they are associated. It should be noted that the low bias regime is the less important regime since the gate leakage is very low (on the order of nA for most of the devices studied). The simulations demonstrate that the gate leakage at higher bias is insensitive to surface trap parameters.

The simulation also shows that the most important factor in determining gate leakage is the Schottky barrier height for the gate contact. The gate leakage increases slowly with gate bias and is weakly dependent on temperature. The impact of series resistance is very small, with most of the voltage dropping across the reverse-biased Schottky junction and a significant portion dropping across the forward-biased pin diode.

The TCAD environment that we have set up here can be effectively used to study strategies for device design and, in particular, optimization of gate leakage. The calibrated model can be used to understand the impact of a given strategy on other device parameters, such as threshold voltage or drain saturation current.

5.5 Conclusion

The gate leakage process has been studied for pGaN HEMTs with the help of TCAD simulations. Just like in our numerical modeling study, two mechanisms namely FNT and TAT are recognized as the principal components of the gate leakage process. Schottky barrier height controls the magnitude of the leakage current. The energy of traps in the pGaN layer has been identified and compared with some known defects in pGaN for calibrating the gate leakage current at low bias.

Chapter 6: Impact of the device structure in the gate leakage simulations for pGaN/AlGaN/GaN HEMTs

6.1 Introduction

The pGaN cap layer is very important for enhancement operation in pGaN/AlGaN/GaN HEMTs. It lifts up the conduction band edge from the fermi-level in the GaN channel. This enables the device to have a positive threshold voltage[87][140][141]. We know that during the forward bias operation, gate metal and pGaN layer form a reverse Schottky diode which is instrumental in determining the leakage current. One of the ways to reduce leakage I_g is to increase Schottky barrier height (ϕ_B). This has been discussed for the 5 devices we have modeled in chapters 4 and 5 with different metals having different ϕ_B controlling I_g . In this chapter, we have used the TCAD model developed from the previous chapter to explore various strategies which have an impact on I_g . We will look at factors as pGaN doping (N_A) and pGaN thickness(t_{pGaN}) and how they influence the leakage current.

To the best of our knowledge, there have been four methods implemented by different research studies in the literature that affect the gate leakage characteristics[84][142][143][144]. The first one is surface passivation which only affects in lower bias region where leakage current is extremely low (~nA order), hence it is less important to the device characteristics. In this chapter, we will focus on other 3 techniques adopted by 3 different research groups. All these 3 techniques involve inserting a very thin layer in between the metal and the pGaN layer. The first technique involves growing an unintentionally doped GaN layer on top of the pGaN[142]. The second technique is the addition of a lightly doped extra cap layer to the existing pGaN layer[143]. Finally, the third technique involves surface reinforcement of the pGaN layer using oxygen plasma which

will convert a few nanometers on top of the pGaN layer into GaON[144]. We will use TCAD model to simulate I_g and I_d for each of these modified structures to see their simulation dependence on experimental characteristics. Furthermore, using the versatile TCAD simulator, we will explore varying some of the parameters in the modified structure to see their effect on the leakage and the drive current.

This chapter is summarized as follows: In section 2, we look at the impact of pGaN doping and thickness on the gate leakage performance. In Section 3, we look at the 3 techniques mentioned earlier through TCAD simulations to see their effect on device performance. Section 4 is the conclusion.

6.2 Impact of pGaN cap layer on the gate leakage

As stated earlier, the pGaN layer is very important to the device operations. Here, we look at the effect of pGaN layer doping density and its thickness on I_g.

6.2.1 Effect of pGaN doping on gate leakage

The doping density (N_A) is very important in electric field calculations. An increase in doping will lead to a higher electric field at the Schottky junction. This will increase I_g. Figure 6-1 shows the influence of N_A on I_g for device from TCAD simulations. N_A has been varied from doping level of 2×10^{18} cm^{-3} to 2×10^{20} cm^{-3} in this study. We can see the huge variation in I_g for the varied doping range. From the simulations, it can be observed that I_g saturates for N_A of 2×10^{20} cm^{-3} and higher, and 2×10^{18} cm^{-3} and lower, respectively.
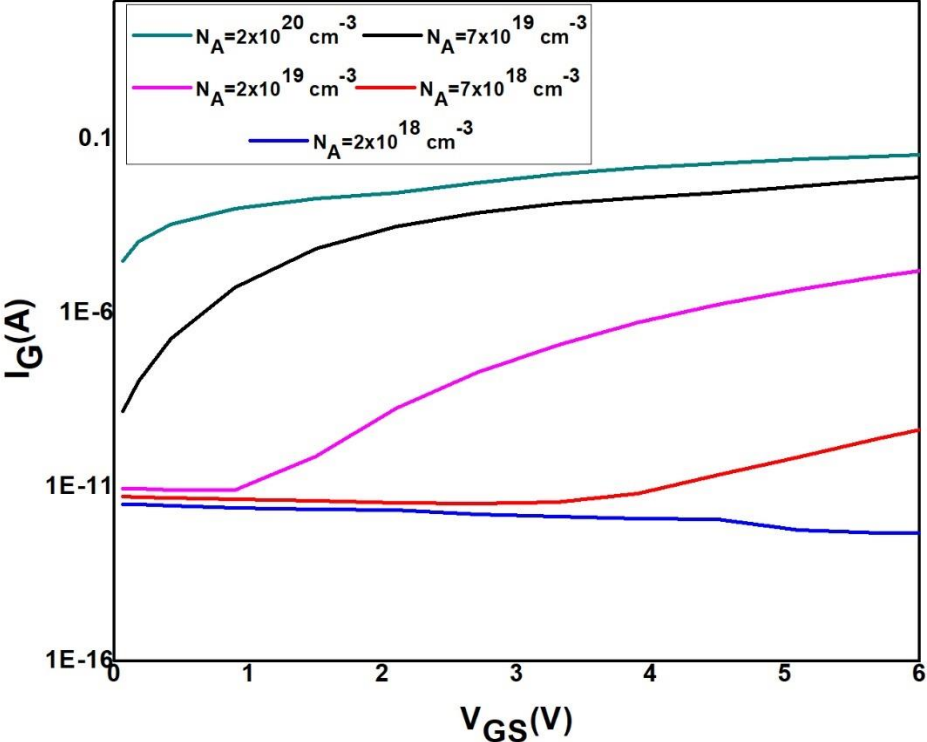
Figure 6-1: Effect of pGaN doping on the gate leakage current.

6.2.2 Effect of pGaN layer thickness on the gate leakage

Another important parameter for the pGaN cap layer is the thickness(t_{pGaN}) of the pGaN cap layer. Generally, the pGaN thickness is varied from 70 nm to 120 nm[145][146]. In our simulation, we have varied t_{pGaN} from 70 nm up to 120 nm. Figure 6-2 demonstrates the impact of t_{pGaN} on I_g.
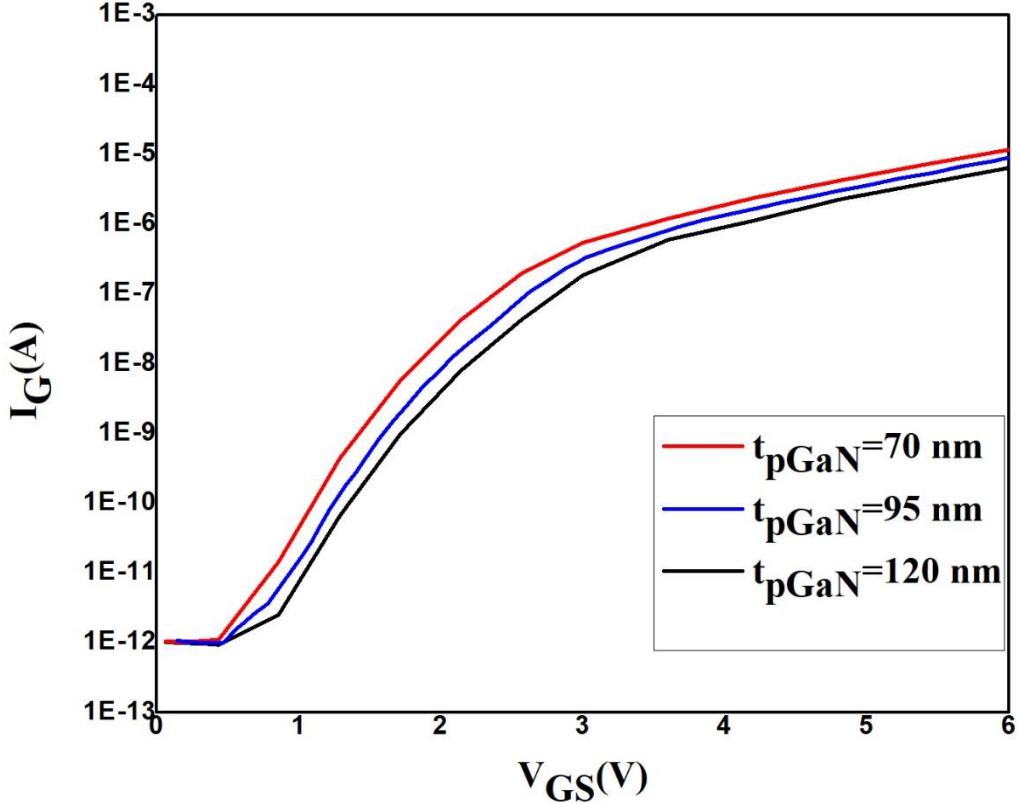
Figure 6-2: Effect of pGaN layer thickness on the gate leakage current.

6.3 Cap layer engineering

One important way to reduce leakage in pGaN HEMTs is to lower the electric field at the Schottky junction. With that in mind, a thin layer (lesser doping than the initial pGaN layer) can be inserted between metal and pGaN layer which will reduce this electric field. Recently, few studies have been conducted implementing this idea[142][143][144]. In this section, we will look at each of these techniques and how it impacts the device performance.

6.3.1 Unintentionally doped GaN cap layer

In the first method, an unintentionally doped (UID) GaN cap layer is grown on top of the pGaN layer. The devices studied here is grown via metal organic chemical vapor deposition (MOCVD) chamber[142]. The thickness of the barrier layer is 15 nm with a mole fraction of 0.2. The pGaN cap layer has a doping concentration (N_A) is 4×10^{19} cm^{-3} and a thickness of 85 nm. This published experimental study involved 2 UID grown devices (B and C) with the thickness of 20 nm and 30 nm respectively. In the TCAD simulations, additionally we have studied an extra case (50 nm thick UID). Figure 6-3 shows the schematic of the unintentionally doped (UID) structure for pGaN/AlGaN/GaN HEMTs.
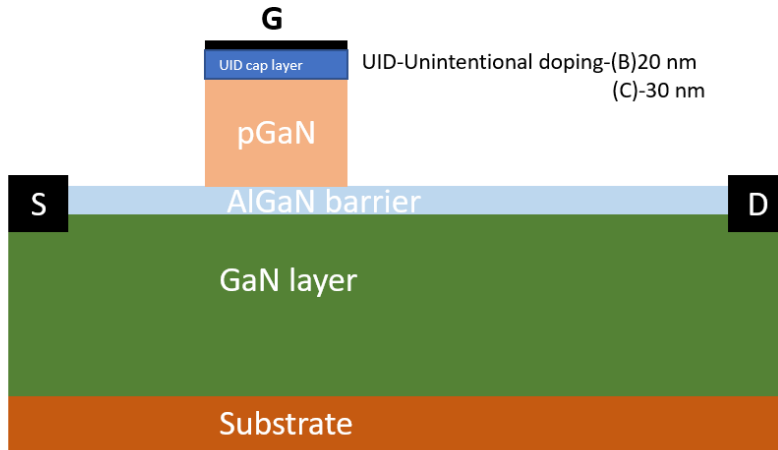
Figure 6-3: Addition of UID extra cap layer on pGaN/AlGaN/GaN structure. Here, the thickness of UID layer of the 2 devices are 20 nm and 30 nm respectively.

One important note is that even though the extra cap is purposefully grown unintentionally doped, Mg ions concentration in this layer is very closer to Mg ion concentration in the pGaN layer due

to the memory effect of Mg ions from MOCVD chamber as stated in [142].The doping profile in UID layer obtained from TCAD simulations is similar to the secondary ion mass spectroscopy (SIMS) profile[142] as shown in Figure 6-4.
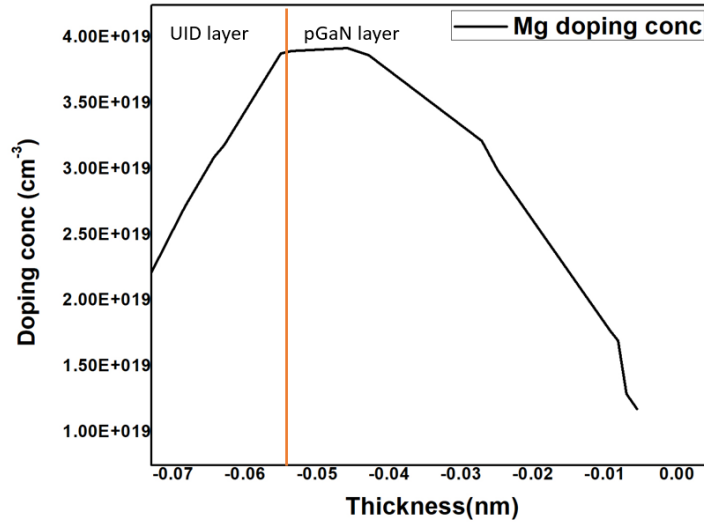
Figure 6-4: Doping profile with thickness for the UID device.

In the TCAD simulations, the value of ϕ_B is taken as 2.12 eV, energy (E_A) to activate Mg ions is taken as 0.16 eV, while trap parameters used are- trap energy level of 0.44 eV from valence band and trap concentration of $3.5 \times 10^{17} cm^{-3}$. The fixed charge at the AlGaN/GaN interface is 1.05×10^{13} cm^{-2}. Now, we look at the I_G-V_G characteristics of this UID structure. Gate current fromTCAD simulations for this UID structure of different thickness (20 nm,30 nm and 50 nm) as well as non UID structure have been shown in figure 6-5 and compared with the experimental study. The increase in thickness of UID layer reduces I_g.
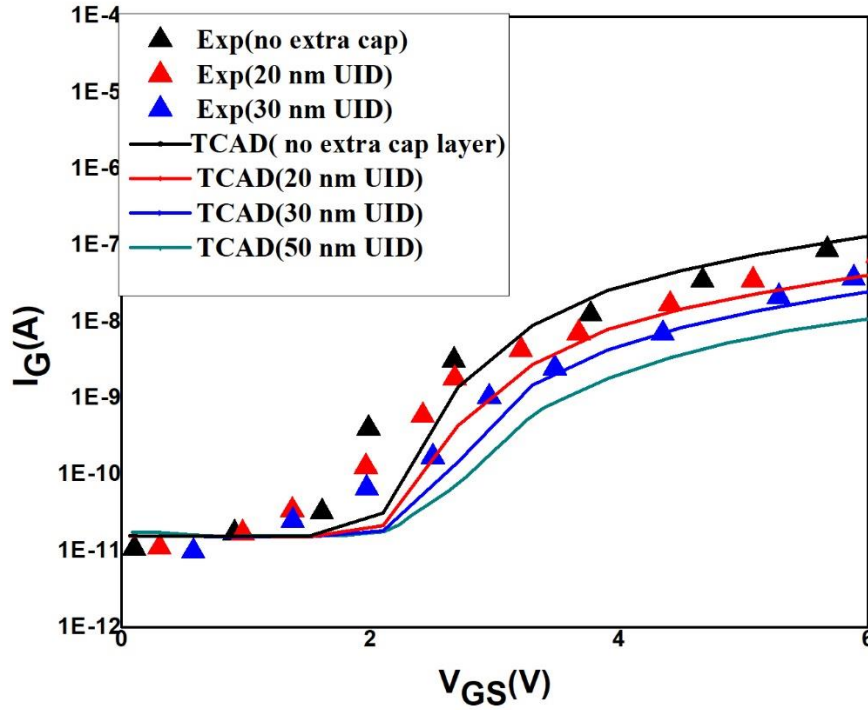
Figure 6-5: Effect of UID cap layer on Ig. The experimental data for the above plot has been extracted from reference[142].

Now, we take look at the I_D-V_G characteristics for this UID from our TCAD simulations and compare it with experimental values as shown in Figure 6-6. The threshold voltage (V_{th}) of experimental study is 2.1 V for all devices (non UID, 20nm and 30 nm UID). In our simulations, V_{th} is 2.2 V for the non-UID device. V_{th} for LDP devices of thickness 20 nm,30 nm and 50 nm were 2.26, 2.3 and 2.36 V, respectively. $I_{ON/OFF}$ ratio is larger than 10^8 for both TCAD simulations and experimental data. The simulated drain saturation current is 0.05 A.

Figure 6-6: Comparison of I_d from experimental measurement to TCAD with & without the UID layers. The experimental data for the above plot has been extracted from reference[142].

6.3.2 Lightly doped cap layer

The second technique involves the insertion of lightly doped pGaN (LDP) cap layer[143] between the gate metal and the pGaN layer. The thickness of the AlGaN layer is 13 nm and its mole fraction is 0.28. The pGaN cap layer has a doping concentration (N_A) is 2×10^{19} cm^{-3} and a thickness of 70 nm. The thickness of LDP layer is 20 nm with a doping density of 2×10^{18} cm^{-3}. In the TCAD simulations, additionally we have studied two other cases of doping (7×10^{17} cm^{-3} and 7×10^{18} cm^{-3}) other than one proposed in the study[143]. For the simulations, the value of ϕ_B is taken as 1.57 eV, energy (E_A) to activate Mg ions is taken as 0.16 eV, while trap parameters used are- trap energy level of 0.55 eV from valence band and trap concentration of 2×10^{17} cm^{-3}. The fixed charge at the

AlGaN/GaN interface is 0.9×10^{13} cm^{-2}. Figure 6-7 shows the schematic of the LDP structure in pGaN/AlGaN/GaN HEMTs device. Figure 6-8 shows the I_g-V_g characteristics.
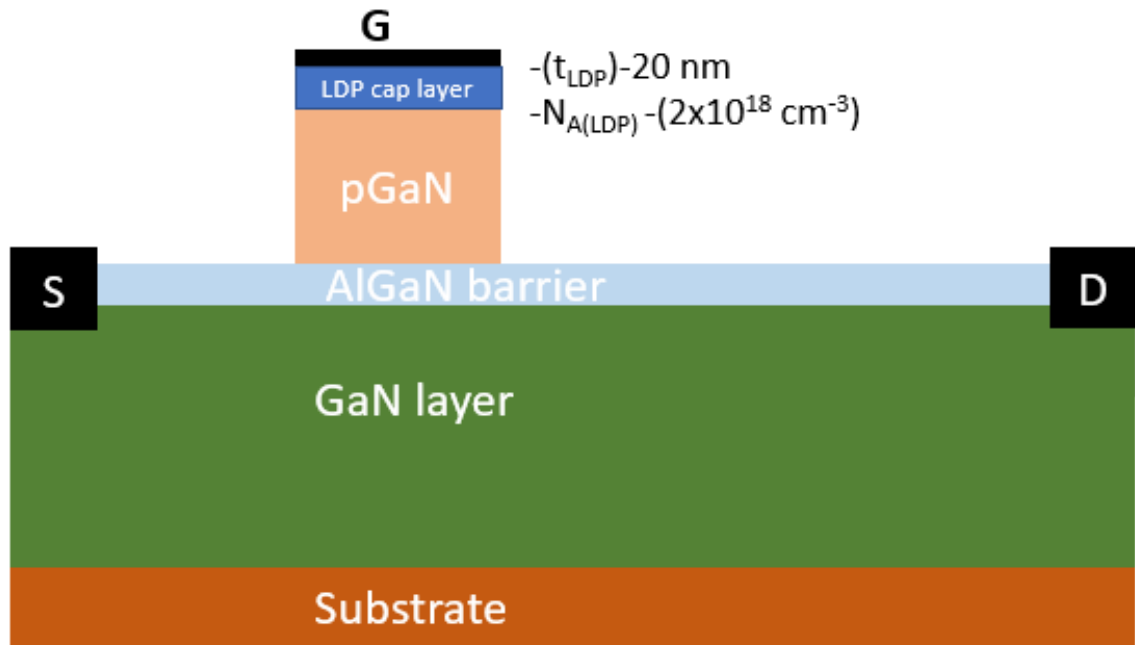
Figure 6-7: Addition of LDP cap layer on pGaN/AlGaN/GaN structure. Here, the thickness and doping density of LDP cap layer are 20 nm and 2×10^{18}cm^{-3} respectively.
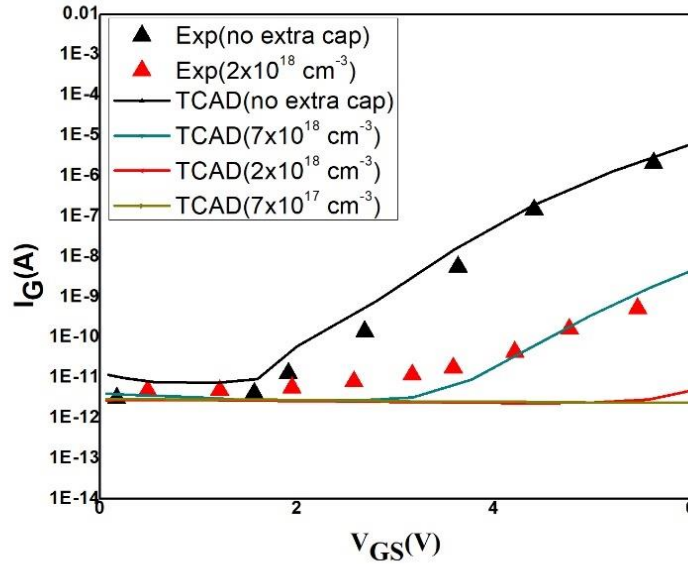
Figure 6-8: Effect of LDP on I_g characteristics. The experimental data for the above plot has been extracted from reference[143].

From Figure 6-8, we observe that our TCAD simulations predict I_g to be much lower than experimental I_g for LDP device doped at $2x10^{18} cm^{-3}$. This is due to a very low electric field. However, the authors in this study do not report any SIMS profile, so it may be quite possible that Mg ions diffuse into this lightly doped pGaN layer and raise the doping concentration in this layer much higher than $2x10^{18} cm^{-3}$ reported for this device. In our I_g simulations, we observe that when doping is in the range of $7x10^{18} cm^{-3}$, simulated I_g fits with experimental I_g for LDP device.

In Figure 6-9, we take look at the I_D-V_G characteristics for this LDP structure using TCAD simulations and compare it with experimental data. The threshold voltages of experimental study were roughly 1.4 V and 1.45 V. In our simulations, V_{th} was 1.5 V for the non-LDP device. The V_{th} for LDP devices with different doping were 1.55 V, 1.6, and 1.66 V. $I_{ON/OFF}$ ratio is approximately 10^9 for both TCAD and experiment. The simulated drain saturation current is 0.015 A.
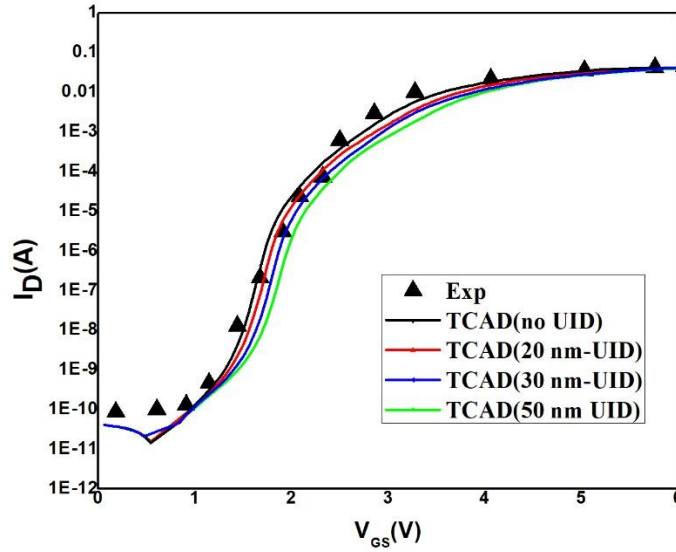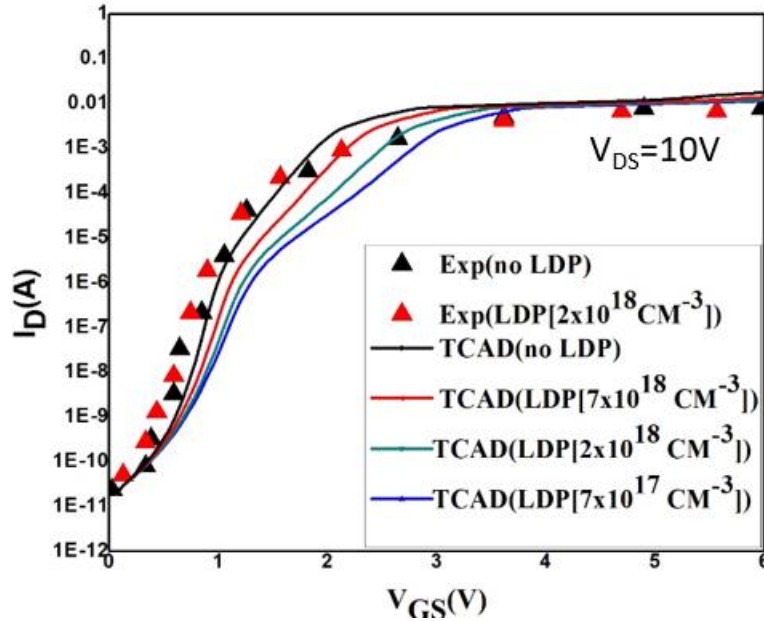
Figure 6-9: Comparison of I_D from experimental characteristics with TCAD with and without

LDP. The experimental data for the above plot has been extracted from reference[143].

6.3.3 Surface reinforcement layer

Finally, we look at effect of oxygen plasma on the pGaN surface which is referred as surface

reinforcement technique[144]. After the top surface of the pGaN layer is subjected to this plasma

treatment, it converts few nanometers of pGaN layer into crystalline GaON nitride layer. The

thickness of the GaON layer is about 4.3 nm and GaON has a bandgap of 4.1 eV. The thickness

of the barrier layer is 15 nm with a mole fraction of 0.2. The pGaN layer has a doping concentration

(N_A) is $3x10^{19}$ cm^{-3} and a thickness of 100 nm. Figure 6-10 shows the schematic of the surface

reinforcement layer (SRL) structure in pGaN/AlGaN/GaN HEMTs.
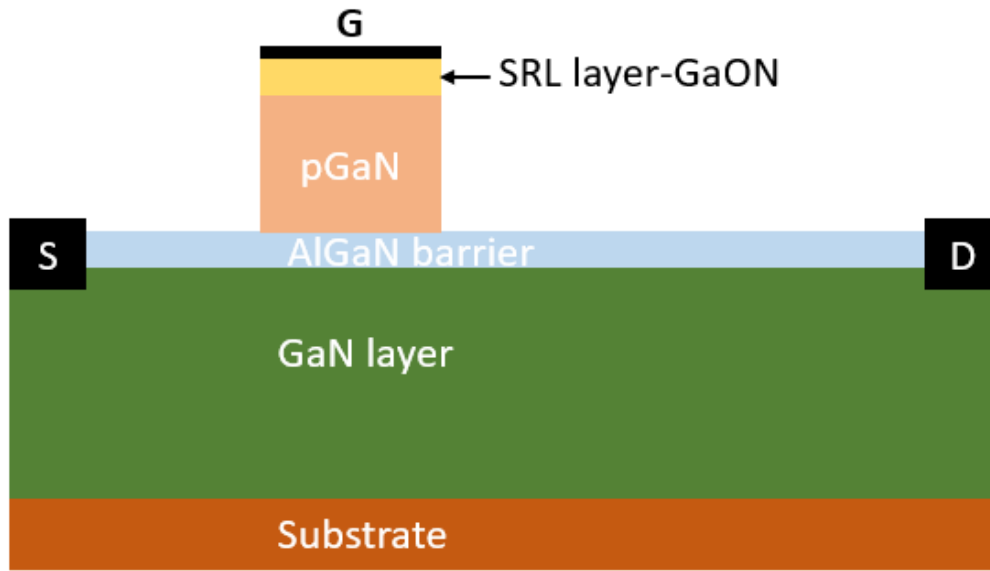
Figure 6-10: Schematic of SRL structure in the modified pGaN/AlGaN/GaN HEMTs.

In the simulations, the value of ϕ_B for the non SRL layer is taken as 1.37 eV, energy (E_A) to activate Mg ions is taken as 0.16 eV, while trap parameters used are- trap energy level of 0.4 eV from the valence band and trap concentration of 2.9 x10^{17}cm^{-3}. The fixed charge at the AlGaN/GaN interface is 0.85x10^{13} cm^{-2}. The value of ϕ_B for the SRL layer is taken as 1.7 eV. Figure 6-11 compares the I_G-V_G characteristics (experiment and TCAD) for this structure.
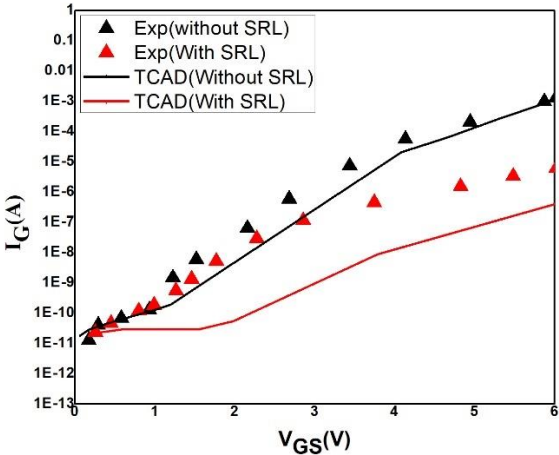
Figure 6-11: Comparison of I_g characteristics from experimental characteristics with TCAD for devices with and without SRL. The experimental data for the above plot has been extracted from references[144].
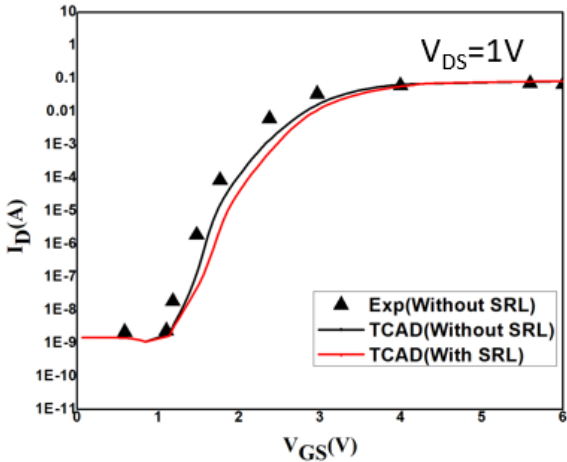
Figure 6-12: Comparison of I_D from experimental characteristics with TCAD with and without SRL. The experimental data for the above plot has been extracted from reference[144].

From Figure 6-11, we observe that our TCAD simulations predict lower I_g than experimental I_g for the SRL based device. This is due to effective reduction in acceptor concentration as pointed

by the author in this study[144]. They do not provide any value for this reduced acceptor concentration. With no SIMS profiling data being available, it is difficult to ascertain the concentration level in SRL layer, so simulated I_g is not fitting well with experimental I_g.

In Figure 6.12, we take look at the I_D-V_G characteristics for this SRL structure using TCAD simulations and compare it with experimental data. The threshold voltage of experimental study was 1.2 V for both the devices. In our simulations, V_{th} was 1.35 V for the non-SRL device. The V_{th} for SRL device was 1.45V. $I_{ON/OFF}$ ratio is approximately 10^8 for both TCAD and experiment. The simulated drain saturation current is 0.07 A. Table 6-1 compares the device performance for three different techniques.

Table 6- 1: Comparison of device performance from TCAD simulations

Technique	Ig(A) [@V_G=6 V]	I_{Dsat}(A)	V_{th}(V)	Ion/off
UID [@t_{UID}=20 nm]	4.5×10^{-8}	0.05[@V_D=1 V]	2.26	10^8
LDP [@t_{LDP}=20 nm, $N_{A,LDP}$=2×10^{18}cm^{-3}]	5×10^{-12}	0.015[@V_D=10 V]	1.6	10^9
SRL [@t_{SRL}=4.3 nm]	3.5×10^{-7}	0.07[@V_D=1 V]	1.45	10^8

In this chapter, we have explored the dependence of doping and the thickness of the pGaN layer on I_g. Higher doping leads to large leakage current. The variation in terms of I_g is huge for (100 order) doping change in pGaN layer. For doping concentrations of 2×10^{18} cm^{-3} and 2×10^{20} cm^{-3}, I_g saturates both at the upper and lower range respectively. The thickness(t_{pGaN}) of the pGaN also impacts I_g. Increasing t_{pGaN} leads to smaller I_g, however this change is very marginal compared to the doping dependence.

We have also investigated 3 techniques (UID, LDP, and SRL) to see their impact on device performance. All these techniques involve inserting a small thin layer between the gate metal and the pGaN layer. Among them, LDP structure has been the most effective in reducing the gate leakage current. This is observed both for experimental as well as TCAD simulations. All three structures have a good $I_{on/off}$ ratio of 10^8 and higher. Also, these modifications have very less effect on I_{Dsat}, pointing out that these promising modifications have a lesser impact on the device channel conductive characteristics while reducing leakage current.

6.4 Conclusions

Throughout this chapter, we have looked at different ways in reducing the gate leakage current. We can conclude that the doping level in the pGaN layer is very crucial in determining the magnitude of I_g. These is further illustrated in the three studies of the modified cap layer. Among them, LDP structure has the most significant impact on reducing the leakage current. The effect of structural modification on the drive current is negligible as illustrated both from experimental as well as TCAD simulations making these structural modification encouraging approaches for optimizing device performance.

Chapter 7: Conclusion and future work

7.1 Conclusion

Gallium nitride is considered an important material in power electronics applications. It has superior material qualities such as high electron mobility, high bandgap, and good thermal conductivity. Despite all its advantages, GaN transistors do have certain reliability concerns such as hot electron degradation, device breakdown, and gate leakage.

This thesis primarily focuses on the gate leakage process in pGaN HEMTs. In the 3rd chapter, we reviewed the gate leakage process by looking at the different mechanisms proposed by different researchers to explain the gate leakage process. We have provided a summary of gate leakage models studied previously and highlighted some of the modeling issues in the leakage model available in the literature. We have provided a detailed description of 5 devices, including the gate leakage experimental characteristics. These devices will be used for modeling in the latter chapters. It was identified the Schottky barrier height is extremely important in leakage modeling and this parameter controls the magnitude of leakage current in each device.

In the 4th chapter, we have provided a numerical model that describes the gate leakage process in pGaN HEMTs as a function of gate bias and temperature. The model is physically justified with a consistent set of parameters that can explain gate leakage in pGaN HEMTs. The purpose of developing such a simple model is to reduce modeling complexities in pGaN HEMT devices. This model considers the voltage division between the two diodes something that previous models have ignored in their studies. The gate leakage happens via Fowler-Nordheim tunneling (FNT) mechanism through a thin triangular barrier formed between the metal and pGaN layer. However, at low gate voltages, FNT underestimates the leakage current, so the leakage current is dominated

by surface traps. Hence, we have used trap assisted tunneling (TAT) mechanism to explain the leakage current at low bias.

The limitation of the numerical model was that it was based on simple assumptions such as using the compact diode equation and ignoring series resistance. In the 5th chapter, we address these limitations using the commercial TCAD simulator. TCAD computes the field distribution in the whole device structure so, all the voltage drops in each layer of the whole gate stack will be accounted for, in the leakage current calculation. Additionally, some of the trap levels have been identified which are responsible for leakage at low bias. These trap levels are compared to the previous known defect levels in pGaN which should help device engineers in the future to optimize their own devices.

As stated throughout the discussion of this thesis, gate leakage is a serious issue in the operation of pGaN HEMTs. In chapter 6, we try to look at factors that influence leakage characteristics. The pGaN cap layer is extremely important for the whole operation of the device. There are two factors concerning the pGaN layer: doping concentration (N_A) and thickness(t_{pGaN}). It has been found that lowering N_A and increasing t_{pGaN} lowers the leakage current. Additionally, we have looked at three structural modifications that have been used to reduce gate leakage. We have calculated both the drain current and the leakage current using TCAD simulations for each of these three modified device structures and compared them with their corresponding experimental values. The simulations closely match with published experimental values, so simulated dependence of leakage and drive current can be useful for further modifications in the structure.

7.2 Future Work

This thesis focuses on the modeling and simulation of the gate leakage current in pGaN HEMTs. Our thesis is based on forward gate leakage process. Further investigation can be made to study reverse bias gate leakage which could be useful in understanding off state reliability issues. In the reverse bias conditions, the Schottky diode will be forward biased, and the pin diode will be reverse biased. In this case, most of the voltage drop in the gate stack will be absorbed by the pin diode and the Schottky drop will be smaller. It would be interesting to see whether FNT would still work for the reverse bias case or if other mechanisms need to be invoked to explain the reverse gate leakage process.

In this thesis, we have stressed the importance of traps in pGaN HEMTs in terms of gate leakage modeling. The knowledge and understanding of trap parameters are so vital for the device operation. Electron trapping leads to current collapse and threshold voltage instability in GaN HEMTs. While some work has been done in terms of surface passivation, surface plasma treatment, and design of field plates to mitigate these problems, there is still scope for a lot of improvements. TCAD can be useful tool in this regard in terms of device design as well as optimization of the process conditions to alleviate these challenges arising from traps.

APPENDIX A

A.1. MATLAB CODE FOR GATE LEAKAGE MODEL

```
clc;
clear all;
%Gate Current model:
syms Ig;
a=zeros;
b=zeros;
Vg_save=zeros;
Ig_save=zeros;
i=0;
for Vg=0:0.5:6
i=i+1;
n=1.0;
U=1.54;
Vt=0.026;
Is=1*10^-13;
Vd=n*Vt*log((Ig/Is)+1);
VpGaN=Vg-Vd;
Vbi=U;
L=VpGaN+Vbi;
Na=2*(10^25);
es=8.85*9.5*(10^-12);
q=1.6*(10^-19);
E=sqrt(2*q*Na*L/(es));
```

```
%FNT

A=1.54*(10^-6);

B=sqrt(0.8)*6.8*(10^9);

X1=B;

S=(A*(E^2))*(1/U);

D=(X1/E)*(U^1.5);

J=S*exp((-1)*D);

IFNT=(1.3*250*(10^-12))*J;

%TAT

m=0.8*9.1*(10^-31);

h1=6.62*(10^-34);

phit=0.1;

K=8*3.14*sqrt(2*q*m);

C=K/(3*h1);

W=C*(phit^(1.5));

R=W/E;

C1log=-5.8;

Ac=log(1.3*250*(10^-12));

O=C1log+Ac;

J=(O-R);

ITAT=exp(J);

Q=Ig-(IFNT+ITAT);

V=double(vpasolve(Q));

N=abs(V);

 a=N;

 Vg_save(i)=Vg;
```

```
Ig_save(i)=a;

disp(Vg)

disp(a)

end

plot (Vg_save,log10(Ig_save));
```

APPENDIX B

B.1. SDEVICE COMMAND TO SIMULATE IG

Electrode {

  {name= "source" voltage=0.0 EqOhmic}

  {name= "drain" voltage=0.0 EqOhmic}

  {name= "gate" voltage=0.0   Schottky Workfunction=5.12}

  {Name="body" Voltage=0}

}

File {

  Grid   = "GLdev12_msh.tdr"

  Parameter   = "GLdev12.par"

  Piezo   = "GLdev12_msh.tdr"

  Current   = "GLdev12_des.plt"

  Plot   = "GLdev12_des.tdr"

  Output   = "GLdev12_des.log"

}

Physics {

    DefaultParametersFromFile

```
   AreaFactor=250

      EffectiveIntrinsicDensity (Nobandgapnarrowing)

       Fermi

    Mobility (

    DopingDependence

    HighFieldSaturation

  )

Piezo (

   Strain=LoadFromFile

   )

   Temperature=298

   Hydrodynamic

    Recombination (

            SRH Radiative Avalanche

      )

Piezoelectric_Polarization(strain)

Aniso (

 Poisson
```

```
    direction (SimulationSystem)= yAxis

  )

eBarrierTunneling "sourceNLM"

  eBarrierTunneling "drainNLM"

  hBarrierTunneling "gateNLM"

}

Plot {

  BuiltinPotential

  EffectiveBandGap

  SemiconductorElectricField

  ElectricField/Vector

  eCurrent/Vector hCurrent/Vector

  DopingConcentration DonorConcentration AcceptorConcentration

  TotalTrapConcentration eTrappedCharge hTrappedCharge

  eDensity hDensity SpaceCharge

  Potential ConductionBandEnergy ValenceBandEnergy

  xMoleFraction

  #nSiliconPlusConcentration pSiliconMinusConcentration
```

```
  eBarrierTunneling hBarrierTunneling

 DonorPlusConcentration

}

Physics (Region="region_pGaN" ){

Traps (

        (Acceptor Level Conc= 2e17 EnergyMid= 0.5 FromValenceBand Add2TotalDoping

        hXSection= 1.5e-14 eXSection= 1.5e-14

            eBarrierTunneling(NonLocal= "gateNLM")

            TrapVolume= 1e-17 HuangRhys= 17 PhononEnergy= 0.01

            )

        )

}

Physics(Region="region_barrier" ){

 MoleFraction( xFraction= 0.15 Grading= 0)

}

Physics (RegionInterface="Nickel/region_pGaN") {GateCurrent(Fowler) }

Physics (RegionInterface="region_barrier/region_GaN") {

Piezoelectric_Polarization(Activation=0.8)
```

```
    Traps (

        (FixedCharge Conc=1e13)

    )

}

Physics (RegionInterface="region_barrier/region_pGaN"){

Piezoelectric_Polarization(Activation=0.8)

    Traps (

        (FixedCharge Conc=1e13)

    )

}

Math {

MetalConductivity

NonLocal "gateNLM" (

  Electrode="gate" Length= 8e-7 Digits= 4 EnergyResolution= 1e-3

)

 NonLocal "sourceNLM"(

  electrode="source" Length= 10e-7 Digits= 4 EnergyResolution= 1e-3

 )
```

```
  NonLocal "drainNLM" (

   electrode="drain" Length= 10e-7 Digits= 4 EnergyResolution= 1e-3

     )

}

Math {

 ExtendedPrecision

#if [string match -nocase @aniso@ yes]

 TensorGridAniso(Aniso)

 #endif

Method= Blocked

 SubMethod = ILS (set=11)

 ILSrc="

 set (11) {

  iterative(gmres(100), tolrel=1e-16, tolunprec=1e-8, tolabs=0, maxit=200);

  preconditioning (ilut(1.0e-15, -1),left);

  ordering (symmetric=nd, nonsymmetric=mpsilst );

  options( compact=yes, linscale=0, refineresidual=60, verbose=0);

 };
```

```
set(11){

  iterative(gmres(100), tolrel=1e-10, tolunprec=1e-4, tolabs=0, maxit=200);

  preconditioning(ilut(1.0e-9,-1), right);

  ordering(symmetric=nd, nonsymmetric=mpsilst);

  options(compact=yes, linscale=0, refineresidual=10, verbose=0);

};

"

-ExitOnUnknownParameterRegion

ComputeDopingConcentration

Number_of_Threads= 4

Digits=5

Iterations=20

Notdamped=30

Transient= BE

Traps (Damping=0.0)

DirectCurrent

ErrRef(electron) = 1e12

ErrRef(hole)  = 1e12
```

```
CDensityMin= 0

RefDens_eGradQuasiFermi_ElectricField= 1e8

RefDens_hGradQuasiFermi_ElectricField= 1e8

eMobilityAveraging= ElementEdge

hMobilityAveraging= ElementEdge

}

Solve {

*- Creating initial guess:

  Coupled (Iterations= 1000 LinesearchDamping= 1e-5) { Poisson }

  Coupled (Iterations= 1000 LinesearchDamping= 1e-5) {Poisson Electron Hole}

Plot (FilePrefix="Atzero_")

*- IdVg sweep:

NewCurrentPrefix="IgVg2_"

Transient (

              InitialTime= 0 FinalTime= 15

              InitialStep= 0.01 MinStep= 1.0e-4 Maxstep= 0.1

          Goal {Name= "gate" Voltage= 6}

      ) {
```

```
Coupled {Poisson Electron Hole}

Plot (FilePrefix="IgVg2" Time= (Range=(0 10) Intervals= 7) NoOverwrite)


      }

}
```

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